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ZT 8902

Single Board 486 Computer

HARDWARE MANUAL

For ZT 8902

Revision B

ZIATECH CORPORATION

ZT M8902
February 25, 1998
10240201



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WHAT'S IN THIS MANUAL?

This manual describes the operation and use of the ZT 8902 Single Board 486 Computer.

The following summarizes the focus of each chapter in this manual.

Chapter 1, "Introduction," introduces the key features of the ZT 8902. It includes a product definition, a list of product features, a functional block diagram, and a description of each block.

Chapter 2, "Getting Started," provides a summary of the information needed to install and configure your ZT 8902.

Chapter 3, "STD Bus Interface," presents a detailed description of the ZT 8902 interface to the STD-80 and STD 32 bus architectures. The topics discussed include compatibility, interrupt structure, and multiple master operation.

Chapter 4, "Interrupt Controller," describes the two Intel-compatible 8259 cascaded interrupt controllers. This chapter summarizes and illustrates the interrupt sources and the interrupt controllers' programmable registers.

Chapter 5, "Counter/Timers," discusses the six programmable counter/timers. It includes a diagram of the counter/timer architecture, a summary of operating modes, and descriptions of the programmable registers.

Chapter 6, "DMA Controller," provides an overview of ZT 8902 DMA architecture and DMA controller operation. Descriptions of DMA controller programmable registers are also included.

Chapter 7, "Real-Time Clock," lists the major features of the real-time clock and provides register descriptions.

Chapter 8, "Serial Controller," discusses operation of the two serial ports and provides register descriptions.

Chapter 9, "Centronics Printer Interface," contains descriptions of the programmable registers for the Centronics-compatible printer interface.

Chapter 10, "Parallel I/O," describes the functional blocks of the parallel I/O. It also provides register descriptions.

Chapter 11, "Watchdog Timer," explains operation of the watchdog timer and includes code for arming and strobing the timer.

Chapter 12, "System Registers," provides register descriptions and a brief overview of the three System registers used to control and monitor a variety of functions on the ZT 8902. Chapter 10 provides a more detailed discussion of the Ziatech 16C48 ASIC that implements the registers.

Chapter 13, "Local Bus Video," introduces the features of the local bus interface that gives high speed peripherals direct access to the CPU bus.

Chapter 14, "Programmable LED," provides code for turning the LED on and off.

Chapter 15, "AC Power Fail," explains AC power-fail detection.

Appendix A, "Jumper Configurations," describes the jumpers and cuttable traces on the ZT 8902. This appendix details factory default settings as well as information to tailor your board to a specific application.

Appendix B, "Specifications," contains the electrical, environmental, and mechanical specifications for the ZT 8902. This appendix also provides illustrations of cables and connector pinouts, and tables showing connector pin assignments.

Appendix C, "Parallel I/O Considerations," offers tips for system configuration to prevent latchup conditions.

Appendix D, "Customer Support," offers a product revision history, technical assistance and warranty information, and the necessary information should you need to return your ZT 8902 for repair.

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CHAPTER 1. INTRODUCTION

This chapter provides a brief introduction to the ZT 8902. It includes a product definition, a list of product features, a functional block diagram, and a description of each block. Unpacking information and installation instructions are found in Chapter 2, "Getting Started."

PRODUCT DEFINITION

The following topics cover ZT 8902 vs. ZT 89LT02 features, stand-alone operation, STD-80 vs. STD 32 single master architecture, and STD 32 multiple master architecture.

ZT 8902 vs. ZT 89LT02 Features

ZT 8902

The ZT 8902 is a highly integrated, single board computer that is factory configured to operate with a 25 MHz 486SX, 33 MHz 486SX, 33 MHz 486DX, 50 MHz 486DX2, 66 MHz DX2, or 100 MHz 486DX4 microprocessor. The board meets the needs of a wide range of industrial control and processing applications by operating stand alone, as a single master in an STD-80 or STD 32® architecture, or as a permanent or temporary master in an STD 32 architecture.

ZT 89LT02

The ZT 89LT02, a low temperature version with an extended operating range for harsh environments, is now available on a build-to-order basis. The ZT 8902 operating range of 0° to +65° C is extended in the ZT 89LT02 to -40° to +70° C. Contact Ziatech for details.

Except for the temperature variation, all other features of the ZT 89LT02 are the same as for the ZT 8902. Unless explicitly stated otherwise, all references in this manual to the ZT 8902 include the ZT 89LT02 as well.

Stand-Alone Operation

The ZT 8902 does not require an STD bus backplane to operate. The ZT 8902 is able to operate stand alone in many applications because of the large selection of the most commonly needed peripheral devices. Peripheral devices include:

- Flash file system for disk support
- Local bus expansion for keyboard and video support
- Parallel I/O
- Serial I/O
- Printer interface
- Speaker interface
- Interrupt controllers
- Counter/timers
- Watchdog timer
- Real-time clock

STD-80 or STD 32 Single Master Architecture

The ZT 8902 supports additional memory and I/O through the STD bus. In an STD-80 architecture, all 16-bit data transfers are automatically reduced to 8-bit transfers for complete backwards compatibility with STD-80 boards. In an STD 32 architecture, the data transfers are dynamically adjusted to support 8-bit and 16-bit boards.

STD 32 Multiple Master Architecture

Through jumper selection, the ZT 8902 is configured to operate in a multiple master architecture as a permanent master or a temporary master. With this architecture, up to seven ZT 8902 boards share STD bus memory and I/O resources.

FEATURES OF THE ZT 8902

- STD-80 and STD 32 bus compatible
- Occupies single STD bus slot
- Single and multiple master operation
- 25 to 100 MHz 486SX/DX/DX2/DX4 operation
- Numeric coprocessor support (486DX/DX2)
- 8 Kbytes of CPU cache
- 4, 8, or 16 Mbytes of DRAM memory
- 1, 2, or 4 Mbytes of Flash memory
- Optional 32-bit local bus video support
- Standard AT® peripherals include:
  - Two interrupt controllers (8259)
  - Three counter/timers (one 8254)
  - Real-time clock/CMOS RAM (146818)
  - Two DMA controllers (8237)
- Three additional counter/timers (second 8254)
- 24-point digital I/O (compatible with Opto 22 racks and Ziatech's ZT 2226 rack) with event sense capability
- Centronics printer port
- Two RS-232 serial ports
- Single stage watchdog timer
- Speaker interface
- Pushbutton reset
- Software programmable LED
- AC/DC power monitor
- Compatible with the following software: MS-DOS®, OS/2®, UNIX®, QNX®, VRTX32®, and Windows™ 3.1
- DOS and STAR BIOS options
- STD bus standard 4.5" x 6.5" board format
- +5 V-only operation (Flash memory programming requires +12 V)
- Burned in at 55° Celsius and tested to guarantee reliability
- Five-year warranty

DEVELOPMENT CONSIDERATIONS

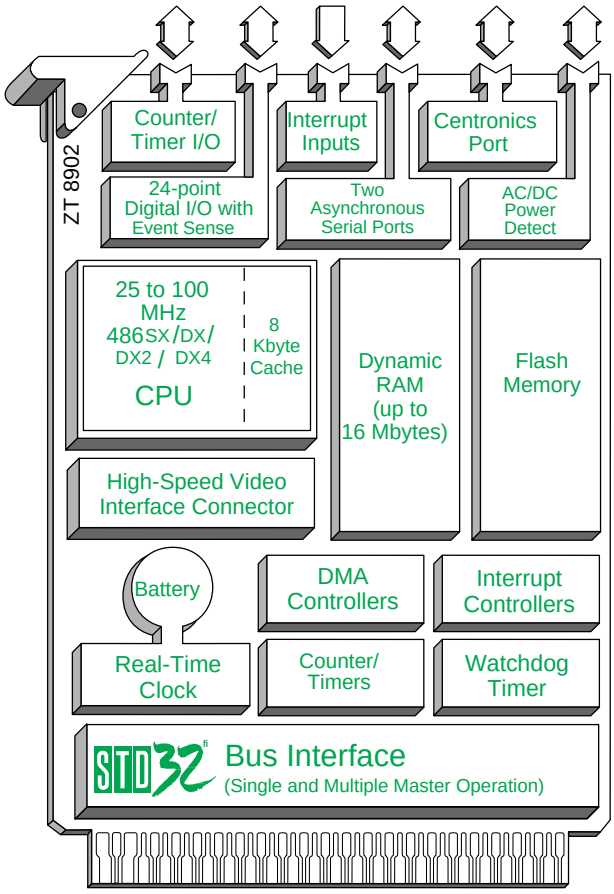
Ziatech offers two software development systems for ZT 8902 applications: DOS and the STD 32 STAR SYSTEM™.

DOS is Microsoft's MS-DOS residing on the ZT 8902. The DOS system provides a development platform similar to a PC, enabling applications to be developed quickly. DOS includes support for many of the ZT 8902 peripherals and is supported by a large number of development tools such as program editors, compilers, assemblers, and debuggers. Refer to the Ziatech system manual for configuration and operating instructions.

The STD 32 STAR SYSTEM is the DOS platform operating on more than one master in a single STD bus system. Each master includes local memory, local I/O, and the DOS operating system. Each master is capable of sharing STD bus memory and I/O, such as fixed disks, floppy disks, and video. Refer to the STAR SYSTEM operating manual for configuration and operating instructions.

FUNCTIONAL BLOCKS

The following figure illustrates a functional block diagram of the ZT 8902. An overview of each functional block follows.



Functional Block Diagram.

STD Bus Interface

The ZT 8902 operates in both STD-80 and STD 32 systems. In an STD-80 system, all data transfers between the ZT 8902 and STD bus memory or I/O boards are automatically reduced to 8 bits with 8 MHz timings.

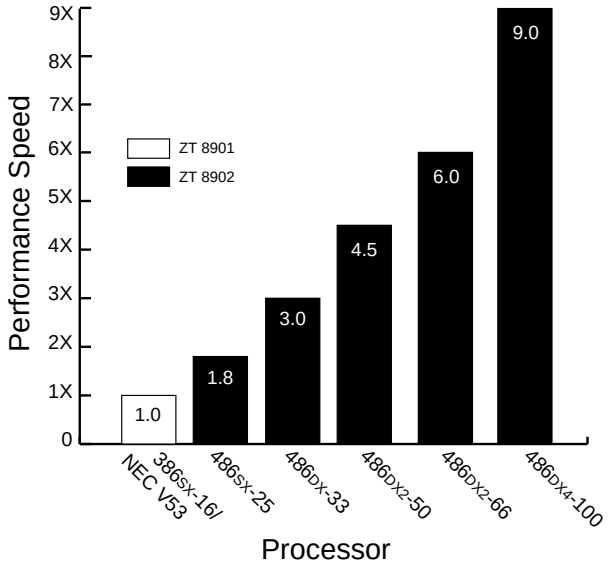
In an STD 32 system, data transfers are dynamically sized for either 8 bits or 16 bits. All STD-80 compatible memory and I/O boards are supported using 8-bit transfers. STD 32 compatible memory and I/O boards are dynamically sensed to determine the width of the data transfer. In addition to 16-bit data transfers, the STD 32 system provides the platform needed for multiple master operation. In a multiple master system, up to seven ZT 8902 boards share STD bus resources with a fixed or rotating priority granted by an external bus arbiter, such as the ZT 89CT39.

486SX/DX/DX2/DX4 Processors

The ZT 8902 supports the 486SX-25, 486SX-33, 486DX-33, 486DX2-50, 486DX2-66, and 486DX4-100 processors. The processors differ in operating speeds and hardware support of floating point operations. The 486SX-25 operates at 25 MHz and does not include floating point hardware. The 486SX-33 operates at 33 MHz and does not include floating point hardware. The 486DX-33 operates at 33 MHz and does include floating point hardware. The 486DX2-50 operates at 25 MHz externally and 50 MHz internally and includes floating point hardware. The 486DX2-66 operates at 33 MHz externally and 66 MHz internally and includes floating point hardware. The 486DX4-100 operates at 33 MHz externally and 100 MHz internally and includes floating point hardware.

Note: The 486DX4-100 is a 3.3 V processor. This reduces the energy needed by the CPU as well as the waste heat generated during operation. Special circuitry is loaded on the ZT 8902 to provide a highly efficient 3.3 V power source for the CPU.

The figure "Performance Comparison" illustrates relative processor performance.



Performance Comparison.
ZT 8902, ZT 8901 (V53), and 386SX.

Memory and I/O Addressing

The ZT 8902 includes two 64-pin SIMM sockets that support up to 16 Mbytes of DRAM. The ZT 8902 also supports Flash memory soldered directly on the board. Memory operations up to 16 Mbytes that are not decoded by local memory devices are directed to the STD bus. Data transfers are dynamically adjusted to support standard architecture boards with an 8-bit or 16-bit data path.

The ZT 8902 also includes many I/O peripherals required for industrial control applications. I/O operations up to 64 Kbytes not decoded by local I/O devices are directed to the STD bus. The STD bus I/O expansion signal, IOEXP, is supported to limit the addressing redundancy of I/O boards decoding fewer than 16 bits of address. Data transfers are dynamically adjusted to support standard architecture boards with an 8-bit or 16-bit data path.

Local Bus Video

The ZT 8902 supports both STD bus and local bus video adapters. For STD bus video, Ziatech offers video boards that support VGA and flat panel displays. For local bus video, Ziatech offers zVID adapters that plug directly onto the ZT 8902 J4 local bus connector. Local bus video is up to 700% faster than STD bus video because the data transfers occur at CPU speed (up to 33 MHz) and bus width (up to 32 bits). For space-constrained applications, the zVID offerings have the added advantage of not requiring the additional card cage slot needed by the STD bus offerings.

Serial I/O

Two PC-compatible serial ports are available. The serial ports are implemented with a 5 V charge pump technology to eliminate the need for a ±12 V supply. Both serial ports include a complete set of handshaking and modem control signals, maskable interrupt generation, and data transfer rates up to 115.2 Kbaud.

The serial ports are configured as DTE and are available through 10-pin frontplane connectors (J7 and J8). Optional cables interface the frontplane connectors to 9-pin D-shell connectors. A null-modem option is available to convert the DTE configuration to DCE. Adapter board options are also available to convert the RS-232 interface to an RS-485 interface.

Parallel I/O

The ZT 8902 includes three 8-bit parallel I/O ports for a total of 24 parallel I/O lines. Each line is programmable as an input or an output with readback. One of the three ports includes event sense capability where a positive or negative transition on the input will generate an onboard interrupt. All inputs also feature a programmable debounce circuit. The outputs sink 12 mA and do not glitch during power up or power down. The 24 lines are available through a 50-pin frontplane connector (J5). Optional cables interface the frontplane connector to an 8-, 16-, or 24-position I/O module mounting rack, such as Ziatech's ZT 2226 24-Channel I/O Mounting Rack or those offered by Opto 22.

Interrupts

Two interrupt controllers provide a total of 15 interrupt inputs. Interrupt controller features include support for level-triggered and edge-triggered inputs, fixed and rotating priorities, and individual input masking. Interrupt sources include counter/timers, serial I/O, real-time clock, keyboard, printer, and multiple master communications. There are also five frontplane and five backplane interrupt sources.

Counter/Timers

Six counter/timers are included on the ZT 8902. Operating modes supported by the counter/timers include interrupt on count, frequency divider, square wave generator, software triggered, hardware triggered, and one shot. Three of the counter/timers are dedicated to supporting local devices. Three additional counter/timers are available through a 10-pin frontplane connector (J6).

DMA

Two DMA controllers provide a total of three DMA channels for data transfers between system I/O and local memory. The DMA channels support STD bus DMA slaves by managing the data transfers between the slaves and local memory. The DMA channels also support STD bus masters by making local memory available to the masters during the data transfer. Additional features of the DMA channels include auto initialization, address increment or decrement, and software DMA requests.

One DMA channel is available through STD bus BUSRQ* and BUSAK*. This is an 8-bit DMA channel used primarily for floppy disk expansion. Two additional DMA channels are available through a 10-pin frontplane connector (J10). One frontplane channel is 8-bit DMA channel 0 or 16-bit DMA channel 5. The other frontplane channel is 8-bit channel 1 or 16-bit channel 6.

Watchdog Timer

The watchdog timer optionally monitors system operation. Failure to strobe the watchdog timer within a set time period results in a system reset.

Real-Time Clock

The real-time clock performs timekeeping functions and includes 50 bytes of general-purpose battery-backed CMOS RAM. Timekeeping features include an alarm function, a maskable periodic interrupt, and a 100-year calendar.

Keyboard Controller

The ZT 8902 includes a PC/AT® keyboard controller that operates when the zVID local bus video adapter is installed. The keyboard connector is located on the zVID adapter.

Printer Interface

The ZT 8902 includes a PC/AT printer interface for connection to a Centronics-compatible printer or a software key required by many application packages. The printer interface is available through a 20-pin frontplane connector. An optional cable is available to interface the frontplane connector to a software key or a printer (J2).

Speaker Interface

The ZT 8902 supports an external speaker through a 2-pin frontplane connector (J9).

AC Power-Fail Protection

With the addition of an AC transformer, the ZT 8902 monitors AC power to permit an orderly shutdown during a power failure. When AC power falls below an acceptable operating range, a non-maskable interrupt is generated to notify the CPU of an impending power failure. When the application software receives this notification, it saves critical data before the CPU is reset.

CHAPTER 2. GETTING STARTED

This chapter summarizes the information needed to make the ZT 8902 operational. Please read this chapter before attempting to use the board.

UNPACKING

Please check the shipping carton for damage. If the shipping carton and contents are damaged, notify the carrier and Ziatech for an insurance settlement. Retain the shipping carton and packing material for inspection by the carrier. Do not return any product to Ziatech without a Return Material Authorization (RMA) number. Appendix D explains the procedure for obtaining an RMA number from Ziatech.

WHAT'S IN THE BOX?

The items listed below are included with a ZT 8902 order. System level products, such as the DOS and STAR SYSTEM packages, include additional items not shown. If a system level product has been ordered, refer to the system manual for the packing list.

- ZT 8902 Single Board 486 Computer in anti-static bag
- On-Line Help disk for ZT 8902
- Optional paper version of user's manual in binder

Save the anti-static bag for storing or returning the ZT 8902.

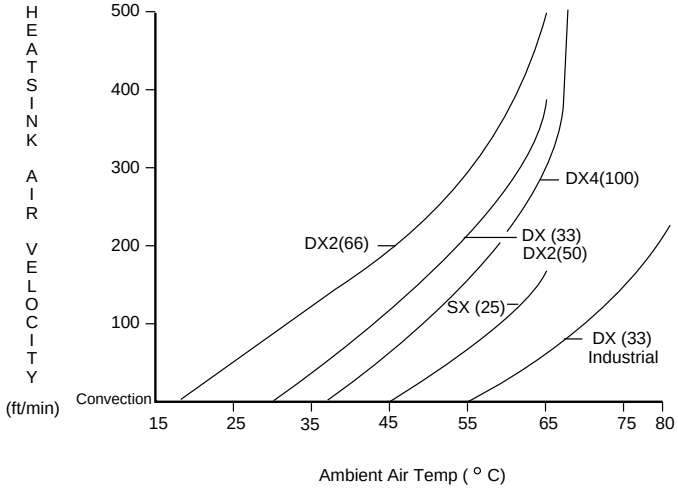
WARNING!

Like all equipment utilizing MOS devices, the ZT 8902 must be protected from static discharge. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the ZT 8902 to handle the board.

SYSTEM REQUIREMENTS

The ZT 8902 is designed for use with or without an STD bus backplane. The ZT 8902 is electrically, mechanically, and functionally compatible with both the STD-80 Series Bus Specification (ZT MSTD80) and the STD 32 Bus Specification (ZT MSTD32) for STD bus applications. An STD 32 system is required for 16-bit data transfers to other STD bus boards and for multiple master operation.

Ziatech recommends vertical mounting and the use of a fan to meet the airflow requirements shown in the "Airflow Requirements" figure. Refer to Appendix B, "Specifications," for additional specifications.



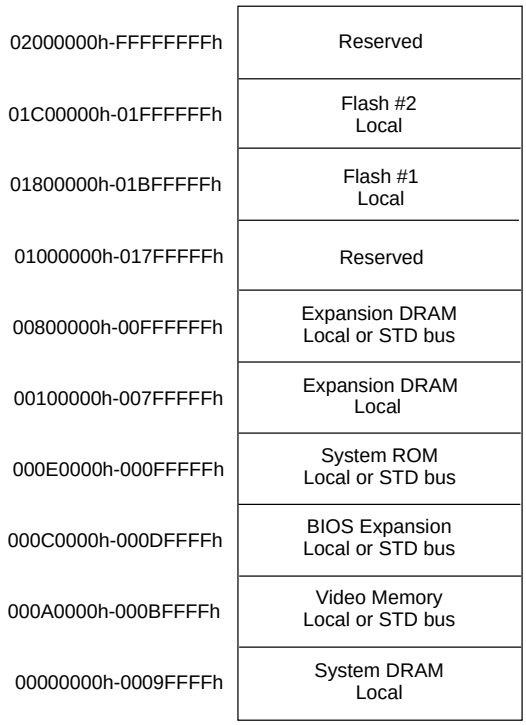
Airflow Requirements.

MEMORY CONFIGURATION

The ZT 8902 addresses up to 32 Mbytes of memory. The address space is divided between memory local to the board and memory on the STD bus. Any memory not reserved or occupied by a local memory device is available for STD bus expansion. During local memory operations, the STD bus is held static to decrease system electrical noise and power consumption.

STD bus memory is transferred at a rate of up to 1 Mbyte/second for 8-bit data and 2 Mbytes/second for 16-bit data. The ZT 8902 supports the STD bus wait request signal, WAITRQ*, to interface to memory boards with longer access time requirements than those defined by the STD-80 and STD 32 specifications.

The ZT 8902 is populated with several memory devices. Local DRAM is contained in one or two 64-pin SIMM sockets. Each SIMM socket supports 4 or 8 Mbytes of DRAM for a total of 16 Mbytes maximum. With current technology, up to 8 Mbytes is possible. Local Flash memory is soldered directly to the board. There is space for one or two Flash devices for a total of 8 Mbytes maximum. The memory address map is shown in the "Memory Address Map" illustration.



Memory Address Map.

I/O CONFIGURATION

The ZT 8902 addresses up to 64 Kbytes of I/O using a 16-bit I/O address. The address space is divided between I/O local to the board and I/O on the STD bus. Any I/O space not reserved or occupied by a local I/O device is available for STD bus expansion. During local I/O operations, the STD bus is held static to decrease system electrical noise and power consumption.

Local and STD bus I/O data is transferred at a rate of up to 1 Mbyte/second for 8-bit data and 2 Mbytes/second for 16-bit data. The ZT 8902 supports the STD bus wait request signal, WAITRQ*, to interface to I/O boards with longer access time requirements than those defined by the STD-80 and STD 32 specifications. The STD bus I/O expansion signal, IOEXP, is also supported. The IOEXP signal is automatically driven low over the I/O address range FC00h to FFFFh. Application software should use this address range to access STD bus I/O boards decoding IOEXP and fewer than 16 bits of address to prevent the board from being redundantly mapped throughout the 64 Kbyte I/O address space.

The ZT 8902 is populated with many of the most commonly used I/O peripheral devices for industrial control and computing applications. The I/O address location for each of the peripherals is shown in the "I/O Address Map" illustration.

0400h-FFFFh	STD Bus [1]
03F8h-03FFh	82C106 Serial #1
03E0h-03F7h	STD Bus
03AFh-03DFh	Video [2]
0380h-03AEh	STD Bus
0378h-037Fh	82C106 Printer
0300h-0377h	STD Bus
02F8h-02FFh	82C106 Serial #2 [3]
0100h-02F7h	STD Bus
00F2h-00FFh	Reserved [4]
00F1h	82C486 Math Coprocessor Reset
00F0h	82C486 Math Coprocessor Busy Clear
00ECh-00EFh	Reserved
00E8h-00EBh	8254 Counter/Timer
00E0h-00E7h	16C50A Parallel I/O, System Configuration
00C0h-00DFh	DMA Controller #2
00A0h-00BFh	82C486 Interrupt Controller #2
0090h-009Fh	Reserved [4]
0080h-008Fh	DMA Page Registers [6]
0072h-007Fh	Reserved [4]
0070h-0071h	82C106 Real Time Clock, 82C486 NMI Mask
0065h-006Fh	Reserved [4]
0064h	82C106 Keyboard Controller [5]
0061h-0063h	Reserved [4]
0060h	82C106 Keyboard Controller [5]
0044h-005Fh	Reserved [4]
0040h-0043h	82C486 Counter/Timer
0020h-003Fh	82C486 Interrupt Controller #1
0000h-001Fh	DMA Controller #1

Notes:
[1] STD bus IOEXP is active over the FC00h to FFFFh address range
[2] If local video is not installed, the address range is available on the STD bus
[3] If serial channel #2 is jumper disabled, the address range is available on the STD bus
[4] I/O operations to reserved address locations are not passed to the STD bus
[5] If the keyboard controller is jumper disabled, the address range is available on the STD bus
[6] I/O write operations over the 80h to 87h address range are passed to the STD bus for diagnostics

I/O Address Map.

FRONTPLANE CONNECTORS

The following table lists the assignments of frontplane connectors J1-J10. Refer to "Connectors" in Appendix B for an illustration showing connector locations and for information on pin assignments and cabling.

Frontplane Connector Assignments.

Connector	Function
J1	AC Power Fail
J2	Centronics Printer Interface
J3	Frontplane Interrupts
J4	Local Bus
J5	Parallel I/O
J6	Auxiliary Counter/Timer
J7, J8	RS-232 Serial Interface, COM2 and COM1
J9	Speaker Signals
J10	Frontplane DMA

JUMPER DESCRIPTIONS

The ZT 8902 includes several jumper options that tailor the operation of the board to specific application requirements. These options are summarized in Appendix A, "Jumper

CHAPTER 3. STD BUS INTERFACE

The ZT 8902 includes several I/O devices common to industrial control applications. The ZT 8902 also operates with the STD-80 and STD 32 bus architectures to support additional I/O and memory mapped devices as required by the application. This chapter discusses the STD-80 and STD 32 architectures and their effect on the operation of the ZT 8902.

STD-80 AND STD 32 OPERATION

The STD-80 Series Bus Specification, developed in the early 1980s by Ziatech Corporation, defines the electrical, mechanical, and functional characteristics of an STD bus system based on the 8088 series of microprocessors. Features of an STD-80 system include an 8-bit data bus, 24-bit address bus, and single bus master operation.

In the late 1980s, Ziatech developed the STD 32 Bus Specification as an extension to the STD-80 Bus Specification. Features of an STD 32 system include compatibility with STD-80 memory and I/O boards, expansion capabilities of up to a 32-bit data bus and a 32-bit address bus, and support for multiple bus master operation.

The following topics discuss STD-80 and STD 32 operation in greater detail.

STD-80 Operation

Data transfers between the ZT 8902 and any STD bus memory or I/O board occur eight bits at a time in an STD-80 system. The ZT 8902 automatically reduces 16-bit operations into two 8-bit transfers, so the application programmer is concerned only with the decrease in performance. In many applications, transfers between the ZT 8902 and STD bus resources are a small percentage of the overall operation and the performance degradation is minimal.

An STD-80 system supports only one ZT 8902.

STD 32 Operation

Data transfers between the ZT 8902 and any STD bus memory or I/O board occur eight bits at a time for boards supporting an 8-bit data bus and 16 bits at a time for boards supporting a 16-bit data bus in an STD 32 system. The ZT 8902 automatically determines the type of transfer at the start of each STD bus operation. If the application software includes a 16-bit operation with an 8-bit STD bus board, the ZT 8902 automatically reduces the transfer into two STD bus cycles. If the application software includes a 16-bit operation with a 16-bit STD bus board, the ZT 8902 performs the transfer in a single STD bus cycle.

As an example, consider the ZT 8902 and the ZT 8980 VGA and Keyboard Interface, both of which operate in STD-80 and STD 32 systems. In an STD-80 system, video RAM transfers between the two are over an 8-bit data path. If the application software performs a 16-bit video RAM read or write, the ZT 8902 automatically divides the 16-bit operation into two 8-bit transfers. In an STD 32 system, video RAM transfers between the ZT 8902 and the ZT 8980 are over a 16-bit data path. If the application software performs a 16-bit video RAM read or write, the ZT 8902 does the transfer in one STD bus operation.

In addition to 16-bit data transfer support, the STD 32 system has another advantage: it supports up to seven ZT 8902 boards in a single system. With the addition of an STD bus arbiter, such as the ZT 89CT39, multiple ZT 8902 boards have fixed or rotating priority access to STD bus memory and I/O resources. This architecture is useful for applications that can be divided into modular control blocks, with each module running on a unique ZT 8902.

STD-80 BUS COMPATIBILITY

The ZT 8902 is fully compatible with Revision 2.3 of the STD-80 Series Bus Specification (Ziatech part number ZT MSTD80). Optional STD-80 features supported by the ZT 8902 include:

- a 24-bit address bus
- four additional maskable interrupts
- dynamically driven I/O expansion
- external master support

The following topics discuss STD-80 address multiplexing, interrupts, I/O expansion, and external masters and DMA slaves.

Address Multiplexing

The STD-80 Series Bus Specification defines a multiplexing scheme to transfer address lines A16 through A19 across the lower half of the data bus during the start of each memory cycle. The ZT 8902 extends this concept by also transferring address lines A20 through A23 across the upper half of the data bus.

This feature is especially useful if all memory mapped STD bus boards used in the system decode 24 bits of address. If a memory mapped board decodes fewer than 24 bits, the board appears multiple times in the 24-bit memory map.

Interrupts

The STD-80 Series Bus Specification defines a single interrupt signal, INTRQ* (P44). If STD bus maskable interrupts are used in the application, the ZT 8902 is jumper configurable to receive INTRQ* and three optional interrupts: INTRQ1* (P37), INTRQ2* (P50), and INTRQ4* (P6). Refer to Chapter 4, "Interrupt Controller," for details. STD bus peripheral boards must be capable of generating an interrupt on INTRQ1*, INTRQ2*, and INTRQ4* to use this feature. Note that an additional interrupt, INTRQ3*, is available in the STD 32 architecture.

I/O Expansion

The STD-80 Series Bus Specification defines an I/O expansion signal, IOEXP, used to reduce addressing redundancy of an I/O board decoding fewer than 16 address lines. The ZT 8902 automatically drives this signal low when the application software performs an STD bus I/O address in the address range FC00h through FFFFh. To use this feature:

- The I/O mapped STD bus board is configured to respond to an active low IOEXP.
- The application software assigns the board to address FC00h plus the board configuration offset.

External Masters and DMA Slaves

The ZT 8902 does not support external masters in an STD-80 architecture; an STD 32 architecture is required for external master support. The ZT 8902 supports DMA slaves in both STD-80 and STD 32 architectures. The ZT 8902 includes a frontplane connector to support DMA slaves in an STD-80 architecture. The frontplane connector provides signals required by DMA slaves that are not defined on the STD-80 bus.

STD 32 BUS COMPATIBILITY

The ZT 8902 is compatible with Revision 1.2 of the STD 32 Bus Specification (Ziatech part number ZT MSTD32). Optional STD 32 features are discussed in terms of compliance levels.

Permanent Master: SA16, SA8-I, MB, SDMA8, SDMA16, SDMABP

Temporary Master: SA16, SA8-{MD}, I, SDMA8, SDMA16, SDMABP

Memory Slave: SA16

The following topic describes the compliance levels in more detail.

Compliance Levels

The following are brief descriptions of the STD 32 compliance levels supported by the ZT 8902.

SA8, SA16 Supports 8-bit and 16-bit data transfers with STD-80 signal format and timings. The ZT 8902 automatically determines the width of the data transfer at the start of each STD bus operation. STD-80 compatible memory and I/O boards are supported.

I Supports four additional STD bus interrupts: INTRQ1*, INTRQ2*, INTRQ3*, and INTRQ4*. These interrupts are input from the STD bus and connected to the interrupt controller through a jumper configuration block for increased flexibility. Refer to Chapter 4, 'Interrupt Controller," for a jumper configuration drawing.

MB Supports the bus exchange protocol (BUSRQ*/BUSAK*) for DMA slaves and bus masters. DMA slaves require ZT 8902 DMA channels to perform the data transfers from the DMA slave to local memory. Bus masters require the ZT 8902 DMA channels (programmed for cascade) to make local memory available for the master to perform the data transfer. The ZT 8902 monitors the STD bus MASTER16* signal to determine if the bus exchange signals are driven by a DMA slave or a bus master.

{MD} Supports the multiple master (DREQx*, DAKx*) protocol. These two signals are used by the ZT 8902 in a multiple master architecture to gain control of STD bus resources. The use of these signals requires a bus arbiter, such as the ZT 89CT39, to be plugged into slot X.

SDMA8, SDMA16 Supports 8-bit or 16-bit Standard Architecture DMA as defined in the STD 32 Bus Specification.

SDMABP Supports Standard Architecture DMA using BUSRQ*/BUSAK* for request and acknowledge and the backplane DMA control signals DMAIOR*, DMAIOW*, and T-C.

STD BUS INTERRUPTS

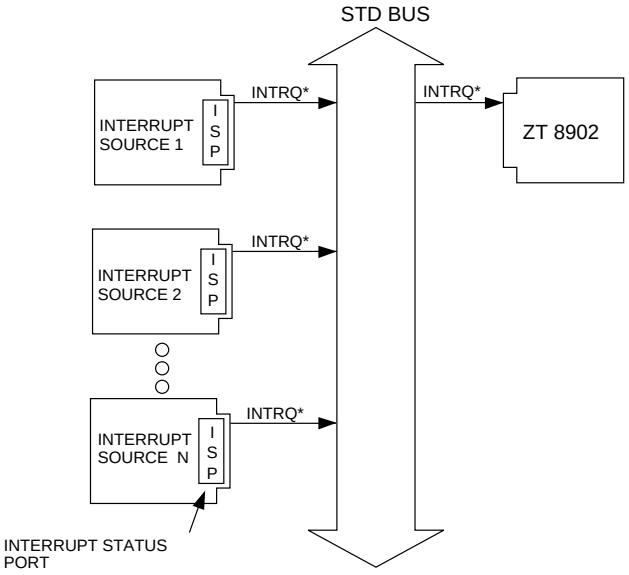
The ZT 8902 supports both maskable and non-maskable interrupts from the STD bus. This section discusses system level issues related to these interrupts. Refer to Chapter 4, "Interrupt Controller," for more information on the maskable interrupt controllers.

Maskable Interrupts

The STD bus maskable interrupts monitored by the ZT 8902 are INTRQ* (P44), INTRQ1* (P37), INTRQ2* (P50), INTRQ3* (E67), and INTRQ4* (P6). These maskable interrupts are routed to a jumper configuration block for added flexibility. Refer to Chapte 4, "Interrupt Controller," for details. Note that an STD 32 backplane is needed to use INTRQ3*.

The ZT 8902 is also capable of generating frontplane interrupts. This feature is useful in multiple master systems to coordinate communications between processors.

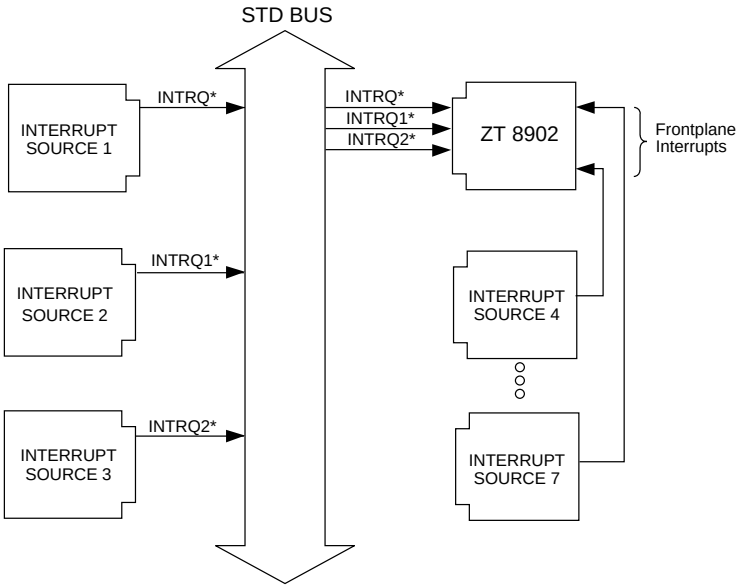
Some applications may find it necessary to share multiple interrupt sources on a single STD bus interrupt request, as shown in the "STD Bus Polled Interrupt Structure" figure. Since the interrupt controller provides a single vector for each input, it is up to the application software to poll each possible source on the shared interrupt request signal to determine which is requesting service. This procedure is fine for most applications, provided that each source can be polled and that the interrupt controller is programmed for level-triggered operation.



STD Bus Polled Interrupt Structure.

Some applications include edge-triggered interrupt sources. For example, the Ziatech DOS System uses edge-triggered interrupts to support the timer used to generate the periodic system tick. Since the interrupt controller inputs are not independently programmable for edge-triggered or level-triggered interrupts, all inputs for these applications must be treated as edge-triggered.

In an edge-triggered architecture, multiple interrupt sources should not share the same interrupt request signal because it is possible to miss an interrupt request from one source while an interrupt request from another source is being serviced. For this architecture, each interrupt source requires a unique connection to the interrupt controller, as shown in the "STD Bus Vectored Interrupt Structure" figure.



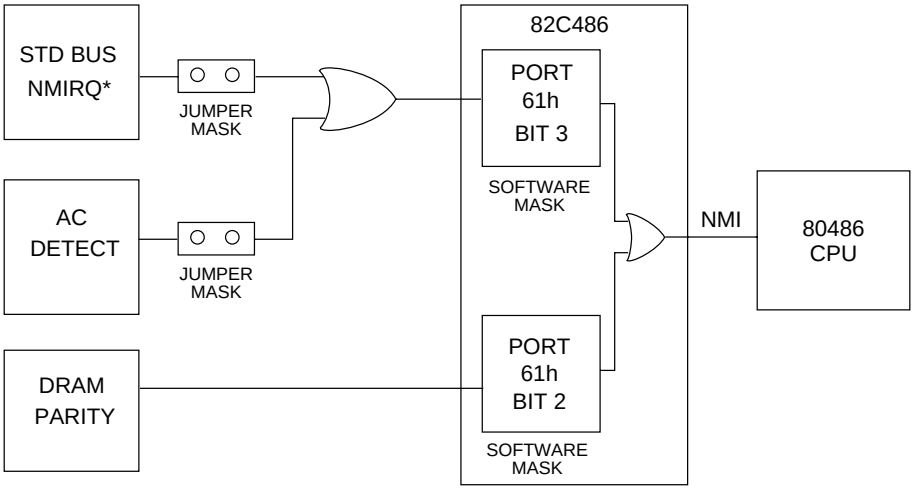
STD Bus Vectored Interrupt Structure.

Non-Maskable Interrupts

The ZT 8902 supports three sources of non-maskable interrupt requests (see the "Non-Maskable Interrupt Structure" illustration):

- STD bus NMIRQ* (P46)
- AC power-fail detection
- DRAM parity

The STD bus NMIRQ* and AC power-fail interrupts must be jumper enabled. All three interrupts are maskable through port 61h.



Non-Maskable Interrupt Structure.

RESET

The ZT 8902 is automatically reset with a precision voltage monitoring circuit that detects when Vcc is below the acceptable operating limit of 4.75 V. Other sources of reset include the watchdog timer, local pushbutton switch, and the STD bus pushbutton reset signal, PBRESET* (P48).

The ZT 8902 responds to any of these reset sources by initializing local peripherals and driving the STD bus system reset, SYSRESET* (P47). The ZT 8902 reset is typically active for 50 milliseconds.

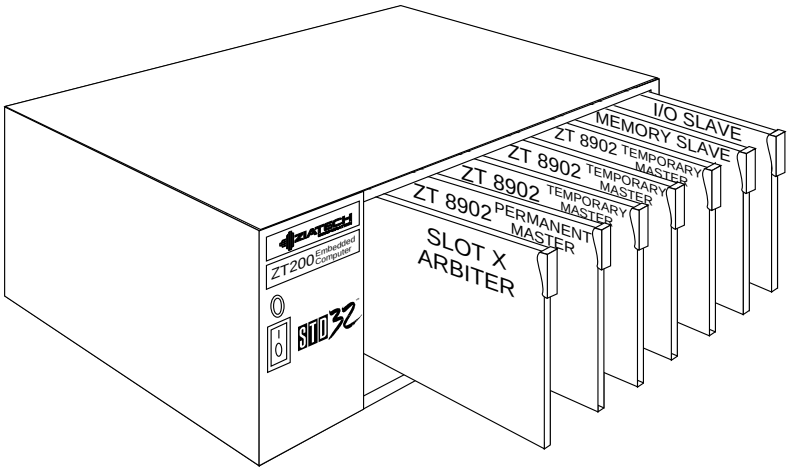
MULTIPLE MASTER AND INTELLIGENT I/O

Ziatech offers two architectures for increasing the number of microprocessors in a single system: multiple master and intelligent I/O. Applications can use multiple master, intelligent I/O, or a combination of the two. The following topics discuss the two architectures.

Multiple Master

A multiple master architecture requires one permanent master and one or more temporary masters, as illustrated in the "Multiple Master Architecture" figure. The ZT 8902 is jumper configurable (jumper W3) for either permanent or temporary master operation. Each master has complete access to STD bus resources and operates at full speed when the local CPU is communicating with local memory and I/O. It is not until the application software attempts an STD bus access that arbitration occurs.

The ZT 8902 responds to an STD bus access from the application software by generating an STD bus request, DREQx* (E16), to an external bus arbiter, such as the ZT 89CT39. The ZT 8902 then suspends all local operation until the bus arbiter returns an STD bus acknowledge, DAKx* (E15). All arbitration is done in hardware on the external bus arbiter board and is transparent to the application software. The amount of time required for this arbitration depends on the amount of time higher priority masters are in control of STD bus resources. A shared resource locking mechanism is supported to guarantee exclusive access to STD bus memory or I/O.



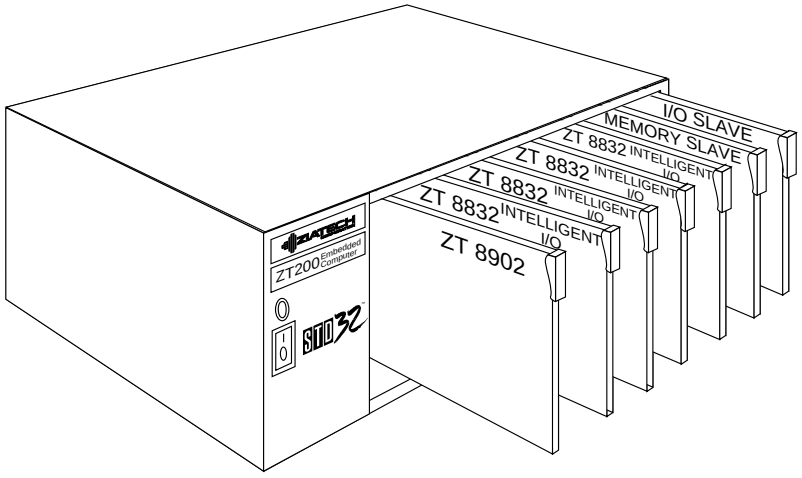
Multiple Master Architecture.

Intelligent I/O

An intelligent I/O system includes a single ZT 8902 and one or more intelligent I/O boards, such as the ZT 8832. This architecture is illustrated in the "Intelligent I/O Architecture" figure. The intelligent I/O board incorporates several I/O devices, a dual-port RAM for processor communications, and a CPU dedicated to controlling these devices.

Each intelligent I/O board operates at full speed when communicating with local memory, local I/O, and dual-port RAM. The ZT 8902 also operates at full STD bus speeds when accessing the dual-port RAM. It is not until the ZT 8902 and the intelligent I/O board access the dual-port RAM at the same time that arbitration occurs.

All arbitration is done in hardware local to each intelligent I/O board, eliminating the need for an external bus arbiter. The arbitration is transparent to the application software. The amount of time required for arbitration depends on the amount of time the device in control of the dual-port RAM requires to complete operation. A shared resource locking mechanism is supported to guarantee exclusive access to dual-port RAM by either the ZT 8902 or the intelligent I/O board.



Intelligent I/O Architecture.

Multiple Master Vs. Intelligent I/O

Both multiple master and intelligent I/O architectures are excellent methods of increasing system performance. The application designer has the freedom to select either architecture or combine both to meet the needs of the specific application. The following is a brief comparison of the multiple master and intelligent I/O architectures.

- An advantage of the multiple master system is that each ZT 8902 has complete access to all STD bus memory and I/O resources. In an intelligent I/O system, only one ZT 8902 has access to STD bus memory and I/O, including the dual-port RAM interface to each intelligent I/O board.
- An advantage of the intelligent I/O system is lower system cost. The intelligent I/O architecture operates in both STD-80 and STD 32 bus structures. Dual port RAM arbitration is local to each intelligent I/O board, eliminating the need for a system arbiter. Also, most multiple master implementations require an STD bus memory slave for communications between the masters. With an intelligent I/O architecture, all communications between the single master and the intelligent I/O boards are through the dual-port RAM local to each intelligent I/O board.

System Requirements, Multiple Master

The following is a list of considerations for the ZT 8902 operating in a multiple master architecture.

- One ZT 8902 must be configured as a permanent master, or there must be another permanent master in the system. The permanent master is responsible for managing the STD bus clock, CLOCK* (P49), and the system reset, SYSRESET* (P47). The remaining ZT 8902 boards must be jumpered for temporary master operation. In addition to jumper modifications, there are two socketed resistor packs, SIP6 and SIP9, that must be installed on the permanent master and removed from all temporary masters. These resistor packs are located between the DRAM memory modules and the STD 32 connector.
- An STD 32 backplane is required. An STD-80 backplane does not support the bus exchange protocol (DREQx* and DAKx*).
- A ZT 89CT39, or equivalent bus arbiter, is needed to manage ZT 8902 access to the STD bus resources. The arbitration may also be built directly on to the permanent master.

Reset, Multiple Master System

The ZT 8902 configured for single master operation is automatically reset with a precision voltage monitoring circuit, watchdog timer, local pushbutton reset, and the STD bus pushbutton reset signal, PBRESET* (P48). In response to any of these signals, the ZT 8902 initializes local peripherals and activates the STD bus system reset, SYSRESET* (P47).

In a multiple master system, a ZT 8902 configured as a permanent master operates the same as a ZT 8902 operating in a single master architecture. A ZT 8902 configured as a temporary master manages reset differently. A temporary master does not monitor PBRESET* and does not generate SYSRESET*. Instead, a temporary master ignores PBRESET* and monitors SYSRESET*. This enables the temporary masters to be reset when the permanent master generates SYSRESET*. This also enables the pushbutton reset on the temporary master to reset only the temporary master while the pushbutton on the permanent master resets the entire system.

CHAPTER 4. INTERRUPT CONTROLLER

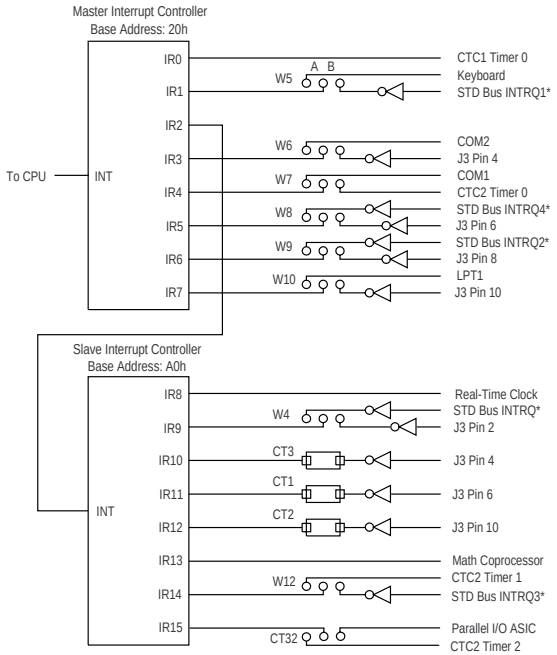
This chapter describes the two Intel-compatible 8259 cascaded interrupt controllers. It summarizes and illustrates the interrupt sources and the interrupt controllers' programmable registers.

ZT 8902 SPECIFICS

The ZT 8902 includes two Intel-compatible 8259 cascaded interrupt controllers that provide a programmable interface between interrupt-generating peripherals and the CPU. The interrupt controllers monitor 15 interrupts with programmable priority. When peripherals request service, the interrupt controller interrupts the CPU with a pointer to a service routine for the highest priority device. The major features of the interrupt architecture are listed below. The ZT 8902 does not support cascaded interrupt controllers on the STD bus.

- 15 individually maskable interrupts
- Level-triggered or edge-triggered recognition
- Fixed or rotating priorities

The interrupt architecture is illustrated in the "Interrupt Architecture" figure. Interrupt configuration jumpers are used to customize the interrupt architecture to the needs of the application. These jumpers connect one of two interrupt sources to an interrupt input. Wire-wrap techniques provide additional flexibility.



Interrupt Architecture.

The interrupt sources are summarized below.

Backplane: There are five STD bus interrupts routed to the interrupt configuration jumpers. These interrupts are labeled INTRQ*, INTRQ1*, INTRQ2*, INTRQ3*, and INTRQ4*. All five interrupts are supported in an STD 32 backplane and all but INTRQ3* are supported in an STD-80 backplane. These interrupts are active-low on the STD bus and inverted before they reach the interrupt configuration jumpers.

Frontplane: There are five frontplane interrupts routed to the configuration jumpers. These interrupts are available through connector J3 as active-low inputs that are inverted before reaching the interrupt configuration jumpers. The pin assignments for connector J3 are given in Appendix B, "Specifications." Many STD bus boards include a J3-compatible connector for routing interrupts to the ZT 8902 through a ribbon cable. This architecture is useful if the application requires more interrupts than are available on the STD bus.

Local: Local interrupt sources include counter/timers (CTC1 and CTC2), serial ports (COM1 and COM2), parallel port (LPT1), keyboard, math coprocessor, and real-time clock.

PROGRAMMABLE REGISTERS

Each interrupt controller includes four initialization registers, three control registers, and three status registers. The I/O port addressing for the interrupt controllers is given in the "Interrupt Controller Register Addressing" table. The base address of the master interrupt controller is 20h and the base address of the slave interrupt controller is A0h.

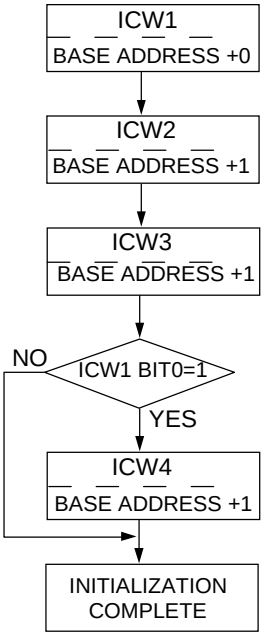
Interrupt Controller Register Addressing.

Address	Register	Operation
Base+0h	IRR, ISR, IPR	Read
Base+0h	ICW1	Write
Base+0h	OCW2, OCW3	Write
Base+1h	OCW1	Read/Write
Base+1h	ICW2, ICW3, ICW4	Write

Initialization Registers (ICW1-ICW4)

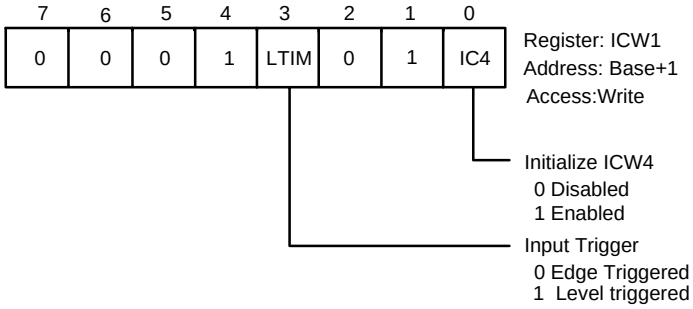
Each interrupt controller must be initialized before it is used. Initialization consists of writing two, three, or four initialization commands. The programming sequence for these registers is given in the "Interrupt Initialization Programming" figure. ICW1, ICW2, and ICW3 must be programmed during each initialization sequence. ICW4 may or may not be programmed, as required by the application.

The following topics show the initialization registers ICW1-ICW4.



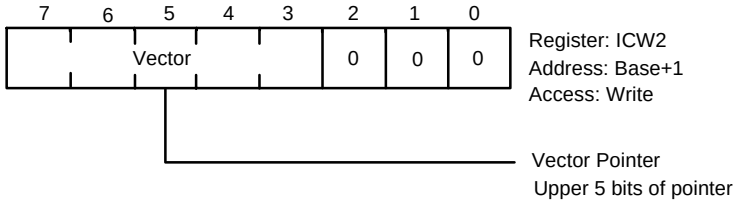
Interrupt Initialization Programming.

Initialization Register ICW1



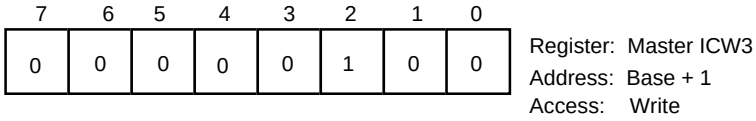
Initialization Register ICW1.

Initialization Register ICW2

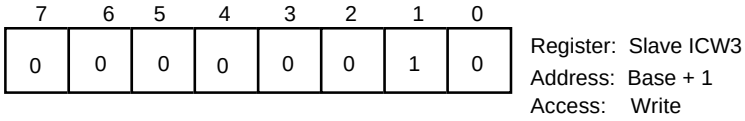


Initialization Register ICW2.

Initialization Register ICW3, Master and Slave

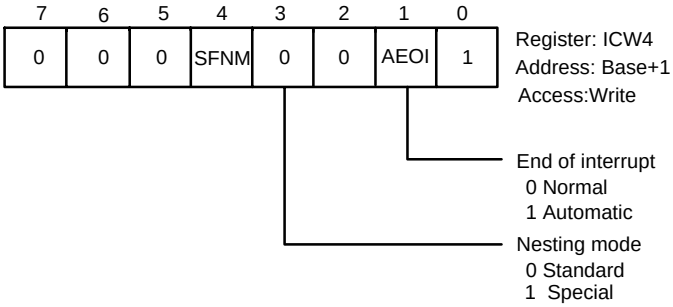


Master Initialization Register ICW3.



Slave Initialization Register ICW3.

Initialization Register ICW4



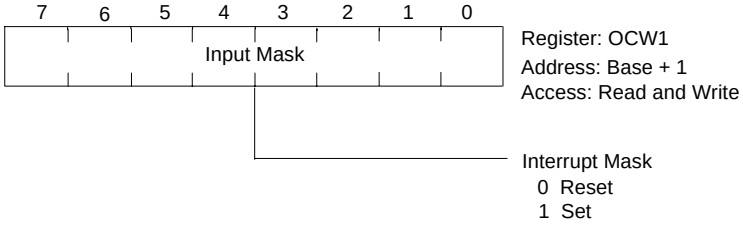
Initialization Register ICW4.

Operational Registers (OCW1-OCW3)

The operation of each interrupt controller is managed by three 8-bit operational registers. These registers are programmed in any sequence for things such as enabling and disabling interrupt requests and changing interrupt priorities.

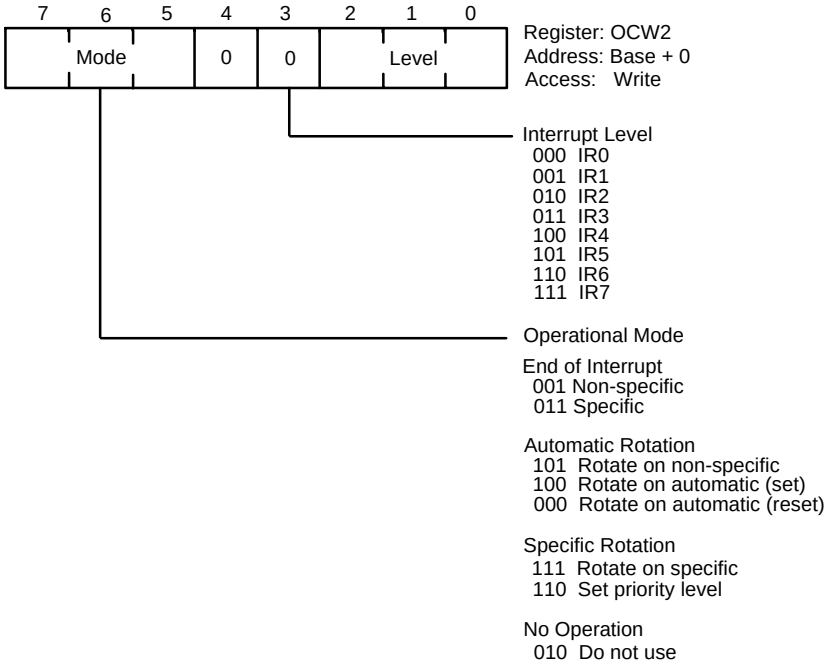
The following topics show the operational registers OCW1-OCW3.

Operational Register OCW1



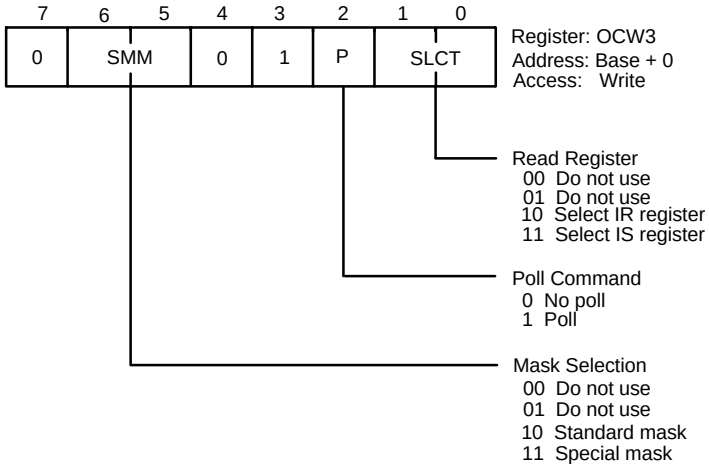
Operational Register OCW1.

Operational Register OCW2



Operational Register OCW2.

Operational Register OCW3



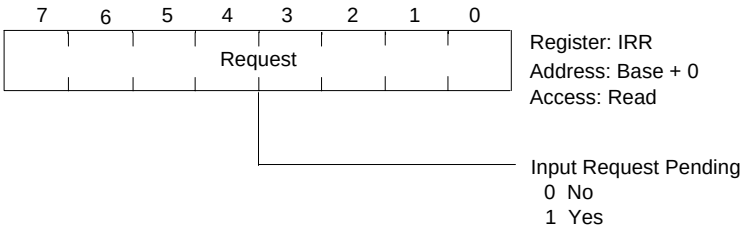
Operational Register OCW3.

Status Registers (IRR, ISR, IPR)

Each interrupt controller includes three status registers. A status register is selected by programming the first three bits of OCW3.

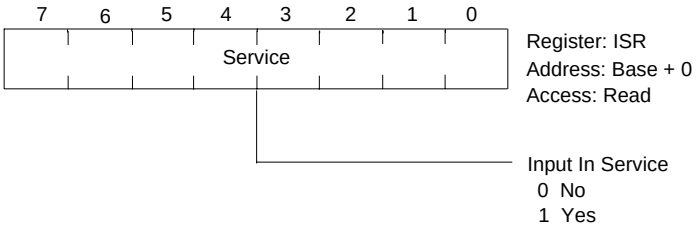
The following topics show the status registers IRR, ISR, and IPR.

Status Register IRR



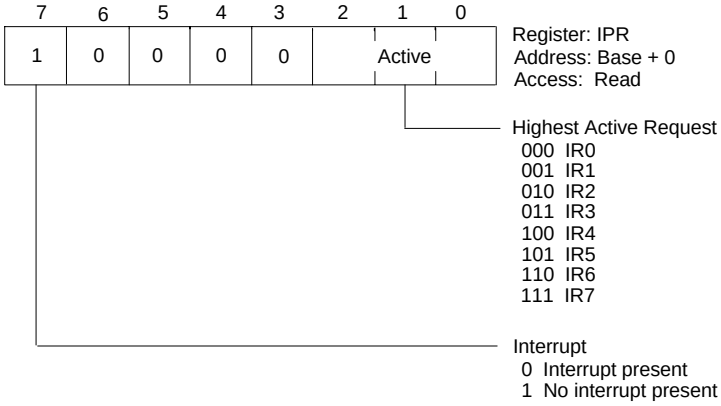
Status Register IRR.

Status Register ISR



Status Register ISR.

Status Register IPR



Status Register IPR.

ADDITIONAL INFORMATION

Refer to the Ziatech Industrial Computer System Manual for more information on the operating system's use of the interrupt inputs. Refer to the VLSI VL82C486 data book for more information on the interrupt controller operating modes.

CHAPTER 5. COUNTER/TIMERS

This chapter discusses the six programmable counter/timers. It includes a diagram of the counter/timer architecture, a summary of operating modes, and descriptions of the programmable registers.

ZT 8902 SPECIFICS

The ZT 8902 includes two Intel-compatible 8254 devices for a total of six programmable counter/timers. The counter/timers are useful for generating timing loops, timed and periodic interrupts, and for counting external asynchronous events. The major features of the counter/timers are listed below.

- Six 16-bit counter/timers
- Six programmable operating modes
- Binary and BCD counting
- Interrupt and polled operation

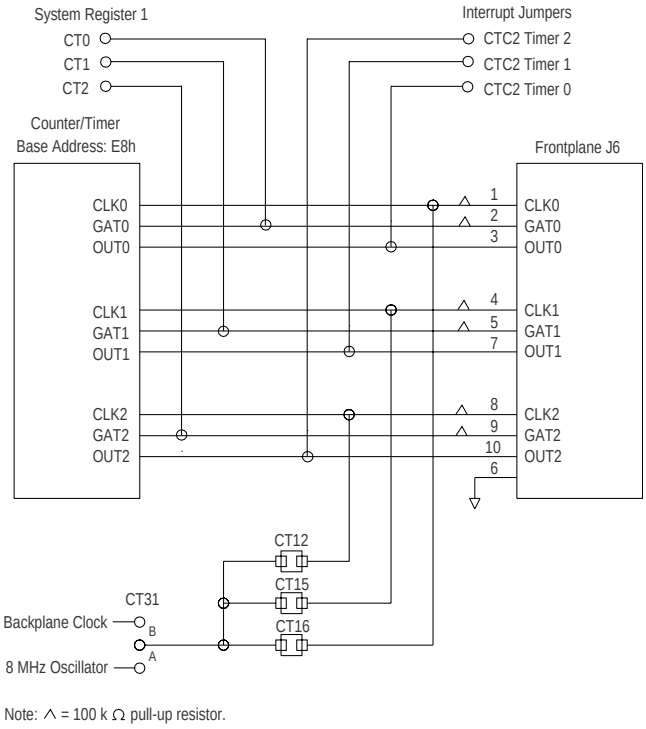
The six programmable operating modes are summarized in the "Counter/Timer Operating Modes" table.

Counter/Timer Operating Modes.

Mode	Counter/Timer Output Operation
0	Transitions after programmed count expires Gate enables and disables counting
1	Transitions after programmed count expires Gate triggers and retriggers counting
2	Periodic single pulse after programmed count expires Gate restarts counting
3	Square wave with frequency equal to programmed count Gate enables and disables counting
4	Single pulse after programmed count expires Gate enables and disables counting
5	Single pulse after programmed count expires Gate triggers and retriggers counting

Three of the six counter/timers are dedicated for use by the system software and three are available for use by the application. The architecture of the available counter/timers is illustrated in the "Counter/Timer Architecture" figure. See Appendix B, "Specifications," for connector J6 pin assignments. The clock source for the three available counter/timers is selectable between the backplane clock, a local 8 MHz oscillator, or the J6 frontplane connector. If a frontplane clock is used, it must meet the following specifications:

- Operating frequency between DC and 8 MHz
- Rise and fall times of less than 25 ns
- Clock low and clock high times of greater than 50 ns



Counter/Timer Architecture.

PROGRAMMABLE REGISTERS

The counter/timers are accessed through four I/O addresses, as shown in the "Counter/Timer Register Addressing" table. Each counter/timer occupies an I/O port address through which the preset count values are written and both the count and status information is read. The control register occupies the remaining I/O port address, which services all three counter/timers.

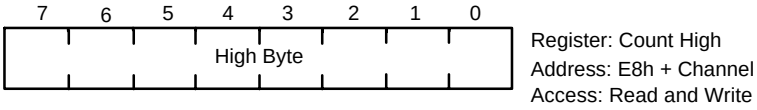
The topics that follow discuss the individual registers.

Counter/Timer Register Addressing.

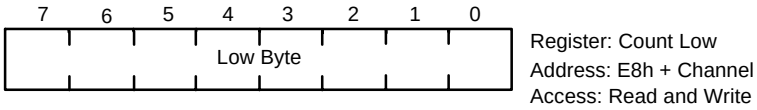
Address	Register	Operation
00E8h	Channel 0 Count	Read/Write
00E8h	Channel 0 Status	Read
00E9h	Channel 1 Count	Read/Write
00E9h	Channel 1 Status	Read
00EAh	Channel 2 Count	Read/Write
00EAh	Channel 2 Status	Read
00EBh	Control	Write

Count Registers and Count Latch

Each counter/timer has a 16-bit count register and count latch. Data is transferred to the counter/timers through the count register and from the counter/timers through the count latch. The control register defines the method for accessing the 16-bit count register through an 8-bit I/O port.



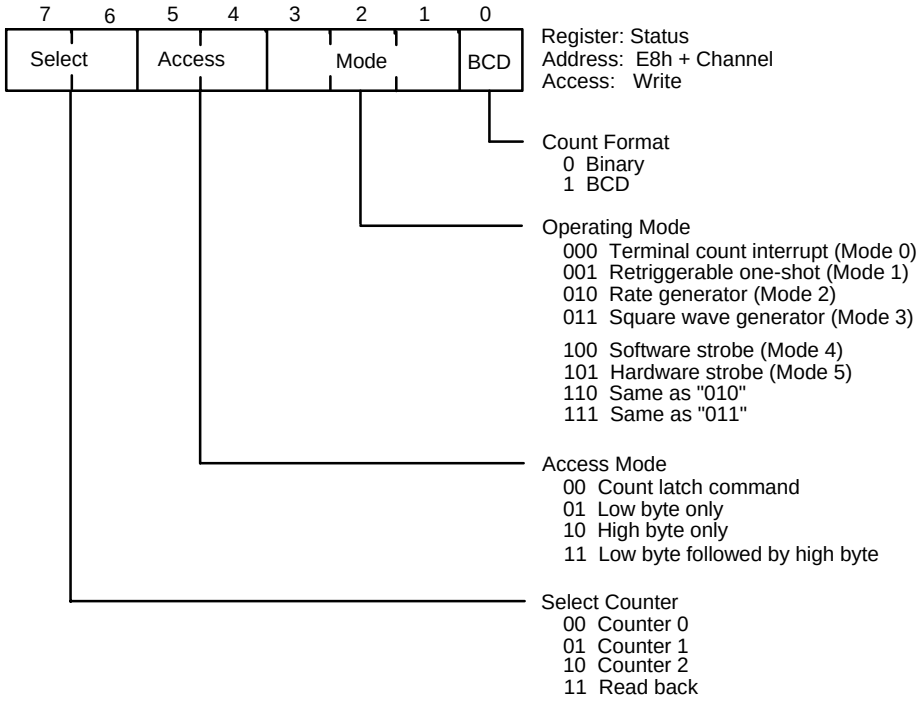
Count Register High Byte.



Count Register Low Byte.

Status Registers

Each counter/timer has a status register. The status register must be read using the multiple latch command specified in the control register.

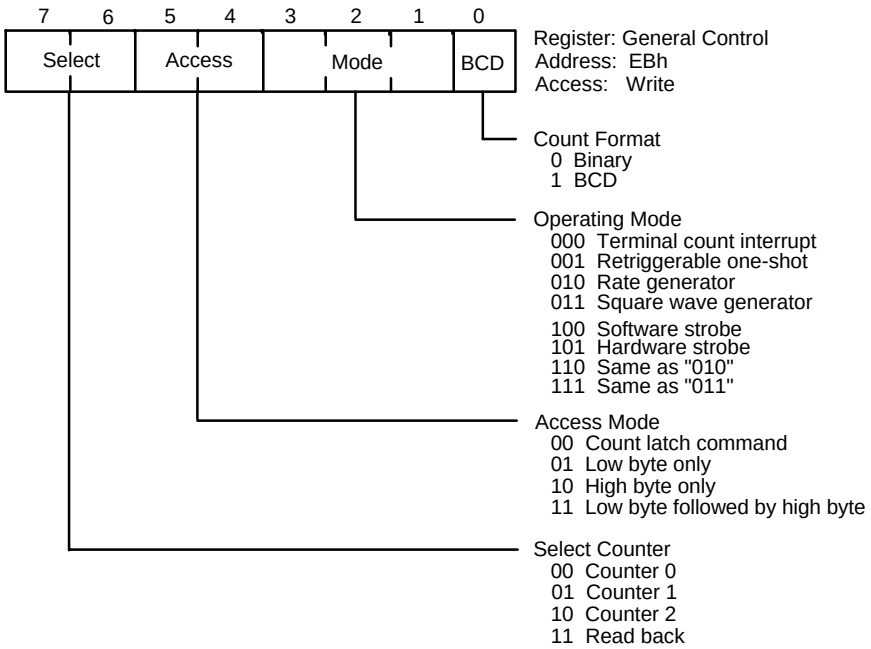


Status Register.

Control Register

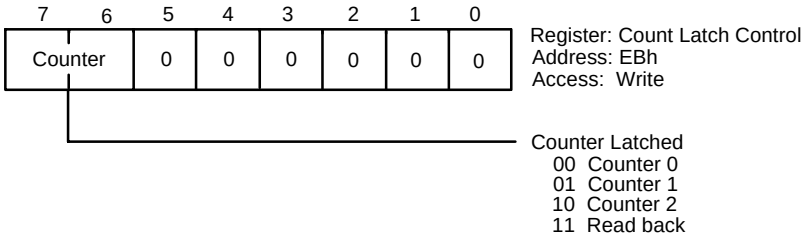
The control register is used to initialize the counter/timers and to select the method of reading the count and status information. The control register is best described by dividing it into three formats: the general control register, count latch control register, and multiple latch control register. The following topics provide illustrations of the three formats.

General Control Register



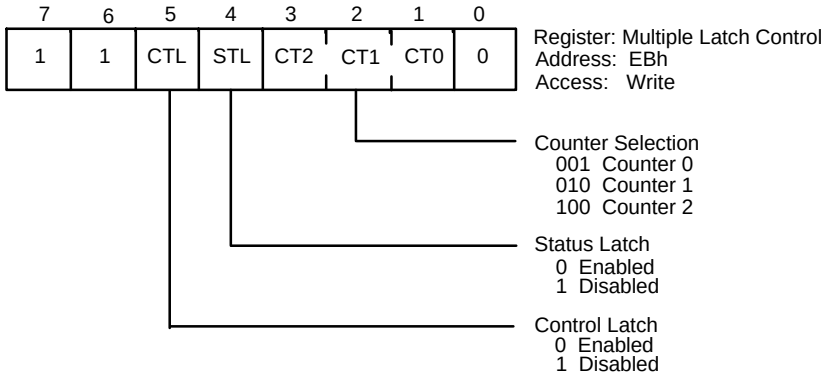
General Control Register.

Count Latch Control Register



Count Latch Control Register.

Multiple Latch Control Register



Multiple Latch Control Register.

ADDITIONAL INFORMATION

Refer to the Ziatech Industrial Computer System Manual for more information on the operating system's use of the counter/timers. Refer to the VLSI VL82C486 data book for more information on the counter/timer operating modes.

CHAPTER 6. DMA CONTROLLER

This chapter provides an overview of ZT 8902 DMA architecture and DMA controller operation. Descriptions of DMA controller programmable registers are also included.

ZT 8902 SPECIFICS

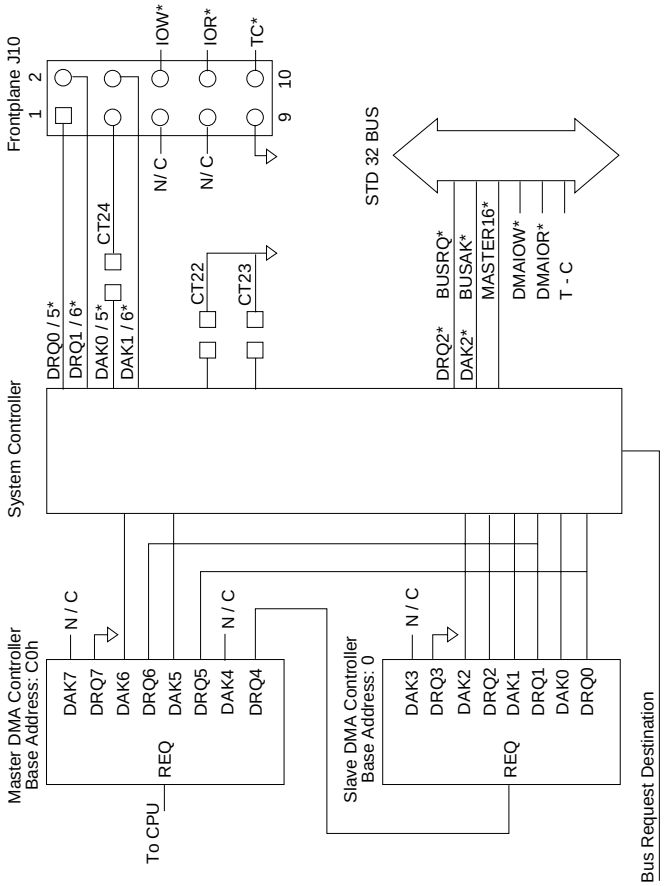
The ZT 8902 includes two Intel-compatible 8237 cascaded DMA controllers to support STD bus DMA slaves and STD bus masters. STD bus DMA slaves are I/O devices that use a ZT 8902 DMA channel to transfer data to or from ZT 8902 memory. STD bus masters are bus cycle generating devices that use a ZT 8902 DMA channel programmed for cascade mode to gain access to ZT 8902 memory. The major features of the DMA architecture are listed below.

- One STD bus DMA channel
- Two frontplane DMA channels
- DMA slave and bus master support
- Independent autoinitialization
- Address increment and decrement
- Single, block, and demand transfers
- DMA transfers over the full local memory range
- Block DMA transfer rates of greater than 2 Mbytes/sec

The DMA architecture is illustrated in the "DMA Architecture" figure on the following page. The architecture includes a slave DMA controller and a master DMA controller. The slave DMA controller includes DMA channels 0 through 3. These channels are dedicated to 8-bit DMA transfers. The master DMA controller includes DMA channels 4 through 7. These channels are dedicated to 16-bit DMA transfers.

A total of three DMA channels are supported. One channel is available through the STD bus and two additional channels are available through a frontplane connector (J10). The STD bus channel is connected to 8-bit DMA channel 2. This channel is required by STD bus floppy disk controllers.

The two frontplane channels are independently selectable for 8-bit or 16-bit operation using cuttable traces CT22 and CT23. One frontplane channel supports DMA channel 0 or 5 and the other frontplane channel supports DMA channel 1 or 6. You must be sure to mask the channels that are not required by the application. Refer to the "Cuttable Trace Descriptions" section in Appendix A, "Jumper Configurations," for a detailed description of the cuttable traces.



DMA Architecture.

OPERATING MODES

All three DMA channels support the following four operating modes:

Single Mode — The DMA controller executes a single transfer for each DMA cycle. The count is adjusted by one for each transfer. A terminal count is generated when the count changes between 0 and FFFFh.

Block Mode — The DMA controller executes repetitive transfers for each DMA cycle. The count is adjusted by one for each transfer. A terminal count is generated when the count changes between 0 and FFFFh. The transfers end on the assertion of terminal count.

Demand Mode — The DMA controller executes repetitive transfers for each DMA cycle. The count is adjusted by one for each transfer. A terminal count is generated when the count changes between 0 and FFFFh. The transfers end on the assertion of terminal count or the removal of DMA request.

Cascade Mode — The DMA controller supports DMA slaves with single, block, and demand transfers. The DMA controller supports bus masters with cascade operation. A DMA channel programmed for cascade operation gains control of local resources and converts the ZT 8902 into a memory slave. Examples or DMA slave and bus master transfers are presented in the following topics.

DMA Slave Operation

1. The DMA slave generates an STD bus BUSRQ* or a frontplane DMA request.
2. The system controller gains control of STD bus resources (multiple master only). The system controller is hardware local to the ZT 8902 that manages the STD bus interface.
3. The system controller generates a DMA request to the DMA controller if the bus request destination bit is active. In a single master system, this bit is held active. In a multiple master system, this bit is software controlled to direct the DMA request to a single destination. The bus request destination bit is located in bit 6 of system register 3. (Refer to Chapter 12, "System Registers.")
4. The DMA controller (programmed to perform a DMA transfer) gains control of local resources and generates a DMA acknowledge to the system controller.
5. The system controller generates an STD bus BUSAK* or a frontplane DMA acknowledge.
6. The DMA controller generates an STD bus or frontplane I/O strobe and a local memory cycle to complete the data transfer.

Bus Master Operation

1. The bus master generates an STD bus BUSRQ* or a frontplane DMA request.
2. The system controller gains control of STD bus resources (multiple master only). The system controller is hardware local to the ZT 8902 that manages the STD bus interface.
3. The system controller generates a DMA request to the DMA controller if the bus request destination bit is active. In a single master system, this bit is held active. In a multiple master system, this bit is software controlled to direct the DMA request to a single destination. The bus request destination bit is located in bit 6 of system register 3. (Refer to Chapter 12, "System Registers.")
4. The DMA controller (programmed for cascade operation) gains control of local resources and generates a DMA acknowledge to the system controller.
5. The system controller generates an STD bus BUSAK* or a frontplane DMA acknowledge.
6. The bus master generates an STD bus MASTER16*.
7. The system controller converts the ZT 8902 into a memory slave to permit the bus master access to local memory.
8. The bus master generates the STD bus memory cycle to complete the data transfer.

PROGRAMMABLE REGISTERS

Each DMA controller is managed through the 16 I/O port addresses shown in the "Slave DMA I/O Port Addressing" table on the following page. Page registers extend the 16-bit DMA address to the full 24-bit address space available on the ZT 8902. I/O port addressing for the DMA page registers is given in the "DMA Page I/O Port Addressing" table on the following page.

The topics that follow illustrate the DMA controller programmable registers.

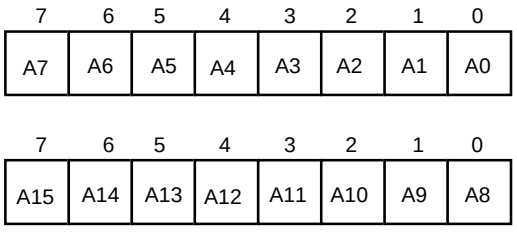
Slave DMA I/O Port Addressing.

Address Slave	Address Master	Register	Operation
0	C0	Channel 0 Base/Current Address	Write
		Channel 0 Current Address	Read
1	C2	Channel 0 Base/Current Count	Write
		Channel 0 Current Count	Read
2	C4	Channel 1 Base/Current Address	Write
		Channel 1 Current Address	Read
3	C6	Channel 1 Base/Current Count	Write
		Channel 1 Current Count	Read
4	C8	Channel 2 Base/Current Address	Write
		Channel 2 Current Address	Read
5	CA	Channel 2 Base/Current Count	Write
		Channel 2 Current Count	Read
6	CC	Channel 3 Base/Current Address	Write
		Channel 3 Current Address	Read
7	CE	Channel 3 Base/Current Count	Write
		Channel 3 Current Count	Read
8	D0	Status	Read
		Command	Write
9	D2	Write Request	Write
A	D4	Write Single Mask	Write
B	D6	Write Mode	Write
C	D8	Clear Byte Pointer	Write
D	DA	Clear Master	Write
E	DC	Clear Mask	Write
F	DE	Write Mask	Write

DMA Page I/O Port Addressing.

Address	Register	Operation
87	Channel 0 A16-23 Address	Read/Write
83	Channel 1 A16-23 Address	Read/Write
81	Channel 2 A16-23 Address	Read/Write
8B	Channel 5 A16-23 Address	Read/Write
89	Channel 6 A16-23 Address	Read/Write

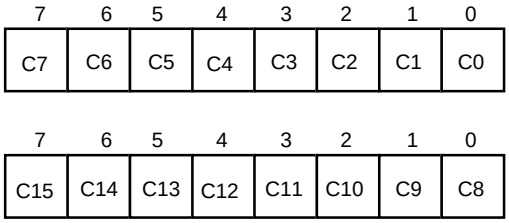
Address Register



Register: Address
Address: See "Slave DMA I/O Port Addressing" Table
Access: Read and Write

Address Register.

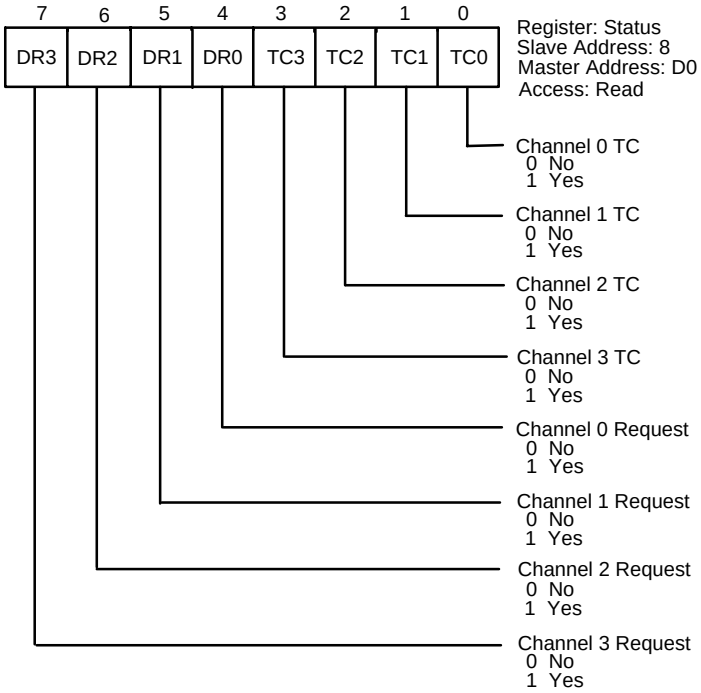
Count Register



Register: Count
Address: See "Slave DMA I/O Port Addressing" Table
Access: Read and Write

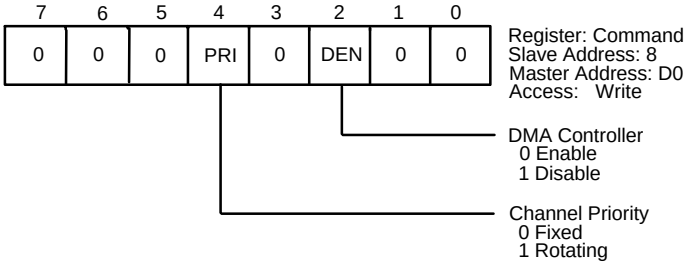
Count Register.

Status Register



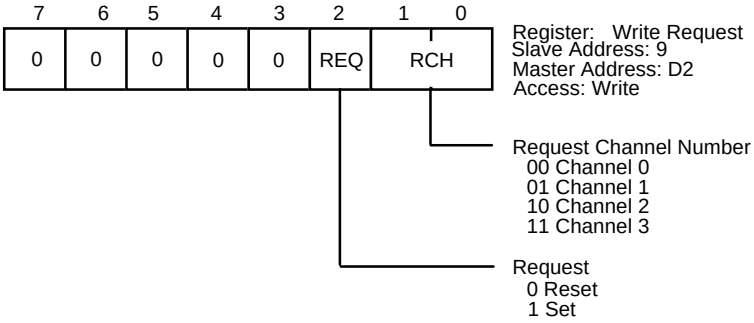
Status Register.

Command Register



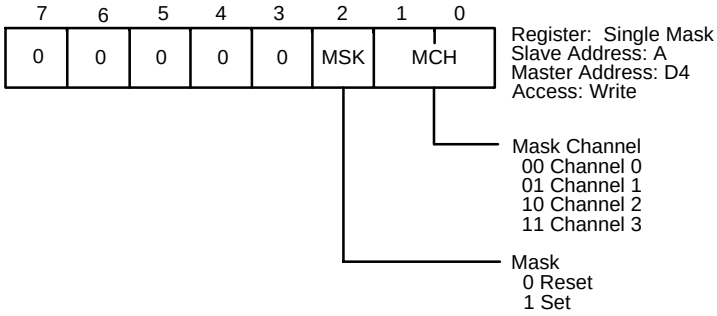
Command Register.

Write Request Register



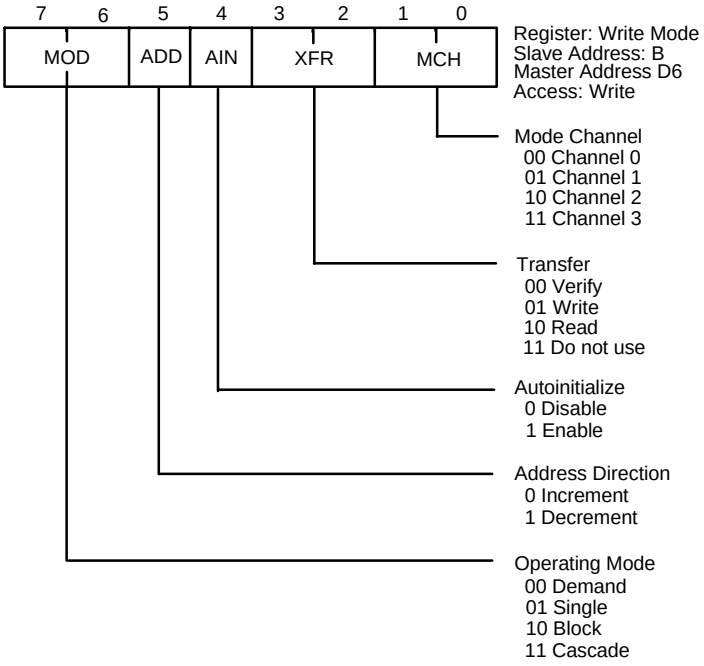
Write Request Register.

Write Single Mask Register



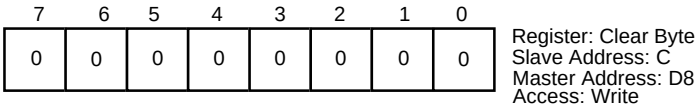
Write Single Mask Register.

Write Mode Register



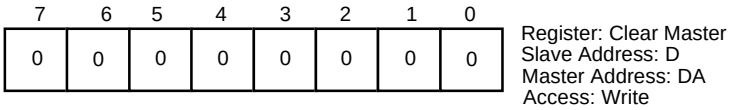
Write Mode Register.

Clear Byte Register



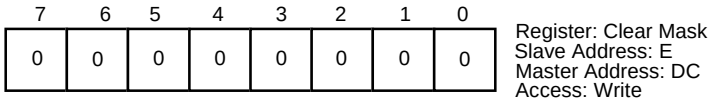
Clear Byte Register.

Clear Master Register



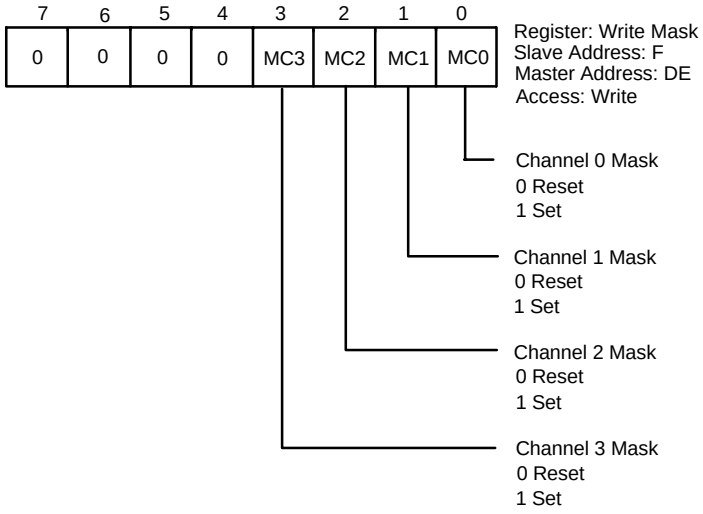
Clear Master Register.

Clear Mask Register



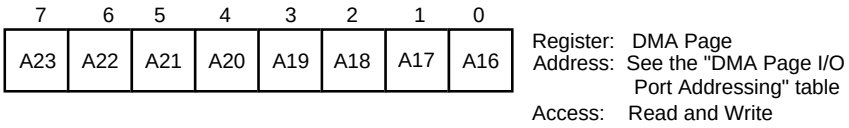
Clear Mask Register.

Write Mask Register



Write Mask Register.

DMA Page Register



DMA Page Register.

ADDITIONAL INFORMATION

Refer to the VLSI VL82C486 data book for more information on the DMA controller operating modes.

CHAPTER 7. REAL-TIME CLOCK

The ZT 8902 includes one Motorola-compatible 146818 real-time clock. The real-time clock provides clock and calendar information in addition to 50 bytes of CMOS setup static RAM (this RAM is used by the BIOS and is not available to the user). These functions are battery backed for continuous operation even in the absence of system power. The major features of the real-time clock are listed below.

- Timekeeping to a 1 second resolution
- 50 bytes of CMOS setup RAM
- Leap year compensation
- Optional Daylight Savings Time compensation
- Optional interrupt generation
- Battery backed

PROGRAMMABLE REGISTERS

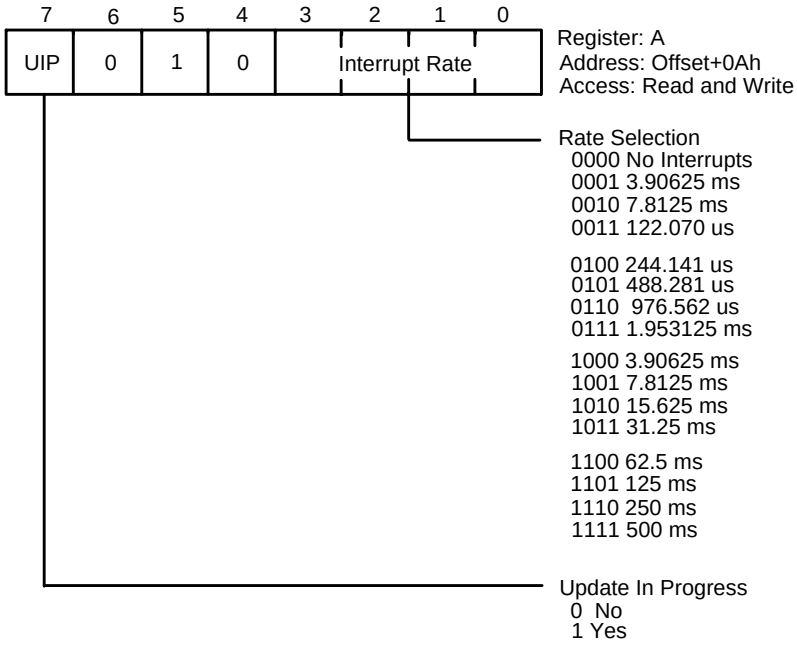
The real-time clock includes 64 register locations. These registers are accessed through I/O port locations 70h and 71h. A real-time clock register is accessed by first writing the offset address of the register to I/O port location 70h. Data is then transferred to or from the register through I/O port location 71h. This sequence must be repeated to read the same register a second time. The I/O port addressing for the real-time clock is given in the "Real-Time Clock Register Addressing" table.

The topics that follow illustrate the programmable registers for the real-time clock.

Real-Time Clock Register Addressing.

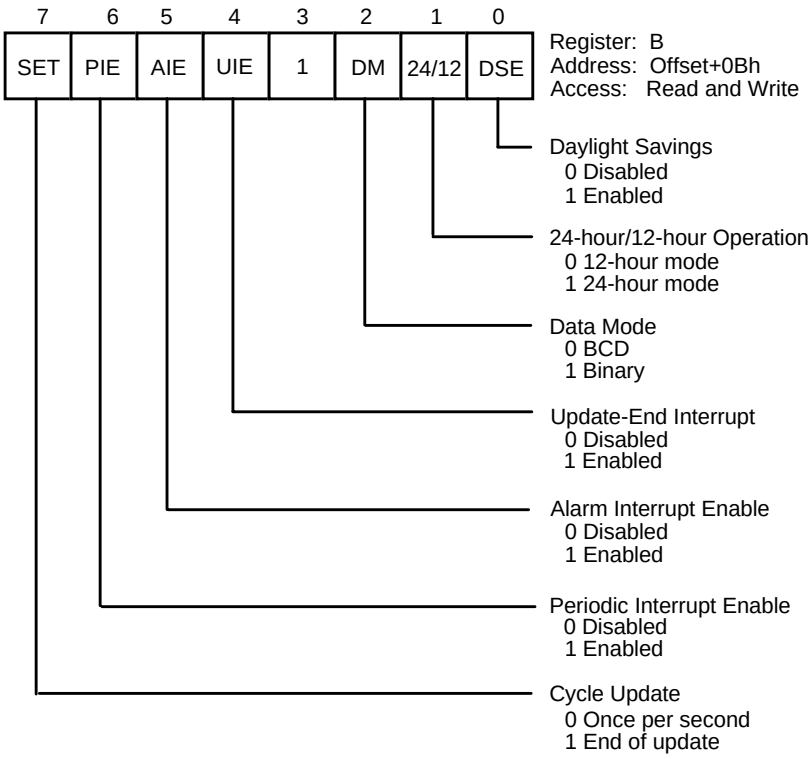
Address Offset	Function	Range
0h	Time-Seconds	0-59
1h	Alarm-Seconds	0-59
2h	Time-Minutes	0-59
3h	Alarm-Minutes	0-59
4h	Time-Hours (12 hour mode)	1-12
4h	Time-Hours (24 hour mode)	0-23
5h	Alarm-Hours	0-23
6h	Day of Week	1-7
7h	Date of Month	1-31
8h	Month	1-12
9h	Year	0-99
Ah-Dh	Register A-D	----
Eh-3Fh	General Purpose	----

Register A



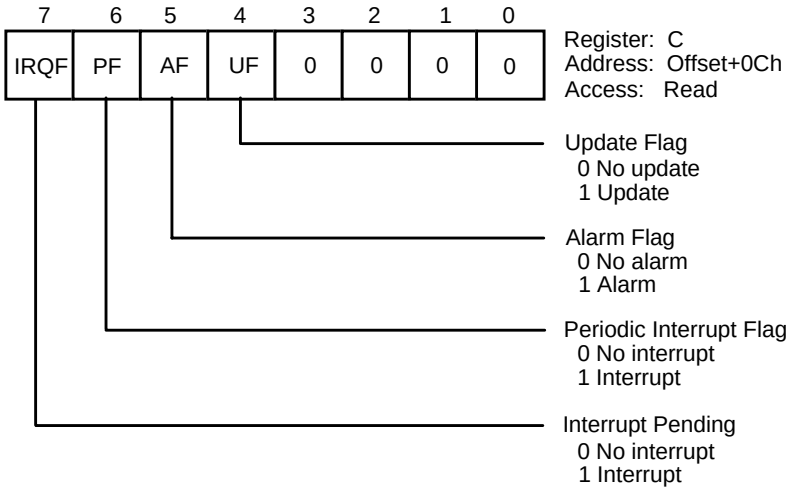
Register A.

Register B



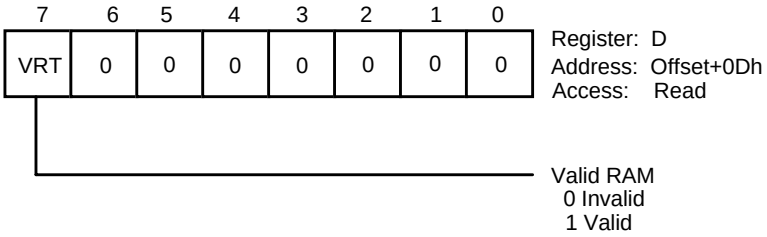
Register B.

Register C



Register C.

Register D



Register D.

ADDITIONAL INFORMATION

Refer to the VLSI VL82C106 data book for more information on the real-time clock operating modes.

CHAPTER 8. SERIAL CONTROLLER

This chapter discusses operation of the two serial ports and provides register descriptions.

ZT 8902 SPECIFICS

The ZT 8902 includes two serial ports that are compatible with the industry standard 16450/8250. The serial ports are implemented with a 5 V charge pump technology to eliminate the need for a ±12 V supply. Both serial ports include a complete set of handshaking and modem control signals, maskable interrupt generation, and data transfer rates up to 115 Kbaud. The major features of the serial ports are listed below.

- Two independent RS-232 channels
- Does not require ±12 V
- Baud rates up to 115 Kbaud
- Polled and interrupt operation
- Loopback diagnostics

The serial ports are configured as DTE and are available through 10-pin frontplane connectors. COM1 is available through J8 and COM2 is available through J7. See the "J7 and J8 Serial I/O Pinout" table in Appendix B, "Specifications," for the frontplane connector pin assignments. Optional cables interface the frontplane connectors to 9-pin D-shell connectors. A null-modem option is available to convert the DTE configuration to DCE. Adapter board options are also available to convert the RS-232 interface to an RS-485 interface.

NOTICE

Pins 1 through 9 of J7 and J8 are organized for direct ribbon cable connection to a 9-pin D-shell connector. Pin 10 is a 5 V output.

PROGRAMMABLE REGISTERS

There are six registers for initializing and controlling each serial channel. The "Serial Controller Register Addressing" table shows the I/O port addressing for these registers. The COM1 serial port is located at address 3F8-3FFh. The COM2 serial port is located at address 2F8-2FFh. It is possible to jumper disable COM2 and free up that address range for STD bus expansion; refer to the description of jumper W17 in Appendix A, "Jumper Configurations."

The topics that follow illustrate the 16-bit divisor latch, baud rate divisors, and the six programmable registers for each serial channel.

Serial Controller Register Addressing.

Address	Register	Operation
0xF8h (DIV=0)	Receive Buffer	Read
0xF8h (DIV=0)	Transmit Buffer	Write
0xF8h (DIV=1)	Divisor Latch LSB	Read/Write
0xF9h (DIV=0)	Interrupt Control	Read/Write
0xF9h (DIV=1)	Divisor Latch MSB	Read/Write
0xFAh	Interrupt Status	Read
0xFBh	Line Control	Read/Write
0xFCh	Modem Control	Read/Write
0xFDh	Line Status	Read
0xFEh	Modem Status	Read
0xFFh	Reserved	

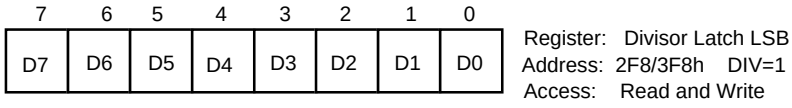
Baud Rate Divisors

The "Divisor Latch LSB" and "Divisor Latch MSB" figures that follow illustrate the 16-bit divisor latch. The "Baud Rate Divisors" table lists the divisors for popular baud rates. It also includes the percent error based on the difference between the exact divisor for a specified baud rate and the divisor obtainable with a 16-bit integer format. To guarantee proper operation, the percent error should never be greater than four.

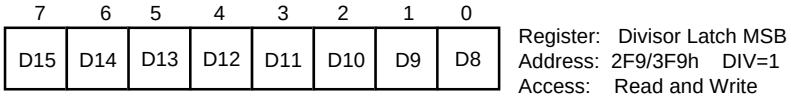
Baud Rate Divisors.

Baud Rate	Divisor (dec/hex)	Percent Error
50	2304/1440h	0
75	1536/960h	0
150	768/480h	0
300	384/240h	0
600	192/120h	0
1200	96/60h	0
1800	64/40h	0
2000	58/3Ah	0.69
2400	48/30h	0
3600	32/20h	0
4800	24/18h	0
7200	16/10h	0
9600	12/Ch	0
19200	6/6h	0
38400	3/3h	0
56000	2/2h	2.86
57600	2/2h	0
115200	1/1h	0

Divisor Latch LSB and MSB

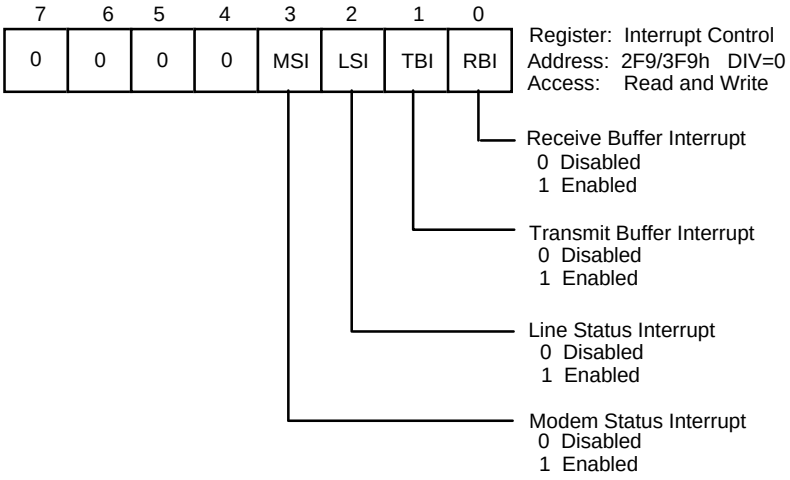


Divisor Latch LSB.



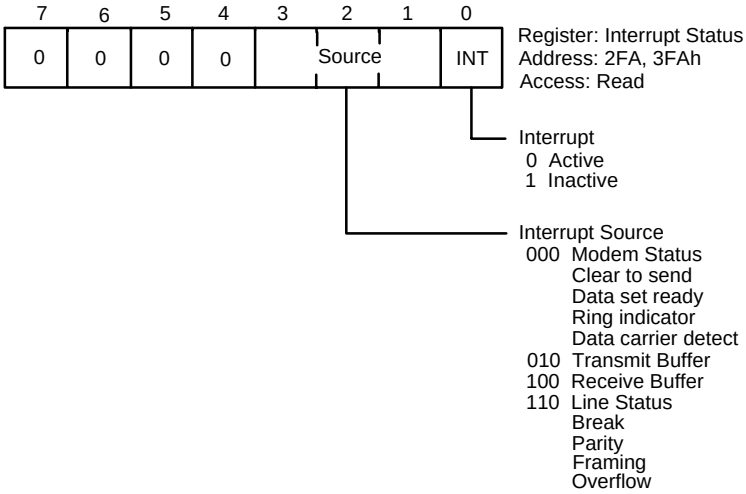
Divisor Latch MSB.

Interrupt Control Register



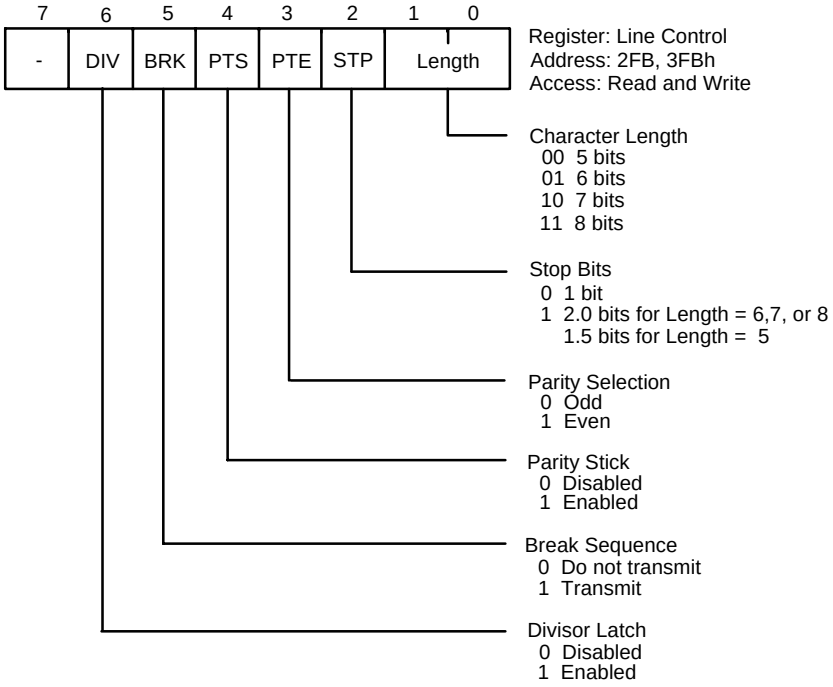
Interrupt Control Register.

Interrupt Status Register



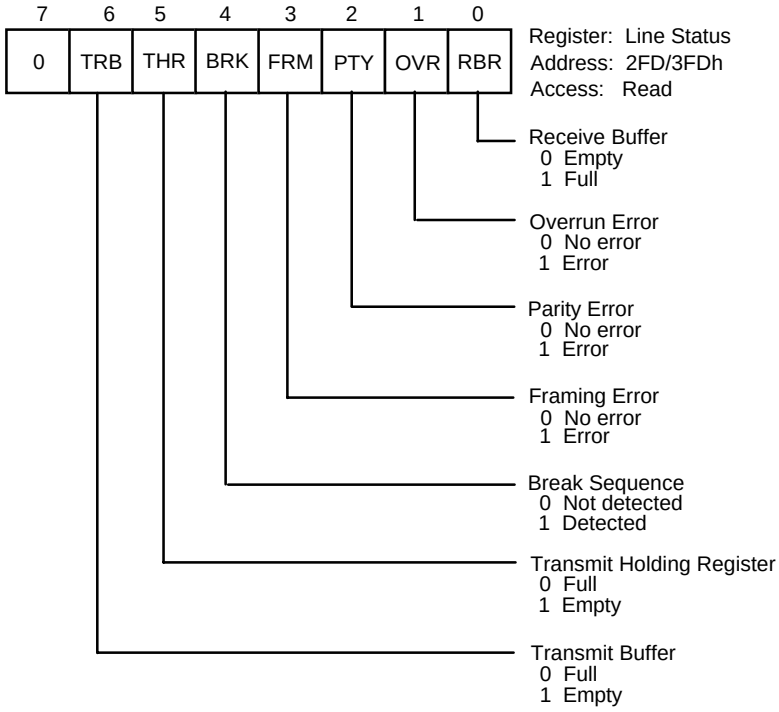
Interrupt Status Register.

Line Control Register



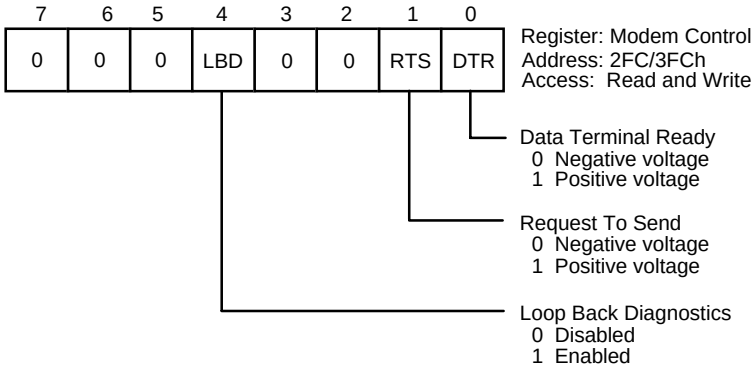
Line Control Register.

Line Status Register



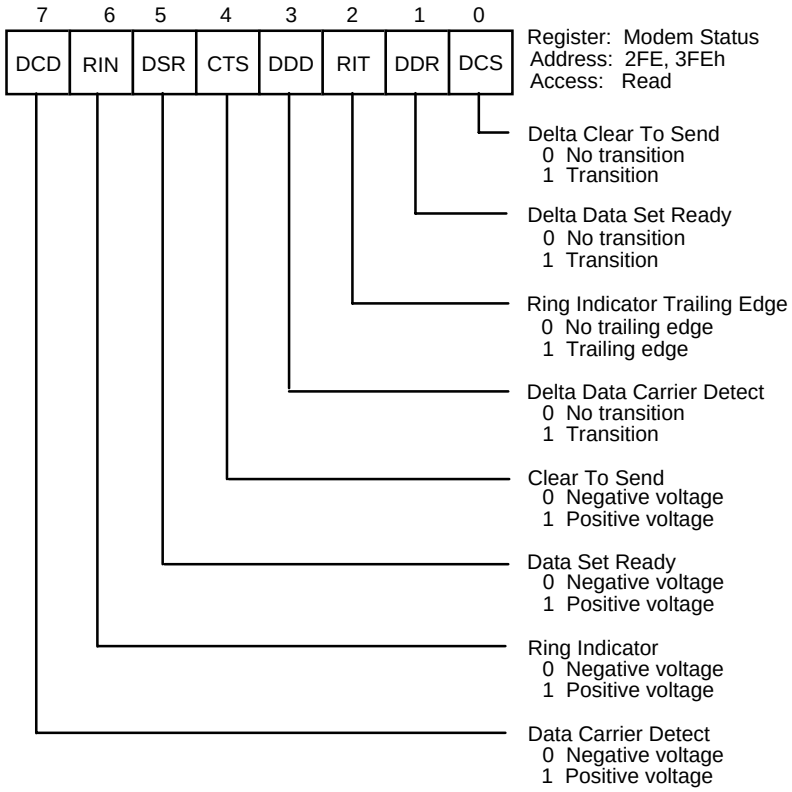
Line Status Register.

Modem Control Register



Modem Control Register.

Modem Status Register



Modem Status Register.

ADDITIONAL INFORMATION

Refer to the VLSI VL82C106 data book for more information on the serial controller operating modes.

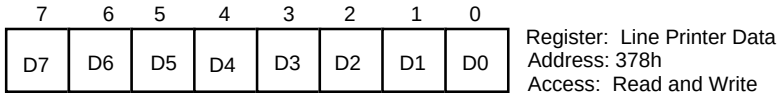
CHAPTER 9. CENTRONICS PRINTER INTERFACE

The bidirectional printer interface fully supports a Centronics-compatible printer. The Centronics interface is available through the J2 connector. See the "J2 Centronics Printer Pinout" table in Appendix B, "Specifications," for the connector pin assignments.

PROGRAMMABLE REGISTERS

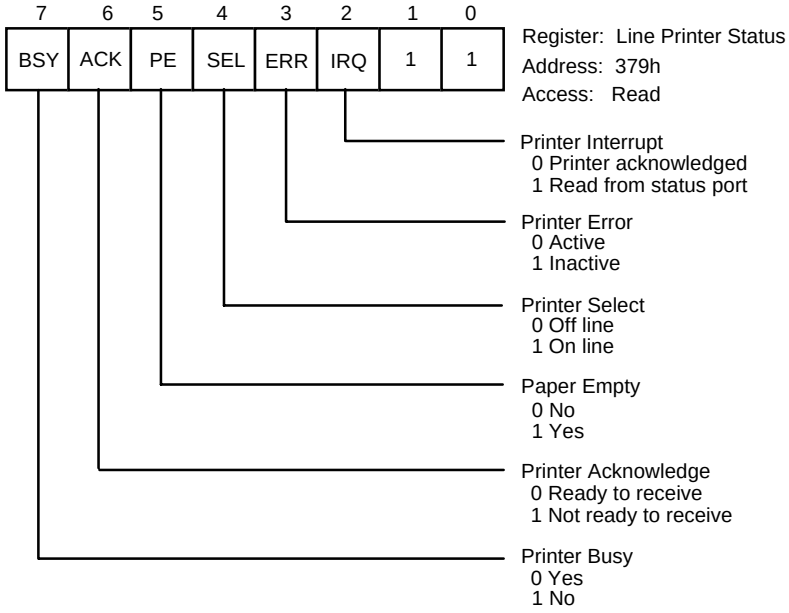
The following topics illustrate the programmable registers for the Centronics printer interface.

Line Printer Data Register



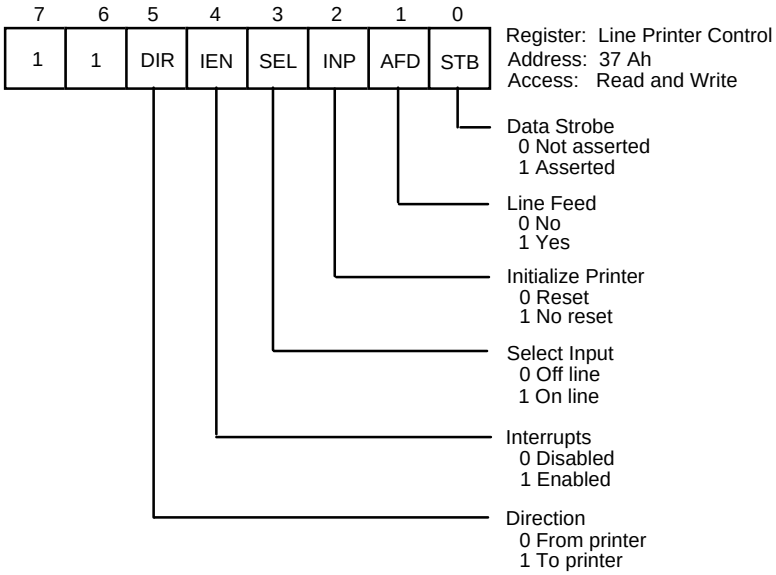
Line Printer Data Register.

Line Printer Status Register



Line Printer Status Register.

Line Printer Control Register



Line Printer Control Register.

ADDITIONAL INFORMATION

Refer to the VLSI VL82C106 data book for more information on the serial controller operating modes.

CHAPTER 10. PARALLEL I/O

The ZT 8902 includes six 8-bit parallel ports for a total of 48 I/O signals. Three of the parallel ports are used to control and monitor dedicated operations. Chapter 12, "System Registers," includes a detailed description of these parallel ports. The remaining three parallel ports are available through frontplane connector J5 for use by the application. Refer to the "J5 Parallel I/O Pinout" table in Appendix B, "Specifications," for the connector pin assignments.

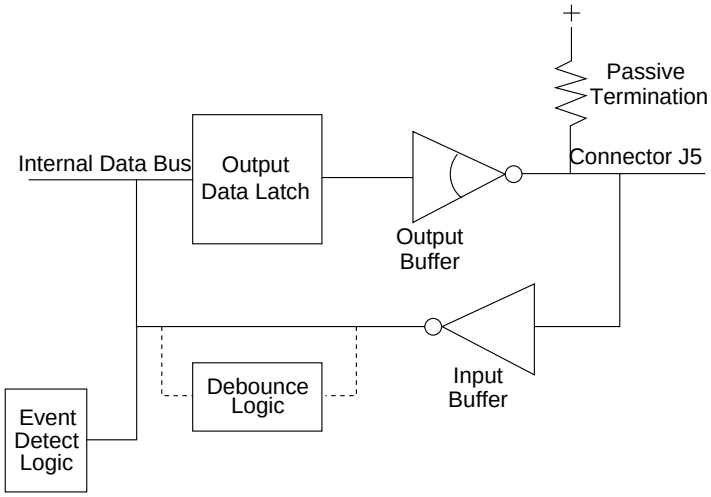
Each of the 25 parallel I/O signals is configured as an input or an output with readback under software control. The major features of the parallel I/O are listed below.

- 12 mA sink current
- Stable outputs during power up and reset
- Continuous data transfer rates up to 1 Mbyte/second
- Each I/O signal is independently programmable as an input or an output with readback
- Optional cable for direct connection to industry-standard I/O module mounting racks
- Event sensing and debouncing on all ports under software control

FUNCTIONAL DESCRIPTION

The parallel I/O signals are supported through the 16C50A, a custom ASIC device designed by Ziatech. Refer to Appendix C, "Parallel I/O Considerations," for tips on preventing latchup from the CMOS parts in the 16C50A. Appendix C provides illustrations of proper system configuration.

A functional diagram of each I/O signal is illustrated in the "Parallel Port Functional Diagram" figure. The diagram includes an output latch, an output buffer, and an input buffer. These functional blocks are described in the following topics.



Parallel Port Functional Diagram.

Output Latch

The output latch stores the data present on the internal data bus during a write operation to the parallel port. The data is latched until altered by another parallel port write, until a system reset, or until the power is turned off. The output latch is initialized with a logical 0 during power on and system reset.

Output Buffer

The output buffer isolates the output latch from connector J5. The output buffer is an inverting open-collector device with 12 mA of sink current and glitch-free operation during power cycles. The inversion means that a logical 0 written to the parallel port appears as a TTL high at connector J5, and a logical 1 written to the parallel port appears as a TTL low at connector J5.

The open collector feature permits each parallel I/O signal to be software configured as an input. To use a parallel port signal as an input, a logical 0 must first be written to the output latch. This causes the output buffer to become an open-collector gate and prevents contention with the input signal. The passive termination ranges from 25 k Ω minimum to 120 k Ω maximum. Applications needing a predictable rise time should provide additional termination.

Input Buffer

The input buffer is enabled during read operations to transfer the data from connector J5 to the internal data bus. If the parallel port bit is configured as input, the data read is the data driven by an external device.

The input buffer is an inverting device. This means that data read from the parallel port as a logical 0 is a TTL high at connector J5, and data read from the parallel port as a logical 1 is a TTL low at connector J5.

Enhanced Features

Refer to the ICPSMCI-16C50A Digital Specification to use enhanced features of the digital ASIC.

PROGRAMMABLE REGISTERS

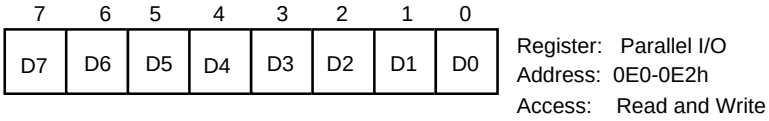
There are a total of six parallel I/O registers. Three of the registers are dedicated to controlling and monitoring local operations and three are available through connector J5 for application use. The dedicated registers are discussed in Chapter 12, "System Registers." There is also a mask register to independently inhibit parallel port write operations. The address of each of the registers is shown in the "I/O Port Addressing" table.

The topics that follow illustrate the parallel I/O registers and the mask register.

I/O Port Addressing.

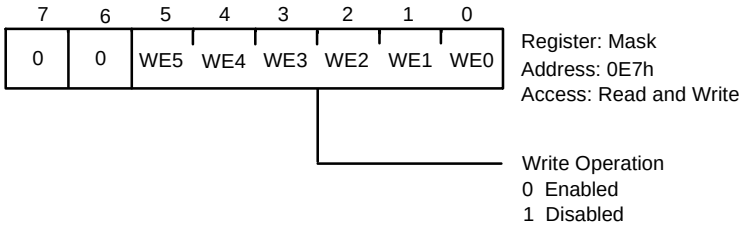
Address	Register	Operation
00E0h	Parallel I/O 0	Read/Write
00E1h	Parallel I/O 1	Read/Write
00E2h	Parallel I/O 2	Read/Write
00E3h	System Register	Dedicated
00E4h	System Register	Dedicated
00E5h	System Register	Dedicated
00E6h	Not Supported	
00E7h	Mask Register	Read/Write

Parallel I/O Registers



Parallel I/O Registers.

Mask Register



Mask Register.

ADDITIONAL INFORMATION

Refer to the ICPSMCI-16C50A Digital Specification to use enhanced features of the digital ASIC.

CHAPTER 11. WATCHDOG TIMER

The primary function of the watchdog timer is to monitor ZT 8902 operation and to take corrective action if the system fails to function as programmed. The major features of the watchdog timer are listed below.

- Enabled and disabled through software control
- Armed and strobed through software control
- Generates a CPU reset if allowed to time out

The watchdog timer is armed and strobed with the WDE bit in system register 3 (refer to Chapter 12, "System Registers"). The watchdog timer is disabled after power on or system reset. Writing a logical 1 to the watchdog timer bit arms the watchdog timer. Once armed, the watchdog timer must be strobed with a periodic frequency less than the timeout period or a system reset is generated. The factory configured timeout period is 550 ms. The watchdog timer is strobed by first writing a logical 0 to WDE, immediately followed by writing a logical 1 to WDE.

The following code shows the procedure for arming and strobing the watchdog timer.

```
mov         dx,0e7h  ;disable system register mask
in          al,dx
and         al,0dfh
out         dx,al

mov         dx,0e5h  ;arm watchdog
in          al,dx
or          al,1
out         dx,al

mov         dx,0e5h  ;strobe watchdog
in          dx,al
and         al,0feh
out         dx,al
or          al,1
out         x,al
```

CHAPTER 12. SYSTEM REGISTERS

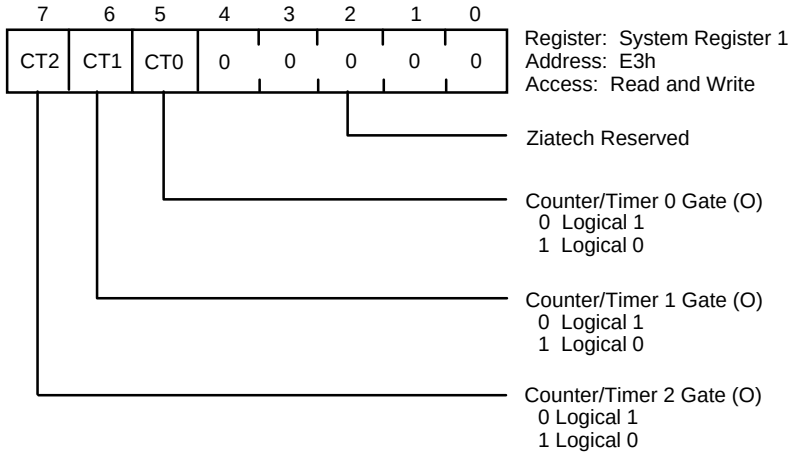
There are three system registers used to control and monitor a variety of functions on the ZT 8902. These registers are implemented with the same Ziatech 16C50A ASIC that implements the 24 parallel I/O lines discussed in the "Parallel I/O" chapter. The 16C50A operating instructions are outlined below. Refer to Chapter 10, "Parallel I/O," for a complete discussion.

- The reset state for all bits is a logical 0
- Bits dedicated to input operation must remain programmed with a logical 0 to prevent contention with the input device
- Bits dedicated to output operation have readback capabilities

PROGRAMMABLE REGISTERS

The following topics illustrate system registers 1, 2, and 3 and the mask register.

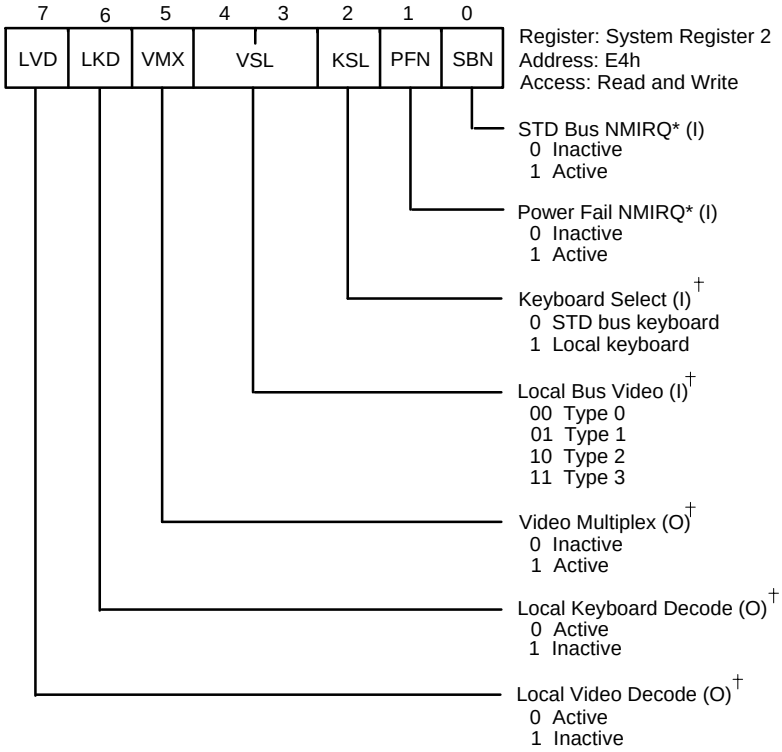
System Register 1



Note: (O) indicates output.

System Register 1.

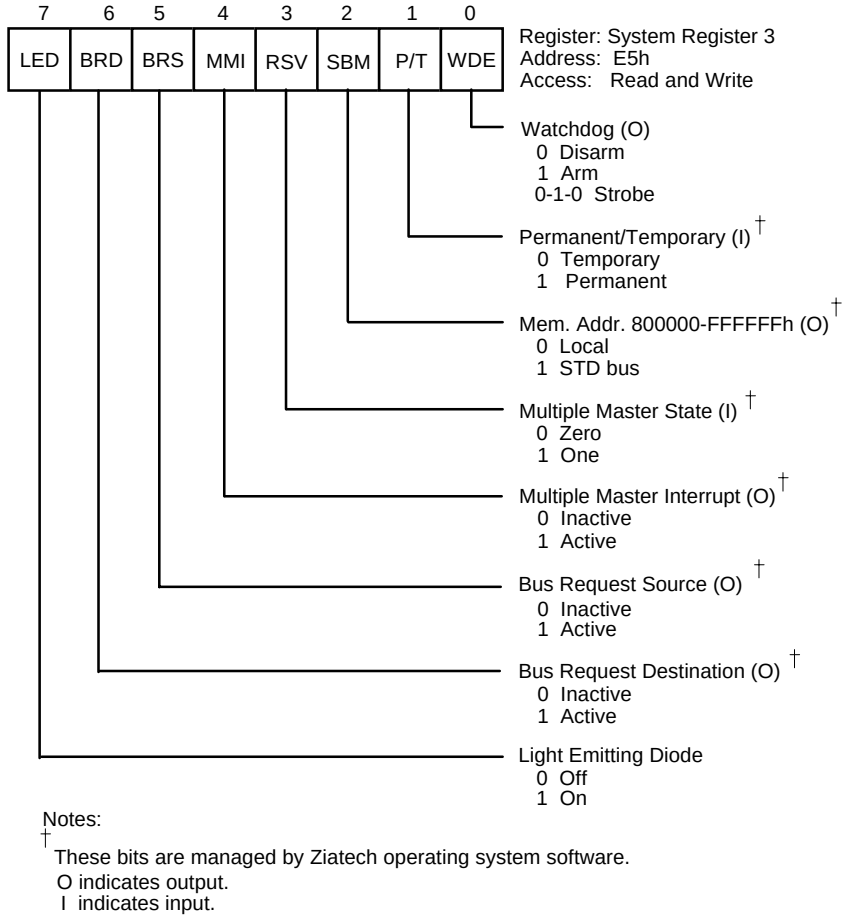
System Register 2



Notes:
† These bits are managed by Ziatech operating system software.
O indicates output.
I indicates intput.

System Register 2.

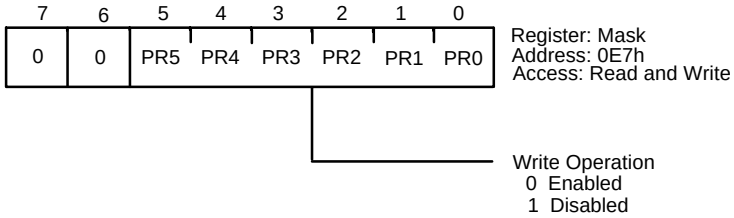
System Register 3



Notes:
† These bits are managed by Ziatech operating system software.
O indicates output.
I indicates input.

System Register 3.

Mask Register



Mask Register.

ADDITIONAL INFORMATION

The ZT 8902 includes several other system registers that are exclusively managed by Ziatech operating system software. These registers are located in the VLSI VL82C486. Refer to the VLSI data book for more information on these registers.

CHAPTER 13. LOCAL BUS VIDEO

The ZT 8902 includes a local bus interface to permit high speed peripherals direct access to the CPU bus. This bus supports 32-bit data and address busses and operates synchronously at CPU speeds of up to 33 MHz. Ziatech offers zVID video adapters designed specifically for this local bus interface. These adapters give superior performance over STD bus video solutions by running with four times the data width and more than four times the operating frequency. Major features of the video adapters are listed below. Refer to the zVID manual for installation and operating instructions.

- Up to 700 times the performance of STD bus solutions
- Reduces STD bus traffic by keeping all video operations local
- Combined single-slot occupancy for both the ZT 8902 and zVID
- Flat panel and feature connector support
- Keyboard support
- Resolutions up to 1024 x 768 x 256 colors

CHAPTER 14. PROGRAMMABLE LED

The ZT 8902 includes a Light-Emitting Diode (LED) located immediately below the board extractor. The LED is software programmable through the LED bit in system register 3 (refer to Chapter 12, "System Registers"). Writing a logical 0 to the LED bit turns the LED off and writing a logical 1 to the LED bit turns the LED on. The LED is turned off after a power cycle or a reset.

The following code shows how to turn the LED on and off.

```
;-------------------------------------
; The multiple master interrupt is
; a bidirectional bit.  The current
; software state of multiple master
; interrupt is maintained in the
; multiple master state bit. Input_e5
; updates the multiple master bit with
; the current software state maintained
; in the multiple master state bit.
;-------------------------------------

input_e5        macro
                local   multiple_on
                in      al,0e5h
                test    al,8
                jnz     multiple_on
                and     al,not 8
multiple_on:
                endm

;-------------------------------------
; led_on turns on the led.  Bits 1 and
; 3 are inputs which must be written as
; a zero.  Bit 4 is bidirectional, which
; is handled by the input_e5 macro.
;-------------------------------------

led_on:         pushf
                cli
                input_e5
                and     al,not 2
                or      al,80h
                out     0e5h,al
                popf
                ret

;-------------------------------------
; led_off turns off the led.  Bits 1 and
; 3 are inputs which must be written as
; a zero.  Bit 4 is bidirectional, which
; is handled by the input_e5 macro.
;-------------------------------------

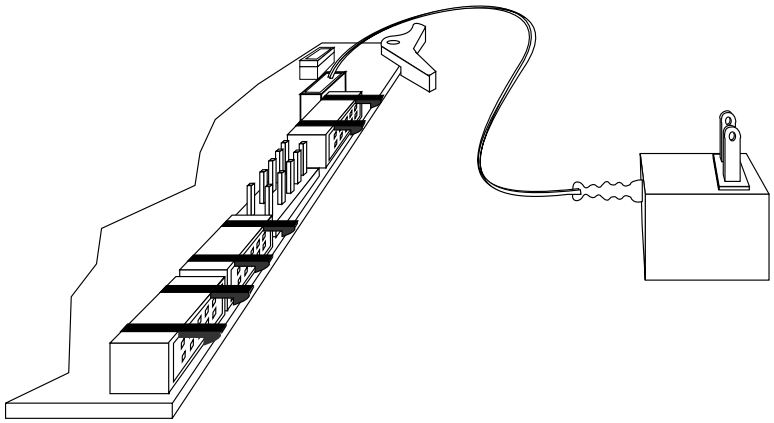
led_off:        pushf
                cli
                input_e5
                and     al,not (82h)
                out     0e5h,al
                popf
                ret
```

CHAPTER 15. AC POWER FAIL

The ZT 8902 supports AC power-fail detection for giving the application advanced warning of an impending power failure. The advanced warning is used by the application for performing operations such as saving critical data and entering a dormant state.

The ZT 8902 requires a transformer-isolated AC voltage of no more than 30 V from the same source that provides the system power. Ziatech's optional AC wall transformer (ZT 90071) meets these requirements. The wall transformer is connected to the J1 frontplane connector, as shown in the "AC Wall Transformer Installation" figure. The pin assignments for connector J1 are given in Appendix B.

Caution: Do not plug the AC adapter into J9 (the speaker output connector). Doing so may damage the board and void the warranty.



AC Wall Transformer Installation.

In operation, a non-maskable interrupt is generated when AC power falls below 95 VRMS. The non-maskable interrupt must be enabled through jumper selection. The application software must include a non-maskable interrupt service routine to perform the following:

- Determine if the AC power fail is the source of the interrupt request. The three sources of non-maskable interrupts are AC power fail, STD bus NMIRQ*, and Parity Error.
- Preserve any critical information into Flash memory, either for failure analysis or for system restart.
- Place the CPU in a dormant state using a halt instruction or a looping sequence that is not reading or writing critical data to memory or I/O.

APPENDIX A. JUMPER CONFIGURATIONS

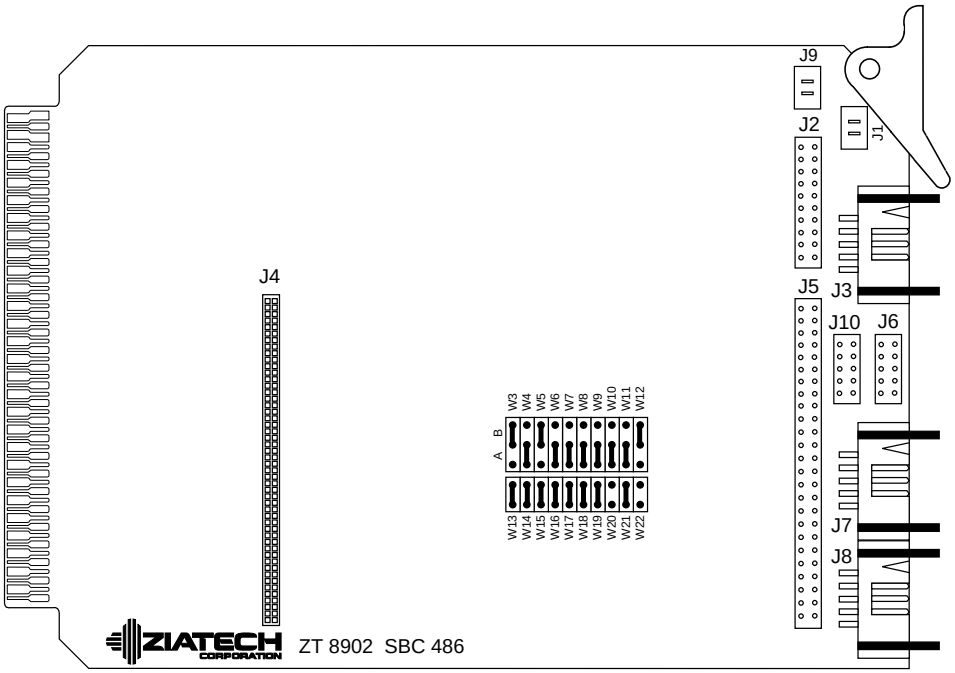
The ZT 8902 includes several options that tailor the operation of the board to requirements of specific applications. The options are selected by installing and removing shorting receptacles (jumpers) or surface mount 0 Ω resistors (cuttable traces).

The ZT 8902 includes jumpers with two posts and jumpers with three posts. Jumpers having only two posts are labeled W**x,** where **x** defines the jumper number. Jumpers having three posts are labeled W**x** "a" and "b." These jumpers have two possible selections, where "a" is one selection and "b" is another. Similarly, cuttable traces with only two pads are labeled CT**x,** while cuttable traces having three pads are labeled CT**x** "a" and "b."

This appendix provides detailed descriptions of all jumper and cuttable trace options, as well as illustrations of the board showing the locations of all jumpers and cuttable traces.

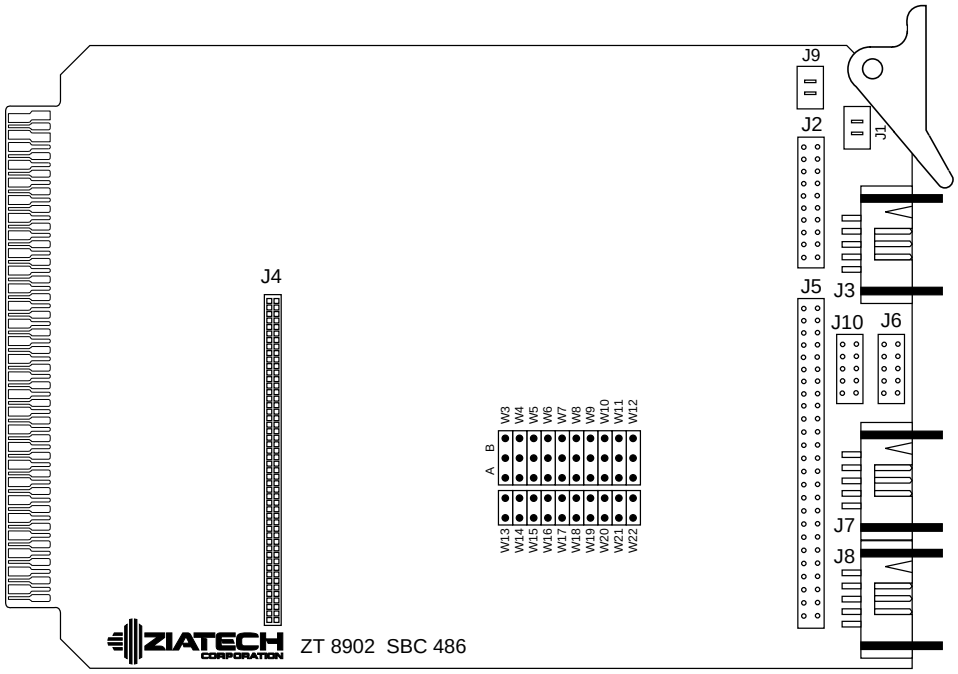
FACTORY DEFAULT JUMPER CONFIGURATION

The "DOS Factory Default Configuration" figure below illustrates the factory default jumper configuration for ZT 8902 boards purchased in a DOS system. Note that spare jumper-shorting connectors are shipped on W14 and W19.



DOS Factory Default Configuration.

"Customer Jumper Configuration" shows the jumper pin locations on the board. Use a printout of this figure to document your jumper configuration if it differs from the factory default.



Customer Jumper Configuration.

JUMPER CROSS-REFERENCE TABLE

The following table divides the jumper options into functional groups.

Jumper Cross Reference.

Function	Jumpers
CMOS RAM Erase	W11
Keyboard Delay	W21
Local or STD Bus Boot	W15
Local or STD Bus COM2	W17
Local or STD Bus Keyboard	W20
Maskable Interrupts	W4-10,12
Multiple Master Interrupt	W3
Non-Maskable Interrupts	W13,22
Permanent or Temporary Master	W18
Reserved	W1,2
Spare Jumper Locations	W14, W19
STD Bus Access Inhibit	W16

JUMPER DESCRIPTIONS

The following topics list the jumpers in numerical order and provide a detailed description of each jumper. A dagger (†) indicates the default jumper configuration.

W1, W2--Reserved

W1 and W2 are not used on ZT 8902 Revision B.

W3--Multiple Master Interrupt

W3 defines the signal path for the multiple master interrupt. Selecting INTRQ4* releases INTRQ* for application use. On occasion, INTRQ4* is defined for VBAT on the STD bus. If this is the case, select INTRQ* for the multiple master interrupt and remove cuttable trace CT11. (CT11 is discussed at the end of this appendix.)

	W3a	W3b	Multiple Master Interrupt
	IN	OUT	STD Bus INTRQ* (P44)
†	OUT	IN	STD Bus INTRQ4* (P5)

†Factory default configuration for DOS systems

W4-W10, W12--Maskable Interrupts

W4-W10 and W12 assign up to nine interrupt sources to the interrupt controller inputs. Each interrupt input has two possible sources selected by installing a jumper in position "a" or position "b." Other combinations are possible with wire wrap techniques. Interrupt inputs not used in the application must be masked in software.

Refer to the "Interrupt Architecture" illustration in Chapter 4 for details.

	Jumper	Interrupt Source	Interrupt
†	W4a	STD bus INTRQ*	IR9
	W4b	J3 pin 2	IR9
	W5a	Keyboard	IR1
†	W5b	STD bus INTRQ1*	IR1
†	W6a	Serial COM2	IR3
	W6b	J3 pin 4	IR3
†	W7a	Serial COM1	IR4
	W7b	Timer 2 channel 0	IR4
†	W8a	STD bus INTRQ4*	IR5
	W8b	J3 pin 6	IR5
†	W9a	STD bus INTRQ2*	IR6
	W9b	J3 pin 8	IR6
†	W10a	Printer LPT1	IR7
	W10b	J3 pin 10	IR7
	W12a	Timer 2 channel 1	IR14
†	W12b	STD bus INTRQ3*	IR14

†Factory default configuration for DOS systems

W11--CMOS RAM Erase

W11 removes the contents of the battery backed CMOS configuration RAM. The CMOS RAM is erased by turning off the power and moving the W11a shorting jumper to position W11b and back to W11a again.

	W11a	W11b	CMOS Configuration RAM
†	IN	OUT	Normal operation
	OUT	IN	Erase

†Factory default configuration for DOS systems

W13, W22--Non-Maskable Interrupts

W13 and W22 arm the STD bus and AC power-fail interrupts to generate non-maskable interrupt requests. These interrupts combine with the parity error interrupt before being routed to the CPU. Bit 3 of the port 61h register, located in the 82C486, enables and disables the combined interrupt source to the CPU. Bit 2 of the port 61h register, also located in the 82C486, indicates whether a non-maskable interrupt was generated by a parity error. (See the "Non-Maskable Interrupt Structure" figure in Chapter 3, "STD Bus Interface.") The ZT 8902 system register 2, located in the 16C50A, indicates whether a non-maskable interrupt was generated by the STD bus or an AC power failure. Refer to Chapter 12, "System Registers," for an illustration of system register 2.

	W13	STD Bus NMIRQ*
†	IN	Enabled
	OUT	Disabled

	W22	AC Power Fail NMIRQ*
	IN	Enabled
†	OUT	Disabled

†Factory default configuration for DOS systems

W14--Spare Jumper

Spare jumper storage location. Factory default installs W14.

W15--Local or STD Bus Boot

W15 enables the ZT 8902 to begin program execution from local Flash devices or an STD bus memory board. Select the system boot operation if the local Flash devices are corrupted and the ZT 8902 fails to boot properly. With system boot enabled, the ZT 8902 begins program execution from STD bus memory mapped at address FFFFF0h.

	W15	Boot Source
†	IN	Local Flash memory
	OUT	STD bus memory

†Factory default configuration for DOS systems

W16--STD Bus Access Inhibit

W16 prevents all operations from reaching the STD bus. This function permits a temporary master operating with DOS to be installed in a system as a stand-alone processor.

	W16	STD Bus Access
†	IN	Enabled
	OUT	Disabled

†Factory default configuration for DOS systems

W17--Local or STD Bus Serial Channel COM2

W17 determines if serial channel COM2 is addressed locally to the ZT 8902 or on the STD bus. The STD bus selection is useful for operating the ZT 8902 with other STD bus peripherals, such as a modem, which require COM2 mapping.

	W17	Serial Channel COM2
†	IN	Enabled
	OUT	Disabled

†Factory default configuration for DOS systems

W18--Permanent or Temporary Master

W18 configures the ZT 8902 to operate as a permanent or temporary master. In a single master architecture, the ZT 8902 must be configured for permanent master operation.

Refer to the description of cuttable trace CT33 at the end of this appendix for information on forcing BIOS to configure the ZT 8902 as a permanent master regardless of the position of jumper W18.

	W18	Master Configuration
†	IN	Permanent
	OUT	Temporary

†Factory default configuration for DOS systems

W19--Spare Jumper

Spare jumper storage location. Factory default installs W19.

W20--Local or STD Bus Keyboard

W20 determines the location of the keyboard controller. Select Local keyboard if the ZT 8902 includes an optional local bus video adapter installed in connector J4.

	W20	Keyboard Location
	IN	Local keyboard
†	OUT	System keyboard

†Factory default configuration for DOS systems

W21--Keyboard Delay

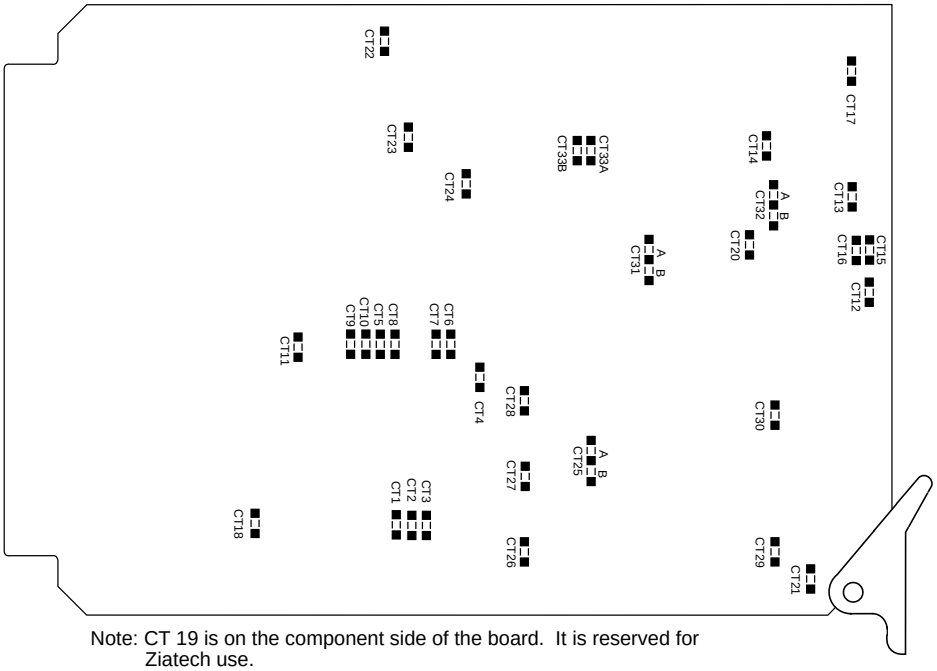
W21 delays the CPU by two seconds during initial startup to permit the keyboard controller to complete initialization.

	W21	Keyboard Delay
†	IN	Enabled
	OUT	Disabled

†Factory default configuration for DOS systems

CUTTABLE TRACE OPTIONS AND LOCATIONS

The ZT 8902 supports several less frequently selected options with the addition or removal of 0 ohm surface mount resistors. This operation requires a solder iron and someone qualified to use it on small surface mount devices. Cuttable traces are labeled CT**x**, where **x** defines the cuttable trace number. The cuttable trace locations are illustrated in the figure below.



Note: CT 19 is on the component side of the board. It is reserved for Ziatech use.

Customer Cuttable Trace Locations.

CUTTABLE TRACE CROSS-REFERENCE TABLE

The following table divides the cuttable trace options into functional groups.

Cuttable Trace Cross-Reference.

Function	Cuttable Traces
Aux. Counter/Timer Clock Source	CT12, 15, 16
Counter/Timer Clock Selection	CT31
Frontplane DMA Enable	CT24
Frontplane DMA Select	CT22, 23
Frontplane Interrupts	CT1 - CT3
INTRQ4* Enable	CT11
IR15 Source	CT32
Perm. Master Programming Selection	CT33
Reserved	CT4 - CT10,CT13, 14, 17-21, CT 25-30

CUTTABLE TRACE DESCRIPTIONS

The following topics list the cuttable traces in numerical order and provide a detailed description of each trace. A dagger (†) indicates the default configuration.

CT1-CT3--Frontplane Interrupts

CT1-CT3 assign up to three frontplane interrupt sources to the interrupt controller inputs.

	CT1	Function
†	IN	Connects J3 pin 6 to IR11
	OUT	No connection

	CT2	Function
†	IN	Connects J3 pin 10 to IR12
	OUT	No connection

	CT3	Function
†	IN	Connects J3 pin 4 to IR10
	OUT	No connection

†Factory default configuration for DOS systems

CT4-CT10--Reserved

Reserved for Ziatech use.

CT11--INTRQ4* Enable

CT11 enables INTRQ4* onto STD bus P5. This cuttable trace should remain installed unless VBAT is driven onto P5 by any board in the STD bus system.

	CT11	STD Bus P5
†	IN	Drive INTRQ4* with the DC Power Down (DCPDN*) interrupt
	OUT	No connection

†Factory default configuration for DOS systems

CT12, CT15, CT16--Aux. Counter/Timer Clock Source Selection

CT12, CT15, and CT16 connect the clock source of each auxiliary counter/timer to either a local 8 MHz source or the frontplane connector J6.

	CT12	Timer 2 Channel 3 Clock Source
†	IN	8 MHz 50% duty cycle
	OUT	J6 pin 8

	CT15	Timer 2 Channel 2 Clock Source
†	IN	8 MHz 50% duty cycle
	OUT	J6 pin 4

	CT16	Timer 2 Channel 1 Clock Source
†	IN	8 MHz 50% duty cycle
	OUT	J6 pin 1

†Factory default configuration for DOS systems

CT13, CT14, CT17-CT21--Reserved

Reserved for Ziatech use.

CT22, CT23--Frontplane DMA Selection

CT22 and CT23 select the DMA channels that are routed to the DMA frontplane connector J10. (Refer to Appendix B, "Specifications," for a pinout of J10.).

	CT22	DMA Frontplane Connector (J10) Pins 2, 4
†	IN	16-bit DMA channel 6
	OUT	8-bit DMA channel 1

	CT23	DMA Frontplane Connector (J10) Pins 1, 3
	IN	16-bit DMA channel 5
†	OUT	8-bit DMA channel 0

†Factory default configuration for DOS systems

CT24--Frontplane DMA Enable

Enables frontplane connector J10 pins 1 and 3 to support a second DMA channel. This cuttable trace must be removed if the DMA frontplane connector is used with an STD bus board that grounds pin 3.

	CT24	DMA Frontplane Connector (J10) Pins 1, 3
	IN	DMA acknowledge
†	OUT	No connection

†Factory default configuration for DOS systems

CT25-CT30--Reserved

Reserved for Ziatech use.

CT31--Counter/Timer Clock Selection

Selects the clock input source for all three counter/timers.

	CT31a	CT31b	Clock Source
	IN	OUT	8 MHz oscillator to counter/timer
†	OUT	IN	8 MHz backplane clock

†Factory default configuration for DOS systems

CT32--IR15 Source

Selects either the output from counter/timer 2 or the interrupt output from the digital I/O ASIC.

	CT32a	CT32b	IR15 Source
†	IN	OUT	Interrupt from counter/timer 2 drives IR15
	OUT	IN	Interrupt from digital I/O ASIC (U10) drives IR15

†Factory default configuration for DOS systems

CT33--Permanent Master Programming Selection

Used only in special permanent master configurations. This cuttable trace should remain in the factory default position.

	CT33a	CT33b	Permanent Master ID Input to ASIC
	IN	OUT	Force BIOS to configure board as permanent master regardless of jumper W18 position
†	OUT	IN	BIOS looks at jumper W18 for master/slave configuration

†Factory default configuration for DOS systems

APPENDIX B. SPECIFICATIONS

This appendix describes the electrical, environmental, and mechanical specifications of the ZT 8902. It also includes illustrations of the board dimensions, the P/E connector pinouts, and cables commonly used with the ZT 8902, as well as tables showing the pin assignments for the ZT 8902's 10 connectors.

ELECTRICAL AND ENVIRONMENTAL

The following topics list electrical and environmental specifications, including absolute maximum ratings, DC operating characteristics, battery backup characteristics, and STD bus loading characteristics.

Absolute Maximum Ratings

Supply Voltage, Vcc: 0 to 7 V

Supply Voltage, AUX +V: 0 to 12.6 V (required for Flash programming only)

Supply Voltage, AUX -V: Not used

Storage Temperature: -40° to +85° Celsius

Operating Temperature (ZT 8902): 0° to +65° Celsius

Operating Temperature (ZT 89LT02): -40° to +70° Celsius

Non-Condensing Relative Humidity: <95% at 40° Celsius

DC Operating Characteristics

Supply Voltage, Vcc: 4.75 to 5.25 V

Supply Voltage, AUX +V: 11.4 to 12.6 V

Supply Voltage, AUX -V: Not used

Supply Current, Icc:

486SX-25: 0.9 A typ., 1.5 A max.

486SX-33: 1.0 A typ., 1.6 A max.

486DX-33: 1.2 A typ., 2.0 A max.

486DX2-50: 1.3 A typ., 2.2 A max.

486DX2-66: 1.5 A typ., 2.5 A max.

486DX4-100: 1.4 A typ., 2.3 A max.

(Numbers assume 4 Mbytes of DRAM and 1 Mbyte of Flash)

Supply Current, AUX +V: 0.010 A typ., 0.030 A max.

Battery Backup Characteristics

Battery Voltage: 3 V

Battery Capacity: 255 mAH

Real-time clock requirements: 5 µA max. (when Vcc is below acceptable operating limits)

Real-time clock data retention: 10 years min., 30 years typ.

Electrochemical Construction: Poly-carbonmonofluoride

STD Bus Loading Characteristics

The unit load is a convenient method for specifying the input and output drive capability of STD bus cards. With this method, one unit load is equal to one LSTTL load as follows:

- Current for single input load: 20 µA
- Current for single output drive: -400 µA

The unit load reflects current requirements at worst case conditions over the recommended supply voltage and operating temperature ranges. An output drive of 60 unit loads drives 60 STD bus cards having input ratings of one unit load. The "STD Bus Loading, P Connector" table includes load values for STD-80 connections. The "STD Bus Loading, E Connector" table includes load values for STD 32 connections.

STD Bus Loading, P Connector.

PIN (CIRCUIT SIDE) / OUTPUT DRIVE / INPUT LOAD / MNEMONIC							PIN (COMPONENT SIDE) / OUTPUT DRIVE / INPUT LOAD / MNEMONIC
+5 VDC	REQ		2	1		REQ	+5 VDC
GND	REQ		4	3		REQ	GND
DCPDN*		40	6	5	55	1	VBAT (INTRQ4*)
D7/A13 [1]	1	55	8	7	55	1	D3/A19 [1]
D6/A22 [1]	1	55	10	9	55	1	D2/A18 [1]
D5/A21 [1]	1	55	12	11	55	1	D1/A17 [1]
D4/A20 [1]	1	55	14	13	55	1	D0/A16 [1]
A15	1	55	16	15	55	1	A7
A14	1	55	18	17	55	1	A6
A13	1	55	20	19	55	1	A5
A12	1	55	22	21	55	1	A4
A11	1	55	24	23	55	1	A3
A10	1	55	26	25	55	1	A2
A9	1	55	28	27	55	1	A1
A8	1	55	30	29	55	1	A0
RD*	1	55	32	31	55	1	WR*
MEMRQ*	1	55	34	33	55	1	IORQ*
BHE	1	55	36	35	55	1	IOEXP
ALE*	1	55	38	37		1	INTRQ1*
STATUS 0*	1	55	40	39	55	1	STATUS 1*
BUSRQ* [2]	1	55	42	41	55	1	BUSAK* [2]
INTRQ*	1	55	44	43			INTAK*
NMIRQ*	1		46	45		1	WAITRQ*
PBRESET*	1		48	47	55	1	SYSRESET* [3]
INTRQ2* (CNTRL*)	1		50	49	55	1	CLOCK* [3]
PCI [4]	1		52	51			PCO [4]
AUX GND	REQ		54	53		REQ	AUX GND
AUX-V			56	55		REQ	AUX+V [5]

Notes:

REQ indicates required connection.

[1] High order address bits multiplied over the data bus.

[2] BUSRQ* and BUSAK* are bi-directional.

[3] SYSRESET* and CLOCK* are outputs in permanent master configuration and inputs in temporary master configuration.

[4] PCI is connected to PCO.

[5] AUX +V required for flash programming only.

STD Bus Loading, E Connector.

PIN (CIRCUIT SIDE) / OUTPUT DRIVE / INPUT LOAD / MNEMONIC							PIN (COMPONENT SIDE) / OUTPUT DRIVE / INPUT LOAD / MNEMONIC
RSVD			E2	E1			GND
XA23			E4	E3			XA19
XA22			E6	E5			XA18
XA21			E8	E7			XA17
XA20			E10	E9			XA16
RSVD			E12	E11			NOWS*
+5 VDC	REQ		E14	E13		REQ	+5 VDC
DREQx*		55	E16	E15		1	DAKx*
GND	REQ		E18	E17		REQ	GND
D31			E20	E19			D27
D30			E22	E21			D26
D29			E24	E23			D25
D28			E26	E25			D24
GND	REQ		E28	E27			D23
D15	1	55	E30	E29			D22
D14	1	55	E32	E31			D21
D13	1	55	E34	E33			D20
D12	1	55	E36	E35		REQ	GND
D11	1	55	E38	E37			D19
D10	1	55	E40	E39			D18
D9	1	55	E42	E41			D17
D8	1	55	E44	E43			D16
MASTER16*	1	55	E46	E45		REQ	GND
AENx*			E48	E47			IRQx
BE3*			E50	E49			BE1*
BE2*			E52	E51			BE0*
GND	REQ		E54	E53	55	1	MEM16*
W-R			E56	E55			M-IO
DMAIOR*		55	E58	E57	55		DMAIOW*
EX8*			E60	E59		1	IO16*
START*			E62	E61			CMD*
EX32*			E64	E63			EX16*
T-C		55	E66	E65			EXRDY
+5 VDC	REQ		E68	E67		1	INTRQ3*
MREQx*			E70	E69			MAKx*
MSBURST*			E72	E71			SLBURST*
XA31*			E74	E73			XA27*
XA30*			E76	E75			XA26*
XA29*			E78	E77			XA25*
XA28*			E80	E79			XA24*

Note: REQ indicates required connection.

MECHANICAL

The following topics list mechanical specifications, including card dimensions and weight, connectors, and cables.

Card Dimensions and Weight

The ZT 8902 meets the STD-80 Series Bus Specification for all mechanical parameters. In a card cage with 0.625 inch spacing, the ZT 8902 requires one card slot with or without the zVID local bus video adapter installed. The figure "Board Dimensions" shows the mechanical dimensions of the ZT 8902.

Board Length: 16.51±0.063 cm (6.500 ±0.025 inches)

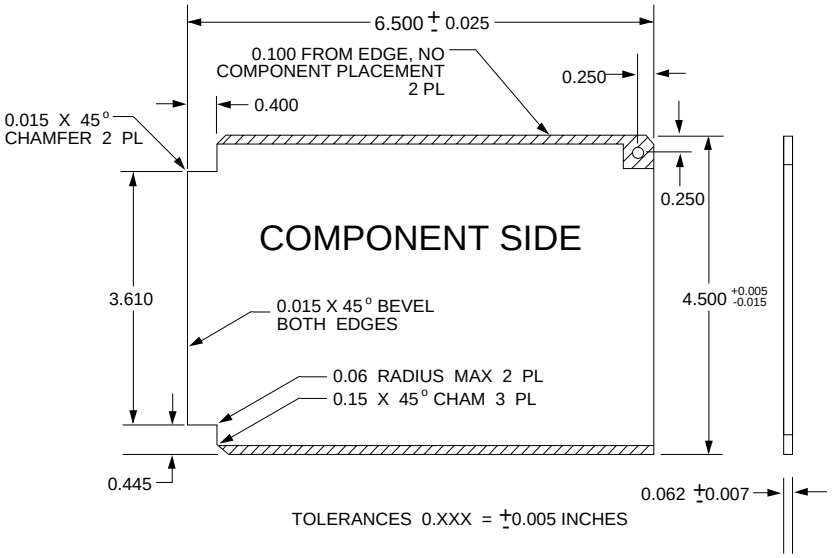
Board Width: 11.43±0.038 cm (4.500 ±0.015 inches)

Board Thickness: 0.158 ±0.013 cm (0.062 ±0.005 inches)

Board Weight: 200 grams (7 ounces)

Board Height From Top Surface: 1.27 cm (0.5 inches)

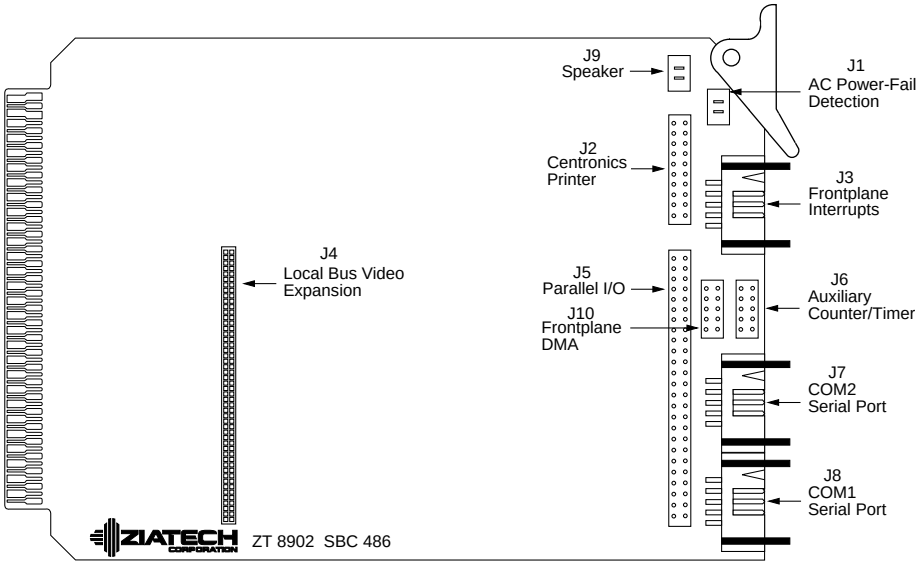
Board Height From Bottom Surface: 0.18 cm (0.07 inches)



Board Dimensions.

Connectors

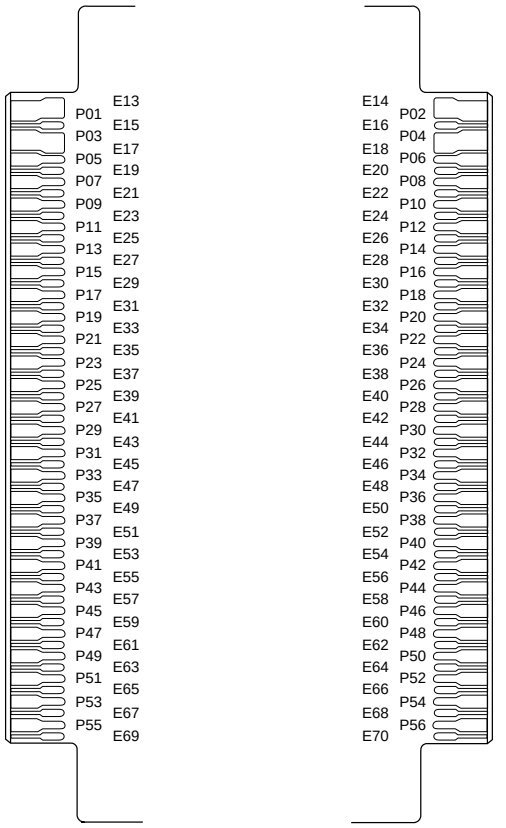
The ZT 8902 includes 12 connectors to interface to the STD bus and to application-specific devices. A description and pin map for each connector is given below.



Connector Locations.

P: The P connector is the interface between the ZT 8902 and the STD-80 bus. This connector is a 56-pin (dual 28-pin) card-edge connector with fingers on 0.125 inch contact spacing. The mating connector is a Viking 3VH28/1CNK5 or equivalent for the solder tail, or a Viking 3VH28/1CND5 or equivalent for a three-level wire wrap. The "P/E Connector Pinout" illustration shows pin assignments for the P connector, and the "STD Bus Loading, P Connector" table shows signal assignments.

E: The E connector extends the P connector to interface the ZT 8902 to the STD 32 bus. This connector combines with the P connector to make a 114-pin (dual 57-pin) card-edge connector with fingers on 0.0625 inch contact spacing. The mating connector is a Viking S3VT68/5DP12 or equivalent for the solder tail, or a Viking S3VT68/5DE12 or equivalent for the card extender. The "P/E Connector Pinout" illustration shows pin assignments for the E connector, and the "STD Bus Loading, E Connector" table shows signal assignments.



P/E Connector Pinout.

J1: J1 is a latching 2-pin male low-profile header with 0.1 inch contact spacing. The AC input signals for the optional power-fail detection feature are available through this connector. The pin assignments are given in the "J1 AC Power-Fail Pinout" table. The mating connector is a Molex 39-01-0023 or equivalent. The mating connector also requires two Molex 39-01-0031 terminals or equivalent.

J1 AC Power-Fail Pinout.

Pin #	Signal	Type	Description
1	AC1	In	AC 1
2	AC2	In	AC2

J2: J2 is a 20-pin (dual 10-pin) vertical male header with 0.1 inch contact spacing. This connector includes the standard Centronics printer control and data signals. The pin assignments are given in the "J2 Centronics Printer Pinout" table. The mating connector is a T&B Ansley #622-2030 or equivalent.

J2 Centronics Printer Pinout.

Pin #	Signal	Type	Description
1	STB*	Out	Data strobe
2	AFD*	Out	Autofeed
3	PD0	In/out	Data bit 0
4	ERR*	In	Error
5	PD1	In/out	Data bit 1
6	INIT*	Out	Initialize
7	PD2	In/out	Data bit 2
8	SLIN*	Out	Select to printer
9	PD3	In/out	Data bit 3
10	GND	------	Ground
11	PD4	In/out	Data bit 4
12	GND	------	Ground
13	PD5	In/out	Data bit 5
14	GND	------	Ground
15	PD6	In/out	Data bit 6
16	BUSY	In	Printer busy
17	PD7	In/out	Data bit 7
18	PE	In	Paper error
19	ACK*	In	Acknowledge
20	SLCT	In	Select from printer

J3: J3 is a latching 10-pin (dual 5-pin) male transition connector with 0.1 inch contact spacing. Frontplane interrupts are available through this connector. The pin assignments are given in the "J3 Frontplane Interrupt Pinout" table. The mating connector is a T&B Ansley #622-1030 or equivalent.

J3 Frontplane Interrupt Pinout.

Pin #	Signal	Type	Description
1	GND	------	Ground
2	FP1*	In	Interrupt level 9
3	GND	------	Ground
4	FP3*	In	Interrupt level 3
5	GND	------	Ground
6	FP5*	In	Interrupt level 5
7	GND	------	Ground
8	FP6*	In	Interrupt level 6
9	GND	------	Ground
10	FP7*	In	Interrupt level 7

Notes:

1. The interrupt levels shown are the most common configuration. Refer to the "Interrupt Architecture" figure in Chapter 4, "Interrupt Controller," for other possibilities.
2. The frontplane interrupts are active low inputs that are routed through an inverter before being applied to the interrupt controller.

J4: J4 is a 100-pin (dual 50-pin) vertical receptacle with 0.050 inch contact spacing. This connector includes the signals needed for a local bus interface. This interface is used by optional piggyback adapters, such as the zVID1 Local Bus VGA Video Adapter. The pin assignments are given in the "J4 Local Bus Pinout" table. The mating connector is an AMP 1-104655-1 (0.250 inch mated height), 1-10456-0 (0.320 inch mated height), or 1-104693-0 (0.390 inch mated height).

J4 Local Bus Pinout.

Pin #	Signal	Type	Description	Pin #	Signal	Type	Description
1	VCC	-----	+5 Volts	51	D12	In/Out	CPU Data
2	VCC	-----	+5 Volts	52	D13	In/Out	CPU Data
3	A02	Out	CPU Address	53	D14	In/Out	CPU Data
4	GND	-----	Ground	54	D15	In/Out	CPU Data
5	A04	Out	CPU Address	55	D16	In/Out	CPU Data
6	A03	Out	CPU Address	56	D17	In/Out	CPU Data
7	A06	Out	CPU Address	57	D18	In/Out	CPU Data
8	A05	Out	CPU Address	58	VCC	-----	+5 Volts
9	A08	Out	CPU Address	59	D20	In/Out	CPU Data
10	A07	Out	CPU Address	60	D19	In/Out	CPU Data
11	GND	-----	Ground	61	D22	In/Out	CPU Data
12	A09	Out	CPU Address	62	D21	In/Out	CPU Data
13	A10	Out	CPU Address	63	D24	In/Out	CPU Data
14	A11	Out	CPU Address	64	D23	In/Out	CPU Data
15	A12	Out	CPU Address	65	GND	-----	Ground
16	A13	Out	CPU Address	66	D25	In/Out	CPU Data
17	A14	Out	CPU Address	67	D26	In/Out	CPU Data
18	A15	Out	CPU Address	68	D27	In/Out	CPU Data
19	A16	Out	CPU Address	69	D28	In/Out	CPU Data
20	A17	Out	CPU Address	70	D29	In/Out	CPU Data
21	A18	Out	CPU Address	71	D30	In/Out	CPU Data
22	GND	-----	Ground	72	D31	In/Out	CPU Data
23	A20	Out	CPU Address	73	*BE0	Out	Byte Enable
24	A19	Out	CPU Address	74	GND	-----	Ground
25	A22	Out	CPU Address	75	*BE1	Out	Byte Enable
26	A21	Out	CPU Address	76	*SLCT	In	Module Select
27	A24	Out	CPU Address	77	*BE2	Out	Byte Enable
28	A23	Out	CPU Address	78	*PRES	In	Module Present
29	VCC	-----	+5 Volts	79	*BE3	Out	Byte Enable
30	A25	Out	CPU Address	80	*RDY	In	Ready
31	A26	Out	CPU Address	81	GND	-----	Ground
32	A27	Out	CPU Address	82	*BRDY	In	Burst Ready
33	A28	Out	CPU Address	83	ADS	Out	Address Status
34	A29	Out	CPU Address	84	*BLAST	Out	Burst Last
35	A30	Out	CPU Address	85	M/I	Out	Memory/IO
36	A31	Out	CPU Address	86	*LBA	In	Local Bus Ack.
37	D00	In/Out	CPU Data	87	W/R	Out	Write/Read
38	GND	-----	Ground	88	*KEN	Out	Cache Enable
39	D02	In/Out	CPU Data	89	D/C	Out	Data/Control
40	D01	In/Out	CPU Data	90	*VIDEN	Out	Video Enable
41	D04	In/Out	CPU Data	91	RESET	Out	CPU Reset
42	D03	In/Out	CPU Data	92	KBD	Out	Keyboard Data
43	D06	In/Out	CPU Data	93	RSVD	-----	Reserved
44	D05	In/Out	CPU Data	94	KBC	Out	Keyboard Clock
45	D08	In/Out	CPU Data	95	GND	-----	Ground
46	D07	In/Out	CPU Data	96	GND	-----	Ground
47	GND	-----	Ground	97	CLK14	Out	14.318 MHz Clock
48	D09	In/Out	CPU Data	98	CLK	Out	CPU Clock
49	D10	In/Out	CPU Data	99	VCC	-----	+5 Volts
50	D11	In/Out	CPU Data	100	VCC	-----	+5 Volts

J5: J5 is a 50-pin (dual 25-pin) vertical male header with 0.1 inch contact spacing. The parallel I/O signals are included in this connector. The pin assignments are given in the "J5 Parallel I/O Pinout" table. The pin assignments are chosen for direct connection to an I/O module mounting rack, such as those offered by Ziatech (ZT 2226) and Opto 22. The mating connector is a T&B Ansley #622-5030 or equivalent.

J5 Parallel I/O Pinout.

Pin #	Signal	Type	Description	Pin #	Signal	Type	Description
1	MOD23	In/Out	Port E2, bit 7	26	GND	-----	Ground
2	GND	-----	Ground	27	MOD10	In/out	Port E1, bit 2
3	MOD22	In/Out	Port E2, bit 6	28	GND	-----	Ground
4	GND	-----	Ground	29	MOD09	In/Out	Port E1, bit 1
5	MOD21	In/Out	Port E2, bit 5	30	GND	-----	Ground
6	GND	-----	Ground	31	MOD08	In/Out	Port E1, bit 0
7	MOD20	In/Out	Port E2, bit 4	32	GND	-----	Ground
8	GND	-----	Ground	33	MOD07	In/Out	Port E0, bit 7
9	MOD19	In/Out	Port E2, bit 3	34	GND	-----	Ground
10	GND	-----	Ground	35	MOD06	In/Out	Port E0, bit 6
11	MOD18	In/Out	Port E2, bit 2	36	GND	-----	Ground
12	GND	-----	Ground	37	MOD05	In/Out	Port E0, bit 5
13	MOD17	In/Out	Port E2, bit 1	38	GND	-----	Ground
14	GND	-----	Ground	39	MOD04	In/Out	Port E0, bit 4
15	MOD16	In/Out	Port E2, bit 0	40	GND	-----	Ground
16	GND	-----	Ground	41	MOD03	In/Out	Port E0, bit 3
17	MOD15	In/Out	Port E1, bit 7	42	GND	-----	Ground
18	GND	-----	Ground	43	MOD02	In/Out	Port E0, bit 2
19	MOD14	In/Out	Port E1, bit 6	44	GND	-----	Ground
20	GND	-----	Ground	45	MOD01	In/Out	Port E0, bit 1
21	MOD13	In/Out	Port E1, bit 5	46	GND	-----	Ground
22	GND	-----	Ground	47	MOD00	In/Out	Port E0, bit 0
23	MOD12	In/Out	Port E1, bit 4	48	GND	-----	Ground
24	GND	-----	Ground	49	VCC	-----	+5 V
25	MOD11	In/Out	Port E1, bit 3	50	GND	-----	Ground

J6: J6 is a 10-pin (dual 5-pin) vertical male header with 0.1 inch contact spacing. The auxiliary counter/timer input, output, and control signals are available through this connector. The pin assignments are shown in the "J6 Auxiliary Counter/Timer Pinout" table. The mating connector is a T&B Ansley #622-1000 or equivalent. The polarization tab is not used on this mating connector since it would interfere with a mating connector plugged into J10.

J6 Auxiliary Counter/Timer Pinout.

Pin #	Signal	Type	Description
1	CLK0	In	Counter/timer 0 clock
2	CTL0	In	Counter/timer 0 control
3	OUT0	Out	Counter/timer 0 output
4	CLK1	In	Counter/timer 1 clock
5	CTL1	In	Counter/timer 1 control
6	GND	-----	Ground
7	OUT1	Out	Counter/timer 1 output
8	CLK2	In	Counter/timer 2 clock
9	CTL2	In	Counter/timer 2 control
10	OUT2	Out	Counter/timer 2 output

J7, J8: J7 and J8 are each latching 10-pin (dual 5-pin) male transition connectors with 0.1 inch contact spacing. These connectors include the RS-232 serial interface signals for COM2 and COM1, respectively. The pin assignments are included in the "J7 and J8 Serial I/O Pinout" table. The mating connector is a T&B Ansley #622-1030 or equivalent.

J7 and J8 Serial I/O Pinout.

Pin #	Signal	Type	Description
1	DCD	In	Data carrier detect
2	DSR	In	Data set ready
3	RXD	In	Receive data
4	RTS	Out	Request to send
5	TXD	Out	Transmit data
6	CTS	In	Clear to send
7	DTR	Out	Data terminal ready
8	RI	In	Ring indicator
9	GND	----	Signal ground
10	VCC	----	+5 V

J9: J9 is a latching 2-pin male low-profile header with 0.1 inch contact spacing. The speaker signals are available through this connector. The pin assignments are given in the "J9 Speaker Pinout" table. The mating connector is a Molex 39-01-0023 or equivalent. The mating connector also requires two Molex 39-01-0031 terminals or equivalent.

J9 Speaker Pinout.

Pin #	Signal	Type	Description
1	SP1	Out	Speaker output
2	VCC	----	+5V

J10: J10 is a 10-pin (dual 5-pin) vertical male header with 0.1 inch contact spacing. Two frontplane DMA channels are available through this connector. The pin assignments are given in the "J10 Frontplane DMA" table. The mating connector is a T&B Ansley #622-1000 or equivalent. The polarization tab is not used on this mating connector since it would interfere with a mating connector plugged into J5.

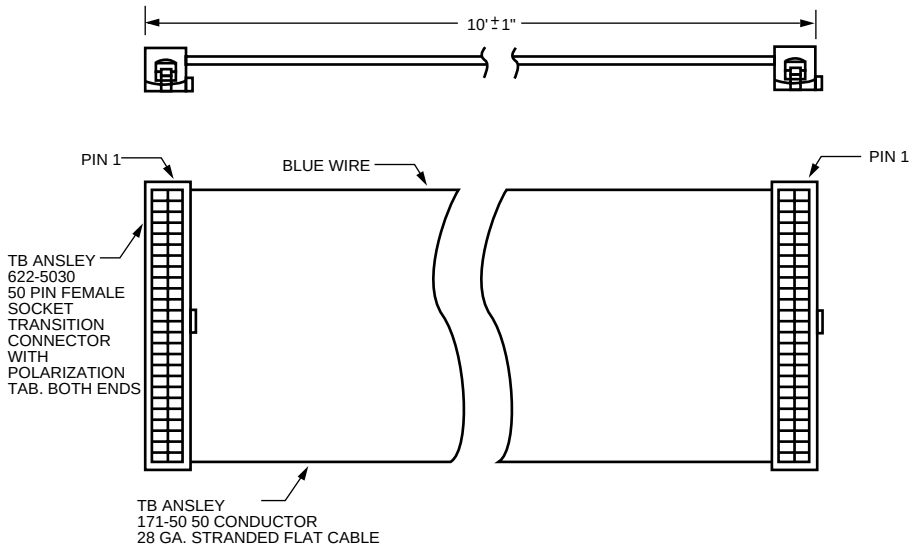
J10 Frontplane DMA Pinout.

Pin #	Signal	Type	Description
1	DRQ0/5*	In	DMA request 0 or 5
2	DRQ1/6*	In	DMA request 1 or 6
3	DAK0/5*	Out	DMA acknowledge 0 or 5
4	DAK1/6*	Out	DMA acknowledge 1 or 6
5	Reserved	----	No connection
6	DMAIOW*	Out	I/O write
7	Reserved	----	No connection
8	DMAIOR*	Out	I/O read
9	GND	----	Ground
10	TC*	Out	Terminal count

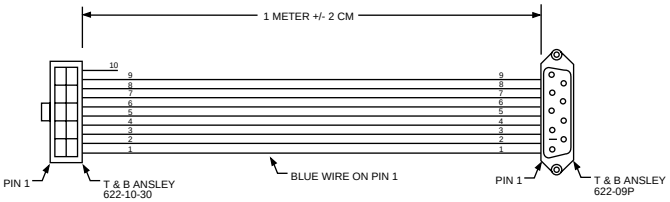
Notes:
1. Channel selection is made with cuttable traces.
2. DMAIOW* and DMAIOR* must be qualified by the respective DMA acknowledge by the DMA I/O slave.

Cables

The following cables are available from Ziatech Corporation. They are included here for those who wish to make their own cables:



ZT 90072 Rev. A Digital I/O Cable.

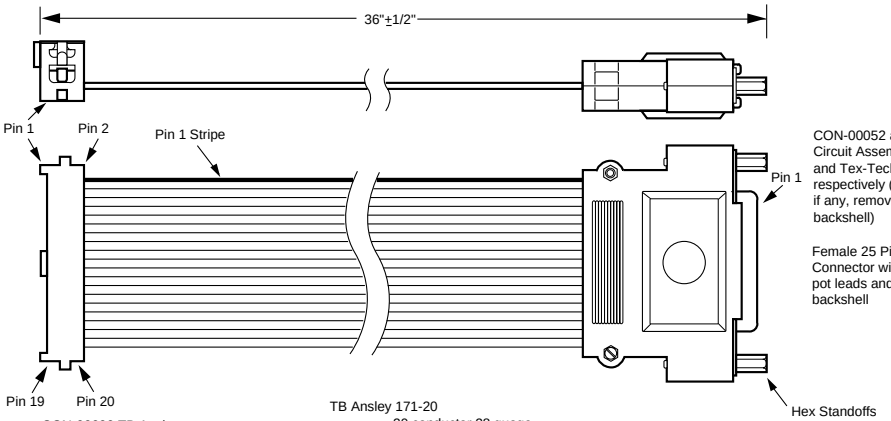


1. TRIM ALL CABLE ENDS FLUSH WITH CONNECTOR BODIES.
2. USE T & B ANSLEY #171-10 STRANDED 28 AWG RIBBON CABLE.
3. ZIATECH APPROVAL REQUIRED FOR PARTS SUBSTITUTIONS.

CONNECTION TABLE

622-10-30	622-09P
10	NA
9	5
8	9
7	4
6	8
5	3
4	7
3	2
2	6
1	1

ZT 90136 Rev. 0 Serial Cable.

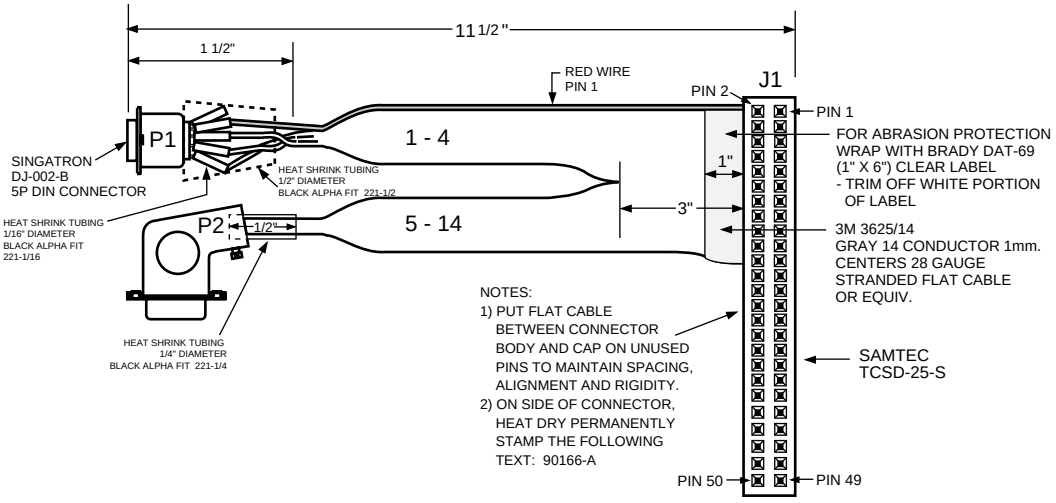


Pin Assignment Chart

Wire No.	25 Pin D Pin No	Wire No.	25 Pin D Pin No
1	1	11	6
2	14	12	21-23 *
3	2	13	7
4	15	14	24-25 *
5	3	15	8
6	16	16	11
7	4	17	9
8	17	18	12
9	5	19	10
10	18-20 *	20	13

Note: *Pins 18-25 are tied in common

ZT 90157 Rev. A Printer Cable.



ZT 90166 Rev. A Video/Keyboard Cable.

APPENDIX C. PARALLEL I/O CONSIDERATIONS

The 16C50A Parallel Interface Adapter (PIA) device used on the ZT 8902 is designed by Ziatech to offer bidirectional I/O signals with or without event sense capability. This device features low power, high speed, wide temperature operation achievable only by utilizing CMOS technology.

Although CMOS technology offers many advantages, you must observe a few cautions when interfacing to any CMOS parts.

- CMOS inputs and outputs can exhibit latchup characteristics. These inherent characteristics of any CMOS technology can result in the formation of a Silicon-Controlled Rectifier (SCR) that appears between Vcc and ground when voltages greater than Vcc or less than ground are applied to inputs or outputs. When this happens, Vcc is effectively shorted to ground. The only way to remove the latchup condition is to shut off the power supply. If a large current is allowed to flow through the chip, its operating temperature may increase, it may exhibit intermittent operation, or it may be damaged.
- CMOS inputs must be protected from slow rising signals and inductive coupling on their inputs. Failure to do so will allow a potentially large current to flow through the chip, damaging the chip.

The purpose of this appendix is to illustrate precautions you should take to prevent latchup conditions and protect inputs.

PREVENTING SYSTEM LATCHUP

The most common causes of latchup are:

- Input signals applied before the input circuitry is powered, resulting in a signal to power supply sequence mismatch
- Input signals greater than Vcc or less than ground, resulting in a signal level mismatch

Each of these conditions is covered in the following topics.

Power Supply Sequence Mismatch

A common application is to interface to a 24-position ZT 2226, Opto 22, or equivalent I/O module rack. Vcc and ground are provided from the ZT 8902 through connector J5, with Vcc protected by a 1 A fuse. (See the "J5 Parallel I/O Pinout" table in Appendix B, "Specifications," for the J5 pinout.) This application is illustrated in Figure 1. In this application, no power supply sequence mismatch exists because the power supplying the input circuitry within the PIA is applied before or at the same time as the power supplying the external signals. Proper system operation will result.

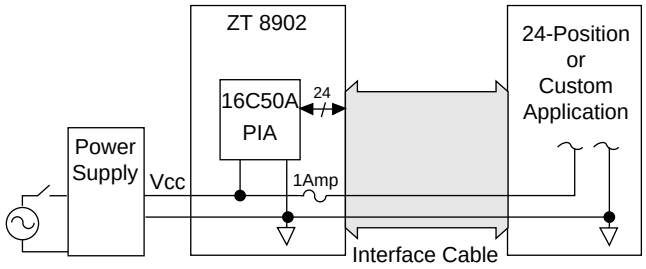


Figure 1. I/O Rack Vcc and Ground Supplied Via Interface Cable. Correct Power Supply Sequence, Signal Level Matched.

However, if a power source other than that supplying the PIA is used to power the external signals, then a power sequence mismatch could occur, resulting in a latchup condition. An external power source might be required if the external circuitry requires more than the 1 A supplied by the cable or if a custom interface is being designed (see Figure 2).

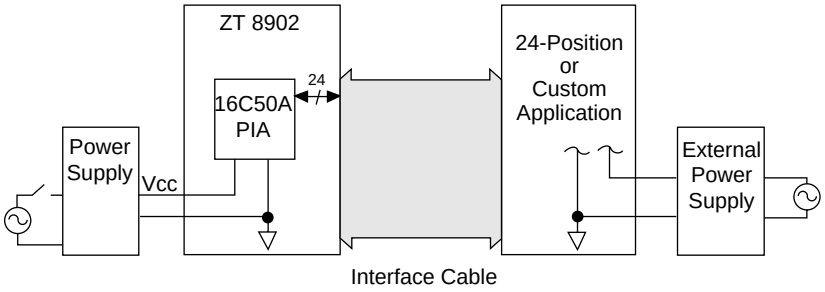


Figure 2. I/O Rack Vcc and Ground Supplied Externally.
Potential Power Supply Sequence Mismatch, Signal Level Mismatch.

One solution is to switch the external signals' power supply with an output that is controlled by the computer. In this manner, if the computer is off, so is the external power supply. This solution is illustrated in Figure 3.

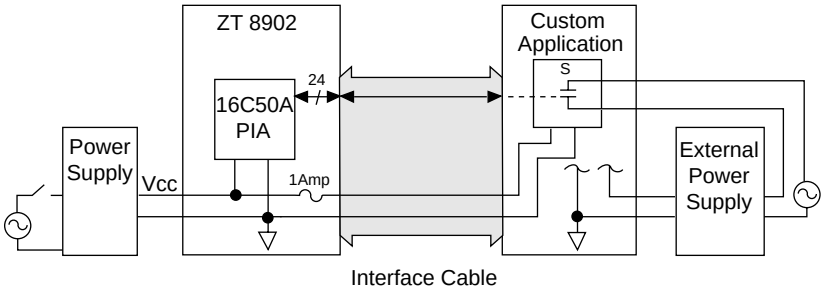


Figure 3. Computer-Switched External Power Supply.
Correct Power Supply Sequence, Potential Signal Level Mismatch.

A simpler solution is to power the relay controlling the external power supply directly from Vcc and ground supplied by the interface cable.

Another solution is to utilize the same switch to control the computer's power supply and the external signals' power supply (see Figure 4). This is an acceptable solution for power supply sequence mismatches as long as the computer supply ramps up faster than the external power supply. This ensures the PIA input circuitry is powered before the external signal circuitry.

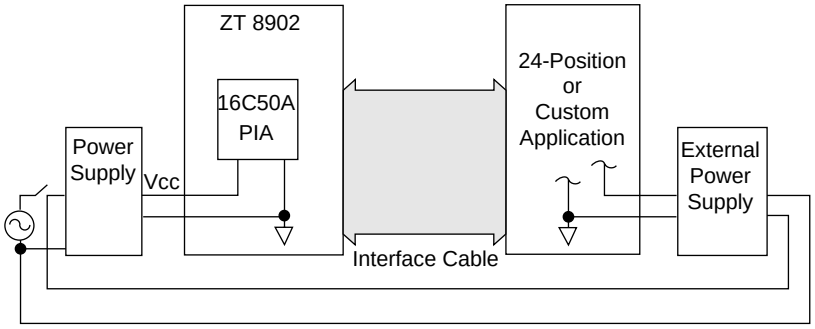


Figure 4. Computer & Ext. Power Supply w/ Common Switch.
Correct Power Supply Sequence, Potential Signal Level Mismatch.

Signal Level Mismatch

Power supplying the external signal in Figure 1 is always relative to the PIA input circuitry power because power is provided over the interface cable. Signal level mismatches will not occur and proper system operation will result. However, if separate power supplies are used, there are two predominant causes of signal level mismatches.

The first (assuming no sequencing problems) occurs when the two supplies are not referenced to each other, as illustrated in Figures 2, 3, and 4. This results in signals that may be higher than Vcc or lower than ground, potentially causing SCR latchup. All that is generally needed is to reference one supply to the other, typically by connecting a common ground. The most convenient way of connecting a common ground is to use the interface cable. Figures 5, 6, and 7 illustrate correct ground connections.

The second cause of mismatch occurs when the two power supplies are referenced to each other but the Vcc difference between the two power supplies exceeds .5 V. This results in signals that could be greater than Vcc, causing SCR latchup. This is easily remedied by adjusting the external power supply voltage to be within .5 V of the computer power supply voltage.

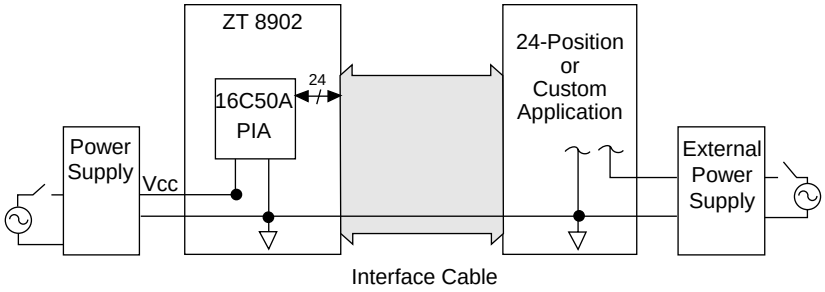


Figure 5. I/O Rack Vcc Supplied Externally, Common Ground. Potential Power Supply Seq. Mismatch, Correct Signal Level Match.

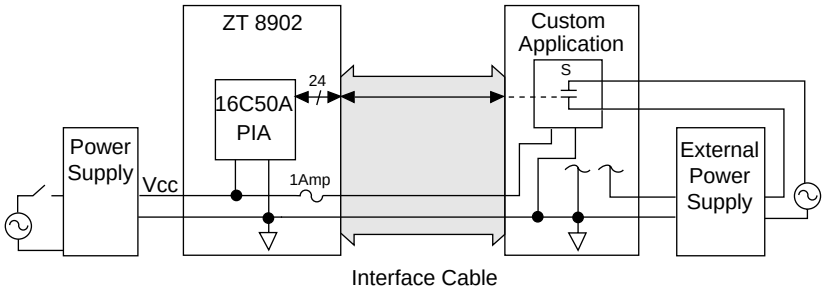


Figure 6. Computer-Switched External PS, Common Ground. Correct Power Supply Sequence, Correct Signal Level Match.

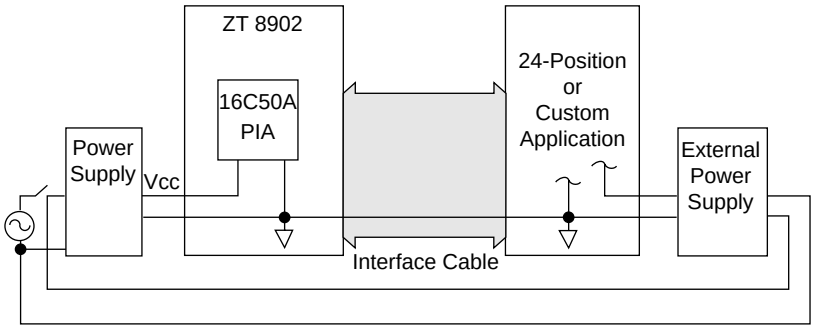


Figure 7. Computer & External PS w/ Common Switch & Ground. Correct Power Supply Sequence, Correct Signal Level Match.

PROTECTING CMOS INPUTS

The most common causes of damaged inputs are:

- Slow rise times, resulting in a ground bounce within the chip
- Inductive coupling on I/O lines causing noise to be coupled into the chip, resulting in intermittent operation

Each of these conditions is covered in the following topics.

Rise Times

Slow rise times on a CMOS input can easily cause the transistor to bounce between Vil and Vih. When this oscillation occurs, the operating current goes up, resulting in "ground bounce." Ground bounce can cause internal latchup or can cause other system components to malfunction. A pullup termination resistor is used to increase the rise time.

Input rise times must be kept to less than 50 ns. Given a maximum chip capacitance of 10 pF, a 5 k Ω resistor is the largest that could be used without additional cabling. As cabling is added, the capacitance goes up, resulting in the use of a smaller pullup resistor until the maximum sink current of the output is achieved.

If the 16C50A PIA device is driving the output, its maximum sink current at a Vol of .4 V is 12 mA. This gives a lower limit of 420 ohms for the pullup resistor, allowing a maximum cabling capacitance of 110 pF. Note that while the input feature of the PIA may not be used by your application (PIA used as an output only), the input circuitry remains in parallel; therefore, the output rise time is still a critical parameter that the input still sees. The output rise time must not exceed 50 ns.

Be wary of using low pass filters to remove electrical noise. The resulting capacitance is typically too large to meet the 50 ns rise time requirement.

Typically, optical isolators are used to help remove electrical noise while providing for different grounds. Separate grounds are achieved through the use of an additional power supply for the optocoupler rather than using the computer's power supply. If the computer's power supply powers the optocouplers, electrical isolation is defeated. An example of one such circuit is illustrated in Figure 8. The circuit can be altered to allow for design considerations.

Assuming a Vil of 1 V maximum for the 16C50A PIA, the HP Dual Optocoupler must have a Vol of less than or equal to 1 V over the operating temperature. Using a TTL-compatible optocoupler gives a Vol of .6 V maximum with rise and fall times (50 ns and 10 ns, respectively) that are easily compatible with the PIA, given a 1 k ohm pullup.

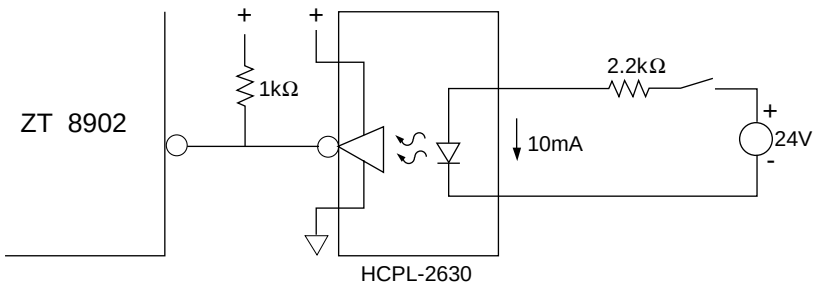


Figure 8. PIA-to-Optocoupler Interface Example.

Inductive Coupling

Inductive coupling on I/O lines can cause noise to be coupled into the chip, resulting in intermittent operation. This situation occurs when the PIA I/O signals are routed with other signals within a wire bundle. One way to filter inductively coupled noise, or any noise for that matter, within a system with the same ground (not using optocouplers) is illustrated in Figure 9.

In the above circuit, the Texas Instruments 74S1053 Schottky diode clamps limit a transient to ±1 V above +5 V or below ground. The ferrite bead has a 50 ohm impedance at the frequency of interest. As the diodes begin to clamp and current flows through them, the voltage across the LCA05 5 V bidirectional TransZorbs® increases, causing them to conduct and allowing the majority of energy to flow through them instead of through the diode clamps. The 39 pF capacitor, in conjunction with the ferrite bead, forms an additional low pass filter, and is entirely optional. The 1 k ohm pullup ensures adequate rise time on the signal. The fuse acts as additional insurance against catastrophic events that might destroy the TransZorb and diode clamps.

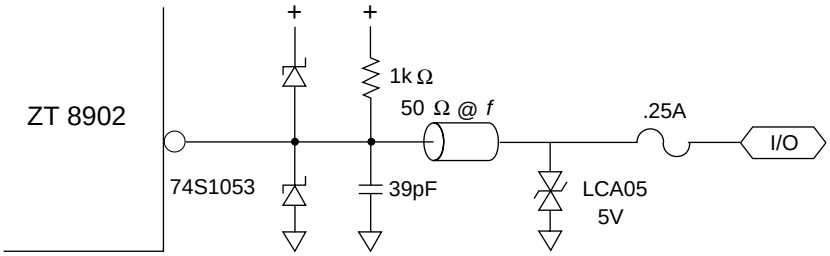


Figure 9. PIA-to-Filter Interface Example.

ADDITIONAL INFORMATION

You can find additional design information in the Advanced CMOS Logic Designer's Handbook, published by Texas Instruments.

APPENDIX D. CUSTOMER SUPPORT

This appendix offers a product revision history, technical support information, the Ziatech warranty, and instructions for returning the ZT 8902 if service is necessary.

REVISION HISTORY

Revision 0--Original Beta Site Release, 10/20/92

A limited number of these boards were produced, and they were updated to Revision 0.1 upon completion of the beta testing.

Revision 0.1--Initial Production Release, 2/15/93

The functional differences between Rev 0.1 and Rev 0 are listed below.

- Added complete multiple master support.
- Eliminated the requirement for jumper W2. W2 is now reserved for Ziatech use and must be installed in position A.
- Eliminated the requirement for jumper W3. W3 is now reserved for Ziatech use and must be installed in position A.
- Eliminated the requirement for cuttable trace CT11. CT11 is now reserved for Ziatech use.
- Changed the factory default settings for cuttable traces CT12, CT15, and CT16. These cuttable traces are now installed at the factory, connecting an 8 MHz signal as the clocking source for the auxiliary timer.

Revision A--5/15/93

The functional differences between Rev A and Rev 0.1 are listed below.

- Moved the J4 local bus connector up 0.1 inches to eliminate interference between piggyback zVID adapters and the adjacent card guide.
- Added connector J9 to provide a speaker interface.
- Added a MOSFET switch to gate +12 V to the Flash devices under program control.
- Added a jumper option to connect the multiple master interrupt through STD bus INTRQ4*.
- Added an inverter between the real-time clock and the interrupt controller to support real-time clock interrupts.
- Modified the bus exchange (BUSRQ*/BUSAK*) protocol to support floppy disk controllers as DMA slaves. This moves the DMA controller from the floppy disk board to the ZT 8902 for compatibility with applications such as Windows SMARTDRV. This modification eliminates support for the ZT 8950 floppy disk controller and adds support for the ZT 8954 floppy disk controller.
- Added connector J10 to provide two frontplane DMA channels for data transfers between STD bus DMA slaves and local memory.

Revision A.1--10/5/93

The functional differences between Rev A.1 and Rev A are listed below.

- Added a 10 k Ω pullup resistor to the LOCK* net for improved termination to the LOCK* signal between the i486 CPU and the chipset.
- Replaced PALSM-40043B with PALSM-40043C to prevent contention during the fetch of the boot vector after CPU reset.

Revision A.2--11/22/93

The functional differences between Rev A.2 and Rev A.1 are listed below.

- Added a 4.75 k ohm pullup resistor to the ASIC WDE* signal to prevent spurious resets generated by the watchdog/timer circuit.

Revision A.3--4/7/94

The functional differences between Rev A.3 and Rev A.2 are listed below.

- Changed the backplane pullup resistor from 4.75 k ohm to 1.8 k ohm to prevent application software from attempting to read nonexistent memory or I/O mapped on the backplane.
- Modified the MEM16* 74BCT125 driver circuit. This change is required in a STAR SYSTEM environment when a CPU performs transfers to a 16-bit backplane memory device and a ZT 8902 performs floppy (or other type of DMA) transfers at the same time. The ZT 8902 would drive MEM16* for the duration of its INT 13h and contend with the MEM16* requirements of the CPU talking to the 16-bit memory device.

Revision B--1/10/95

The functional differences between Rev B and Rev A.3 are listed below.

Revision B provides support for the following:

- 3.3 V 486DX4-100 CPUs
- Selection of the external counter/timer clock
- 16C50A digital ASIC
- IR15 selection (ASIC or CTOUT2)
- DRAM sockets with a center post
- A clearance area around the CPU for extraction tools

TECHNICAL ASSISTANCE

If you have a technical question, please call Ziatech's Customer Support Service at the number below, or e-mail our technical support team at *tech_support@ziatech.com*. Ziatech also maintains an FTP site located at *ftp.ziatech.com*.

If you have a sales question, please contact your local Ziatech Sales Representative or the Regional Sales Office for your area. Address, telephone and FAX numbers, and additional information is available at Ziatech's website, located at *http://www.ziatech.com*.

Corporate Headquarters

1050 Southwood Drive
San Luis Obispo, CA 93401 USA
Tel (805) 541-0488
FAX (805) 541-5088

HOW RELIABILITY IS ACHIEVED

Ziatech has taken extra care in the design of the ZT 8902 to ensure reliability. The three major ways in which reliability is achieved are:

1. The product was designed in top-down fashion, utilizing the latest in hardware and software design techniques, so that unwanted side effects and unclean interactions between parts of the system have been eliminated.
2. Ziatech tests each board by exercising its functions, burns it in under power, and retests it to ensure that the infant mortality phase is passed before the product is shipped.
3. Each ZT 8902 has an identification number and Ziatech maintains a lifetime data base on each one and on the parts used. Any negative trends in reliability are spotted and Ziatech's suppliers are informed and/or changed.

RETURNING THE ZT 8902 FOR SERVICE

Before returning any of Ziatech's products, you must obtain a Return Material Authorization (RMA) number by calling (805) 541-0488. We need the following information to expedite shipment of the repaired product or replacement to you:

1. Your company name and address for invoice
2. Shipping address and phone number
3. Product I.D. number
4. If possible, the name of technically qualified individual at your company familiar with the mode of failure on the board

If the unit is out of warranty, service is available at a predesignated service charge. Contact Ziatech for pricing and supply a purchase order number for invoicing the repair.

Pack the ZT 8902 in ***anti-static*** material and ship in a sturdy cardboard box with enough packing material to adequately cushion the board. ***Any product improperly packed will immediately void the warranty for that particular product!*** Mark the RMA number clearly on the outside of the box before shipping.

ZIATECH 5+5 WARRANTY

Ziatech provides a five year limited warranty to its customers with a special extended warranty option. Ziatech also has an explicit policy regarding the use of Ziatech products in life support systems. These topics are covered in the following sections.

Five-Year Limited Warranty

Products manufactured by Ziatech Corporation are covered from the date of purchase by a five-year warranty against defects in materials, workmanship, and published specifications applicable to the date of manufacture. During the warranty period, Ziatech will repair or replace, solely at its option, defective units provided they are returned at customer expense to an authorized Ziatech repair facility. Products which have been subjected to misuse, abuse, neglect, alteration, or unauthorized repair, determined at the sole discretion of Ziatech, whether by accident or otherwise, are excluded from warranty. The warranty on fans and disk drives is limited to two years and the warranty on flat panel displays is limited to nine months from date of purchase. Other products and accessories not manufactured by Ziatech are limited to the warranty provided by the original manufacturer. Consumable items (fuses, batteries, etc.) and software are not covered by this warranty.

Ziatech Corporation warrants that for a period of ninety (90) days from the date of purchase; the media on which software is furnished will be free of defects in materials and workmanship under normal use; and the software contains the features described in the Ziatech price list. Otherwise, the software is provided "AS IS". This limited warranty extends only to Customer as the original licensee. Customer's exclusive remedy and Ziatech's entire liability under this limited warranty will be, at Ziatech's option, to repair or replace the software, or refund the license fee paid therefore.

Ziatech may offer, where applicable and available, replacement products; otherwise, repairs requiring components, assemblies, and other purchased materials may be limited by market availability.

Ziatech assumes no liability resulting from changes to government regulations affecting use of materials, equipment, safety, and methods of repair. Ziatech may, at its discretion, offer replacement products.

THE ABOVE WARRANTY IS IN LIEU OF ANY OTHER WARRANTY, WHETHER EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING, BUT NOT LIMITED TO, ANY WARRANTY FOR FITNESS OF PURPOSE, MERCHANTABILITY, OR FREEDOM FROM INFRINGEMENT OR THE LIKE, AND ANY WARRANTY OTHERWISE ARISING OUT OF ANY PROPOSAL, SPECIFICATIONS, OR SAMPLE.

Ziatech neither assumes nor authorizes any person to assume for it any other liability. The liability of Ziatech under this warranty agreement is limited to a refund of the purchase price. In no event shall Ziatech be liable for loss of profits, use, incidental, consequential, or other damage, under this agreement.

Special Extended Warranty Option

In addition to the standard five-year warranty, Ziatech offers, for a nominal fee, an extended period of warranty up to five extra years. This extended warranty period provides similar coverage and conditions as stated above in the five-year limited warranty agreement.

Life Support Policy

Ziatech products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Ziatech Corporation. As used herein:

1. Life support devices or systems are devices or systems which support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be expected to cause the failure of the life support device or system, affect its safety, or limit its effectiveness.

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