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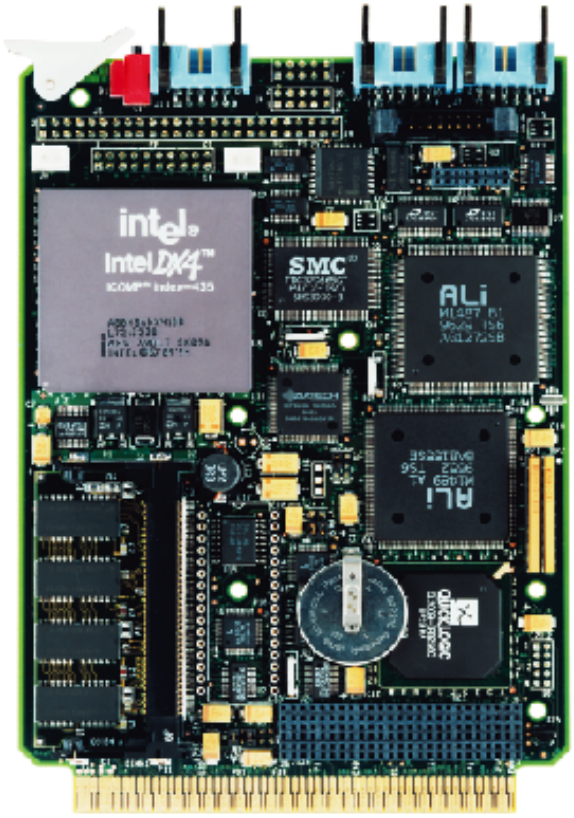
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ZT 8907



Single Board Computer
with IntelDX4™ Microprocessor

Hardware User Manual

ZIATECH
CORPORATION

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MANUAL ORGANIZATION

This manual describes the operation and use of the ZT 8907 Single Board Computer with IntelDX4™ Microprocessor. The following summarizes the focus of each major section in this manual.

Chapter 1, "Introduction," introduces the key features of the ZT 8907. It includes a product definition, a list of product features, a functional block diagram, and a description of each block.

Chapter 2, "Getting Started," provides a summary of the information needed to install and configure your ZT 8907.

Chapter 3, "STD Bus Interface," presents a detailed description of the ZT 8907 interface to the STD-80 and STD 32 bus architectures. The topics discussed include compatibility, interrupt structure, and multiple master operation.

Chapter 4, "Interrupt Controller," describes the two Intel-compatible 8259 cascaded interrupt controllers. This chapter summarizes the interrupt sources and the interrupt controllers' register addressing.

Chapter 5, "Counter/Timers," discusses the six programmable counter/timers. It includes a diagram of the counter/timer architecture, and a summary of the operating modes and the programmable registers.

Chapter 6, "DMA Controller," provides an overview of ZT 8907 DMA architecture and briefly describes the DMA controller programmable registers.

Chapter 7, "Real-Time Clock," lists the major features of the real-time clock and briefly describes the real-time clock programmable registers.

Chapter 8, "Serial Controller," discusses operation of the two serial ports and briefly describes the programmable registers.

Chapter 9, "Parallel Printer Port Interface," describes the different modes for the Centronics-compatible printer interface. Address mapping, interrupt selection, and programmable registers are also discussed.

Chapter 10, "Parallel I/O," discusses the general operation of the six parallel ports and the functional blocks of the parallel I/O. It also provides register descriptions and illustrations.

Chapter 11, "System Registers," provides register descriptions and illustrations as well as a brief overview of the three System registers used to control and monitor a variety of functions on the ZT 8907.

Chapter 12, "Watchdog Timer," explains operation of the watchdog timer and includes code for arming and strobing the timer.

Chapter 13, "PCI Mezzanine Local Bus," introduces the features of the PCI bus interface that allows the CPU high speed access to PCI mezzanine peripherals.

Chapter 14, "Programmable LED," provides code for turning the LED on and off.

Chapter 15, "AC Power-Fail," explains AC power-fail detection.

Chapter 16, "Memory Module Socket (U17)," explains the various functions of socket U17 including the optional static RAM that can be used to hold critical system information in the event of power loss.

Chapter 17, "Optional IDE Interface," provides details on the optional high speed local IDE disk drive interface.

Chapter 18, "Optional Local Floppy Disk Interface," provides details on the optional local floppy disk drive interface.

Appendix A, "Board Configuration," describes the jumpers and cuttable traces on the ZT 8907. This appendix details factory default settings as well as information to tailor your board to a specific application.

Appendix B, "Specifications," contains the electrical, environmental, and mechanical specifications for the ZT 8907. This appendix also provides illustrations of cables and connector locations, and tables showing connector pin assignments.

Appendix C, "Digital I/O ASIC System Setup Considerations," offers tips for system configuration to prevent latchup conditions.

Appendix D, "PCI Configuration Space Map," presents the generic layout of the PCI Configuration Header for all PCI compliant devices. It also contains a table showing the PCI bus mapping of the ZT 8907's onboard devices.

Appendix E, "ZT 8907 Vs. ZT 8902: Technical Differences," describes the technical differences between the ZT 8907 and the ZT 8902 single board computers. It includes information to help existing ZT 8902 customers adapt their applications to the ZT 8907.

Appendix F, "Customer Support," offers technical assistance and warranty information, and the necessary information should you need to return your ZT 8907 for repair.

1. INTRODUCTION

This chapter provides a brief introduction to the ZT 8907. It includes a product definition, a list of product features, and descriptions of each of the ZT 8907's functional blocks. Reference unpacking information and installation instructions are found in Chapter 2, "Getting Started."

PRODUCT DEFINITION

ZT 8907

The ZT 8907 is a highly integrated, single board computer that is factory configured to operate with a 100 MHz i486™ IntelDX4™ microprocessor. (Contact Ziatech for support of other 486 microprocessor configurations). The board meets the needs of a wide range of industrial control and processing applications by operating stand alone, as a single master in an STD 32® architecture, or as a permanent or temporary master in an STD 32 architecture.

ZT 89LT07

The ZT 89LT07, a low temperature version with an extended operating range for harsh environments, is now available on a build-to-order basis. The ZT 8907 operating range of 0º to +70º C is extended in the ZT 89LT07 to -40º +70º C. Contact Ziatech for details.

Stand-Alone Operation

The ZT 8907 does not require an STD bus backplane to operate. The ZT 8907 is able to operate stand alone in many applications because of the large selection of the most commonly needed peripheral devices. Peripheral devices include:

- Parallel I/O
- Counter/timers
- Real-time clock
- Watchdog timer
- Speaker interface
- Keyboard controller
- Interrupt controllers
- AC/DC power-fail detection
- Optional local PCI video support (VGA/Flat-Panel)
- Optional static RAM memory with battery backup

- Bi-directional multi-mode printer interface
- Optional local high speed IDE disk drive
- Serial I/O (two 16550 compatible ports)
- Optional local floppy drive interface
- Flash file system (up to 4 Mbytes)
- COM1/COM2 (16550 compatible)

STD-80 or STD 32 Single Master Architecture

The ZT 8907 supports additional memory and I/O through the STD bus. In an STD-80 architecture, all 16-bit data transfers are automatically reduced to 8-bit transfers for complete backwards compatibility with STD-80 boards. In an STD 32 architecture, the data transfers are dynamically adjusted to support 8-bit and 16-bit boards.

See Chapter 3, "STD Bus Interface," for a detailed description of the ZT 8907 interface to the STD bus architecture.

STD 32 Multiple Master Architecture

The ZT 8907 can be configured to operate in a multiple master architecture as a permanent master or a temporary master. With this architecture, up to seven ZT 8907 boards share STD bus memory and I/O resources.

See Chapter 3, "STD Bus Interface," for a detailed description of the ZT 8907 interface to the STD bus architecture.

FEATURES

- STD 32 bus compatible
- Occupies single STD bus slot
- Single and multiple master operation
- 25 to 100 MHz 486SX/DX4 operation
- Numeric coprocessor support (486DX4)
- 8 Kbytes of CPU cache (16 Kbytes on DX4)
- 4, 8, 16, or 32 Mbytes of DRAM memory (EDO)
- 2 or 4 Mbytes of flash memory
- Optional 32-bit PCI bus video support
- Standard AT® peripherals include:

  - –Two interrupt controllers (8259)
  - –Three counter/timers (one 8254)
  - –Real-time clock/CMOS RAM (146818 compatible)
  - –Two DMA controllers (8237)
- Three additional user counter/timers (second 8254)
- 24-point digital I/O (compatible with Opto 22 racks and Ziatech's ZT 2226 rack) with event sense capability
- Bi-directional multi-mode printer interface (Centronics/Extended Mode)
- Two RS-232 serial ports
- Single stage watchdog timer
- Speaker interface
- Push-button reset
- Software programmable LED
- AC/DC power monitor
- Optional static RAM memory with battery backup
- Optional local high speed IDE disk drive (requires one extra slot)
- Optional local floppy drive interface (requires one extra slot, contact Ziatech)
- Compatible with MS-DOS®, QNX®, VxWorks®, Windows® 3.1, Windows 95, and other PC-compatible operating systems
- STD DOS and STAR BIOS options
- STD bus standard 4.5" x 6.5" board format
- +5 V only operation
- Five-year warranty

DEVELOPMENT CONSIDERATIONS

Ziatech offers DOS and STD 32 STAR SYSTEM™ software development systems for ZT 8907 applications. DOS is Microsoft's MS-DOS residing on the ZT 8907. The DOS system provides a development platform similar to a PC, enabling applications to be developed quickly. DOS includes support for many of the ZT 8907's peripherals and is supported by a large number of development tools such as program editors, compilers, assemblers, and debuggers. Refer to the *Ziatech Industrial BIOS for CompactPCI and STD 32 Systems* software manual on Ziatech's web site http://www.ziatech.com.

The STD 32 STAR SYSTEM is the DOS platform operating on more than one master in a single STD bus system. Each master includes local memory, local I/O, and the DOS operating system. Each master is capable of sharing STD bus memory and I/O, such as fixed disks, floppy disks, and video. Refer to the STAR SYSTEM operating manual for configuration and operating instructions.

Ziatech also offers software development kits for QNX® and VxWorks® operating systems. Contact Ziatech for details or view Ziatech's web site at http://www.ziatech.com/.

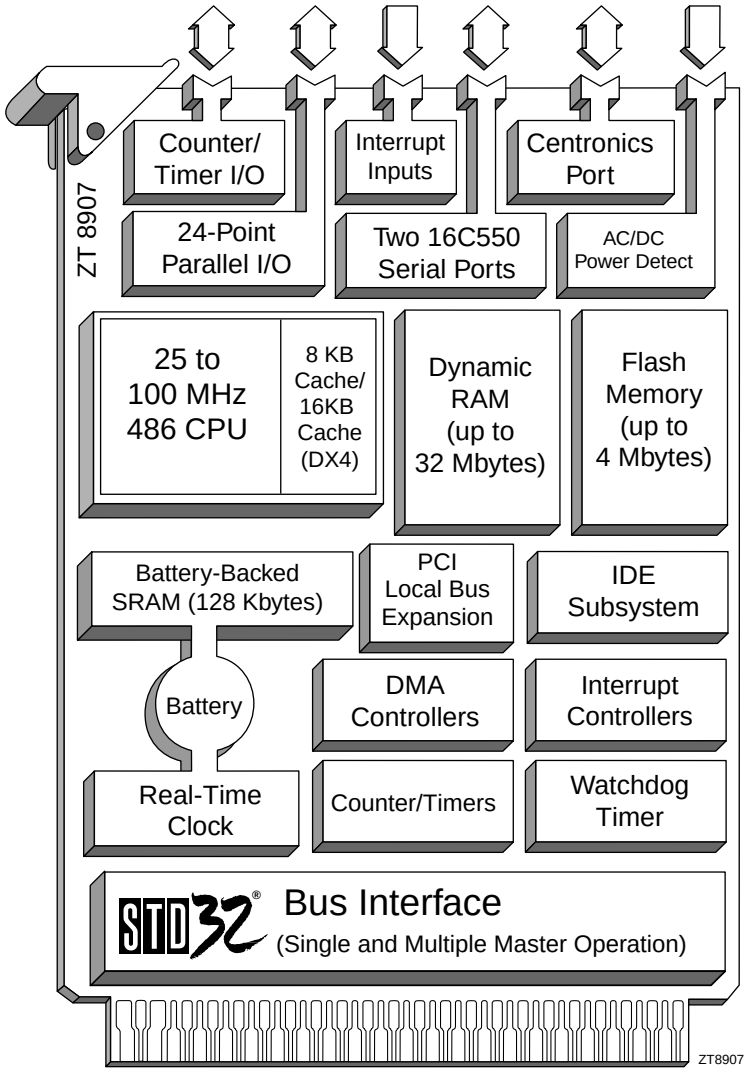
FUNCTIONAL BLOCKS

The Functional Block Diagram figure of the ZT 8907 is on the following page. The blocks correspond to topics remaining in this chapter.

The following topics, not represented on the diagram, are also in this chapter:

- Keyboard Controller
- Speaker Interface
- Optional Floppy Disk Interface

Functional Block Diagram



STD Bus Interface

In an STD 32 system, data transfers are dynamically sized for either 8 bits or 16 bits. STD 32 compatible memory and I/O boards are dynamically sensed to determine the width of the data transfer.

In addition to 16-bit data transfers, the STD 32 system provides the platform needed for multiple master operation. In a multiple master system, up to seven ZT 8907 boards share STD bus resources with a fixed or rotating priority granted by an external bus arbiter, such as the ZT 89CT39. If used, the ZT 89CT39 must be Revision D or higher.

See Chapter 3, "STD Bus Interface," for a detailed description of the ZT 8907 interface to the STD bus architecture.

486SX/DX4 Processors

The ZT 8907 supports the 486SX-25, 486SX-33, and 486DX4-100 processors. The processors differ in operating speeds and hardware support of floating point operations, as shown in the following table.

Processor	Operating Speed	Supports Floating Point Operations
486SX-25	25 MHz	No
486SX-33	33 MHz	No
486DX4-100	33 MHz external, 100 MHz internal	Yes

Note: The 486DX4-100 is a 3.3 V processor. This reduces the energy needed by the CPU as well as the waste heat generated during operation. The ZT 8907 is equipped with a highly efficient 3.3 V power source for the CPU and the DRAM memory.

Memory and I/O Addressing

The ZT 8907 includes two 72-pin SO-DIMM sockets that support up to 32 Mbytes of EDO DRAM. The ZT 8907 also supports flash memory soldered directly on the board. Memory operations up to 32 Mbytes that are not decoded by local memory devices are directed to the STD bus. Data transfers are dynamically adjusted to support standard architecture boards with an 8-bit or 16-bit data path.

The ZT 8907 also includes many I/O peripherals required for industrial control applications. I/O operations not decoded by local I/O devices are directed to the STD bus. The STD bus I/O expansion signal, IOEXP, is supported to limit the addressing redundancy of I/O boards decoding fewer than 16 bits of address. Data transfers are dynamically adjusted to support standard architecture boards with an 8-bit or 16-bit data path.

PCI Bus Video

The ZT 8907 supports both STD bus and local PCI bus video adapters. For STD bus video, Ziatech offers video boards that support VGA and flat panel displays. For local bus video, Ziatech offers zPM adapters that plug directly onto the ZT 8907's PCI mezzanine local bus interface connector (J13).

PCI bus video is up to 700% faster than STD bus video because the data transfers occur at CPU speed (up to 33 MHz) and bus width (up to 32 bits). For space-constrained applications, use of zPM adapters has the advantage of not requiring the additional card cage slot that STD bus video boards would need. Refer to Chapter 13, "PCI Mezzanine Local Bus," for more information.

Serial I/O

The ZT 8907 includes two PC-compatible serial ports. The serial ports are implemented with a 5 V charge pump technology to eliminate the need for a ±12 V supply. Both serial ports include a complete set of handshaking and modem control signals, maskable interrupt generation, and data transfer rates up to 115.2 Kbaud.

The serial ports are configured as DTE and are available through 10-pin frontplane connectors (J3 COM2 and J4 COM1). Optional cables interface the frontplane connectors to standard 9-pin D-shell connectors (male). For more on the operation of the two serial ports, see Chapter 8, "Serial Controller."

Parallel I/O

The ZT 8907 includes three 8-bit parallel I/O ports for a total of 24 parallel I/O lines. Each line is programmable as an input or an output with readback. All three ports include event sense capability where a positive or negative transition on the input will generate an onboard interrupt.

All inputs also feature a programmable debounce circuit. The outputs sink 12 mA and do not glitch during power up or power down. The 24 lines are available through a 50-pin frontplane connector (J5). Optional cables interface the frontplane connector to an 8-, 16-, or 24-position I/O module mounting rack, such as Ziatech's ZT 2226 24-Channel I/O Mounting Rack or those offered by Opto 22. See Chapter 10, "Parallel I/O," for more information.

Interrupts

The ZT 8907's two interrupt controllers provide a total of 15 interrupt inputs. Interrupt controller features include support for level-triggered and edge-triggered inputs, fixed and rotating priorities, and individual input masking.

Interrupt sources include counter/timers, serial I/O, real-time clock, keyboard, printer, hard disk, floppy disk and multiple master communications. There are also five frontplane and five backplane interrupt sources. See Chapter 4, "Interrupt Controller," for more information.

Counter/Timers

Six counter/timers are included on the ZT 8907. Operating modes supported by the counter/timers include interrupt on count, frequency divider, square wave generator, software triggered, hardware triggered, and one shot.

Three of the counter/timers are dedicated to supporting local devices. Three additional counter/timers are available through a 10-pin frontplane connector (J2). See Chapter 5, "Counter/Timers," for more information.

DMA

The ZT 8907's two DMA controllers provide a total of four DMA channels for data transfers between STD bus I/O and local memory. The DMA channels support STD bus DMA slaves by managing the data transfers between the slaves and local memory. Additional features of the DMA channels include auto initialization, address increment or decrement, and software DMA requests.

DMA channel 2, is an 8-bit channel available on the backplane through STD bus BUSRQ* and BUSAK*. Channel 2 is primarily used for floppy disk expansion. Three additional DMA channels are available through a 10-pin frontplane connector (J6).

Each of the three frontplane DMA channels can be independently configured for 8-bit or 16-bit operation. These are designated as DMA0/5, DMA1/6 and DMA 3/7. DMA channels 0, 1 and 3 are 8-bit channels. DMA channels 5, 6 and 7 are 16-bit DMA channels. See Chapter 6, "DMA Controller," for more information.

Watchdog Timer

The watchdog timer optionally monitors system operation. If the watchdog timer is enabled it must be strobed at least every 500 ms. Failure to strobe the watchdog timer within this time period will result in a system reset. See Chapter 12, "Watchdog Timer," for more information.

Real-Time Clock

The real-time clock performs timekeeping functions and includes 128 bytes of battery-backed CMOS RAM. Timekeeping features include an alarm function, a maskable periodic interrupt, and a 100-year calendar. See Chapter 7, "Real-Time Clock," and Chapter 16, "Memory Module Socket (U17)," for more information.

Keyboard Controller

The ZT 8907 includes a PC/AT® keyboard controller that operates when a zPM PCI bus video adapter is installed (in connectors J11 and J13). The keyboard and VGA video signals are available at connector J7. An optional cable is available through Ziatech.

Parallel Printer Port Interface

The ZT 8907 includes a PC/AT printer interface for connection to a Centronics™-compatible printer. The printer interface is available through a 20-pin frontplane connector (J9). An optional cable is available from Ziatech to interface the frontplane connector to a standard 25-pin female D connector. For more information, see Chapter 9, "Parallel Port Printer Interface."

Speaker Interface

The ZT 8907 supports an external speaker through a 2-pin frontplane connector (J8).

AC Power-Fail Protection

With the addition of an AC transformer, the ZT 8907 monitors AC power to permit an orderly shutdown during a power failure. When AC power falls below an acceptable operating range, a non-maskable interrupt is generated to notify the CPU of an impending power failure. When the application software receives this notification, it saves critical data before the CPU is reset.

Connection to the low voltage AC (24 V nom.) is provided through a 2-pin frontplane connector (J10). See Chapter 15, "AC Power-Fail," for more information.

Optional Hard Disk Interface

The ZT 8907 supports an optional local IDE hard disk interface. The interface does not depend on the STD bus, permitting the ZT 8907 to boot from a localized operating system. This feature is especially useful in multiprocessing applications that require more than one operating system. See Chapter 17, "Optional IDE Interface," for more information.

Optional Floppy Disk Interface

An optional floppy disk interface is also available on the front of the board. This is designed for higher volume applications requiring a single board solution without a card cage. For all other applications, a ZT 8954 Low Profile Floppy Disk Controller provides a more modular solution. See Chapter 18, "Optional Local Floppy Disk Interface," for more information.

2. GETTING STARTED

This chapter summarizes the information needed to make the ZT 8907 operational. Please read this chapter before attempting to use the board.

UNPACKING

Please check the shipping carton for damage. If the shipping carton and contents are damaged, notify the carrier and Ziatech for an insurance settlement. Retain the shipping carton and packing material for inspection by the carrier. Save the anti-static bag for storing or returning the ZT 8907.

Do not return any product to Ziatech without a Return Material Authorization (RMA) number. "Customer Support," Appendix F, explains the procedure for obtaining an RMA number from Ziatech.



Warning: Like all equipment utilizing MOS devices, the boards must be protected from static discharge. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the ZT 8907 to handle the boards.

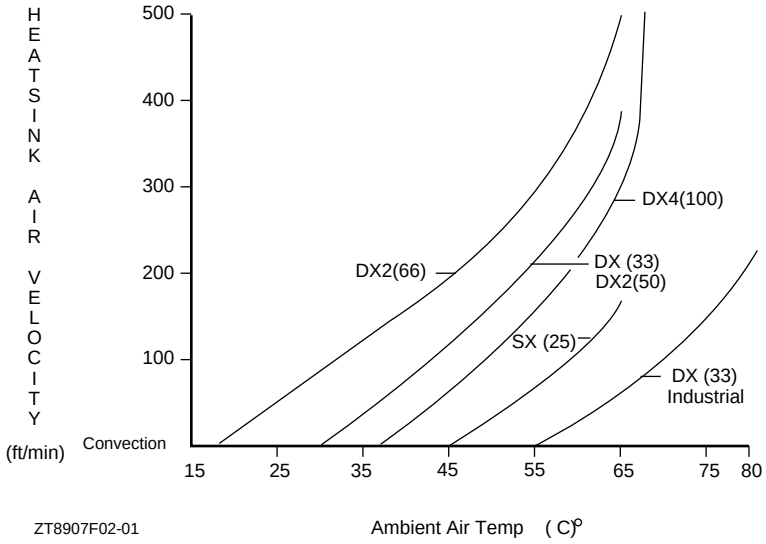
SYSTEM REQUIREMENTS

The ZT 8907 is designed for use with or without an STD bus backplane. The ZT 8907 is electrically, mechanically, and functionally compatible with both the *STD 32 Bus Specification* (ZT MSTD32) for STD bus applications. An STD 32 system is required for 16-bit data transfers to other STD bus boards and for multiple master operation.

Note: If installing the ZT 8907 in an STD 32 card cage with the ZT 8920 32-Bit Memory System, the ZT 8920 should be installed as close to the end as possible. In backplanes with 20 or more slots, install it in slot 17 or higher. Refer to Ziatech's *ZT 8920 32-Bit Memory System hardware manual* for further information. This online manual is in Adobe Acrobat format. To view this file, you need Acrobat Reader, which can be downloaded from the web site http://www.adobe.com.

Ziatech recommends vertical mounting and the use of a fan to meet the airflow requirements shown in the "Airflow Requirements" figure below. Refer to Appendix B, "Specifications," for additional specifications.

Airflow Requirements



MEMORY CONFIGURATION

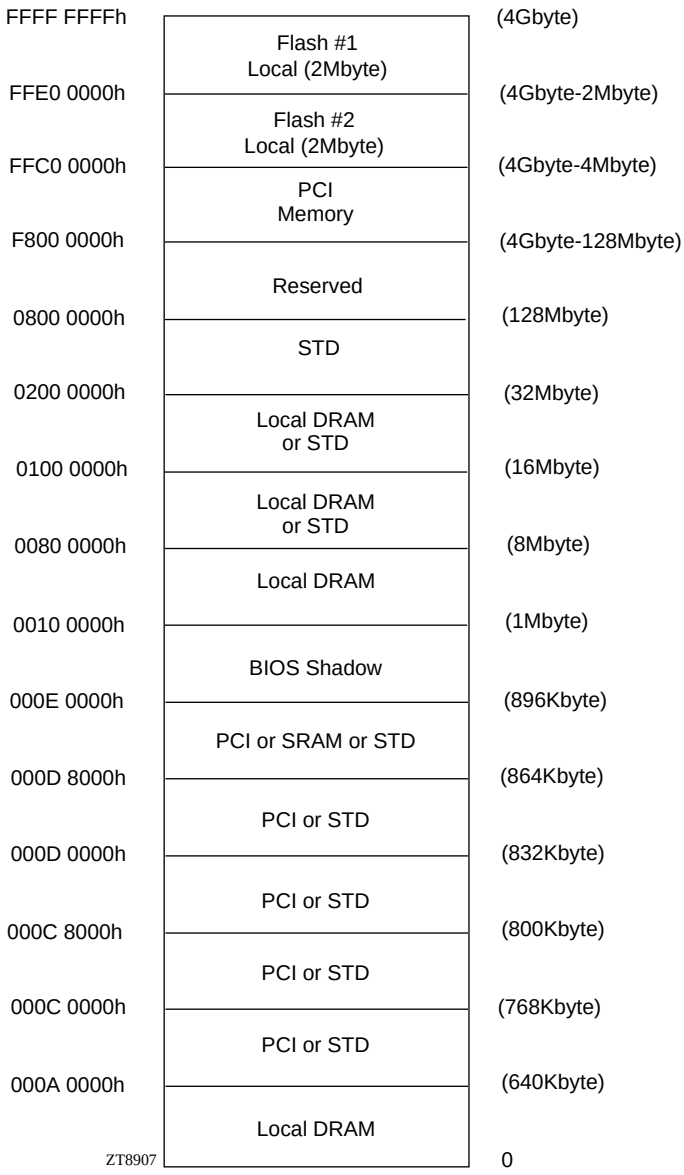
The ZT 8907 can address up to 128 Mbytes of memory. The address space is divided between memory local to the board and memory on the STD bus. Any memory not reserved or occupied by a local memory device is available for STD bus expansion. During local memory operations, the STD bus is held static to decrease system electrical noise and power consumption.

STD bus memory is transferred at a rate of up to 1 Mbyte/second for 8-bit data and 2 Mbytes/second for 16-bit data. The ZT 8907 supports the STD bus wait request signal, WAITRQ*, to interface to memory boards with longer access time requirements than those defined by the STD 32 specifications.

The ZT 8907 is populated with several memory devices. Local DRAM plugs into one or two 72-pin SO-DIMM (small outline-dual inline memory module) sockets. Each SO-DIMM socket supports 4, 8, or 16 Mbytes of DRAM for a total of 32 Mbytes onboard. Local flash memory is soldered directly to the board.

There is space for one or two 2 Mbyte flash devices for a total of 4 Mbytes onboard. A socket is provided for an optional static RAM device (128 Kbytes) that may be battery backed. For more information, see Chapter 16, "Memory Module Socket (U17)". The memory address map is shown in the "Memory Address Map" illustration below.

Memory Address Map



I/O CONFIGURATION

The ZT 8907 addresses up to 64 Kbytes of I/O using a 16-bit I/O address. The address space is divided between I/O local to the board and I/O on the STD bus. Any I/O space not reserved or occupied by a local I/O device is available for STD bus expansion. During local I/O operations, the STD bus is held static to decrease system electrical noise and power consumption.

Local and STD bus I/O data is transferred at a rate of up to 1 Mbyte/second for 8-bit data and 2 Mbytes/second for 16-bit data. The ZT 8907 supports the STD bus wait request signal, WAITRQ*, to interface to I/O boards with longer access time requirements than those defined by the STD 32 specifications. The STD bus I/O

expansion signal, IOEXP, is also supported. The IOEXP signal is automatically driven low over the I/O address range FC00h to FFFFh. Application software should use this address range to access STD bus I/O boards decoding IOEXP and fewer than 16 bits of address to prevent the board from being redundantly mapped throughout the 64 Kbyte I/O address space.

The ZT 8907 is populated with many of the most commonly used I/O peripheral devices for industrial control and computing applications. The I/O address location for each of the peripherals is shown in the "I/O Address Range Selection" table below.

Attention ZT 8902 users: ZT 8902 customers who are adapting their applications for use with the ZT 8907 should be aware that there are some differences between the ZT 8902 and ZT 8907 I/O maps. Compare the I/O maps provided in the respective manuals to learn these differences.

ZT 8902 customers should review Appendix E, "ZT 8907 Vs. ZT 8902: Technical Differences," for more information about how the ZT 8902 and ZT 8907 boards differ.

I/O Address Range Selection

I/O Address Range	I/O Usage	Function
8000h - FFFFh	STD 32 Address Space	
5000h - 7FFFh	PCI I/O Address Space	
4E70h - 4FFFh	PCI I/O Address Space	
46E8h - 46EFh	STD 32 or PCI I/O Address Space	VGA Configuration Register
4000h - 46E7h	PCI I/O Address Space	
1000h - 3FFFh	PCI I/O Address Space	
0C00h - 0FFFh	PCI I/O Address Space	
0900h - 0BFFh	STD 32 Address Space	
0800h - 08FFh	PCI I/O Address Space	
0780h - 07FFh	STD 32 Address Space	
0700h - 077Fh	STD 32 or PCI I/O Address Space	LPT ECP Ports Bits
0500h - 06FFh	STD 32 Address Space	
0400h - 04FFh	PCI I/O Address Space	
03F8h - 03FFh	STD 32 or PCI I/O Space	COM1 Register Set
03F6h	STD 32 or PCI I/O Space	Primary IDE Registers Set
03F0h - 03F5h, 03F7h	STD 32 or PCI I/O Space	Floppy Register Set
03E0h - 03EFh	STD 32 Address Space	
03B0h - 03DFh	STD 32 or PCI I/O Address Space	VGA Register Set
0380h - 03AFh	STD 32 Address Space	
037Ch - 037Fh	STD 32 or PCI I/O Address Space	LPT EPP
0378h - 037Bh	STD 32 or PCI I/O Address Space	LPT Port
0376h	PCI I/O Address Space	Secondary IDE Register
0370h - 0375h, 0377h	STD 32 Address Space	
0300h - 036Fh	STD 32 Address Space	
02F8h - 02FFh	STD 32 or PCI I/O Address Space	COM2 Register Set
0200h - 02F7h	STD 32 Address Space	

I/O Address Range Selection (continued)

I/O Address Range	I/O Usage	Function
01F8h - 01FFh	STD 32 Address Space	
01F0h - 01F7h	STD 32 or PCI I/O Address Space	Primary IDE Register Set
0178h - 01EFh	STD 32 Address Space	
0170h - 0177h	PCI I/O Address Space	Secondary IDE Register Set
0100h - 016Fh	STD 32 Address Space	
00F0h - 00FFh	PCI I/O Address Space	Onboard Coprocessor
00E8h - 00EFh	PCI I/O Address Space	Reserved
00E0h - 00E7h	PCI I/O Address Space	Onboard Digital I/O
00C0h - 00DFh	PCI I/O Address Space	Onboard Slave DMAC
00B0h - 00BFh	PCI I/O Address Space	Reserved
00A0h - 00AFh	PCI I/O Address Space	Onboard Interrupt Controller
0093h - 009Fh	PCI I/O Address Space	Reserved
0092h	PCI I/O Address Space	Fast Reset & Gate A20
0090h - 0091h	PCI I/O Address Space	Reserved
0081h - 008Fh	PCI I/O Address Space	Onboard DMA Page Registers
0080h	PCI I/O Address Space	Diagnostic Port 080h
0079h - 007Fh	PCI I/O Address Space	Reserved
0078h	PCI I/O Address Space	ZT 8905 System Register 0
0070h - 0077h	PCI I/O Address Space	Onboard Real time Clock
0068h - 006Fh	PCI I/O Address Space	
0067h	STD 32 or PCI I/O Address Space	VGA Control Register
0065h – 0066h	PCI I/O Address Space	
0064h	STD 32 or PCI I/O Address Space	Keyboard
0061h - 0063h	PCI I/O Address Space	
0060h	STD 32 or PCI I/O Address Space	Keyboard
0050h - 005Fh	PCI I/O Address Space	Reserved
0040h - 004Fh	PCI I/O Address Space	Onboard Counter Timers
0030h - 003Fh	PCI I/O Address Space	Reserved
0020h - 002Fh	PCI I/O Address Space	Onboard master Interrupt
0000h - 001Fh	PCI I/O Address Space	Onboard Master DMAC

Notes:

"STD 32 Address Space" refers to STD 32 backplane devices.

"PCI I/O Address Space" refers to mezzanine devices or devices on board the ZT 8907.

CONNECTORS

The ZT 8907 includes several connectors to interface to application-specific devices. Refer to the "Connectors" section in Appendix B for complete connector descriptions and connector pinouts, as well as cabling information.

JUMPER DESCRIPTIONS

The ZT 8907 includes several jumper and cuttable trace configuration options for features that cannot be provided through the BIOS SETUP utility (discussed in the "Setup" section below). Refer to Appendix A, "Board Configuration," for details.

REMOVING THE zPM MEZZANINE CARD

Ziatech zPM mezzanine cards plug into the 150-pin PCI mezzanine connector provided on many Ziatech CPUs (J13 on the ZT 8908). Mechanical connection of the boards is reinforced by metal or nylon standoffs that are screwed through mounting holes in each board.

Important: If it is necessary to disconnect a zPM mezzanine card, Ziatech recommends removing only the screws attaching the card to the standoffs. If it is necessary to remove the standoffs from the CPU, be aware that on some CPUs washers may be located between the PCB and the standoffs. Be sure to retain and reinstall these washers to their original position if they are removed for any reason.

Also take care when installing and removing the zPM mezzanine card to prevent premature wear or accidental bending of the 150-pin (and on some mezzanine cards, an additional 16-pin) connector. When removing the card, disengage the pins evenly across the length of the connectors instead of prying only from one side. It may be helpful to gently wiggle the card from side to side when removing it.



Warning: To avoid damage to the CPU and the mezzanine card, install and remove the mezzanine card at a static-free workstation.

SETUP

The ZT 8907 has many features that can be configured with the BIOS SETUP utility. The SETUP utility is executed during the boot sequence when the **"s"** key is typed. In DOS systems, SETUP may be executed by running the SETUP.COM program from the command line.

The BIOS SETUP utility on all Ziatech CPUs allows configuration of options such as base memory and extended memory size selection, boot source, hard disk type, and floppy disk type. On the ZT 8907, the BIOS SETUP also allows routing of interrupts, memory mapping, and I/O mapping for the STD 32 bus.

Previous generation CPU products required jumpers to configure these options. This change makes configuration both faster and more intuitive. PCI peripherals are also automatically configured through the BIOS.

The following topics present an introduction to the setup and configuration of the ZT 8907.

BIOS SETUP Screens

The BIOS SETUP utility for the ZT 8907 is organized as two screens, shown on the last page of this chapter and described below.†

- Screen 1: **Generic options list.** Screen 1 lists the options shared among all Ziatech CPUs. Base memory and extended memory size selection, boot source, hard disk type, and floppy disk type are configurable through this screen.

- Screen 2: **ZT 8907-specific SETUP options.** Options such as interrupt routing and STD 32 memory addressing are configurable through this screen. Screen 2 is detailed in the section "ZT 8907-Specific SETUP Options" in Appendix A.

The parameters in the SETUP screens are easily changed. Use the arrow keys to select a parameter, then press **+** or **-** to step through the valid choices for that parameter. A dynamic help line at the bottom of the screens helps you determine how to set each parameter. SETUP accepts only valid parameter sets: if changing one parameter invalidates another, SETUP automatically updates the invalid parameter. After setting the parameters, press the F10 key to accept them. Press the **Page Down** and **Page Up** keys to switch between SETUP screens.

System Configuration Overview

The Ziatech Industrial BIOS and MS-DOS operating system software is preprogrammed in the ZT 8907's onboard flash memory. The BIOS includes embedded support to allow the ZT 8907 flash memory to be used as a solid-state drive (SSD) in the MS-DOS environment. Ziatech also supplies SSD support for other popular operating systems such as Windows NT and QNX (contact Ziatech for SSD drivers for specific operating systems).

The ZT 8907 is configured during the boot sequence by the BIOS. The BIOS uses system configuration information stored as SETUP parameters.

To access the SETUP utility, either boot the system and press the "**s**" key during the system RAM check, or run the SETUP.COM utility from the MS-DOS prompt.

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† A third screen for STAR SYSTEM configuration options is available when running SETUP on permanent master CPUs. Refer to the *STD 32 STAR SYSTEM User's Manual* for more information.

The SETUP parameters are saved in the battery-backed RAM portion of the ZT 8907's real-time clock device. The SETUP parameters can also be saved in a file format, or as the programmed BIOS defaults.

Operating System Installation

It may be necessary to install an operating system such as Windows NT or QNX on the ZT 8907 system. This section describes the generic OS installation process. For OS-specific information, refer to the documentation provided by the OS vendor.

Note: If the installation requires a CD-ROM drive, the appropriate drivers must first be installed in order to access the CD-ROM drive.

1. Use screen 1 in the BIOS SETUP utility to configure the appropriate peripheral devices. Note that the Fixed Disk parameters (used for EIDE drives) include an "AUTO" setting which will cause SETUP to query the drive to determine the correct geometry (cylinders/heads/sectors).

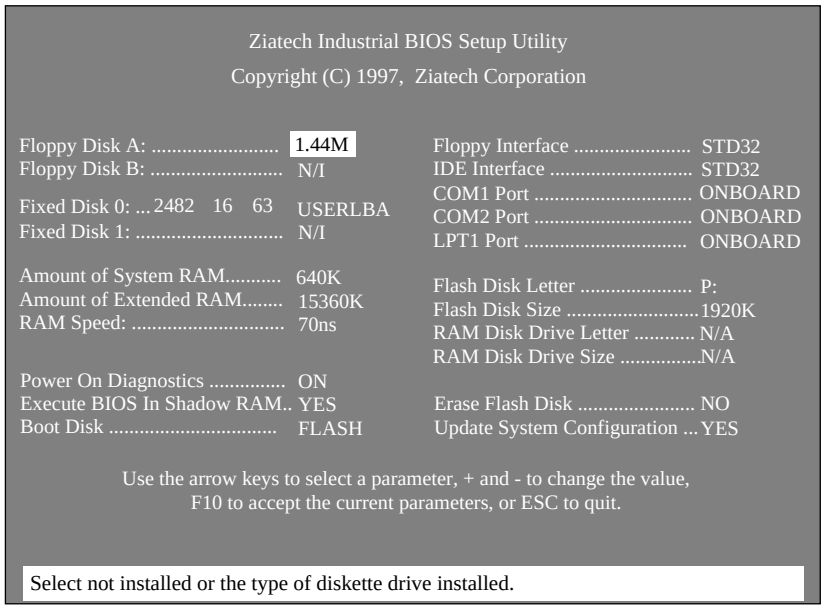
2. Select the proper boot source in the SETUP utility depending on the OS installation media that will be used. For example, if the OS includes a bootable installation floppy, select "FLOPPY" for "Boot Disk" and reboot the system with the installation floppy installed in the floppy drive.

3. Proceed with the OS installation as directed, being sure to select appropriate device types if prompted. See the "ZT 8907 On-Board Device PCI Bus Mapping" table in Appendix D for a list of the PCI devices used on the ZT 8907.

4. When installation is complete, the system should be rebooted and the SETUP "Boot Disk" parameter should be set for the appropriate boot media.

BIOS SETUP Utility: Screen 1

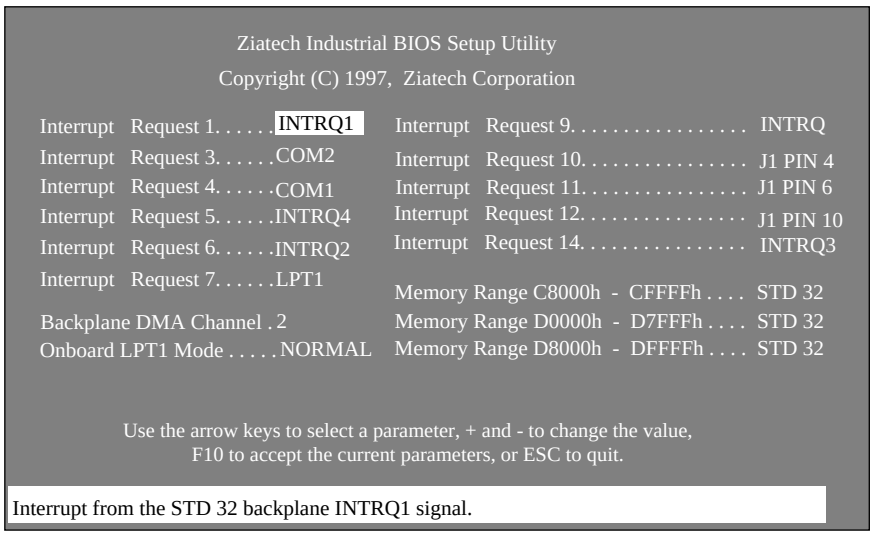
Generic SETUP Options



ZT8907

BIOS SETUP Utility: Screen 2

ZT 8907-Specific SETUP Options



ZT8907

3. STD BUS INTERFACE

The ZT 8907 includes several I/O devices common to industrial control applications. The ZT 8907 also operates with the STD 32 bus architecture to support additional I/O and memory mapped devices as required by the application. This chapter discusses the STD 32 architecture and its effect on the operation of the ZT 8907.

STD-80 AND STD 32 OPERATION

The *STD-80 Series Bus Specification*, developed in the early 1980s by Ziatech Corporation, defines the electrical, mechanical, and functional characteristics of an STD bus system based on the 8088 series of microprocessors. Features of an STD-80 system include an 8-bit data bus, 24-bit address bus, and single bus master operation.

In the late 1980s, Ziatech developed the *STD 32 Bus Specification* as an extension to the *STD-80 Bus Specification*. Features of an STD 32 system include compatibility with STD-80 memory and I/O boards, expansion capabilities of up to a 32-bit data bus and a 32-bit address bus, and support for multiple bus master operation.

The following topic discusses STD 32 operation in greater detail.

STD 32 Operation

Data transfers between the ZT 8907 and any STD bus memory or I/O board occur eight bits at a time for boards supporting an 8-bit data bus and 16 bits at a time for boards supporting a 16-bit data bus in an STD 32 system. The ZT 8907 automatically determines the type of transfer at the start of each STD bus operation.

If the application software includes a 16-bit operation with an 8-bit STD bus board, the ZT 8907 automatically reduces the transfer into two STD bus cycles. If the application software includes a 16-bit operation with a 16-bit STD bus board, the ZT 8907 performs the transfer in a single STD bus cycle.

In addition to 16-bit data transfer support, the STD 32 system has another advantage: it supports up to seven ZT 8907 boards in a single system. With the addition of an STD bus arbiter, such as the ZT 89CT39, multiple ZT 8907 boards have fixed or rotating priority access to STD bus memory and I/O resources. This architecture is useful for applications that can be divided into modular control blocks, with each module running on a unique ZT 8907. The ZT 89CT39, if used, must be Revision D or higher.

STD-80 BUS COMPATIBILITY

Address Multiplexing

The *STD-80 Series Bus Specification* defines a multiplexing scheme to transfer address lines A16 through A19 across the lower half of the data bus during the start of each memory cycle. The ZT 8907 extends this concept by also transferring address lines A20 through A23 across the upper half of the data bus.

This feature is especially useful if all memory mapped STD bus boards used in the system decode 24 bits of address. If a memory mapped board decodes fewer than 24 bits, the board appears multiple times in the 24-bit memory map. A20 is located at port 92h. Set bit 1 to 1 for disable, 0 for enable.

Interrupts

The *STD-80 Series Bus Specification* defines a single interrupt signal, INTRQ* (P44). If STD bus maskable interrupts are used in the application, the ZT 8907 is configurable (through the BIOS SETUP utility, screen 2) to receive INTRQ* and three optional interrupts: INTRQ1* (P37), INTRQ2* (P50), and INTRQ4* (P6).

STD bus peripheral boards must be capable of generating an interrupt on INTRQ1*, INTRQ2*, and INTRQ4* to use this feature. Note that an additional interrupt, INTRQ3*, is available in the STD 32 architecture. Chapter 4, "Interrupt Controller," summarizes the interrupt sources.

I/O Expansion

The *STD-80 Series Bus Specification* defines an I/O expansion signal, IOEXP, used to reduce addressing redundancy of an I/O board decoding fewer than 16 address lines. The ZT 8907 automatically drives this signal low when the application software performs an STD bus I/O address in the address range FC00h through FFFFh. To use this feature:

- The I/O mapped STD bus board is configured to respond to an active low IOEXP.
- The application software assigns the board to address FC00h plus the board configuration offset.

External Masters and DMA Slaves

The ZT 8907 does not support external masters in an STD-80 architecture; an STD 32 architecture is required for external master support. The ZT 8907 supports DMA slaves in both STD-80 and STD 32 architectures.

The ZT 8907 includes a frontplane connector (J6) to support DMA slaves in an STD-80 architecture. J6 provides signals (not defined on the STD-80 bus) that are required by DMA slaves. See Chapter 6, "DMA Controller," for an overview of ZT 8907 DMA architecture and DMA controller operation.

STD 32 BUS COMPATIBILITY

The ZT 8907 is compatible with Version 2.1 of the *STD 32 Bus Specification*. Optional STD 32 features are discussed in terms of compliance levels.

Permanent Master: SA16, SA8-I, SDMA8, SDMA16, SDMABP

Temporary Master: SA16, SA8-{MD}, I, SDMA8, SDMA16, SDMABP

The following topic describes the compliance levels in more detail.

Compliance Levels

The following are brief descriptions of the STD 32 compliance levels supported by the ZT 8907.

SA8, SA16 Supports 8-bit and 16-bit data transfers with STD-80 signal format and timings. The ZT 8907 automatically determines the width of the data transfer at the start of each STD bus operation. STD-80 compatible memory and I/O boards are supported.

I Supports four additional STD bus interrupts: INTRQ1*, INTRQ2*, INTRQ3*, and INTRQ4*. These interrupts are input from the STD bus and connected to the interrupt controller through a software configurable switch. This feature is selected through the BIOS SETUP utility. Refer to the "Interrupt Architecture" table in Chapter 4 for interrupt routing options.

{MD} Supports the multiple master (DREQx*, DAKx*) protocol. These two signals are used by the ZT 8907 in a multiple master architecture to gain control of STD bus resources. The use of these signals requires a bus arbiter, such as the ZT 89CT39, to be plugged into slot X. The ZT 89CT39 must be Revision D or higher.

SDMA8, SDMA16 Supports 8-bit or 16-bit Standard Architecture DMA as defined in the STD 32 Bus Specification.

SDMABP Supports Standard Architecture DMA using BUSRQ*/BUSAK* for request and acknowledge and the backplane DMA control signals DMAIOR*, DMAIOW*, and TC.

STD BUS INTERRUPTS

The ZT 8907 supports both maskable and non-maskable interrupts from the STD bus. This section discusses system level issues related to these interrupts. Refer to Chapter 4, "Interrupt Controller," for more information on the ZT 8907's maskable interrupts.

Maskable Interrupts

The STD bus maskable interrupts monitored by the ZT 8907 are INTRQ* (P44), INTRQ1* (P37), INTRQ2* (P50), INTRQ3* (E67), and INTRQ4* (P6). These maskable interrupts are configurable through the BIOS SETUP utility. Refer to Chapter 4, "Interrupt Controller," for details. Note that an STD 32 backplane is needed to use INTRQ3*.

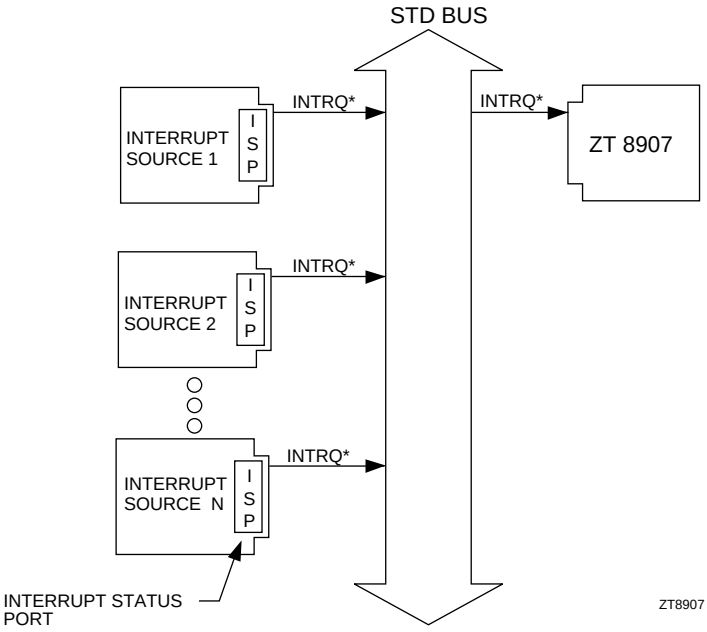
Some applications may find it necessary to share multiple interrupt sources on a single STD bus interrupt request, as shown in the "STD Bus Polled Interrupt Structure" figure. Since the interrupt controller provides a single vector for each input, it is up to the application software to poll each possible source on the shared interrupt request signal to determine which is requesting service. This procedure is fine for most applications, provided that each source can be polled and that the interrupt controller is programmed for level-triggered operation.

Some applications include edge-triggered interrupt sources. For example, the Ziatech DOS System uses edge-triggered interrupts to support the timer used to generate the periodic system tick. The interrupt controller inputs are independently programmable for edge-triggered or level-triggered interrupts.

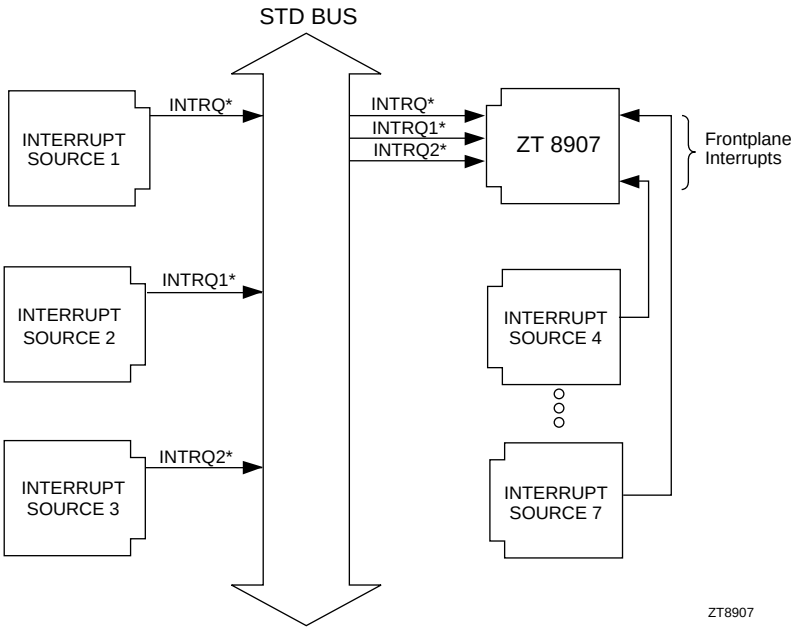
PCI interrupt sources will be programmed as level triggered. All other interrupts will be programmed as edge triggered (to maintain PC compatibility) by the BIOS. The selection of which interrupts are used for PCI can be changed through screen 2 of the BIOS SETUP utility (refer to the section, "ZT 8907-Specific SETUP Options" in Appendix A).

In an edge-triggered architecture, multiple interrupt sources should not share the same interrupt request signal because it is possible to miss an interrupt request from one source while an interrupt request from another source is being serviced. In an edge-triggered architecture, each interrupt source requires a unique connection to the interrupt controller, as shown in the "STD Bus Vectored Interrupt Structure" figure below.

STD Bus Polled Interrupt Structure



STD Bus Vectored Interrupt Structure



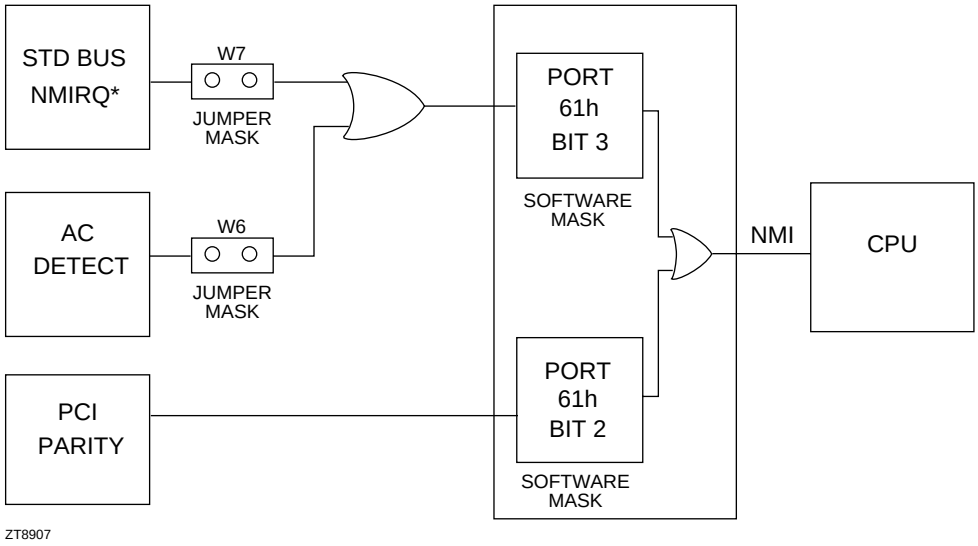
Non-Maskable Interrupts

As shown in the "Non-Maskable Interrupt Structure" figure, the ZT 8907 supports three sources of non-maskable interrupt requests:

- STD bus NMIRQ* (P46)
- AC power-fail detection
- PCI bus parity error

The STD bus NMIRQ* and AC power-fail interrupts (enabled through jumpers W6 and W7) combine with the PCI bus parity error interrupt before being routed to the CPU. Both the STD bus NMIRQ* and AC power-fail interrupts are maskable through port 61h. Bits 0 and 1 on the Digital I/O ASIC's System Register 2 (E4h) indicate whether a non-maskable interrupt was generated by the STD bus or an AC power failure. Bit 2 of the port 61h register indicates whether a non-maskable interrupt was generated by a parity error.

Non-Maskable Interrupt Structure



RESET

The ZT 8907 is automatically reset with a precision voltage monitoring circuit that detects when Vcc is below the acceptable operating limit of 4.75 V. Other sources of reset include the watchdog timer, local pushbutton switch, and the STD bus pushbutton reset signal, PBRESET* (P48).

The ZT 8907 responds to any of these reset sources by initializing local peripherals and driving the STD bus system reset, SYSRESET* (P47). STAR SYSTEM temporary

masters do not drive SYSRESET*. The SYSRESET* activation can be disabled by removing cuttable trace CT53. The ZT 8907 reset is typically active for 500 ms.

MULTIPLE MASTER AND INTELLIGENT I/O

Ziatech offers two architectures for increasing the number of microprocessors in a single system: multiple master and intelligent I/O. Applications can use multiple master, intelligent I/O, or a combination of the two. The following topics discuss the two architectures.

Multiple Master

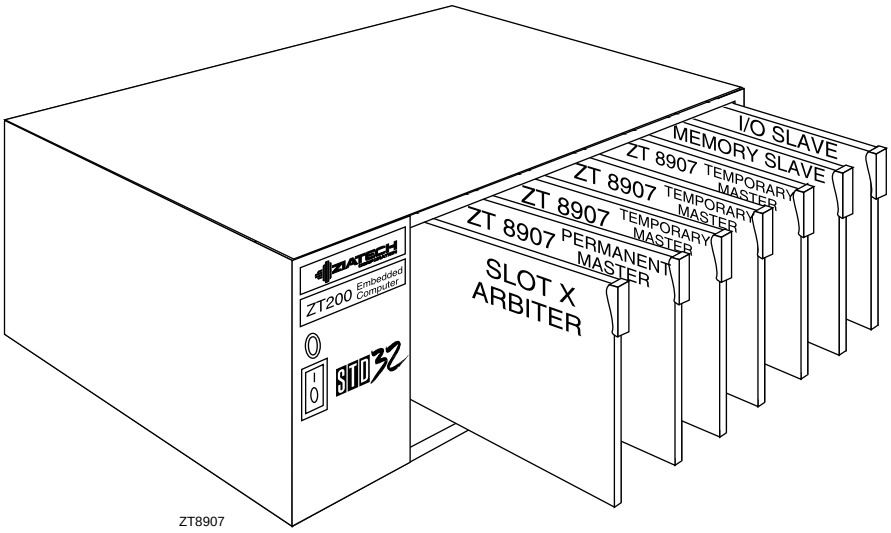
A multiple master architecture requires one permanent master and one or more temporary masters, as illustrated in the "Multiple Master Architecture" figure below. The ZT 8907 is configurable (by installing or removing resistor packs RP1 and RP2) for either permanent or temporary master operation.

Each master has complete access to STD bus resources and operates at full speed when the local CPU is communicating with local memory and I/O. It is not until the application software attempts an STD bus access that arbitration occurs.

The ZT 8907 responds to an STD bus access from the application software by generating an STD bus request, DREQx* (E16), to an external bus arbiter, such as the ZT 89CT39. The ZT 8907 then suspends all local operation until the bus arbiter returns an STD bus acknowledge, DAKx* (E15). The ZT 89CT39, if used, must be Revision D or higher.

All arbitration is done in hardware on the external bus arbiter board and is transparent to the application software. The amount of time required for this arbitration depends on the amount of time higher priority masters are in control of STD bus resources. A shared resource locking mechanism is supported to guarantee exclusive access to STD bus memory or I/O.

Multiple Master Architecture



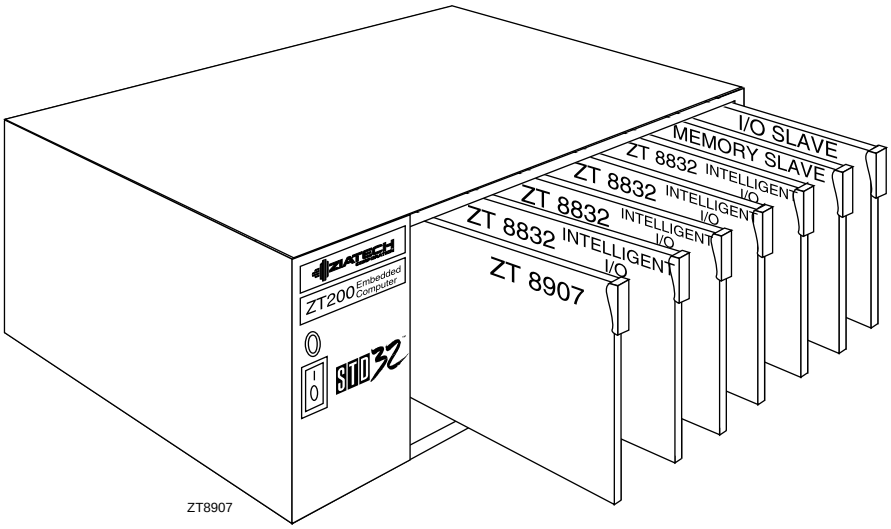
Intelligent I/O

An intelligent I/O system includes a single ZT 8907 and one or more intelligent I/O boards, such as the ZT 8832. The "Intelligent I/O Architecture" figure below illustrates this architecture. The intelligent I/O board incorporates several I/O devices, a dual-port RAM for processor communications, and a CPU dedicated to controlling these devices.

Each intelligent I/O board operates at full speed when communicating with local memory, local I/O, and dual-port RAM. The ZT 8907 also operates at full STD bus speeds when accessing the dual-port RAM. It is not until the ZT 8907 and the intelligent I/O board access the dual-port RAM at the same time that arbitration occurs.

All arbitration is done in hardware local to each intelligent I/O board, eliminating the need for an external bus arbiter. The arbitration is transparent to the application software. The amount of time required for arbitration depends on the amount of time the device in control of the dual-port RAM requires to complete operation. A shared resource locking mechanism is supported to guarantee exclusive access to dual-port RAM by either the ZT 8907 or the intelligent I/O board.

Intelligent I/O Architecture



Multiple Master Vs. Intelligent I/O

Both multiple master and intelligent I/O architectures are excellent methods of increasing system performance. The application designer has the freedom to select either architecture or combine both to meet the needs of the specific application. The following is a brief comparison of the multiple master and intelligent I/O architectures.

- An advantage of the multiple master system is that each ZT 8907 has complete access to all STD bus memory and I/O resources. In an intelligent I/O system, only one ZT 8907 has access to STD bus memory and I/O, including the dual-port RAM interface to each intelligent I/O board.

- An advantage of the intelligent I/O system is lower system cost. The intelligent I/O architecture operates in both STD-80 and STD 32 bus structures. Dual port RAM arbitration is local to each intelligent I/O board, eliminating the need for a system arbiter. Also, most multiple master implementations require an STD bus memory slave for communications between the masters. With an intelligent I/O architecture, all communications between the single master and the intelligent I/O boards are through the dual-port RAM local to each intelligent I/O board.

Multiple Master System Requirements

The following is a list of considerations for the ZT 8907 operating in a multiple master architecture.

- One ZT 8907 must be configured as a permanent master, or there must be another permanent master in the system. The permanent master is responsible for managing the STD bus clock, CLOCK* (P49), and the system reset, SYSRESET* (P47). The remaining ZT 8907 boards must be configured for temporary master operation.

There are two socketed resistor packs (RP1 and RP2) that must be installed on the permanent master and removed from all temporary masters. These resistor packs are located on the edge of the board between the Ziatech logo and connector J12.

- An STD 32 backplane is required. An STD-80 backplane does not support the bus exchange protocol (DREQx* and DAKx*).

- A ZT 89CT39, or equivalent bus arbiter, is needed to manage ZT 8907 access to the STD bus resources. The bus arbiter must be installed in Slot 'X' of the STD 32 backplane. The ZT 89CT39 must be Revision D or higher.

Multiple Master System Reset

The ZT 8907 configured for single master operation is automatically reset with a precision voltage monitoring circuit, watchdog timer, local pushbutton reset, and the STD bus pushbutton reset signal, PBRESET* (P48).

In response to any of these signals, the ZT 8907 initializes local peripherals and activates the STD bus system reset, SYSRESET* (P47). STAR SYSTEM temporary masters do not drive SYSRESET*. The SYSRESET* activation can be disabled by removing cuttable trace CT53.

In a multiple master system, a ZT 8907 configured as a permanent master operates the same as a ZT 8907 operating in a single master architecture. A ZT 8907 configured as a temporary master manages reset differently.

A temporary master does not monitor PBRESET* and does not generate SYSRESET*. Instead, a temporary master ignores PBRESET* and monitors SYSRESET*. This enables the temporary masters to be reset when the permanent master generates SYSRESET*. This also enables the pushbutton reset on the temporary master to reset only the temporary master while the pushbutton on the permanent master resets the entire system.

4. INTERRUPT CONTROLLER

The ZT 8907 includes two Intel 8259-compatible cascaded interrupt controllers that provide a programmable interface between interrupt-generating peripherals and the CPU. The interrupt controllers monitor 15 interrupts with programmable priority. When peripherals request service, the interrupt controller interrupts the CPU with a pointer to a service routine for the highest priority device.

Note: The ZT 8907 does not support cascaded interrupt controllers on the STD bus.

It may be helpful before reading this chapter to review Chapter 3, "STD Bus Interface," for a discussion on the STD-80 and STD 32 architectures and their effect on the operation of the ZT 8907.

The major features of the interrupt architecture are listed below.

- 15 individually maskable interrupts
- Jumperless configuration
- Level-triggered or edge-triggered recognition
- Fixed or rotating priorities
- PCI Interrupt support
- PCI Extended Mode register support

The interrupt architecture is shown in the "Interrupt Architecture" table below. Interrupt configuration is performed through screen 2 of the BIOS SETUP utility, allowing the user to set up the interrupt architecture to the needs of the application. The BIOS SETUP utility allows most of the interrupt controller interrupts to be configured from a variety of interrupt sources. See the section "ZT 8907-Specific SETUP Options" in Appendix A. The ZT 8907 supports the Extended Mode register, which allows individual programming of low-level triggered or active high-edge triggered interrupts.

Interrupt Architecture (see notes following table)

Notes	CPU Interrupt	Programmable Interrupt Sources (default in bold)
1	IRQ0	**System Timer 0**
2, 3	IRQ1	**Local keyboard** or **INTRQ1*** CTC2, Ch.0
4	IRQ2	**Cascade**
3	IRQ3	**COM2** CTC 2, Ch.1
3	IRQ4	**COM1** CTC 2, Ch.0
3	IRQ5	**INTRQ4*** CTC 2, Ch.1
3	IRQ6	**INTRQ2*** CTC 2, Ch.0
3	IRQ7	**Local LPT** CTC 2, Ch.1
5	IRQ8	**Real-Time Clock**
3	IRQ9	**INTRQ*** CTC 2, Ch.0
3	IRQ10	**J1, pin 4** CTC 2, Ch.1 CTC 2, Ch.0 PCI
3	IRQ11	**J1, pin 6** CTC 2, Ch.0 CTC 2, Ch.1 PCI
3	IRQ12	**J1, pin 10** CTC 2, Ch.1 CTC 2, Ch.0 PCI
6	IRQ13	**Math Coprocessor**
3, 7	IRQ14	**Local IDE** or **INTRQ3-** CTC 2, Ch.0
8	IRQ15	**CTC 2, Ch.2**

Notes:

1. CTC1-Ch0: System Timer.
2. The default IRQ1 source depends on the status of jumper W5: when W5 is removed, IRQ1 = Local Keyboard; when W5 is installed, IRQ1 = INTRQ1*. IRQ1 is normally used for the keyboard interrupt. If your system has a backplane video card with a keyboard controller (such as the ZT 8982), install jumper W5 to disable the on-board keyboard controller. W5 must be removed when using local video or no-video.
3. Also supports INTRQ*, INTRQ1* INTRQ2*, INTRQ3*, INTRQ4*, and J1--pins 2, 4, 6, 8, 10.
4. Second interrupt controller (8259).
5. Real Time Clock interrupt.
6. Math coprocessor exception interrupt.
7. Enable the ZT 8907 for either local IDE or STD 32 IDE operation through the BIOS SETUP utility. See "Selecting IDE Operation Type" in Chapter 17 for details.
8. The default IRQ15 source depends on the status of cuttable traces CT7 and CT8 (see Appendix A, "Board Configuration"). Other interrupt sources are possible for IRQ15 with custom software configuration. Contact Ziatech for details.

INTERRUPT SOURCES

The interrupt sources are summarized below.

Backplane: There are five STD bus interrupts routed to the interrupt configuration logic, configurable through the BIOS SETUP utility, screen 2. These interrupts are labeled INTRQ*, INTRQ1*, INTRQ2*, INTRQ3*, and INTRQ4*. All five interrupts are supported in an STD 32 backplane and all but INTRQ3* are supported in an STD-80 backplane. These interrupts are active-low on the STD bus and inverted before they reach the interrupt configuration logic.

Frontplane: There are five frontplane interrupts routed to the interrupt configuration logic. These interrupts are available through connector J1 as active-low inputs that are inverted before reaching the interrupt configuration logic. The pin assignments for connector J1 are given in the "Connectors" topic in Appendix B, "Specifications." Many STD bus boards include a J1-compatible connector for routing interrupts to the ZT 8907 through a ribbon cable. This architecture is useful if the application requires more interrupts than are available on the STD bus.

PCI: Three interrupt levels may be assigned to the PCI bus when not used for other devices. IR10, IR11, and IR12 may be allocated to PCI through

screen 2 of the SETUP utility. The PCI configuration utility then assigns interrupts to PCI devices as needed.

Local: Local interrupt sources include counter/timers (CTC1 and CTC2), serial ports (COM1 and COM2), parallel port (LPT1), keyboard, math coprocessor, real-time clock and local IDE.

PROGRAMMABLE REGISTERS

Each interrupt controller includes four initialization registers, three control registers, and three status registers. The I/O port addressing for the interrupt controllers is given in the "Interrupt Controller Register Addressing" table below. The base address of the master interrupt controller is 20h and the base address of the slave interrupt controller is A0h.

Interrupt Controller Register Addressing

Address	Register	Operation
Base+0h	IRR, ISR, IPR	Read
Base+0h	ICW1	Write
Base+0h	OCW2, OCW3	Write
Base+1h	OCW1	Read/Write
Base+1h	ICW2, ICW3, ICW4	Write

ADDITIONAL INFORMATION

Refer to the *Ziatech Industrial BIOS for CompactPCI and STD 32 Systems* software manual for more information on the operating system's use of the interrupt inputs. Refer to the Acer Labs *FINALI-486 M1487/M1489 486 PCI Chip Set Preliminary Data Sheet* for more information on the interrupt controller registers.

5. COUNTER/TIMERS

The ZT 8907 includes two Intel-compatible 8254 devices for a total of six programmable counter/timers. The counter/timers are useful for generating timing loops, timed and periodic interrupts, and for counting external asynchronous events. The major features of the counter/timers are listed below.

- Six 16-bit counter/timers
- Six programmable operating modes
- Binary and BCD counting
- Interrupt and polled operation

The six programmable operating modes are summarized in the "Counter/Timer Operating Modes" table below.

Three of the counter/timers are PC-compatible and are **dedicated** for use by the system software. The architecture for these is illustrated in the "PC-Compatible Counter/Timer (CTC 1) Architecture" figure on the following page.

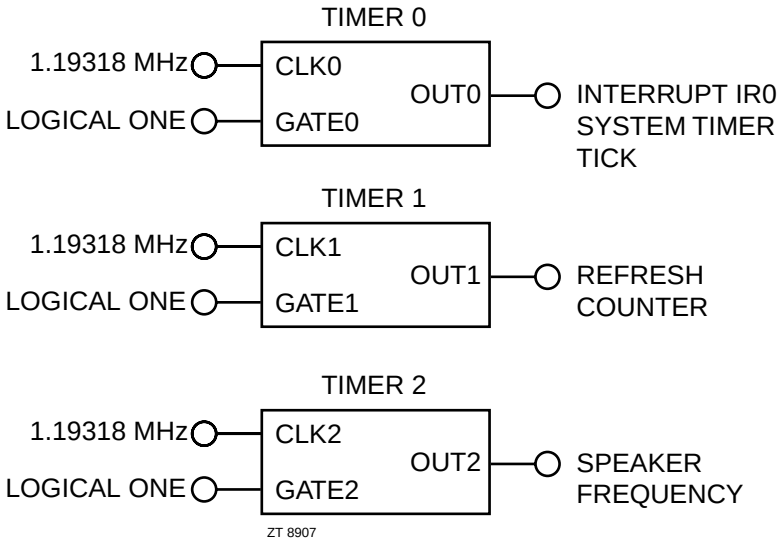
The other three counter/timers are auxiliary counter/timers **available to the user** for use by the application. The architecture for these is illustrated in the "Auxiliary Counter/Timer (CTC 2) Architecture" figure on the following page. The clock source for these counter/timers is selectable between the backplane clock, a local 8 MHz oscillator (default), or frontplane connector J2 by configuring cuttable traces CT4-CT6. If a frontplane clock is used, it must meet the following specifications:

- Operating frequency between DC and 10 MHz
- Rise and fall times of less than 25 ns
- Clock low and clock high times of greater than 50 ns

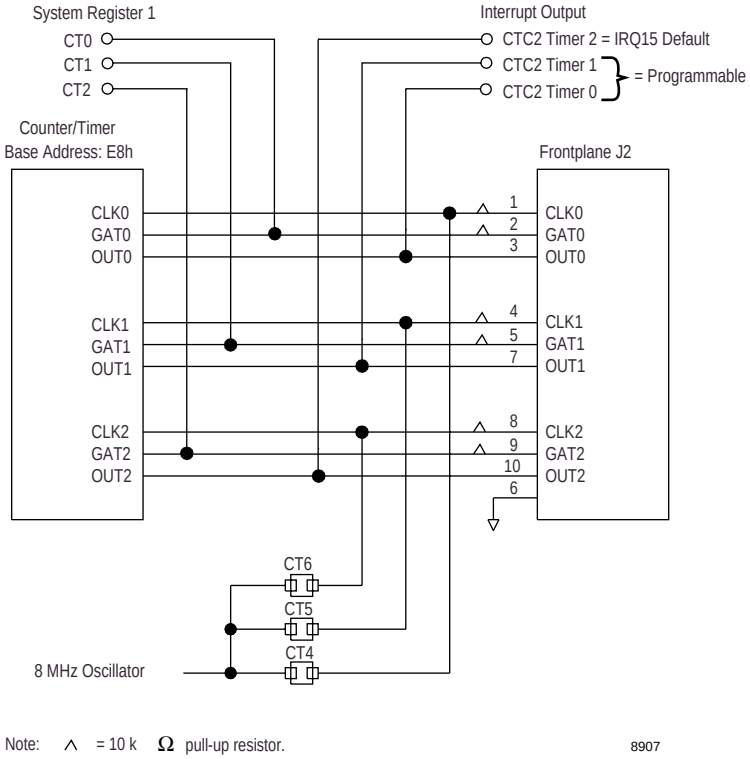
Counter/Timer Operating Modes

Mode	Counter/Timer Output Operation
0	Transitions after programmed count expires Gate enables and disables counting
1	Transitions after programmed count expires Gate triggers and retriggers counting
2	Periodic single pulse after programmed count expires Gate restarts counting
3	Square wave with frequency equal to programmed count Gate enables and disables counting
4	Single pulse after programmed count expires Gate enables and disables counting
5	Single pulse after programmed count expires Gate triggers and retriggers counting

PC-Compatible Counter/Timer (CTC 1) Architecture



Auxiliary Counter/Timer (CTC 2) Architecture



PROGRAMMABLE REGISTERS

The user-available auxiliary counter/timers are accessed through four I/O addresses, as shown in the "Auxiliary Counter/Timer (CTC 2) Register Addressing" table below. Each counter/timer occupies an I/O port address through which the preset count values are written and both the count and status information is read. The control register occupies the remaining I/O port address, which services all three counter/timers.

Auxiliary Counter/Timer (CTC 2) Register Addressing

Address	Register	Operation
00E8h	Channel 0 Count	Read/Write
00E8h	Channel 0 Status	Read
00E9h	Channel 1 Count	Read/Write
00E9h	Channel 1 Status	Read
00EAh	Channel 2 Count	Read/Write
00EAh	Channel 2 Status	Read
00EBh	Control	Write

ADDITIONAL INFORMATION

Refer to the *Ziatech Industrial BIOS for CompactPCI and STD 32 Systems* software manual for more information on the operating system's use of the counter/timers.

Refer to the Intel *82C54 CHMOS Programmable Interval Timer* data sheet for more information on the 8254 Programmable Interval Timer registers. The data sheet is available online at http://developer.intel.com/design/periphrl/datashts/231244.htm.

The data sheet is in Adobe Acrobat format (PDF). If you do not have the Acrobat Reader, it is available on the Adobe Home Page at www.adobe.com.

6. DMA CONTROLLER

The ZT 8907 includes two cascaded, Intel 8237-compatible Direct Memory Access controllers that provide a programmable interface for direct transfers between peripherals and main memory. Seven channels of DMA are available from the two cascaded 8237 DMA controllers. Up to four STD bus DMA slaves and up to two onboard (local) DMA slaves are supported, depending on configuration. DMA slaves are I/O devices that use a ZT 8907 DMA channel to transfer data to or from ZT 8907 memory. The major features of the DMA architecture are listed below.

- Independent auto-initialization
- Address increment and decrement
- Single, block, and demand transfers
- One STD bus backplane DMA channel
- Three STD bus frontplane DMA channels
- DMA transfers over the 0-16 Mbyte memory address range
- Block DMA transfer rates of greater than 2 Mbytes/sec
- One DMA channel for ECP (parallel printer) support
- One DMA channel for (optional) local floppy drive

The DMA architecture is illustrated in the "DMA Architecture" figure. The architecture includes a slave DMA controller and a master DMA controller. The slave DMA controller includes DMA channels 0 through 3. These channels are dedicated to 8-bit DMA transfers. The master DMA controller includes DMA channels 4 through 7. These channels are dedicated to 16-bit DMA transfers.

A maximum of five DMA devices may be connected to the ZT 8907 simultaneously: one DMA channel for floppy drive (either backplane or onboard), one DMA channel for onboard ECP support, and three DMA channels available through frontplane connector J6.

DMA CHANNELS

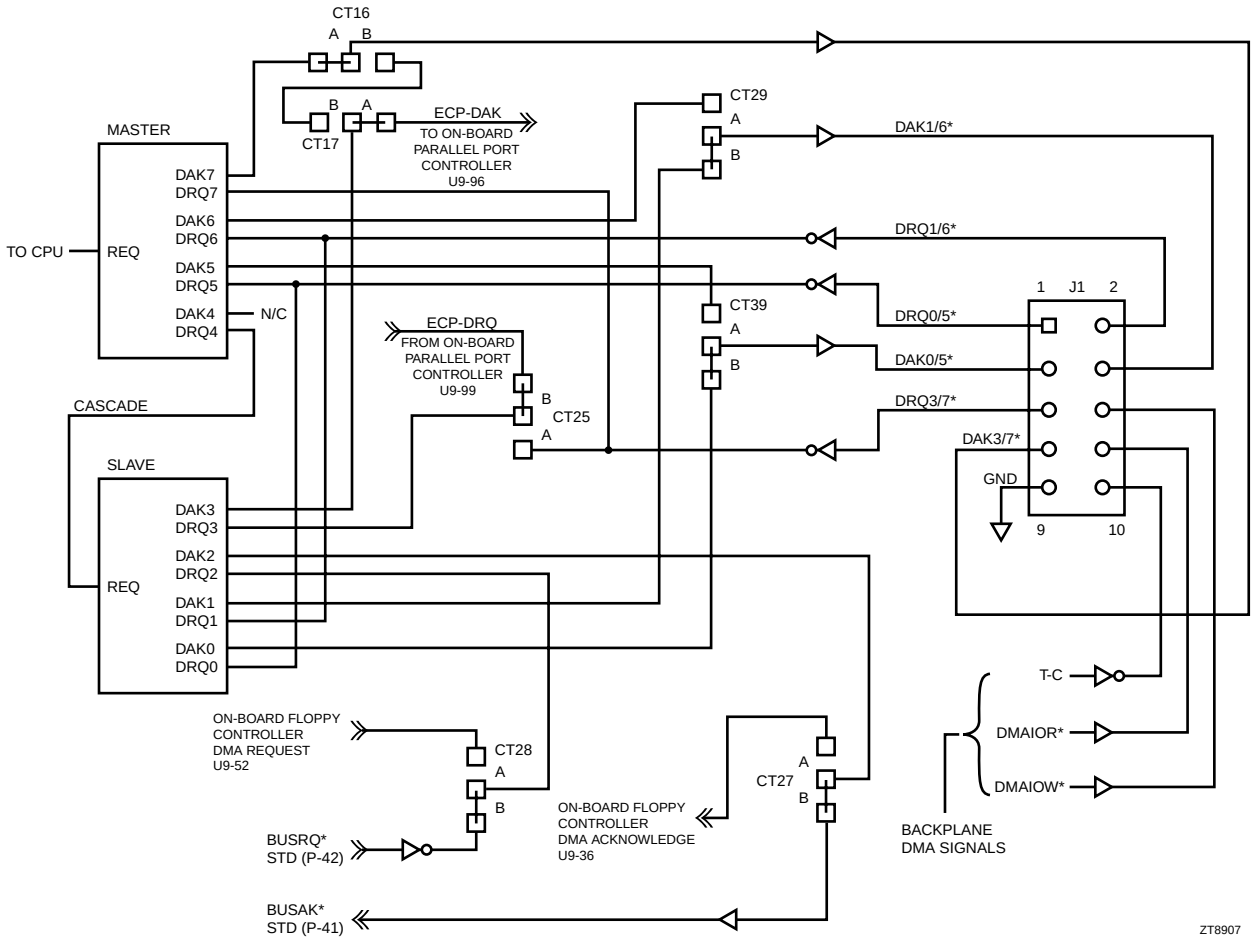
The DMA channels are summarized below.

Backplane: DMA service is available for the BUSRQ*/BUSAK signals on the STD backplane. This channel is required by the STD bus floppy disk controller and uses DMA channel 2. If a floppy disk controller is not used in the system, DMA channel 2 may be used for other peripherals. Note that if the optional local floppy option is selected it will use DMA channel 2, making the backplane DMA channel unavailable to the ZT 8907.

Frontplane: Three channels of DMA are accessible through frontplane connector J6. The three frontplane channels are independently selectable (through cuttable traces CT16, CT17, CT25, CT29, and CT39) for 8-bit or 16-bit operation. One frontplane channel supports DMA channels 0 or 5. The second frontplane channel supports DMA channels 1 or 6. The third frontplane channel supports DMA channels 3 or 7. Be sure to mask the channels not required by the application.

Local: The onboard IEEE 1284 Parallel Port (see Chapter 9 "Parallel Printer Port Interface") can be configured to use DMA channel 3 for data transfers.

DMA Architecture



OPERATING MODES

All DMA channels support the following three operating modes:

Single Mode: The DMA controller executes a single transfer for each DMA cycle. The count is adjusted by one for each transfer. A terminal count is generated when the count changes between 0 and FFFFh.

Block Mode: The DMA controller executes repetitive transfers for each DMA cycle. The count is adjusted by one for each transfer. A terminal count is generated when the count changes between 0 and FFFFh. The transfers end on the assertion of terminal count.

Demand Mode: The DMA controller executes repetitive transfers for each DMA cycle. The count is adjusted by one for each transfer. A terminal count is generated when the count changes between 0 and FFFFh. The transfers end on the assertion of terminal count or the removal of DMA request.

DMA Slave Operation

1. The DMA slave generates an STD bus BUSRQ* or a frontplane DMA request.

2. The system controller gains control of STD bus resources (multiple master only). The system controller is hardware local to the ZT 8907 that manages the STD bus interface.

3. The system controller generates a DMA request to the DMA controller if the **Bus Own** bit (bit 5 of System Register 3 (E5h)) is active. In a single master system, this bit is held active. In a multiple master system, this bit is software controlled to direct the DMA request to a single destination.

4. The DMA controller (programmed to perform a DMA transfer) gains control of local resources and generates a DMA acknowledge to the system controller.

5. The system controller generates an STD bus BUSAK* or a frontplane DMA acknowledge.

6. The DMA controller generates an STD bus or frontplane I/O strobe and a local memory cycle to complete the data transfer.

PROGRAMMABLE REGISTERS

Each DMA controller is managed through the 16 I/O port addresses shown in the table "Slave DMA I/O Port Addressing" on the following page. Page registers extend the 16-bit DMA address to the full 24-bit address space available on the ZT 8907. I/O port addressing for the DMA page registers is given in the "DMA Page I/O Port Addressing" table below.

Note: The ZT 8907 only supports DMA into the lower 16 Mbytes of DRAM memory and does not support DMA Extended Page I/O Port addressing. Windows 95 users with more than 16 Mbytes of RAM must ensure that their DMA controller properties are set to restrict DMA transfers to memory below 16 Mbytes. Windows 95 may not auto-detect these settings.

DMA Page I/O Port Addressing

Address	Register	Operation
87h	Channel 0 A16-23 Address	Read/Write
83h	Channel 1 A16-23 Address	Read/Write
81h	Channel 2 A16-23 Address	Read/Write
82h	Channel 3 A16-23 Address	Read/Write
8Bh	Channel 5 A16-23 Address	Read/Write
89h	Channel 6 A16-23 Address	Read/Write
8Ah	Channel 7 A16-23 Address	Read/Write

Slave DMA I/O Port Addressing

Address			
Slave	**Master**	**Register**	**Operation**
0	C0	Channel 0 Base/Current Address	Write
		Channel 0 Current Address	Read
1	C2	Channel 0 Base/Current Count	Write
		Channel 0 Current Count	Read
2	C4	Channel 1 Base/Current Address	Write
		Channel 1 Current Address	Read
3	C6	Channel 1 Base/Current Count	Write
		Channel 1 Current Count	Read
4	C8	Channel 2 Base/Current Address	Write
		Channel 2 Current Address	Read
5	CA	Channel 2 Base/Current Count	Write
		Channel 2 Current Count	Read
6	CC	Channel 3 Base/Current Address	Write
		Channel 3 Current Address	Read
7	CE	Channel 3 Base/Current Count	Write
		Channel 3 Current Count	Read
8	D0	Status	Read
		Command	Write
9	D2	Write Request	Write
A	D4	Write Single Mask	Write
B	D6	Write Mode	Write
C	D8	Clear Byte Pointer	Write
D	DA	Clear Master	Write
E	DC	Clear Mask	Write
F	DE	Write Mask	Write

7. REAL-TIME CLOCK

The ZT 8907 includes one Motorola 146818-compatible real-time clock. The real-time clock provides clock and 100-year calendar information in addition to 114 bytes of CMOS setup static RAM. These functions are battery backed for continuous operation even in the absence of system power.

The RAM is used by the operating system BIOS to store configuration information. The system BIOS is also Year 2000 Compliant. For more information on battery backing, see Chapter 16, "Memory Module Socket (U17)". The major features of the real-time clock are listed below.

- Battery backed
- Leap year compensation
- Optional interrupt generation
- Optional Daylight Savings Time compensation
- Timekeeping to a 1 second resolution
- 114 bytes of CMOS setup RAM

PROGRAMMABLE REGISTERS

The real-time clock includes 128 register locations. These registers are accessed through I/O port locations 70h and 71h. A real-time clock register is accessed by first writing the offset address of the register to I/O port location 70h. Data is then transferred to or from the register through I/O port location 71h. This sequence must be repeated to read the same register a second time. The I/O port addressing for the real-time clock is given in the "Real-Time Clock Register Addressing" table below.

I/O port location 70h is a write only register. Bit 7 of this register is used to enable/disable the non-maskable interrupt (bit 7 = 1: NMI disabled, bit 7 = 0: NMI enabled). I/O port location 70h bits 6-0 are used for the offset address. Any write to I/O port location 70h should be followed by an action to I/O port location 71h, otherwise the real-time clock could be left in an undefined state.

Real-Time Clock Register Addressing

Offset Address	Function	Range
0h	Time-Seconds	0-59
1h	Alarm-Seconds	0-59
2h	Time-Minutes	0-59
3h	Alarm-Minutes	0-59
4h	Time-Hours (12 hour mode)	1-12
4h	Time-Hours (24 hour mode)	0-23
5h	Alarm-Hours	0-23
6h	Day of Week	1-7
7h	Date of Month	1-31
8h	Month	1-12
9h	Year	0-99
Ah-Dh	Register A-D	----
Eh-7Fh	General Purpose	----

ADDITIONAL INFORMATION

Refer to the Acer Labs *FINALI-486 M1487/M1489 486 PCI Chip Set Preliminary Data Sheet* for more information on the real-time clock operating modes.

8. SERIAL CONTROLLER

The ZT 8907 includes two serial ports that are compatible with the industry standard 16C550. The interface for each serial port is implemented with a 5 V charge pump technology to eliminate the need for a ±12 V supply. The serial ports include a complete set of handshaking and modem control signals, maskable interrupt generation, and data transfer rates up to 115.2 Kbaud. The major features of the serial ports are listed below.

- Loopback diagnostics
- Does not require ±12 V
- Baud rates up to 115 Kbaud
- Two independent RS-232 channels
- Polled and interrupt operation

The serial ports are configured as DTE and are available through 10-pin frontplane connectors J3 (COM2) and J4 (COM1). Optional cables interface the frontplane connectors to 9-pin D-shell connectors. Ziatech also offers a ZT 2592 RS-232-to-RS-485 interface conversion frontplate for the ZT 260/ZT 310 enclosures. The ZT 2592 is also offered in an optically isolated version.

Note: Pins 1 through 9 of J3 and J4 are organized for direct ribbon cable connection to a 9-pin D-shell connector. Pin 10 is a 5 V output.

PROGRAMMABLE REGISTERS

There are seven registers for initializing and controlling each serial channel. The "Serial Controller Register Addressing" table below shows the I/O port addressing for these registers. COM1 is located at address 3F8-3FFh; COM2 is located at address 2F8-2FFh.

Screen 1 of the BIOS SETUP utility allows you to disable COM1 and/or COM2 and free up that address range for STD bus expansion.

Serial Controller Register Addressing

Address	Register	Operation
0xF8h (DIV=0)	Receive Buffer	Read
0xF8h (DIV=0)	Transmit Buffer	Write
0xF8h (DIV=1)	Divisor Latch LSB	Read/Write
0xF9h (DIV=0)	Interrupt Control	Read/Write
0xF9h (DIV=1)	Divisor Latch MSB	Read/Write
0xFAh	Interrupt Status	Read
0xFAh	FIFO Control	Write
0xFBh	Line Control	Read/Write
0xFCh	Modem Control	Read/Write
0xFDh	Line Status	Read
0xFEh	Modem Status	Read
0xFFh	Reserved	

Note: COM1 is located at address 3F8-3FFh; COM2 is located at address 2F8-2FFh.

ADDITIONAL INFORMATION

Refer to the *Standard Microsystems Corporation™ FDC37C665GT* data book for more information on the serial controller operating modes. The data sheet is available online at http://www.smsc.com/main/catalog/fdc37c665gt.html

The data sheet is in Adobe Acrobat format (PDF). If you do not have the Acrobat Reader, it is available on the Adobe Home Page at http://www.adobe.com/.

9. PARALLEL PRINTER PORT INTERFACE

The ZT 8907 supports a Centronics™-compatible printer port interface, available through connector J9. The printer port is configurable for normal ("nibble mode") or extended ("bi-directional mode") through screen 2 of the BIOS SETUP utility.

The ZT 90157 cable assembly (shown in the "Cables" section in Appendix B) allows the onboard LPT1 channel to be interfaced directly to 25-pin D-Shell parallel port devices, as used in PC applications. The onboard port may be disabled through screen 2 of the BIOS SETUP utility to allow use of STD 32 based parallel interfaces.

PARALLEL PRINTER PORT CONFIGURATION OPTIONS

The different modes for the printer port are described below. Details for the parallel port on the ZT 8907 are discussed in the following topics. Shown in parenthesis is the description for each of the modes as presented in screen 2 of the BIOS SETUP utility.

Parallel Port Mode	Description	Max. Data Rate
Compatibility (Normal)	Uni-directional data configuration. The original PC-AT Mode. Also known as "nibble mode" because the four status bits in the cable are used for feedback from devices such as tape back-up units (when restoring data from a tape). Software based protocol.	50-150 Kbits/s
Extended (Ext)	Bi-directional data transfer capability. Similar to Compatibility mode, but allows 8-bit data in both directions; faster for interfaces needing to supply data to the computer (such as scanners, tape back-up); software based protocol.	50-150 Kbits/s

ADDRESS MAPPING

The address mapping for the PC standard architecture and the ZT 8907 is shown below. The onboard port may be disabled through screen 2 of the BIOS SETUP utility to allow an STD 32 LPT port to be used.

Parallel Port	PC Port Address	ZT 8907 Port Address
LPT1	3BC (typically)	378-37B - Compatibility, Extended

INTERRUPT SELECTION

The interrupt mapping for the PC standard architecture and the ZT 8907 is shown below.

Parallel Port	PC Interrupt	ZT 8907 Interrupt
LPT1	IR5	IR7 or disabled for off-board LPT support

PROGRAMMABLE REGISTERS

There are three registers for the compatibility/extended mode parallel port interface. The "Compatibility/Extended Mode Parallel Port Interface Addressing" table below shows the I/O port addressing.

Compatibility/Extended Mode Parallel Port Interface Addressing

Address	Register	Operation
0378h	Line Printer Data	Read/Write
0379h	Line Printer Status	Read
037Ah	Line Printer Control	Read/Write

ADDITIONAL INFORMATION

Refer to the *Standard Microsystems® FDC37C665GT* data book for more information on the parallel controller operating modes. The data sheet is available online at http://www.smsc.com/main/catalog/fdc37c665gt.html.

The data sheet is in Adobe Acrobat format (PDF). If you do not have the Acrobat Reader, it is available on the Adobe Home Page at www.adobe.com.

10. PARALLEL I/O

The ZT 8907 includes six 8-bit parallel ports for a total of 48 I/O signals. Three of the 8-bit ports are available to the user through connector J5. The remaining three parallel ports are dedicated to controlling an monitoring local operations. The general operation of the six parallel ports is explained in this chapter. The specific features managed by the dedicated ports are presented in the register drawings in "System Registers," Chapter 11.

Each of the 25 parallel I/O signals is configured as an input or an output with readback under software control. The major features of the parallel I/O are listed below.

- 12 mA sink current
- Stable outputs during power up and reset
- Continuous data transfer rates up to 1 Mbyte/second
- Each I/O signal is independently programmable as an input or an output with readback
- Optional cable for direct connection to industry-standard I/O module mounting racks
- Event sensing and debouncing on all ports under software control

FUNCTIONAL DESCRIPTION

The parallel I/O signals are supported through the 16C50A Digital I/O ASIC, a custom ASIC device designed by Ziatech.

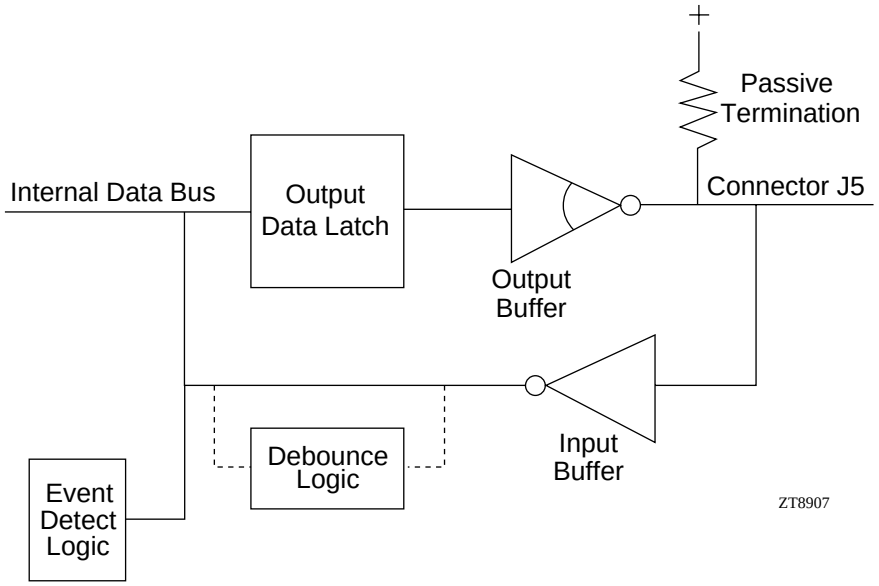
The 16C50A Digital I/O ASIC supports standard and enhanced operating modes. Standard mode is not available to ZT 8907 users; enhanced operating mode is automatically configured by the ZT 8907 BIOS. There are three register banks (see the "Programmable Registers" topic later in this chapter) used for controlling the device's features. These register banks are selected by programming bits 6 and 7 of I/O port E7h with a "00" for bank 0, and a "01" for bank 1, and a "10" for bank 2.

The "Parallel Port Functional Diagram" on the following page shows the internal circuitry of each I/O signal. The diagram includes an output latch, an output buffer, and an input buffer. These functional blocks are described in the following topics.

Refer to Appendix C, "Digital I/O ASIC System Setup Considerations," for tips on preventing latchup from the CMOS parts in the 16C50A Digital I/O ASIC.

Three ports of the on-board 16C50A Digital I/O ASIC device are used for system registers to monitor and control other board functions. These registers are illustrated in Chapter 11, "System Registers."

Parallel Port Functional Diagram



Output Latch

The output latch stores the data present on the internal data bus during a write operation to the parallel port. The data is latched until altered by another parallel port write, until a system reset, or until the power is turned off. The output latch is initialized with a logical 0 during power on and system reset.

Output Buffer

The output buffer isolates the output latch from connector J5. The output buffer is an inverting open-collector device with 12 mA of sink current and glitch-free operation during power cycles. The inversion means that a logical 0 written to the parallel port appears as a TTL high at connector J5, and a logical 1 written to the parallel port appears as a TTL low at connector J5.

The open collector feature permits each parallel I/O signal to be software configured as an input. To use a parallel port signal as an input, a logical 0 must first be written to the output latch. This causes the output buffer to become an open-collector gate and prevents contention with the input signal. The passive termination ranges from 25 k Ω minimum to 120 k Ω maximum. Applications needing a predictable rise time should provide additional termination.

Input Buffer

The input buffer is enabled during read operations to transfer the data from connector J5 to the internal data bus. If the parallel port bit is configured as input, the data read is the data driven by an external device.

The input buffer is an inverting device. This means that data read from the parallel port as a logical 0 is a TTL high at connector J5, and data read from the parallel port as a logical 1 is a TTL low at connector J5.

Debounce Control Logic

The debounce control logic is a feature of the 16C50A Digital I/O ASIC. This feature eliminates the need for external logic or extensive software to remove unstable input signals to the Digital I/O ASIC. The internal circuitry of the Digital I/O ASIC automatically filters out glitches that can occur in received signals.

For example, if the Digital I/O ASIC is programmed for an 8 ms period, the incoming signal must be stable for the entire 8 ms period, with no glitches, before it is recognized by the Digital I/O ASIC.

The debounce control logic is controlled on the 16C50A by registers E0h, E1h, E2h, and E3h in register bank 2. An 8 MHz clock is used by the 16C50A for a timing reference, thus allowing the debounce circuit to be programmed for a debounce delay of 4 µs, 64 µs, 1 ms, or 8 ms.

Upon initialization of the debounce circuitry, be sure to delay at least the programmed debounce time before reading any of the input ports or the external event signals. This guarantees that the input data is valid prior to being used by the software.

Event Sense Detection Logic

The 16C50A Digital I/O ASIC contains event sense logic that allows detection of either positive or negative events. The event input edge is controlled on a nibble basis by software. The event bits are enabled on an individual basis.

Registers E0-E6h in Register Bank 1 are used to control and monitor the event sense logic. The Event Sense interrupt can be assigned to IRQ15 by modifying the default configuration of cuttable trace CT7. Be sure to see the topic "CT7, CT8 (IRQ15 Input Source Selection)" in Appendix A for a table showing the proper configuration.

Note that modifying cuttable traces requires soldering ability. Incorrect modifications by the user could void the product warranty. Contact Ziatech for custom configuration.

To use the event inputs:

1. Determine which events are to be enabled and what polarity is to be detected, high to low (negative) or low to high (positive) transitions.

2 Set each port to the desired polarity.

3. Enable each of the event inputs to be detected.

All I/O and external event inputs are reset to negative events, and disabled after a Reset signal has occurred.

PROGRAMMABLE REGISTERS

The 16C50A Digital I/O ASIC supports standard and enhanced operating modes. Standard mode is not available to ZT 8907 users; enhanced operating mode is automatically configured by the ZT 8907 BIOS. There are three register banks used for controlling the device's features. These register banks are selected by programming bits 6 and 7 of I/O port E7h with a "00" for **bank 0**, a "01" for **bank 1**, and a "10" for **bank 2**. The six 8-bit ports are allocated as follows:

- Enhanced Bank 0 I/O Port Addressing
- Enhanced Bank 1 I/O Port Addressing
- Enhanced Bank 2 I/O Port Addressing

Enhanced Bank 0 I/O Port Addressing

Select this register bank by programming bits 6 and 7 of I/O port E7h with a "00".

Address	Register	Read Operation	Write Operation
00E0h	Port 0 Data	MOD00-MOD07	MOD00-MOD07
00E1h	Port 1 Data	MOD00-MOD08	MOD00-MOD15
00E2h	Port 2 Data	MOD00-MOD16	MOD00-MOD23
00E3h	Port 3 Data	System Register	System Register
00E4h	Port 4 Data	System Register	System Register
00E5h	Port 5 Data	System Register	System Register
00E6h	Reserved	-----	-----
00E7h	Write Inhibit/ Bank Address	Status	Control

Enhanced Bank 1 I/O Port Addressing

Note: Select this register bank by programming bits 6 and 7 of I/O port E7h with a "01".

Address	Register	Read Operation	Write Operation
00E0h	Port 0 Event Sense	Status	Control
00E1h	Port 1 Event Sense	Status	Control
00E2h	Port 2 Event Sense	Status	Control
00E3h	Port 3 Event Sense	Reserved	Reserved
00E4h	Port 4 Event Sense	Reserved	Reserved
00E5h	Port 5 Event Sense	Reserved	Reserved
00E6h	Event Sense Manage	Status	Control
00E7h	Bank Address	Status	Control

Enhanced Bank 2 I/O Port Addressing

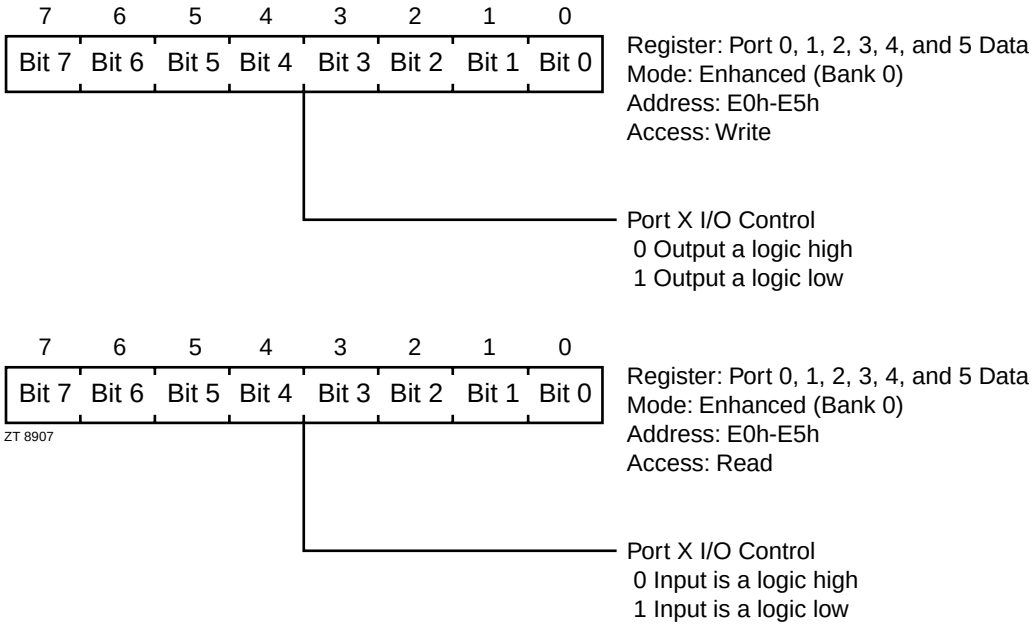
Note: Select this register bank by programming bits 6 and 7 of I/O port E7h with a "10".

Address	Register	Read Operation	Write Operation
00E0h	Debounce Configure	Status	Control
00E1h	Debounce Duration	Status	Control
00E2h	Debounce Duration	Status	Control
00E3h	Debounce Clock	-----	Control
00E4h	Reserved	-----	-----
00E5h	Reserved	-----	-----
00E6h	Reserved	-----	-----
00E7h	Bank Address	Status	Control

Port Data Registers

The six I/O ports assign the least significant I/O line to the least significant data line (D0). Each bit is changed or monitored by writing or reading the individual I/O port. On a power up or reset, the ports are reset to 0, forcing the outputs to be set high.

Parallel Port Data Registers



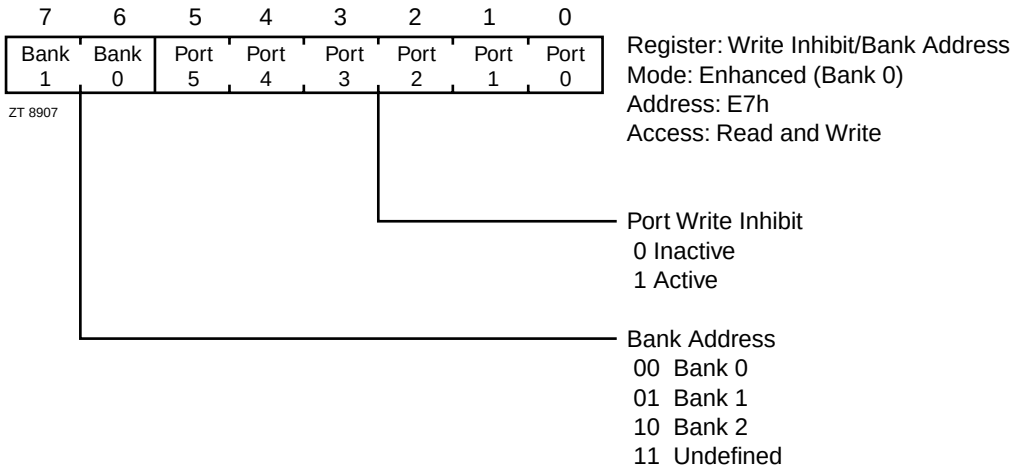
Note: To set a particular port and bit as an input, write a logic 0 to that port and bit.

Write Inhibit / Bank Address Register

The Write Inhibit/Bank Address Register is used to mask the ability to write data to the six output ports. Power-up default has the register unmasked to allow writes to the output ports. Writing the Write Inhibit/Bank Address Register bits 0-5 with a 1 masks I/O ports 0 - 5, respectively, while a read returns the status of the Write Inhibit/Bank Address Register.

Bits 7 and 6 of the register determines which bank of registers is selected. A logic 00 selects bank 0, a 01 selects bank 1, and 10 selects bank 2, respectively. A logic 11 is an invalid state and should never be written to the Write Inhibit/Bank Address Register.

Parallel Port Write Inhibit / Bank Address Register

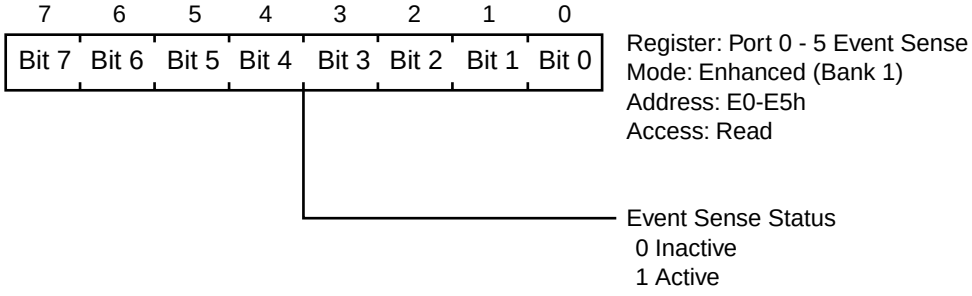


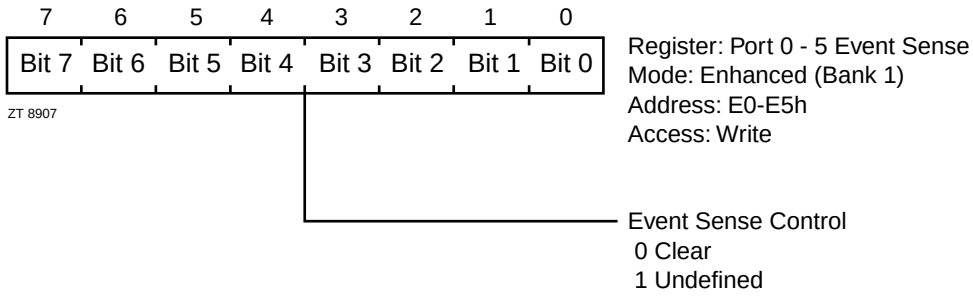
Port Event Sense Register

Reading the event sense status of each port gets the status of each I/O port sense line. Writing to the event sense status of each port with the corresponding bit equal to 0 clears that particular sense line.

When writing ports 0 - 5, each data bit written with a logic 0 clears its corresponding event sense flip-flop. Each data bit of ports 0 - 5 must be written with a 1 to re-enable the corresponding event sense input after it is cleared. Reading ports 0 - 5 returns the event sense flip-flop status.

Parallel Port Event Sense Register



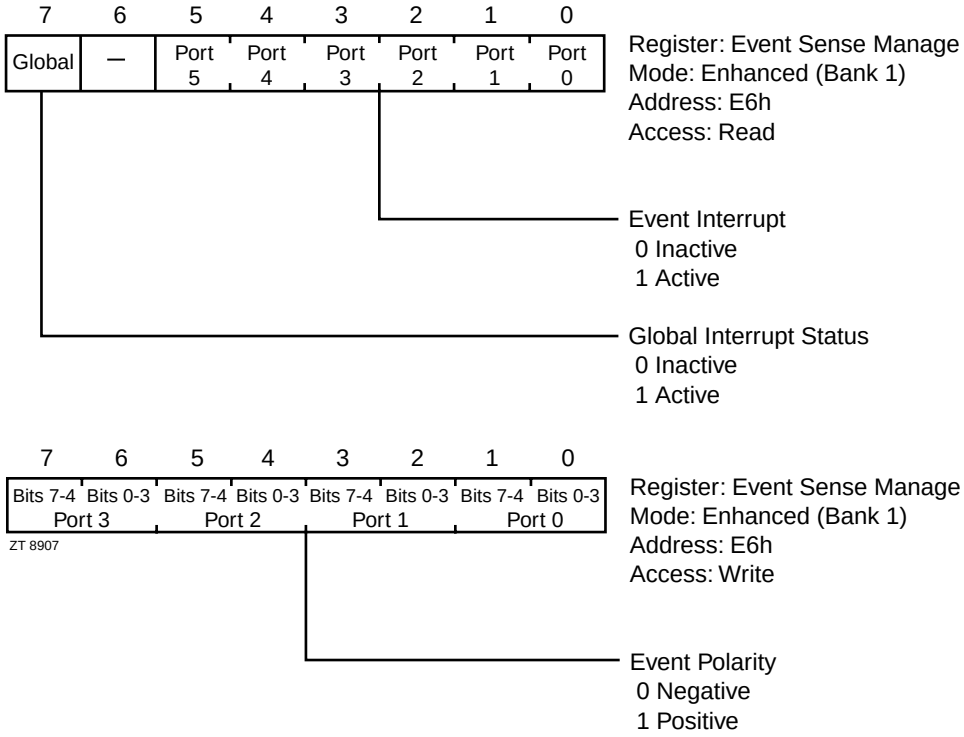


Event Sense Manage Register

A write to this register controls the polarity of the Sense Event for I/O ports 0 - 3. Each bit represents a nibble (4 bits) of the port. A logic 0 senses negative events, while a 1 senses positive events. The polarity of the event sense logic must be set prior to enabling the event input logic.

A read from this register returns the event status on I/O ports 0 - 5 and the status of the interrupt pin. Bit 7, the global interrupt pin, indicates an event sense was detected on any of the six ports (1 = interrupt is asserted).

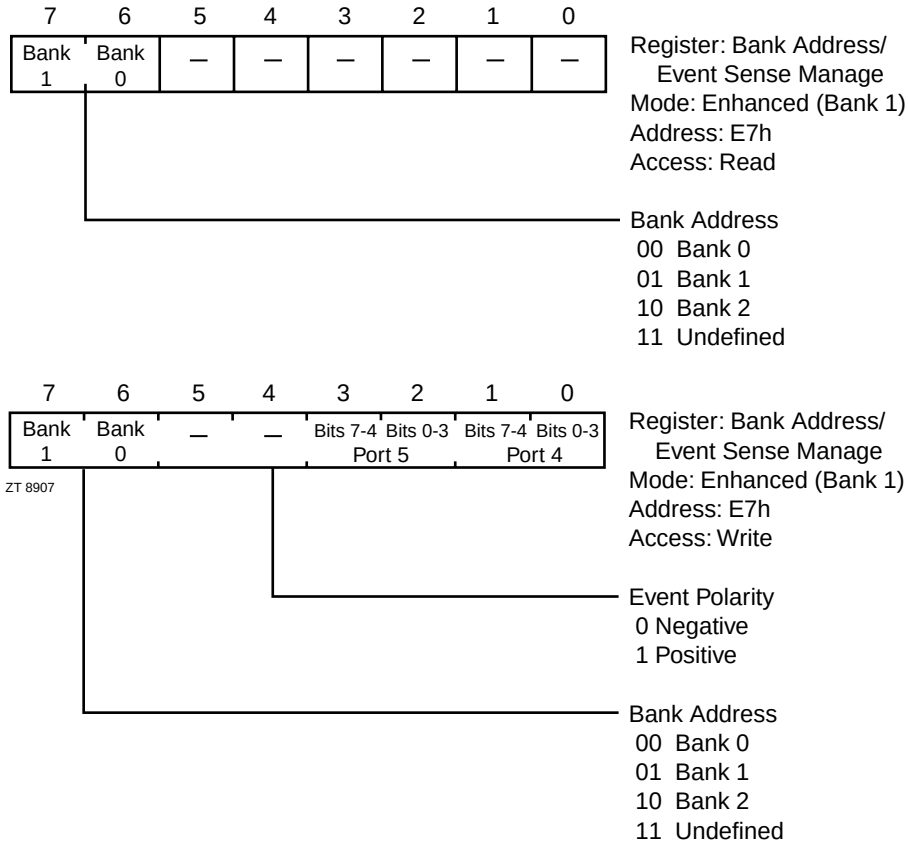
Parallel Port Event Sense Manage Register



Bank Address Register

This register controls the polarity of the Sense Event for I/O ports 4 and 5. A 0 senses negative events, while a 1 senses positive events. Bits 6 and 7 select an individual bank. A read from this register returns only the bank status information.

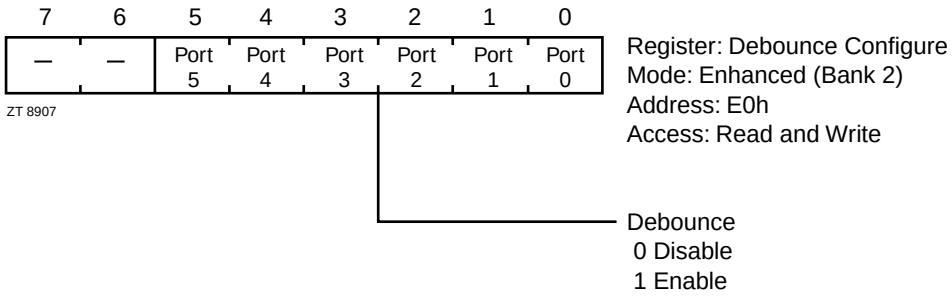
Parallel Port Bank Address Register



Debounce Configure Register

This register controls whether each individual port is passed through the debounce logic. A logic 0 disables the debounce logic, and a logic 1 enables the debounce logic.

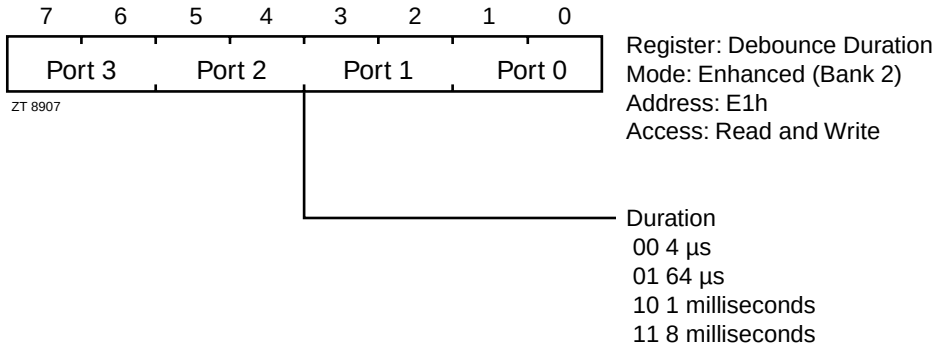
Parallel Port Debounce Configure Register



Debounce Duration Register (Ports 0-3)

This register controls the duration required by each input signal before it is recognized for ports 0 - 3. The debounce times available are 4 µs, 64 µs, 1 ms, and 8 ms. A debounce value of 00 sets 4 µs, 01 sets 64 µs, 10 sets 1 ms, and 11 sets 8 ms. This register controls ports 0 - 3. The default value is 00 for a 4 µs debounce period.

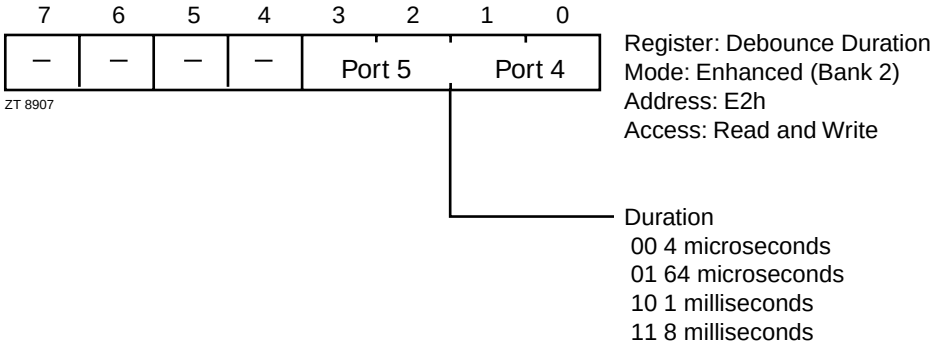
Parallel Port Debounce Duration Register (Ports 0-3)



Debounce Duration Register (Ports 4-5)

This register controls the duration required by each input signal before it is recognized for ports 4 and 5. The debounce times available are 4 µs, 64 µs, 1 ms, and 8 ms. A debounce value of 00 sets 4 µs, 01 sets 64 µs, 10 sets 1 ms, and 11 sets 8 ms. This register controls ports 4 and 5. The default value is 00 for a 4 µs debounce period.

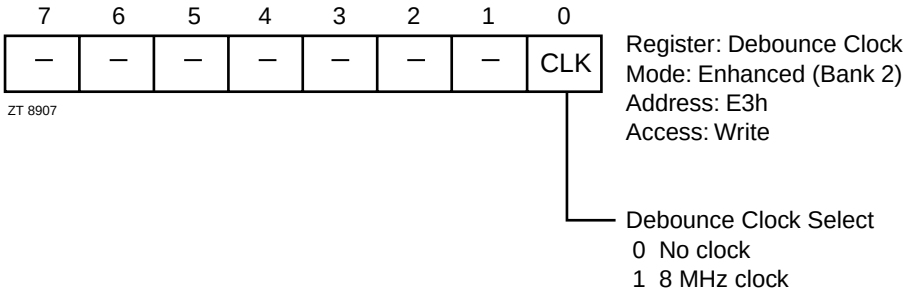
Parallel Port Debounce Duration Register (Ports 4-5)



Debounce Clock Register

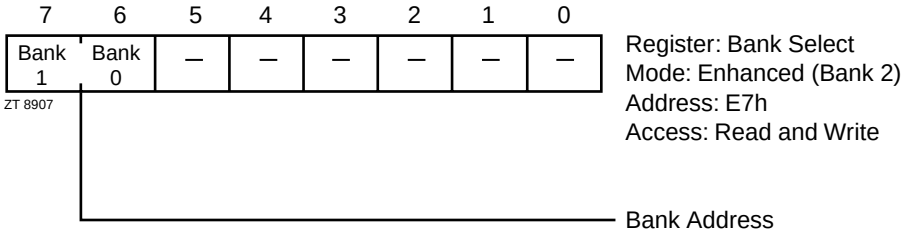
This bit must be set to a 1 to use the debounce feature. The default value is 0. A read from this port is undefined.

Parallel Port Debounce Clock Register



Bank Select Register

Parallel Port Bank Select Register



Register: Bank Select
Mode: Enhanced (Bank 2)
Address: E7h
Access: Read and Write

Bank Address
00 Bank 0
01 Bank 1
10 Bank 2
11 Undefined

11. SYSTEM REGISTERS

The ZT 8907 uses three ports of the onboard 16C50A Digital I/O ASIC device for system registers. These registers are mapped to I/O ports E3h through E5h and are illustrated in the following topics.

- For more information on how the Digital I/O ASIC works, see Chapter 10, "Parallel I/O," section heading "Functional Description".
- Refer to Appendix C, "Digital I/O ASIC System Setup Considerations," for tips on preventing latchup from the CMOS parts in the 16C50A.
- Note that the Digital I/O ASIC inputs are inverting; thus, a logic high (+5 V) will be read as a logic low (0 V).

The 16C50A operating instructions are outlined below.

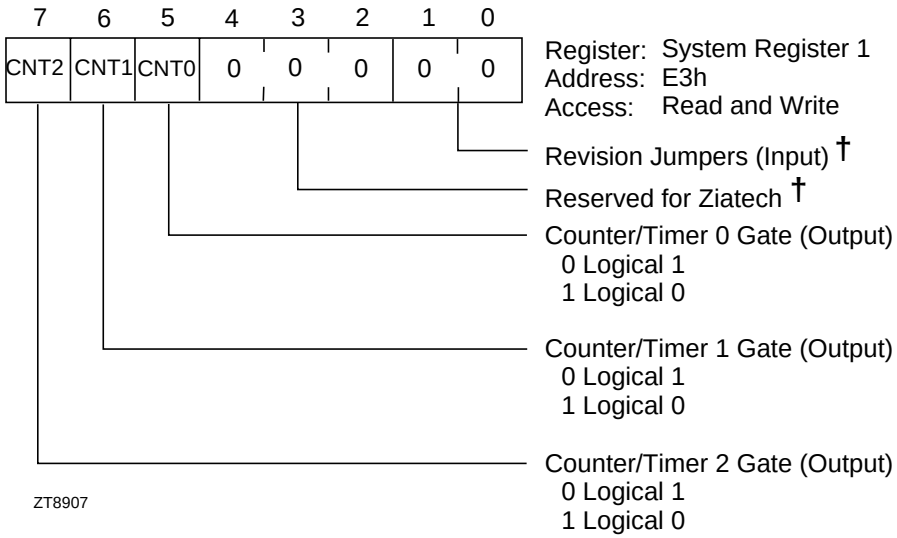
- The reset state for all bits is a logical 0.
- Unless specifically noted otherwise, bits dedicated to input operation must remain programmed with a logical 0 to prevent contention with the input device.
- Bits dedicated to output operation have readback capabilities.

PROGRAMMABLE REGISTERS

The following topics illustrate System Registers 1, 2, and 3.

System Register 1

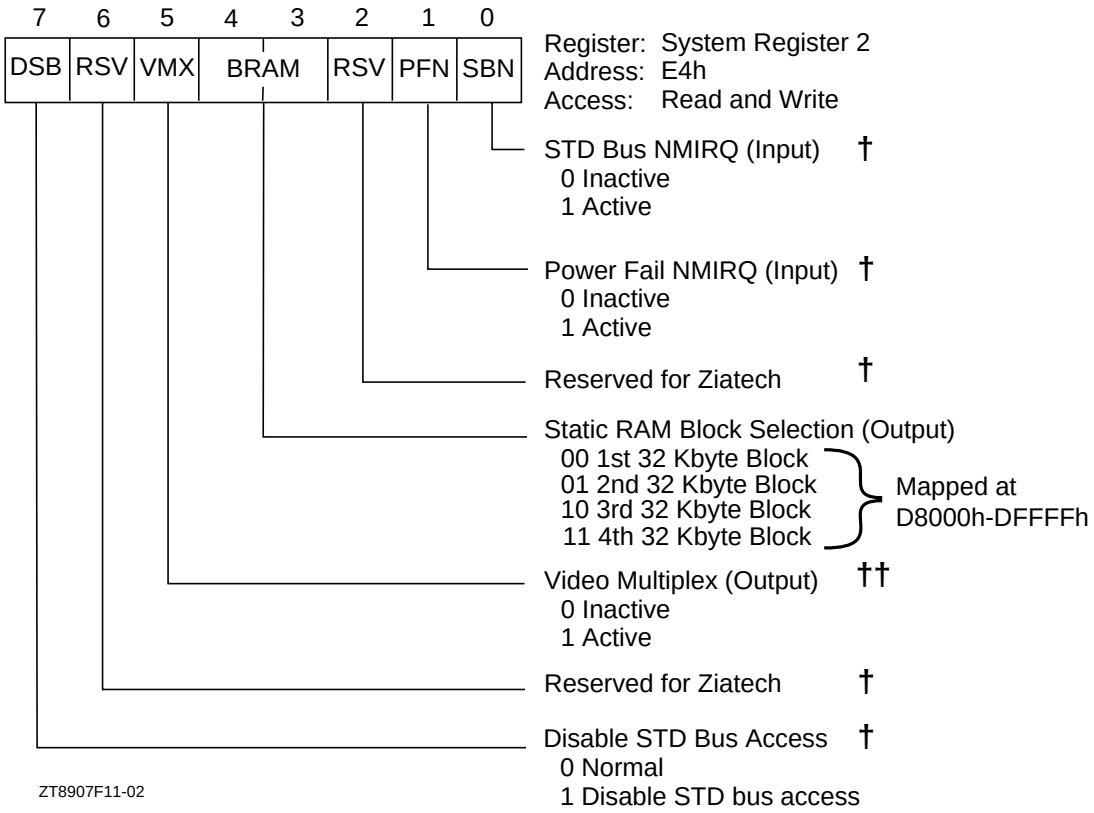
Digital I/O ASIC System Register 1



† Always write these bits as zero.

System Register 2

Digital I/O ASIC System Register 2

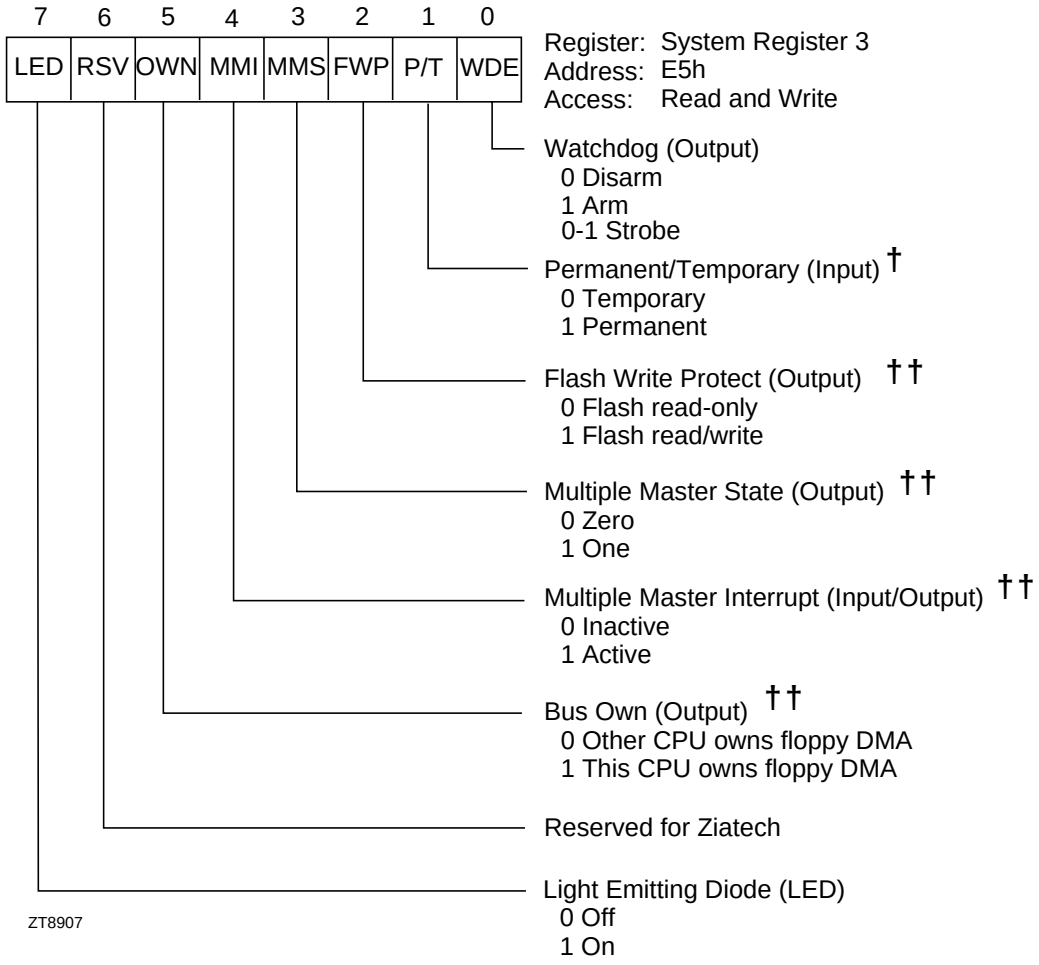


† Always write these bits as zero.

†† Register bits managed by Ziatech operating system software.

System Register 3

Digital I/O ASIC System Register 3



† Always write this bit to the same value as Read. DO NOT change the state of this bit

†† Register bits managed by Ziatech operating system software.

Note: Be sure to use the code fragments listed in Chapter 12 "Watchdog Timer" and Chapter 14 "Programmable LED" before writing to this register. It is critical for STAR SYSTEM operation that the state of bits 1, 3, 4, 5, and 6 be maintained as the code fragments indicate.

ADDITIONAL INFORMATION

The ZT 8907 includes several other system registers that are exclusively managed by Ziatech operating system software. These registers are located in the ALi chipset. Refer to the Acer Labs *FINALI-486 M1487/M1489 486 PCI Chip Set Preliminary Data Sheet* for more information on these registers.

12. WATCHDOG TIMER

The primary function of the watchdog timer is to monitor ZT 8907 operation and to take corrective action if the system fails to function as programmed. The major features of the watchdog timer are listed below.

- Enabled and disabled through software control
- Armed and strobed through software control
- Generates a CPU reset if allowed to time out

WATCHDOG TIMER OPERATION

The watchdog timer is armed and strobed with bit 0 of the Digital I/O ASIC's System Register 3 (E5h) (refer to Chapter 11, "System Registers"). The watchdog timer is disabled after power on or system reset. Writing a logical 1 to the watchdog timer bit arms the watchdog timer.

Once armed, the watchdog timer must be strobed with a periodic frequency less than the timeout period or a system reset is generated. The factory configured timeout period is 550 ms. The watchdog timer is strobed by first writing a logical 0 to WDE, immediately followed by writing a logical 1 to WDE.

The following code shows the procedure for arming and strobing the watchdog timer.

```
;-------------------------------------
; The multiple master interrupt is
; a bi-directional bit.  The current
; software state of multiple master
; interrupt is maintained in the
; multiple master state bit. Input_e5
; updates the multiple master bit with
; the current software state maintained
; in the multiple master state bit.
;-------------------------------------

input_e5    macro
            local   multiple_on
            in      al,0e5h
            test    al,8
```

```
            jnz     multiple_on
            and     al,not 10h
multiple_o
n:
            endm

;---------------------------------------------------------------
; strobe_wd strobes and re-arms the watchdog timer.
; The state of Bit 1 must be maintained (write the same value
as was read).
; Bits 3 & 4 must be handled as shown in the input_e5 macro
;---------------------------------------------------------------
strobe_wd   pushf
            cli
            input_
            e5
            and     al,not 1
            out     0e5h,al
            or      al,1
            out     0e5h,al
            popf
            ret
```

ADDITIONAL INFORMATION

The chip used for the watchdog timer is a DS 1238A. Refer to the Dallas Semiconductor *DS1705/DS1706 3.3 and 5.0 V MicroMonitor*™ data sheet for more information on the watchdog timer and the associated operating modes. The data sheet is available online at http://www.dalsemi.com/DocControl.

The data sheet is in Adobe Acrobat format (PDF). If you do not have the Acrobat Reader, it is available on the Adobe Home Page at http://www.adobe.com.

13. PCI MEZZANINE LOCAL BUS

The ZT 8907 includes a PCI compatible local bus interface (J13) to CompactPCI mezzanine devices. The PCI mezzanine bus operates at the same speed as the CPU *external* clock speed. Ziatech offers PCI peripheral adapters designed specifically for this local bus interface. These adapters provide superior performance over STD bus solutions by running with up to four times the data width and up to four times the operating frequency. Major features of the PCI interface are listed below.

- 25 or 33 MHz operation (determined by CPU speed)
- Reduces STD bus traffic by keeping all PCI operations local
- Single-slot occupancy capable (VGA)

See the section, "Removing The zPM Mezzanine Card," in Chapter 2 for details about the mechanical connection of mezzanine devices to Ziatech CPUs.

PCI OPERATION FREQUENCY

The PCI operating frequency is derived from the frequency at which the 486 CPU is operating. The 486 is available with several different internal clock multipliers (1X, 2X, and 3X).

Processor Speed (MHz)	Internal Clock Multiplier	External Processor Speed	PCI Operating Frequency
25	1X	25.0	25.0
33	1X	33.3	33.3
100	3X	33.3	33.3

ADDITIONAL INFORMATION

Refer to the individual peripheral data sheets for additional details and for installation and operating instructions.

14. PROGRAMMABLE LED

The ZT 8907 includes a Light-Emitting Diode (LED) located immediately below the board extractor. The LED is software programmable through bit 7 of the Digital I/O ASIC's System Register 3 (E5h) (refer to Chapter 11, "System Registers"). Writing a logical 0 to the LED bit turns the LED off and writing a logical 1 to the LED bit turns the LED on. The LED is turned off after a power cycle or a reset.

The following code shows how to turn the LED on and off.

```
;-------------------------------------
; The multiple master interrupt is
; a bi-directional bit.  The current
; software state of multiple master
; interrupt is maintained in the
; multiple master state bit. Input_e5
; updates the multiple master bit with
; the current software state maintained
; in the multiple master state bit.
;-------------------------------------
input_e5        macro
                local   multiple_on
                in      al,0e5h
                test    al,8
                jnz      multiple_on
                and      al,not 10h
multiple_on:
                endm
;-------------------------------------
; led_on turns on the led. Bit 7 controls the
; LED. The state of bit 1 must be maintained
; (write the same value as was read). Bits 3
; and 4 must be handled as shown in the
; input_e5 macro.
;-------------------------------------
led_on:         pushf
                cli
                input_e5
                or      al,80h
```

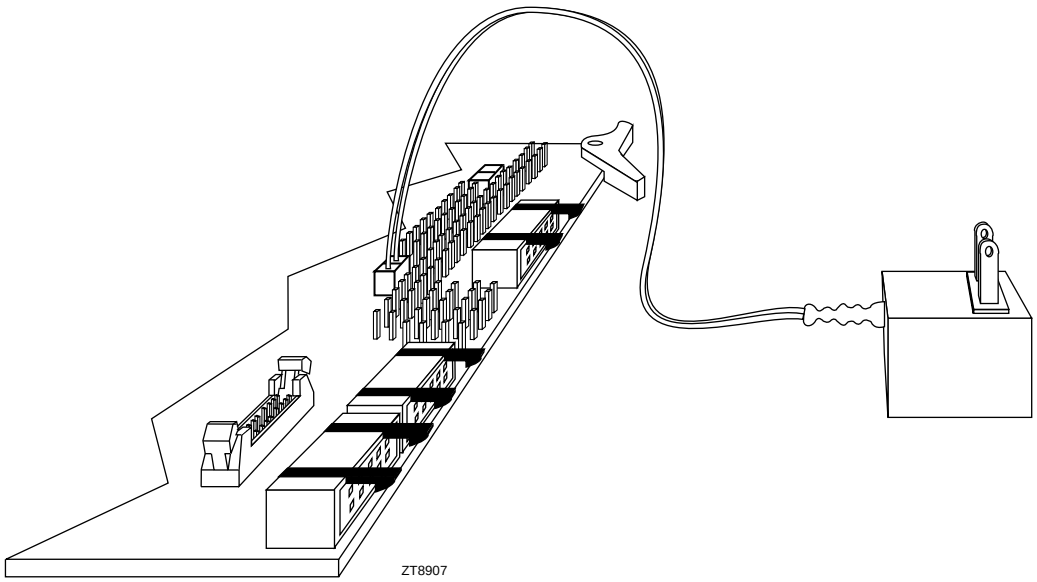
```
                out     0e5h,al
                popf
                ret
;--------------------------------------
; led_off turns off the led. Bit 7 controls the
; LED. The state of bit 1 must be maintained
; (write the same value as was read). Bits 3
; and 4 must be handled as shown in the
; input_e5 macro.
;--------------------------------------
led_off:        pushf
                cli
                input_e5
                and     al,not 80h
                out     0e5h,al
                popf
                ret
```

15. AC POWER-FAIL

The ZT 8907 provides AC power-fail detection to give the application advanced warning of an impending power failure. The advanced warning is used by the application for performing operations such as saving critical data and entering a dormant state.

The ZT 8907 requires a transformer-isolated AC voltage of no more than 30 V from the same source that provides the system power. Ziatech's optional AC wall transformer (ZT 90071) meets these requirements. The wall transformer is connected to connector J10, as shown in the "AC Wall Transformer Installation" figure below.

AC Wall Transformer Installation



Warning: Do not plug the AC adapter into J8 (the speaker output connector). Doing so may damage the board and void the warranty.

In operation, a non-maskable interrupt is generated when AC power falls below 95 VRMS. The non-maskable interrupt must be enabled through jumper W6. The application software must include a non-maskable interrupt service routine to perform the following:

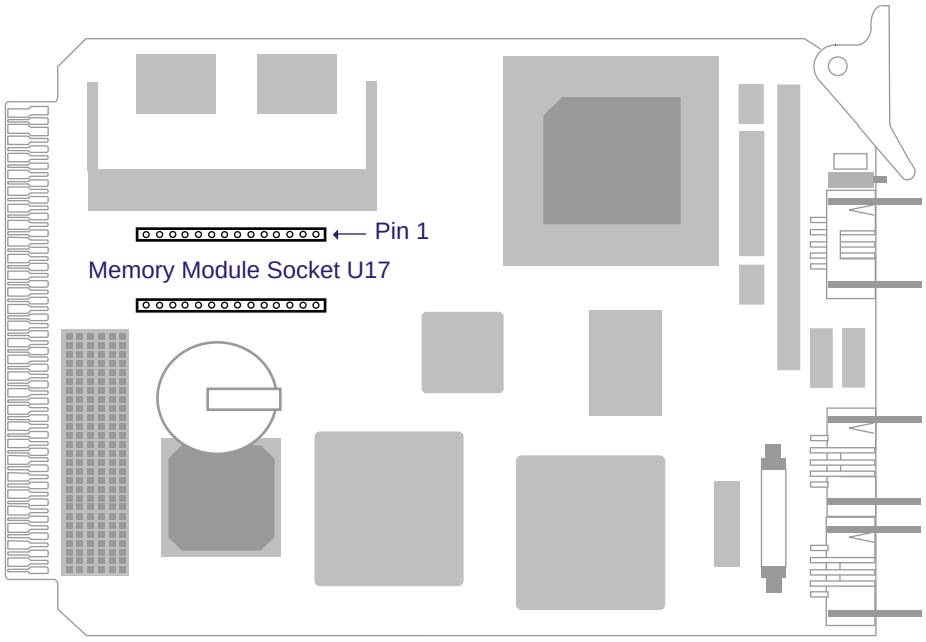
- Determine if the AC power fail is the source of the interrupt request. The three sources of non-maskable interrupts are:
  - AC power fail
  - STD bus NMIRQ*
  - PCI Parity Error
- Preserve any critical information into the optional battery backed static RAM (option T1) or flash memory. These data can then be retrieved at system restart with appropriate user software.
- Place the CPU in a dormant state using a halt instruction or a looping sequence that is not reading or writing critical data to memory or I/O.

16. MEMORY MODULE SOCKET (U17)

The ZT 8907's multi-purpose memory module socket (U17) has three functions, configured through jumpers W2 and W4. The functions are listed below and discussed in the following topics.

- BIOS recovery
- User Static RAM
- STAR SYSTEM Video Emulation SRAM

Memory Module Socket (U17)



BIOS RECOVERY

If the ZT 8907's BIOS becomes corrupted, recover it by installing a PROM programmed with the BIOS into socket (U17). The PROM allows the board to boot and the BIOS to be reflashed. To order the PROM (ZT 95204), contact Ziatech.

The steps below explain how to boot from the boot socket and reflash the BIOS. For more details, see the *Ziatech Industrial Computer System Manual for BIOS Version 4*, or refer to the Technical Briefs maintained on Ziatech's FTP site located at ftp://ziatech.com/Tech_support.

1. Install jumpers W2A and W4B

2. Insert the PROM into the boot socket. Make sure the device is correctly oriented.

3. Power on the system with the CPU reinstalled. The CPU will boot either to a Mini Command colon prompt (:) or a P: prompt if the P: drive contents are still intact.

4. To reflash the BIOS, insert the STD 32 Development Software diskette (ZT 97137) into the floppy drive and type either

   ```
   A:\UTIL\FLASH /B A:\IMAGES\SYS8907.B00
   ```

   or

   ```
   A:\UTIL\FLASH /B A:\IMAGES\SYS8907M.B00
   ```

   depending on whether you are recovering a STAR BIOS image or a standard BIOS image. An `M` at the end of the filename indicates STAR BIOS; no `M` indicates standard BIOS. Type the **"Y"** key to respond to the warning messages and the BIOS will be reflashed.

5. After reflashing the BIOS, turn off the power, remove the PROM, remove jumper W2A, and return jumper W4 to the "A" position.

USER STATIC RAM

Installing a 128 Kbyte SRAM module into socket U17 provides four 32 Kbyte pages of SRAM memory for use by user programs. Perform the steps below.

1. Install a 128 Kbyte SRAM module into socket U17.

2. Install jumper W2B. This maps the 32 Kbyte pages into the BIOS Extension region (D8000h -- DFFFFh) when the system re-boots.

3. Install jumper W4A to battery-back the SRAM (to preserve battery life).

4. Boot the system and access the BIOS SETUP utility by pressing the **"S"** key during the system RAM check, or by running the SETUP.COM utility from the MS-DOS prompt.

5. In screen 2 of the BIOS SETUP utility, set the parameter "Memory Range D8000 – DFFFFh" to "PCI" in order to access the onboard SRAM.

6. User programs switch between pages by writing to the Digital I/O ASIC's System Register 2 (E4h). Bits 3 and 4 select which 32 Kbyte page of the SRAM is mapped into memory range D8000 – DFFFFh. Chapter 11 illustrates the System Registers.

STAR SYSTEM VIDEO EMULATION SRAM

When the ZT 8907 is used in a STAR SYSTEM and sharing a video card with other CPUs, a 128 Kbyte SRAM module must be installed in socket U17. Perform the steps below.

1. Install a 128 Kbyte SRAM module into socket U17.

2. Remove all jumpers from W2 to enable the video RAM region when the system re-boots.

3. To conserve battery life, always battery-back this SRAM by making sure jumper W4A is installed; installing W4B may increase battery drain when SRAM is installed.

17. OPTIONAL IDE INTERFACE

The ZT 8907 supports a local Intelligent Drive Electronics (IDE) hard disk interface (J15) attached to the solder side of the board. This feature is useful for single board applications as well as for STAR SYSTEMs where the ZT 8907 needs to have a local (non-shared) hard disk.

Because the hard disk drive market continually improves capacity, the specific size of the drive (in megabytes) sold with this option may change. In general, Ziatech offers a higher capacity drive for the same or similar price when a new drive is qualified.

The onboard IDE interface is a factory load option at Ziatech. Option D1 to the ZT 8907 includes a hard disk, cable, and connector. When configured for local IDE operation, the ZT 8907 requires one additional slot in the STD 32 card cage.

HARD DISK MOUNTING

The IDE hard disk is mounted to the solder-side of ZT 8907 on short standoffs. A cable (ZT 90201) interfaces to connector J15 on the ZT 8907 to provide power and IDE signals to the drive. The integrated drive is a 2.5 inch family drive, using a 2 mm connector interface. Local 3.5 inch IDE drives are not supported by the ZT 8907.

SELECTING IDE OPERATION TYPE

Enable the ZT 8907 for either onboard IDE or STD 32 IDE operation through the BIOS SETUP utility. Access the SETUP utility by pressing the "**S**" key while the system is booting.

STD 32 IDE Operation (default)

In screen 1, set the **IDE Interface** parameter to **STD32**.

In screen 2, set the **Interrupt Request 14** parameter to **INTRQ3**. †

Onboard IDE Operation

In screen 1, set the **IDE Interface** parameter to **ONBOARD**.

In screen 2, set the **Interrupt Request 14** parameter to **IDE**.

The ZT 8907 provides a red hard disk activity light for local IDE accesses.

STAR SYSTEM APPLICATIONS

Certain STAR SYSTEM applications require a CPU board to have exclusive access to an IDE drive, such as when a CPU is booting a unique operating system, or when, for performance reasons, a CPU requires isolated (non-shareable) hard disk capability. All of these needs are met by using an onboard IDE interface, although actual hard drive performance is no better than that provided by peripheral hard drive controller boards like the ZT 8952 or ZT 8953.

Overall system performance, however, is superior when using an onboard IDE interface because without local IDE accesses impacting the STD 32 bus, other processors experience lower latency times to system-wide resources. Additionally, the local processor does not have to arbitrate for the STD 32 bus in order to perform local IDE transfers.

SINGLE BOARD APPLICATIONS

When the ZT 8907 is used in single board applications with a local IDE hard disk, Ziatech suggests that the application provide power to the ZT 8907 via a mating STD 32 connector. For mounting support, both the STD 32 connector and standoffs (to PCB mounting holes located on the ZT 8907) should be used to physically support the assembly. This will vary depending on the application. Contact Ziatech for assistance.

18. OPTIONAL LOCAL FLOPPY DISK INTERFACE

The ZT 8907 can be factory configured to use a local (non-STD) floppy disk drive. This is a special order option and is intended for higher volume applications where a remotely mounted floppy drive is required. Optional connector J14 on the solder side of the board is loaded for access to the floppy signals. A special BIOS is also required.

Installing the local floppy option requires one additional STD 32 slot. No mounting for this floppy drive is provided. Contact Ziatech for details.

A. BOARD CONFIGURATION

The ZT 8907 includes several options that tailor the operation of the board to requirements of specific applications. Most of the options are selected through the BIOS SETUP utility. Some options cannot be software controlled and are configured with jumpers or cuttable traces. Jumper options are made by installing and removing shorting receptacles. Cuttable trace options are made by installing and removing surface mount 0 Ω resistors.

This appendix is organized according to the three types of configuration options: BIOS SETUP, jumpers, and cuttable traces. It also provides illustrations showing the locations of the ZT 8907's jumpers and cuttable traces.

BIOS SETUP OVERVIEW

The ZT 8907 has many features that can be configured with the BIOS SETUP utility. The SETUP utility is executed during the boot sequence when the **"S"** key is typed. In DOS systems, SETUP may be executed by running the SETUP.COM program from the command line.

BIOS SETUP Screens

The BIOS SETUP utility for the ZT 8907 is organized as two screens, listed below.†

- Screen 1: **Generic option list.** Options shared among all Ziatech CPUs are listed on this screen. Base memory and extended memory size selection, boot source, hard disk type, and floppy disk type are configurable through this screen.

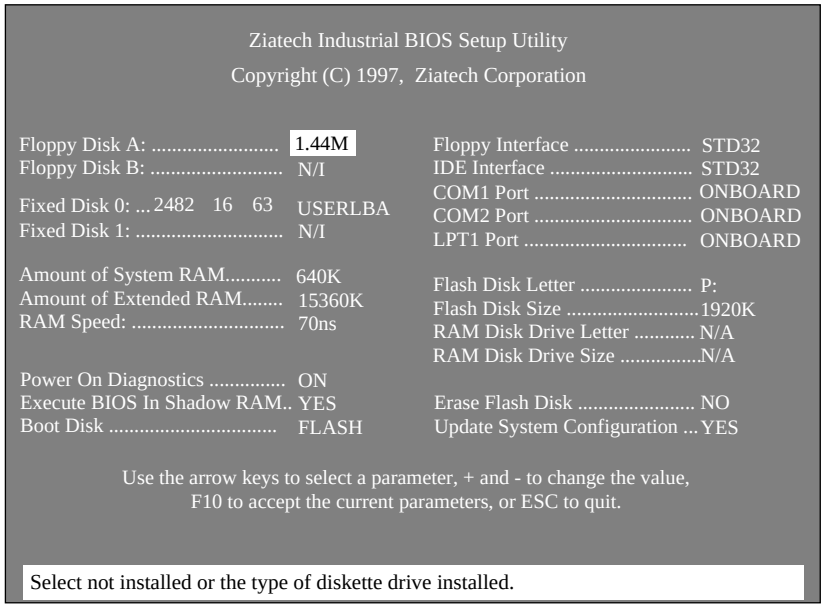
- Screen 2: **ZT 8907-specific SETUP options.** Options such as interrupt routing and STD 32 memory and I/O addressing are configurable through this screen. See the following topic, "ZT 8907-Specific SETUP Options," for more information.

The parameters in the SETUP screens are easily changed. Use the arrow keys to select a parameter, then press + or - to step through the valid choices for that parameter. A dynamic help line at the bottom of the screens helps you determine how to set each parameter. SETUP accepts only valid parameter sets: if changing one parameter invalidates another parameter, SETUP automatically updates the invalid parameter. After setting the parameters, press the F10 key to accept them. Press the **Page Down** and **Page Up** keys to switch between SETUP screens.

† Factory default configuration

BIOS SETUP Utility: Screen 1

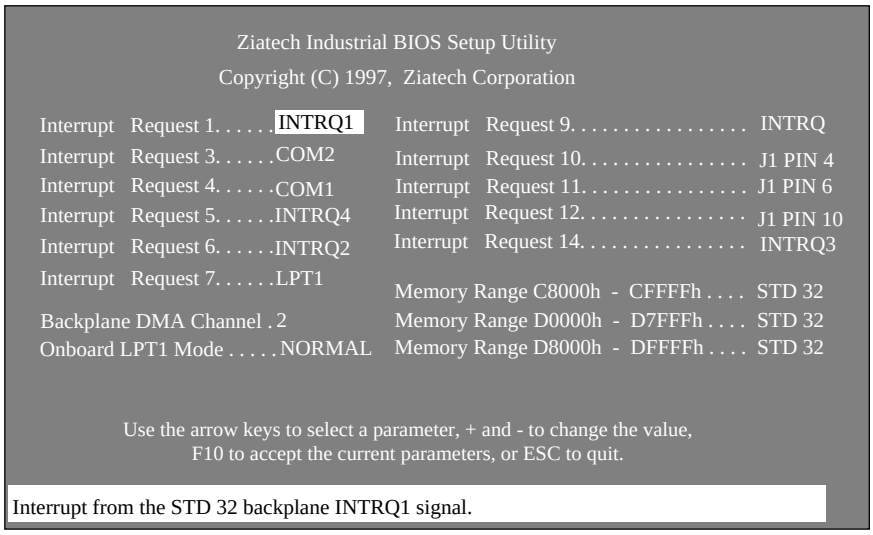
Generic SETUP Options



ZT8907

BIOS SETUP Utility: Screen 2

ZT 8907-Specific SETUP Options



ZT8907

ZT 8907-Specific SETUP Options

ZT 8907-specific SETUP options, such as interrupt routing and STD 32 memory addressing, are configurable through screen 2 of the SETUP utility and are discussed below.

- Interrupt routing

  The source for individual interrupt controller inputs is selectable through screen 2 of the SETUP utility. The STD 32 backplane interrupts, frontplane interrupts, and PCI interrupts are options.

- Backplane DMA (via BUSRQ*/BUSAK*) channel selection

  Normally, the BUSRQ*/BUSAK* signals are used to allow DMA to a backplane based floppy disk controller (for example, ZT 8954), but other devices may use this mechanism in the absence of a floppy disk controller. Though the SETUP utility allows either channel 2 (for floppy disks) or channel 5 (for 16-bit operations) to be selected as the backplane DMA channel, the ZT 8907D does not support DMA channel 5 on the backplane. Always set the backplane DMA parameter to channel 2 for proper operation.

- STD 32 memory address decoding

  Locations in the lower 1 Mbyte and in extended memory can be dedicated to the STD 32 bus. Regions that are configured for STD 32 cannot be used for PCI peripherals. The following regions are selectable:

  † 000C8000h - 000CFFFFh (This region must be set to STD 32 for STAR SYSTEM operation.)

  † 000D0000h - 000D7FFFh (This region must be set to PCI for access to the battery backed static RAM.)

  † 000D8000h - 000DFFFFh

JUMPER OPTIONS AND LOCATIONS

The ZT 8907 includes nine jumpers, W1-W9. The default configuration of these jumpers is shown in the "Factory Default Jumper Configuration" figure on the following page. The "Customer Jumper Configuration" figure on the following page provides a blank jumper layout; use this figure to document your jumper configuration if it differs from the factory default.

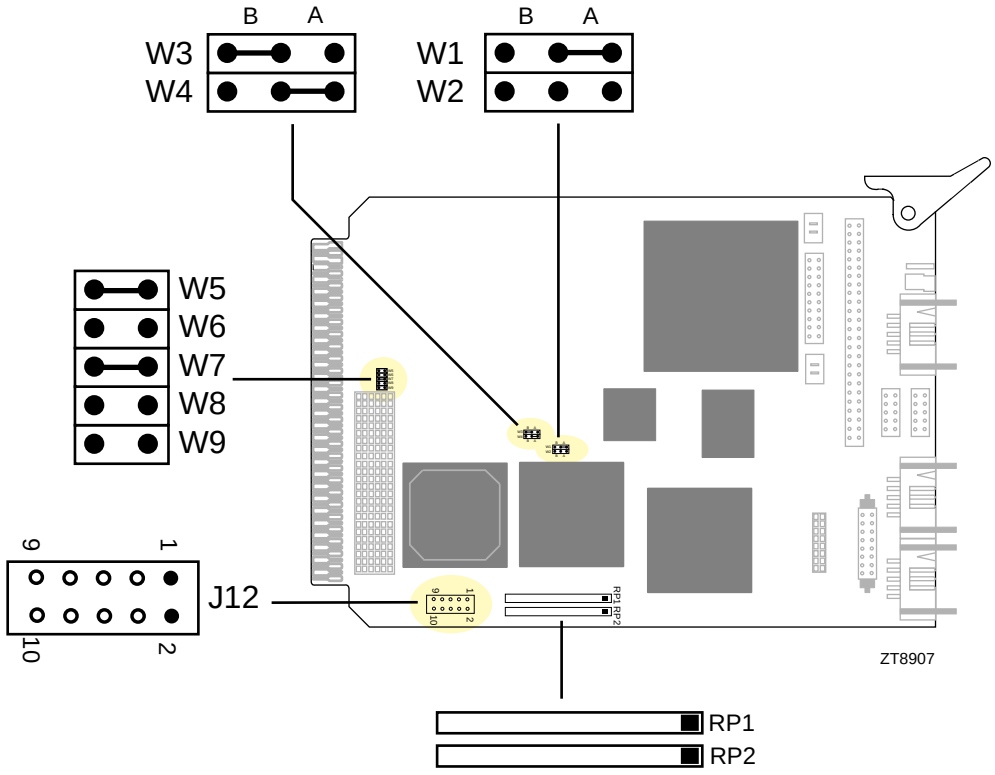
† Factory default configuration

The "Jumper Cross Reference" table below divides the jumper options into functional groups.

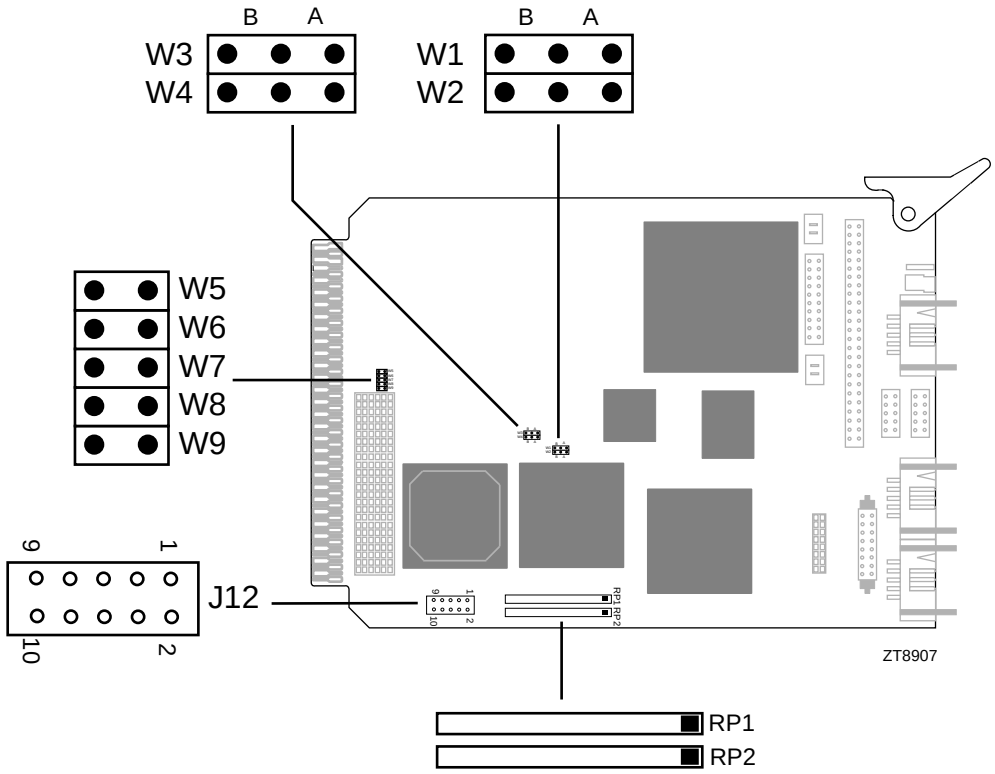
Jumper Cross Reference

Function	Jumpers
AC Power-Fail NMIRQ* Enable	W6
CMOS RAM Erase	W3
Flash Write Protect	W9
Local Keyboard Disable	W5
Multiple Master Interrupt	W1
Port 80 Test Mode	J12
PROM/SRAM Selection	W2
SRAM Battery Backup	W4
STD Bus Access Disable	W8
STD Bus NMIRQ* Enable	W7

Factory Default Jumper Configuration



Customer Jumper Configuration



JUMPER DESCRIPTIONS

The ZT 8907 includes jumpers with two posts and jumpers with three posts. Jumpers having only two posts are labeled W**x,** where **x** defines the jumper number (for example, W5). Jumpers having three posts are labeled W**x** "A" and "B" (for example, W1A and W1B). These jumpers have two possible selections, where "A" is one selection and "B" is another.

This section also documents J12, which serves as both the In-System Programming connector (see Appendix B, "Specifications") and the Port 80 Decode jumper below.

The following topics list the jumpers in numerical order and provide a detailed description of each jumper. A dagger (†) indicates the default jumper configuration.

W1 (Multiple Master Interrupt)

Configuring W1 selects the signal path for the **multiple master** interrupt (required for operation in an STD 32 STAR SYSTEM). By default (W1A = In) the ZT 8907 uses INTRQ4* for the multiple master interrupt and makes INTRQ* available for application use.

However, some STD 32 systems define INTRQ4* for VBAT (battery backup) on the STD bus. When that is the case, select INTRQ* for the multiple master interrupt (W1B = In) and remove cuttable trace CT48.

	W1A	W1B	CT48	Function
†	In	Out	In	INTRQ4* is multiple master interrupt
	Out	In	Out	INTRQ* is multiple master interrupt

W2 (PROM/SRAM Selection)

W2 defines the three functions of socket U17. Proper configuration of W4 is also required. See the "W4 (SRAM Battery Backup)" table on the following page.

1. BIOS Recovery: If the ZT 8907's BIOS becomes corrupted, recover it by installing jumper W2A and installing a PROM programmed with the BIOS into socket (U17). See the "BIOS Recovery" topic in Chapter 16 for step-by-step instructions.

2. User Static RAM: Installing jumper W2B and installing a 128 Kbyte SRAM module into socket U17 provides four 32 Kbyte pages of SRAM memory for use by user programs. SRAM is selectable through bits 3 and 4 of System Register 2 (E4h). In screen 2 of the BIOS SETUP utility, set the parameter "Memory Range D8000 – DFFFFh" to "PCI" in order to access the on-board SRAM. To conserve battery life, always battery back this SRAM by making sure jumper W4A is installed. See the "User Static RAM" topic in Chapter 16 for step-by-step instructions.

3. STAR SYSTEM Video Emulation SRAM: When the ZT 8907 is used in a STAR SYSTEM and is sharing a video card with other CPUs, remove all jumpers from W2 and install a 128 Kbyte SRAM module in socket U17. To conserve battery life, always battery back this SRAM by making sure jumper W4A is installed. See the "STAR SYSTEM Video Emulation SRAM" topic in Chapter 16 for step-by-step instructions.

	Function	Installed in U17	W2A	W2B	State of W4
	BIOS Recovery	PROM (ZT 95204)	In	Out	Position B jumpered
†	User Static RAM	128 Kbyte SRAM	Out	In	Position A jumpered
†	STAR SYSTEM Video Emulation SRAM	128 Kbyte SRAM	Out	Out	Position A jumpered

Note: In no case should W4 be totally unjumpered.

† Factory default configuration

W3 (CMOS RAM Erase)

W3 clears the contents of the battery backed CMOS configuration RAM. The CMOS RAM is erased by removing the card from the backplane or other power source and moving the W3B jumper to position W3A and back to W3B again.

	W3A	W3B	Function
	In	Out	Erase CMOS
†	Out	In	Normal

W4 (SRAM Battery Backup)

Installing W4A battery backs the SRAM installed in socket U17. Always install W4A if SRAM is installed in U17. Installing W4B may increase battery drain when SRAM is installed.

Note: In no case should W4 be totally unjumpered.

	W4A	W4B	Function
†	In	Out	SRAM is battery backed
	Out	In	SRAM is not battery backed. Use this configuration only when no SRAM is installed in socket U17.

W5 (Local Keyboard Disable)

If W5 is not installed, the ZT 8907's on-board keyboard controller is enabled (and available through connector J7). Installing W5 (default configuration) disables the local keyboard controller on the ZT 8907. W5 must be installed when using a keyboard controller located on the backplane.

	W5	Function
†	In	STD keyboard enabled
	Out	Local keyboard enabled

† Factory default configuration

W6, W7 (Non-Maskable Interrupts)

W6 and W7 arm the AC power-fail (Chapter 15) and STD bus interrupts (Chapters 3 and 4) to generate non-maskable interrupt requests. These interrupts combine with the PCI bus parity error interrupt before being routed to the CPU.

Bit 3 of the port 61h register enables and disables the combined interrupt source to the CPU. Bit 2 of the port 61h register indicates whether a non-maskable interrupt was generated by a parity error. (See the "Non-Maskable Interrupt Structure" figure in Chapter 3, "STD Bus Interface").

System Register 2 (E4h), bits 0 and 1, on the Digital I/O ASIC device indicate whether a non-maskable interrupt was generated by the STD bus or an AC power failure.

The AC input signals for the optional power-fail detection feature are available through connector J10. See Chapter 11, "System Registers," for more information about the Digital I/O ASIC device.

	W6	**AC Power Fail NMIRQ***
	In	Enabled
†	Out	Disabled
	W7	**STD Bus NMIRQ***
†	In	Enabled
	Out	Disabled

W8 (STD Bus Access Disable)

Installing W8 prevents all operations from reaching the STD bus, allowing a ZT 8907 with a standard BIOS to be installed in a system as a stand-alone processor (see note below). Configuration of this jumper sets bit 7 of the Digital I/O ASIC's System Register 2 (E4h).

	W8	**Function**
	In	STD access inhibited
†	Out	Normal STD access

Note: To use the ZT 8907 as a stand-alone processor, resistor packs RP1 and RP2 must be properly configured.

† Factory default configuration

W9 (Flash Write Protect)

Installing W9 write protects the contents of the flash memory; removing W9 makes the flash writable.

	W9	Function
	In	Flash is write protected
†	Out	Flash is writable

J12 (Port 80 Decode)

Installing a jumper across pins 1 and 2 on J12 enables the Port 80 diagnostic codes. These codes are sent to connector J5 and are for debugging purposes only.

J12 also serves as the In-System Programming Connector.

	J12 Pins 1 and 2	Function
	Jumpered	Port 80 codes sent to PIO7-PIOO (J5, pins 33-48)
†	Not jumpered	Normal operation

RP1, RP2 (Permanent Master Pullups)

Resistor packs RP1 and RP2 serve two related purposes, detailed below.

1. **Permanent Master Configuration**. When RP1 and RP2 are installed, the ZT 8907 is configured as a Permanent Master and pulls up the STD 32 bus signals. In a STAR SYSTEM, only one CPU (the Permanent Master) is allowed to pull up the STD 32 bus signals.

2. **CLOCK* and SYSRESET***. When RP1 and RP2 are installed, the ZT 8907 drives the CLOCK* and SYSRESET* signals; removing RP1 and RP2 inhibits the CPU from driving the CLOCK* and SYSRESET* signals. Only the Permanent Master is allowed to drive these signals.

† Factory default configuration

RP1 and RP2	ZT 8907 Configuration	STD 32 Bus Signals
Installed	Permanent Master in a STAR SYSTEM or Single Master in a non-STAR SYSTEM	Pulled up; CLOCK* and SYSRESET* driven by this CPU
Installed	ZT 8907 is operating as a stand-alone processor not installed in a backplane	------
Removed	Temporary Master in a STAR SYSTEM or stand-alone processor in a backplane with other CPUs	Not pulled up; CLOCK* and SYSRESET* not driven by this CPU

Note: To use the ZT 8907 as a stand-alone processor, jumper W8 must be installed.

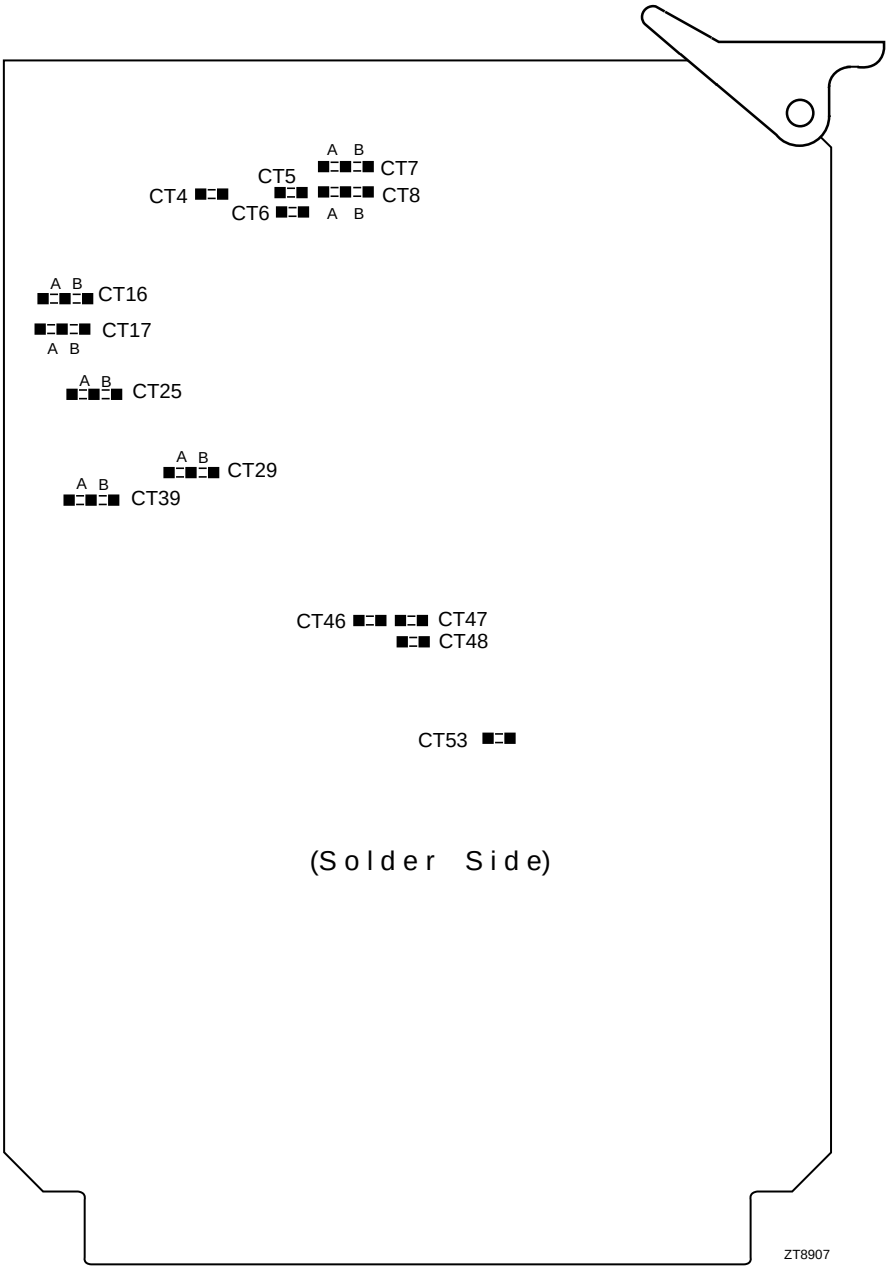
CUTTABLE TRACE OPTIONS AND LOCATIONS

The ZT 8907 contains several cuttable traces (zero ohm shorting resistors) for configuring less frequently selected board options. The "Cuttable Trace Locations" figure below shows the placement of the ZT 8907 cuttable traces. The "Cuttable Trace Definitions" table provides a quick cross-reference for the ZT 8907 cuttable trace descriptions that follow.

There are two types of cuttable traces on the ZT 8907: single-option and double-option. **Single option** cuttable traces (labeled CT**x--**for example, CT2) have two surface mount pads. A zero ohm shorting resistor is then soldered between these pads to make the connection. **Double option** cuttable traces (labeled CT**x** "A" and "B"--for example, CT1A and CT1B) are implemented using three surface mount pads. The zero ohm shorting resistor is then soldered between one set of pads, depending on the chosen option.

Note: Cuttable trace modifications should only be performed by a qualified technician familiar with surface mount soldering techniques. The product warranty is voided if the board is damaged by customer modifications. If a qualified technician is not available to you, contact Ziatech Technical Support. For large production orders, Ziatech can also set up specials that are pre-configured at the factory. Contact Ziatech for more information.

Cuttable Trace Locations



Cuttable Trace Definitions

CT#	Default	Description
CT4	In	Counter Timer 2 Clock Source
CT5	In	Counter Timer 1 Clock Source
CT6	In	Counter Timer 0 Clock Source
CT7	A	IRQ15 Selection
CT8	A	IRQ15 Selection
CT16	A	DMA Channel 3/7 DAK Selection
CT17	A	DMA Channel 3/7 DAK Selection
CT25	B	DMA Channel 3 DRQ Selection
CT29	B	DMA Channel 1/6 DAK Selection
CT39	B	DMA Channel 0/5 DAK Selection
CT46	Out	Board Revision Indicator. Do not modify.
CT47	In	Board Revision Indicator. Do not modify.
CT48	In	INTRQ4* STD Connection
CT53	In	STD Reset Configuration

CT4-CT6 (Counter/Timer Clock Sources)

When these cuttable traces are installed (default), channel clocks 0-2 of the auxiliary counter/timer are driven with the on-board 8 MHz clock. When these cuttable traces are removed, the clock source must be driven from pins on connector J2. See the table below for more details. See Chapter 5, "Counter/Timers" for more information about the auxiliary counter/timer device.

CT #		State	Function
CT4	†	In	Clock channel 2 driven with on-board 8 MHz clock
		Out	Clock source driven from J2, pin 8
CT5	†	In	Clock channel 1 driven with on-board 8 MHz clock
		Out	Clock source driven from J2, pin 4
CT6	†	In	Clock channel 0 driven with on-board 8 MHz clock
		Out	Clock source driven from J2, pin 1

CT7, CT8 (IRQ15 Input Source Selection)

Configuration of these cuttable traces routes the sources described below to the interrupt controller IRQ15 input.

Auxiliary counter/timer: When CT7A and CT8A are installed (default), the output of auxiliary counter/timer channel 2 is routed to IRQ15. When the counter output on counter/timer channel 2 is active, an interrupt will be sent to the interrupt controller input IRQ15.

Digital I/O Event Sense: When CT7B and CT8A are installed and the Digital I/O ASIC chip is programmed to interrupt on an external event, an interrupt is sent to the interrupt controller input IRQ15. See the "Event Sense Detection Logic" topic in Chapter 10 for more information about the 16C50A Digital I/O ASIC's event sense feature.

Connector J1 pin 8: When CT8B is installed, frontplane interrupt J1 pin 8 (FP6) is routed to the interrupt controller input IRQ15. A typical use for this is connection of a secondary IDE controller (ZT 8944).

	CT7	CT8	Source Routed to Interrupt Controller IRQ15 Input
†	A	A	Auxiliary counter/timer channel 2
	B	A	16C50A Digital I/O ASIC Event Sense interrupt
	---	B	Connector J1, pin 8

† Factory default configuration

CT16, CT17, CT25, CT29, CT39 (Frontplane DMA Channel Selection)

The ZT 8907 supports either 8-bit or 16-bit frontplane DMA, available on connector J6. Up to three frontplane DMA channels are available simultaneously. These cuttable traces configure the three chosen frontplane DMA channels to be either 8-bit or 16-bit. Be sure to mask unused channels not required by the application. Refer to Chapter 6, "DMA Controller," for more information.

Default Frontplane DMA Settings

	Channel Selection	Cuttable Trace	Data Size	Available on J6...
†	DMA channel 0	CT39B	8-bit	pins 1 (DRQ) and 3 (DAK)
†	DMA channel 1	CT29B	8-bit	pins 2 (DRQ) and 4 (DAK)
†	DMA channel 7	CT16A, CT17A, CT25B	16-bit	pins 5 (DRQ) and 7 (DAK)

Alternate Frontplane DMA Settings

	Channel Selection	Cuttable Trace	Data Size	Available on J6...
	DMA channel 5	CT39A	16-bit	pins 1 (DRQ) and 3 (DAK)
	DMA channel 6	CT29A	16-bit	pins 2 (DRQ) and 4 (DAK)
‡	DMA channel 3	CT16B, CT17B, CT25A	8-bit	pins 5 (DRQ) and 7 (DAK)

CT46, CT47 (Board Revision)

These cuttable traces are set at the factory depending on the current board revision and should not be modified by the user.

CT48 (INTRQ4* STD Connection)

Configuring CT48 selects the function of pin P5 on the STD 32 connector. By default (CT48 = In), the ZT 8907 uses pin P5 for signal INTRQ4*.

---

† Factory default configuration

‡ By default, DMA channel 3 is assigned to the on-board parallel printer port. Route DMA channel 3 to connector J6 by configuring CT16, CT17, and CT25 as shown above.

However, some STD 32 systems define P5 for VBAT (battery backup). If the ZT 8907 is used in a system that requires P5 to be configured as VBAT, then CT48 should be removed.

CT #		State	Function
CT48	†	In	STD 32 connector pin P5 for INTRQ4*
		Out	STD 32 connector pin P5 for VBAT

Note: Do not remove CT48 if resistors RP1 and RP2 are also removed, as when the ZT 8907 is configured as a STAR SYSTEM temporary master. If you need to operate the ZT 8907 in this configuration (VBAT operation with RP1 and RP2 removed), contact Ziatech for assistance.

CT53 (STD Reset Configuration)

By default, the ZT 8907 uses pin P47 on the STD 32 connector for the SYSRESET signal. SYSRESET is generated by the permanent master in a STAR SYSTEM. To keep the ZT 8907 from resetting when this signal is present on the backplane, disconnect the SYSRESET signal by removing CT53.

CT #		State	Function
CT53	†	In	Enable SYSRESET detection (permanent master)
		Out	Disable SYSRESET detection

† Factory default configuration

B. SPECIFICATIONS

This appendix describes the electrical, environmental, and mechanical specifications of the ZT 8907. It also includes illustrations of the board dimensions, the P/E connector pinouts, the connector locations, and various cables, as well as tables showing the pin assignments for the ZT 8907's 15 connectors.

ELECTRICAL AND ENVIRONMENTAL

The section covers the following electrical and environmental specifications.

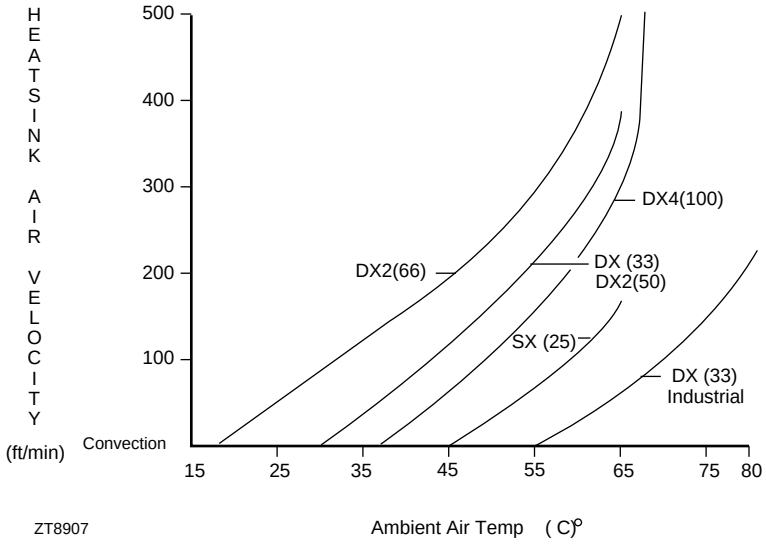
- Absolute maximum ratings
- DC operating characteristics
- Battery backup characteristics
- STD bus loading characteristics

Absolute Maximum Ratings

Supply Voltage, Vcc:	0 to 7 V
Storage Temperature:	-55° to +100° Celsius
Operating Temperature:	0º to +70º Celsius
Relative Humidity:	<95% at 40º Celsius, non-condensing

Ziatech recommends vertical mounting and the use of a fan to meet the airflow requirements shown in the "Airflow Requirements" figure below.

Airflow Requirements



DC Operating Characteristics

Numbers assume 4 Mbytes of DRAM and 2 Mbyte of flash.

Supply Voltage, Vcc:	4.75 to 5.25 V
Supply Voltage, AUX +V:	+12 V Nominal †
Supply Voltage, AUX -V:	-12 V Nominal †
Supply Current, Icc:	
486SX-25:	0.9 A typ., 1.5 A max.
486SX-33:	1.1 A typ., 1.8 A max.
486DX4-100:	1.4 A typ., 2.3 A max.

† ±12 V not required for ZT 8907 operation. However, some PCI mezzanine cards may require these voltages. Refer to the documentation provided with the particular PCI mezzanine card installed on your ZT 8907 for more information.

Battery Backup Characteristics

Battery Voltage:	3 V
Battery Capacity:	255 mAH
Real-time Clock Requirements:	2 µA (typical); 5 µA (maximum) †
Optional 128 Kbyte SRAM req.:	2 µA (typical); 10 µA (maximum) †
Real-time Clock Data Retention (without optional SRAM module in U17):	5 years (minimum); 8 years (typical)
Real-time Clock Data Retention (with optional SRAM module in U17):	2 years (minimum); 5 years (typical)
Electrochemical Construction:	Long life lithium with solid-state polycarbon monofluoride cathode

STD-80 Compatibility

The ZT 8907 is designed for use in an STD 32 backplane environment. While designed to be backward compatible with STD-80 systems, the ZT 8907 is not guaranteed to work in all system topologies.

STD Bus Loading Characteristics

The unit load is a convenient method for specifying the input and output drive capability of STD bus cards. With this method, one unit load is equal to one LSTTL load as follows:

- Current for single input load: 20 µA
- Current for single output drive: -400 µA

The unit load reflects current requirements at worst case conditions over the recommended supply voltage and operating temperature ranges. An output drive of 60 unit loads drives 60 STD bus cards having input ratings of one unit load. The figure "STD Bus Loading, P Connector" includes load values for STD-80 connections. The "STD Bus Loading, E Connector" figure includes load values for STD 32 connections.

† When Vcc is below acceptable operating limits.

STD Bus Loading, P Connector

PIN (CIRCUIT SIDE) / OUTPUT DRIVE / INPUT LOAD / MNEMONIC							PIN (COMPONENT SIDE) / OUTPUT DRIVE / INPUT LOAD / MNEMONIC
+5 VDC	REQ		P2	P1		REQ	+5 VDC
GND	REQ		P4	P3		REQ	GND
DCPDN*		40	P6	P5	24	1	INTRQ4* (VBAT)
D7/A13 [1]	1	24	P8	P7	24	1	D3/A19 [1]
D6/A22 [1]	1	24	P10	P9	24	1	D2/A18 [1]
D5/A21 [1]	1	24	P12	P11	24	1	D1/A17 [1]
D4/A20 [1]	1	24	P14	P13	24	1	D0/A16 [1]
A15	1	24	P16	P15	24	1	A7
A14	1	24	P18	P17	24	1	A6
A13	1	24	P20	P19	24	1	A5
A12	1	24	P22	P21	24	1	A4
A11	1	24	P24	P23	24	1	A3
A10	1	24	P26	P25	24	1	A2
A9	1	24	P28	P27	24	1	A1
A8	1	24	P30	P29	24	1	A0
RD*	1	24	P32	P31	24	1	WR*
MEMRQ*	1	24	P34	P33	24	1	IORQ*
BHE	1	24	P36	P35	24	1	IOEXP
ALE*	1	24	P38	P37		1	INTRQ1*
STATUS 0*	1	24	P40	P39	24	1	STATUS 1*
BUSRQ* [2]	1	24	P42	P41	24	1	BUSAK* [2]
INTRQ*	1	24	P44	P43			INTAK*
NMIRQ*	1		P46	P45		1	WAITRQ*
PBRESET*	1		P48	P47	24	1	SYSRESET* [3]
INTRQ2* (CNTRL*)	1		P50	P49	24	1	CLOCK* [3]
PCI [4]	1		P52	P51			PCO [4]
AUX GND	REQ		P54	P53		REQ	AUX GND
AUX-V			P56	P55		REQ	AUX+V [5]

ZT8907

Notes:

REQ indicates required connection.

[1] High order address bits multiplied over the data bus.

[2] BUSRQ* and BUSAK* are bi-directional

[3] SYSRESET* and CLOCK* are outputs in permanent master configuration and inputs in temporary master configuration.

[4] PCI is connected to PCO.

[5] AUX +V required for flash programming only.

STD Bus Loading, E Connector

PIN (CIRCUIT SIDE) MNEMONIC	OUTPUT DRIVE	INPUT LOAD			OUTPUT DRIVE	INPUT LOAD	PIN (COMPONENT SIDE) MNEMONIC
RSVD			E2	E1			GND
XA23			E4	E3			XA19
XA22			E6	E5			XA18
XA21			E8	E7			XA17
XA20			E10	E9			XA16
RSVD			E12	E11			NOWS*
+5 VDC	REQ		E14	E13		REQ	+5 VDC
DREQx*		24	E16	E15		1	DAKx*
GND	REQ		E18	E17		REQ	GND
D31			E20	E19			D27
D30			E22	E21			D26
D29			E24	E23			D25
D28			E26	E25			D24
GND	REQ		E28	E27			D23
D15	1	24	E30	E29			D22
D14	1	24	E32	E31			D21
D13	1	24	E34	E33			D20
D12	1	24	E36	E35		REQ	GND
D11	1	24	E38	E37			D19
D10	1	24	E40	E39			D18
D9	1	24	E42	E41			D17
D8	1	24	E44	E43			D16
MASTER16*	1	24	E46	E45		REQ	GND
AENx*			E48	E47			IRQx
BE3*			E50	E49			BE1*
BE2*			E52	E51			BE0*
GND	REQ		E54	E53	24	1	MEM16*
W-R			E56	E55			M-IO
DMAIOR*		24	E58	E57	24		DMAIOW*
EX8*			E60	E59		1	IO16*
START*			E62	E61			CMD*
EX32*			E64	E63			EX16*
T-C		24	E66	E65			EXRDY
+5 VDC	REQ		E68	E67		1	INTRQ3*
MREQx*			E70	E69			MAKx*
MSBURST*			E72	E71			SLBURST*
XA31*			E74	E73			XA27*
XA30*			E76	E75			XA26*
XA29*			E78	E77			XA25*
XA28*			E80	E79			XA24*

Note: REQ indicates required connection.

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MECHANICAL

This section covers the following mechanical specifications:

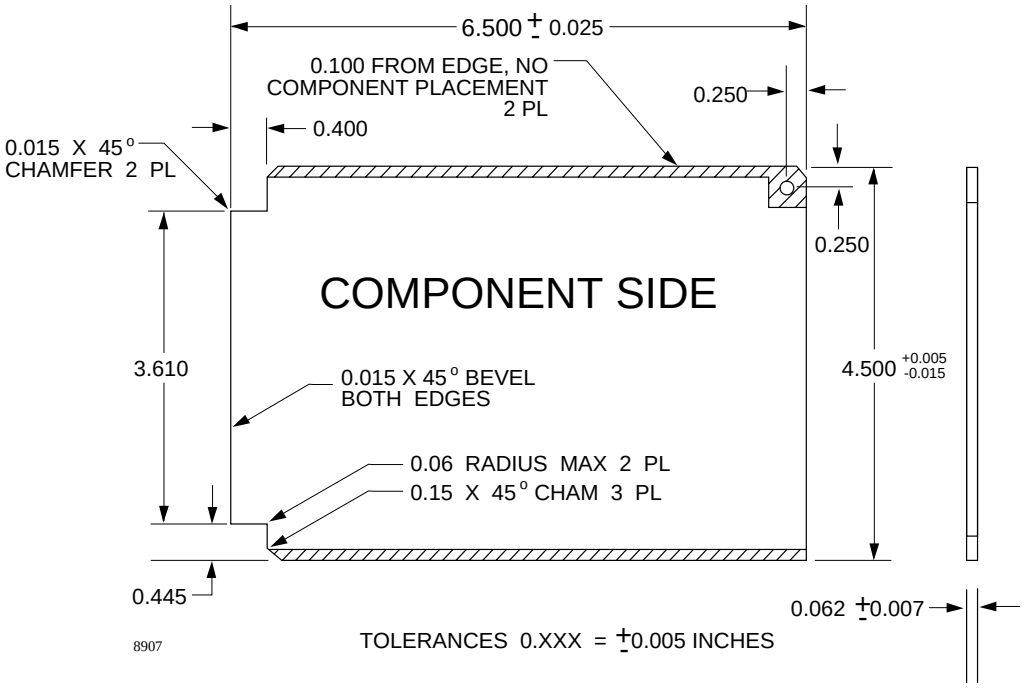
- Card dimensions and weight
- Connectors (including connector locations, descriptions, and pinouts)
- Cables

Board Dimensions and Weight

The ZT 8907 meets the *STD-80 Series Bus Specification* for all mechanical parameters. In a card cage with 0.625 inch spacing, the ZT 8907 requires one card slot with or without the zPM PCI bus video adapter installed. The "Board Dimensions" figure below shows the mechanical dimensions of the ZT 8907.

Length:	16.51±0.063 cm (6.500 ±0.025 inches)
Width:	11.43±0.038 cm (4.500 ±0.015 inches)
Thickness:	0.158 ±0.013 cm (0.062 ±0.005 inches)
Weight:	198 grams (7 ounces)
Height From Top Surface:	1.27 cm (0.5 inches)
Height From Bottom Surface:	0.11 cm (0.043 inches)

Board Dimensions



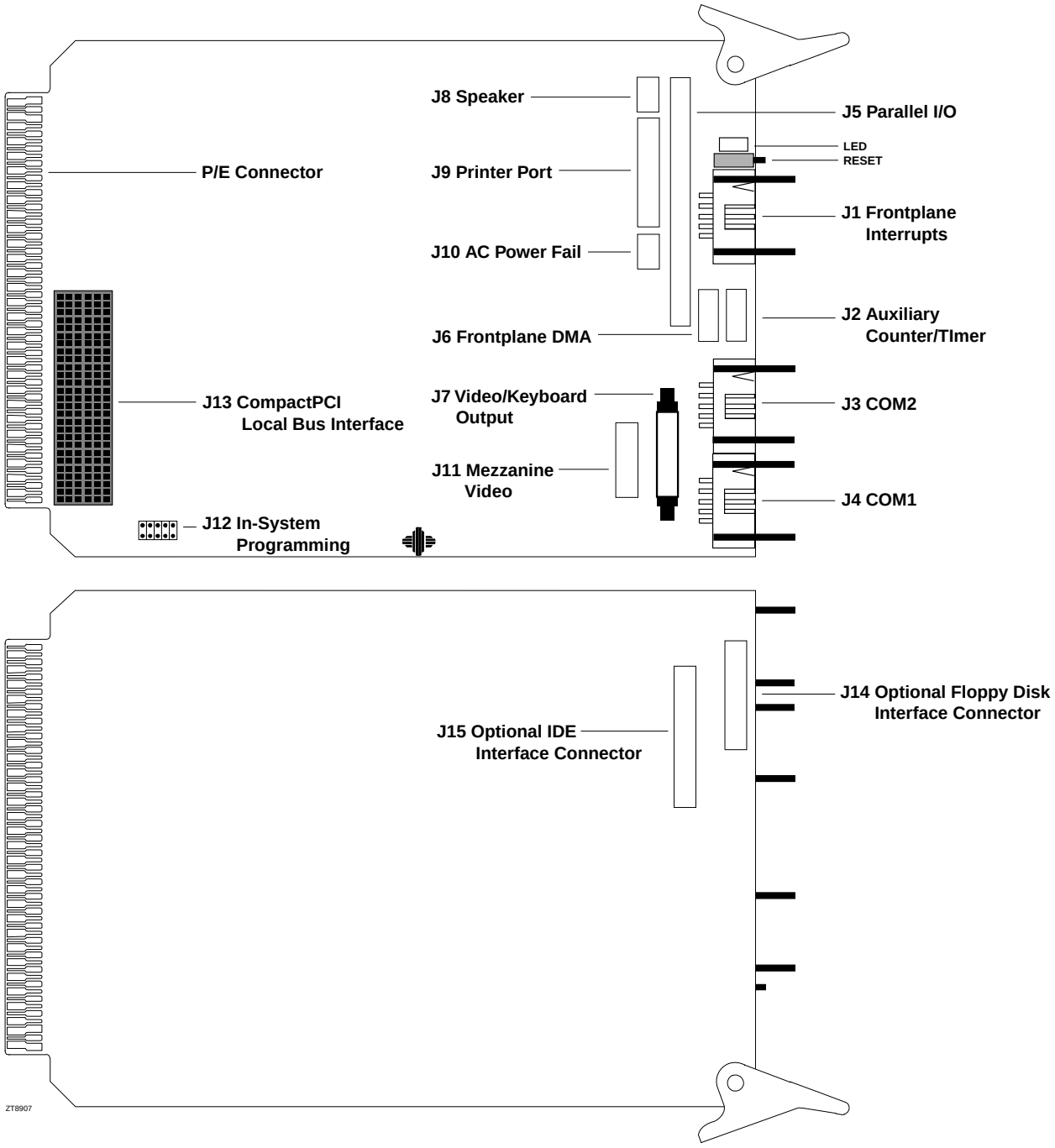
Connectors

As shown in the "Connector Locations" illustration on the following page, the ZT 8907 includes several connectors to interface to the STD bus and application-specific devices. A complete description and pinout for each connector is provided in the following topics. A brief description of each connector is shown in the "Connector Assignments" table below.

Connector Assignments

Connector	Function
J1	Frontplane Interrupt Connector
J2	Auxiliary Counter/Timer Connector
J3	COM2 Connector
J4	COM1 Connector
J5	Parallel I/O Interface Connector
J6	Frontplane DMA Connector
J7	Video/Keyboard Connector
J8	Speaker Connector
J9	Printer Port Interface Connector
J10	AC Power-Fail Connector
J11	Mezzanine Video Interface Connector
J12	In-System-Programming Connector
J13	PCI Local Bus Interface Connector
J14	Floppy Disk Controller Interface Connector
J15	IDE Hard Disk Interface

Connector Locations

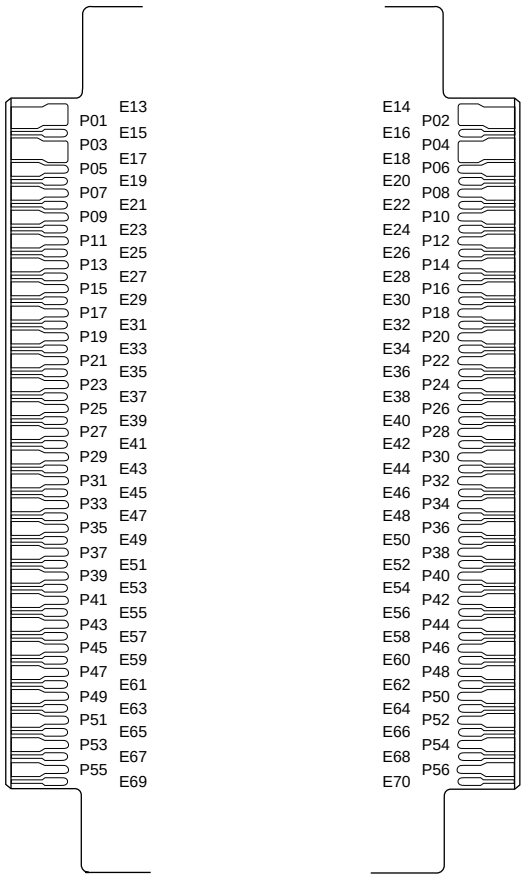


STD 32 P/E Connector

P: The P connector is the interface between the ZT 8907 and the STD-80 bus. This connector is a 56-pin (dual 28-pin) card-edge connector with fingers on 0.125 inch contact spacing. The mating connector is a Viking 3VH28/1CNK5 or equivalent for the solder tail, or a Viking 3VH28/1CND5 or equivalent for a three-level wire wrap. The "P/E Connector Pinout" illustration below shows pin assignments for the P connector, and the "STD Bus Loading, P Connector" figure shows signal assignments.

E: The E connector extends the P connector to interface the ZT 8907 to the STD 32 bus. This connector combines with the P connector to make a 114-pin (dual 57-pin) card-edge connector with fingers on 0.0625 inch contact spacing. The mating connector is a Viking S3VT68/5DP12 or equivalent for the solder tail, or a Viking S3VT68/5DE12 or equivalent for the card extender. The "P/E Connector Pinout" illustration below shows pin assignments for the E connector, and the "STD Bus Loading, E Connector" figure shows signal assignments.

P/E Connector Pinout



Component Side Solder Side

ZT8907

J1 (Frontplane Interrupt Connector)

J1 is a latching 10-pin (dual 5-pin) male transition connector with 0.1 inch contact spacing. The mating connector is a T&B Ansley #622-1030 or equivalent. Frontplane interrupts are available through this connector. The pin assignments are shown in the "J1 Frontplane Interrupt Connector Pinout" table below.

Program the interrupts through screen 2 of the BIOS SETUP utility to be any of the following: 3, 4, 5, 6, 7, 9, 10, 11, 12, or 14. Chapter 4, "Interrupt Controller," summarizes and illustrates the interrupt sources and the interrupt controllers' programmable registers.

J1 Frontplane Interrupt Connector Pinout

Pin #	Signal	Type	Default
1	GND	Ground	------
2	FP1*	In	Not routed
3	GND	Ground	------
4	FP3*	In	IR 10
5	GND	Ground	------
6	FP5*	In	IR 11
7	GND	Ground	------
8	FP6*	In	Not routed
9	GND	Ground	------
10	FP7*	In	IR 12

Notes:

1. The interrupt levels shown are the default configuration.
2. The frontplane interrupts are active low inputs that are routed through an inverter before being applied to the interrupt controller.

J2 (Auxiliary Counter/Timer Connector)

J2 is a 10-pin non-latching (dual 5-pin) male transition connector with 0.1 inch contact spacing. The auxiliary counter/timer input, output, and control signals are available through this connector (depending on the configuration of cuttable traces CT4-CT6).

The pin assignments are shown in the "J2 Auxiliary Counter/Timer Connector Pinout" table below. The mating connector is a T&B Ansley #622-1000 or equivalent. See Chapter 5, "Counter/Timers" for more information about the auxiliary counter/timer device.

J2 Auxiliary Counter/Timer Connector Pinout

Pin #	Signal	Type	Description
1	CLK0	In/Out	Counter/timer 0 clock
2	CTL0	In	Counter/timer 0 control
3	OUT0	Out	Counter/timer 0 output
4	CLK1	In/Out	Counter/timer 1 clock
5	CTL1	In	Counter/timer 1 control
6	GND	-----	Ground
7	OUT1	Out	Counter/timer 1 output
8	CLK2	In/Out	Counter/timer 2 clock
9	CTL2	In	Counter/timer 2 control
10	OUT2	Out	Counter/timer 2 output

Notes:

1. CLK0, CLK1, and CLK2 can be clock inputs or outputs depending on the configuration of cuttable traces CT4, CT5, and CT6:
2. Remove CT4 for external CLK2
3. Remove CT5 for external CLK1
4. Remove CT6 for external CLK0

J3/J4 (COM2/COM1 Connectors)

J3 and J4 are each latching 10-pin (dual 5-pin) male transition connectors with 0.1 inch contact spacing. These connectors include the RS-232 serial interface signals for COM2 and COM1. The pin assignments are shown in the "J3/J4 COM2/COM1 Connectors Pinout" table below. The mating connector is a T&B Ansley #622-1030 or equivalent.

J3/J4 COM2/COM1 Connectors Pinout

Pin #	Signal	Type	Description
1	DCD	In	Data carrier detect
2	DSR	In	Data set ready
3	RXD	In	Receive data
4	RTS	Out	Request to send
5	TXD	Out	Transmit data
6	CTS	In	Clear to send
7	DTR	Out	Data terminal ready
8	RI	In	Ring indicator
9	GND	----	Signal ground
10	VCC	----	+5 V

J5 (Parallel I/O Interface Connector)

J5 is a 50-pin (dual 25-pin) vertical male header with 0.1 inch contact spacing. The Digital I/O ASIC signals are included in this connector. The pin assignments are shown in the "J5 Parallel I/O Interface Connector Pinout" table below. The pin assignments are chosen for direct connection to an I/O module mounting rack, such as those offered by Ziatech (ZT 2226) and Opto 22. The mating connector is a T&B Ansley #622-5030 or equivalent.

J5 Parallel I/O Interface Connector Pinout

Pin #	Signal	Type	Description	Pin #	Signal	Type	Description
1	MOD23	In/Out	Port E2, bit 7	26	GND	-----	Ground
2	GND	-----	Ground	27	MOD10	In/out	Port E1, bit 2
3	MOD22	In/Out	Port E2, bit 6	28	GND	-----	Ground
4	GND	-----	Ground	29	MOD09	In/Out	Port E1, bit 1
5	MOD21	In/Out	Port E2, bit 5	30	GND	-----	Ground
6	GND	-----	Ground	31	MOD08	In/Out	Port E1, bit 0
7	MOD20	In/Out	Port E2, bit 4	32	GND	-----	Ground
8	GND	-----	Ground	33	MOD07	In/Out	Port E0, bit 7
9	MOD19	In/Out	Port E2, bit 3	34	GND	-----	Ground
10	GND	-----	Ground	35	MOD06	In/Out	Port E0, bit 6
11	MOD18	In/Out	Port E2, bit 2	36	GND	-----	Ground
12	GND	-----	Ground	37	MOD05	In/Out	Port E0, bit 5
13	MOD17	In/Out	Port E2, bit 1	38	GND	-----	Ground
14	GND	-----	Ground	39	MOD04	In/Out	Port E0, bit 4
15	MOD16	In/Out	Port E2, bit 0	40	GND	-----	Ground
16	GND	-----	Ground	41	MOD03	In/Out	Port E0, bit 3
17	MOD15	In/Out	Port E1, bit 7	42	GND	-----	Ground
18	GND	-----	Ground	43	MOD02	In/Out	Port E0, bit 2
19	MOD14	In/Out	Port E1, bit 6	44	GND	-----	Ground
20	GND	-----	Ground	45	MOD01	In/Out	Port E0, bit 1
21	MOD13	In/Out	Port E1, bit 5	46	GND	-----	Ground
22	GND	-----	Ground	47	MOD00	In/Out	Port E0, bit 0
23	MOD12	In/Out	Port E1, bit 4	48	GND	-----	Ground
24	GND	-----	Ground	49	VCC	-----	+5 V
25	MOD11	In/Out	Port E1, bit 3	50	GND	-----	Ground

J6 (Frontplane DMA Connector)

J6 is a 10-pin (dual 5-pin) vertical male header with 0.1 inch contact spacing. Three frontplane DMA channels are available through this connector (depending on the configuration of cuttable traces CT16, CT17, CT25, CT29 and CT39). The pin assignments are shown in the "J6 Frontplane DMA Connector Pinout" table below. The mating connector is a T&B Ansley #622-1000 or equivalent. Refer to Chapter 6, "DMA Controller" for more information.

J6 Frontplane DMA Connector Pinout

Pin #	Signal	Type	Description
1	DRQ0/5*	In	DMA request 0 or 5
2	DRQ1/6*	In	DMA request 1 or 6
3	DAK0/5*	Out	DMA acknowledge 0 or 5
4	DAK1/6*	Out	DMA acknowledge 1 or 6
5	DRQ3/7	In	DMA request 3 or 7
6	DMAIOW*	Out	I/O write
7	DAK3/7	Out	DMA acknowledge 3 or 7
8	DMAIOR*	Out	I/O read
9	GND	----	Ground
10	TC*	Out	Terminal count

Notes:

1. Channel selection is made with cuttable traces CT16, CT17, CT25, CT29 and CT39.
2. DMAIOW* and DMAIOR* must be qualified with the respective DMA acknowledge by the DMA I/O slave.

J7 (Video/Keyboard Output Connector)

J7 is a latching 16-pin (dual 8-pin) vertical male header with 2 mm spacing. VGA video and keyboard signals are available through this connector (when W5 = Out). The pin assignments are shown in the "J7 Video/Keyboard Output Connector Pinout" table below. The mating connector is a Samtec TCSD-08-01-N.

J7 Video/Keyboard Output Connector Pinout

Keyboard Interface		VGA Interface	
Pin #	**Function**	**Pin #**	**Function**
1	Vcc	5	ENABLE
2	KBCLK	6	HSYSNC
3	GND	7	GND
4	KBDATA	8	VSYSNC
		9	RGND
		10	RED
		11	GGND
		12	GRN
		13	BGND
		14	BLU
		15	DDCCLK
		16	DDCDAT

J8 (Speaker Connector)

J8 is a latching 2-pin male low-profile header with 0.1 inch contact spacing. The speaker signals are available through this connector. The pin assignments are shown in the "J8 Speaker Connector Pinout" table below. The mating connector is a Molex 39-01-0023 or equivalent. The mating connector also requires two Molex 39-01-0031 terminals or equivalent.

J8 Speaker Connector Pinout

Pin #	Signal	Type	Description
1	SP1	Out	Speaker output
2	VCC	----	+5V

J9 (Parallel Printer Port Interface Connector)

J9 is a 20-pin (dual 10-pin) vertical male header with 0.1 inch contact spacing. This connector includes the standard Centronics printer control and data signals. The pin assignments are shown in the "J9 Parallel Printer Port Interface Connector Pinout" table below. The mating connector is a T&B Ansley #622-2030 or equivalent. See Chapter 9, "Parallel Printer Port Interface" for more information.

J9 Parallel Printer Port Interface Connector Pinout

Pin #	Signal	Type	Description
1	STB*	Out	Data strobe
2	AFD*	Out	Autofeed
3	PD0	In/out	Data bit 0
4	ERR*	In	Error
5	PD1	In/out	Data bit 1
6	INIT*	Out	Initialize
7	PD2	In/out	Data bit 2
8	SLIN*	Out	Select to printer
9	PD3	In/out	Data bit 3
10	GND	------	Ground
11	PD4	In/out	Data bit 4
12	GND	------	Ground
13	PD5	In/out	Data bit 5
14	GND	------	Ground
15	PD6	In/out	Data bit 6
16	BUSY	In	Printer busy
17	PD7	In/out	Data bit 7
18	PE	In	Paper error
19	ACK*	In	Acknowledge
20	SLCT	In	Select from printer

J10 (AC Power-Fail Connector)

J10 is a latching 2-pin male low-profile header with 0.1 inch contact spacing. The mating connector is a Molex 39-01-0023 or equivalent. The mating connector also requires two Molex 39-01-0031 terminals or equivalent. The AC input signals for the optional power-fail detection feature are available through this connector. The pin assignments are shown in the "J10 AC Power-Fail Connector Pinout" table below. Refer to Chapter 15, "AC Power-Fail," for more information.



Caution: Do not connect directly to AC line.

J10 AC Power-Fail Connector Pinout

Pin #	Signal	Type	Description
1	AC1	In	AC1
2	AC2	In	AC2

J11 (Mezzanine Video Interface Connector)

J11 provides an interface for optional PCI VGA interface boards to route video signals to the ZT 8907. Video signals are then routed through the J7 Video/Keyboard Output Connector. The zPM11 Super VGA Interface uses this mechanism. The pin assignments are shown in the "J11 Mezzanine Video Interface Connector Pinout" table below.

J11 Mezzanine Video Interface Connector Pinout

Pin #	Signal	Type	Description
1	RED	Out	VGA Red
2	GRN	Out	VGA Green
3	BLUE	Out	VGA Blue
4	NC	------	No Connect
5	GND	------	Ground (Dig)
6	GND	------	Ground (Red)
7	GND	------	Ground (Green)
8	GND	------	Ground (Blue)
9	NC	------	No Connect
10	GND	------	Ground (Sync)
11	NC	------	No Connect
12	SDA	In/Out	VGA Data
13	HSYNC	Out	VGA Hor. Sync.
14	VSYNC	Out	VGA Ver. Sync.
15	SCL	Out	VGA Data Clock
16	NC	------	No Connect

J12 (In-System Programming Connector)

J12 is the In-System-Programming (ISP) port used during the manufacturing process to program on-board PLD devices. The pin assignments are shown in the "J12 In-System Programming Connector Pinout" table below.

J12 also serves as the Port 80 Decode jumper. See Appendix A, "Board Configuration" for more about this function.

J12 In-System Programming Connector Pinout

Pin #	Description
1	GND
2	Port 80 Decode
3	Reserved
4	Reserved
5	Reserved
6	Reserved
7	Reserved
8	Reserved

J13 (PCI Mezzanine Local Bus Interface Connector)

J13 is a 150-pin 2 mm x 2 mm female receptacle providing the PCI local bus interface to optional mezzanine adapters designed for this application. J13 provides a complete 32-bit PCI interface. This connector is CompactPCI compatible. Refer to the *CompactPCI Specification* for details.

The pin assignments are shown in the "J13 PCI Mezzanine Local Bus Interface Connector Pinout" table below. See Chapter 13, "PCI Mezzanine Local Bus" for more information.

Note: Rows 12-14 on J13 are not for adapter use. Adapters use pin D6 for CLK, pin A6 for REQ#, and pin E5 for GNT#.

J13 PCI Mezzanine Local Bus Interface Connector Pinout

Pin #	A	B	C	D	E	F
25	5V	NC	NC	3.3V	NC	GND
24	AD[1]	5V	5V	AD[0]	ACK64#	GND
23	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	3.3V	AD[9]	AD[8]	GND	C/BE[0]#	GND
20	AD[12]	GND	5V	AD[11]	AD[10]	GND
19	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	3.3V	NC	NC	GND	PERR#	GND
16	DEVSEL#	GND	5V	STOP#	LOCK#	GND
15	3.3V	FRAME#	IRDY#	GND	TRDY#	GND
14	CLK13	GND	NC	CLK13	NC	GND
13	GNT2#	CLK02	NC	GND	NC	GND
12	REQ1#	GND	GNT1#	CLK13	REQ2#	GND
11	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	AD[26]	GND	5V	AD[25]	AD[24]	GND
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	REQ#	GND	3.3V	CLK02	AD[31]	GND
5	BRSV	NC	RST#	GND	GNT#	GND
4	BRSV	GND	5V	INTP	INTS	GND
3	INTA#	INTB#	INTC#	5V	INTD#	GND
2	TCK	5V	NC	NC	NC	GND
1	5V	-12V	NC	+12V	5V	GND
Pin	**A**	**B**	**C**	**D**	**E**	**F**

J14 (Optional Floppy Disk Interface Connector)

J14 is a surface mount connector location for a 26-pin optional floppy disk (located on the solder-side of the board). This interface is provided primarily for single board computer operation (without an STD 32 backplane. STD 32 users should use the ZT 8954 Floppy Disk Controller Interface for floppy support).

The pin assignments are shown in the "J14 Optional Floppy Disk Interface Connector Pinout" table below. See Chapter 18, "Optional Local Floppy Disk Interface" for more information.

J14 Optional Floppy Disk Interface Connector Pinout

Pin#	Function	Pin#	Function	Pin#	Function	Pin#	Function
1	Vcc	8	READY	15	GND	22	WP
2	INDEX	9	DENSTAT	16	WDATA	23	GND
3	Vcc	10	MOTON	17	GND	24	RDATA
4	DRSEL0	11	DENSEL	18	WGATE	25	GND
5	Vcc	12	DIR	19	GND	26	HDSEL
6	DSKCHG	13	GND	20	TRK0		
7	DRSEL1	14	STEP	21	GND		

J15 (Optional IDE Interface Connector)

J15 is a 44-pin surface mount connector location providing a local Integrated Drive Electronics (IDE) hard disk interface. The pin assignments are shown in the "J15 Optional IDE Interface Connector Pinout" table below.

Ordering option D1 includes an IDE drive integrated with the ZT 8907. This option is useful for single board computer operation (no STD 32 backplane) or for STAR SYSTEM operation where the hard disk interface is local to the ZT 8907. See Chapter 17, "Optional IDE Interface" for more information.

J15 Optional IDE Interface Connector Pinout

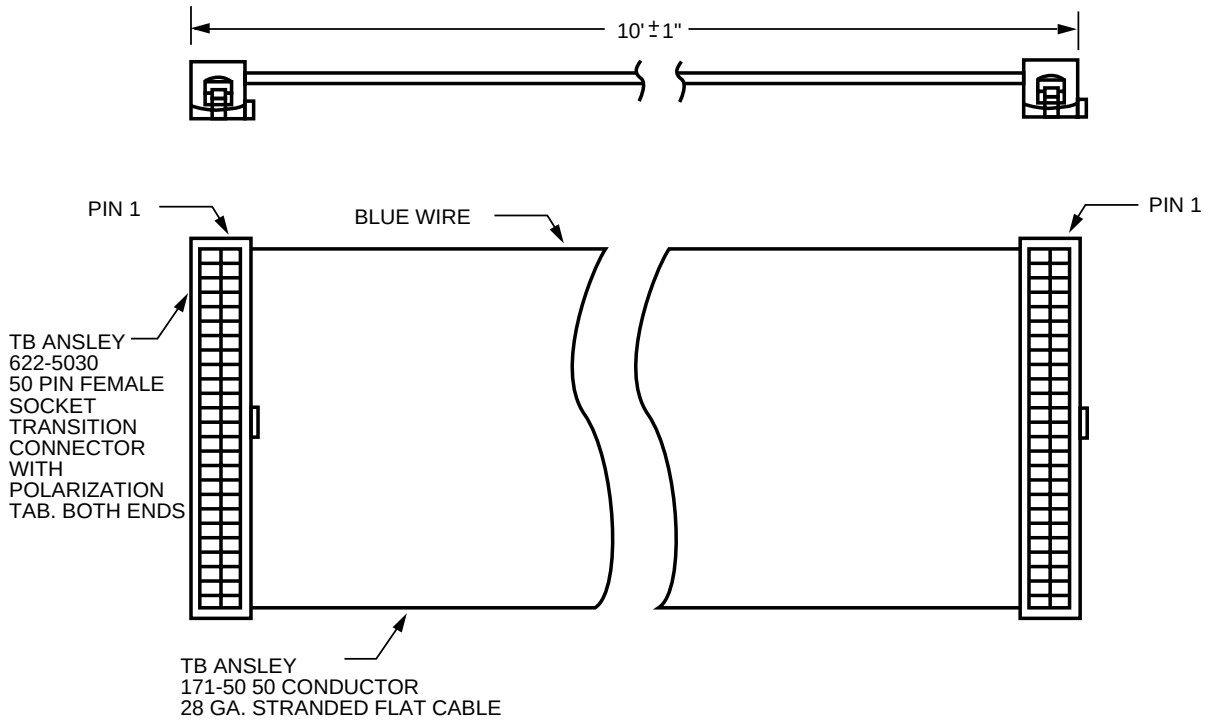
Pin#	Signal	Type	Description	Pin#	Signal	Type	Description
1	RESET*	Out	Reset	2	GND	------	Ground
3	D7	In/Out	Data Bit 7	4	D8	In/Out	Data Bit 8
5	D6	In/Out	Data Bit 6	6	D9	In/Out	Data Bit 9
7	D5	In/Out	Data Bit 5	8	D10	In/Out	Data Bit 10
9	D4	In/Out	Data Bit 4	10	D11	In/Out	Data Bit 11
11	D3	In/Out	Data Bit 3	12	D12	In/Out	Data Bit 12
13	D2	In/Out	Data Bit 2	14	D13	In/Out	Data Bit 13
15	D1	In/Out	Data Bit 1	16	D14	In/Out	Data Bit 14
17	D0	In/Out	Data Bit 0	18	D15	In/Out	Data Bit 15
19	GND	------		20	KEY	------	Cable Key
21	RSVD	------	Reserved	22	GND	------	Ground
23	IOWR*	Out	I/O Write Strobe	24	GND	------	Ground
25	IORD*	Out	I/O Read Strobe	26	GND	------	Ground
27	RSVD	------	Reserved (IORDY)	28	ALE	Out	Address Latch En.
29	RSVD	------	Reserved	30	GND	------	Ground
31	IRQ	In	Interrupt Request	32	IOCS16*	In	16-bit I/O handshake
33	A1	Out	Address Bit 1	34	PDIAG	------	Inter-drive diagnostics
35	A0	Out	Address Bit 0	36	A2	Out	Address Bit 2
37	CS0*	Out	Chip Select (1F0h-1FFh)	38	CS1*	Out	Chip Select (3F6h)
39	ACT*	In	Active/Slave present	40	GND	------	Ground
41	VCC	------	+5V - Drive Logic	42	VCC	------	+5V - Drive Motor
43	GND	------	Ground	44	XT/AT	Out	Drive Mode = AT

Cables

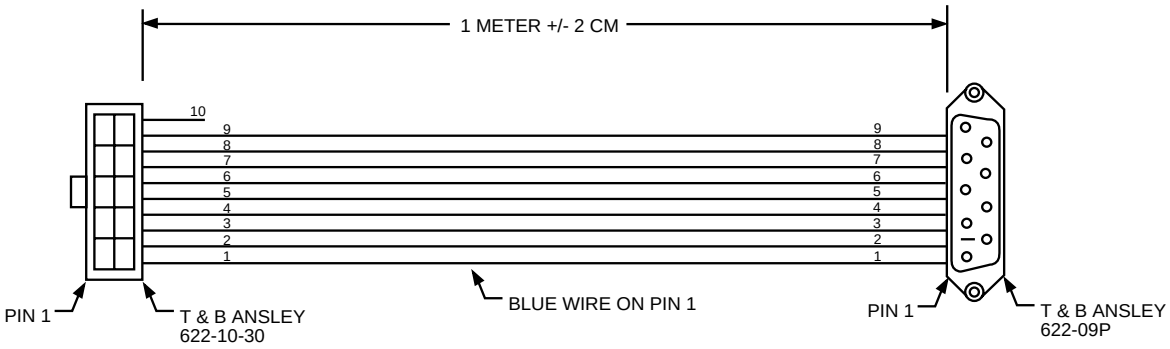
The following cables are available from Ziatech. Illustrations are included on the following pages for those who wish to make their own cables.

- ZT 90072 Digital I/O Cable
- ZT 90136 Serial Cable
- ZT 90157 Printer Cable
- ZT 90233 Video/Keyboard Cable
- ZT 90201 IDE Cable

ZT 90072 Digital I/O Cable



ZT 90136 Serial Cable

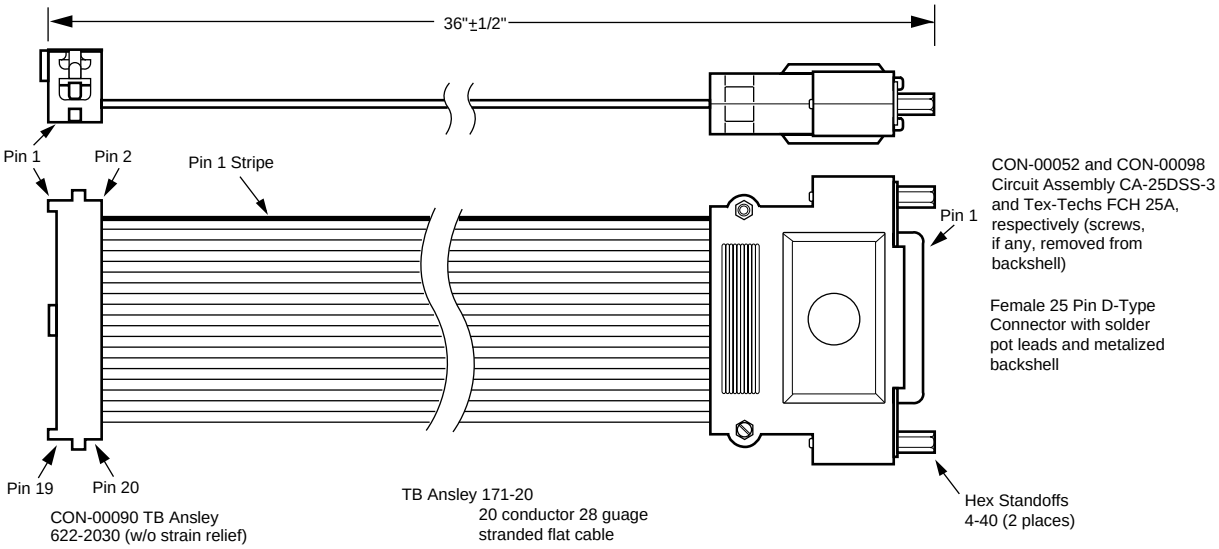


CONNECTION TABLE

622-10-30	622-09P
10	NA
9	5
8	9
7	4
6	8
5	3
4	7
3	2
2	6
1	1

1. TRIM ALL CABLE ENDS FLUSH WITH CONNECTOR BODIES.
2. USE T & B ANSLEY #171-10 STRANDED 28 AWG RIBBON CABLE.
3. ZIATECH APPROVAL REQUIRED FOR PARTS SUBSTITUTIONS.

ZT 90157 Printer Cable

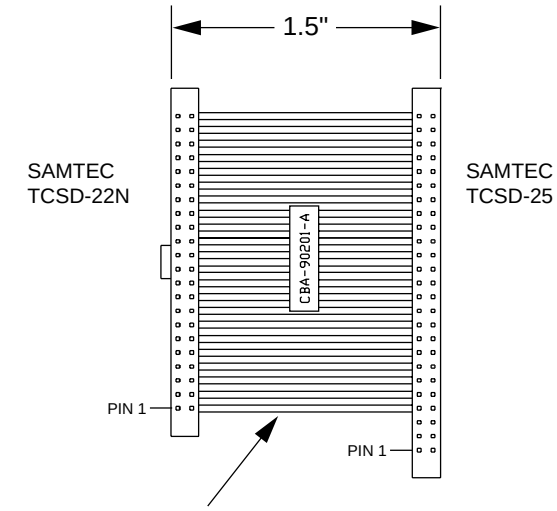


Pin Assignment Chart

Wire No.	25 Pin D Pin No	Wire No.	25 Pin D Pin No
1	1	11	6
2	14	12	21-23 *
3	2	13	7
4	15	14	24-25 *
5	3	15	8
6	16	16	11
7	4	17	9
8	17	18	12
9	5	19	10
10	18-20 *	20	13

Note: *Pins 18-25 are tied in common

ZT 90233 Video/Keyboard Cable



3M 3625/44, GRAY 44-CONDUCTOR,
1MM CENTERS, 28 GUAGE
STRANDED FLAT CABLE

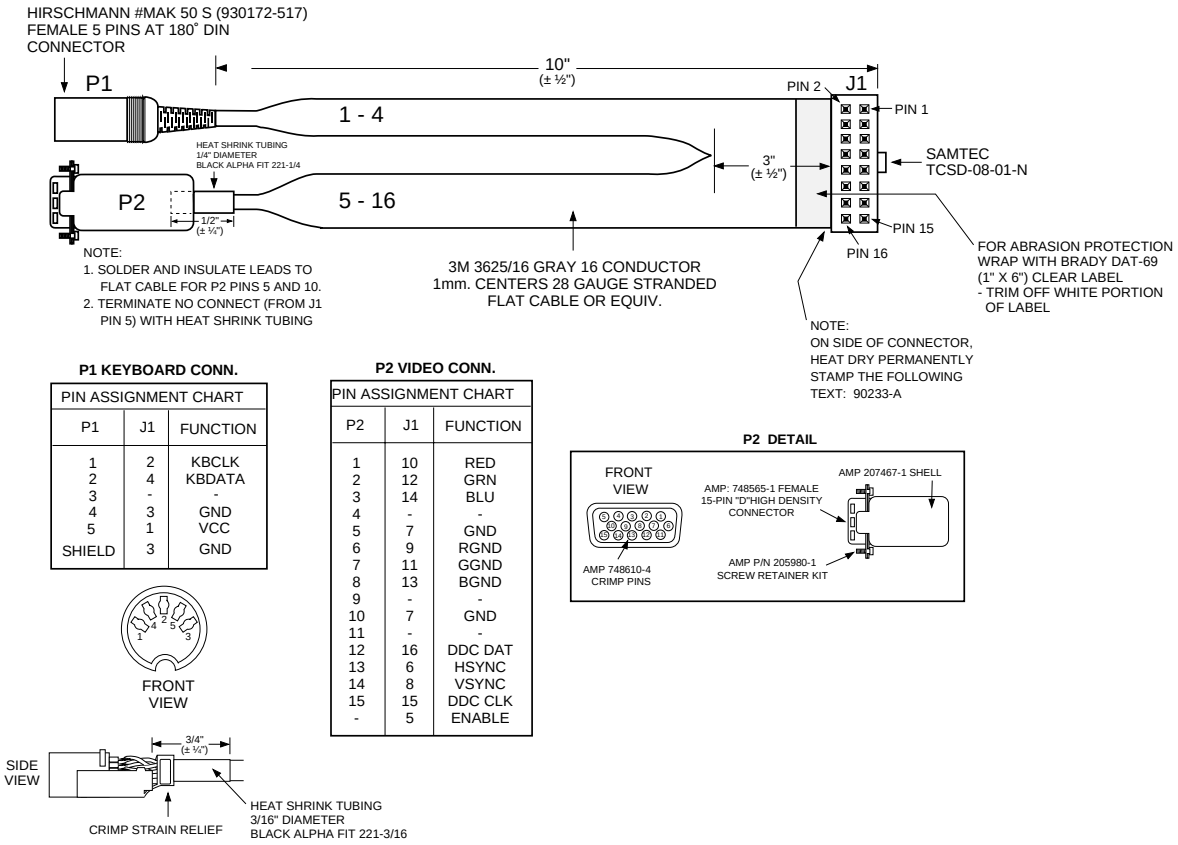
ZT8907

PIN CONNECTION TABLE

TCSD-22N	TCSD-25	TCSD-22N	TCSD-25
1	7	23	29
2	8	24	30
3	9	25	31
4	10	26	32
5	11	27	33
6	12	28	34
7	13	29	35
8	14	30	36
9	15	31	37
10	16	32	38
11	17	33	39
12	18	34	40
13	19	35	41
14	20	36	42
15	21	37	43
16	22	38	44
17	23	39	45
18	24	40	46
19	25	41	47
20	26	42	48
21	27	43	49
22	28	44	50

NOTES:
1. PINS 1, 2, 3, 4, 5, AND 6 OF THE TCSD-25 CONNECTOR ARE NOT CONNECTED

ZT 90201 IDE Cable



P1 KEYBOARD CONN.

PIN ASSIGNMENT CHART		
P1	J1	FUNCTION
1	2	KBCLK
2	4	KBDATA
3	-	-
4	3	GND
5	1	VCC
SHIELD	3	GND

FRONT
VIEW

P2 VIDEO CONN.

PIN ASSIGNMENT CHART		
P2	J1	FUNCTION
1	10	RED
2	12	GRN
3	14	BLU
4	-	-
5	7	GND
6	9	RGND
7	11	GGND
8	13	BGND
9	-	-
10	7	GND
11	-	-
12	16	DDC DAT
13	6	HSYNC
14	8	VSYNC
15	15	DDC CLK
-	5	ENABLE

P2 DETAIL

C. DIGITAL I/O ASIC SYSTEM SETUP CONSIDERATIONS

The purpose of this appendix is to illustrate precautions you should take to prevent latchup conditions and protect inputs.

The 16C50A Digital I/O ASIC device used on the ZT 8907 is designed by Ziatech to offer bi-directional I/O signals with or without event sense capability. This device features low power, high speed, wide temperature operation achievable only by utilizing CMOS technology.

Although CMOS technology offers many advantages, you must observe a few cautions when interfacing to any CMOS parts.

- CMOS inputs and outputs can exhibit latchup characteristics. These inherent characteristics of any CMOS technology can result in the formation of a Silicon-Controlled Rectifier (SCR) that appears between Vcc and ground when voltages greater than Vcc or less than ground are applied to inputs or outputs. When this happens, Vcc is effectively shorted to ground. The only way to remove the latchup condition is to shut off the power supply. If a large current is allowed to flow through the chip, its operating temperature may increase, it may exhibit intermittent operation, or it may be damaged.

- CMOS inputs must be protected from slow rising signals and inductive coupling on their inputs. Failure to do so will allow a potentially large current to flow through the chip, damaging the chip.

For more information on how the Digital I/O ASIC works, refer to the section "Functional Description" in Chapter 10, "Parallel I/O."

Several ports of the on-board 16C50A Digital I/O ASIC device are used for monitoring and controlling other board functions. See the section Chapter 11, "System Registers," for more information.

PREVENTING SYSTEM LATCHUP

The most common causes of latchup are:

- Input signals applied before the input circuitry is powered, resulting in a signal to power supply sequence mismatch

- Input signals greater than Vcc or less than ground, resulting in a signal level mismatch

These conditions are covered in the following topics.

Power Supply Sequence Mismatch

A common application is to interface to a 24-position ZT 2226, Opto 22, or equivalent I/O module rack. Vcc and ground are provided from the ZT 8907 through connector J5, with Vcc protected by a 1 A fuse. This application is illustrated in Figure 1. In this application, no power supply sequence mismatch exists because the power supplying the input circuitry within the Digital I/O ASIC is applied before or at the same time as the power supplying the external signals. Proper system operation will result.

However, if a power source other than that supplying the Digital I/O ASIC is used to power the external signals, then a power sequence mismatch could occur, resulting in a latchup condition. An external power source might be required if the external circuitry requires more than the 500 mA supplied by the cable or if a custom interface is being designed (see Figure 2).

One solution is to switch the external signals' power supply with an output that is controlled by the computer. In this manner, if the computer is off, so is the external power supply. This solution is illustrated in Figure 3.

A simpler solution is to power the relay controlling the external power supply directly from Vcc and ground supplied by the interface cable.

Another solution is to utilize the same switch to control the computer's power supply and the external signals' power supply (see Figure 4). This is an acceptable solution for power supply sequence mismatches as long as the computer supply ramps up faster than the external power supply. This ensures the Digital I/O ASIC input circuitry is powered before the external signal circuitry.

Figure 1. I/O Rack Vcc and Ground Supplied Via Interface Cable

Correct Power Supply Sequence, Signal Level Matched

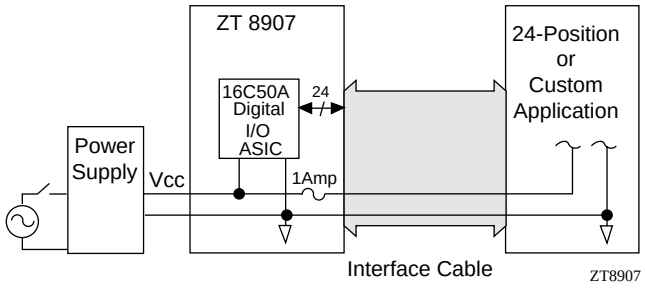


Figure 2. I/O Rack Vcc and Ground Supplied Externally

Potential Power Supply Sequence Mismatch, Signal Level Mismatch

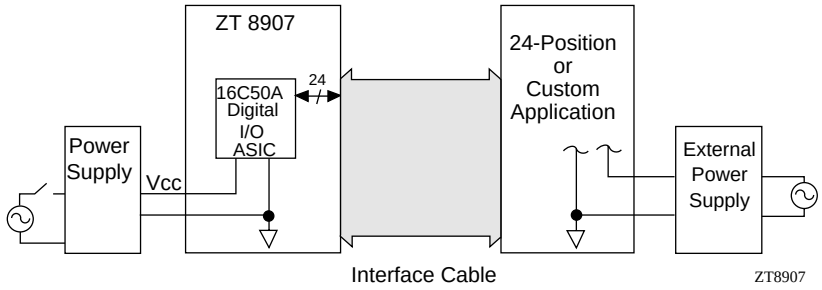


Figure 3. Computer-Switched External Power Supply

Correct Power Supply Sequence, Potential Signal Level Mismatch

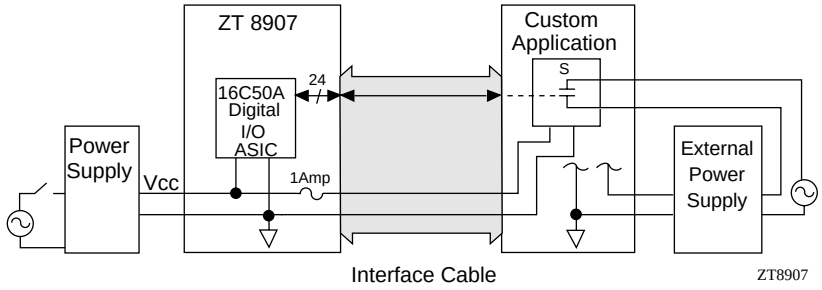
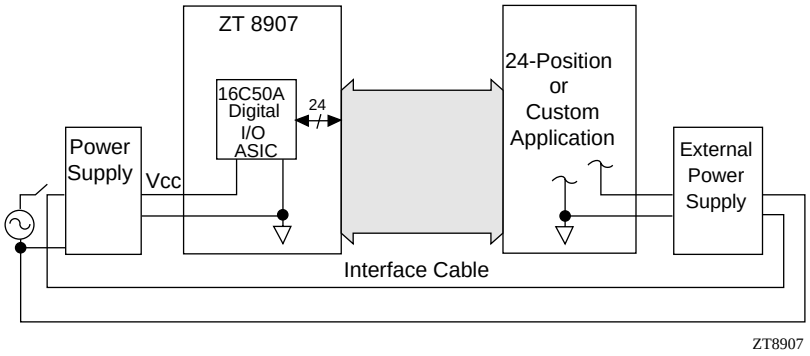


Figure 4. Computer and External Power Supply with Common Switch
Correct Power Supply Sequence, Potential Signal Level Mismatch



Signal Level Mismatch

Power supplying the external signal in Figure 1 is always relative to the Digital I/O ASIC input circuitry power because power is provided over the interface cable. Signal level mismatches will not occur and proper system operation will result. However, if separate power supplies are used, there are two predominant causes of signal level mismatches.

The first (assuming no sequencing problems) occurs when the two supplies are not referenced to each other, as illustrated in Figure 2, Figure 3, and Figure 4. This results in signals that may be higher than Vcc or lower than ground, potentially causing SCR latchup. All that is generally needed is to reference one supply to the other, typically by connecting a common ground. The most convenient way of connecting a common ground is to use the interface cable. Figure 5, Figure 6, and Figure 7 illustrate correct ground connections.

The second cause of mismatch occurs when the two power supplies are referenced to each other but the Vcc difference between the two power supplies exceeds 0.5 V. This results in signals that could be greater than Vcc, causing SCR latchup. This is easily remedied by adjusting the external power supply voltage to be within 0.5 V of the computer power supply voltage.

Figure 5. I/O Rack Vcc Supplied Externally, Common Ground
Potential Power Supply Seq. Mismatch, Correct Signal Level Match

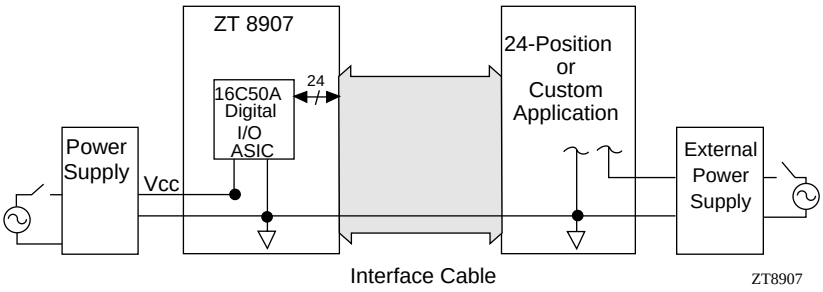


Figure 6. Computer-Switched External Power Supply, Common Ground

Correct Power Supply Sequence, Correct Signal Level Match

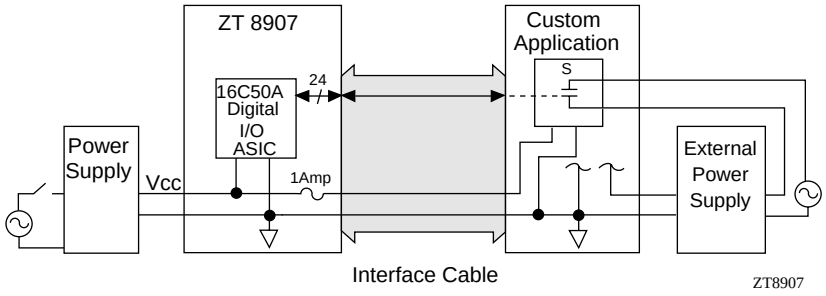
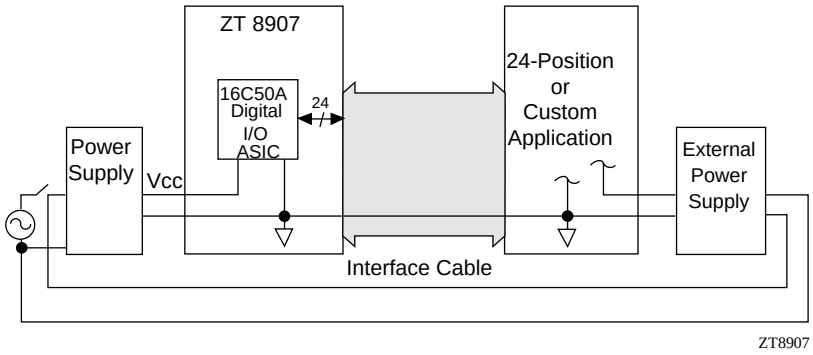


Figure 7. Computer and External Power Supply with Common Switch and Ground

Correct Power Supply Sequence, Correct Signal Level Match



PROTECTING CMOS INPUTS

The most common causes of damaged inputs are:

- Slow rise times, resulting in a ground bounce within the chip
- Inductive coupling on I/O lines causing noise to be coupled into the chip, resulting in intermittent operation

Each of these conditions is covered in the following topics.

Rise Times

Slow rise times on a CMOS input can easily cause the transistor to bounce between Vil and Vih. When this oscillation occurs, the operating current goes up, resulting in "ground bounce." Ground bounce can cause internal latchup or can cause other system components to malfunction. A pullup termination resistor is used to increase the rise time.

Input rise times must be kept to less than 50 ns. Given a maximum chip capacitance of 10 pF, a 5 k Ω resistor is the largest that could be used without additional cabling. As

cabling is added, the capacitance goes up, resulting in the use of a smaller pullup resistor until the maximum sink current of the output is achieved.

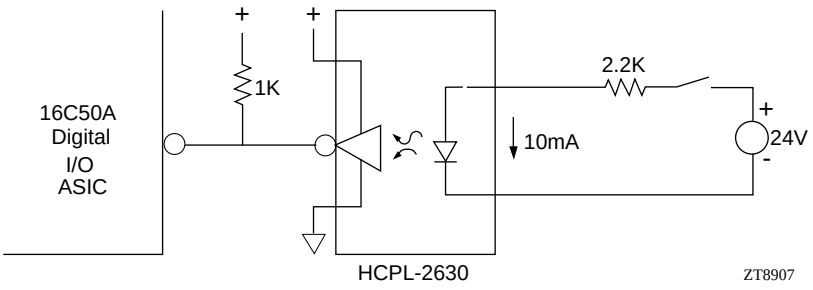
If the 16C50A Digital I/O ASIC device is driving the output, its maximum sink current at a Vol of .4 V is 12 mA. This gives a lower limit of 420 ohms for the pullup resistor, allowing a maximum cabling capacitance of 110 pF.

Note that while the input feature of the Digital I/O ASIC may not be used by your application (Digital I/O ASIC used as an output only), the input circuitry remains in parallel; therefore, the output rise time is still a critical parameter that the input still sees. The output rise time must not exceed 50 ns. Be wary of using low pass filters to remove electrical noise. The resulting capacitance is typically too large to meet the 50 ns rise time requirement.

Typically, optical isolators are used to help remove electrical noise while providing for different grounds. Separate grounds are achieved through the use of an additional power supply for the optocoupler rather than using the computer's power supply. If the computer's power supply powers the optocouplers, electrical isolation is defeated. An example of one such circuit is illustrated in Figure 8. The circuit can be altered to allow for design considerations.

Assuming a Vil of 1 V maximum for the 16C50A Digital I/O ASIC, the Hewlett-Packard® Dual Optocoupler must have a Vol of less than or equal to 1 V over the operating temperature. Using a TTL-compatible optocoupler gives a Vol of .6 V maximum with rise and fall times (50 ns and 10 ns, respectively) that are easily compatible with the Digital I/O ASIC, given a 1 k ohm pullup.

Figure 8. Digital I/O ASIC-to-Optocoupler Interface Example



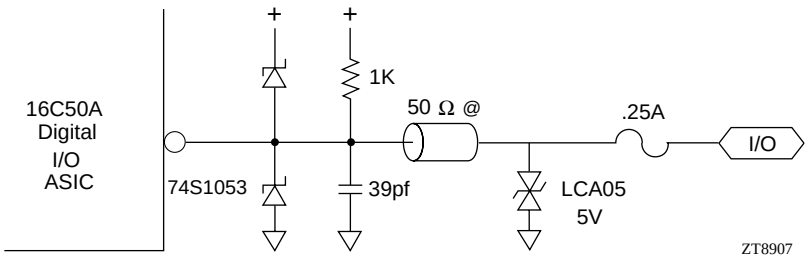
Inductive Coupling

Inductive coupling on I/O lines can cause noise to be coupled into the chip, resulting in intermittent operation. This situation occurs when the Digital I/O ASIC I/O signals are routed with other signals within a wire bundle. One way to filter inductively coupled noise, or any noise for that matter, within a system with the same ground (not using optocouplers) is illustrated in Figure 9.

In the above circuit, the Texas Instruments 74S1053 Schottky diode clamps limit a transient to ±1 V above +5 V or below ground. The ferrite bead has a 50 ohm impedance at the frequency of interest. As the diodes begin to clamp and current flows through them, the voltage across the LCA05 5 V bi-directional TransZorb® increases, causing them to conduct and allowing the majority of energy to flow through them instead of through the diode clamps.

The 39 pF capacitor, in conjunction with the ferrite bead, forms an additional low pass filter, and is entirely optional. The 1 k ohm pullup ensures adequate rise time on the signal. The fuse acts as additional insurance against catastrophic events that might destroy the TransZorb and diode clamps.

Figure 9. Digital I/O ASIC-to-Filter Interface Example



ADDITIONAL INFORMATION

Additional design information is available in the *Advanced CMOS Logic Designer's Handbook*, published by Texas Instruments. The web site for Texas Instruments is http://www.ti.com.

D. PCI CONFIGURATION SPACE MAP

All PCI compliant devices contain a PCI configuration header. The generic layout of the header is shown in the "PCI Configuration Header" figure below.

Additionally, a device may contain unique configuration registers (at location > 40h). For the ZT 8907, these are shown in the "On-Board Device PCI Bus Mapping" table below.

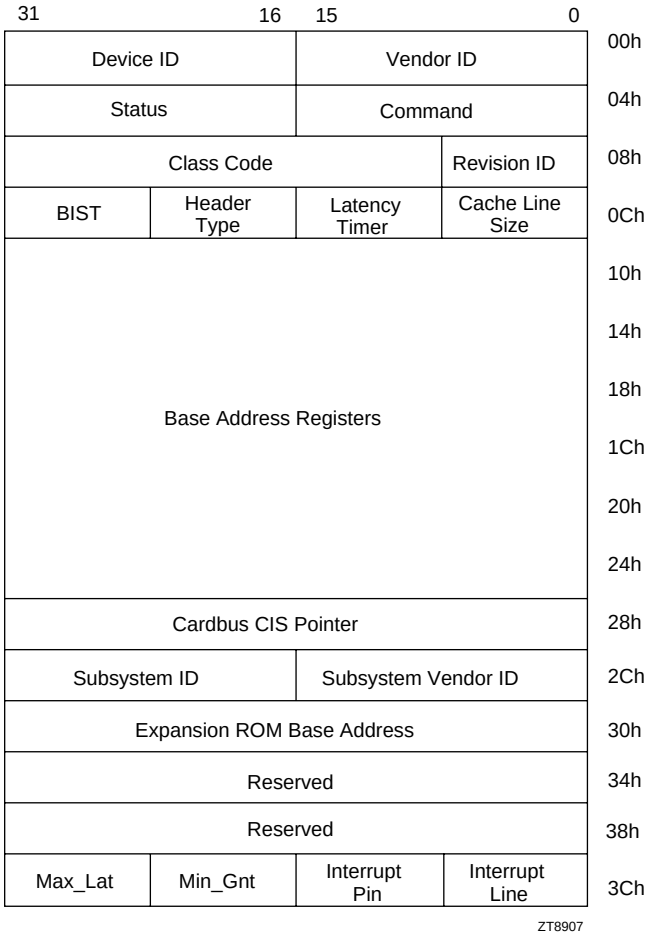
Details for each device's configuration space can be found in the respective manufacturer's data manuals. For more information on the PCI chipset implemented on the ZT 8907, refer to the *FINALi-486 M1489/M1487 486 PCI Chip Set Data Sheet*, or contact ALi distributor Pacific Group Technology at (408) 764-0644.

On-Board Device PCI Bus Mapping

Bus # (hex)	Dev # (hex)	Fcn # (hex)	Vendor ID	Device ID	Description
00	00	00	10B9	1489	ALi 1489 PCI Controller
00	01	00	1138	8905	Ziatech PCI-to-STD Bridge
00	03	00	†	†	Mezzanine Connector

† The vendor and device ID will vary depending upon the device plugged into the mezzanine connector.

PCI Configuration Header



E. ZT 8907 VS. ZT 8902: TECHNICAL DIFFERENCES

This section describes the technical differences between the ZT 8907 and the ZT 8902 single board computers. It includes information to help existing ZT 8902 customers adapt their applications to the ZT 8907.

ZT 8907 NEW FEATURES

As shown in the list below, the ZT 8907 incorporates new features that are improvements over the ZT 8902 design.

- Software configuration of interrupt routing options via screen 2 of the BIOS SETUP utility.
- A 128 Kbyte battery-backed SRAM module is available on the ZT 8907. This SRAM can be paged into the memory map (real mode) as a location to save critical data without having to write to flash memory.
- A flash memory "write-protect" jumper (W9) physically gates the write line to the flash memory device(s).
- The ZT 8907 uses industry standard 72-pin SO-DIMM DRAM modules (commonly implemented on laptop computers). Modules may be purchased in 4, 8, or 16 Mbyte sizes allowing for 4 Mbytes minimum and 32 Mbytes maximum onboard memory capacity.
- An integrated 1.4 Gbyte IDE drive can be mounted to an optional onboard IDE interface on the back of the ZT 8907. Option D1 to the ZT 8907 includes a hard disk, cable, and connector. When configured for local IDE operation, the ZT 8907 requires one additional slot in the STD 32 card cage.

ZT 8907 MECHANICAL ISSUES

The ZT 8907 was designed to minimize the amount of system redesign necessary for existing ZT 8902 applications. The ZT 8907's frontplane connectors were designed to be compatible (mechanically and pin-to-pin) with those on the ZT 8902 board. The "ZT 8907 / ZT 8902 Connector Cross Reference" table presents the connector designations on each board.

Due to chipset differences between the ZT 8902 and ZT 8907, the ZT 8907 does not support the "local bus" style mezzanine boards (zVID1 and zVID2). Instead, the ZT 8907 implements a local PCI mezzanine connector (J13) to accommodate Ziatech PCI mezzanine video boards (zPM11, zPM12). J13 provides a complete 32-bit PCI interface. In addition to offering substantially increased performance over STD bus video, both "local bus" (ZT 8902) and PCI bus video solutions (ZT 8907) have the

advantage of not requiring the additional card cage slot that STD bus video boards require.

In order to support the video interface design of Ziatech's local PCI mezzanine boards, the ZT 8907 includes an additional connector (J7) for attaching a 2 mm ribbon cable for VGA and keyboard support. The 2 mm cable connected to the zVID2 card in existing ZT 8902 applications is easily modified: replace the 50-pin (female) header with a 16-pin (female) header for mating to J7 on the ZT 8907.

ZT 8907 / ZT 8902 Connector Cross Reference

Connector Function	Pin Count	ZT 8907 Designation	ZT 8902 Designation
AC Power Fail	2	J10	J1
Aux. Counter/Timers	10	J2	J6
COM1 Serial (RS-232)	10	J4	J8
COM2 Serial (RS-232)	10	J3	J7
Digital I/O (24 lines)	50	J5	J5
Frontplane DMA	10	J6	J10
Frontplane Interrupts	10	J1	J3
Hard Drive Connector	44	J15	N/A
Local Bus Video	100	N/A	J4
Local PCI Mezzanine	175	J13	N/A
Printer Port	20	J9	J2
Speaker Interface	2	J8	J9
VGA Transition Connector	16	J11	N/A
VGA/Keyboard Interface	16	J7	N/A (50-pin on zVID2)

ZT 8907 PROGRAMMING ISSUES

In most cases, ZT 8902 applications that do not program any VLSI chipset registers or flash memory ports directly will not require modification in order to run on the ZT 8907.

Unchanged configurable items include:

- The COM1, COM2, Digital I/O, and Timer/Counters peripherals are in the same I/O locations on both boards.
- The available interrupt routing selections are the same on both boards.
- Software configuration of interrupt routing (via the BIOS SETUP utility) is similar on both boards.

Device and/or mapping differences on the ZT 8907 include:

- Chipset: Acer Labs (ALi) FINALi Chipset (M1489/M1487) 486 PCI chipset
- Flash memory: Up to two 2 Mbyte AMD or Intel flash devices may be factory installed. Flash memory is mapped in one contiguous block accessible from FFC00000h - FFFFFFFFh (if 4 Mbytes are installed). Of this, the BIOS occupies ranges FFFFF000h - FFFFFFFFh (top 64 Kbytes) and FFEE0000h - FFF00000h.
- I/O Map Changes: There are some differences between the ZT 8902 and ZT 8907 I/O maps. Compare the I/O maps in the respective manuals to learn these differences.

ZT 260 AND ZT 310 ENCLOSURES

Listed below are the new options added to the ZT 2502 and ZT 2503 front plates to support the ZT 8907 video/keyboard connector.

- ZT 2502-V8: System Plate for ZT 8907 (single CPU system)
- ZT 2502-V9: System Plate for multiple ZT 8907s in a STAR SYSTEM
- ZT 2503-V8: Video/Keyboard Access Plate for a single ZT 8907 (STAR SYSTEM temporary master)
- ZT 2503-V9: Video/Keyboard Access Plate for multiple ZT 8907s in a STAR SYSTEM

F. CUSTOMER SUPPORT

This appendix offers technical and sales assistance information for this product, warranty information, and necessary information for the return of a Ziatech product.

TECHNICAL/SALES ASSISTANCE

If you have a technical question, please call Ziatech's Customer Support Service at the number below, or e-mail our technical support team at tech_support@ziatech.com. Ziatech also maintains an FTP site located at ftp://ziatech.com/Tech_support.

If you have a sales question, please contact your local Ziatech Sales Representative or the Regional Sales Office for your area. Address, telephone and FAX numbers, and additional information are available at Ziatech's website, located at http://www.ziatech.com.

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RELIABILITY

Ziatech takes extra care in the design of the product in order to ensure reliability. The product was designed in top-down fashion, using the latest in hardware and software design techniques, so that unwanted side effects and unclean interactions between parts of the system are eliminated. Each product has an identification number. Ziatech maintains a lifetime data base on each board and the components used. Any negative trends in reliability are spotted and Ziatech's suppliers are informed and/or changed.

RETURNING FOR SERVICE

Before returning any of Ziatech's products, you must phone Ziatech at (805) 541-0488 and obtain a Return Material Authorization (RMA) number. Please supply the following information to Ziatech in order to receive an RMA number:

- Your company name and address for invoice
- Your shipping address and phone number
- The product I.D. number
- The name of a technically qualified individual at your company familiar with the mode of failure

Once you have an RMA number, follow these steps to return your product to Ziatech:

1. Contact Ziatech for pricing if the warranty expired.

2. Supply a purchase order number for invoicing the repair if the warranty expired.

3. Pack the board in **anti-static** material and ship in a sturdy cardboard box with enough packing material to adequately cushion it.

Note: Any product returned to Ziatech improperly packed will immediately void the warranty for that particular product!

4. Mark the RMA number clearly on the outside of the box.

ZIATECH WARRANTY

Warranty information for Ziatech products is available at Ziatech's website, located at http://www.ziatech.com.

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