830-0016-03 Rev A 11/15/96

ROSS TECHNOLOGY, INC.

PRELIMINARY

Colorado 4 RT6224K

hyperSPARC™ CPU Module

Features

- **Based on ROSS' fifth-generation hyperSPARC™ processor**
  - **— RT620D Central Processing Unit (CPU)**
  - **— RT626 Cache Controller, Memory Management, and Tag Unit (CMTU)**
  - **— Four (512-Kbyte) or eight (1-Mbyte) RT628 Cache Data Units (CDUs)**
  - **— Intra-Module Bus incorporates low voltage logic to reduce power and increase speed**
- **Full multiprocessing implementation**
  - **— Hardware support for symmetric, shared-memory multiprocessing**
  - **— Level 2 MBus support for cache coherency**
- **SPARC compliant**
  - **— SPARC Instruction Set Architecture (ISA) Version 8 compliant**
  - **— Conforms to SPARC Reference MMU Architecture**
  - **— Conforms to SPARC Level 2 MBus Module Specification (Revision 1.2)**
- **Dual-clock architecture**
  - **— CPU scaleable up to 200 MHz**
  - **— MBus scaleable up to 66 MHz**
- **Each hyperSPARC processor features**
  - **— Superscalar SPARC CPU with integrated floating point unit, 16-Kbyte instruction cache, and 16-Kbyte data cache**
  - **— Speculative fetch keeps primary caches loaded to assure high cache hit rates**
  - **— Zero-wait-state, 512-Kbyte or 1-Mbyte 2nd-level cache**
  - **— Demand-paged virtual memory management**
- **Module design**
  - **— MBus-standard form factor: 3.30" (8.34 cm) x 5.78" (14.67 cm)**
  - **— Provides CPU upgrade path at module level**
  - **— Advanced packaging technology for a compact design**
- **High performance ***
  - **— 224-229 SPECint92**
  - **— 247-259 SPECfp92**

  *** in a 66MHz MBus system**

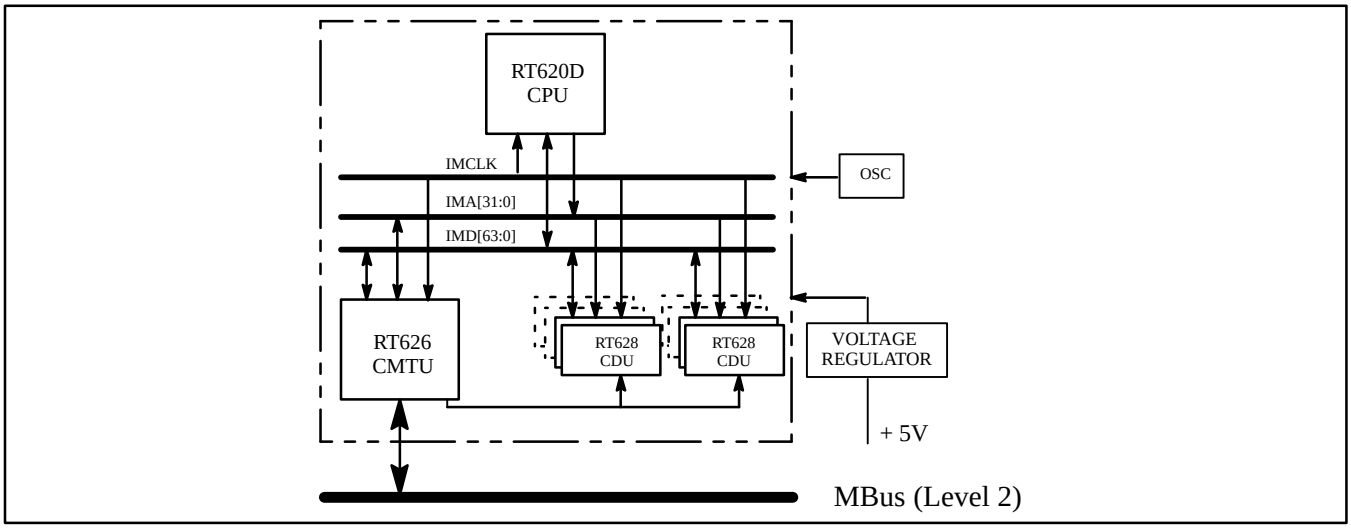


Figure 1. Logic Block Diagram

Selection Guide

Part Number: RT6224K *	-180/512	-180/1024	-200/512	-200/1024
CPU Operating Frequency (MHz)	180	180	200	200
Typical Power Consumption (w)**				
Second-level Cache Size	512K	1M	512K	1M
SPECint92 / SPECfp92			224 / 247	229 / 259
SPECrateint92 / SPECratefp92 (single processor)				
SPECrateint92 / SPECratefp92 (dual processor)				

*See Appendix C for hyperSPARC ordering information

** Commercial

Functional Description

The RT6224K hyperSPARC Module is a complete SPARC CPU, including on-board primary and secondary cache memories. It is packaged as a compact PCB and interfaces to the remainder of the system via a SPARC-standard MBus connector. The CPU on the RT6224K consists of a high-speed superscalar, highly pipelined processor with dual integer ALUs and an on-chip floating-point unit (RT620D), a Cache Controller, Memory Management, and Tag Unit (RT626), and four (512-Kbyte cache configuration) or eight (1-Mbyte cache configuration) RT628 Cache Data Units. The RT6224K fits within the clearance envelope for MBus modules per the SPARC MBus Specification.

The RT6224K interfaces to the rest of the system via the SPARC MBus and conforms to the SPARC Reference MMU. This standardization allows the RT6224K to be interchangeable with other SPARC MBus-based CPU modules without having to modify any portion of the memory system or I/O. This CPU "building block" strategy not only decreases the user's time to market, but provides a mechanism for upgrading in the field.

Component Overview

Superscalar SPARC Processor (RT620D)

The RT620D Central Processing Unit is the heart of ROSS' fifth-generation of microprocessor. The RT620D CPU architecture employs two advanced concepts for increasing computer system performance: superscalability and superpipelining.

The RT620D is a high performance full-custom CMOS implementation of integrated SPARC integer and floating-point logic, with separate on-chip instruction and data caches.

Advanced architecture and manufacturing technologies give the RT620D ultra high performance without requiring software recompilation. *Figure 2* is a logic block diagram of the RT620D.

IDP. The Integer Data Path comprises several units. Two independent Arithmetic and Logic Units (ALUs) handle integer arithmetic, logical, and shift instructions. The Load/Store Unit (LSU) handles instructions that load and store data between memory and registers, which includes the loading and storing of both integer and floating-point data. The Special

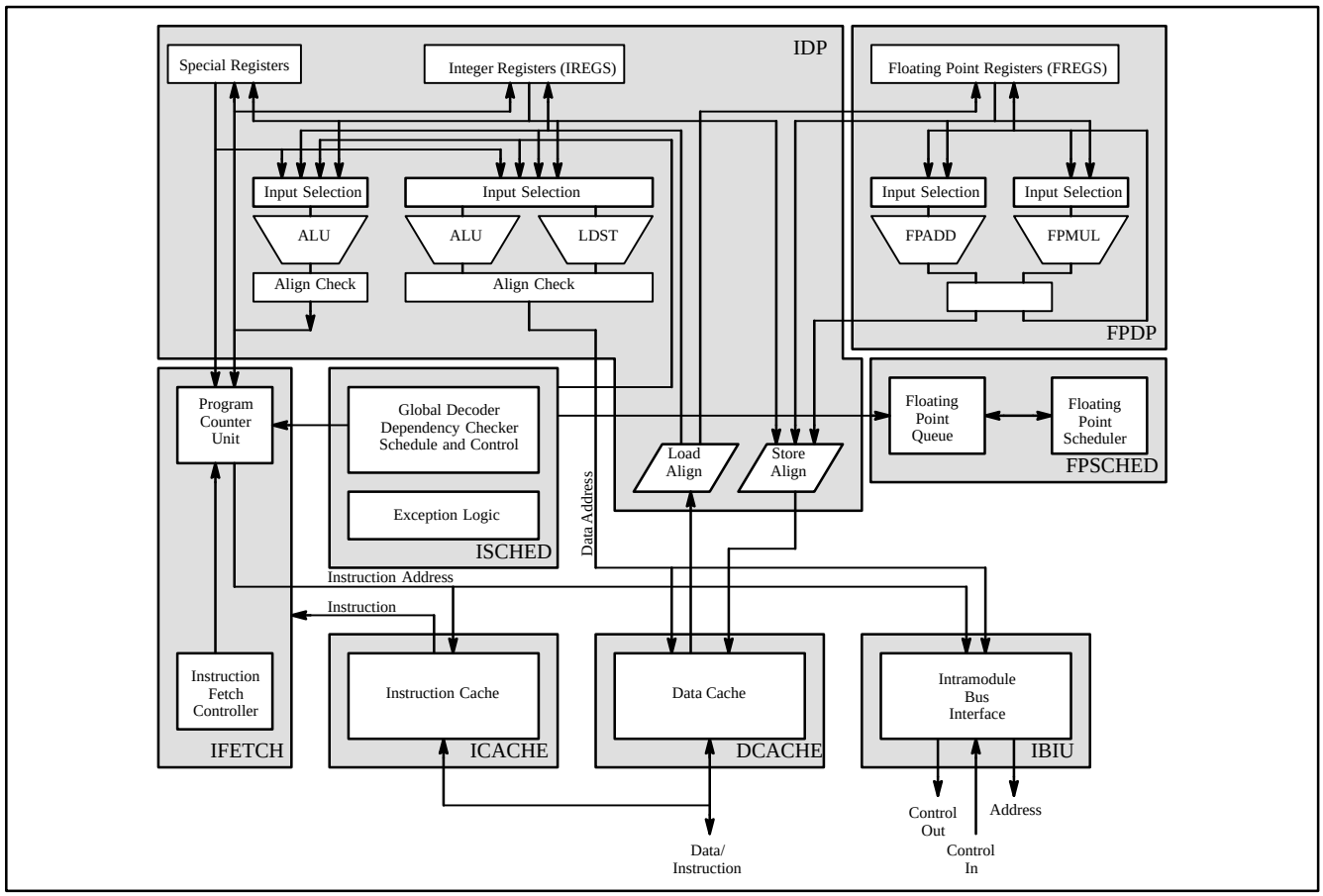


Figure 2. RT620D CPU Logic Block Diagram

Register Unit (SRU) handles instructions that read and write the SPARC Special Registers (SREGS). The Integer Register File (IREGS) is also contained in the IDP.

FPDP. The Floating-Point Data Path also comprises several units. These are the Floating-Point Queue (FPQ), the Floating-Point Arithmetic Unit (FAU), The Floating-Point Multiplier Unit (FMU), the Floating-Point Register File (FREGS), and the Floating-Point Status Register (FSR). The multiplier unit implements full double-precision multiplies. These floating-point units handle all SPARC floating-point instructions.

ISCHED. The Integer Scheduler performs key control functions. It provides global instruction decodes to identify which execution unit resources are required, and determines whether sequential or simultaneous execution is possible.

The ISCHED also determines whether data forwarding can be performed and whether instruction dispatches (also called "launches") need to be delayed due to data dependencies. The ISCHED initiates instruction launch and identifies and controls interrupt and trap handling**.**

FPSCHED. The Floating-Point Instruction Scheduler performs key control functions for the floating-point unit. When the Integer Unit detects floating-point instructions in the decode stage, it offloads these instructions to the floating-point functional units and continues processing. Therefore, functional blocks exist that perform necessary decode, scheduling, and control for the floating-point operations.

The FPSCHED performs floating-point instruction decoding, resolves floating-point data dependency and data-forwarding conditions, and provides the ISCHED with floating-point execution status. Delayed instructions are stored temporarily in the Floating-Point Instruction Queue (FPQ). Instructions are launched from the FPQ as data dependencies are resolved.

IFETCH. The Instruction Fetch Unit consists of two major functional blocks referred to as the Program Counter Unit (PCU) and the Instruction Fetch Controller (IFETCHC).

The PCU calculates the address of the next instruction to be fetched. It handles instructions that cause program control transfer, such as CALL and BRANCH. This unit handles both integer and floating-point branch instructions.

The IFETCHC fetches two instructions at a time, and in each clock cycle, the CPU attempts to launch both at once. To improve ICACHE hit rates, the CPU attempts to fetch the next doubleword each time a miss is detected. This speculative fetch succeeds if there are no pending data accesses and if the required data resides in the secondary cache.

ICACHE. The on-chip instruction cache is organized as a four way set associative buffer. The ICACHE stores 16 Kbytes of instructions. Its inclusion follows the Harvard architecture approach, reducing bus contention during memory accesses. The ICACHE has a 4 to 5 CPU clock cycle cache miss penalty.

DCACHE. The on-chip data cache is organized as a four way set associative buffer. The DCACHE is 16 Kbytes, organized as 512 lines of 32 bytes each. Lines are virtually indexed and virtually tagged. The DCACHE uses a write through with no write allocate policy, with a pseudo random replacement algorithm. One doubleword is fetched for every DCACHE miss. To improve the hit ratio, the next speculative fetch is performed in the same cache line in the DCACHE.

Unlike the ICACHE, the DCACHE is always a subset of the secondary cache. Secondary cache snoop invalidates and line replacements automatically cause a line in the DCACHE to be invalidated. Since the DCACHE is virtually addressed and has no context information, the entire DCACHE must be flushed on context switches and page remapping. Also, the DCACHE line size may not be the same as the secondary cache, so a flush must always use a stride of 32 bytes to assure the DCACHE is flushed completely.

IBIU. The Intra-Module Bus Interface Unit provides the interface between the RT620D CPU and the external world. The IBIU samples incoming control signals and propagates controls to appropriate functional blocks. The IBIU is responsible for generating memory access control signals to the cache memory subsystem. Data and instructions are read from memory and data is written to memory, through the IBIU.

Cache Control, Memory Management, and Tag Unit (RT626)

The CMTU (RT626) is a combined Cache Controller and Memory Management Unit optimized for multiprocessing systems. The CMTU is a high-speed CMOS implementation of the SPARC Reference MMU, combined with cache, a memory controller, and on-chip physical cache tag memory. The CMTU supports the SPARC MBus Level 2 protocol for multiprocessing systems. *Figure 3* depicts the CMTU block diagram.

The CMTU directly connects to the RT620D Central Processing Unit and RT628 Cache Data Units without any external circuitry. The RT626 CMTU uses four or eight RT628 CDUs to realize 512 Kbytes or 1 Mbyte, respectively, of zero-wait-state, direct-mapped virtual cache memory.

MMU. The MMU portion of the CMTU provides translation from a 32-bit virtual address (4 gigabytes) to 36-bit physical address (64 gigabytes), as provided in the SPARC reference MMU specification. Virtual addresses are further extended with the use of a context register, which is used to identify up to 4096 contexts or tasks. The TLB entries contain context numbers to identify tasks or processes. This minimizes unnecessary TLB entry replacement during task switching.

The CMTU performs its address translation task by comparing a virtual address supplied by the RT620D through the Intra-Module Bus to the address tags in the TLB entries. If a "hit" occurs, the physical address stored in the TLB is used to translate the virtual-to-physical address. If the virtual address does not match any valid TLB entry, a "miss" occurs. This causes a table walk to be performed by the MMU. The table walk is a search performed by the MMU through the address translation tables stored in main memory. Upon finding the PTE, the MMU translates the address and selects a TLB entry for replacement.

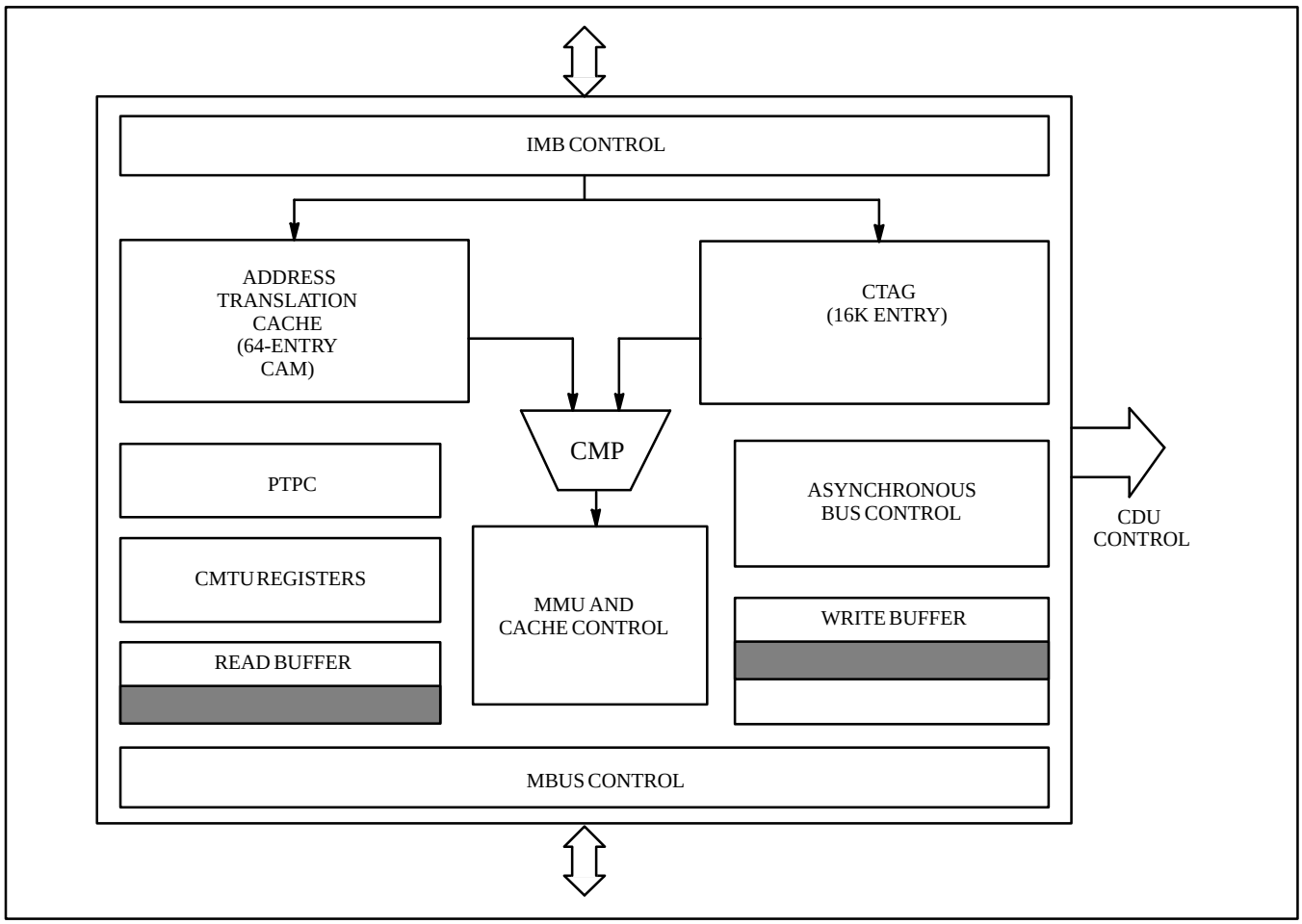


Figure 3. RT626 CMTU Block Diagram

Cache Controller The CMTUs cache controller supports two modes of caching: write-through with no write allocate and copy-back with write allocate. The cache is "virtually indexed" and "physically tagged."

In 1-Mbyte secondary cache versions, the cache is organized as 16384 lines with two sub-blocks, each of which is 32 bytes. Intra-module address bits IMA[19:6] select the cache line, IMA[5] selects the sub-block, and IMA[4:3] select the 64-bit word of the cache line. In 512-Kbyte secondary cache versions, only one sub-block is populated, and IMA[18:5] select the cache line and IMA[4:3] select the 64-bit word of the cache line.

The 16384 cache tag entries in the RT626 are virtual address indexed. From the processor side, the virtual address on the intramodule bus is used to select a cache line entry and its corresponding cache tag entry. The translated physical address is then compared against the physical address in the selected cache tag entry to determine if the required data resides in the cache.

From the MBus side, the superset virtual address bits are concatenated with physical address bits [11:5] to select a cache line entry and its corresponding cache tag entry. The physical address on MBus is then compared against the physical address in the selected cache tag entry to determine if the required data resides in the cache.

A 64-byte write buffer and a 32-byte read buffer are provided in the RT626 to fully buffer the transfer of cache lines. This feature allows the CMTU to simultaneously read a cache line from main memory as it flushes a modified cache line from the cache.

MBus. The CMTU supports the SPARC MBus interface standard and the SPARC MBus Level 2 cache coherency protocol. It supports data transfers in transaction sizes of 1, 2, 4, 8, or 32 bytes. These data transfers are performed in either burst or non-burst mode, depending upon the size. Data transactions larger than 8 bytes are transferred in burst mode. Bus mastership is granted and controlled by an external bus arbiter.

The CMTU also supports the MBus Module Identifier feature of the MBus, in which it accepts the Module Identifier input from the MBus and embeds it in the MBus address phase of all MBus transactions initiated by the CMTU.

Cache Data Units (RT628)

The RT628 is organized as four arrays of 32-Kbytes each. It contains a one-deep write buffer pipeline, byte write logic,

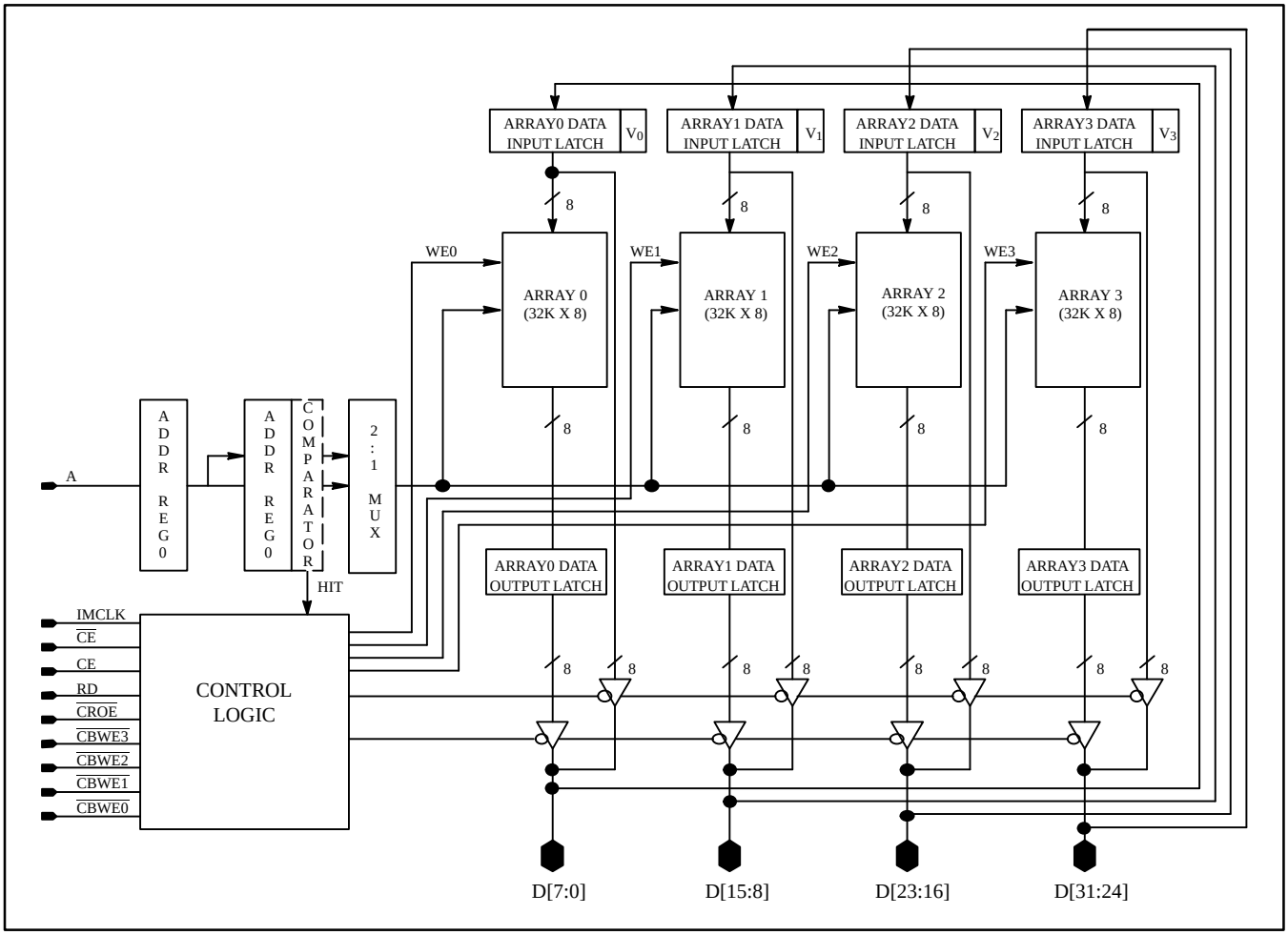


Figure 4. RT628 Block Diagram

registered inputs, data-in and data-out latches, and data forwarding logic for the write buffer.

Writing into the RAM core is delayed until the next write access. To allow data forwarding, the CDU incorporates a comparator to compare the address of the write-buffer to the incoming read address. If a match occurs, data is forwarded directly from the write-buffer to satisfy the current read cycle.

For a more complete description of the individual SPARC components used in the RT6224K, please refer to the *ROSS SPARC RISC User's Guide* and *Appendix B*.

Module Design

Advanced Packaging Technology

The RT6224K employs multi-die packaging (MDP) technology to facilitate higher clock frequencies and reliable operation. Each MDP component contains a complete hyperSPARC CPU chipset. MDP technology improves electrical characteristics by reducing electrical parasitics, allowing multiple discrete chips to function as a single monolithic die.

Clock Distribution

The RT6224K uses two MBus clock signals (MCLK[0] and MCLK[1]) as defined in the MBus Specification. In order to minimize clock skew, traces have been carefully routed. All clock lines are routed on inner layers of the module PCB, and their lengths and impedances are matched. The MBus clock lines have diode termination to reduce signal undershoot and overshoot, and all intramodule clock lines use a parallel resistive termination of 60Ω.

MBus Connector (Module)

The RT6224K interface is via the 100-pin SPARC MBus connector, which is a two-row male connector with 0.050" spacing (AMP part number 121354-4 or Fujitsu part number FCN-264P100-G/C). The connector is a controlled impedance-type (50Ω ±10%) based on a microstrip configuration that provides a controlled characteristic impedance plus very low inductance and capacitance. Separate power and ground blades are provided for isolation to prevent noise transference. *Table 1* details the RT6224K standard connector pinout. This MBus connector supports Level 2 MBus.

Mating MBus Connector (System Interface Board)

The module connects to the system interface through the standard MBus female connector (vertical receptacle assembly, AMP part number 121340-4 or Fujitsu FCN-264J100-G/0).

Reset and Interrupt Signals

A power-on reset signal is generated to the module from the MBus via the $\overline{\text{RSTIN}}$ signal. Level sensitive interrupts (15 max) are generated to the RT620D via the MIRL0[3:0] lines from the MBus. A value of 0000b means that there is no interrupt, while a value of 1111b means an NMI (Non-Maskable Interrupt) is being asserted. IRL values between 1 and 14 represent interrupt requests that can be masked by the processor.

MBus Request and Grant Signals

One set of request and grant signals ($\overline{\text{MBR[0]}}$ and $\overline{\text{MBG[0]}}$) are generated to/from the RT6224K modules to arbitration logic on the motherboard.

MBus SCAN Test Feature

The RT6224K module also supports the Boundary SCAN test feature of the MBus. For more details on the SCAN test, please refer to the *ROSS SPARC RISC User's Guide* and *SPARC MBus Interface Specification*.

MID Lines

MID[0] is tied to ground.

Table 1. MBus Connector Pinout [1]

Pin #	Signal Name	Blade	Pin #	Signal Name
1	TDI	Blade #1	2	TMS
3	TDO	Ground	4	$\overline{\text{TRST}}$
5	TCLK		6	MIRL0[1]
7	MIRL0[0]	Ground	8	MIRL0[3]
9	MIRL0[2]		10	RES
11	MAD[0]	Ground	12	MAD[1]
13	MAD[2]		14	MAD[3]
15	MAD[4]	Ground	16	MAD[5]
17	MAD[6]		18	MAD[7]
19	MAD[8]		20	MAD[9]
21	MAD[10]	Blade #2	22	MAD[11]
23	MAD[12]	+5V	24	MAD[13]
25	MAD[14]		26	MAD[15]
27	MAD[16]	+5V	28	MAD[17]
29	MAD[18]		30	MAD[19]
31	MAD[20]	+5V	32	MAD[21]
33	MAD[22]		34	MAD[23]
35	MAD[24]	+5V	36	MAD[25]
37	MAD[26]		38	MAD[27]
39	MAD[28]		40	MAD[29]
41	MAD[30]	Blade #3	42	MAD[31]
43	$\overline{\text{MBR[0]}}$	Ground	44	$\overline{\text{MSH}}$
45	$\overline{\text{MBG[0]}}$		46	$\overline{\text{MIH}}$
47	MCLK[0]	Ground	48	$\overline{\text{MRTY}}$
49	MCLK[1]		50	$\overline{\text{MRDY}}$
51	MCLK[2]	Ground	52	$\overline{\text{MERR}}$
53	MCLK[3]		54	$\overline{\text{MAS}}$
55	RES	Ground	56	$\overline{\text{MBB}}$
57	RES		58	RSVD0
59	MAD[32]		60	MAD[33]
61	MAD[34]	Blade #4	62	MAD[35]
63	MAD[36]	+5V	64	MAD[37]
65	MAD[38]		66	MAD[39]
67	MAD[40]	+5V	68	MAD[41]
69	MAD[42]		70	MAD[43]
71	MAD[44]	+5V	72	MAD[45]
73	MAD[46]		74	MAD[47]
75	MAD[48]	+5V	76	MAD[49]
77	MAD[50]		78	MAD[51]
79	MAD[52]		80	MAD[53]
81	MAD[54]	Blade #5	82	MAD[55]
83	MAD[56]	Ground	84	MAD[57]
85	MAD[58]		86	MAD[59]
87	MAD[60]	Ground	88	MAD[61]
89	MAD[62]		90	MAD[63]
91	RSVD1	Ground	92	RES
93	RES		94	RES
95	RES	Ground	96	$\overline{\text{AERR}}$
97	$\overline{\text{RSTIN}}$		98	MID[1]
99	MID[2]		100	MID[3]

Notes:

1. RES and RSVD pins are not used in the RT6224K but reserved for other MBus module upgrades. See the System Design Considerations section for the assignment of these reserved pins per the SPARC MBus Specification.

Absolute Maximum Ratings [2] (Provided as guidelines; not tested.)

Parameter	Description		Rating	Units
V_{CC}	Supply Voltage Range		–0.5 to +7.0	V
P_D	Maximum Power Consumption	RT6224K–180/512		W
		RT6224K–180/1024		W
		RT6224K–200/512		W
		RT6224K–200/1024		W
I_{CC}	Maximum Supply Current	RT6224K–180/512, V_{CC} = 5.0V		W
		RT6224K–180/512, V_{CC} = 5.0V		W
		RT6224K–200/1024, V_{CC} = 5.0V		W
		RT6224K–200/1024, V_{CC} = 5.0V		W
V_I	Input Voltage Range		–0.3 to +7.0	V
T_{STG}	Storage Temperature		–20 to +75	°C
RH_{STG}	Storage Relative Humidity [3]		5 to 80	%

Recommended Operating Conditions [4]

Parameter	Description		Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage		4.75	5.00	5.25	V
V_{IH}	Input HIGH Voltage	5V signals	2.0		V_{CC}	V
V_{IL}	Input LOW Voltage		–0.5		0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 2.0 mA	2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
I_{IZ}	Input Leakage Current (non-clock pins)	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$	–10		+10	µA
I_{CLKZ}	Input Leakage Current (clock pins)	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$	–40		+40	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$	–15		+15	µA
I_{SC}	Output Short Circuit Current [5]	V_{CC} = Max., V_{OUT} = 0V	– 30		– 350	mA
T_A	Operating Ambient Air Temperature [6]		0		50	°C
RH_{OP}	Operating Relative Humidity [3]		5		95	%

Capacitance [7]

Parameter	Description		Max.	Units
C_{IN}	Input Capacitance	V_{CC} = 5.0V T_A = 25°C f = 1 MHz	18	pF
C_{OUT}	Output Capacitance		20	pF
C_{IO}	Input/Output Capacitance		23	pF
C_{INCLK}	Clock Input Capacitance		28	pF

Notes:

2. All power and ground pins must be connected to other pins of the same type before any power is applied to the RT6224K. At least three clock cycles must be applied to set up the internal chip drivers properly.
3. Non-condensing. Maximum rate of change of 30% per hour.
4. Recommended use of this module does not include ‘‘hot-socketing” or ‘‘live-insertion” (i.e., it is not recommended that the RT6224K be placed in the MBus socket with the power supply on).
5. Not more than one output should be tested at one time. Duration of the short circuit should not be more than one second.
6. See Appendix A. hyperSPARC Module Thermal Specifications. This temperature should not be exceeded when the device is consuming maximum power with 300 linear feet per minute (LFM) of airflow at sea level.
7. Tested initially and after any design or process changes that may affect these parameters.

AC Electrical Characteristics Over the Operating Range [8,9]

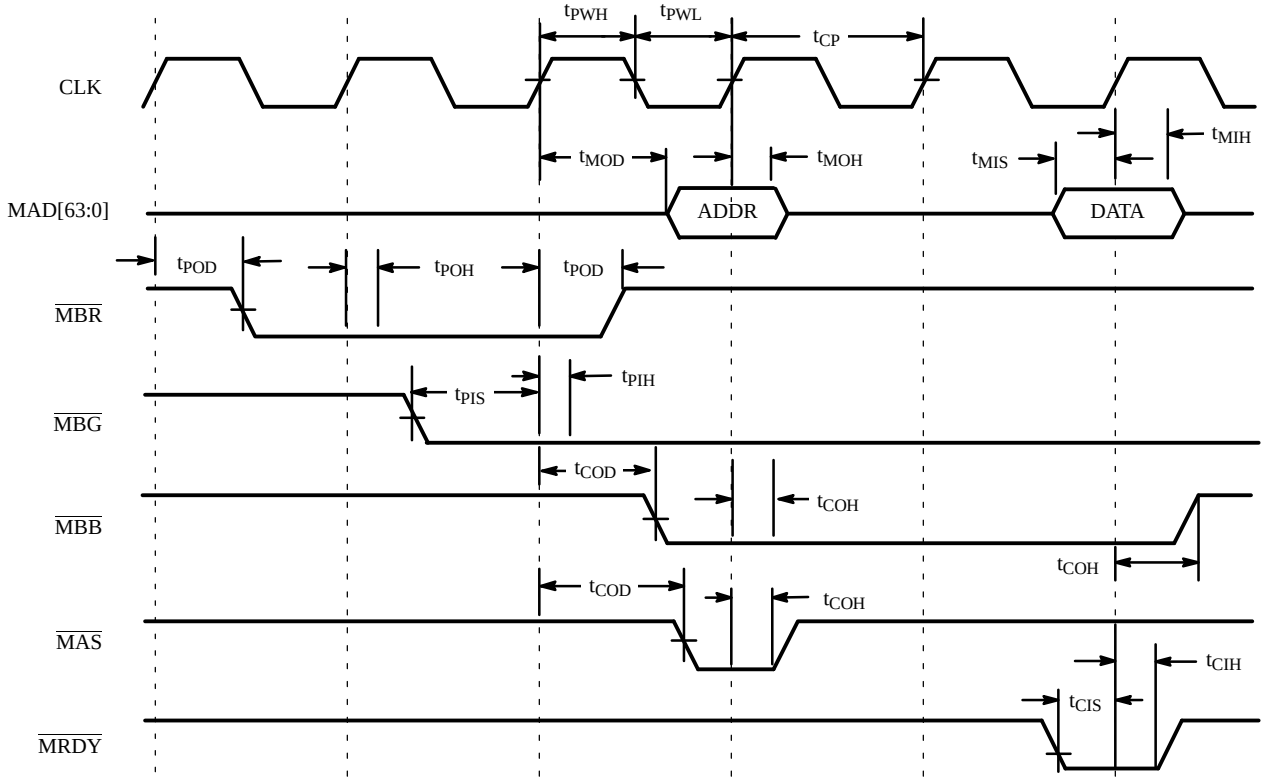
Param	Description	50 MHz MBus		66 MHz MBus		Unit
		Min.	Max.	Min.	Max.	
Synchronous signals [10]						
t_{CP}	MBus Clock period	20		15		ns
t_{PWH}	MBus Clock High period	9.2		6.9		ns
t_{PWL}	MBus Clock Low period	9.2		6.9		ns
t_{CSR}	MBus Clock Slew Rate (between 0.8V and 2.0V)	0.8		0.8		$V/_{ns}$
t_{SKU}	MBus Clock Skew[11]		1.0		0.5	ns
t_{MOD}	MAD(63:0) Output Delay		13.5		10.0	ns
t_{MOH}	MAD(63:0) Output Valid	4.0		2.5		ns
t_{MIS}	MAD(63:0) Input Set-Up	3.5		3.5		ns
t_{MIH}	MAD(63:0) Input Hold	2.0		2.0		ns
t_{COD}	MBus Bused Control Output Delay		13.5		9.5	ns
t_{COH}	MBus Bused Control Output Valid	4.0		2.5		ns
t_{CIS}	MBus Bused Control Input Set-Up	5.5		3.5		ns
t_{CIH}	MBus Bused Control Input Hold	2.0		2.0		ns
t_{POD}	MBus Point-to-Point Control Output Delay		13.5		9.5	ns
t_{POH}	MBus Point-to-Point Control Output Valid	4.0		2.5		ns
t_{PIS}	MBus Point-to-Point Control Input Set-Up	5.5		3.5		ns
t_{PIH}	MBus Point-to-Point Control Input Hold	2.0		2.0		ns
Asynchronous Signals						
t_{RST}	MBus Reset Duration [12]	100		100		ms

Notes:

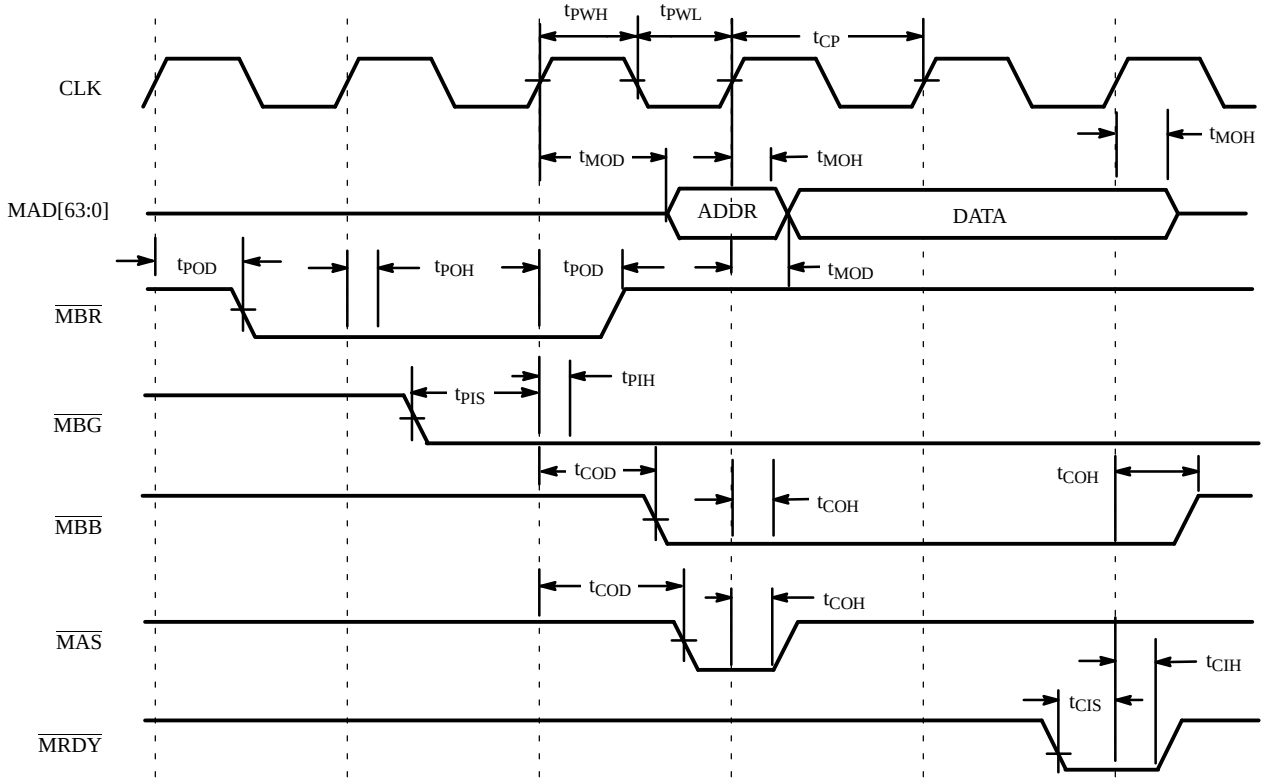
8. Test conditions assume signal transition times of 3 ns or less, a timing reference level of 1.5V, input levels of 0 to 3.0V, and output loading of 80-pF capacitance, not including the module itself (with the exception of MBus point-to-point control signals, tested with an output loading of 40 pF).
9. All measurements made at MBus connector.
10. All timing parameters are relative to one of the two processors (e.g., t_{MOD} is guaranteed relative to MCLK[0]).
11. Measured between any two MCLK signals.
12. This is the minimum time for which $\overline{\text{RSTIN}}$ must be asserted after both high and low power supply voltages are stable.

MBus Timing Diagrams

Single Read Transaction



Single Write Transaction



System Design Considerations

The RT6224K implements a subset of all possible MBus signals. Signals that are optional and/or specifically for multiprocessor modules may not be supported. The MBus connector, per the SPARC MBus Specification, defines the assignments listed in *Table 2* for pins reserved on the RT6224K. Although these signals are not used on the RT6224K, systems designers should be aware of these assignments to preserve compatibility with other MBus modules.

Table 2. Pins Reserved on RT6224K

Pin #	Signal Name
10	$\overline{\text{INTOUT}}$
51	MCLK2
53	MCLK3
55	$\overline{\text{MBR[1]}}$
57	$\overline{\text{MBG[1]}}$
58*	RSVD0
91*	RSVD1
92	MIRL1[0]
93	MIRL1[1]
94	MIRL1[2]
95	MIRL1[3]

* Non-floating. Reserved for ROSS internal use only. These signals should not be driven.

All MAD, bused control, and point to point control signals use 8-mA drivers. The $\overline{\text{MSH}}$ and $\overline{\text{AERR}}$ signals use open-drain drivers.

10-Kohm pull up resistors are required on $\overline{\text{MAS}}$, $\overline{\text{MRDY}}$, $\overline{\text{MRTY}}$, $\overline{\text{MERR}}$, $\overline{\text{MBB}}$, and $\overline{\text{MIH}}$. A 1.5-Kohm pull up resistor is recommended on $\overline{\text{AERR}}$. A 619 ohm pull up resistor is recommended on $\overline{\text{MSH}}$. MAD signals require holding amplifiers.

In order to assure that all module scan circuitry is initialized to the normal operating state on reset, the following is recommended for the MBus scan signals. TDI and TMS should be pulled up to 5V with 10KΩ resistors. TCLK must toggle at least 3 full cycles while $\overline{\text{TRST}}$ is asserted in order to reset all scan circuitry. $\overline{\text{RSTIN}}$ may be driven by the module when the module is in scan mode, so it should be buffered from the rest of the system. These requirements may be met by connecting each signal as shown in *Figure 5*. The RT6224K uses MCLK[0] to clock the processor and MCLK[1] for test.

As the frequency of operation increases, transmission line effects play a bigger role. Care must be taken to keep skew between any two clock signals at the MBus connector within the specifications given in the Synchronous Signals table in the AC Characteristics section. MBus signal lines must be routed carefully to minimize crosstalk and interference. A thorough SPICE analysis of the motherboard design is recommended.

Use of HH Smith #4387 (3/4” length by 1/4” OD) stand-offs or equivalent is recommended on the motherboard to support the module and prevent damage to the connector.

If mounting screws are used, nylon screws are recommended to prevent over-torquing and damage to the PCB.

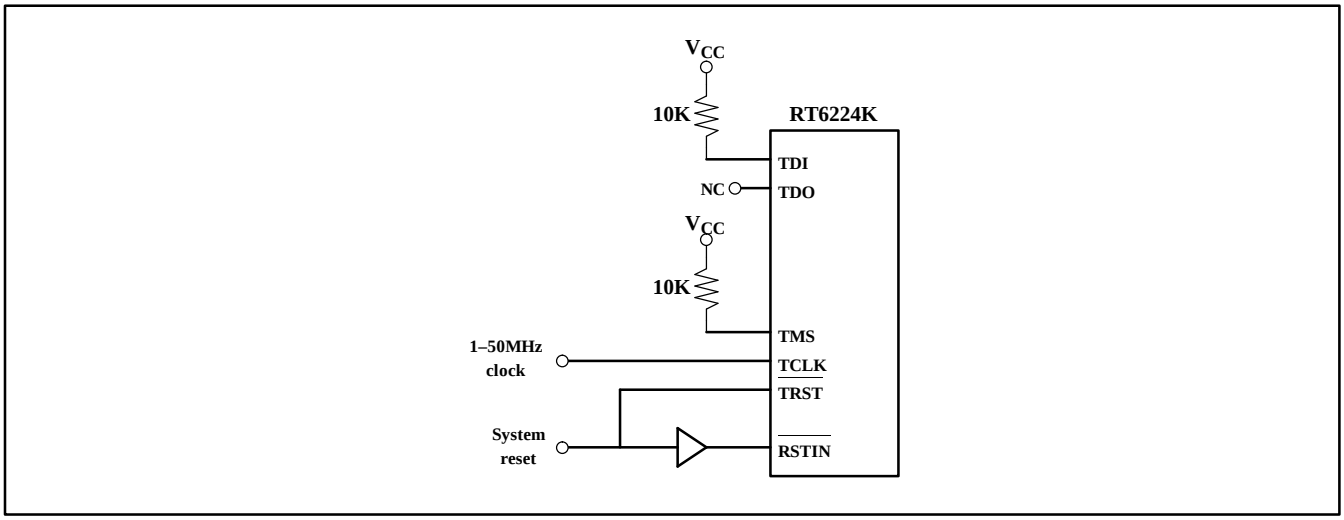


Figure 5. Scan Pin Connections

RT6224K Mechanical Drawing [13,14, 15]

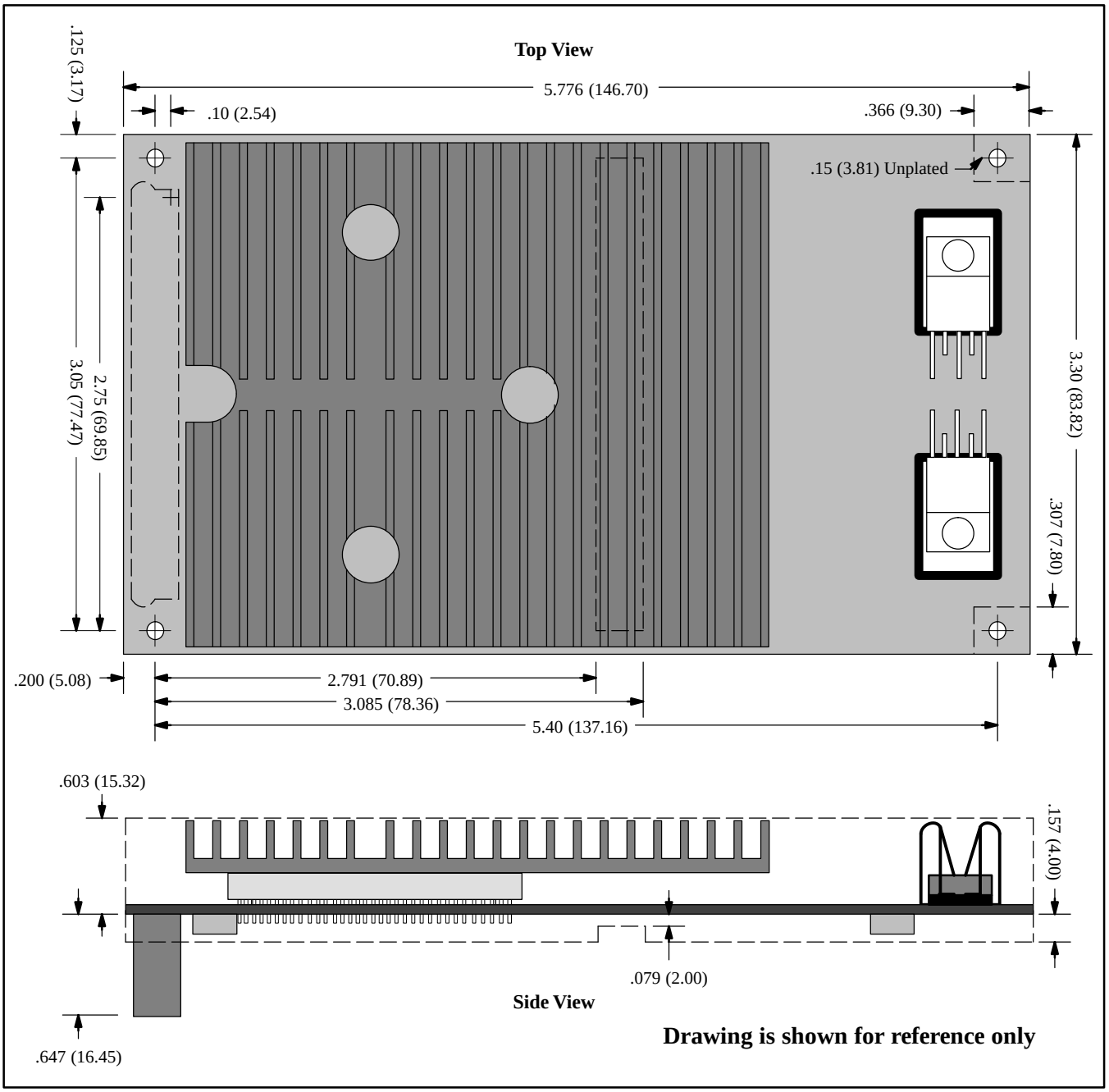


Figure 6. RT6224K Mechanical Dimensions

Notes:

13. Drawing is for reference only. Appearance of module is subject to change without notice.
14. Drawing is not to scale. All dimensions are in inches (mm).
15. To ensure compliance with all future MBus modules, systems developers should design to the MBus module envelope per the SPARC MBus Specification.

RT6224K Module Label Specification

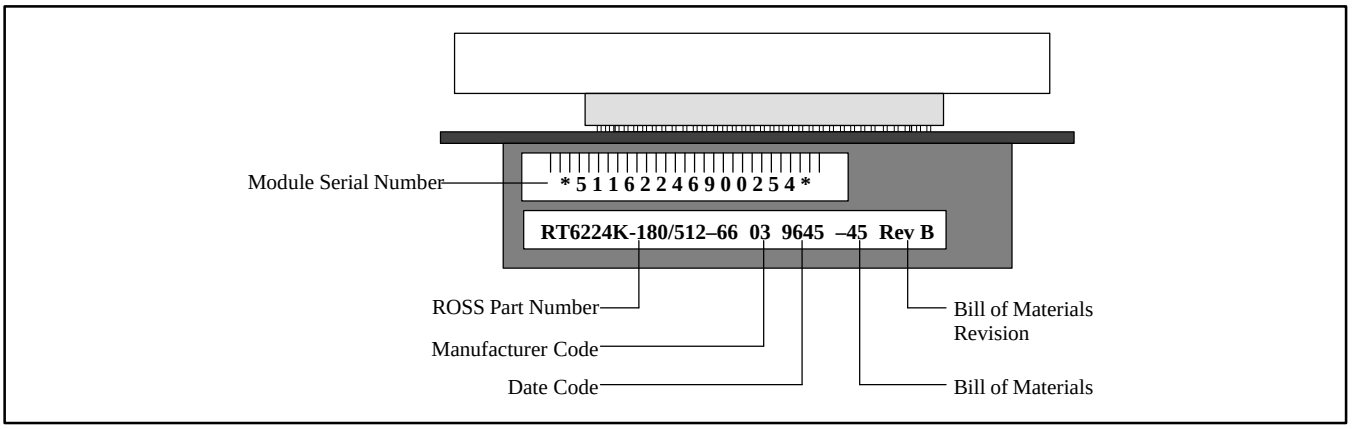


Figure 7. RT6224K Module Labeling

Appendix A. hyperSPARC Module Thermal Specifications

Ambient Temperature

Ambient temperatures as high as 50°C are acceptable for the RT6224K provided airflow is 300 linear feet per minute (LFM) minimum through the heatsink fins at all locations indicated in *Figure 8*. In this context, ambient temperature is defined as the air temperature in immediate proximity to the module.

Module airflow measurements must be taken with the anemometer probe in front of the fins, approximately 1/2" above the top of the PCB at the indicated locations. The airflow must meet the minimum requirements at all locations indicated in *Figure 8*. When taking airflow measurements the module should be installed in a system that is configured in the same fashion as the actual final production system (for example, all external covers and panels should be installed, and any internal ducting or baffling should also be installed).

Ambient temperature should be measured within the system, as it enters the fins of the heatsinks on the module.

For further information regarding thermal measurements contact ROSS Applications Engineering.

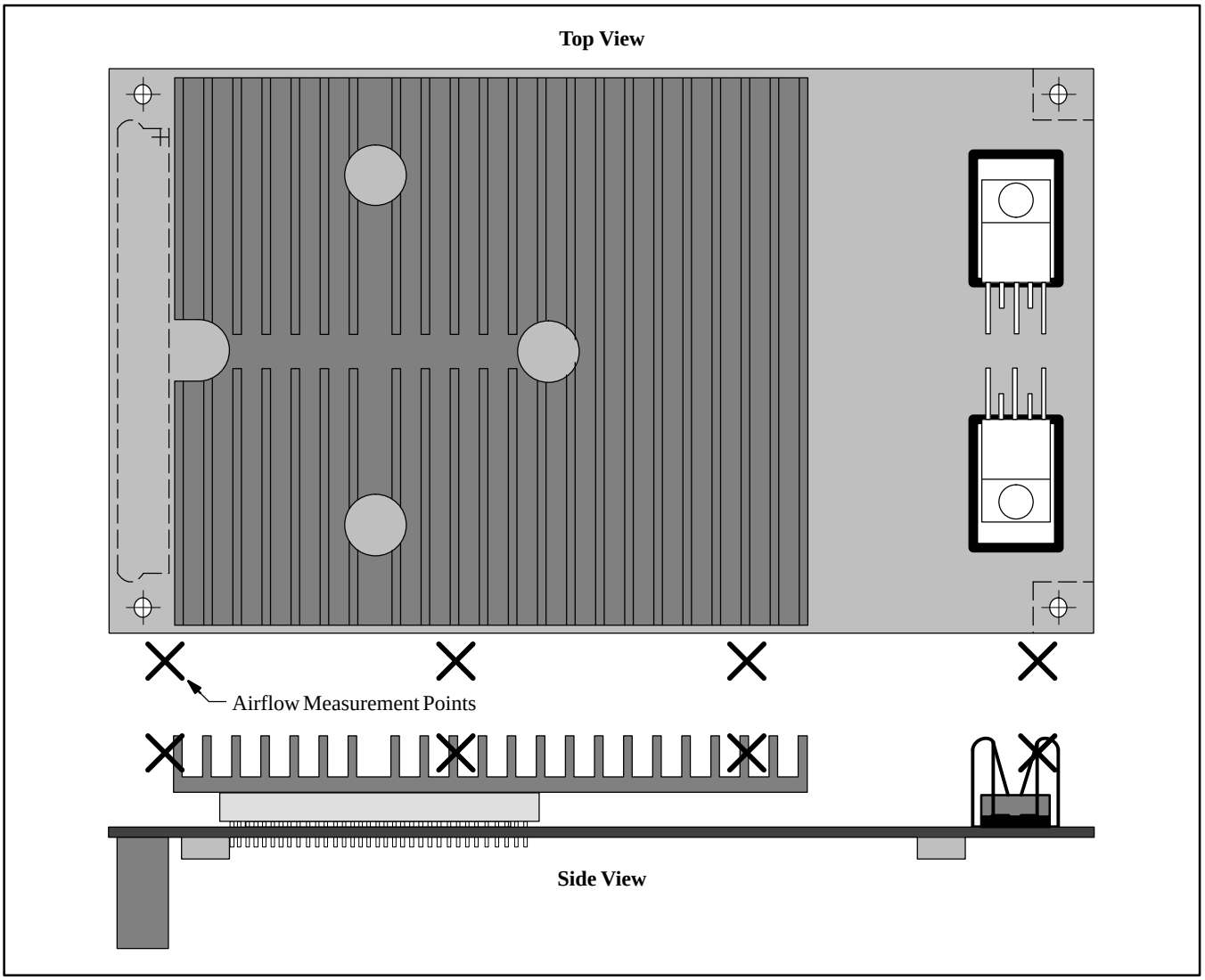


Figure 8. RT6224K Airflow Measurement

Appendix B. Impact of Cache Size on System Design.

Hardware Differences

hyperSPARC modules with 256-Kbytes of secondary cache utilize the RT625 Cache Controller, Memory Management, and Tag Unit (CMTU) and four RT627 Cache Data Units (CDUs). Modules with 512-Kbytes or 1-Mbytes of secondary cache utilize the RT626 CMTU and either four or eight RT628 CDUs.

CDU. The RT628 is functionally equivalent to the RT627 described in the *ROSS SPARC RISC User's Guide* except that the RT628 is based on a 32-Kbyte x 32-bit SRAM core.

CMTU. The RT626 is functionally equivalent to the RT625 described in the *ROSS SPARC RISC User's Guide*, with the few exceptions outlined below.

The RT626 supports two cache sizes: 512-Kbyte and 1-Mbyte. Cache lines are directly addressed by the RT620 CPU with the Intra-Module Address Bus (IMA[31:0]). The 512-Kbyte cache is organized into 16384 lines of 32 bytes each. IMA[18:5] select the cache line, and IMA[4:3] select the 64-bit word of the cache line, as illustrated in *Figure 9*. The 1-Mbyte cache is organized into 16384 lines with two sub-blocks, each sub-block being 32 bytes. Address bits IMA[19:6] select the cache line, address bit IMA[5] selects the sub-block, and address bits IMA[4:3] select the 64-bit word of the cache line, as illustrated in *Figure 10*.

The RT626 cache tag array consists of 16384 direct-mapped physical address cache tag entries. The layout of the cache tag entries is identical to that of the RT625. The 16384 CTAG entries are virtual address indexed.

From the processor side, the cache line select field, IMA[18:5] in the case of the 512-Kbyte cache or IMA[19:6] in the case of the 1-Mbyte cache, is used to select a cache line entry and its corresponding cache tag entry.

From the MBus side, the index field for CTAG, as supplied by the MBus, is formed by concatenating the superset virtual address bits [18:12] (MAD[52:46]) in the case of 512-Kbyte cache or [19:12] (MAD[53:46]) in the case of 1-Mbyte cache with physical address bits [11:5] (MAD[11:5]) as shown in *Figure 9* and *10*.

The System Control Register (SCR) is the same in both the RT625 and RT626, except for the *Cache Size* bit (SCR[12]). In the RT626, CS=0 indicates a 512-Kbyte cache subsystem, and CS=1 indicates a 1-Mbyte cache subsystem.

RT626 CTAG entries may be accessed using word LDST Alternate instructions with the cache tag entry address and ASI=0x0E. Each tag entry can be read as a Load single or can be written as a Store single by the RT620. The address mapping for the Cache Tag entries is shown in *Table 3*.

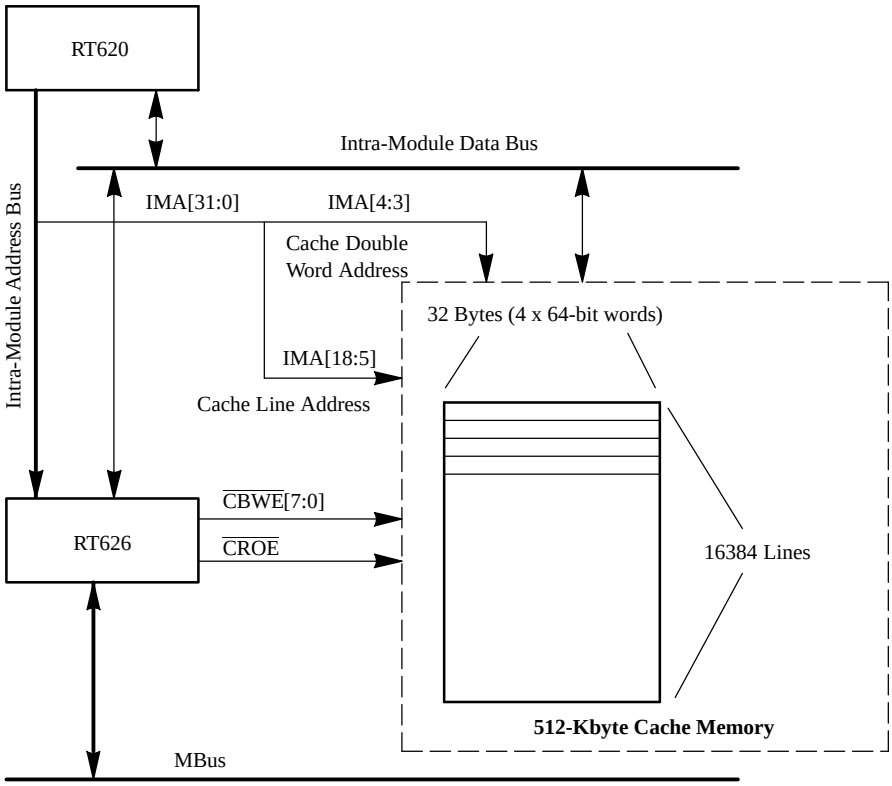


Figure 9. 512-KByte Cache Memory Subsystem

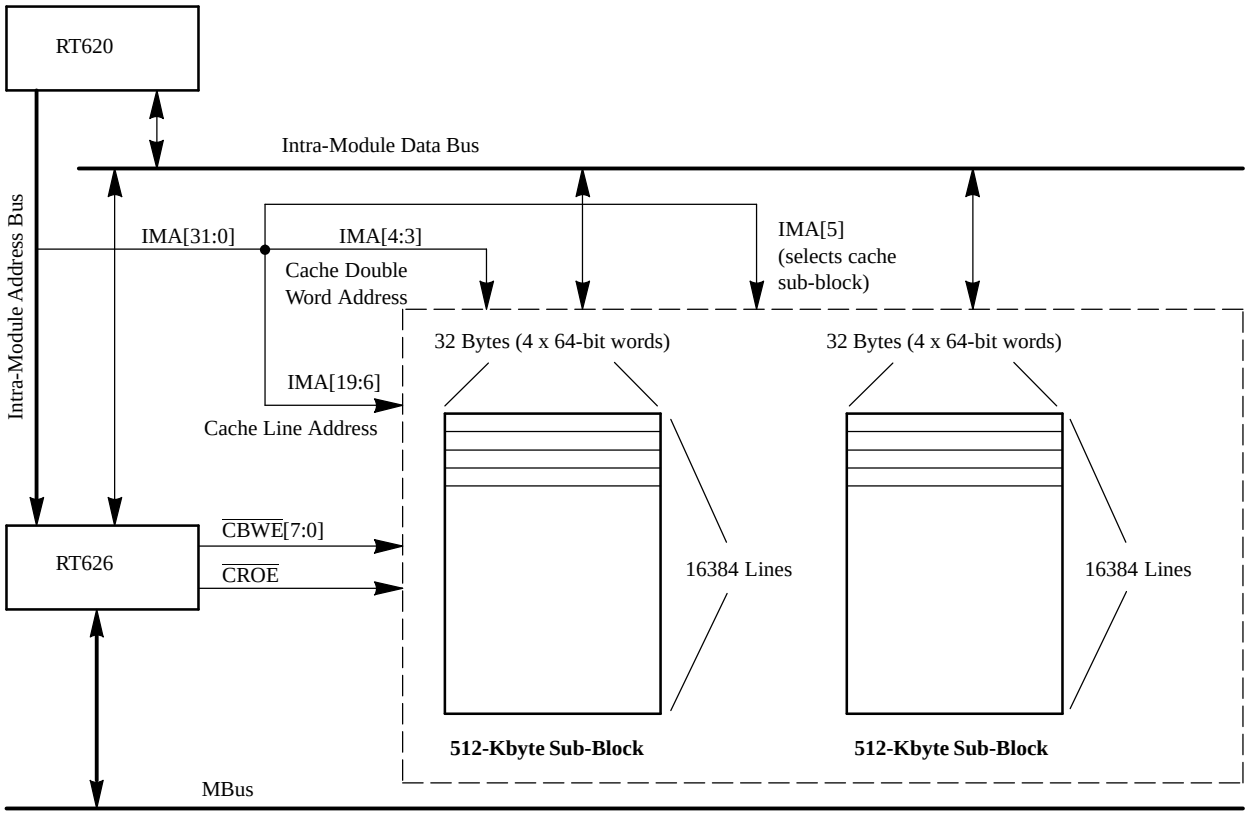


Figure 10. 1-Mbyte Cache Memory Subsystem

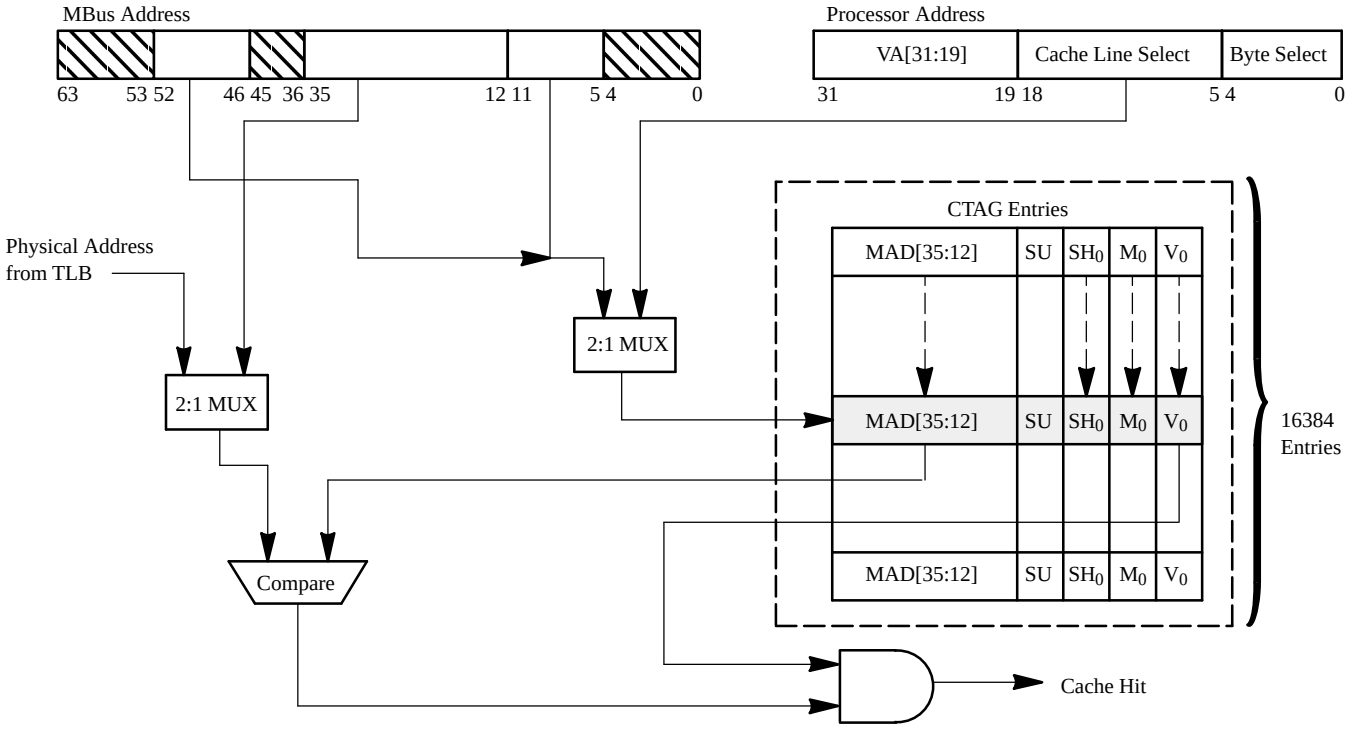


Figure 11. RT626 Cache TAG (CTAG) Comparison (512-Kbyte Cache)

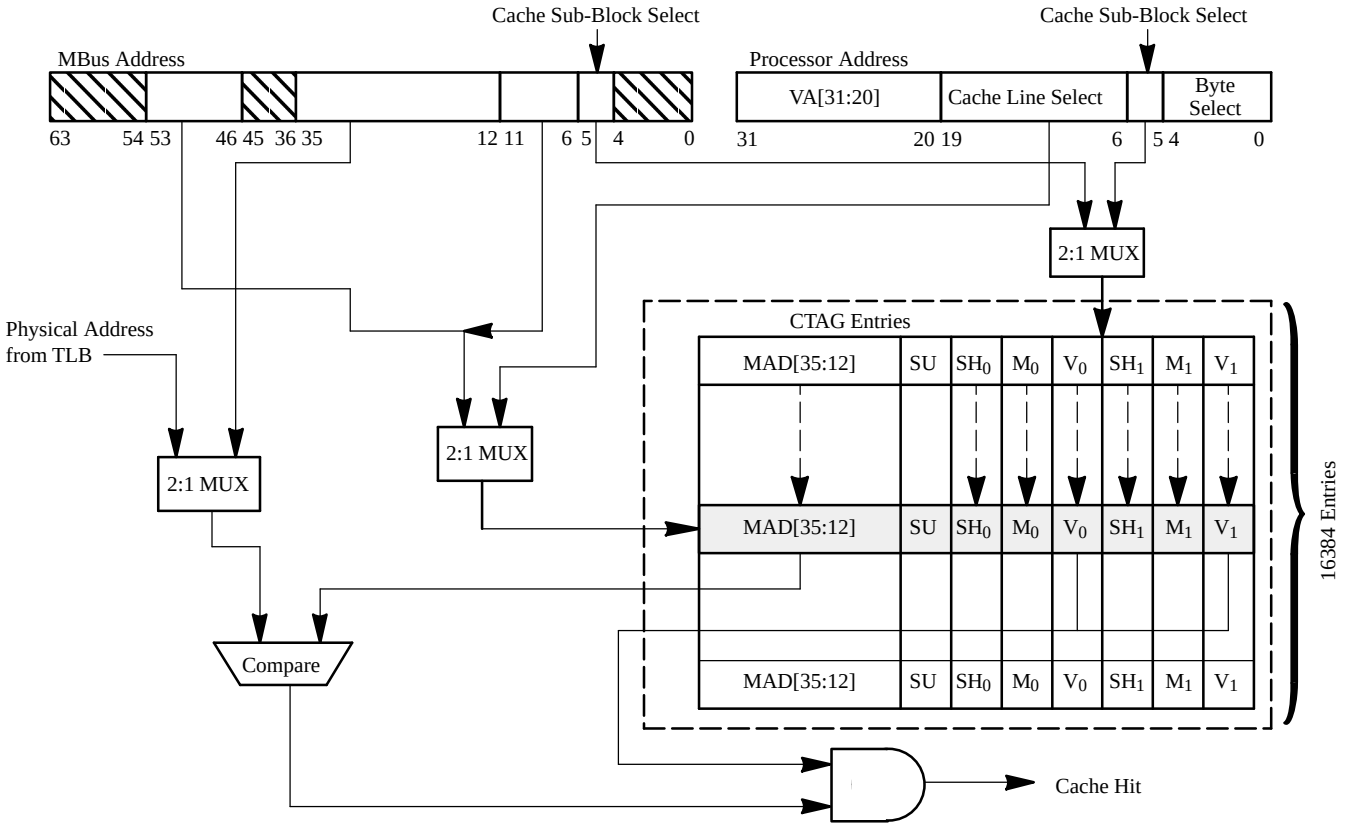


Figure 12. RT626 Cache TAG (CTAG) Comparison (1-Mbyte Cache)

Software Differences

OBP. The Open Boot PROM (OBP) is responsible for determining the size of the cache, setting the *Cache Size* bit in the System Control Register (SCR), and passing cache line size and number of cache lines on to the operating system kernel. The cache size may be hard coded, or it may be determined dynamically by scanning for the largest byte stored using the CACHE DATA ASI (0xF), as shown in the following pseudo-code segment:

```
set   (2*1024*1024), %o0     ! 2-Mbyte cache
sta   %o0, [%o0]ASI_CACHE_DATA
set   (1*1024*1024), %o0     ! 1-Mbyte cache
sta   %o0, [%o0]ASI_CACHE_DATA
set   (512*1024), %o0     ! 512-Kbyte cache
sta   %o0, [%o0]ASI_CACHE_DATA
set   (256*1024), %o0     ! 256-Kbyte cache
sta   %o0, [%o0]ASI_CACHE_DATA
set   (128*1024), %o0     ! 128-Kbyte cache
sta   %o0, [%o0]ASI_CACHE_DATA
lda   [%g0]ASI_CACHE_DATA, %o1
```

The register %o1 will contain the size of the installed cache, since addresses which are larger than the installed cache wrap around to virtual index 0.

When flushing cache lines, a stride of 32-bytes should always be used to assure the primary and secondary caches are both flushed.

Colorado 4 modules are supported by OBPs available from ROSS (Rev 2.25.1H or later). For more information, contact ROSS Applications Engineering.

Operating System. Generally, no operating system modifications should be necessary due to changes in secondary cache size. Solaris 2.4 and earlier, however, contains a bug which limits operation to systems with cache sizes of 256-Kbytes or less. The bug causes a data area to be overwritten when the cache size exceeds 256-Kbytes. In all standard Solaris 2.4 kernels investigated by Sun, the data area overwritten is not used, so the bug is not evident. It may be possible, however, that a non-standard kernel with a different data layout may experience problems. This bug has been corrected in Solaris 2.5 and later. For more information, contact ROSS Applications Engineering.

Table 3. Cache Tag Entry Address Mapping

512-Kbyte		1-Mbyte	
Address	**Cache Tag Entry**	**Address**	**Cache Tag Entry**
0000x H	0	00000x H	0
0002x H	1	00004x H	1
0004x H	2	00008x H	2
0006x H	3	0000cx H	3
•	•	•	•
•	•	•	•
•	•	•	•
7FFEx H	16383	1FFFCx H	16383

(X = Don’t Care)

ROSS TECHNOLOGY, INC.

PRELIMINARY

Colorado 4 RT6224K

Appendix C. hyperSPARC Ordering Information

Ordering Code	CPU Clock Frequency (MHz)	Second-level Cache size	MBus Clock Frequency (MHz)
RT6224K-180/512	180	512K	50
RT6224K-180/512-66	180	512K	66
RT6224K-180/1024	180	1M	50
RT6224K-180/1024-66	180	1M	66
RT6224K-200/512	200	512K	50
RT6224K-200/512-66	200	512K	66
RT6224K-200/1024	200	1M	50
RT6224K-200/1024-66	200	1M	66

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