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wanPTMC-C4T1E1

High-Performance PTMC Communications Module

Hardware Technical Reference, Rev. 1.0, Jan. 24, 2002

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SBE is based in San Ramon, California, and can be reached at 925-355-2000 or online at http://www.sbei.com

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1. About This Manual

This manual is the technical reference for the wanPTMC-C4T1E1 HDLC/SS7 communications module. This manual is intended for hardware and software engineers who are incorporating the wanPTMC-C4T1E1 into a system.

The *wanPTMC-C4T1E1 Technical Reference* includes the following:

- Introduction and background on the wanPTMC-C4T1E1 communications module
- Installation instructions
- Physical characteristics and specifications of the module
- Programming information

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1-1. Documentation Conventions

In this document, the term T1 implies E1 and J1, unless specifically noted otherwise.

The term DS0 is used to mean either one of 24 64Kbps T1/J1 channels, or one of 32 64Kbps E1 channels.

The term “channel” connotes “full duplex channel” unless otherwise specified.

PTMC refers to the PICMG 2.15 PCI Telecom Mezzanine Card standard.

E1 is synonymous with CEPT.

Signal names with a # after the name indicates a low active signal.

Signal names with a / in front of the signal name indicates a low active signal.

The term CPLD refers to Complex Programmable Logic Device.

COMET, or Quad COMET, refers to the PMC-Sierra Quad COMET PM4354.

WORD in terms of addressing refers to 32-bit addressing.

Registers	Register bits are numbered starting with 0. Bit 0 is the least significant and bit 7 is the most significant bit of a byte. Unless otherwise noted, register bits that are identified as “unused” do not affect the function of the register, and, if read, yield no information.
Signals	When referring to a signal function in text, signal names do not indicate polarity, and the / is not used. Occasionally a signal name may be followed by an asterisk (*), a pound sign (#), a **#** after the name, or with a / in front of the signal name. These are valid ways of indicating active low signals.
Code	`Code is in New Courier typeface.`

Throughout this manual you may find notes, cautions, and warnings that emphasize certain portions of the material presented in the text.

Caution! Points out possible ways the product can be damaged if proper precautions are not followed.

Warning! States potential dangers to the user if a procedure is not properly followed.

Note: Provides information that is important to the surrounding text.

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1-2. Related Documents

The following references can be used for background or additional information about this product. References are for informational purposes only and do not express or imply wanPTMC-C4T1E1 product features and functions.

- Conexant CN8478/4/2A MUSYCC data sheet (document #100660E).
- PMC-Sierra Quad COMET PM4354 data sheet.
- Lucent Ambassador T8100A and T8105 data sheet.
- PICMG 2.15 R1.0, CompactPCI Telecom Mezzanine Specification, April 3, 2001, PICMG.
- PCI Special Interest Group, “PCI Local Bus Specification”, Revision 2.1, June 1995.
- IEEE 1386-2001, Standard for a Common Mezzanine Card (CMC), Aug. 21, 2001, IEEE.
- IEEE 1386.1-2001, Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC), Aug. 16, 2001, IEEE.
- PICMG 2.0 R3.0, CompactPCI Specification, Oct. 1, 1999, PICMG.
- PICMG 2.3 R1.0, PMC on CompactPCI Specification, Aug. 7, 1998, PICMG.
- PICMG 2.5 R1.0, CompactPCI Telephony Specification, 1997, PICMG.
- H.110 Hardware Compatibility Specification: CT Bus, Revision 1.0, ECTF.
- GR-63-CORE, Network Equipment-Building Systems (NEBS) Requirements: Physical Protection, Issue 1, October 1995.
- GR –1089-CORE, Electromagnetic Compatibility and Electrical Safety – Generic Criteria for Network Telecommunications Equipment, Issue 2, December 1997, Bellcore.
- GR-78-CORE, Generic Requirements for the Physical Design and Manufacture of Telecommunications Products and Equipment, Issue 1, September 1997, Bellcore.
- G.703, “Physical/electrical characteristics of hierarchical digital interfaces”, October 1998, ITU-T.
- G.704, “Synchronous Frame Structures used at Primary and Secondary Hierarchical Levels”, October 1998, ITU-T.
- Serial EEPROM Exel Microelectronics XL93LC46B data sheet.

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2. Introduction

2-1. Product Description and Functional Characteristics

The wanPTMC-C4T1E1 is an HDLC/SS7 communications module. The board is in the form of a standard PTMC module and has four shielded RJ48c connectors at the front bezel. It uses the Conexant CN8474A Multi-channel Synchronous Communications Controller (MUSYCC) as the protocol-processing engine. This component supports up to 128 DS0 channels. Its primary function is to translate data between the PTMC CT-Bus, the host PCI bus, and its own T1/E1/J1 ports.

Data can be processed for up to 128 full duplex standard DS0s, hyperchannels, and subchannels in HDLC, SS7, or transparent modes.

The PCI interface conforms to the PCI 2.1 specification. It transfers 32 bits of data at up to 33MHz. The board is capable of 3.3V signalling and is 5.0V tolerant.

The Lucent T8105 H.110 Interface and Time Slot Interchanger are used to interface to the PTMC CT-Bus connections. The MUSYCC and COMET TDM busses are connected to the T8105, whose H.110 bus is connected to Pn3 of the wanPTMC-C4T1E1. The T8105 also provides time slot interchange and time slot assignment functions.

The T1/E1/J1 interface is presented with shielded RJ48C connectors located on the front panel of the wanPTMC-C4T1E1 module. A software selectable option allows the T1/E1/J1 interfaces to be routed to connector Pn4 for rear I/O support. The board uses the PMC-Sierra Quad COMET T1/E1 framer, which allows software to select between T1, E1, and some J1 modes of operation, with programmable line buildout.

The board supports a software selectable transmit clock, with four choices: a recovered receive clock, the CT-Bus NETREF clocks, or one of the onboard oscillators (1.544 or 2.048MHz).

The wanPTMC-C4T1E1 can receive a Central Office clock source for data synchronization. Any one of the input ports may be used for this purpose and clock selection is under software control. The T1/E1 interface supports local oscillator clocking for diagnostics and external clock failure. If the external clock fails, the framers revert to the local oscillator clock until the external clock reference is restored. Accuracy of the onboard oscillators is +/- 50 PPM tolerance.

There is an onboard DSU/CSU, with full secondary surge protection, for each T1/E1 port.

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The wanPTMC-C4T1E1 board employs a serial EEPROM used to store an electronically accessible serial number that is applied during the manufacturing process.

2-2. Unpacking Instructions

1. If the carton is damaged when you receive it, request that the carrier's agent be present when you unpack and inspect the equipment.
2. After unpacking, verify that all items listed in the packing list are present.
3. Inspect the equipment for shipping damage.
4. Save all packing material for storage or return shipment of the equipment.
5. For repairs or replacement of equipment damaged during shipment, contact SBE, Inc. to obtain a Return Materials Authorization (RMA) number and further shipping instructions. See Section 3-9.

2-3. Handling Procedures

The wanPTMC-C4T1E1 module uses CMOS components that can be easily damaged by static electrical discharge. To avoid damage, familiarize yourself with electrostatic discharge (ESD) procedures, which include the following precautions:

Caution! The module should be handled only by trained service personnel at an approved ESD workstation.

- Refer to ANSI/IPC-A-610 developed by the Institute for Interconnecting and Packaging Electronic Circuits (IPC).

Caution! DO NOT insert the module onto or remove it from the host board while power is applied.

- Keep the module in a sealed conductive plastic bag while in transit.
- When installing the module in the field, ground yourself to the computer before removing the module from the sealed conductive plastic bag (the power plug must be installed on the computer for this to be effective).
- Any equipment used to work on the module must be grounded. Any person handling the module must be grounded.
- Check alignment and polarization of cables and connectors before applying power.
- **Do not** apply external voltages to any devices on the module with power removed from the module.
- **Do not** attempt to straighten any part soldered to the module, as pin breakage or internal damage could occur.

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2-4. Installation

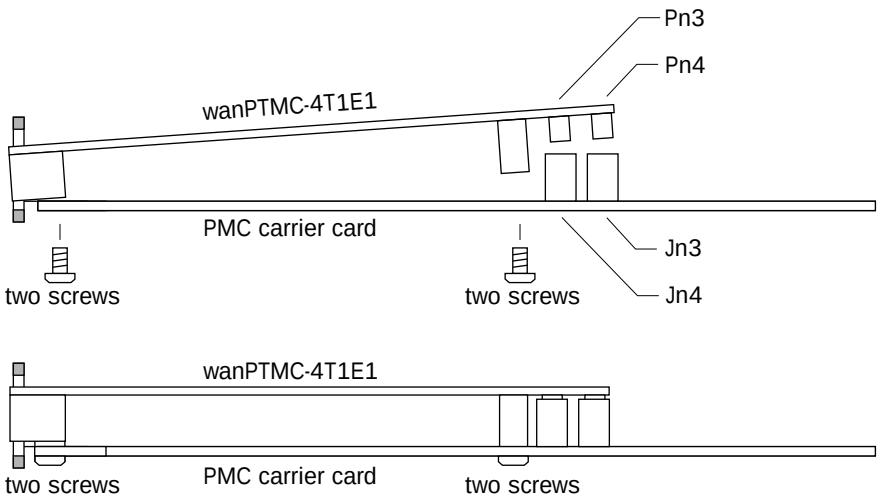
Installing the wanPTMC-C4T1E1 onto a host board

The primary component sides of the wanPTMC-C4T1E1 and the host board face each other when connected. See Figure 2-1.

Caution! Be sure to follow safe ESD procedures when handling electronic hardware.

1. Remove the wanPTMC-C4T1E1 from the protective bag.
2. Press the wanPTMC-C4T1E1 bezel into the cutout in the PMC carrier I/O panel. The gasket around the wanPTMC-C4T1E1 bezel makes a tight fit to ensure an electromagnetic seal. Check that the bezel and gasket are pressed firmly into the carrier I/O panel.
3. Press the wanPTMC-C4T1E1 down onto the carrier so Pn1 through Pn4 plug into Jn1 through Jn4 on the PMC carrier.
4. Install four screws to secure the wanPTMC-C4T1E1 in place.

Figure 2-1 Installing the wanPTMC-C4T1E1



Note: Check the alignment and polarization of connectors before applying any power to the module. Failure to install the module correctly can cause damage to the board.

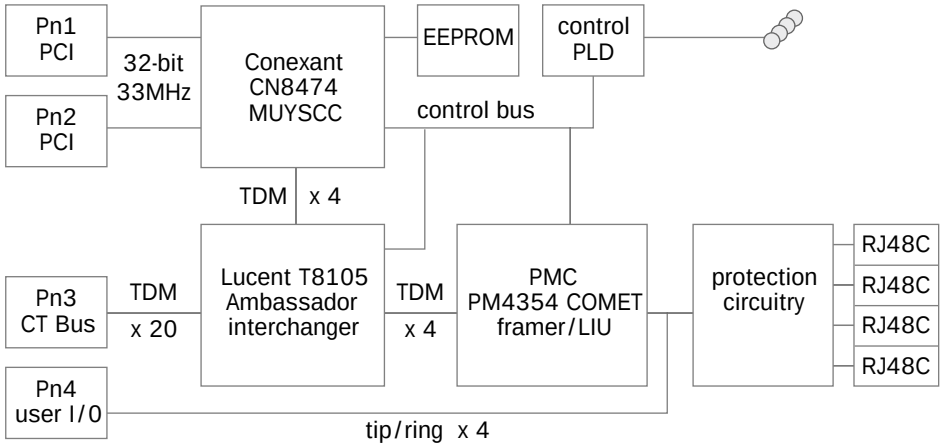
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3. Specifications

This chapter details the physical characteristics and specifications for the wanPTMC-C4T1E1 communications module. Figure 3-1 is a block diagram of the wanPTMC-C4T1E1 functionality.

Figure 3-1 wanPTMC-C4T1E1 functional block diagram



3-1. Communications Controller

Conexant MUSYCC communications controller

The wanPTMC-C4T1E1 uses a Conexant CN8474A Multichannel Synchronous Communications Controller (MUSYCC) as the HDLC processing engine.

- The MUSYCC is an advanced, multichannel, synchronous communications controller that formats and deformats 128 HDLC channels in a single CMOS IC.
- The MUSYCC provides HDLC channels for internetworking applications such as Frame Relay, X.25, Signaling System 7 (SS7), ISDN D-channel signaling, and LAN/WAN data transport.
- Under minimal host supervision, the MUSYCC manages a linked list of channel data buffers in host memory by performing direct memory access (DMA) for the 128 channels, Tx and Rx.

The MUSYCC interfaces with four independent serial data streams, such as T1/E1/J1 signals, and then transfers data across the peripheral component interface (PCI) bus to system memory at a rate of up to 132 MBps. The wanPTMC-C4T1E1 operates in either T1 (1.544MHz) or E1 (2.048MHz) mode. Logical channels can be mapped as any combination of DS0 time slots to support ISDN hyperchannels (Nx64Kbps) or as any number of bits in a DS0 for subchanneling applications (Nx8Kbps).

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COMET framer The PMC-Sierra Quad Framer interface component (PM4354 Quad COMET) allows the software to select between T1, E1 (120 Ohm), and J1 configurations.

3-2. I/O

T1/E1/J1 ports The wanPTMC-C4T1E1 has four T1/E1/J1-compatible ports. A PMC-Sierra PM4354 Quad COMET provides the framing and line interface unit functions for all four ports. Selection between T1, E1, and J1 modes of operation is under software control. Line buildout, pulse shaping, and framing mode selection are fully programmable.

The ports can be accessed either at the PTMC front bezel through shielded RJ48c connectors, or through the Pn4 connectors for rear I/O applications. Front bezel access includes full onboard CSU and secondary surge protection for all ports. For rear Pn4 access, the CSU and secondary surge protection must be provided on the rear transition module (see Section 4-4). Selection of front or rear access is under software control.

Contact SBE technical support (800-444-0990) for a list of software available for the wanPTMC-C4T1E1 communications controller.

3-3. Compatibility

The wanPTMC-C4T1E1 is compatible with systems that have the following characteristics:

- PMC form factor
- PTMC Configuration #2 I/O
- 32 bit, 33MHz operating environment
- PCI Specification, revision 2.1

Note: The wanPTMC-C4T1E1 can be used in a standard PMC site. However, the CT-Bus interface is disabled in this situation.

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3-4. Operating Requirements

This product is designed to function within these environmental parameters:

Storage temperature:	–40 to 85 °C (–40 to 176 °F)
Operating temperature:	–5 to 55 °C (23 to 136 °F) ambient temperature with power applied
Operating humidity:	20% to 85% noncondensing
Storage humidity:	20% to 95% noncondensing
Power requirements:	7.5 watts maximum
Voltages:	5V

The PCI interface conforms to the PCI 2.1 specification for 32-bit 33MHz operation. Both 3.3V and 5V PCI bus signaling are supported.

Caution! Bring the wanPTMC-C4T1E1 communications controller to operating temperature in a noncondensing environment. The rate of change in board temperature should not exceed 2 °C (3.6 °F) per minute.

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3-5. Physical Characteristics

On a single PTMC module the wanPTMC-C4T1E1 incorporates four T1/E1/J1 framers, DSUs, CSUs, and fuses as well as the communications controller, timeslot interchanger, and CT-Bus interface. Figure 3-2 shows the physical profile of the wanPTMC-C4T1E1 module. Table 3-1 lists the dimensions.

Figure 3-2 wanPTMC-C4T1E1 physical profile

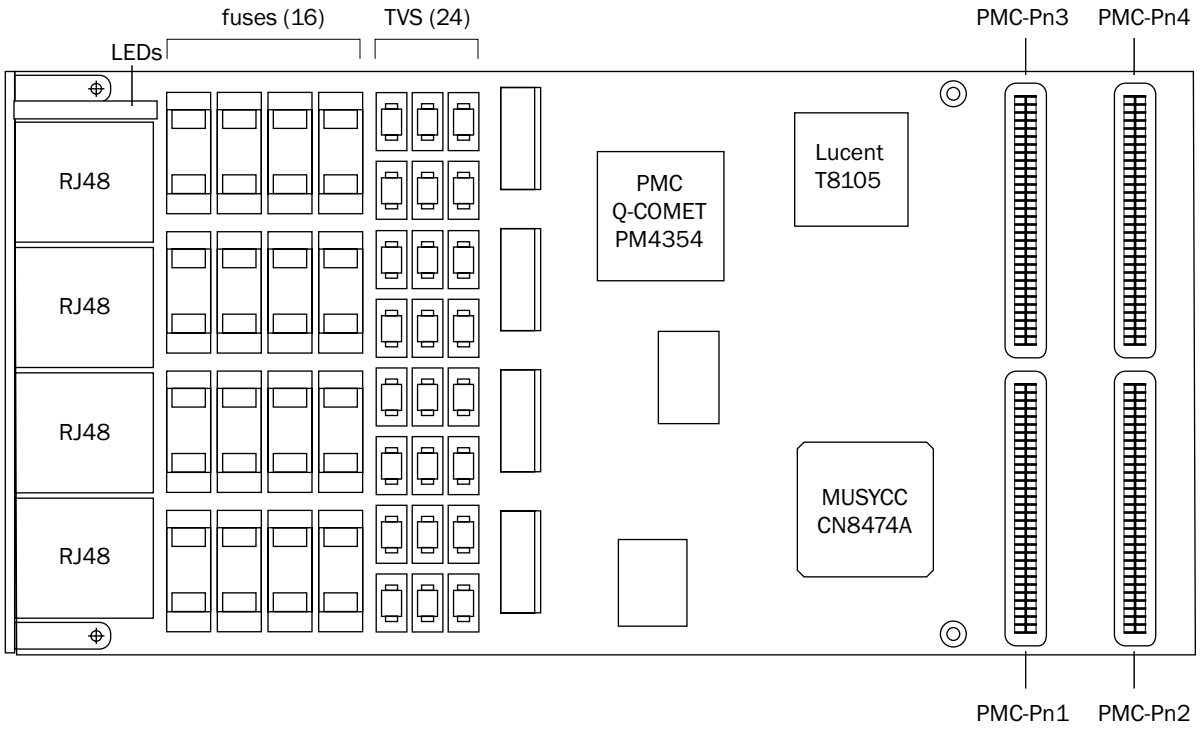


Table 3-1 wanPTMC-C4T1E1 dimensions

Length:	5.866in (149mm)
Width:	2.913in (74.0mm)
Primary side maximum component height; I/O area:	0.393 in (10.0mm)
Primary side maximum component height; component area:	0.185in (4.7mm)
Secondary side maximum component height:	0.078in (2.0mm)
Board thickness:	0.062in (1.6mm)

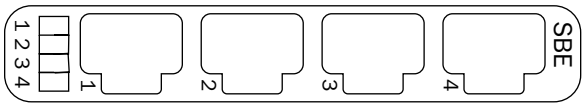
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Front bezel

The wanPTMC-C4T1E1 includes a standard IEEE 1386 outline front bezel. Two screws attach the front bezel to the PCB and connect it to frame ground. The standard EMC gasket that sits on the outside of the bezel is included.

There are cutouts in the bezel to provide access to the four RJ-48c connectors and the LEDs.

Figure 3-3 wanPTMC-C4T1E1 front bezel



Part number and serial number

All boards are marked with the manufacturing part number and assembly revision directly in ink on the PCB.

All boards are serialized physically by applying a serial number label directly to the secondary side of the PCB. A unique, electronically accessible serial number is also programmed into non-volatile memory during the manufacturing process.

Keying

Voltage keying holes in the PCB allow the module to operate in either a 5 Volt or a 3.3 Volt signaling environment.

Power

The carrier board supplies power to the wanPTMC-C4T1E1. Current is drawn from the 5-Volt power pins only. The tolerance on the 5V supply is +/-10% in accordance with the PCI Local Bus Specification.

Voltage regulators on the board generate the required 3.3 Volt and 2.5 Volt power.

Switches

The wanPTMC-C4T1E1 has no shorting jumpers or switches.

3-6. Mean Time Between Failures

The part failure source rate for the wanPTMC-C4T1E1 was calculated in accordance with the TELCORDIA TECHNOLOGIES Specification TR-332, version 6, using the Stress Analysis method. This is based on an ambient temperature of 50 °C (122 °F) in a benign, controlled environment, using Quality Level II parts.

The wanPTMC-C4T1E1 has a mean time between failures (MTBF) of 399,000 hours.

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3-7. Industry Standards Compliance

The wanPTMC-C4T1E1 complies with the following industry standard specifications:

- PICMG 2.15 R1.0, PCI Telecom Mezzanine Specification, April 3, 2001, PICMG.
- PCI Special Interest Group, “PCI Local Bus Specification”, Revision 2.1, June 1995.
- IEEE 1386-2001, Standard for a Common Mezzanine Card (CMC), Aug. 21, 2001, IEEE.
- IEEE 1386.1-2001, Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC), Aug. 16, 2001, IEEE.
- GR-63-CORE, “Network Equipment-Building Systems (NEBS) Requirements: Physical Protection”, Issue 1, October 1995, Bellcore.
- GR –1089-CORE, Electromagnetic Compatibility and Electrical Safety – Generic Criteria for Network Telecommunications Equipment, Issue 2, December 1997, Bellcore.
- GR-78-CORE, Generic Requirements for the Physical Design and Manufacture of Telecommunications Products and Equipment, Issue 1, September 1997, Bellcore.
- G.703, “Physical/electrical characteristics of hierarchical digital interfaces”, October 1998, ITU-T.
- G.704, “Synchronous Frame Structures used at Primary and Secondary Hierarchical Levels”, October 1998, ITU-T.
- G.705, “Characteristics Required to Terminate Digital Links on a Digital Exchange”, 1991, ITU-T.
- G.706, “Frame Alignment and Cyclic Redundancy Check (CRC) Procedures Relating to Basic Frame Structures Defined in Recommendation G.704”, 1991, ITU-T.
- ANSI T1.403, “Carrier-to-customer Installation - DS1 Metallic Interface”, 1995.
- AT&T PUB 43801, “Digital Channel Banks - Requirements and Objectives” November 1982.
- CB 142, “The Extended Superframe Format Interface Specification”, Issue 3, December 1983.
- AT&T TR 54016, “Requirements for Interfacing Digital Terminal Equipment to Services Employing the Extended Superframe Format”, May 1986.
- AT&T TR 62411, “ACCUNET T1.5 Service Description and Interface Specification”, December 1990.
- TR-TSY-000510, “System Interfaces, LATA Switching Systems Generic Requirements (LSSGR): Section 10", Issue 2, July 1987.

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- I.431, “Primary Rate User-Network Interface - Layer 1 Specification”, ITU-T Recommendation I.431, March 1993.
- ANSI T1.102, “Digital Hierarchy - Electrical Interfaces”, 1993.
- ANSI T1.107, “Digital Hierarchy - Formats Specifications”, 1995.
- K.20, “Resistibility of Telecommunication Equipment Installed in a Telecommunications Centre to Overvoltages and Overcurrents”, ITU-T Recommendation K.20, February 2000.
- K.21, “Resistibility of Subscriber's terminal to Overvoltages and Overcurrents”, February 2000, ITU.

3-8. Certifications

Certifications pending

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3-9. Returns/Service

Before returning any equipment for service you must obtain a Return Material Authorization (RMA) number from SBE:

TEL: 800-925-2666 (Toll free, USA)
TEL: +925-355-2000 (Outside of USA)
FAX: +925-355-2020

Ship all returns to SBE's USA Service Center:

SBE, Inc.
2305 Camino Ramon, Suite 200
San Ramon, CA 94583

SBE's Customer Service department can be reached at 800-444-0990.

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4. Functional Interfaces

4-1. PCI Bus Interface

The wanPTMC-C4T1E1 interfaces to the host system using a 32bit/33MHz PCI 2.1 compliant bus controller. The wanPTMC-C4T1E1 can operate in a 64-bit PMC site; however, it functions in 32-bit mode with the PTMC functionality disabled.

The MUSYCC manages data transfer between the serial interfaces and shared memory over the PCI bus. The wanPTMC-C4T1E1 supports 32-bit data transfers at a clock rate of up to 33MHz. For Pn1 and Pn2 pinout definitions, see Section 8-1 and Section 8-2.

BUSMODE pins and signals

Since the wanPTMC-C4T1E1's bus protocol at the PMC connectors is PCI, the BUSMODE1# pin is asserted LOW to indicate its presence to the host and that it is capable of performing PCI protocol (see Table 4-1). The wanPTMC-C4T1E1 responds within ten PCI clock cycles after detecting the state of BUSMODE[4:2]# pins.

Table 4-1 BUSMODE support

BUSMODE[4:2]# State	Mode	BUSMODE1# State	Response Explanation
000	"Card Present" Test	0	"Card Present" Mode no bus protocol is used
001	Return Card Present if PCI capable and uses PCI protocol	0	Capable of performing PCI protocol
all other states	-	1	-

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PT interface implementation requirements

PTID signals. The PICMG 2.15 standard requires three pins (PTID[2:0]) for option identification. The wanPTMC-C4T1E1 presents Configuration #2. Upon powerup, the PTID[2:0] signals are interrogated by the host. While PTENB# is deasserted, interface signals on Pn3 and Pn4 connectors are electrically isolated from the host carrier.

Configuration #2 is presented to the carrier by having the PTID[2:0] signals in the following state:

PTID2	PTID1	PTID0
0	0	1

PTGNDZ signals

The PTGNDZ signals are special-purpose grounds that are electrically isolated from the Pn3 and become enabled when PTENB# is asserted.

JTAG interface

The wanPTMC-C4T1E1 complies with the PICMG 2.15 R1.0 CompactPCI Telecom Mezzanine Specification. The optional Pn2/Pn1 JTAG signals are implemented.

4-2. T1/E1/J1 Line Interfaces

The wanPTMC-C4T1E1 product supports four T1/E1/J1 ports. Selection of line mode between T1, E1, or J1 can be done via software command. All physical interfaces supported can be channelized to the DS0 level. The user may also aggregate DS0 channels to form fractionalized T1 data rates if the protocol on those channels is HDLC.

The wanPTMC-C4T1E1 has DSU/CSU functionality, including secondary surge protection. The physical interfaces can connect directly to public telephone networks using either an ANSI T1, TTC J1 (1.544MHz), or an European ITU CEPT telecommunications facility. These interfaces comply with FCC Part 68, CS-03, CTR-13, and Bellcore GR-1089-CORE.

The ports accommodate standard twisted pair cabling using shielded RJ48c connectors accessible from the front bezel. Customized or breakout cables are not required for connection to standards compliant facilities. Line buildouts for DSX-1 (T1 Short-haul), DS1 (T1 Long-haul), and 120Ω CEPT lines are supported. Direct connection to 75Ω coaxial cable for legacy CEPT environments is not supported.

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4-3. PTMC Interface (CT-Bus Control and Time Slot Interchange)

The PTMC interface is defined in the PICMG 2.15 specification.

The wanPTMC-C4T1E1 uses Configuration #2 of PICMG 2.15, which calls out a CT-Bus on Pn3 and User I/O on Pn4. Additionally there are a series of PTMC PTID pins that indicate Configuration #2 to the host.

The PTMC-specific functionality of the wanPTMC-C4T1E1 is centered on its PTMC CT-Bus interface. The H.110-compatible PTMC Configuration #2 CT-Bus interface on the wanPTMC-C4T1E1 has the following characteristics:

- Functionality implemented by the Lucent T8105 H.110 controller
- Connection to all 20 PTMC CT-Bus TDM streams
- Ability to map up to 512 time slots to or from any CT-Bus time slots
- Ability to map all T1/E1 time slots to any of the CT-Bus time slots
- Ability to map all MUSYCC time slots to any of the CT-Bus time slots
- Ability to map T1/E1 time slots between ports
- Ability to map T1/E1 time slots to the MUSYCC without using the CT-Bus
- Dynamic software control of all time slot mapping functionality

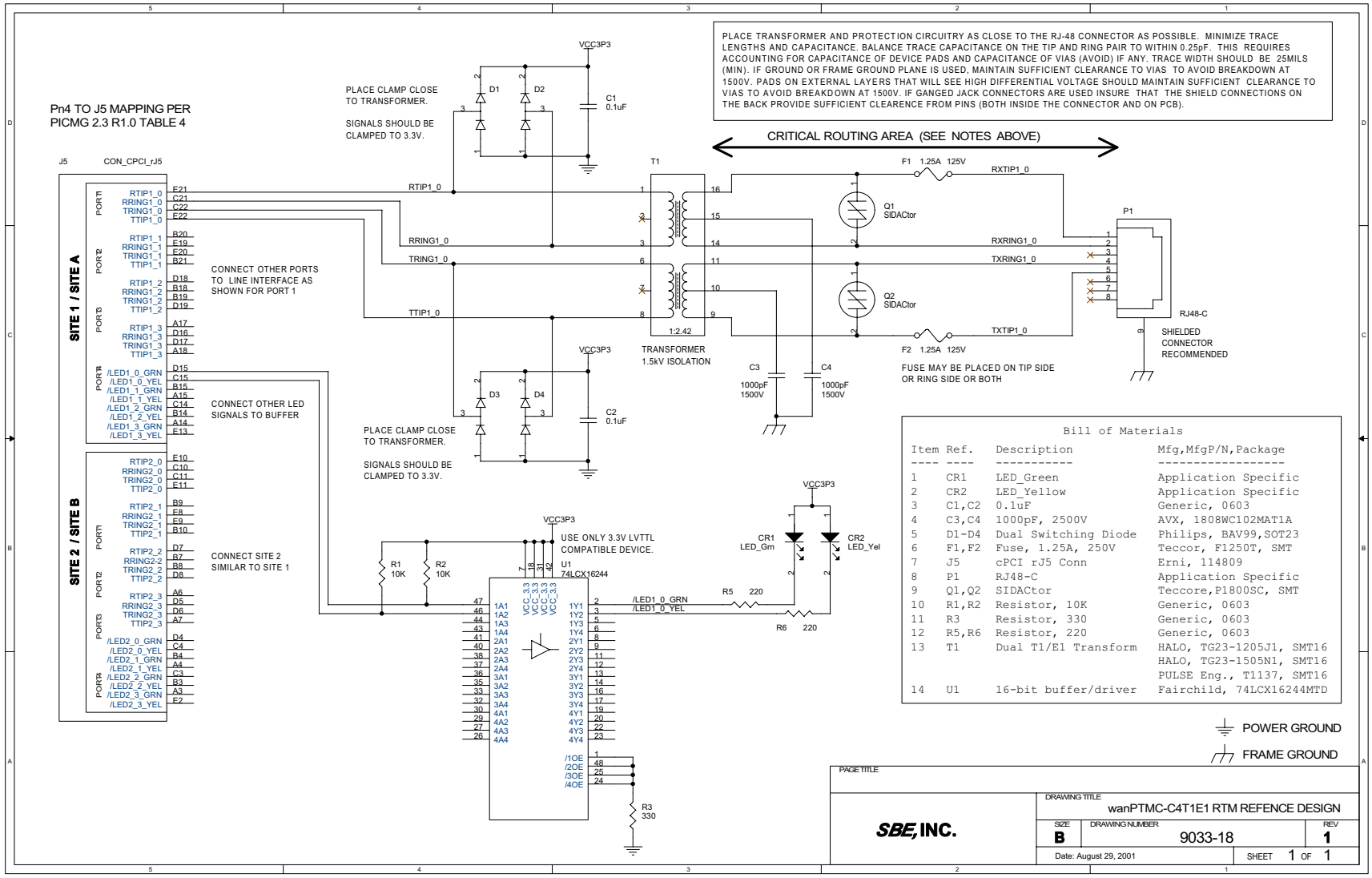
4-4. Rear I/O Option

The T1/E1 physical ports are accessible via a Rear Transition Module (when the module is installed on an appropriate carrier card). The tip and ring signals for each T1/E1 interface are switchable from front to rear access under software control. Front I/O is the default condition.

See Figure 4-1 for a wanPTMC-C4T1E1-compatible reference design.

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Figure 4-1 wanPTMC-C4T1E1 Rear Transition Module reference design



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5. Clocking

The wanPTMC-C4T1E1 supports a wide variety of network clock recovery, generation, and distribution configurations. A master clock signal can be recovered from any of the four T1/E1 ports or the CT-Bus (FrameA, FrameB, CT_C8A, CT_C8B, NetrefA, NetrefB) to provide system-wide clock synchronization. The transmit clock for each T1/E1 port can be sourced from its own recovered receive clock, the master clock, or an onboard oscillator. The onboard oscillators also provide an automatic fallback clock mechanism to allow continued data transmission if the active clock source is lost. The wanPTMC-C4T1E1 can act either as the CT-Bus clock master or as a CT-Bus clock slave.

Clock recovery and distribution is accomplished by three components: the Quad COMET, the T8105, and the CPLD. The T8105 and Quad COMET each have numerous and complex internal clock control circuits incorporating multiple PLL circuits, dividers, multipliers, multiplexers, JAT, and slip buffers. Figure 5-1 provides a simplified overview of the clock distribution and selection options on the wanPTMC-C4T1E1. See the T8105 and Quad COMET manuals for details of the internal clocking options within each component.

5-1. wanPTMC-C4T1E1 Clocking Modes

The following clocking modes are supported by the wanPTMC-C4T1E1:

- Internally Generated Clock. In this mode, the wanPTMC-C4T1E1 acts as the Central Office and provides clocking to the COMET as well as the PTMC CT-Bus.
- FrameA/CT_C8A. This mode uses the FrameA/CT_C8A signal pair from the PTMC CT-Bus to generate the appropriate clocking for the COMET.
- FrameB/CT_C8B. This mode uses the FrameB/CT_C8B signal pair from the PTMC CT-Bus to generate the appropriate clocking for the COMET.
- NetrefA. In this mode, the T8105 generates its own clocks, but the clocks are synchronized to the NetrefA signal from the PTMC CT-Bus.
- NetrefB. In this mode the T8105 generates its own clocks, but the clocks are synchronized to the NetrefB signal from the PTMC CT-Bus.
- Recovered COMET (RSYNC). In this mode clock synchronization is generated by recovering the clock from the specified COMET port (T1/E1). The recovered clock can then be used to generate the frame (FrameA/B) and bit clock (CT_C8A/CT_C8B) for the PTMC CT-Bus.

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5-2. Clock Generation

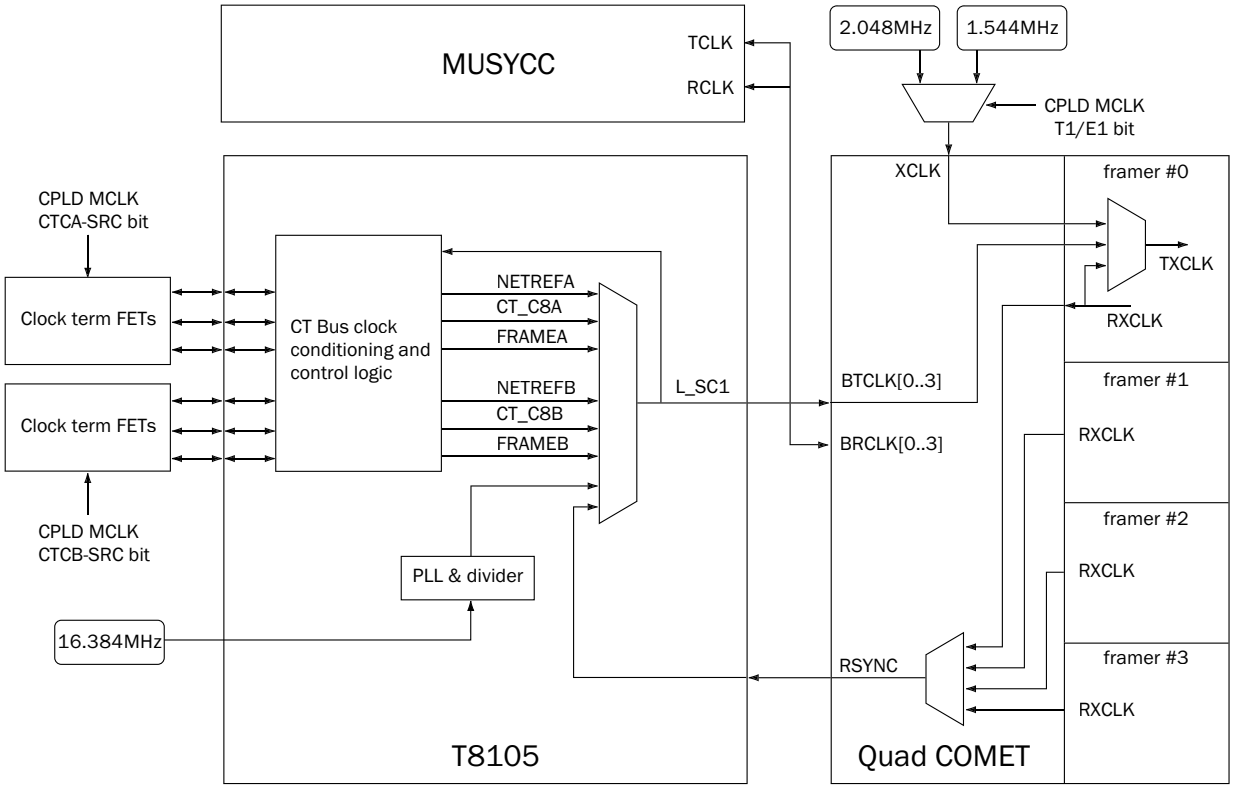
PCI clock The PCI bus provides the primary clock to the MUSYCC. The MUSYCC generates a clock (ECLK) equal to the frequency of the PCI clock, but inverted. The ECLK must be enabled, and is the main clock for all logic functions.

1.544MHz oscillator An onboard 1.544MHz oscillator with a tolerance of 50PPM is available for data synchronization when the T1 central office clock is not available.

2.048MHZ oscillator An onboard 2.048MHz oscillator with a tolerance of 50PPM is available for data synchronization when the E1 central office clock is not available.

T8105 The T8105 uses a 16.384MHz crystal with a tolerance of 32PPM.

Figure 5-1 wanPTMC-C4T1E1 clock distribution and selection options (simplified overview)



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6. Powerup and Reset

6-1. Reset Functions

All major components on the board are reset upon powerup and when PCI reset is asserted.

Additionally, a reset register in the PLD provides the capability to individually reset the COMET and the T8105. The MUSYCC has an integral software reset capability.

The wanPTMC-C4T1E1 employs an onboard power monitor that generates a reset signal if VCC_3.3 drops below 2.88V. It has a trip voltage between 2.80V and 2.97V (2.88V trip voltage is typical).

The wanPTMC-C4T1E1 employs an undervoltage detection circuit for the 2.5V regulator that asserts /RESET when an undervoltage condition exists. It has a trip voltage between 2.0V and 2.2V.

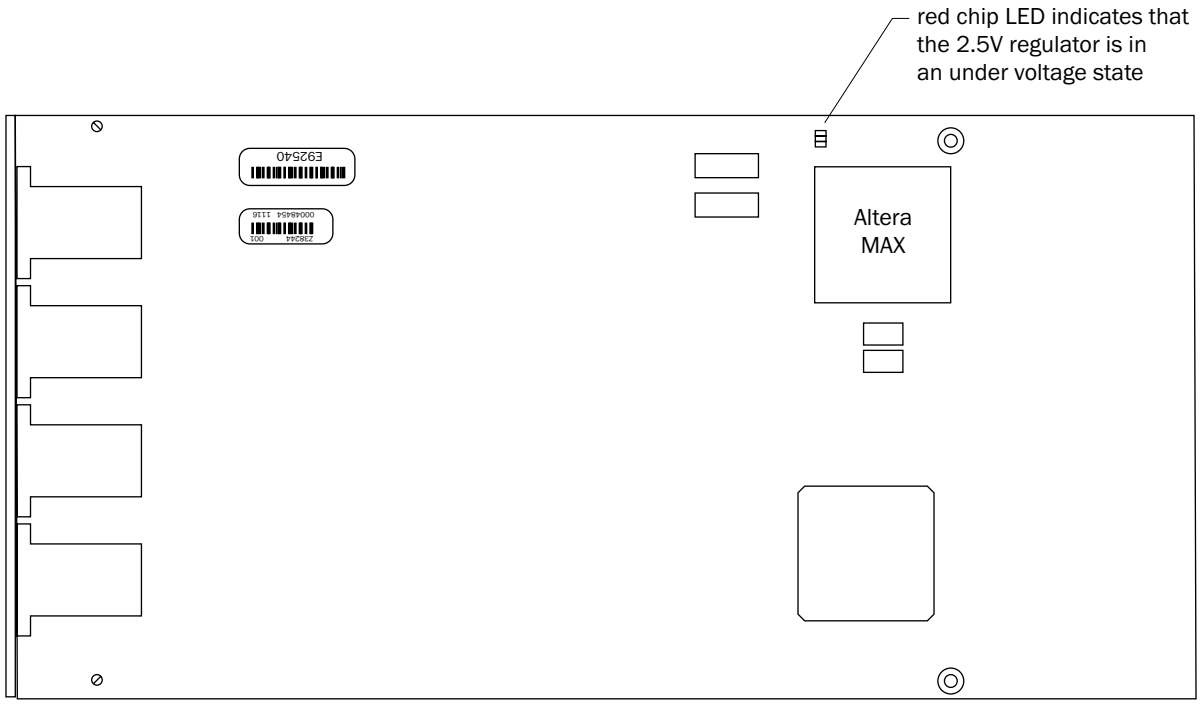
A power monitor circuit holds the board in reset when the supply voltage is more than 10% out of tolerance.

6-2. Voltage Regulator and Powerup Sequencing

The wanPTMC-C4T1E1 draws all of its power from the 5.0V power pins on the PTMC connectors. It does not use the 3.3V, +12V, or –12V power pins. Circuitry to provide regulated 3.3V and 2.5V power for onboard components is included on the wanPTMC-C4T1E1 to ensure the required tolerance, powerup sequencing, and undervoltage detection requirements are met. A 5V supply with a ±10% tolerance is the only source required from the host card. An undervoltage indicator LED for the onboard 2.5V supply is located as indicated in Figure 6-1.

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Figure 6-1 LED indicates undervoltage state



Powerup sequencing

The power sequence is 5V, then 3.3V, then 2.5V. The 3.3V regulator is delayed by 150ms by means of an undervoltage (UV) detector that holds the 3.3V regulator in an off state until the 5V source reaches 4.5V. The 2.5V regulator follows the 3.3V.

The wanPTMC-C4T1E1 must be reset and initialized before it can be programmed. The host must configure the MUSYCC as a PCI master and allow the MUSYCC to access host memory addresses. The host also must write to the function 1 PCI configuration command register, enabling access to the wanPTMC-C4T1E1 EBus space.

The following steps outline the sequence of events to bring up the board after a reset condition.

1. Map function 0 and function 1 into the PCI's memory address space. Each function requires at least 1 megabyte of memory space.
2. Enable memory accesses into the PMC's address space.
3. Write to the Global Configuration Descriptor in the MUSYCC that sets up the access time and enables the EBus for individual accesses.
4. Depending on how you want the board configured, write to the MCLK register to configure which ports are E1 and which are T1. Then write to the master clock select register (MCSR) to define which port(s) should be master.
5. Initialize the COMETs based on the MCSR setting.
6. Initialize the MUSYCC to support your specific requirements.

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7. Programming Information

7-1. Memory Map

The EBUS (Expansion Bus) of the MUSYCC is connected to four devices: the Quad COMET, the serial EEPROM, the T8105, and the CPLD. The CPLD manages the timing between the Serial EEPROM and the EBUS. The EBUS interface uses the lower 20 bits from the PCI address lines (AD[19:0]) to construct a byte address for the EBUS. Specifically, PCI address lines AD[19:2] are remapped to EBUS address lines EAD[17:0]. Addressing is on a word boundary. Data is presented in the least significant byte of the word boundary.

Table 7-1 Memory map for the I/O devices

Device	EAD Address	PCI Address	
	Begin Address	Begin	End
Quad COMET	xxx20000 Hex	xxx80000 Hex	xxx80800
Serial EEPROM	xxx30000 Hex	xxxC0000 Hex	xxxC0001
CPLD	xxx34000 Hex	xxxD0000 Hex	xxxD0010
T8105	xxx38000 Hex	xxxE0000 Hex	xxxE000C

Only single word (32-bit) PCI operations can be performed when accessing the EBUS.

See the CN8478/CN8474A datasheet for more detail.

7-2. Clock Registers and Parameters

The clock registers within the T8105 are addressed indirectly through the main registers in the T8105.

To read the indirect registers from the T8105, the AMR (address mode register) and LAR (lower address register) must be set up to point to the correct indirect register. After these two main registers are written, the requested data can be accessed by doing a read from the IDR (indirect data register).

To write the indirect registers, the AMR and the LAR registers must be set up to point to the correct indirect register. Writing data to the IDR will cause the data to be transferred to the appropriate indirect register.

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Table 7-2 T8105 main registers

Direct Register Name	Offset	Description
MCR	0x00	Master Control and Status
LAR	0x01	Lower Address Register
AMR	0x02	Address Mode Register
IDR	0x03	Indirect Data Register

Table 7-3 Indirect registers used to set up T8105 clocking

Indirect Register Name	Offset (LAR Value)	Description
CKM	0x00	Main Clock Selection
CKR	0x03	Clock- Resource Selection
CKMD	0x07	Main Divider Value
CKRD	0x09	Resource Divider Value
CON	0x0E	Connection Delay Type

Example 1: To write a value to CKMD (indirect register):

1. write 0 to AMR
2. write 0x07 to LAR
3. write the value to IDR

Example 2: To read a value from CKRD (indirect register):

1. write a 0 to AMR
2. write 0x09 to LAR
3. read the value from IDR

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Table 7-4 T8105 register settings for different clock modes

Clock Type	CKM	CKR	CKMD	CKRD	CON
Internal	0x00	0x40	0xff	0x03	N/C
Sync Local CT Frame A	0x02	0x40	0xff	0x01	N/C
Sync Local CT Frame B	0x03	0x40	0xff	0x01	N/C
Sync Local CT Netref 1	0x01	0x50	0xff	0x00	0x00
Sync Local CT Netref 2	0x01	0x50	0xff	0x00	0x20
Sync on COMET Recovered Sync	0x08	0x90	0x00	N/C	N/C

7-3. CPLD Registers

The Complex Programmable Logic Device (CPLD) contains all of the necessary logic required by the MUSYCC to communicate with its peripheral components.

The CPLD handles the following logic functions:

- Serial EEPROM control
- COMET control
- Register
- Clock routing
- T8105 control
- LED control

Serial EEPROM control functions

The host must manipulate three low-order data bits of the EAD bus to successfully write to and read from the serial EEPROM.

Serial EEPROM – PCI Address = xxxC0000H **Write/ Read**

AD Bit 7	AD Bit 6	AD Bit 5	AD Bit 4	AD Bit 3	AD Bit 2	AD Bit 1	AD Bit 0
Not used	Not used	Not used	Not used	Not used	Chip Sel	Data in	Data out

Chip Sel = 1 Selects the serial EEPROM device.

= 0 Deselects the serial EEPROM device.

Data in Data from the serial EEPROM is read on this bit.

Data out Data to the serial EEPROM is written using this bit.

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Data transfers to and from the serial EEPROM are done in a serial fashion. The format for the stream of bits is as follows:

Start Bit	Opcode	Address Bits	Read Op	Data bits	Terminate Bit
1 bit	2 bits	7 bits	1 bit	8 bits	1 bit

SCLK generation. The CPLD generates SCLK. The SCLK clock has a minimum cycle time of 500ns with a clock high time specification of 250ns minimum.

Read operations. The serial EEPROM has a data cycle time of 550ns (min). Since the MUSYCC's data cycle time is approximately 300ns, the algorithm by which data is read from the serial EEPROM in a timely fashion is:

1. Host burst accesses are not allowed.
2. A minimum of 500ns delay must exist between each single host access to and from the serial EEPROM.
3. Host writes 10 bits in succession consisting of the Start Bit, OPCODE, and ADDRESS bits. This involves setting EAD2 bit = 1, and EAD0 bit to the desired Start Bit, opcode and address.
4. The first read after a write is a dummy read and the host ignores this bit. During this read cycle, the CPLD latches the first data bit from the serial EEPROM.
5. With the following read, the MUSYCC transfers the bit from the register to the EAD1 bit of the Expansion Bus. During this cycle, the CPLD fetches the second data bit. Thus, on the third read cycle, the second bit is present on EAD1 of the Expansion Bus, and so on.
6. Host continues to read until all data bits are successfully read.
7. Terminating the read operation is done by a final write to the MUSYCC. This write sets EAD2 bit = 0, which drops chip select to the serial EEPROM. The serial EEPROM clock (SEPCLK) is generated by the CPLD.

Write operations.

1. Host burst accesses are not allowed.
2. A minimum of 500ns delay must exist between each single host access to and from the serial EEPROM.
3. Host writes 10 bits in succession consisting of the SB, OPCODE, and ADDRESS bits. This involves setting EAD2 bit = 1, and EAD0 bit to the desired Start Bit, opcode, and address.
4. Host continues to write eight bits representing the byte that is to be stored in the serial EEPROM.
5. Terminating the write operation is done by a final write to the MUSYCC. This write sets EAD2 bit = 0, which drops chip select to the serial EEPROM. The SEP-CLK signal is generated by the CPLD.

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Board ID Register (BIDR)

The BIDR contains fixed values for manufacturing support. The byte value is used to identify the wanPTMC-C4T1E1 board.

BIDR Register – PCI Address = xxxD0000H **Read Only**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	0	0	0	1

MCLK Register (MCLKR)

The framers require a MCLK that can be either T1 (1.544MHz) or E1 (2.048MHz). Two onboard oscillators are provided to be the source of those clocks. The MCLK register is used to select between the aforementioned oscillators. The MCLK register is a write/read register that defaults to zero after powerup or system reset.

The MCLK register also allows the selection of the tip and ring (transmit/ receive) signals to be routed to the RJ48 connectors or to the Pn4 connector for rear I/O connectivity.

The two most significant bits of the MCLK register are used to select the receive or transmit functions of CT_FRAME_A, CT_FRAME_B, CT_C8A, and CT_C8B.

The table below defines the bits of the MCLK register:

MCLKR – PCI Address = xxxD0004H **Write/ Read**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CTC8 A-SRC	CTC8 B-SRC	Enable Pullup	Rsvd	PTENB	LED 'ON'	Rear I/O Support	T1/E1

CTC8A-SRC = 0 CT_FRAME_A, CT_C8A in receive mode.
= 1 CT_FRAME_A, CT_C8A in transmit mode.

CTC8B-SRC = 0 CT_FRAME_B, CT_C8B in receive mode.
= 1 CT_FRAME_B, CT_C8B in transmit mode.

EN_PULLUP = 0 T8105 LPUE, disables all pull-ups except CT_Dxx lines and legacy clocks.
= 1 Enables all pull-ups.

PTENB = 0 Host has not enabled the PT Bus (read only).
= 1 Host has enabled the PT Bus.

LEDON = 0 LED drivers are 'OFF' (tri-stated).
= 1 LED drivers are 'ON'.

T1/E1 = 0 Select the 1.544MHz oscillator.
= 1 Select the 2.048MHz oscillator.

Rear_IO = 0 Allows Front Panel (Bezel) Connectivity.
= 1 Allows Rear I/O (Pn4) Connectivity.

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LED function registers

The wanPTMC_C4 has four LEDs that are visible from the front of the bezel. Each of the LEDs is bi-color, yellow and green. There are four registers that control the various functions:

- The LED0/1 Function Register (LED01FR) controls LEDs 0 and 1.
- The LED2/3 Function Register (LED23FR) controls LEDs 2 and 3.
- The LED Blink Rate Register (LEDBRR) controls the frequency at which the bi-color alternates between yellow and green.
- The LED Variable Rate Duty Cycle Register (LEDVDCR) controls the ratio of green to yellow when blinking is selected.

Eight different frequencies are selectable. The slowest frequency is 24 Hertz and the fastest frequency is 3016 Hertz. The LED Variable Duty Cycle Register (LEDVDCR) controls the length of time the LED is green or yellow as a function of the duty cycle of the LED Blink Rate Registers (LEDBRR) frequency. The duty cycle values range from 00H to FFH. For example, a value of 40H loaded into the LEDVDCR permits a duty cycle of 25/75, allowing the LED to display more green than yellow.

The signals that control the four LEDs are also routed to Pn4 connector of the wanPTMC-C4T1E1. All LED signals to connector Pn4 are tri-stated while /RESET is asserted or /PTENB is not asserted.

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LED 0/1 Function Register (LED01FR). The register is split into two four-bit nibbles. The left nibble controls LED 1 and the right nibble controls LED 0. Values for the LED01FR not listed below are reserved.

LED01FR – PCI Address = xxxD0008H **Write/ Read**

LED 1 (upper nibble)				LED 0 (lower nibble)			
Bit 7 VDC	Bit 6 BLK_1	Bit 5 GRN_1	Bit 4 YEL_1	Bit 3 VDC	Bit 2 BLK_0	Bit 1 GRN_0	Bit 0 YEL_0
8	4	2	1	8	4	2	1

Upper nibble = 0H LED 1 off

Upper nibble = 1H LED 1 Yellow on

Upper nibble = 2H LED 1 Green on

Upper nibble = 5H LED 1 Yellow Blinking – fixed blinking at 1.5 Hertz

Upper nibble = 6H LED 1 Green Blinking – fixed blinking at 1.5 Hertz

Upper nibble = 7H LED 1 Alternate Yellow/Green Blinking – fixed at 3 Hertz

Upper nibble = BH LED 1 Variable Blink Rate and Color Combination. Subject to the values loaded into the LEDBRR and the LEDVDCR.

Lower nibble = 0H LED 0 off

Lower nibble = 1H LED 0 Yellow on

Lower nibble = 2H LED 0 Green on

Lower nibble = 5H LED 0 Yellow Blinking – fixed blinking at 1.5 Hertz

Lower nibble = 6H LED 0 Green Blinking – fixed blinking at 1.5 Hertz

Lower nibble = 7H LED 0 Alternate Yellow/Green Blinking – fixed at 3 Hertz

Lower nibble = BH LED 0 Variable Blink Rate and Color Combination. Subject to the values loaded into the LEDBRR and the LEDVDCR.

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LED 2/3 Function Register (LED23FR). The register is split into two four-bit nibbles. The left nibble controls LED 3 and the right nibble controls LED 2. Values for the LED23FR not listed below are reserved.

LED23FR – PCI Address = xxxD0014H **Write/ Read**

LED 3 (upper nibble)				**LED 2 (lower nibble)**			
Bit 7 VDC	Bit 6 BLK_3	Bit 5 GRN_3	Bit 4 YEL_3	Bit 3 VDC	Bit 2 BLK_2	Bit 1 GRN_2	Bit 0 YEL_2
8	4	2	1	8	4	2	1

Upper nibble = 0H LED 3 off

Upper nibble = 1H LED 3 Yellow on

Upper nibble = 2H LED 3 Green on

Upper nibble = 5H LED 3 Yellow Blinking – fixed blinking at 1.5 Hertz

Upper nibble = 6H LED 3 Green Blinking – fixed blinking at 1.5 Hertz

Upper nibble = 7H LED 3 Alternate Yellow/Green Blinking – fixed at 3 Hertz

Upper nibble = BH LED 3 Variable Blink Rate and Color Combination. Subject to the values loaded into the LEDBRR and the LEDVDCR.

Lower nibble = 0H LED 2 off

Lower nibble = 1H LED 2 Yellow on

Lower nibble = 2H LED 2 Green on

Lower nibble = 5H LED 2 Yellow Blinking – fixed blinking at 1.5 Hertz

Lower nibble = 6H LED 2 Green Blinking – fixed blinking at 1.5 Hertz

Lower nibble = 7H LED 2 Alternate Yellow/Green Blinking – fixed at 3 Hertz

Lower nibble = BH LED 2 Variable Blink Rate and Color Combination. Subject to the values loaded into the LEDBRR and the LEDVDCR.

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LED Blink Rate Register (LEDBRR). The LEDBRR is used to set the rate at which the LED alternates between yellow and green. Eight frequencies are available, defined in the table below.

LEDBRR – PCI Address = xxxD0018H **Write/ Read**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	4	2	1

LEDBBR = 07H Sets the blink rate to 3016 Hertz

LEDBBR = 06H Sets the blink rate to 1507 Hertz

LEDBBR = 05H Sets the blink rate to 754 Hertz

LEDBBR = 04H Sets the blink rate to 377 Hertz

LEDBBR = 03H Sets the blink rate to 186 Hertz

LEDBBR = 02H Sets the blink rate to 94 Hertz

LEDBBR = 01H Sets the blink rate to 48 Hertz

LEDBBR = 00H Sets the blink rate to 24 Hertz

LED Variable Duty Cycle Register (LEDVDCR). The LEDVDCR sets the duty cycle of the LEDBRR. The duty cycle values range from 00H to FFH. For example, a value of FFH loaded into the LEDVDCR permits only yellow, while a value of 00 permits only green. A value of C0H permits a duty cycle of 75/25, allowing the LED to display more yellow than green. A value of 40H permits a duty cycle of 25/75, allowing the LED to display more green than yellow; thus a value of 00H permits only green.

LEDVDCR – PCI Address = xxxD001CH **Write/Read**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

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Interrupt Register (INTR)

The MUSYCC requires the use of INTA# and INTB#.

The MUSYCC drives INTA# to indicate a MUSYCC interrupt condition to the PCI host processor.

The MUSYCC drives INTB# to notify the PCI host processor of an interrupt pending from the EBUS. Interrupts from the T8105 and COMET are latched in the Interrupt Register resident in the CPLD. The interrupts are logically OR-ed to generate /EINT to the MUSYCC. The MUSYCC transfers /EINT from the EBUS to the PCI INTB# pin. The PCI host processor reads the Interrupt Register to determine which device was responsible for the interrupt.

INTR – PCI Address = xxxD000CH **Read Only**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T8105 System	T8105 Clock	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	COMET

Interrupt Enable Register (INTENR)

The Interrupts Enable Register is used to allow the interrupts from the devices. Immediately after /RESET is asserted, the INTENR masks all of the interrupt.

INTMR – PCI Address = xxxD0010H **Write/Read**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mask 7	Mask 6	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Mask 0

Mask 7 = 1 Allow T8105 system interrupt
= 0 Mask T8105 system interrupt

Mask 6 = 1 Allow T8105 clock interrupt
= 0 Mask T8105 clock interrupt

Mask 0 = 1 Allow COMET interrupts
= 0 Mask COMET interrupts

COMET control functions

The CPLD translates write and read operations, which are executed by the MUSYCC via its EBUS, to generate the appropriate chip select and write/read control timing signals for the COMET to execute.

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7-4. MUSYCC Initialization

The MUSYCC must be initialized prior to the initialization of the T8105 and the COMETs. Most of the MUSYCC configuration is application-specific. The registers indicated in Table 7-5 should be set to ensure proper connectivity between the MUSYCC and the T8105. Refer to the MUSYCC documentation for more detail.

Table 7-5 MUSYCC registers to set for proper connectivity with T8105

Register Name	Register Offset	Value	Description
DUAL_ADR_PTR	0x0004	0x0000	32-bit memory addressing
GLOBAL CONFIGURATION DESCRIPTOR	0x0600	0x786C	BLAPSE=7 (Exp bus access time) ECKEN=1 (Exp bus clock enable) ALAPSE=1 (Exp bus addr duration) ELAPSE=7 (Exp bus data duration) INTAMSK=1 (INTA interrupt disable) INTBMSK=1 (INTB interrupt disable)
PORT_CFG_DSC	0x0618	0x0211(E1) 0x0210(T1)	Transmit Tri State Disabled ROOF sampled on falling edge RSYNC sampled on falling edge RDAT sampled on falling edge TSYNC sampled on falling edge TDAT sampled on rising edge

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7-5. COMET Initialization

Table 7-6 COMET initialization

Register Name	Register Offset	T1 Initial Value	T1 Description	E1 Initial Value	E1 Description
GLOBALCFG	0x00	0x80	T1 mode, PIO output enabled	0x81	Set E1/T1B=1 for E1 mode.
CSUCFG	0xD6	0x01	Set MODE[2:0]=1, BCLK=2.048MHz, XCLK=1.544MHz, TCLKO=1.544MHz	0x00	Set MODE[2:0]=0, XCLK=2.048MHz, TCLKO=2.048MHz
CDRCCFG	0x10	0x00	Set AMI=0 for B8ZS line decoding	0x00	Set AMI=0 for HDB3 line decoding
RXESCFG	0x1C	0x00	Set IR=0 and OR=0 to enable the RX-ELST for T1 mode	0x03	Set IR=1 and OR=1 to enable the RX-ELST for E1 mode
TXESCFG	0x20	0x00	Set IR=0 and OR=0 to enable the TX-ELST for T1 mode	0x03	Set IR=1 and OR=1 to enable the TX-ELST for E1 mode
T1XBASCFG	0x54	0x30	Set ESF=1 for ESF framing and B8ZS=1 for B8ZS		
T1CFG	0x48	0x30	Set ESF=1 to receive T1-ESF framing format		
T1ALMCFG	0x60	0x10	Set ESF=1 and FMS1=0 and FMS0=0 for ESF mode with 4Kbit FDL Data rate		
E1TRANCFG	0x80			0x10	Set GENCRC=1, SIGEN=0, DLEN=0 CRC Multi-frame only AMI=0 for HDB3 line encoding
E1FRMRFAO	0x90			0xC2	Set CRCEN=1, CASDIS=1 to receive E1 CRC Multi-frame format
RXCE1CTL	0x28			0x00	Disable T1 receive data link (required in E1 mode)
TXCI1CTL	0x38			0x00	Disable T1 transmit data link (required in E1 mode)
RXLINECFG	0x03			0x00	Turn off auto alarms & RUNI=0 recover received clock

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Table 7-6 COMET initialization (continued)

Register Name	Register Offset	T1 Initial Value	T1 Description	E1 Initial Value	E1 Description
SIGXCFG	0x50	0x04	Set ESF=1 for ESF mode, PCCE=0 the Per-Timeslot/ Per-Channel Configuration Register	0x00	Set PCCE=0 to disable the Per-Timeslot/Per-Channel Configuration Register
BTIFCFG	0x40	0x39	BTCLK=Clock Slave Mode, Full Framed. BTPCM and BTSIG are sampled on the falling edge of BTCLK. BTFP is sampled on the rising edge of BTCLK. Backplane clock=2.048M	0x29	BTCLK=Clock Slave Mode, Full Framed. BTPCM and BTSIG are sampled on the falling edge of BTCLK. BTFP is sampled on the rising edge of BTCLK. Backplane clock=2.048M
BTIFPULSE	0x41	0x85	Set FPMODE=1, BTFP is in frame pulse slave mode, ESF enabled, Map=1 Tslots 0..23	0x01	Set FPMODE=1, BTFP is in frame pulse slave mode
BTIFBIT	0x44	0x00	Set BOFF_EN=0, disable delaying the data after FP	0x00	Set BOFF_EN=0, disable delaying the data after FP
BRIFCFG	0x30	0x29	BRCLK=Clock Slave Mode, Full Framed. BRPCM and BRSIG are updated on the rising edge of BRCLK. BRFP is sampled on the rising edge of BTCLK. Backplane clock=2.048M	0x39	BRCLK=Clock Slave Mode, Full Framed. BRPCM and BRSIG are updated on the rising edge of BRCLK. BRFP is sampled on the rising edge of BTCLK. Backplane clock=2.048M
BRIFPULSE	0x31	0xa0	SET FPMODE=1, BRFP is in frame pulse slave mode, Map=1 Tslots 0..23.	0x20	SET FPMODE=1, BRFP is in frame pulse slave mode
BRIFPARITY	0x32	0x01	Set TR[1:0]=01, to enable the backplane data and signaling (High impedance mode off)	0x01	Set TR[1:0]=01, to enable the backplane data and signaling (High impedance mode off)
BRIFBIT	0x34	0x00	Set BOFF_EN=0, disable delaying the data after FP	0x00	Set BOFF_EN=0, disable delaying the data after FP
MASTERDIAG	0x0A	0x00	Ensure diagnostics are turned off	0x00	Ensure diagnostics are turned off
MASTERTEST	0x0B	0x00	Ensure COMET tests are turned off	0x00	Ensure COMET tests are turned off

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Table 7-6 COMET initialization (continued)

Register Name	Register Offset	T1 Initial Value	T1 Description	E1 Initial Value	E1 Description
TXTIMING	0x06	0x0c	Set the transmit jitter attenuator to use TCLKI as the reference clock and to enable the transmit Elastic Store	0x0c	Set the transmit jitter attenuator to use TCLKI as the reference clock and to enable the transmit Elastic Store
TJATRCLK	0x19			0xff	Set N1 divisor to max
TJATOCLK	0x1A			0xff	Set N2 divisor to max
RXLINECFG	0x03	0x00	RUNI=0 recover received clock		
RLPSCFG	0xF8	0x01	Set LONGE=1, enables the equalizer	0x01	Set LONGE=1, enables the equalizer
RLPSALOST	0xF9	0x00	ALOS clearance	0x00	ALOS clearance
RLPSALOSD	0xFA	0x01	DET_PER[0]=1, 16 pulse intervals	0x01	DET_PER[0]=1, 16 pulse intervals
RLPSALOSC	0xFB	0x01	CLR_PER[0]=1, 16 pulse intervals	0x01	CLR_PER[0]=1, 16 pulse intervals
RLPSADDR	0xFC	0x00	EQ_ADDR[7:0]=0	0x00	EQ_ADDR[7:0]=0
RLPSRW	0xFD	0x80	RWB=0, a write to the RAM is desired	0x80	RWB=0, a write to the RAM is desired
RLPSELOOP	0xFE	0x00	LOCATION[7:0]=0	0x00	LOCATION[7:0]=0
RLPSECFG	0xFF	0x0b	Set EQFBL_EN=1, Configure the receive line equalization for the correct feedback loop frequency and to enable the feedback loop, must always be 1	0x0b	Set EQFBL_EN=1, Configure the receive line equalization for the correct feedback loop frequency and to enable the feedback loop, must always be 1
TJATCFG	0x1B	0x10	LIMIT=0, CENT=1, Set the transmit jitter attenuator FIFO to center when 4UI from being overflowed or underflowed	0x10	LIMIT=0, CENT=1, Set the transmit jitter attenuator FIFO to center when 4UI from being overflowed or underflowed
RJATCFG	0x17	0x10	LIMIT=0, CENT=1, Set the receive jitter attenuator FIFO to center when 4UI from being overflowed or underflowed	0x10	LIMIT=0, CENT=1, Set the receive jitter attenuator FIFO to center when 4UI from being overflowed or underflowed

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Table 7-6 COMET initialization (continued)

Register Name	Register Offset	T1 Initial Value	T1 Description	E1 Initial Value	E1 Description
RXOPTIONS	0x02	0x08	Set the RJATBYP=0 to enable the attenuator on the receive line side, RSYNC=8K rate	0x08	Set the RJATBYP=0 to enable the attenuator on the receive line side, RSYNC=8K rate
XLPGATPOS	0xF4	0x01	TPC[0] = 1, enable active low	0x01	TPC[0] = 1, enable active low
XLPGATNEG	0xF5	0x01	TNC[0] = 1, enable active low	0x01	TNC[0] = 1, enable active low
RLPSEVOLT	0xDC	0x2c	Configure the RLPS Equalizer Voltage Reference	0x3D	Configure the RLPS Equalizer Voltage Reference
RLPSEFUSE	0xDD	0x00	RLPS Fuse Control and Status	0x00	RLPS Fuse Control and Status

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7-6. Quad COMET Waveform Templates

The COMET's internal D/A pulse waveform template registers can be used to create a custom waveform. These are accessed indirectly throught the XLPG Pulse Waveform Storage Write Address and the XLPG Pulse Waveform Storage Data register. The values written into the pulse waveform storage registers correspond to one of 127 quantized levels. Twenty-four samples are output during every transmit clock cycle.

The waveform being programmed is completely arbitrary and programming must be done to meet the various T1 and E1 template specifications. The SCALE bits of the Line Driver Configuration Register bits are used to obtain the proper output amplitude.

Table 7-7 XLPG line driver configuration (Register 0xF0)

Bit	Type	Function	Default
7	R/W	HIGHZ	1
6		Unused	
5		Unused	
4	R/W	SCALE[4]	0
3	R/W	SCALE[3]	0
2	R/W	SCALE[2]	0
1	R/W	SCALE[1]	0
0	R/W	SCALE[0]	0

HIGHZ controls whether the TXTIP and TXRING outputs are to be tri-stated or not. When HIGHZ is set to a logic 1, the output are put into a high impedance state.

The SCALE bits control the amplitude of the D/A output waveform. A value of 0 tristates the output, while a maximum value of 21 (0x15) sets the full scale current to 234 mA.

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XLPG pulse waveform storage

Table 7-8 XLPG pulse waveform storage write address (Register 0xF2)

Bit	Type	Function	Default
7	R/W	SAMPLE [4]	0
6	R/W	SAMPLE [3]	0
5	R/W	SAMPLE [2]	0
4	R/W	SAMPLE [1]	0
3	R/W	SAMPLE [0]	0
2	R/W	UI[2]	0
1	R/W	UI[1]	0
0	R/W	UI[0]	0

The pulse waveform write address is composed of a unit interval selector and a sample selector. The unit interval selector (UI[2:0]) selects which unit interval is being written to a given sample. There are five unit intervals, numbered 0 to 4. UI[2:0] can have the values 0–4. The values 5–7 are undefined. The sample selector (SAMPLE[4:0]) selects which sample is being written for a given unit interval. There are 24 samples, numbered from 0 to 23. Valid values for sample are from 0x00 to 0x17. 0x18–0x1F are undefined.

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CLPG pulse waveform storage data

Table 7-9 CLPG pulse waveform storage data (Register 0xF3)

Bit	Type	Function	Default
7		Unused	X
6	R/W	WDAT[6]	X
5	R/W	WDAT[5]	X
4	R/W	WDAT[4]	X
3	R/W	WDAT[3]	X
2	R/W	WDAT[2]	X
1	R/W	WDAT[1]	X
0	R/W	WDAT[0]	X

WDAT[6:0] allows software to program the contents of any one of the 120 internal waveform template registers, addressed by UI[2:0] and SAMPLE [4:0] bits in the Pulse Waveform Storage Write Address Register. When accessing the internal waveform storage registers, the address of the desired register must be first written to the Indirect Address register. By writing the Indirect Data register, the microprocessor can write the data to the selected write address.

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7-7. Quad COMET Receive Line Equalizer RAM

For correct operation, properly initialize the line receiver:

1. Set the Reserved bit of the RLPS Equalizer Configuration register to a logic 1.
2. Program the EQ_VREF[5:0] bits of the RLPS Equalizer Voltage Reference register to 0x2C.
3. Initialize a RAM table.

Since the line receiver supports both E1 and T1 standards over short haul and long haul cables, the line receiver has two modes of operation, as selected by the T1/E1 bit in the Global Configuration register.

Table 7-10 RLPS Equalization Indirect Address (Register 0xFC)

Bit	Type	Function	Default
7	R/W	EQ_ADDR[7]	0
6	R/W	EQ_ADDR[6]	0
5	R/W	EQ_ADDR[5]	0
4	R/W	EQ_ADDR[4]	0
3	R/W	EQ_ADDR[3]	0
2	R/W	EQ_ADDR[2]	0
1	R/W	EQ_ADDR[1]	0
0	R/W	EQ_ADDR[0]	0

Writing to this register initiates an internal uP access request cycle to the RAM. Depending on the RWB bit inside register 0xFD, a read or a write operation is performed. During a write cycle, the indirect data bits located in registers 0xD8–0xDB are written into RAM. During a read operation, the contents of the RAM location are written to these registers. This register is the last one written for a uP access.

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RLPS Equalization Read/Write Select Register

Table 7-11 RLPS Equalization Read/Write Select (Register 0xFD)

Bit	Type	Function	Default
7	R/W	RWB	0
6		Unused	X
5		Unused	X
4		Unused	X
3		Unused	X
2		Unused	X
1		Unused	X
0		Unused	X

This bit selects the operation to be performed on the RAM. When RWB = 1, a read operation will be performed. When 0, a write operation will occur.

RLPS Equalization Indirect Data Registers

Table 7-12 RLPS Equalization Indirect Data Registers (0xD8, 0xD9, 0xDA, 0xDB)

Bit	Type	RLPS0 (0xD8)	RLPS1 (0XD9)	RLPS2 (0XDA)	RLPS3 (0XDB)	Default
7	R/W	EQ_DATA[31]	EQ_DATA[23]	EQ_DATA[15]	EQ_DATA[7]	0
6	R/W	EQ_DATA[30]	EQ_DATA[22]	EQ_DATA[14]	EQ_DATA[6]	0
5	R/W	EQ_DATA[29]	EQ_DATA[21]	EQ_DATA[13]	EQ_DATA[5]	0
4	R/W	EQ_DATA[28]	EQ_DATA[20]	EQ_DATA[12]	EQ_DATA[4]	0
3	R/W	EQ_DATA[27]	EQ_DATA[19]	EQ_DATA[11]	EQ_DATA[3]	0
2	R/W	EQ_DATA[26]	EQ_DATA[18]	EQ_DATA[10]	EQ_DATA[2]	0
1	R/W	EQ_DATA[25]	EQ_DATA[17]	EQ_DATA[9]	EQ_DATA[1]	0
0	R/W	EQ_DATA[24]	EQ_DATA[16]	EQ_DATA[8]	EQ_DATA[0]	0

These registers consist of two parts: read-only and write-only, Writing to this register affects the least significant byte of the input-data to the equalization RAM. Reading it returns the least significant byte of the RAM location indexed by register 0xFC.

For T1 and E1 equalization data, see Chapter 10, *Appendix C: T1 /E1 Equalization Data Tables*.

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8. Appendix A: PTMC-Pn Pinout Definitions

8-1. PTMC-Pn1 pinout definitions

Table 8-1 PTMC-Pn1 connector pin assignments

PTMC Signal Name	Pn1 Pin #	wanPTMC-C4T1E1 Signal	PTMC Signal Name	Pn1 Pin #	wanPTMC-C4T1E1 Signal
TCK	1	TCK	-12V	2	-12V
Ground	3	Ground	INTA#	4	/INTA
INTB#	5	/INTB	INTC#	6	/INTC
BUSMODE1#	7	/BUSMODE1	+5V	8	+5V
INTD#	9	/INTD	PCI-RSVD	10	PCI-RSVD
Ground	11	PTGNDZ1	PCI-RSVD	12	PCI-RSVD
CLK	13	REFCLK	Ground	14	Ground
Ground	15	Ground	GNT#	16	/GNT
REQ#	17	/REQ	+5V	18	+5V
V (I/O)	19	V[I-O]1	AD[31]	20	AD[31]
AD[28]	21	AD[28]	AD[27]	22	AD[27]
AD[25]	23	AD[25]	Ground	24	Ground
Ground	25	Ground	C/BE[3]#	26	/C/BE[3]
AD[22]	27	AD[22]	AD[21]	28	AD[21]
AD[19]	29	AD[19]	+5V	30	+5V
V (I/O)	31	V (I/O)2	AD[17]	32	AD[17]
FRAME#	33	/FRAME	Ground	34	Ground
Ground	35	Ground	IRDY#	36	/IRDY
DEVSEL#	37	/DEVSEL	+5V	38	+5V
Ground	39	Ground	LOCK#	40	/LOCK
SDONE#	41	/SDONE	SBO#	42	/SBO
PAR	43	PAR	Ground	44	Ground
V (I/O)	45	V (I/O)4	AD[15]	46	AD[15]
AD[12]	47	AD[12]	AD[11]	48	AD[11]
AD[09]	49	AD[09]	+5V	50	+5V
Ground	51	Ground	C/BE[0]#	52	/C/BE[0]
AD[06]	53	AD[06]	AD[05]	54	AD[05]
AD[04]	55	AD[04]	Ground	56	Ground
V (I/O)	57	V (I/O)3	AD[03]	58	AD[03]
AD[02]	59	AD[02]	AD[01]	60	AD[01]
AD[00]	61	AD[00]	+5V	62	+5V
Ground	63	Ground	REQ64#	64	/REQ64

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8-2. PTMC-Pn2 pinout definitions

Table 8-2 PTMC-Pn2 connector pin assignments

PTMC Signal Name	Pn2 Pin #	wanPTMC-C4T1E1 Signal	PTMC Signal Name	Pn2 Pin #	wanPTMC-C4T1E1 Signal
+12V	1	+12V	TRST#	2	/TRST
TMS	3	TMS	TDO	4	TDO
TDI	5	TDI	Ground	6	Ground
Ground	7	Ground	PCI-RSVD	8	PCI-RSVD
PCI-RSVD*	9	PCI-RSVD*	PCI-RSVD	10	PCI-RSVD
BUSMODE2#	11	/BUSMODE2	+3.3V	12	+3.3V
RST#	13	/RST	BUSMODE3#	14	/BUSMODE3
+3.3V	15	+3.3V	BUSMODE4#	16	/BUSMODE4
PCI-RSVD*	17	PCI-RSVD*	Ground	18	Ground
AD[30]	19	AD[30]	AD[29]	20	AD[29]
Ground	21	Ground	AD[26]	22	AD[26]
AD[24]	23	AD[24]	+3.3V	24	+3.3V
IDSEL	25	IDSEL	AD[23]	26	AD[23]
+3.3V	27	+3.3V	AD[20]	28	AD[20]
AD[18]	29	AD[18]	Ground	30	Ground
AD[16]	31	AD[16]	C/BE[2]#	32	/C/BE[2]
Ground	33	Ground	PMC-RSVD	34	PMC-RSVD
TRDY#	35	/TRDY	+3.3V	36	+3.3V
Ground	37	Ground	STOP#	38	/STOP
PERR#	39	/PERR	Ground	40	Ground
+3.3V	41	+3.3V	SERR#	42	SERR#
C/BE[1]#	43	/C/BE[1]	Ground	44	Ground
AD[14]	45	AD[14]	AD[13]	46	AD[13]
Ground	47	Ground	AD[10]	48	AD[10]
AD[08]	49	AD[08]	+3.3V	50	+3.3V
AD[07]	51	AD[07]	PMC-RSVD	52	PMC-RSVD
+3.3V	53	+3.3V	PMC-RSVD	54	PMC-RSVD
PMC-RSVD	55	PMC-RSVD	Ground	56	Ground
PMC-RSVD	57	PMC-RSVD	PMC-RSVD	58	PMC-RSVD
Ground	59	Ground	PMC-RSVD	60	PMC-RSVD
ACK64#	61	/ACK64	+3.3V	62	+3.3V
Ground	63	Ground	PMC-RSVD	64	PMC-RSVD

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8-3. PTMC-Pn3 pinout definitions

Table 8-3 PTMC-Pn3 connector pin assignments

PTMC Signal Name	Pn3 Pin #	wanPTMC-C4T1E1 Signal	PTMC Signal Name	Pn3 Pin #	wanPTMC-C4T1E1 Signal
MDIO	1	MDIO	GROUND	2	GND
GROUND	3	GND	STX	4	STX
MDC	5	MDC	SRX	6	SRX
RXER	7	RXER	GROUND	8	GND
PTID2	9	PTID2	TXD0	10	TXD0
PTGNDZ	11	PTGNDZ1	TXD1	12	TXD1
REFCLK	13	REFCLK	GROUND	14	GND
GROUND	15	GND	RXD0	16	RXD0
CT_FA	17	/HT_FRAME_A	RXD1	18	RXD1
CT_FB	19	/HT_FRAME_B	GROUND	20	GND
PTID0	21	PTID0	TXEN	22	TXEN
PTGNDZ	23	PTGNDZ3	CAS/DV	24	CAS/DV
CT_C8A	25	HT_C8_A	GROUND	26	GND
GROUND	27	GND	NETFEF1	28	HT_NETREF_1
CT_D18	29	CTD18	USER	30	USER1
CT_D16	31	CTD16	GROUND	32	GND
GROUND	33	GND	NETREF2	34	HT_NETREF_2
CT_D14	35	CTD14	USER	36	USER2
CT_D12	37	CTD12	GROUND	38	GND
PCENB#	39	/PCENB	CT_D19	40	CTD19
PTGNDZ	41	PTGNDZ2	CT_D17	42	CTD17
CT_C8B	43	HT_C8_B	GROUND	44	GND
GROUND	45	GND	CT_D15	46	CTD15
CT_D10	47	CTD10	CT_D13	48	CTD13
CT_D8	49	CTD8	CT_D11	50	CTD11
GROUND	51	GND	CT_D9	52	CTD9
CT_D6	53	CTD6	CT_D7	54	CTD7
CT_D4	55	CTD4	GROUND	56	GND
PTID1	57	PTID1	CT_D5	58	CTD5
CT_D2	59	CTD2	CT_D3	60	CTD3
CT_D0	61	CTD0	GROUND	62	GND
GROUND	63	GND	CT_D1	64	CTD1

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8-4. PTMC-Pn4 pinout definitions

Table 8-4 PTMC-Pn4 connector pin assignments

PTMC Signal Name	Pn4 Pin #	wanPTMC-C4T1E1 Signal	PTMC Signal Name	Pn4 Pin #	wanPTMC-C4T1E1 Signal
USER	1	TTIP0_Pn4	USER	2	
USER	3	TRING0_ Pn4	USER	4	
USER	5		USER	6	RTIP0_ Pn4
USER	7		USER	8	RRING0_ Pn4
USER	9	TTIP1_ Pn4	USER	10	
USER	11	TRING1_ Pn4	USER	12	
USER	13		USER	14	RTIP1_ Pn4
USER	15		USER	16	RRING1_ Pn4
USER	17	TTIP2_ Pn4	USER	18	
USER	19	TRING2_ Pn4	USER	20	
USER	21		USER	22	RTIP2_ Pn4
USER	23		USER	24	RRING2_ Pn4
USER	25	TTIP3_ Pn4	USER	26	
USER	27	TRING3_ Pn4	USER	28	
USER	29		USER	30	RTIP3_ Pn4
USER	31		USER	32	RRING3_ Pn4
USER	33		USER	34	
USER	35		USER	36	
USER	37	/LED0_GRN	USER	38	/LED0_YEL
USER	39	/LED1_GRN	USER	40	/LED1_ YEL
USER	41		USER	42	
USER	43	/LED2_GRN	USER	44	/LED2_ YEL
USER	45	/LED3_GRN	USER	46	/LED3_ YEL
USER	47		USER	48	
USER	49		USER	50	
USER	51		USER	52	
USER	53		USER	54	
USER	55		USER	56	
USER	57		USER	58	
USER	59		USER	60	
USER	61		USER	62	
USER	63		USER	64	

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9. Appendix B: Waveform Tables

The following tables are included in this appendix:

- Table 9-1, Transmit Waveform Values for T1 Shorthaul (0–110 ft.)
- Table 9-2, Transmit Waveform Values for T1 Shorthaul (110–220 ft.)
- Table 9-3, Transmit Waveform Values for T1 Shorthaul (220–330 ft.)
- Table 9-4, Transmit Waveform Values for T1 Shorthaul (440–550 ft.)
- Table 9-5, Transmit Waveform Values for T1 Shorthaul (550–660 ft.)
- Table 9-6, Transmit Waveform Values for T1 Long Haul (LBO 0 dB)
- Table 9-7, Transmit Waveform Values for T1 Long Haul (LBO 7.5 dB)
- Table 9-8, Transmit Waveform Values for T1 Long Haul (LBO 15 dB)
- Table 9-9, Transmit Waveform Values for T1 Long Haul (LBO 22.5 dB)
- Table 9-10, Transmit Waveform Values for E1 Long Haul (120 Ohms)
- Table 9-11, Transmit Waveform Values for E1 Long Haul (75 Ohms)

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9-1. Transmit Waveform Values for T1 Shorthaul (0–110 ft.)

Table 9-1 Transmit Waveform Values for T1 Shorthaul (0–110 ft.)

sample #	UI 0	UI 1	UI 2	UI 3	UI 4
0	0x00	0x46	0x00	0x00	0x00
1	0x0A	0x45	0x00	0x00	0x00
2	0x20	0x43	0x00	0x00	0x00
3	0x3D	0x41	0x00	0x00	0x00
4	0x3D	0x40	0x00	0x00	0x00
5	0x3C	0x40	0x00	0x00	0x00
6	0x3C	0x00	0x00	0x00	0x00
7	0x3B	0x00	0x00	0x00	0x00
8	0x3A	0x00	0x00	0x00	0x00
9	0x39	0x00	0x00	0x00	0x00
10	0x39	0x00	0x00	0x00	0x00
11	0x38	0x00	0x00	0x00	0x00
12	0x37	0x00	0x00	0x00	0x00
13	0x36	0x00	0x00	0x00	0x00
14	0x30	0x00	0x00	0x00	0x00
15	0x10	0x00	0x00	0x00	0x00
16	0x58	0x00	0x00	0x00	0x00
17	0x53	0x00	0x00	0x00	0x00
18	0x50	0x00	0x00	0x00	0x00
19	0x4E	0x00	0x00	0x00	0x00
20	0x4C	0x00	0x00	0x00	0x00
21	0x4A	0x00	0x00	0x00	0x00
22	0x48	0x00	0x00	0x00	0x00
23	0x47	0x00	0x00	0x00	0x00
Scale *					
front I/O	0x0D				
rear I/O	TBD				

*Value of XLPG line driver configuration (register: 0F0H)

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9-2. Transmit Waveform Values for T1 Shorthaul (110–220 ft.)

Table 9-2 Transmit Waveform Values for T1 Shorthaul (110–220 ft.)

sample #	UI 0	UI 1	UI 2	UI 3	UI 4
0	0x00	0x45	0x00	0x00	0x00
1	0x0A	0x44	0x00	0x00	0x00
2	0x33	0x42	0x00	0x00	0x00
3	0x33	0x41	0x00	0x00	0x00
4	0x33	0x40	0x00	0x00	0x00
5	0x33	0x40	0x00	0x00	0x00
6	0x30	0x00	0x00	0x00	0x00
7	0x2F	0x00	0x00	0x00	0x00
8	0x2E	0x00	0x00	0x00	0x00
9	0x2D	0x00	0x00	0x00	0x00
10	0x2C	0x00	0x00	0x00	0x00
11	0x2B	0x00	0x00	0x00	0x00
12	0x2A	0x00	0x00	0x00	0x00
13	0x29	0x00	0x00	0x00	0x00
14	0x19	0x00	0x00	0x00	0x00
15	0x5A	0x00	0x00	0x00	0x00
16	0x54	0x00	0x00	0x00	0x00
17	0x50	0x00	0x00	0x00	0x00
18	0x4E	0x00	0x00	0x00	0x00
19	0x4C	0x00	0x00	0x00	0x00
20	0x4B	0x00	0x00	0x00	0x00
21	0x48	0x00	0x00	0x00	0x00
22	0x48	0x00	0x00	0x00	0x00
23	0x47	0x00	0x00	0x00	0x00
Scale *					
front I/O	0x11				
rear I/O	TBD				

*Value of XLPG line driver configuration (register: 0F0H)

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9-3. Transmit Waveform Values for T1 Shorthaul (220–330 ft.)

Table 9-3 Transmit Waveform Values for T1 Shorthaul (220–330 ft.)

sample #	UI 0	UI 1	UI 2	UI 3	UI 4
0	0x00	0x45	0x00	0x00	0x00
1	0x0A	0x44	0x00	0x00	0x00
2	0x36	0x43	0x00	0x00	0x00
3	0x36	0x41	0x00	0x00	0x00
4	0x34	0x40	0x00	0x00	0x00
5	0x34	0x40	0x00	0x00	0x00
6	0x30	0x00	0x00	0x00	0x00
7	0x2F	0x00	0x00	0x00	0x00
8	0x2E	0x00	0x00	0x00	0x00
9	0x2D	0x00	0x00	0x00	0x00
10	0x2C	0x00	0x00	0x00	0x00
11	0x2B	0x00	0x00	0x00	0x00
12	0x2A	0x00	0x00	0x00	0x00
13	0x29	0x00	0x00	0x00	0x00
14	0x23	0x00	0x00	0x00	0x00
15	0x4A	0x00	0x00	0x00	0x00
16	0x60	0x00	0x00	0x00	0x00
17	0x55	0x00	0x00	0x00	0x00
18	0x53	0x00	0x00	0x00	0x00
19	0x50	0x00	0x00	0x00	0x00
20	0x4E	0x00	0x00	0x00	0x00
21	0x4C	0x00	0x00	0x00	0x00
22	0x48	0x00	0x00	0x00	0x00
23	0x47	0x00	0x00	0x00	0x00
Scale *					
front I/O	0x12				
rear I/O	TBD				

*Value of XLPG line driver configuration (register: 0F0H)

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9-4. Transmit Waveform Values for T1 Shorthaul (440–550 ft.)

Table 9-4 Transmit Waveform Values for T1 Shorthaul (440–550 ft.)

sample #	UI 0	UI 1	UI 2	UI 3	UI 4
0	0x00	0x46	0x00	0x00	0x00
1	0x0A	0x45	0x00	0x00	0x00
2	0x3A	0x43	0x00	0x00	0x00
3	0x3A	0x41	0x00	0x00	0x00
4	0x37	0x40	0x00	0x00	0x00
5	0x37	0x40	0x00	0x00	0x00
6	0x2F	0x00	0x00	0x00	0x00
7	0x2E	0x00	0x00	0x00	0x00
8	0x2D	0x00	0x00	0x00	0x00
9	0x2C	0x00	0x00	0x00	0x00
10	0x2B	0x00	0x00	0x00	0x00
11	0x2A	0x00	0x00	0x00	0x00
12	0x29	0x00	0x00	0x00	0x00
13	0x28	0x00	0x00	0x00	0x00
14	0x19	0x00	0x00	0x00	0x00
15	0x4A	0x00	0x00	0x00	0x00
16	0x64	0x00	0x00	0x00	0x00
17	0x57	0x00	0x00	0x00	0x00
18	0x53	0x00	0x00	0x00	0x00
19	0x4F	0x00	0x00	0x00	0x00
20	0x4C	0x00	0x00	0x00	0x00
21	0x4b	0x00	0x00	0x00	0x00
22	0x48	0x00	0x00	0x00	0x00
23	0x47	0x00	0x00	0x00	0x00
Scale *					
front I/O	0x13				
rear I/O	TBD				

*Value of XLPG line driver configuration (register: 0F0H)

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9-5. Transmit Waveform Values for T1 Shorthaul (550–660 ft.)

Table 9-5 Transmit Waveform Values for T1 Shorthaul (550–660 ft.)

sample #	UI 0	UI 1	UI 2	UI 3	UI 4
0	0x00	0x46	0x00	0x00	0x00
1	0x0A	0x45	0x00	0x00	0x00
2	0x3F	0x43	0x00	0x00	0x00
3	0x3F	0x41	0x00	0x00	0x00
4	0x3F	0x40	0x00	0x00	0x00
5	0x3F	0x40	0x00	0x00	0x00
6	0x2E	0x00	0x00	0x00	0x00
7	0x2E	0x00	0x00	0x00	0x00
8	0x2A	0x00	0x00	0x00	0x00
9	0x29	0x00	0x00	0x00	0x00
10	0x28	0x00	0x00	0x00	0x00
11	0x27	0x00	0x00	0x00	0x00
12	0x26	0x00	0x00	0x00	0x00
13	0x25	0x00	0x00	0x00	0x00
14	0x24	0x00	0x00	0x00	0x00
15	0x4A	0x00	0x00	0x00	0x00
16	0x7F	0x00	0x00	0x00	0x00
17	0x63	0x00	0x00	0x00	0x00
18	0x53	0x00	0x00	0x00	0x00
19	0x51	0x00	0x00	0x00	0x00
20	0x4C	0x00	0x00	0x00	0x00
21	0x4B	0x00	0x00	0x00	0x00
22	0x48	0x00	0x00	0x00	0x00
23	0x47	0x00	0x00	0x00	0x00
Scale *					
front I/O	0x15				
rear I/O	TBD				

*Value of XLPG line driver configuration (register: 0F0H)

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9-6. Transmit Waveform Values for T1 Long Haul (LBO 0 dB)

Table 9-6 Transmit Waveform Values for T1 Long Haul (LBO 0 dB)

sample #	UI 0	UI 1	UI 2	UI 3	UI 4
0	0x00	0x44	0x00	0x00	0x00
1	0x0A	0x44	0x00	0x00	0x00
2	0x20	0x43	0x00	0x00	0x00
3	0x32	0x43	0x00	0x00	0x00
4	0x3E	0x42	0x00	0x00	0x00
5	0x3D	0x42	0x00	0x00	0x00
6	0x3C	0x41	0x00	0x00	0x00
7	0x3B	0x41	0x00	0x00	0x00
8	0x3A	0x00	0x00	0x00	0x00
9	0x39	0x00	0x00	0x00	0x00
10	0x39	0x00	0x00	0x00	0x00
11	0x38	0x00	0x00	0x00	0x00
12	0x37	0x00	0x00	0x00	0x00
13	0x36	0x00	0x00	0x00	0x00
14	0x34	0x00	0x00	0x00	0x00
15	0x29	0x00	0x00	0x00	0x00
16	0x4F	0x00	0x00	0x00	0x00
17	0x4C	0x00	0x00	0x00	0x00
18	0x4A	0x00	0x00	0x00	0x00
19	0x49	0x00	0x00	0x00	0x00
20	0x47	0x00	0x00	0x00	0x00
21	0x47	0x00	0x00	0x00	0x00
22	0x46	0x00	0x00	0x00	0x00
23	0x46	0x00	0x00	0x00	0x00
Scale *					
front I/O	0x0C				
rear I/O	TBD				

*Value of XLPG line driver configuration (register: 0F0H)

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9-7. Transmit Waveform Values for T1 Long Haul (LBO 7.5 dB)

Table 9-7 Transmit Waveform Values for T1 Long Haul (LBO 7.5 dB)

sample #	UI 0	UI 1	UI 2	UI 3	UI 4
0	0x00	0x10	0x00	0x00	0x00
1	0x01	0x0E	0x00	0x00	0x00
2	0x02	0x0C	0x00	0x00	0x00
3	0x04	0x0A	0x00	0x00	0x00
4	0x08	0x08	0x00	0x00	0x00
5	0x0C	0x06	0x00	0x00	0x00
6	0x10	0x04	0x00	0x00	0x00
7	0x16	0x02	0x00	0x00	0x00
8	0x1A	0x01	0x00	0x00	0x00
9	0x1E	0x00	0x00	0x00	0x00
10	0x22	0x00	0x00	0x00	0x00
11	0x26	0x00	0x00	0x00	0x00
12	0x2A	0x00	0x00	0x00	0x00
13	0x2B	0x00	0x00	0x00	0x00
14	0x2C	0x00	0x00	0x00	0x00
15	0x2D	0x00	0x00	0x00	0x00
16	0x2C	0x00	0x00	0x00	0x00
17	0x28	0x00	0x00	0x00	0x00
18	0x24	0x00	0x00	0x00	0x00
19	0x20	0x00	0x00	0x00	0x00
20	0x1C	0x00	0x00	0x00	0x00
21	0x18	0x00	0x00	0x00	0x00
22	0x14	0x00	0x00	0x00	0x00
23	0x12	0x00	0x00	0x00	0x00
Scale *					
front I/O	0x07				
rear I/O	TBD				

*Value of XLPG line driver configuration (register: 0F0H)

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9-8. Transmit Waveform Values for T1 Long Haul (LBO 15 dB)

Table 9-8 Transmit Waveform Values for T1 Long Haul (LBO 15 dB)

sample #	UI 0	UI 1	UI 2	UI 3	UI 4
0	0x00	0x2A	0x09	0x01	0x00
1	0x00	0x28	0x08	0x01	0x00
2	0x00	0x26	0x08	0x01	0x00
3	0x00	0x24	0x07	0x01	0x00
4	0x01	0x22	0x07	0x01	0x00
5	0x02	0x20	0x06	0x01	0x00
6	0x04	0x1E	0x06	0x01	0x00
7	0x07	0x1C	0x05	0x00	0x00
8	0x0A	0x1B	0x05	0x00	0x00
9	0x0D	0x19	0x05	0x00	0x00
10	0x10	0x18	0x04	0x00	0x00
11	0x14	0x16	0x04	0x00	0x00
12	0x18	0x15	0x04	0x00	0x00
13	0x1B	0x13	0x03	0x00	0x00
14	0x1E	0x12	0x03	0x00	0x00
15	0x21	0x10	0x03	0x00	0x00
16	0x24	0x0F	0x03	0x00	0x00
17	0x27	0x0D	0x03	0x00	0x00
18	0x2A	0x0D	0x02	0x00	0x00
19	0x2D	0x0B	0x02	0x00	0x00
20	0x30	0x0B	0x02	0x00	0x00
21	0x30	0x0A	0x02	0x00	0x00
22	0x2E	0x0A	0x02	0x00	0x00
23	0x2C	0x09	0x02	0x00	0x00

Scale *	
front I/O	0x03
rear I/O	TBD

*Value of XLPG line driver configuration (register: 0F0H)

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9-9. Transmit Waveform Values for T1 Long Haul (LBO 22.5 dB)

Table 9-9 Transmit Waveform Values for T1 Long Haul (LBO 22.5 dB)

sample #	UI 0	UI 1	UI 2	UI 3	UI 4
0	0x00	0x1F	0x16	0x06	0x01
1	0x00	0x20	0x15	0x05	0x01
2	0x00	0x21	0x15	0x05	0x01
3	0x00	0x22	0x14	0x05	0x01
4	0x00	0x22	0x13	0x04	0x00
5	0x00	0x23	0x12	0x04	0x00
6	0x01	0x23	0x12	0x04	0x00
7	0x01	0x24	0x11	0x03	0x00
8	0x01	0x23	0x10	0x03	0x00
9	0x02	0x23	0x10	0x03	0x00
10	0x03	0x22	0x0F	0x03	0x00
11	0x05	0x22	0x0E	0x03	0x00
12	0x07	0x21	0x0E	0x02	0x00
13	0x09	0x20	0x0D	0x02	0x00
14	0x0B	0x1E	0x0C	0x02	0x00
15	0x0E	0x1D	0x0C	0x02	0x00
16	0x10	0x1B	0x0B	0x02	0x00
17	0x13	0x1B	0x0A	0x02	0x00
18	0x15	0x1A	0x0A	0x02	0x00
19	0x17	0x19	0x09	0x01	0x00
20	0x19	0x19	0x08	0x01	0x00
21	0x1B	0x18	0x08	0x01	0x00
22	0x1D	0x17	0x07	0x01	0x00
23	0x1E	0x17	0x06	0x01	0x00
Scale *					
front I/O	0x02				
rear I/O	TBD				

*Value of XLPG line driver configuration (register: 0F0H)

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9-10. Transmit Waveform Values for E1 Long Haul (120 Ohms)

Table 9-10 Transmit Waveform Values for E1 Long Haul (120 Ohms)

sample #	UI 0	UI 1	UI 2	UI 3	UI 4
0	0x00	0x00	0x00	0x00	0x00
1	0x00	0x00	0x00	0x00	0x00
2	0x0A	0x00	0x00	0x00	0x00
3	0x3F	0x00	0x00	0x00	0x00
4	0x3F	0x00	0x00	0x00	0x00
5	0x39	0x00	0x00	0x00	0x00
6	0x38	0x00	0x00	0x00	0x00
7	0x36	0x00	0x00	0x00	0x00
8	0x36	0x00	0x00	0x00	0x00
9	0x35	0x00	0x00	0x00	0x00
10	0x35	0x00	0x00	0x00	0x00
11	0x35	0x00	0x00	0x00	0x00
12	0x35	0x00	0x00	0x00	0x00
13	0x35	0x00	0x00	0x00	0x00
14	0x2D	0x00	0x00	0x00	0x00
15	0x00	0x00	0x00	0x00	0x00
16	0x00	0x00	0x00	0x00	0x00
17	0x00	0x00	0x00	0x00	0x00
18	0x00	0x00	0x00	0x00	0x00
19	0x00	0x00	0x00	0x00	0x00
20	0x00	0x00	0x00	0x00	0x00
21	0x00	0x00	0x00	0x00	0x00
22	0x00	0x00	0x00	0x00	0x00
23	0x00	0x00	0x00	0x00	0x00
Scale *					
front I/O	0x0C				
rear I/O	TBD				

*Value of XLPG line driver configuration (register: 0F0H)

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9-11. Transmit Waveform Values for E1 Long Haul (75 Ohms)

Table 9-11 Transmit Waveform Values for E1 Long Haul (75 Ohms)

sample #	UI 0	UI 1	UI 2	UI 3	UI 4
0	0x00	0x00	0x00	0x00	0x00
1	0x00	0x00	0x00	0x00	0x00
2	0x0A	0x00	0x00	0x00	0x00
3	0x3E	0x00	0x00	0x00	0x00
4	0x3E	0x00	0x00	0x00	0x00
5	0x3E	0x00	0x00	0x00	0x00
6	0x3C	0x00	0x00	0x00	0x00
7	0x3C	0x00	0x00	0x00	0x00
8	0x3A	0x00	0x00	0x00	0x00
9	0x3A	0x00	0x00	0x00	0x00
10	0x3A	0x00	0x00	0x00	0x00
11	0x3A	0x00	0x00	0x00	0x00
12	0x3A	0x00	0x00	0x00	0x00
13	0x3A	0x00	0x00	0x00	0x00
14	0x35	0x00	0x00	0x00	0x00
15	0x00	0x00	0x00	0x00	0x00
16	0x00	0x00	0x00	0x00	0x00
17	0x00	0x00	0x00	0x00	0x00
18	0x00	0x00	0x00	0x00	0x00
19	0x00	0x00	0x00	0x00	0x00
20	0x00	0x00	0x00	0x00	0x00
21	0x00	0x00	0x00	0x00	0x00
22	0x00	0x00	0x00	0x00	0x00
23	0x00	0x00	0x00	0x00	0x00
Scale *					
front I/O	0x0C				
rear I/O	TBD				

*Value of XLPG line driver configuration (register: 0F0H)

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10. Appendix C: T1 /E1 Equalization Data Tables

Table 10-1 T1 equalization data

First RLPS Equalization Indirect Address Register	Last RLPS Equalization Indirect Address Register	RLPS Indirect Data (0xD8)	RLPS Indirect Data (0xD9)	RLPS Indirect Data (0xDA)	RLPS Indirect Data (0xDB)
0	0	0x3	0xFE	0x18	0x40
1	1	0x3	0xF6	0x18	0x40
2	2	0x3	0xEE	0x18	0x40
3	3	0x3	0xE6	0x18	0x40
4	4	0x3	0xDE	0x18	0x40
5	7	0x3	0xD6	0x18	0x40
8	11	0x3	0xCE	0x18	0x40
12	14	0x3	0xC6	0x18	0x40
15	18	0x3	0xBE	0x18	0x40
19	22	0x3	0xB6	0x18	0x40
23	23	0x3	0xAE	0x18	0x38
24	24	0x3	0xAE	0x18	0x3C
25	28	0x3	0xAE	0x18	0x40
29	29	0x0B	0xB6	0x18	0xB8
30	30	0x0B	0xAE	0x18	0xB8
31	31	0x0B	0xAE	0x18	0xBC
32	33	0x0B	0xAE	0x18	0xC0
34	37	0x0B	0xA6	0x18	0xC0
38	38	0x13	0xA6	0x18	0xC0
39	43	0x13	0x9E	0x18	0xC0
44	45	0x1B	0x96	0x18	0xC0
46	46	0x1B	0x8E	0x18	0xC0
47	47	0x23	0x8E	0x18	0xC0
48	50	0x27	0x96	0x19	0x40
51	53	0x2F	0x9E	0x19	0xC0
54	54	0x2F	0xA6	0x1A	0x40

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Table 10-1 T1 equalization data (continued)

First RLPS Equalization Indirect Address Register	Last RLPS Equalization Indirect Address Register	RLPS Indirect Data (0xD8)	RLPS Indirect Data (0xD9)	RLPS Indirect Data (0xDA)	RLPS Indirect Data (0xDB)
55	55	0x3F	0xA6	0x1A	0x40
56	57	0x2F	0xA6	0x1A	0x40
58	61	0x2F	0x96	0x19	0xC0
62	64	0x37	0x9E	0x1A	0x40
65	67	0x37	0x96	0x1A	0x40
68	68	0x3F	0x96	0x1A	0x40
69	73	0x3F	0x8E	0x1A	0x40
74	78	0x47	0x86	0x1A	0x40
79	84	0x47	0x86	0x1A	0xC0
85	89	0x47	0x7E	0x1A	0xC0
90	92	0x4F	0x7E	0x2A	0xC0
93	93	0x57	0x7E	0x2A	0xC0
94	98	0x57	0x76	0x2A	0xC0
99	101	0x57	0x6E	0x2A	0xC0
102	102	0x5F	0x6E	0x2A	0xC0
103	106	0x5F	0x6E	0x3A	0xC0
107	108	0x67	0x66	0x3A	0xC0
109	112	0x67	0x66	0x4A	0xC0
113	118	0x6E	0x66	0x5A	0xC0
119	121	0x6E	0x7E	0x6B	0x40
122	124	0x6E	0x76	0x6B	0x40
125	127	0x76	0x6E	0x6B	0x3C
128	130	0x7E	0x66	0x6B	0x40
131	131	0x86	0x6E	0x6B	0xB3
132	133	0x86	0x6E	0x6B	0xC0
134	136	0x86	0x66	0x8B	0x8E
137	139	0x8E	0x66	0x9B	0x8E
140	143	0x8E	0x66	0x9B	0x3C
144	145	0x96	0x66	0xAB	0x3C

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Table 10-1 T1 equalization data (continued)

First RLPS Equalization Indirect Address Register	Last RLPS Equalization Indirect Address Register	RLPS Indirect Data (0xD8)	RLPS Indirect Data (0xD9)	RLPS Indirect Data (0xDA)	RLPS Indirect Data (0xDB)
146	148	0x96	0x5E	0xAB	0x3C
149	151	0x9E	0x5E	0xBB	0x3A
152	154	0x9E	0x5E	0xBB	0x40
155	156	0x9E	0x56	0xBB	0x3C
157	157	0xA6	0x56	0xBB	0x3C
158	160	0xA6	0x56	0xBB	0x40
161	163	0xA6	0x56	0xBB	0x47
164	166	0xA6	0x5C	0xBB	0x3C
167	169	0xAE	0x5C	0xBB	0x40
170	172	0xAE	0x54	0xBB	0x3C
173	175	0xB6	0x52	0xBB	0x3C
176	179	0xB6	0x52	0xBB	0x40
180	180	0xB6	0x52	0xDB	0x40
181	182	0xBE	0x52	0xDB	0x40
183	185	0xBE	0x4A	0xDB	0x3C
186	187	0xC6	0x4A	0xDB	0x40
188	188	0xC6	0x4A	0xDB	0xAF
189	189	0xC6	0x4A	0xDB	0xB2
190	191	0xC6	0x4A	0xDB	0xB8
192	194	0xCD	0x4A	0xD7	0xB6
195	197	0xD5	0x4A	0xD7	0xBA
198	200	0xD5	0x4A	0xD7	0xC0
201	202	0xD4	0x42	0xD7	0xB8
203	203	0xDC	0x42	0xD7	0xB8
204	206	0xDC	0x42	0xD7	0xC4
207	208	0xDD	0x42	0xD7	0xC8
209	209	0xE5	0x42	0xD7	0xC8
210	214	0xE5	0x3A	0xD7	0xC0
215	215	0xED	0x3A	0xF7	0xC0

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Table 10-1 T1 equalization data (continued)

First RLPS Equalization Indirect Address Register	Last RLPS Equalization Indirect Address Register	RLPS Indirect Data (0xD8)	RLPS Indirect Data (0xD9)	RLPS Indirect Data (0xDA)	RLPS Indirect Data (0xDB)
216	218	0xED	0x34	0xF7	0xBD
219	219	0xED	0x35	0x17	0xBA
220	221	0xEC	0x35	0x17	0xBA
222	224	0xEC	0x35	0x27	0xBA
225	227	0xF4	0x35	0x37	0xBD
228	228	0xF4	0x35	0x33	0xB7
229	230	0xF4	0x35	0x33	0xBA
231	233	0xFC	0x35	0x33	0xBE
234	236	0xFC	0x35	0x33	0xC0
237	239	0xFC	0x2D	0x33	0xBD
240	255	0xFC	0x2D	0x33	0xC0

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Table 10-2 E1 equalization data

First RLPS Equalization Indirect Address Register	Last RLPS Equalization Indirect Address Register	RLPS Indirect Data (0xD8)	RLPS Indirect Data (0xD9)	RLPS Indirect Data (0xDA)	RLPS Indirect Data (0xDB)
0	1	0x06	0xD6	0x3C	0x10
2	2	0x06	0xCE	0x3C	0x10
3	3	0x06	0xC6	0x3C	0x10
4	6	0x06	0xC6	0x3C	0x2C
7	9	0x06	0xC6	0x4C	0x10
10	1	0x06	0xC6	0x5C	0x10
13	15	0x06	0xCE	0x6C	0x2C
16	18	0x06	0xCE	0x7C	0x2C
19	21	0x06	0xD6	0x8C	0x2C
22	24	0x06	0xD6	0x9C	0x2C
25	27	0x06	0xD6	0xAC	0x2C
28	30	0x06	0xD6	0xBC	0x2C
31	33	0x06	0xD6	0xCC	0x2C
34	36	0x06	0xCE	0xBC	0x2C
37	39	0x06	0xCE	0xCC	0x2C
40	42	0x06	0xCE	0xDC	0x1F
43	45	0x06	0xCE	0xEC	0x1F
46	48	0x0E	0xCE	0xFC	0x1F
49	51	0x0E	0xC6	0xFC	0x05
52	54	0x0E	0xBE	0xFC	0x05
55	57	0x16	0xBE	0xFC	0x2C
58	60	0x16	0xB6	0xFC	0x1A
61	63	0x1E	0xAE	0xFC	0x10
64	66	0x1E	0xB6	0xF8	0x2C
67	69	0x26	0xAE	0xF8	0x1F
70	71	0x26	0xA6	0xF8	0x1F
72	72	0x2E	0x9E	0xF8	0x10
73	73	0x2E	0x9E	0xF8	0x1F

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Table 10-2 E1 equalization data (continued)

First RLPS Equalization Indirect Address Register	Last RLPS Equalization Indirect Address Register	RLPS Indirect Data (0xD8)	RLPS Indirect Data (0xD9)	RLPS Indirect Data (0xDA)	RLPS Indirect Data (0xDB)
74	74	0x2E	0x9F	0x08	0x18
75	75	0x2F	0x9E	0xF8	0x10
76	76	0x2F	0x9E	0xF8	0x1C
77	81	0x37	0x9E	0xF8	0x2C
82	84	0x37	0xB4	0xF8	0x17
85	87	0x37	0xAC	0xF8	0x0A
88	88	0x37	0xA4	0xF8	0x05
89	90	0x3F	0xA4	0xF8	0x05
91	91	0x3F	0xA4	0xF8	0x0A
92	93	0x3F	0x9C	0xF8	0x5
94	94	0x3F	0x9C	0xF8	0x19
95	96	0x47	0x9C	0xF8	0x19
97	99	0x47	0x9C	0xF8	0x27
100	100	0x47	0x94	0xF8	0x1F
101	102	0x4F	0x94	0xF8	0x1F
103	108	0x4F	0x8C	0xF8	0x20
109	109	0x4F	0x84	0xF8	0x2C
110	111	0x57	0x84	0xF8	0x2C
112	114	0x57	0x7C	0xF8	0x20
115	117	0x5F	0x74	0xF8	0x27
118	120	0x5F	0x74	0xF8	0x2F
121	123	0x67	0x6C	0xF8	0x2F
124	124	0x67	0x6C	0xF8	0x3C
125	126	0x6F	0x6C	0xF8	0x3C
127	129	0x6F	0x64	0xF8	0x38
130	131	0x6F	0x6C	0xF8	0xA9
132	132	0x77	0x6C	0xF8	0xB0
133	133	0x77	0x6C	0xF8	0xB7
134	135	0x77	0x6C	0xF8	0xBC

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Table 10-2 E1 equalization data (continued)

First RLPS Equalization Indirect Address Register	Last RLPS Equalization Indirect Address Register	RLPS Indirect Data (0xD8)	RLPS Indirect Data (0xD9)	RLPS Indirect Data (0xDA)	RLPS Indirect Data (0xDB)
136	136	0x75	0x54	0xF8	0xA9
137	138	0x7D	0x54	0xF8	0xA9
139	141	0x7D	0x54	0xF8	0xAD
142	144	0x7D	0x4C	0xF8	0xA6
145	145	0x7D	0x4C	0xF8	0xAF
146	147	0x85	0x4C	0xF8	0xAF
148	150	0x85	0x54	0xF9	0x2F
151	151	0x85	0x54	0xF9	0x3C
152	153	0x8D	0x54	0xF9	0x3C
154	156	0x8D	0x54	0xF9	0xAD
157	157	0x8D	0x54	0xF9	0xB3
158	165	0x95	0x54	0xF9	0xB3
166	168	0x95	0x54	0xFA	0x95
169	171	0x95	0x54	0xFA	0x9A
172	172	0x95	0x54	0xFA	0x9E
173	174	0x9D	0x54	0xFA	0xA1
175	175	0x9D	0x4C	0xFA	0x9D
176	176	0x9D	0x4C	0xFA	0xA1
177	177	0xA5	0x4C	0xFA	0xA1
178	179	0xA5	0x4D	0x2A	0x27
180	180	0xA5	0x4D	0x2A	0x2F
181	181	0xAD	0x4D	0x2A	0x2F
182	183	0xAD	0x49	0x2A	0x27
184	184	0xAD	0x49	0x2A	0x2F
185	185	0xB5	0x49	0x2A	0x2F
186	186	0xB5	0x41	0x2A	0x26
187	187	0xB5	0x41	0x2A	0x29
188	189	0xB5	0x41	0x2A	0x30
190	191	0xBD	0x49	0x2B	0x20

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Table 10-2 E1 equalization data (continued)

First RLPS Equalization Indirect Address Register	Last RLPS Equalization Indirect Address Register	RLPS Indirect Data (0xD8)	RLPS Indirect Data (0xD9)	RLPS Indirect Data (0xDA)	RLPS Indirect Data (0xDB)
192	193	0xBD	0x49	0x2B	0x24
194	194	0xC5	0x51	0x2B	0x9E
195	195	0xC5	0x51	0x2B	0xA2
196	197	0xC5	0x51	0x2B	0xA7
198	198	0xC5	0x49	0x2B	0xA0
199	199	0xCD	0x49	0x2B	0xA3
200	201	0xCD	0x49	0x2B	0xAA
202	203	0xD5	0x41	0x2B	0xA6
204	205	0xD5	0x41	0x2B	0xA9
206	207	0xDD	0x39	0x2B	0xA3
208	208	0xDD	0x39	0x2B	0xA5
209	209	0xDD	0x39	0x2B	0xA6
210	210	0xDD	0x39	0x2B	0xA7
211	215	0xE5	0x41	0x33	0xA4
216	217	0xE5	0x41	0x33	0xAA
218	218	0xE5	0x39	0x33	0xA4
219	219	0xED	0x39	0x33	0xA4
220	221	0xED	0x39	0x33	0xA8
222	223	0xF5	0x31	0x33	0xA2
224	225	0xF5	0x31	0x33	0xA8
226	226	0xF4	0x31	0x43	0xA8
227	227	0xFC	0x31	0x43	0xA8
228	229	0xFC	0x31	0x43	0xAD
230	231	0xFC	0x29	0x43	0xA5
232	233	0xFC	0x29	0x43	0xAC
234	235	0xFC	0x21	0x43	0xA0
236	237	0xFC	0x21	0x43	0xA6
238	239	0xFC	0x21	0x53	0xA6
240	241	0xFC	0x21	0x53	0xAC

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Table 10-2 E1 equalization data (continued)

First RLPS Equalization Indirect Address Register	Last RLPS Equalization Indirect Address Register	RLPS Indirect Data (0xD8)	RLPS Indirect Data (0xD9)	RLPS Indirect Data (0xDA)	RLPS Indirect Data (0xDB)
242	242	0xFC	0x19	0x53	0x9A
243	243	0xFC	0x19	0x53	0x9B
244	244	0xFC	0x19	0x53	0x9C
245	245	0xFC	0x19	0x53	0x9D
246	246	0xFC	0x19	0x53	0x9E
247	247	0xFC	0x19	0x53	0x9F
248	248	0xFC	0x19	0x53	0xA0
249	249	0xFC	0x19	0x53	0xA1
250	250	0xFC	0x19	0x53	0xA2
251	251	0xFC	0x19	0x53	0xA3
252	252	0xFC	0x19	0x53	0xA4
253	253	0xFC	0x19	0x53	0xA5
254	255	0xFC	0x19	0x53	0xA6

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