Model 234X
IEEE 1394 PCI, PMC & CompactCPI Host Bus Adapters (HBAs)

Hardware Manual

2341 PCI

2342 PCI Power Provider

2343 PMC

2344 CompactPCI

2344-CC CompactPCI with conduction cooling

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Preface

This manual describes SBS Model 234X adapters that provide an IEEE 1394 Open Host Controller Interface (OHCI) on PCI, CompactPCI (cPCI) and PMC buses. It includes information about the adapter's operation, installation, and configuration.

To simplify installation and eliminate operation problems, SBS recommends that you review this manual before beginning to install your new adapter card.

- Chapter 1 provides an overview of the adapter, product description, specifications and requirements, and supporting products.
- Chapter 2 gets you started with information about unpacking the adapter package, adapter installation, Help, and additional references.
- Appendices – There are two appendices for quick reference: a glossary of terms and a IEEE 1394 reference.

➔ Important Notes:

- Make sure you follow proper ESD handling procedures (refer to EIA-625, ESD Association Handbook, or MIL-HDBK-263) when working with cards and components.

Be sure power is OFF the host system before installing the adapter card.

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Chapter 1: Introduction

➔ In this manual, all references to PCI apply to both CompactPCI (cPCI) and PCI. If any text refers to just PCI or cPCI, it will be indicated by "PCI only" or "cPCI only". Also, all references to Model 234X apply to Models 2341, 2342, 2343, 2344, and 2344-CC. If any text refers to just one of the models, that model will be identified.

1.0 Overview

SBS's Model 234X IEEE 1394 adapters are add-in cards that provide 1394 ports to a computer through its I/O expansion bus. Each 234X card has three 400M bits/sec 6-pin 1394 ports that are driven by a Texas Instruments TSB41LV03 physical layer chip; 2344-CC conduction cooled card uses Texas Instruments TSB41AB3i; A Texas Instruments TSB12LV23 (TSB12LV26i for the 2344-CC) OHCI (Open Host Controller Interface) link layer chip provides the host computer link layer. The link layer is accessible from the PCI bus and is the mechanism through which the host computer can access the 1394 bus.

Model 234X adapter cards differ as follows:

- Model 2341, a PCI short form factor card, is a Class 4 self-powered 1394 adapter. It is compliant with the *PCI Local Bus Specification* revision 2.2.
- Model 2342, a PCI short form factor card, is a Class 1 cable power provider 1394 adapter. It is compliant with the *PCI Local Bus Specification* revision 2.2.
- Model 2343 is a PMC card. It is a Class 4 self-powered 1394 adapter. Model 2343 is compliant with the *Common Mezzanine Card/Draft Standard and Environmental Layers for PCI Mezzanine Cards: "PMC"* IEEE 1386/Draft 1.6.
- Model 2344 is a 3U CompactPCI (cPCI) card. It is a Class 4 self-powered 1394 adapter and is compliant with the *CompactPCI Specification* PCIMG 2.0 R2.1.
- Model 2344-CC is a conduction cooled, conformal coated, extended termperature version of the 2344 cPCI 1394 host bus adapter.

Model 234X adapters:

- Compliant with *IEEE 1394-1995*, *IEEE 1394a*, and *OHCI* Revision 1.0 specifications.
- Capable of 400M bits/sec, 200M bits/sec, and 100M bits/sec operation. Devices capable of any of these speeds can be interconnected.
- Support 32-bit transfers at PCI clock speeds up to 33 MHz.

Model 2344-CC adapters:

- Compliant with *IEEE 1394A-2000*, *IEEE 1394a*, and *OHCI* Revision 1.0 specifications.

Internal control registers are memory mapped and non-prefetchable, as required by the OHCI specification. The PCI configuration header is accessed via configuration cycles specified by PCI, and provides Plug-and-Play (PnP) compatibility. All Model 234X adapters can transfer a cacheline of data at 132M Bytes/sec after connection to a memory controller. Because PCI latency can be large, deep FIFOs are provided to buffer the 1394 data. Physical write posting buffers are provided as well as a physical data path for optimized SBP-2 performance. Model 234X adapters support multiple isochronous contexts, multiple cacheline burst transfers, and advanced internal arbitration.

➔ Additional programming information and register maps are found in the OHCI rev. 1.0 specification and the Texas Instrument TSB12LV23 Data manual available from TI: Texas Instrument Literature # SLLS328A.

➔ 2344-CC: Additional programming information and register maps are found in the OHCI rev. 1.0 specification and the Texas Instrument TSB12LV26i Data manual available from TI: Texas Instrument Literature # SLLS366C.

1.1 Isolation And Power Classes

Certain classes of 1394 cards can draw power through the 6-wire cable even when the host computer is powered down. These cards' PHY chip acts as a repeater so that other 1394 network nodes can continue to communicate through the unpowered node. All Model 234X adapters support full galvanic isolation that prevents a ground loop to occur if two cards in the 1394 tree have different chassis grounds.

There are several power classes for the 1394 bus. The power class indicates whether a card is self-powered, powered from the cable, is a power provider, or some combination of these. SBS Models 2341, 2343, and 2344 are power Class 4 devices -- they provide their own power when the host computer is powered and draw power from the cable when the host is not powered. Although Class 4 adapters can, these adapters do not provide power to other 1394 devices. Model 2342, a power Class 1 device, can provide up to 20 watts of power to the 1394 cable but cannot be powered from the cable when its host computer is powered down. Model 2344-CC is Power Class 0; it provides its own power and does not provide or take power from the cable.

1.2 Adapter Features

OHCI
The OHCI implements the 1394 link layer protocol plus supports the transaction and bus management layers. OHCI also includes FIFOs and DMA engines for high-performance data transfers.

EEPROM
PCI and 1394 configuration information is stored in the 8K serial EEPROM. The OHCI automatically loads this information at power up.

PHY
The PHY provides three 400M bit/sec 1394 serial bus interfaces.

Conformance:
- IEEE 1394-1995 specifications (234X cards)
- IEEE 1394A-2000 specifications (2344-CC)
- FCC Class A approved.
- CE Marked in compliance with EMC Directive 89/336/EEC: CISPR 22/EN 55022 Class A for emissions; EN 50082-2 (heavy industrial) for immunities.
- Recognized under the component program of Underwriters Laboratories, Inc.

1.2.1 Environment: 2341, 2342, 2343 & 2344

Temperature: 0º to 60º C operating;
-40º to 85º C storage.

Humidity: 0% to 90% non-condensing.

1.2.2 Environment: 2344-CC

Temperature: -40º to +85º C operating;
-55º to +105º C storage.

Humidity: 0% to 90% non-condensing.

1.3 Cables

The 234X adapters require standard 6-pin IEEE 1394A cable containing three twisted pair sets. Maximum cable length is 4.5 meters. *All cables are purchased separately so that you can order the appropriate length for your application.*

2344-CC provides three 1394 ports to CompactPCI connector P2 as rear I/O. It does not use stnadard 1394A 6-pin cables. The three rear I/O 1394A ports may be connected to a specialized 1394 cable at the back of the backplane connector P2, or may be routed on the CompactPCI backplane to their final destinations. This specialized cabeling or backplane routing must conform to requirements defined in the IEEE 1394A-2000 specificiation. See a Appendix B for information about the pins used.

Chapter 2: Getting Started & Installation

Make sure you follow proper ESD handling procedures (refer to EIA-625, ESD Association Handbook, or MIL-HDBK-263) when working with cards and components.

2.0 Unpacking

The SBS Model 234X adapter package contains the following items. Please identify each item and notify SBS (651-905-4700) if any are missing.

- One 1394 circuit card:

Model 2341 PCI	Part Number: 85908470
Model 2342 PCI Power Provider	Part Number: 85908471
Model 2343 PMC	Part Number: 85905230
Model 2344 CompactPCI	Part Number: 85907340
Model 2344-CC CompactPCI	Part Number: 85903226

- Model 234X manual - Part Number: 85905290
- One 1394 I/O cable (purchased separately)

➔ Eight-digit part numbers with card revision level are printed on white labels affixed to the adapter cards.

2.1 Help!

Please have the following items and information handy when calling SBS for technical support:

- Model number and revision level of the adapter, or the serial number located on the white bar code label on the adapter card.
- Configuration information.
- This manual.

Technical support is available from 9:00 a.m. - 5:00 p.m. (Central Time) Monday - Friday, excluding holidays.

Contact SBS at:

Mailing Address:	SBS Technologies, Inc. 1284 Corporate Center Drive St. Paul, MN 55121-1245
Phone:	651-905-4700
Fax:	651-905-4701
Email:	support.commercial@sbs.com
Web:	www.sbs.com

2.2 Hardware Installation

➔ Observe static safety precautions to prevent damage to the cards.

➔ Make sure power is *off* to the computer system before installing the adapter card.

2.2.1 Model 2341 PCI & Model 2342 PCI Power Provider Cards Installation

1. Locate a vacant PCI card slot in the PCI chassis.
2. Remove the metal plate that covers the cable exit at the rear of the chassis.
3. Insert the PCI adapter card into the connector.
4. Fasten the adapter card in place with the mounting screw.
5. Model 2342 requires that a standard 4-pin disk drive cable be plugged into the cable connector located on the top of the card.

2.2.2 Model 2343 PMC Card Installation

1. Insert the card in the host Single Board Computer's PMC connector.
2. Make sure the card is firmly seated.

2.2.3 Model 2344 cPCI Card Installation

1. Locate a vacant 3U peripheral cPCI card slot in the cPCI backplane.
2. Insert the cPCI adapter card into the connector of the selected slot.
3. Make sure the card is firmly seated.

2.2.4 Model 2344-CC Card Installation

➔ 2344-CC card must be installed in a cPCI with rear I/O connection.

➔ If the card is to be used with a PMC, the PMC must be installed and screwed onto the conduction cooling frame.

2.2.5 Connecting The Adapter Cable

➔ The 1394 cable can be installed or removed when power is on. When the cable is plugged in or when a device on the cable is powered up, a 1394 reset occurs to reconfigure the 1394 bus for the new device.

➔ The 1394 cable used must have 6-pin connectors, except for with the 2344-CC. See Appendix B.

1. Plug one end of the 1394 cable onto any of the adapter card's three cable connectors.
2. Plug the other end of the cable into the peripheral or device to be accessed via 1394.
3. Make sure no loops exist in the 1394 cabling since the 1394 signal is point-to-point (there must be exactly one path between any two devices on the 1394 bus).

2.3 Powering Up The System

Because 1394 reconfigures itself each time changes occur in the bus configuration, no restrictions exist for power up. The host, the adapter card, or any other independently powered devices on the 1394 bus may have power applied in any order.

2.4 Additional References

- *Data Format and Bus Compatibility in Multiprocessors*, IEEE Micro, August 1983, is available from IEEE Micro, PO Box 3014, Los Alamitos, CA 90720-1264.
- 1394 OHCI "Open Host Interface Controller" Specification; http://developer.intel.com/technology/1394/sepcs.htm
- Data sheets for TI TSB12LV26i OHCL Lynx and TSB4119B3 receiver are available at the Texas Instruments web site www.ti.com.
- Data sheets for TI TSB12LV23 OHCL Lynx and TSB41LV03 Three port receiver are available at the Texas Instruments web site www.ti.com.

- *IEEE 1394-1995* " Standard for a high performance serial bus" is available from The Institute of Electrical and Electronics Engineers (IEEE), 445 Hoes Lane, Piscataway, NJ 08855-1331.

- *IEEE P1394A-2000,* Draft Standard for a high performance serial bus" is available from The Institute of Electrical and Electronics Engineers (IEEE), 445 Hoes Lane, Piscataway, NJ 08855-1331.

- *ISO/IEC 13213: 1994 ANSI/1EEE Std1212,1994* "Information Technology-Microprocessor Systems-Control and Status Register (CSR) Architecture for Microprocessor Busses " is available from The Institute of Electrical and Electronics Engineers (IEEE), 445 Hoes Lane, Piscataway, NJ 08855-1331.

- *FireWire System Architecture: IEEE 1394;* MindShare, Inc.; Don Anderson; ISBN 0-201-69470-0; Addison-Wesley Books.

- *Texas Instruments TSB12LV23 Data Manual;* Texas Instruments literature number: SLLS328A.

- *Texas Instruments TSB12LV26i Data Manual;* Texas Instruments literature number: SLLS366C.

Appendix A: Glossary

The following terms are used throughout this manual:

"0": Zero.

"1": One.

Asynchronous: A type of transfer that has reliable delivery but no guarantees on latency or bandwidth.

Bit: A single digit in a binary number (0 or 1).

Byte: 8 bits.

EUID: Externally Unique Identifier. A 64-bit number that uniquely identifies a 1394 device. The upper 16-bits are the Organizationally Unique Identifier (OUI) assigned by the IEEE Registration Authority. The lower 48 bits are uniquely assigned to each card by the manufacturer.

Exchanging Interrupts: Sending interrupts to and receiving interrupts from the remote chassis; includes any processing an application should do to acknowledge the receipt of an interrupt.

FIFO: First In First Out. A memory device in which data are retrieved in the same sequence as stored.

G byte: Gigabyte. Two to the thirtieth power (exactly 1,073,741,824 bytes).

Isochronous: A type of transfer that has a reliable latency and guaranteed bandwidth, but no assurance that the data were delivered.

K byte: Kilobyte. Two to the tenth power (exactly 1024) bytes.

Local: Indicates that the resource is on this bus and does not require use of the adapter interface cable to access it.

Longword: 32 bits.

M byte: Megabyte. Two to the twentieth power (exactly 1,048,576) bytes.

M Bytes/sec: Megabytes per second. Exactly 1,000,000 bytes per second.

Memory Mapped Device: A hardware device that allows access to its functionality through memory space. Normal memory instructions can be used to control the device and access its features.

msec: Millisecond. 1/1,000 of a second.

nsec: Nanosecond. 1/1,000,000,000 of a second.

OHCI: Open Host Controller Interface. A standard definition for a 1394 host controller.

Physical Address: The address that is presented to the bus to reference memory locations.

PIO: Programmed I/O; also referred to as random access.

Programmed Interrupts: Interrupts that can be used by applications to synchronize communications between the two buses.

Remote: Indicates that the resource is on the other bus and requires use of the adapter interface cable to access it.

I/O: Any access to the I/O address space that is located in the remote system chassis.

µsec: Microsecond. 1/1,000,000 of a second.

Word: 16 bits; in some specifications 16-bit data are called halfwords.

Appendix B: 2344-CC Pin Use Reference

B.1 Connection To PMC Board Connector P14

PMC_IO1	J14-1	P2-B1	
PMC_IO2	J14-2	P2-B2	
PMC_IO3	J14-3	P2-B3	
PMC_IO4	J14-4	P2-B4	
PMC_IO5	J14-5	P2-B5	
PMC_IO6	J14-6	P2-B6	
PMC_IO7	J14-7	P2-B7	
PMC_IO8	J14-8	P2-B8	
PMC_IO9	J14-9	P2-B9	
PMC_IO10	J14-10	P2-B10	
PMC_IO11	J14-11	P2-B11	
PMC_IO12	J14-12	P2-B12	
PMC_IO13	J14-13	P2-B13	
PMC_IO14	J14-14	P2-B14	
PMC_IO15	J14-15	P2-B15	
PMC_IO16	J14-16	P2-B16	
PMC_IO17	J14-17	P2-B17	
PMC_IO18	J14-18	P2-B18	
PMC_IO19	J14-19	P2-B19	
PMC_IO20	J14-20	P2-B20	
PMC_IO21	J14-21	P2-B21	
PMC_IO22	J14-22	P2-B22	
PMC_IO23	J14-23	P2-C6	(Port1_com, 3101-BP Ethernet board)
PMC_IO24	J14-24	P2-C10	(Port1_com, 3101-BP Ethernet board)
PMC_IO25	J14-25	P2-E3	(Port1_TXP, 3101-BP Ethernet board)
PMC_IO26	J14-26	P2-E1	(Port1_RXP, 3101-BP Ethernet board)
PMC_IO27	J14-27	P2-C8	(Port1_com, 3101-BP Ethernet board)
PMC_IO28	J14-28	P2-C12	(Port1_com, 3101-BP Ethernet board)
PMC_IO29	J14-29	P2-E4	(Port1_TXN, 3101-BP Ethernet board)
PMC_IO30	J14-30	P2-E2	(Port1_RXN, 3101-BP Ethernet board)
PMC_IO31	J14-31	P2-C1	

PMC_IO32	J14-32	P2-C2	
PMC_IO33	J14-33	P2-C14	(Port2_com, 3101-BP Ethernet board)
PMC_IO34	J14-34	P2-C18	(Port2_com, 3101-BP Ethernet board)
PMC_IO35	J14-35	P2-D4	(Port2_TXP, 3101-BP Ethernet board)
PMC_IO36	J14-36	P2-D2	(Port2_RXP, 3101-BP Ethernet board)
PMC_IO37	J14-37	P2-C16	(Port2_com, 3101-BP Ethernet board)
PMC_IO38	J14-38	P2-C20	(Port2_com, 3101-BP Ethernet board)
PMC_IO39	J14-39	P2-D5	(Port2_TXN, 3101-BP Ethernet board)
PMC_IO40	J14-40	P2-D3	(Port2_RXN, 3101-BP Ethernet board)
PMC_IO41	J14-41	P2-C3	
PMC_IO42	J14-42	P2-C4	
PMC_IO43	J14-43	P2-C5	
PMC_IO44	J14-44	P2-C22	
PMC_IO45	J14-45	P2-A11	
PMC_IO46	J14-46	P2-A1	
PMC_IO47	J14-47	P2-A12	
PMC_IO48	J14-48	P2-A2	
PMC_IO49	J14-49	P2-A13	
PMC_IO50	J14-50	P2-A3	
PMC_IO51	J14-51	P2-A14	
PMC_IO52	J14-52	P2-A4	
PMC_IO53	J14-53	P2-A15	
PMC_IO54	J14-54	P2-A5	
PMC_IO55	J14-55	P2-A16	
PMC_IO56	J14-56	P2-A6	
PMC_IO57	J14-57	P2-A17	
PMC_IO58	J14-58	P2-A7	
PMC_IO59	J14-59	P2-A18	
PMC_IO60	J14-60	P2-A8	
PMC_IO61	J14-61	P2-A19	
PMC_IO62	J14-62	P2-A9	
PMC_IO63	J14-63	P2-A20	
PMC_IO64	J14-64	P2-A10	

B.2 1394 Port 1 Twisted Pair A & Twisted Pair B

TP1AN_B	P2-D18
TP1AP_B	P2-D17
TP1BN_B	P2-E19
TP1BP_B	P2-E18

B.3 1394 Port 2 Twisted Pair A & Twisted Pair B

TP2AN_B	P2-D15
TP2AP_B	P2-D14
TP2BN_B	P2-E16
TP2BP_B	P2-E15

B.4 1394 Port 3 Twisted Pair A & Twisted Pair B

TP3AN_B	P2-D12
TP3AP_B	P2-D11
TP3BN_B	P2-E13
TP3BP_B	P2-E12

B.5 1394 Physical Ground

PHY_GND	P2-D13
PHY_GND	P2-D16
PHY_GND	P2-D19
PHY_GND	P2-E11
PHY_GND	P2-E14
PHY_GND	P2-E17
PHY_GND	P2-E20

B.6 Logic Ground

LOGIC_GND	P2-F1
LOGIC_GND	P2-F2
LOGIC_GND	P2-F3
LOGIC_GND	P2-F4
LOGIC_GND	P2-F5
LOGIC_GND	P2-F6
LOGIC_GND	P2-F7
LOGIC_GND	P2-F8
LOGIC_GND	P2-F9
LOGIC_GND	P2-F10
LOGIC_GND	P2-F11
LOGIC_GND	P2-F12
LOGIC_GND	P2-F13
LOGIC_GND	P2-F14
LOGIC_GND	P2-F15
LOGIC_GND	P2-F16
LOGIC_GND	P2-F17
LOGIC_GND	P2-F18
LOGIC_GND	P2-F19
LOGIC_GND	P2-F20
LOGIC_GND	P2-F21
LOGIC_GND	P2-F22

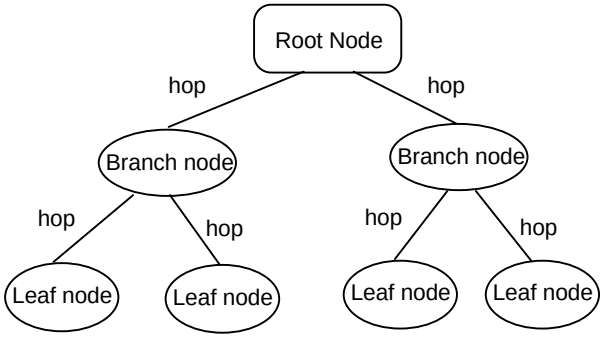
B.7 Not Connected

P2-A21
P2-A22
P2-C7
P2-C9
P2-C11
P2-C15
P2-C17
P2-C19
P2-C21
P2-D1
P2-D6
P2-D7
P2-D8
P2-D9
P2-D10
P2-D20
P2-D21
P2-D22
P2-E5
P2-E6
P2-E7
P2-E8
P2-E9
P2-E10
P2-E21
P2-E22

Appendix C: IEEE 1394 Reference

C.1 Introduction

The IEEE 1394 bus is a scaleable serial bus with transmission speeds of 100, 200, or 400 megabits per second (M bits/sec). Multiple 1394 devices (nodes) may be connected using a point-to-point signaling environment. Each 1394 node can have one or more ports. Each node acts as a repeater, retransmitting any packet received from one port to all other ports if it is not intended for the receiving node.



The bus is connected as a tree structure radiating from a root node. Nodes with only one connection are called leaf nodes. Nodes connecting two or more nodes are called branch nodes. The node highest in the tree is the root node. The root node is actually a branch node but because of its special placement it is given a special name. Each connection between nodes is called a hop. No two nodes can be more than 16 hops removed from each other. The more hops on a 1394 bus, the longer the time required to grant the bus to the next requesting node. The IEEE 1394 bus is hot-pluggable and automatically reconfigures whenever a new device is added to the bus. The 1394 bus appears as a large memory mapped space that has 64 bits of address space. Each 1394 bus may have up to 63 nodes, each of which has 48 bits of address space.

C.2 Resource Managers

The 1394 bus has two special resource managers: the bus manager, and the isochronous resource manager. These managers can be on the same or different nodes.

The bus manager broadcasts the topology and speed maps, manages power, and optimizes bus activity. It is responsible for optimizing the arbitration delays dependent on the maximum number of hops in the topology.

The isochronous resource manager is responsible for allocating bandwidth for isochronous transfers. It can allocate up to a maximum of 80% of the 1394 bandwidth to isochronous transfers. The isochronous resource manager is always an isochronous-capable node.

C.3 1394 Data Transfers

The 1394 bus protocol supports two types of data transfers: isochronous and asynchronous.

C.3.1 Isochronous Transfers

Isochronous transfers are always write transactions and are not acknowledged. They may be written to one or more nodes. Up to a maximum of 80% of the 1394 bandwidth may be allocated to isochronous transfers. The bandwidth allocation is handled by the isochronous resource manager, a 1394 node that may or may not be the same as the 1394 bus manager.

C.3.2 Asynchronous Transfers

Asynchronous transfers are reads or writes to a specific node that are acknowledged. There is error checking and retransmission capability. The maximum quantity of data transmitted via an asynchronous packet is dependent on the 1394 bus speed. For example, a 400M bits/sec part is capable of transmitting 2048 bytes in a single packet.

C.4 1394 Protocol Layers

The 1394 bus has four protocol layers: physical, link, transaction, and bus management.

C.4.1 Physical Layer

The physical layer consists of the electrical signaling, the connector mechanics, the cables, the cable arbitration, and data serial encoding and decoding. 1394 cables are either 4-wire or 6-wire with two twisted pairs for differential signals. The 6-wire version also carries power and ground that may be used to power a device's physical layer even if its host's power is switched off. The 1394 specification allows a maximum length of 4.5 meters for copper cable.

The physical layer influences the bus configuration and arbitration protocol phases. During configuration, the 1394 bus manager organizes all nodes connected to the 1394 bus into a logical tree with the root node at its focal point. This is done whenever a node is added to or removed from the 1394 bus. The configuration process requires a bus reset followed by initialization, tree identification, and self-identification. A bus reset may also be initiated any time through software control. The bus reset clears any topology information within any node. The tree identification process then defines the new bus topology. The self-identification process assigns physical IDs to each node on the bus. Neighboring nodes indicate their transmission speeds to each other. All nodes are made aware of the new topology. Transmission speeds between any two nodes is limited by the speed of the slowest device between the two nodes. During the self-identification process, all nodes wishing to be the isochronous resource manager indicate this in their self-ID packet.

The 1394 bus uses an 8KHz cycle clock to synchronize transactions. Each 1394 cycle is 125 µsec. The cycle master (root node) maintains the cycle clock. At the beginning of each cycle, a cycle start message is transmitted onto the 1394 bus. Each 1394 device synchronizes to this time base. Following the cycle start, all isochronous masters request the 1394 bus. The closest device to the root node is granted the bus. The isochronous master must make certain that the aggregate bandwidth required by isochronous devices does not exceed 80% of the bus bandwidth. After all isochronous devices have transmitted their data, asynchronous devices may begin arbitration. Again, the node closest to the root node is granted the bus. 1394 uses interval fairness, where once a device has been granted the bus, it may not use it again until all 1394 asynchronous devices have had an opportunity to use the bus. This is indicated by the 1394 bus remaining idle for more than the subaction gap, typically 10 µsec. Asynchronous devices may arbitrate for the bus many times within a cycle.

C.4.2 Link Layer

The link layer interfaces to the physical layer and generates and checks the CRC in the 1394 packets. The link layer, which sends and receives isochronous data, uses packet header information to determine the current 1394 transaction's type. The link layer can then inform the transaction layer of the transaction type that is occurring.

C.4.3 Transaction Layer

The transaction layer is only involved during an asynchronous transaction. Because the 1394 protocol uses a request-response mechanism, the transaction layer must send confirmations to the 1394 transaction. Confirmations may be sent immediately or they may be delayed. There are five 1394 transaction types: simple quadlet read, simple quadlet write, variable-length read, variable-length write, and lock transactions.

Transactions can be split, concatenated, or unified. A transaction is split if the receiving device cannot respond immediately to the requesting device. In this case, the request packet will be acknowledged following upon receipt. All asynchronous request packets must be acknowledged immediately after the request is received. The acknowledging node does not need to arbitrate for the 1394 bus, it is automatically granted to the responding node. When the data are ready, the responding node arbitrates for the 1394 bus and a response packet containing the requested data is sent. The node that initiated the read must acknowledge this response packet. If the responding node can provide the requested data immediately following the read request, the response transaction may be concatenated to the request transaction, thus eliminating the need to arbitrate for a separate response transaction. The acknowledge to a write transaction can also be the response to that transaction. This is called a unified transaction. If the responder can accept the data as fast as it is provided, the acknowledge packet can carry a transaction code indicating that the transaction is complete rather than pending.

C.4.4 Bus Management Layer

Several bus management activities are carried out by one or more 1394 nodes: the cycle master (root node), isochronous resource master, and bus master. The root node is always the cycle master and initiates the 125 µsec cycles. The bus manager broadcasts the topology and speed up maps, manages power, and optimizes bus activity. The isochronous resource manager is an isochronous-capable node responsible for allocating the isochronous bandwidth.

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