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ABI-PMC

MIL-STD-1553 Interface

I/O & COMMUNICATIONS

Features

1 dual redundant 1553 channel featuring 100% concurrent and independent operation as a:

- Bus Controller
- 31 Remote Terminals
- Dual Function Bus Monitor

Bus Controller

- Programmable frame lists
- BC-RT, RT-BC, RT-RT
- Mode codes, broadcasts, and time delays

RT Functionality

- RT level protocol selection
- RT definition tables
- Programmable response time

Bus Monitor

- Map monitoring
- Sequential monitoring
- Time stamped
- Double buffered
- Error tables
- Definable monitoring

Architecture

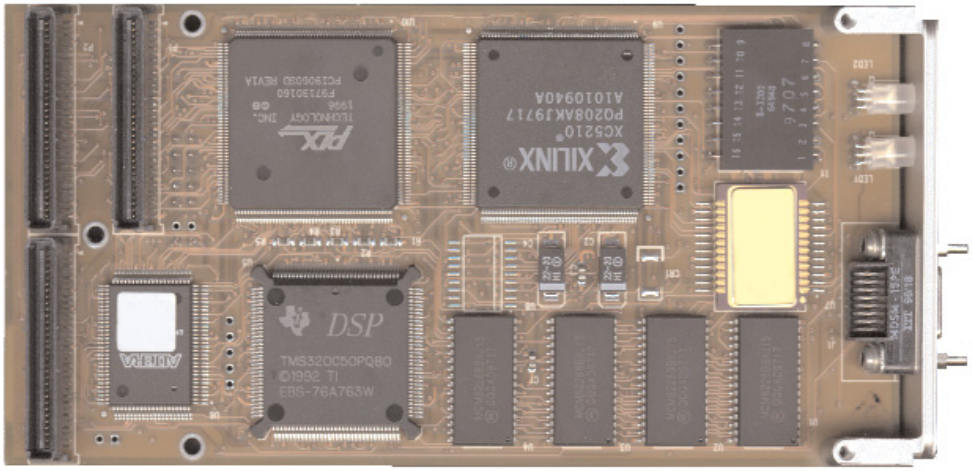
- On-the-fly data structures
- BC and RT linked lists
- High-speed DSP
- Flexible memory structure
- Flash memory

Mezzanine Card

- IEEE P1386 compliant

Software Support

- Complimentary drivers for most operating systems
- Integrated Avionics Library, including source code



ABI-PMC (PCI Mezzanine Card) interface provides a flexible, full function, dual redundant MIL-STD-1553 interface to the PCI Mezzanine. This Advanced Bus Interface (ABI) architecture provides concurrent and independent operation of a Bus Controller (BC), 31 Remote Terminals (RT), and dual function Bus Monitoring (BM). The ABI-PMC interface equips the PMC carrier with a complete 1553 interface. This includes 1553A/1553B selections, pointer-driven transmit and receive buffers and extensive programmable event interrupts.

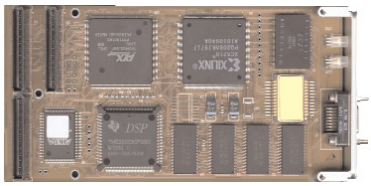
BC simulation structures consist of linked lists of 1553 command messages: BC-to-RT, RT-to-BC, RT-to-RT, mode code, broadcast and time delay block transmissions. We define RT simulation as a simple series of pointers to RT definition tables. The RT definition tables in turn point to control data buffers. We define the bus activity we want to monitor in both the Map and Sequential monitoring modes. This provides user defined linked lists of data buffers and sequential 1553 activity. The user can time stamp and/or double buffer the 1553 activity. Both monitoring modes perform broad error monitoring. They also provide a comprehensive error table that the host processor can read at any time.

Hardware Overview

SBS bases the ABI interface upon an advanced high speed DSP, programmable logic and dual port RAM. It delivers a highly reliable hardware platform that is feature rich and user friendly. Through the 128 kB of dual port RAM, the host processor has access to set up, monitor, and change the 1553 interface data structures at any time. Link-list memory architecture allows the user to structure interface memory usage for the maximum in flexibility and usefulness.

Software Support Overview

SBS distributed software includes host processor device drivers to the dual port control and data structures as well as an application layer to these structures. SBS also provides low-level drivers for most operating systems, and the Integrated Avionics Library with source code, with the interface at no additional cost.



ABI-PMC

Configurations

Model Number	Configuration
ABI-PMC-1	Single Channel 1553 to PMC interface
IRIG	IRIG B Time Receiver (add /IRIG to product number)

Specifications

ABI Functionality:
Bus Controller (BC)

- BC retry
- Minor frame timing and message scheduling
- Intermessage gap selectable
- Programmable delay gaps and null BC blocks
- Multiple BC data buffers in a linked list structure

Remote Terminals (RTs)

- 31 RTs and all subaddresses supported
- Transmit/Receive buffers for each subaddress
- Multiple RT data buffers in a linked list structure
- Programmable RT response time, no-response selection and no-response time-out

Map Monitoring

- Multiple linked buffers for each transmit/receive subaddress
- Mapped buffers read by host processor as time permits
- Number of buffers per transmit/receive subaddress is programmable or user definable to account for various host speeds

Sequential Monitoring

- 100% independent
- Host driver selected messages are double buffered
- Messages time stamped with a 1 µs 32-bit clock or optional 48-bit IRIG-B clock
- Standard firmware performs broad error monitoring
- Comprehensive error table readable at any time by host processor

Self Test

- Power-up test with status register report
- BIT-RAM and encoder/decoder test
- Run-time health status register
- Unit Test application for 1553 bus functionality

Multi-Purpose I/O

- Bi-directional external trigger
- IRIG clock input (optional)
- External TTL/RS-422 system clock input

PMC Functionality

- PCI bus is 2.1 compliant
- 50 Mb per second maximum transfer rate
- 16-bit and 32-bit transfer modes
- Memory mapped
- Programmable DMA controller
- On-board firmware storage via Flash memory

PCI Mezzanine Connection

- IEEE P1386 PMC connection
- PMC P4 to VMEbus P2 support

Interface Connections

- µM in $DB15_F$ to coupling harness (CA-2189)
- Coupling harness to bus and I/O connectors
- DB I/O connector
- $BJ77_F$ Triax connector to 1553 bus

Interface Card Specifications

- Maximum power consumption (98% bus activity) - single channel:
  5 V @ 1.5 A (1.0 A with bus inactive
- Standard commercial temperature:
  0° C to +60° C
  ≤ 95% rH non-condensing
- Mechanical:
  Standard PMC card
  Length 6.0" Width 2.9"

Software and Documentation Support

- Low-level drivers for most operating systems
- Integrated Avionics Library with source code
- Borland and Microsoft® C Compiler compatible
- Hardware and Integrated Avionics Library documentation included on CD. Hard copies of the documentation are available upon request.

Customer Support

- Two-year warranty
- Extended warranties available
- Driver and library upgrades
- Over 18 operating systems supported on various platforms

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