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1553 ADVANCED BUS INTERFACE FOR VME (ABI-V4)

BUS MASTER

REFERENCE MANUAL

Microcode Product Number:
Microcode Version:

SBS Avionics Technologies

December 15, 1995

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ERRATA

This section details corrections to the following documents:

ABI-PC2 Reference Manual, January 18, 1995 (see cover page for current date)
ABI-V3 Reference Manual, August 15, 1994
ABI-Q Reference Manual, August 15, 1994
ABI-V2 Reference Manual, August 15, 1994
ABI-PC/AT Reference Manual, August 15, 1994
ABI-V4 Reference Manual, December 15, 1995

ALL DOCUMENTS

Built-In Test Routines

The procedure for BIT #3 should read as follows:

1. Reset ABI by loading offset 0000h with "1". (Reset CSR)
2. Set MAP register by loading offset 0010h with "3". (Set MAP)
3. Load offset 003Fh with any value.
4. Load offset 0040h with "0000".
5. Start ABI by loading offset 0000h with "0240" followed by loading offset 0000h with "0242". NOTE: If running this test on a PASS-1000, load offset 0000h with "0040", followed by "0042".
6. Load starting test address in offset 0044h. Minimum acceptable value is "0080".
7. Load ending test address in offset 0045h. Maximum acceptable value is "FFFF".
8. Start the test by writing "0001" to the Command (CMD) word at offset 0040h.
9. Wait for offset 0040h to equal "0000".
10. Check offset 0043h. If a nonzero value is present at this offset, errors occurred during the test.

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ABI Operations Overview

Error Table

Add error code 15E to this table. This error occurs when an RT sends an extra data word.

ABI-PC2 & ABI-V3 ONLY

The information contained in the following paragraphs applies only to products having the following microcode loads:

ABI-V3	M019H and above
ABI-PC2	M025E and above

The microcode load is listed on the product box label and is also printed on the labels attached to the actual PROMs on the board. If you are unable to determine the microcode load for your SBS product, contact SBS Technologies at 1-800-SBS-1553 or (505) 875-0600.

Built-In Test Routines

Microcode Organization, second paragraph, page 3-1

For products having the microcode loads listed above, the Built-In-Test (BIT) microcode is found only in the high PROM area. Select a specific BIT routine by calling one of seven starting addresses, listed in Table 3-1.

Table 3-1 BIT Addresses

Microprogram Address	Program Selected	Description
0001h	Built-In-Test # 1	Tests Internal registers and addressing modes
0002h	Built-In-Test #2	Tests ALU and condition code operation
0003h	Built-In-Test #3	Tests RAM with Read/Write/Verify pattern-specific data
0004h	Built-In-Test #4	More testing of internal registers and addressing modes
0005h	Built-In-Test #5	Tests on-board timer sub-system
0006h	Built-In-Test #6	Tests 1553 interface logic and front end
0007h	Built-In-Test #7	Tests external discrete trigger function

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Built-In Tests 1-7, pages 3-3 through 3-12

Each BIT test includes a "Start" instruction which involves loading offset 0000h with either "0242" or "0042." For products having the microcode loads listed above, load offset 0000h with "0242."

Full Function Programmer's Reference

Microcode Initialization, page 4-19

When an ABI module is powered-up or reset, the host software must perform the proper startup procedure to initialize the microcode program.

Table 4-6 Microcode Program Identification

Microprogram ID #		Microprogram Description	Where Discussed
1	0001h	Reserved	-------
2	0002h	Reserved	
3	0003h	Reserved	
4	0004h	Reserved	
5	0005h	Reserved	
6	0006h	Reserved	
7	0007h	Reserved	
8	0008h	Reserved	
9	0009h	Reserved	
10	000Ah	Reserved	
11	000Bh	Reserved	
12	000Ch	Reserved	
13	**000Dh**	**Full Function 1553B**	**"1553 Microcode Program Startup Procedure" in this manual subsection**
14	000Eh	Reserved	-------
15	000Fh	Reserved	

The Application Main Body program is the entry point for the "Full Function 1553B" microcode program that executes the BC, RT, Monitor, and Interrupt functions of this interface.

For products having the microcode loads listed above, the Built-In-Test routines are contained in the upper half of the PROM and application microcode in the lower half. To run the application microcode, select the lower PROM area (set CSR bit 9 to "0") in the "1553 Microcode Program Startup Procedure" which follows in this subsection.

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INTRODUCTION

The Advanced Bus Interface (ABI) is a single card, real-time MIL-STD-1553 interface module for VME host systems. The ABI provides the host system an advanced 1553 interface, including the following features: simultaneous and independent simulation of Bus Controller and 31 Remote Terminals, real-time monitoring, double-buffered monitoring and flexible event Interrupt capabilities. The ABI may be configured for one or more of these functions.

This manual provides detailed information on ABI setup and operations and is organized according to Table Intro-1 (continued on the following page).

Table Intro-1 ABI Manual Organization

Section	Description
Introduction	Provides a description of the Reference Manual organization, and a discussion of the relationship between the Reference Manual and Interface Libraries Manual.
Hardware Installation	This section describes the steps required to install the ABI into the host system. For VME systems, the proper system address must be set on the ABI board. There is also a general discussion on configuring the ABI for short stub (1553A typically) or long stub (1553B) configurations, and the proper physical connections of the ABI to a 1553 bus.
Built-In-Test Routines	This section describes the various ABI Built-In-Test (BIT) routines that provide a comprehensive diagnostic utility for the ABI. Each test description explains the functionality, execution procedure, and the expected results for the BIT.

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Table Intro-1 ABI Manual Organization	
Section	**Description**
Full Function Programmer's Reference	This section provides a detailed overview of the ABI architecture and operations. The section includes an introduction and five subsections, as described below: **Introduction/ABI Operations Overview** - Provides a general system description and details the memory organization of the ABI. **Microcode Init** - Explains the procedure the host computer must follow to properly initialize ABI operations. **BC Simulation** - Describes the ABI Bus Controller functions and the related data structures. **RT Simulation** - Describes the ABI Remote Terminal functions and the related data structures. **Bus Monitoring** - Describes the two types of 1553 bus monitoring available with the ABI (Sequential and Map Monitoring) and the related data structures. The data structures used for Map Monitoring overlap those used for RT Simulation; therefore, both subsections must be read to fully understand Map Monitoring. **Interrupts** - Describes the action taken by the host to cause a 1553 event interrupt on the ABI. This subsection also details the proper procedure for servicing both hardware and software polling interrupts.

Most of the procedures described in the *BIT Routines* section and *Full Function Programmer's Reference* section for setting-up and running ABI 1553 functions are provided as C functions or Ada procedures in the Interface Libraries. For example, the "1553 Microcode Program Startup Procedure" described in the *Full Function Programmer's Reference* can be performed by host software through one of two C function calls: "init_device()" or "start_microcode()". There are many defined library functions provided to simplify the host integration effort.

ABI users should first read the *Full Function Programmer's Reference* section, followed by the Interface Libraries Manual.

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ABI-V4 Hardware Installation
TABLE OF CONTENTS

Introduction HW-1
Operational Storage/Connector Specifications HW-1
VMEbus Characteristics HW-1
Unpacking and Inspecting the Equipment HW-2
Setting the ABI RAM Base Address in VMEbus Memory HW-3
Auxiliary Connector Pinout HW-5
Installing the ABI-V4 in a VMEbus System HW-7
Connecting the ABI to a 1553 Bus HW-7
Power Application HW-8
Testing the Board HW-8

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TABLE OF FIGURES AND TABLES

Figure HW-1 ABI-V4 Board Layout HW-2
Table HW-1 Jumper Blocks and Connectors HW-3
Table HW-2 Base Address Selection HW-4
Figure HW-2 Switch Positions for Default Base Address HW-4
Table HW-3 P5 Pin Assignments HW-5
Figure HW-3 ABI-V4 Front Panel HW-6
Figure HW-4 Bus Coupling (Long Stubs) HW-8

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ABI-V4 HARDWARE INSTALLATION

Introduction

The ABI-V4 is a single board, 1553 interface for systems based on the VMEbus. This section describes unpacking, configuring, and installing an ABI-V4 into a VMEbus system. Because proper installation is critical to successful operation of the ABI-V4, SBS Engineering recommends that the steps described here be followed explicitly. The steps involved in the installation include:

- Unpacking and inspecting the equipment
- Setting the ABI-V4 RAM base address in the VMEbus memory
- Reviewing the System Timer Configuration
- Selecting long or short stub connection
- Installing the configured board in the VMEbus system
- Testing the installed board

This manual section describes the above steps in detail.

> NOTE: This is an electronic product that is sensitive to electrostatic discharge. Observe normal precautions in handling the board to prevent damage.

Operational Storage/Connector Specifications

- Maximum Power Consumption:
  - 5 volts at 2.7 amps
  - 12 volts at 250 milliamps
- Operating Temperature: 0° to 60° Celsius, at less than or equal to 95% humidity
- Storage Temperature: -65° to 150° Celsius, at less than or equal to 95% humidity
- Shock requirements are to the highest commercial standards
- Mean Time Between Failures: >50,000 hours, based on MIL-HDBK-217F
- Mating Connectors: one DB25 male and two Trompeter BJ77 connectors

VMEbus Characteristics

The ABI-V4 board supports both A32 and A24 VMEbus address modes. The desired address mode is switch-configured. Both Supervisor and Non-privileged address modes are supported. The ABI-V4 board supports slave data transfers in D64, D32 and D16 modes. Single transfers are supported in all D32 and D16 modes, and block transfers are supported in either D64 or D32. All Interrupt vectors are type D08.

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The ABI-V4 is also capable of being a VME master device. While in this mode, D64 and D32 block transfers are supported. VME master also supports Supervisor and Non-privileged transfers, in either A24 or A32 address mode.

Unpacking and Inspecting the Equipment

Carefully unpack the ABI board and inspect for any visible damage that could have occurred during shipment. If there is damage, contact SBS Engineering with the board and board serial number available.

Figure HW-1 and Table HW-1 show a layout and description of the switch and jumper block positions on the ABI-V4 board. These switches and jumper blocks are detailed following the illustrations.

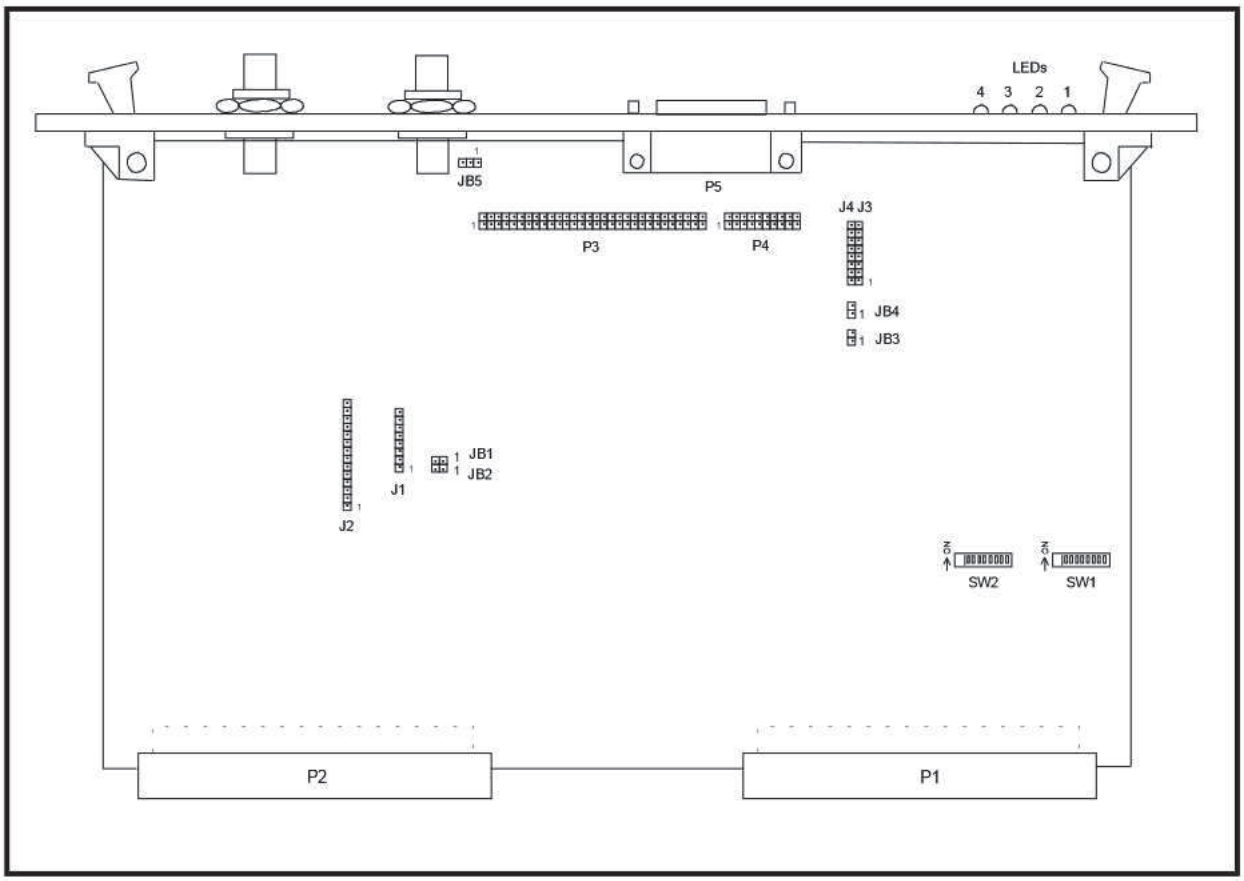


Figure HW-1 ABI-V4 Board Layout

Test blocks (TBs) are for factory test purposes only and are omitted from Figure HW-1.

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Table HW-1 Jumper Blocks and Connectors		
Jumper Block/ Connector	Description	Default Jumper Setting
JB1	VSB Master Xilinx Configuration	none
JB2	Microcode PROM Enable	JB2-1 to JB2-2
JB3	VME Master Xilinx Configuration	JB3-1 to JB3-2
JB4	System Timer Xilinx Configuration	JB4-1 to JB4-2
JB5	External Clock Type Selection	JB5-1 to JB5-2
P1, P2	VMEbus Interface	none
P3, P4	Transceiver Daughterboard Connectors.	none
P5	External Connector. Assorted signals for external input/output connections.	none
P6	1553 Bus A (Primary)	none
P7	1553 Bus B (Secondary)	none
J1	VSB Master Download Test Connector	none
J2	Sequencer Test Points	none
J3	VME Master Download Test Connector	none
J4	System Timer Download Test Connector	none

Setting the ABI RAM Base Address in VMEbus Memory

The base ABI-V4 appears as 64K 16-bit words (128K bytes) of RAM mapped into the local address space as either A32 or A24 addressable memory. The user must set the desired offset address of this memory in the local VMEbus system. The selection of address type A32 or A24 and the selection of a base address offset are made by modifying SIP switches SW1 and SW2. Setting the address bits maps the ABI-V4 RAM to a 64K word boundary. Figure HW-1 shows the locations of the jumper blocks and SIP switches on the ABI-V4 board. Setting a switch to "on" sets the value of the corresponding address bit to "0"; setting a switch to "off" sets the value of the corresponding address bit to "1". Table HW-2 and Figure HW-2 demonstrate an offset base address of 4800 0000h and a selection of A32 address mode (the default setting of the board when shipped).

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Table HW-2 Base Address Selection			
Address Bit	Desired Value	Switch Location	Switch Setting
A31	0	SW1-1	ON
A30	1	SW1-2	OFF
A29	0	SW1-3	ON
A28	0	SW1-4	ON
A27	1	SW1-5	OFF
A26	0	SW1-6	ON
A25	0	SW1-7	ON
A24	0	SW1-8	ON
A23	0	SW2-1	ON
A22	0	SW2-2	ON
A21	0	SW2-3	ON
A20	0	SW2-4	ON
A19	0	SW2-5	ON
A18	0	SW2-6	ON
A17	0	SW2-7	ON
A32/A24 Select	0**	SW2-8	ON

Notes:
1. ** A32 address mode is selected by setting this switch ON; A24 address mode is selected by setting this switch OFF.
2. When using A24 addressing, the positions of the switches in SW1 are "Don't Care" values.

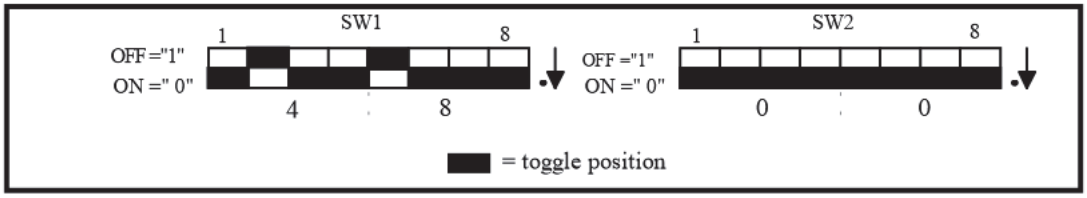


Figure HW-2 Switch Positions for Default Base Address

Determine the base address to be used for the ABI-V4 and set SW1 and SW2 accordingly.

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Auxiliary Connector Pinout

External connector P5 is used for various external input/output signals. The pin assignments are listed in Table HW-3.

Table HW-3 P5 Pin Assignments

Pin #	Signal
1	Primary 1553 Bus +
2	Secondary 1553 Bus +
3	Reserved
4	Reserved
5	Reserved
6	Reserved
7	External Trigger In/Out *
8	Reserved
9	External Clock + **(For version 03 boards only: also connected to pin C6 on connector P2)**
10	External Enable *
11	External Clear *
12	Reserved
13	+5 VDC
14	Primary 1553 Bus -
15	Primary 1553 Bus -
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Ground
21	Ground
22	External Clock -
23	Ground
24	Ground
25	Ground

Reserved = DO NOT CONNECT TO THESE PINS
+ = Active High portion of differential signal pair
- = Active Low portion of differential signal pair
* = Active Low signal

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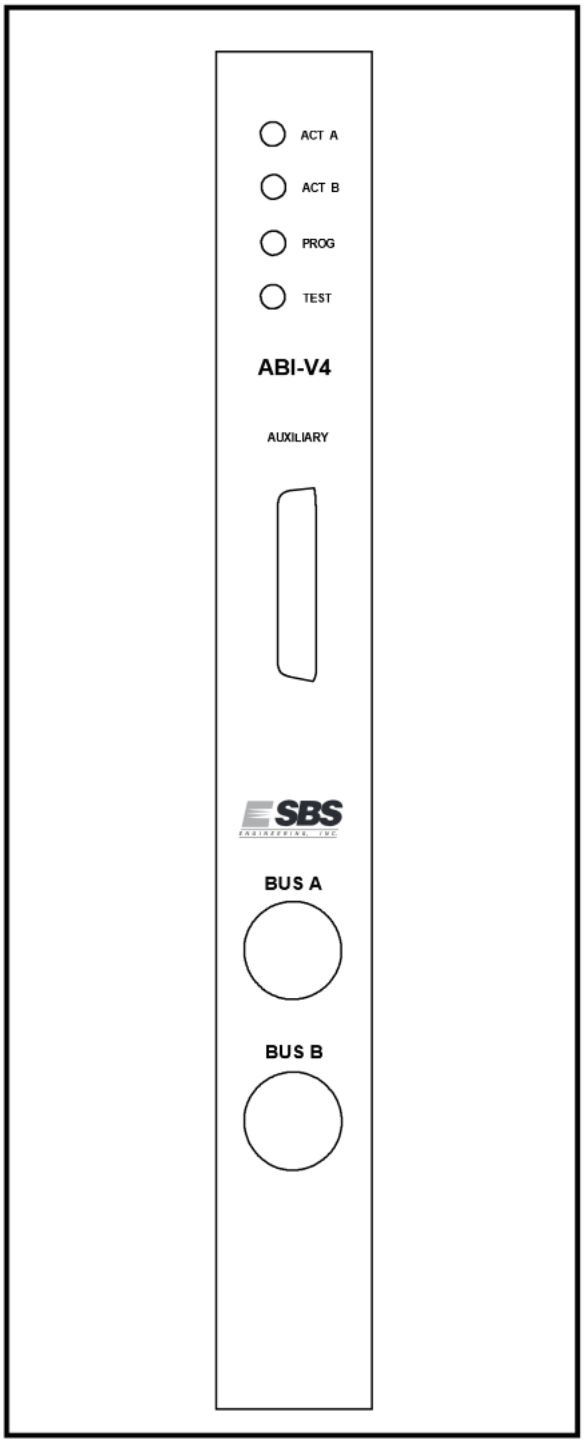


Figure HW-3 ABI-V4 Front Panel

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Installing the ABI-V4 in a VMEbus System

Install the ABI-V4 board into the desired slot in the host system. Follow the instructions supplied by the system manufacturer.

Connecting the ABI to a 1553 Bus

For operation, the ABI must be connected to a 1553 bus. These 1553 bus connections must be made very carefully. **The ABI will not operate properly if the bus connections are not correct.** (For test purposes it is sufficient to simply connect standard bus terminators to the A and B bus connectors on the front panel of the interface.)

The 1553 bus consists of a twisted-pair cable with terminators at each end, ranging in length from a few inches to several hundred feet. The physical connection of a subsystem to this bus is called a stub. The configuration used for the connection is referred to as long-stub coupling and requires a transformer and two resistors, used at the exact point where the connection is made to the bus. These components are typically enclosed in a small module called a *bus coupler*. These couplers may provide for connection of only one stub or several stubs. The coupler has two connectors for the bus (usually at opposite ends of the coupler) and a connector for each stub (typically mounted perpendicular to the bus connectors).

Subsystem stubs will not function properly if connected directly together. Proper coupling devices must be used for each stub and the bus must be properly terminated. Figure HW-7 illustrates the proper and improper connection schemes for long-stub coupling and the terminology used for the various components associated with the bus. A three-stub coupler is shown in the figure. In this case, the bus is contained entirely within the coupler. If other devices are to be connected to the bus, one of the terminators must be removed and replaced with a cable connecting this coupler to another coupler. The other coupler could then be terminated or the bus extended further.

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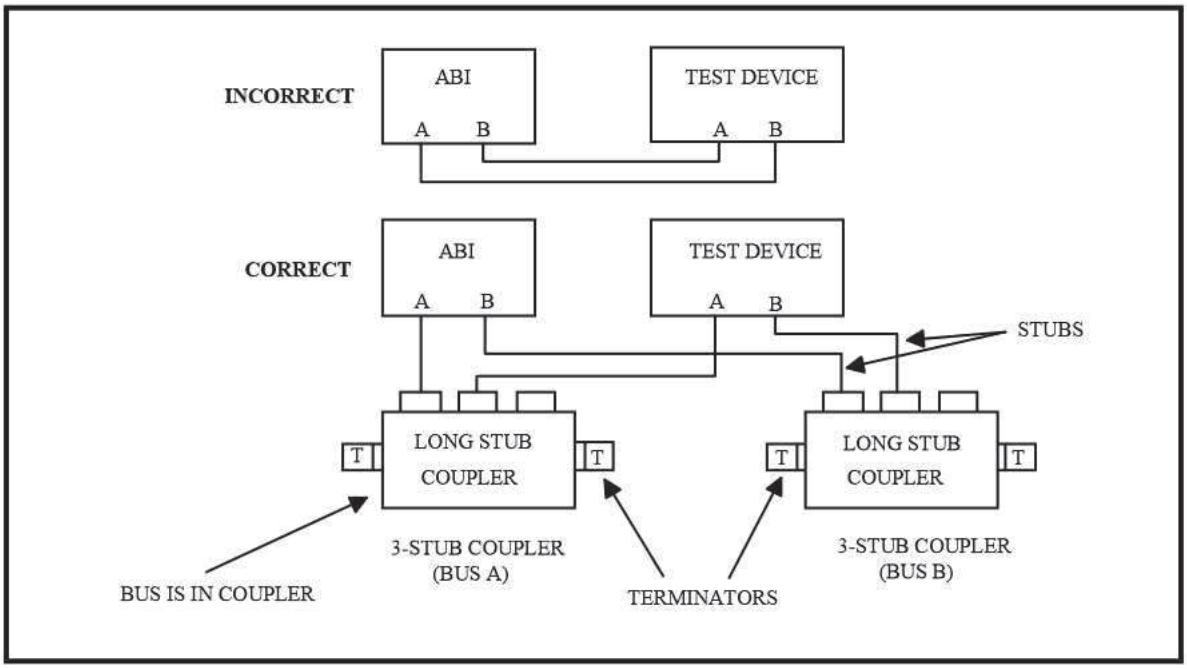


Figure HW-4 Bus Coupling (Long Stubs)

Power Application

Power up the host computer system to apply power to the ABI. Figure HW-3 shows four LEDs that are visible on the ABI's front panel. The LED labeled TEST indicates proper initialization of the board and should be green following power-up. The LED labeled PROG is a user programmable LED, and is described in the following paragraph "Testing the Board". If the TEST LED is not green, contact SBS Engineering.

Testing the Board

When the TEST LED is green, the ABI can be accessed by the host at the address selected during configuration. Determine a suitable method for accessing the board from host software. The method used depends on the operating system and the language used for programming.

Once the method has been determined, write a program to test the board. SBS supplies a number of diagnostic functions in microcode which may be used to test the operation of the board. The section entitled "Built-In Test Routines" discusses the procedures to be followed to utilize these functions. Test routines should be run daily as part of an operation-readiness user program.

There is a simple test that may be performed (prior to the complex diagnostic test series) to determine if the ABI is being properly accessed. To perform this test, turn the PROG LED green by loading a 0800h into the Control/Status register (offset 0000h). Next, turn the PROG LED

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red by loading a 0400h into the Control/Status register. This test is to be used only during initial testing of the board.

> **Warning:** The Control/Status register is used by the ABI microcode. Writing to this register during actual operation of the board could cause the ABI to malfunction.

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BUILT-IN TEST ROUTINES

Introduction

The ABI contains built-in-test capabilities which provide the user with an added level of hardware confidence and help to ease integration into new or existing systems. Many different routines are available to provide the user with information about various subsystems or devices on the ABI. This section describes each of these test routines, demonstrates how to execute them and explains how to interpret the results. Troubleshooting tips are also provided to assist in the initial integration and subsequent use of the board.

Microcode Organization

The ABI microcode is stored in a set of five registered PROMs with a capacity of 8K bytes of microprogram data. The address bus for these PROMs is a 12-bit pipelined bus. An additional bit is used to select a high or low PROM area (See Table 4-2 in the "ABI Operations Overview" subsection of the *Full Function Programmer's Reference*). This **PROM SEL** bit (bit 9 of the Control Status Register) allows the microcode PROMs to store two separate and independent microprograms. When this bit is set to "0", the low PROM area is selected; when the bit is set to "1", the high PROM area is selected.

Each PROM area (high and low) contains Built-In-Test (BIT) microcode followed by application microcode. The ABI may select a specific BIT routine or MIL-STD-1553 application microcode by calling one of 15 starting addresses. These microprogram starting addresses are listed in Table BIT-1.

Table BIT-1 Microprogram Addresses

Microprogram Address	Program Selected	Description
0001h	Built-In-Test # 1	Tests Internal registers and addressing modes.
0002h	Built-In-Test # 2	Tests ALU and condition code operation.
0003h	Built-In-Test # 3	Tests RAM with Read/Write/Verify pattern-specific data
0004h	Built-In-Test # 4	More testing of internal registers and addressing modes.
0005h	Reserved	
0006h	Built-In-Test # 6	Tests 1553 interface logic and front end.
0007h	Reserved	
000Dh	Application Code	Starts application code. (See "Microcode Init" subsection of *Full Function Programmer's Reference*)

The following pages show how to perform each BIT and how to interpret the results.

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Executing the ABI Built-In-Tests

Certain memory offsets must be loaded with specific values prior to executing a built-in test. Instructions for programming these locations are included with each test procedure.

BIT # 1

Procedure:

1. Reset ABI by loading offset 0000h with "1". (Reset CSR)
2. Set MAP register by loading offset 0010h with "1". (Set MAP)
3. Load offset 003Fh with any value.
4. Load offsets 0040h to 004Fh with "0".
5. Load offsets 0044h, 004Ch, and 004Eh with "FFFF".
6. Start ABI by loading offset 0000h with "0042". (Start)

BIT #1 is complete when offset 0040h has changed from "0" (after a few microseconds) to a non-zero value. Check the results against Table BIT-2.

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Results:

Table BIT-2 BIT #1 Results		
Address	**Expected Contents**	**Description**
0040h	non-zero value	BIT Code revision number. Exact number may vary, but should be similar to 0402.
0041h	0001	Base register 0, pipeline source okay
0042h	0002	Base register 1, pipeline source okay
0043h	FFFF	Indirect register 0 , pipeline source okay
0044h	0000	Indirect register 1, pipeline source okay
0045h	XXXX	Echo input. Value written here will also be written to location 46 when BIT 1 is executing.
0046h	(45)	Echoed value of contents of location 45.
0048h	XXXX	Counter pattern. Indicates microcode is operating. Will be different every time it is read.
0049h	0001	Base register 0, ALU source okay
004Ah	0002	Base register 1, ALU source okay
004Bh	FFFF	Indirect register 0, ALU source okay
004Ch	0000	Indirect register 1, ALU source okay
004Dh	FFFF	Base register 0, ALU Instruction source okay
004Eh	0000	Base register 1, ALU Instruction source okay
004Fh	non-zero value	Revision number for entire diagnostic & utilities microcode. Exact number may vary.

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BIT # 2

Procedure:

1. Reset ABI by loading offset 0000h with "1". (Reset CSR)
2. Set MAP register by loading offset 0010h with "2". (Set MAP)
3. Load offset 003Fh with any value.
4. Load offset 0040h with "FFFF".
5. Start ABI by loading offset 0000h with "0042". (Start)
6. Wait four microseconds.
7. Check contents of offset 0040h.

Results:

The contents of offset 0040h should be "0". Any bits set to "1" indicate an error; these are explained in Table BIT-3.

Table BIT-3 BIT #2 Errors

BIT #	INDICATES
1	Failure of ZERO Condition Code
2	Failure of NEGATE Condition Code
3	Failure of CARRY Condition Code
4	Failure of OVERFLOW Condition Code

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BIT # 3

Procedure:

1. Reset ABI by loading offset 0000h with "1". (Reset CSR)
2. Set MAP register by loading offset 0010h with "3". (Set MAP)
3. Load offset 003Fh with any value.
4. Load offset 0040h with "FFFF".
5. Start ABI by loading offset 0000h with "0042". (Start)
6. Load **starting** test address in offset 0044h.
7. Load **ending** test address in offset 0045h.
8. Start the test by writing one of the following values to the Command (CMD) word at offset 0040h.

Value	Result
"1"	Start test and perform one time only from the starting address to the ending address.
"2"	Start test and perform continuously from the starting address to the ending address. Halt only if an error occurs.
"3"	Start test and perform continuously from the starting address to the ending address. Do not halt even if an error occurs.

BIT #3 performs a series of READ/WRITE/VERIFY operations, beginning with the starting address and continuing to each subsequent address. There are three values, "0000", "FFFF" and DATA=ADDR, used for these operations. The operations are performed for a random number of address locations using one of these values (i.e. "0000"). The BIT test then uses another of these values (i.e. "FFFF") to test the next group of addresses. After a random number of addresses have been tested with the second value, the BIT test will begin using the third value for the operations. This test pattern continues through the ending address. If more than one cycle has been requested, the next pattern will be different from the previous. The address locations used by the BIT #3 microcode are listed in Table BIT-4.

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Results:

Table BIT-4 BIT #3 Addresses	
Address	**Description**
40	CMD - Command word, used to start test.
41	RSP - Response word. Microcode copies the CMD word to this location.
42	LCNT - Loop Count. Number of test loops completed.
43	EADR - Error Address. Indicates address where R/W/Verify error.
44	LOW - Starting Address for test range.
45	HI - Ending Address for test range.

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Built-In Test # 4

Procedure:

1. Reset ABI by loading offset 0000h with "1". (Reset CSR)
2. Set MAP register by loading offset 0010h with "4". (Set MAP)
3. Load offset 003Fh with any value.
4. Load offsets 0040h through 0042h with "0000".
5. Start ABI by loading offset 0000h with "0042". (Start)
6. Wait for one second, or for offset 0040h = "FFFF".

Results:

The information shown in Table BIT-5 is provided by the microcode.

Table BIT-5 BIT#4 Results

Address	Contents	Description
0040h	FFFF	Indicates test completion.
0041h	0000	No Errors.
0041h	0001	Failure during Base Register 0 Verify.
0041h	0002	Failure during Base Register 1 Verify.
0042h	xxxx	Base register contents at time of failure.
0043h	xxxx	Desired value of data.
0044h	xxxx	Actual value of data.

This test performs base register tests similar to those in BIT # 1.

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Built-In Test # 6

Procedure:

1. Reset ABI by loading offset 0000h with "1". (Reset CSR)
2. Set MAP register by loading offset 0010h with "6". (Set MAP)
3. Load offset 003Fh with any value.
4. Load offsets 0040h through 005Fh with "0000".
5. Load offset 001Fh with "00F0". (Set variable voltage control register.)
6. Start ABI by loading offset 0000h with "0042". (Start)

NOTE: This test must be performed on a **properly terminated** 1553 bus or with terminators installed directly on the front panel connectors. The ABI is intended to be connected to the 1553 bus via a data bus coupler if long stub operation is selected. There must be no extraneous activity on the bus while BIT # 6 is being performed. If BIT #6 fails while the ABI is connected to the 1553 bus: disconnect the ABI from the bus, install terminators directly onto the board and perform the test again.

Results:

The information shown in Table BIT-6 is provided by the microcode.

Table BIT-6 BIT #6 Addresses

Address	Contents	Description
0040h	CMD	Command Word. Should be "0000".
0041h	LPC	Loop count.
0042h	ERC	Error counter.
0043h	TNM	Test number of failure.
0044h	ERR	Error number.

If the bus is properly terminated and BIT #6 fails, note the TNM and ERR values and contact SBS Engineering. These values are defined in Tables BIT-7 and BIT-8.

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Table BIT-7 TNM Values	
TNM Value (in hex)	**Description**
0010	Prime Bus Active (PBA)/Alternate Bus Active (ABA) Initial Check.
0021	Serial Data Transmit/Receive Test.
0022	Serial Data Transmit/Receive Test.
0023	Serial Data Transmit/Receive Test.
0024	Serial Data Transmit/Receive Test.
0031	Gap Timer Test # 1.
0032	Gap Timer Test # 2.
0033	Gap Timer Test # 3.
0034	Gap Timer Test # 4.
0035	Gap Timer Test # 5.
0036	Gap Timer Test # 6.
0041	Data Lost Bit Test.
0042	Data Lost Bit Test

Table BIT-8 ERR Values	
ERR Value (in hex)	**Description**
0001	PBA = 1 > 20 Microseconds Error.
0002	ABA = 1 Error.
0003	Remote Terminal/Subaddress Data Error.
0004	Data Error.
0005	Invalid Word Error.
0006	Sync Type Error.
0007	Gap Too Short Error.
0008	Gap Too Long Error.
0009	Gap Static Data Error.
000A	Gap Counter Data Error.
000B	Lost Not Set Error.
000C	Lost Set 1 Error.
000D	Lost Set 2 Error.
000E	PBA Time-out Error.
000F	Data Ready (DRDY) Time-out Error.
0010	SARDY Time-out Error.
0011	XRDY Time-out Error.

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ABI Operations Overview **OVW-2**
ABI VMEbus Master Overview OVW-3
Addressing Considerations for Host Application Programs OVW-3
ABI Memory Organization OVW-5
VMEbus Configurations OVW-5
Control Registers: 0000-03FFh OVW-6
Data Structure Memory: 0400-FFFFh OVW-6
Control Register Descriptions OVW-7
Key Hardware Registers OVW-12
Control and Status Register (CSR) OVW-12
Host DMA Channel Registers (DMA CNTL, ABI ADDL, ABI ADDH, VME ADDL, VME ADDH, WORD CNT) OVW-14
ABI ADDL, ABI ADDH OVW-16
VME ADDL, VME ADDH OVW-16
WORD CNT OVW-16
Host Initiated DMA Transfer OVW-17
VMEbus Interrupt Level and Vector Programming (CSR, DMA CNTL, INTV_DMA, INTV_1553) OVW-17
MAP control register OVW-17
PSTEP control register OVW-17
Timing Hardware Registers OVW-18
ITCR (Internal Timer Control Register) OVW-18
Bit 0 - Clock Enable/Disable OVW-18
Bit 1 - Reserved OVW-18
Bit 2 - Timer Clear OVW-18
Bit 3 - External Clock Select OVW-18
Bit 4 - External Enable Output OVW-18
Bit 5 - External Clock Master Enable OVW-18
Bit 6 - External Enable Input OVW-18
Bit 7 - Internal/External Clears OVW-18
ITDRL, ITDRM, ITDRH (Internal Timer Data Registers) OVW-19
VVDR (Variable Voltage DAC Register) OVW-20
DMAERR, DMAQPT, DMAQLN (DMA Processing Queue Registers) OVW-21
Error Table OVW-21

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Hardware Reset OVW-24

Microcode Initialization MC-1

1553 Microcode Program Startup Procedure MC-2

Bus Controller Simulation BC-1

Control Block Structure BC-2

TYPE BC-3

CMD 1 ..... BC-4

CMD 2 ..... BC-4

STS 1 ..... BC-4

STS 2 ..... BC-4

FLAGS BC-4

Bit 0 - Disable Interrupt on Error BC-4

Bit 1 - Continue on Error/Masked Status BC-4

Bit 2 - Interrupt on Masked Status BC-5

Bit 3 - Disable Interrupt on BC Halt BC-5

Bit 6 - Enable BC Retry BC-5

Bit 15 - Bus Select BC-5

BPTR/DLY BC-5

DMA CNTL, ABI ADDH, ABI ADDL, VME ADDH, VME ADDL, WORD CNT BC-5

DMA Options BC-8

TIME3, TIME2, TIME1 ..... BC-8

LINK BC-9

Controlling BC Operation - BCIPTR, BCCPTR, BCLPTR BC-9

Status Word Mask - BCSMSK BC-9

BC Retries - BRTCNT,BRTBUS,BRTCMD,BRTRTC BC-10

Mode Codes BC-10

Remote Terminal Simulation RT-1

Status Word Table - Enabling RT Simulation RT-3

Status Word Response Bits RT-4

Bit 0 - Terminal Flag Bit RT-4

Bit 1 - Bus Control Accept Bit RT-4

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Bit 2 - Subsystem Flag Bit RT-4
Bit 3 - Busy RT-4
Bit 4 - Broadcast Command Received Bit RT-5
Bit 8 - Service Request Bit RT-5
Bit 9 - Instrumentation Bit RT-5
Bit 10 -Message Error Bit RT-5
RT Address Data Structures RT-5
Defining Data Word Buffers RT-5
Address Table RT-6
Buffer Pointer Table RT-7
Data Buffer Format RT-7
POINTER RT-7
DMA, ABI ADDH, ABI ADDL, VME ADDH, VME ADDL, WORD CNT RT-7
TIME3, TIME2, TIME1 ..... RT-10
FLAG WORD RT-10
Broadcast Considerations RT-10
Minimum Programming Requirements for the RT Address Data Structures RT-11
Filter Table RT-11
Bit 0 - Sequential Monitor Enable RT-12
Bit 1 - Interrupt on RT/SA RT-12
Bit 2 - Sequential Monitor Buffer Swap on Message RT-12
Bit 3 - Generate Parity Error RT-12
Minimum Programming Requirements for the Filter Table RT-12
Protocol Table RT-13
Bit 0 - Standard Protocol RT-13
Bit 1 - Mapped Monitor Enable RT-13
Bit 2 - Dynamic Bus Control RT-13
Bit 3 - Treatment of SA31 ..... RT-14
Bit 4 - Bus A Operation RT-14
Bit 5 - Bus B Operation RT-14
Minimum Programming Requirements for the Protocol Table RT-14
RT Mode Code Simulation RT-14
Mode Code Data Structures Required for ABI Operations RT-16
Last Status Word Data Structure RT-16

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RT Phase Data Structure RT-17
Transmit Vector Word Data Structure RT-18
Last Sync Word Data Structure RT-19
Last Command Data Structure RT-20
Bit Word Data Structure RT-21
Optional Mode Code Data Structures RT-21
Filter Table RT-21
RT Address Data Structures RT-21
Mode Command Interrupt Table RT-21
RT Address Mode Code Data Buffer Format RT-22
Mode Interrupt Mask Table RT-23
Variable Intermessage and Status Response Gap Times RT-24

1553 Bus Monitoring MON-1
Sequential Monitoring MON-1
Filter Table MON-2
Sequential Monitor Buffers MON-3
DMA CNTL, ABI ADDH, ABI ADDL, VME ADDH, VME ADDL, WORD CNT MON-4
Message Block Format MON-7
TYPE Word MON-8
Bits 0-6 - Message Type MON-8
Bit 7 - Bus Identification Bit MON-8
Bits 8-13 - Word Count MON-8
Bit 14 - Error Flag MON-8
TIME3, TIME2, TIME1 ..... MON-8
Data Words MON-8
Message With Error MON-8
Minimum Programming Requirements for Sequential Monitor Buffers MON-9
Buffer Swap Detection MON-9
Forcing Buffer Swaps MON-9
Map Monitoring MON-10
Map Monitoring Data Structures MON-11

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Interrupts **INT-1**
Interrupt Types INT-1
Interrupt Queue Data Structures and Control Registers INT-3
Minimum Programming Requirements for Interrupt Queues INT-4
Hardware Interrupt Service Procedure INT-6
Software Polling Interrupt Service Procedure INT-7

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TABLE OF FIGURES AND TABLES

Figure OVW-1 ABI Architecture OVW-2
Figure OVW-2 ABI Memory Organization OVW-4
Table OVW-1 ABI Control Registers OVW-7
Figure OVW-3 Control Status Register Bits OVW-12
Table OVW-2 Control Status Register Bit Definitions OVW-13
Figure OVW-4 Host DMA CNTL Word Bits OVW-14
Table OVW-3 Host DMA Control Word OVW-15
Table OVW-4 Variable Voltage DAC Register OVW-20
Table OVW-5 ABI Error Table OVW-21
Table MC-1 Microcode Program Identification MC-1
Figure BC-1 BC Control Structures BC-3
Table BC-1 BC Type Codes BC-4
Table BC-2 DMA Control Word BC-6
Figure RT-1 RT Status Word Table (SWTPTR) RT-3
Figure RT-2 RT Address Data Structures RT-6
Table RT-1 DMA Control Word RT-8
Figure RT-3 Filter Table Data Structures RT-11
Figure RT-4 Protocol Table RT-13
Table RT-2 ABI Mode Code Operations RT-15
Figure RT-5 Last Status Word Data Structure RT-16
Figure RT-6 RT Phase Table Data Structure RT-17
Figure RT-7 Transmit Vector Word Table RT-18
Figure RT-8 Last Sync Word Table RT-19
Figure RT-9 Last Command Word Table RT-20
Figure RT-10 Bit Word Table RT-21
Figure RT-11 RT Address Mode Code Data Buffer RT-22
Figure RT-12 Mode Interrupt Mask Table RT-23
Figure MON-1 Filter Table Data Structures MON-2
Figure MON-2 Sequential Monitor Buffer Data Structures MON-4
Table MON-1 DMA Control Word MON-5
Figure MON-3 Sequential Monitor Buffer Message Blocks MON-7
Figure MON-4 RT Address Data Structures MON-10
Figure MON-5 Protocol Table MON-11
Table INT-1 ABI Interrupt Types INT-2

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TABLE OF FIGURES AND TABLES

Figure INT-1 ABI Interrupt Queues and Control Registers INT-3
Table INT-2 Interrupt Word Descriptions INT-5
Table INT-3 Hardware Interrupt Service Procedure INT-6
Table INT-4 Software Polling Interrupt Service Procedure INT-7

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FULL FUNCTION PROGRAMMER'S REFERENCE - V4

The Advanced Bus Interface Version 4 (ABI-V4 - known herein as ABI) module provides the host computer with a real-time MIL-STD-1553 interface. The ABI is capable of simultaneous and independent Bus Controller (BC) and 31 Remote Terminals (RT) simulation as well as Map and Sequential Monitoring operations. The ABI also has the most advanced VME/VSBbus interface in the 1553 industry, capable of D32/D64 bus master and slave operations at over 40 megabytes per second. VSB transfer rates are at over 20 megabytes with a D32 width. (Actual transfer rates are dependent on the system configuration.) This section of the manual details the operations of the ABI and contains the following subsections:

- Introduction / ABI Operations Overview
- Microcode Initialization
- BC Simulation
- RT Simulation
- Bus Monitoring
- Interrupts

NOTE: This manual section assumes the user has previous knowledge of MIL-STD-1553 and VME/VSBbus operations.

The "ABI Operations Overview" subsection discusses ABI memory organization, VME/VSBbus master operations, and microcode program operations. The "Microcode Initialization" subsection explains the required steps in initializing an ABI. The three subsections following Microcode Initialization detail ABI configuration for Bus Controller, Remote Terminal and Monitor operations. The "Interrupts" subsection explains ABI interrupt capabilities and the recommended servicing procedures for hardware and software polled interrupts.

The ABI may have two 1553 microcode protocols resident on-board. (See the cover sheet of this manual for the available microcode loads.) The user may switch between these protocols through a software bit switch in a key control register. This section details the "Full Function 1553B" protocol for the V4 VME Bus Master card. Please see the "Microcode Initialization" subsection for more details on selecting and initializing the desired protocol. Contact SBS Engineering for more information on special protocol requirements.

The accompanying manual, 1553 Interface Libraries, provides a detailed description of the software libraries provided by SBS. These libraries provide the interface to a customer's real-time application software and are compatible with most computer operating systems. Review this *Full Function Programmer's Reference - V4* section before reading the 1553 Interface Libraries manual.

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ABI OPERATIONS OVERVIEW

The ABI is a bit-slice microcomputer with 4Kx48 bit microcode instructions containing programs customized for real-time 1553 applications. Figure OVW-1 provides a block diagram of the ABI. When installed in the host computer, the ABI appears as a contiguous block of virtual or physical 128K, 512K or 4M bytes of high speed SRAM. This pseudo dual-port memory resides on the ABI and is mapped or connected to the host system for user application program access. The ABI module provides an arbiter circuit to allow access to memory by either the on-board microcomputer or the host system on request. The onboard SRAM is 64 bits wide for the fastest possible D64 VMEbus transfers (allows for single cycle, 64 bit wide access to SRAM). The ABI supports A24 or A32 VMEbus addressing modes.

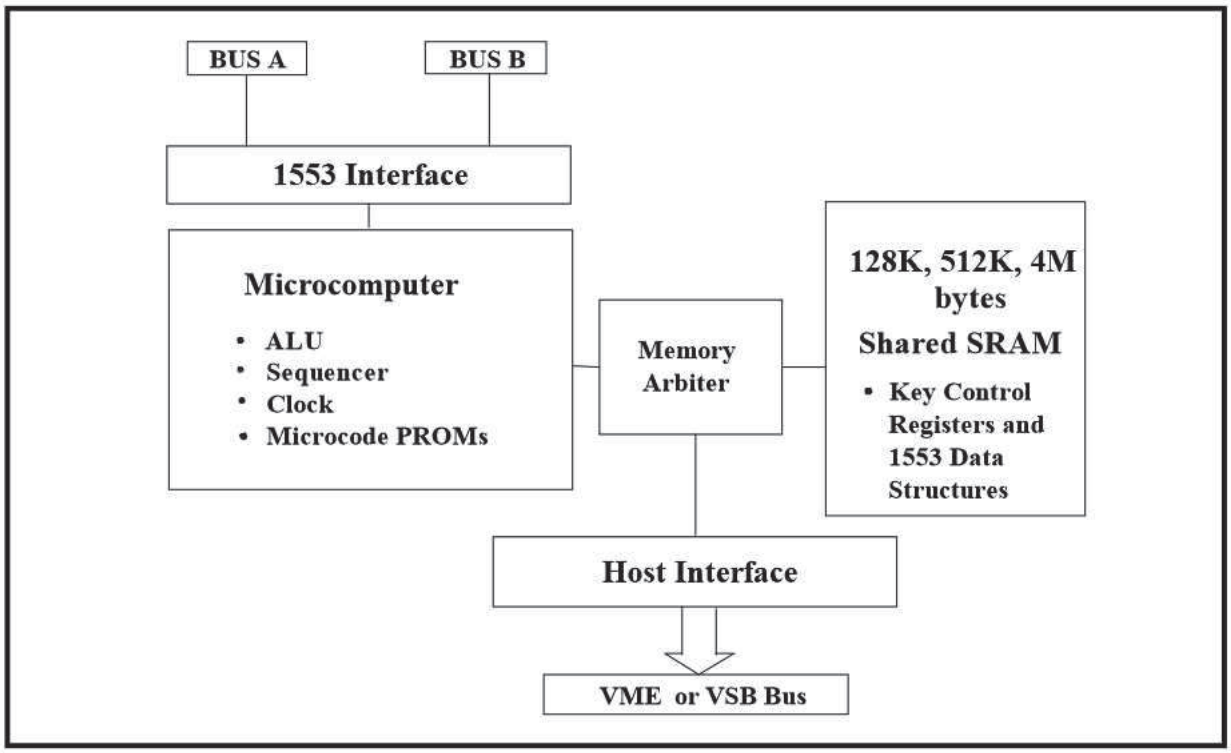


Figure OVW-1 ABI Architecture

The user's controlling application program initializes and downloads into the ABI memory, the data structures and control registers for BC, RT, Monitoring and Interrupts. BC data structures consist of linked-list encoded command blocks which the microcode program interprets for proper BC command message simulation. The BC linked-list allows for easy construction of minor and major frame formats. RT data structures consist of word array blocks or tables, arranged by RT address, which provide holding areas for Status and Data Words. There are two types of monitor structures: Map Monitoring utilizes linked-list word buffers and Sequential Monitoring uses double word buffers. Map Monitoring stores real-time 1553 message traffic in linked-list data word buffers shared with RT functions. Sequential Monitoring provides double-buffering for time-stamped 1553 data logging. For interrupt events there is a

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double-buffered Interrupt queue data structure which provides the host system with information for ABI generated interrupts. All of these data structures have root addresses and setup information stored in a small area of reserved RAM called **control register** memory.

The host system always has real-time access to the data buffers used for BC command blocks, RT simulation, map monitoring, sequential monitor buffers, and interrupt queues. This access provides the user with an advanced 1553 interface to the host system.

ABI VMEbus Master Overview

The ABI is capable of direct memory access (DMA - also known as VMEbus block) transfers as a VMEbus master. During DMA transfers, data buffers can be automatically transferred between ABI memory and host memory. There are two DMA channels on the ABI: a host channel where the host starts a DMA transfer to/from ABI memory, and an internal ABI channel where 1553 events in BC, RT and Sequential Monitor data structures trigger a DMA transfer. ABI 1553 events which may trigger DMA transfers include the receipt of a 1553 message in a BC or RT buffer and a Sequential Monitor buffer swap (one data logging buffer fills and a swap occurs for double buffering). An example of a host initiated transfer is the user's application program commanding the ABI to read or write to VMEbus memory. The following features are programmable on both internal and host blocks: transfer address and data widths (A24/32 and D32/D64), completion interrupts, Bus Request level, priviledged/supervisor mode designation, and address increment/no increment (for memory or FIFO transfers).

This automated DMA mechanism greatly reduces the host's need to service interrupts or conduct polling of 1553 data buffers to receive or monitor 1553 bus data. Furthermore, since 1553 data is automatically transferred from ABI to host memory, the host application code processes 1553 data in local memory, optimizing processor performance (many processors have very efficient local memory schemes, but process I/O or VMEbus events degrade overall performance).

The following paragraphs detail the host interface to the ABI control registers, host DMA channel programming, and on-board timer setup. They are followed by subsections for BC, RT, Monitor and Interrupt data structures.

Addressing Considerations for Host Application Programs

The ABI module is a shared memory device where the memory appears to the host system software as a single contiguous block. Virtual memory systems such as UNIX and VMS require some type of mapping procedure to tie the physical ABI memory address to the actual host program memory. Physical memory systems such as VxWorks, DOS and PDOS can usually access the ABI memory directly through program addressing. Please see the 1553 Interface Libraries manual for more details on ABI module mapping to host computer systems.

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NOTE: The discussions throughout this section refer to word (16 bits) addressing of ABI control registers and data structures. Like the 1553 bus, the ABI interface is 16-bit word aligned with the right-most bit being the least significant and numbered "0". Most host systems access memory on byte boundaries which means any address mentioned in this section must be multiplied by two (or shifted one bit left) to determine the proper byte address. Table OVW-1 lists user accessible control registers and provide both the word and byte address in the ABI memory space.

When an ABI is installed, a unique base address for the board must be selected in the host address space. This manual section refers to offsets relative to a base address of zero and in **word** boundaries (addresses 0000-FFFFh). Host systems which simply use physical addressing to access the board construct an address by adding the offset to the base address. If this type of host system places the ABI module at **byte** address 400 0000h, the ABI byte address range would be 400 0000h to 401 FFFEh for a 64-kilobyte model (FFFFh is shifted one bit left to obtain 1FFFEh, then added to base address 400 0000h).

Virtual memory systems obtain a pointer from the operating system which is used to subsequently access the board. This pointer is used with the offset to access a specific location on the ABI. *Note that the ABI does not support byte accesses.*

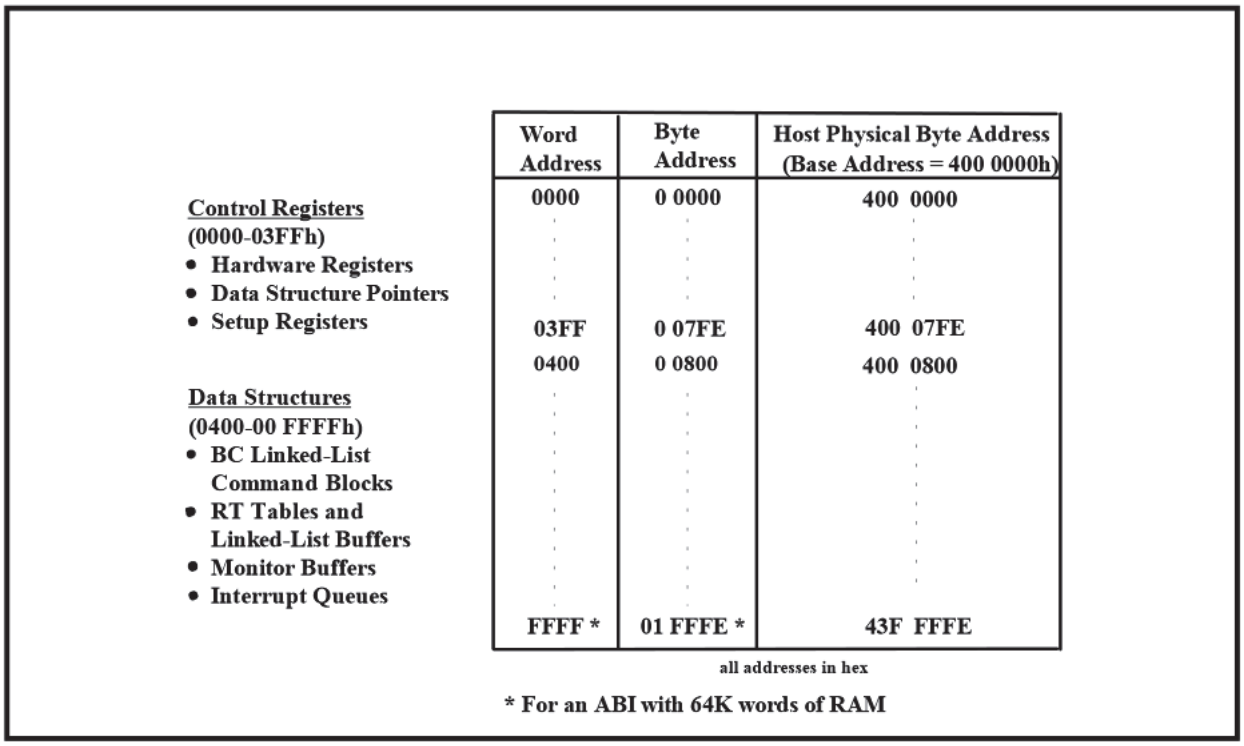


Figure OVW-2 ABI Memory Organization

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ABI Memory Organization

Figure OVW-2 shows the RAM sections for ABI control registers and data structure area. The ABI is unique in that user defined BC command block chains, RT response tables, Monitor data structures, and Interrupt queues can be located in any location above 03FFh. This allows great flexibility in the host software because data structures can be defined in host memory and copied into any ABI memory location above 03FFh. Areas below 0400h are reserved for control registers that the host software accesses for hardware initialization and pointer definitions to data structures in the 0400h to 01 FFFFh area.

ABI MEMORY CONFIGURATION IS DEPENDENT ON PURCHASED MEMORY OPTIONS. THE STANDARD BOARD COMES WITH TWO SRAM SIMS OF 128K BYTES. LARGER MEMORY OPTIONS INCLUDE 512K BYTES AND 4M BYTES. PLEASE SEE THE FRONT COVER PAGE OF THIS MANUAL FOR INFORMATION ON THE PURCHASED CONFIGURATION.

If the ABI module contains 128 kilobytes of memory, the maximum word address for data structures is FFFFh. If the module contains 512 kilobytes, the maximum word address is 3 FFFFh. If it contains four megabytes, the maximum word address is 1F FFFFh.

Upon ABI power-up, the host software must perform two steps to process 1553 data:

1. Initializes ABI memory.

2. Starts up an on-board microcode program through a defined procedure of accesses to control registers.

Next, the host software loads BC, RT, Monitor, and Interrupt data structures into upper ABI memory, and programs the control registers in lower ABI memory with initial data structure addresses. The host then sets a flag in a reserved control register that tells the ABI microcode that data structure addresses have been loaded and 1553 data processing can begin.

VMEbus Configurations

The ABI-V4 has two possible sets of VMEbus interrupt levels and vectors. One of these sets is used for microcomputer events where the ABI microcode program generates an interrupt based on a 1553 event. This type of interrupt is programmed by the user in ABI data structures. The second set is reserved for DMA events where the host computer receives an ABI interrupt after the successful completion or error detection of an ABI initiated VMEbus master transfer (DMA transfer to/from the host as bus master). For either function, the interrupt level and vector values are programmed in reserved ABI control registers by the host prior to starting the ABI microcode program. The registers used for this function are CSR, DMA CNTL, INTV_1553, and INTV_DMA. They are described in Table OVW-1.

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The following paragraphs review the control register area of memory and provide useful hints for successful ABI operations. The subsections "BC Simulation", "RT Simulation", "Bus Monitoring," and "Interrupts" detail the actual data structures used in each mode of operation.

Control Registers: 0000-03FFh

The memory area below 0400h is reserved for ABI hardware control registers, data structure pointers and setup registers. The first 64 words (0000 to 003Fh) are ABI hardware registers accessed by the host system only during ABI startup, ABI clock programming/reading and for interrupt handling. The main hardware register is the Control/Status Register (CSR) located at address 0000. This register enables ABI microcode operations and controls other fundamental operations like interrupt enabling. Besides the CSR, there are only a handful of hardware registers the host software should access (for proper microcode program startup and setting ABI clock options).

The host always has access to the CSR. There is a bit in this register that enables or disables host access to the remaining hardware registers. The "Microcode Initialization" subsection of this manual details the proper startup procedure and the disabling of hardware register access.

Control Registers 0040h - 03FFh contain microcode program registers, pointers and setup registers, and microcode scratch-pad registers. The host software uses this area of memory to initialize addresses and buffer sizes for data structures located above 03FFh. Some control registers in this area provide definition settings for 1553 simulation and monitoring functions, such as BC intermessage gap times, BC retry counts, RT response times, etc. Another group of control registers in this area make up an error table which provides the host with a comprehensive listing of the error status of 1553 protocol and ABI microcode execution. Tables OVW-1 and OVW-4 provide detailed descriptions of all user accessible control registers from 0000h to 03FFh. **Reading or writing to control register locations not listed in these tables will produce unpredictable results.**

Data Structure Memory: 0400-3F FFFFh

This area of memory is reserved for user configured data structures for BC command lists, RT response and data buffers, Monitor buffers, and Interrupt queues. All data structures have root addresses held in a respective control register as detailed in Table OVW-1. Details of data structures for BC, RT, Monitor, and Interrupt functions are detailed in their respective subsections of this manual.

There are required minimum length data structures for RT Simulation/Map Monitoring, Sequential Monitoring, and Interrupt queues. Required structures occupy only a fraction of the data structure area (less than 512 words), leaving nearly 63 kilobytes for user defined applications.

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Control Register Descriptions

Tables OVW-1 and OVW-4 provide a comprehensive list of all user-accessed control registers in the 0000 to 03FFh memory area. Table OVW-1 is divided into functional sections. Each register has a program acronym, word and byte address, page reference (in this manual), and a description. An asterisk ("*") after an acronym indicates this register must be programmed with a value or an address to a required minimum length BC, RT, Monitor, or Interrupt data structure. Hardware registers are discussed following the table.

Table OVW-1 ABI CONTROL REGISTERS

Acronym (host access)	Word Address Byte Address (in hex)	Page Ref.	Description
HARDWARE / PROCESSING			
CSR (r/w)	00 000	OVW-12	Control/Status Register. Key register for proper initialization and operation of the ABI. This is the only register always accessible to the host. See the description following this table.
HOST DMA CNTL (r/w)	01 002	OVW-14	Key register for DMA transfer operations. See the description following this table.
ABI ADDL (wo)	02 004	OVW-16	Used in conjunction with ABI ADDH. This register holds the lower 16 bits of the 21-bit ABI source/destination address used for a DMA operation to or from the VME bus.
ABI ADDH (wo)	03 006	OVW-16	Used in conjunction with ABI ADDL. Bits 0-4 of this register hold the upper five bits of the 21-bit ABI source/destination address used for a DMA operation to or from the VME bus. Bits 5-31 are not used and should be set to "0".
VME ADDL (wo)	04 008	OVW-16	Used in conjunction with VME ADDH. This register holds the lower 16 bits of the VME address (either 24 or 32 bits, as defined by bit 4 of DMA CNTL) used for a DMA operation.
VME ADDH (wo)	05 00A	OVW-16	Used in conjunction with VME ADDL. This register holds the upper 8 or 16 bits of the VME address (either 24 or 32 bits, as defined by bit 4 of DMA CNTL) used for a DMA operation.
WORD CNT (wo)	06 00C	OVW-16	This register holds the number of D64 or D32 words to be transferred over the VME bus during a DMA operation. Bit 5 of DMA CNTL specifies the data width and WORD CNT must be between 2 and 65535.
INTV_DMA (r/w)	07 00E	OVW-16	Bits 0-7 of this register set the VME Interrupt Vector for DMA transfer operations. Bit 0 is the least-significant bit.
ITCR (r/w)	08 010	OVW-17	Internal Timer Control Register. Defines the mode of operation for the timer.
ITDRL (r/w)	09 012	OVW-18	Internal Timer Data Register. Lower 16 bits of the system timer.
ITDRM (r/w)	0A 014	OVW-18	Internal Timer Data Register. Middle 16 bits of the system timer.
ITDRH (r/w)	0B 016	OVW-18	Internal Timer Data Register. Upper 16 bits of the system timer.
VVDR (wo)	0C 180	OVW-18	Controls output voltage. See the description following this table.

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Table OVW-1 ABI CONTROL REGISTERS			
Acronym (host access)	Word Address Byte Address (in hex)	Page Ref.	Description
INTV_1553 (r/w)	0E 01C	OVW-16	Bits 0-7 of this register set the VME Interrupt Vector for 1553 event interrupts. Bit 0 is the least-significant bit.
MAP (wo)	10 020	OVW-17	Holds the microcode starting address. See the description following this table.
GINT (wo)	1A 034	--	Write any value to this register to generate an interrupt. Use to test hardware interrupt handshaking.
PSTEP (wo)	3F 07E	OVW-17	Causes a "pipestep" instruction to occur. See the description following this table.
MICPC (ro)	40 080	MC-2	Microcode Product Code
MICVC (ro)	41 082	MC-2	Microcode Version Code
CMD (wo)	80 100	--	Commands the starting of 1553 bus processing. Write a non-zero value to this register to start bus processing. Write a zero to this register to halt bus processing. Program registers 82h to 9Ch prior to setting this register to a non-zero (active) value.
RESP (ro)	81 102	--	This word continuously increments in RESPONSE to CMD (above) not set to zero. This provides a simple check that the micromachine is running. While counting, this word should never be equal to zero (zero is skipped in the counting).
INTERRUPT PROCESSING			
IQRSP (wo)	82 104	INT-4	Interrupt Queue Response flag word: If IQRSP=FFFFh, host is processing interrupts; if IQRSP=0001h, processing is complete.
IQPTR1 * (r/w)	83 106	INT-4	Offset to interrupt queue 1. This queue is processed by the host computer. Each entry consists of four words: Word 1 is the interrupt code; Words 2-4 depend on the interrupt code.
IQPTR2 * (r/w)	84 108	INT-4	Offset to interrupt queue 2. This is the queue which is currently active. The host should NOT process this queue.
IQCNT1 (ro)	85 10A	INT-4	The number of entries in interrupt queue 1. This is used by the host computer's ISR to process the IQPTR1 queue.
IQCNT2 (wo)	86 10C	INT-4	The number of entries in interrupt queue 2. **Do not access this register while the ABI is processing 1553 data.**
IQNUM (r/w)	87 10E	INT-4	The number of interrupt slots in each queue. The default is 4 entries. If the number of entries exceeds the value in IQNUM, an error is generated.
SEQUENTIAL MONITOR			
M1PTR * (wo)	8C 118	MON-3	Offset to sequential monitor buffer 1. This is the active buffer. **Do not access this register while the ABI is processing 1553 data.**
M2PTR * (r/w)	8D 11A	MON-3	Offset to sequential monitor buffer 2. This is the non-active buffer. This buffer should be processed by the host computer after M1PTR and M2PTR are swapped. Wait a minimum of 20 microseconds after a swap before processing the M2PTR table.

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Table OVW-1 ABI CONTROL REGISTERS			
Acronym (host access)	Word Address Byte Address (in hex)	Page Ref.	Description
MBLEN * (wo)	8E 11C	MON-3	Unsigned 16-bit number indicating length in words of each sequential monitor buffer. Minimum length is 50 words. The microcode will swap buffer pointers when the number of words left in the buffer is less than the minimum buffer length.
MBFLG (r/w)	9F 13E	--	Sequential monitor buffer control word. Set to "1" to cause the monitor buffer pointers to swap. Set to "2" to cause a swap and a Monitor Buffer Swap interrupt code 2. When the operation is completed, the microcode sets this word to "0".
SMBCNT (wo)	AB 14D	MON-4	Sequential Monitor Buffer Counter.
BUS CONTROLLER (BC)			
BCIPTR (wo)	8F 11E	BC-9	Initial Bus Control program block. This location is continuously monitored by the ABI's microcode. When BCIPTR is non-zero, the microcode will execute a chain of BC program blocks beginning at the offset defined in BCIPTR.
BCCPTR (r/w)	90 120	BC-9	Contains the offset to the currently active BC program block. Load with "0" to stop BC execution after the current BC program block finishes.
BCLPTR (r/w)	91 122	BC-9	Contains the offset to the last BC program block that executed before the microcode stopped processing BC program blocks.
BCSMSK (r/w)	92 124	BC-9	BC status mask. If bit 2 of the flag word in a BC program block is set to "1", the contents of BCSMSK is logically "ANDed" with the returned status word(s). If the resultant is non-zero, an interrupt occurs. The Continue-On-Error/Masked Status bit in the flag word of the BC program block determines if the BC chain will be stopped.
BCERVL (ro)	A7 14E	--	Contains the last BC error table entry. This value is reset to "0" at the start of each BC chain.
BCIGP (r/w)	AE 15C	RT-24	Use to change the intermessage gap time for BC messages: *BCIGP = (time_in_microseconds - 4) * gap_count* (time_in_microseconds = desired gap time, must be > 4) (gap_count = MIP rating of ABI) Accurate to within five microseconds of desired gap time.
BC RETRY			
BRTCNT (r/w)	AF 15E	BC-10	Number of retries to be performed for a BC error condition. The maximum is 16.
BRTBUS (r/w)	B0 160	BC-10	Defines bus (A or B) to be used for BC retries. Bit 0=1st retry of message, Bit 1=2nd retry of message, etc. If bit=0, retry is on the same bus as original message. If bit=1, retry is on the opposite bus.
BRTCMD (r/w)	B1 162	BC-10	Contains the last BC command that was retried. This value is reset to "0" at the start of each BC chain.
BRTRTC (r/w)	B2 164	BC-10	Contains the actual number of retried messages. This value is reset to "0" at the start of each BC chain.

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Table OVW-1 ABI CONTROL REGISTERS

Acronym (host access)	Word Address Byte Address (in hex)	Page Ref.	Description
			REMOTE TERMINAL (RT)
SWTPTR * (r/w)	88 110	RT-3	The Status Response Table pointer is an offset to the beginning of a 64-word table. The first 32 words are for the host computer; the last 32 words are for the microcode. Each entry corresponds to an RT. The actual status response word sent to the 1553 bus is obtained through a logical "OR" operation involving the host entry and the microcode entry for a particular RT, except for the ME bit. The ME bit is set by the microcode in the microcode entry. A non-zero entry enables the corresponding RT for simulation. RT 0 is a special case; it is enabled by storing "0400h" in the first entry of the table.
ATPTR * (r/w)	89 112	RT-5	The Address Table pointer is an offset to a 32-word table arranged by RT (the RT address table) whose entries are each an offset to a buffer pointer table. A buffer pointer table is a table of 64 words; the first 32 are for the receive subaddresses, the last 32 are for the transmit subaddresses. Each entry is an offset to an RT data buffer linked list. An RT data buffer consists of a link offset, a flag word, and 32 data words.
FTPTR * (r/w)	8A 114	RT-11	Filter Table pointer is an offset to a table of 32 words arranged by RT number. Each entry of this table is an offset to a subaddress filter table. A subaddress filter table is 64 words: 32 for receive subaddresses, 32 for transmit subaddresses. Each entry of the subaddress filter table contains control bits for a particular RT-t/r-SA. Bit 0: Sequential Monitor Enable, Bit 1: Interrupt on Message Received, Bit 2: Sequential Monitor Buffer Swap on Message, Bit 3: Generate Parity Error.
			RT MODE COMMANDS
RTPPTR * (r/w)	95 12A	RT-17	Remote Terminal Phase Table is an offset to a 32-word table arranged by RT number. It is used by the microcode for saving current transmitter state in response to Transmitter Shutdown mode code and for saving current terminal flag inhibit state for Inhibit Terminal Flag Bit mode code.
BITPTR * (r/w)	96 12C	RT-21	BITPTR is an offset to a 32-word table arranged by RT number. This table contains the BIT entry sent for each RT upon receipt of a transmit BIT mode command.
LCDPTR * (r/w)	97 12E	RT-20	LCDPTR is an offset to a 32-word table arranged by RT number. This table contains the last command word sent to each RT. The last command for a particular RT is obtained from this table and transmitted upon receipt of a Transmit Last Command mode code.
TVWPTR * (r/w)	98 130	RT-18	TVWPTR is an offset to a 32-word table arranged by RT number. This table contains the vector word entry sent for each RT upon receipt of a transmit vector word mode command.

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Table OVW-1 ABI CONTROL REGISTERS			
Acronym (host access)	Word Address Byte Address (in hex)	Page Ref.	Description
LSWPTR * (r/w)	99 132	RT-16	LSWPTR is an offset to a 32-word table arranged by RT number. This table contains the status word for the last valid command for each RT. The last command for a particular RT is obtained from this table and transmitted upon receipt of a Transmit Last Status mode code.
LSYPTR * (r/w)	9A 134	RT-19	LSYPTR is an offset to a 32-word table arranged by RT number. This table contains the value sent by the BC for each RT on the last synchronize with data word mode command.
PROPTR * (r/w)	9C 138	RT-13	PROPTR is an offset to a 32-word table arranged by RT number. Each entry contains a protocol word definition - Bit 0: must be "0", Bit 1: enable map monitor, Bit 2: dynamic bus control accept, Bit 3: 1553B treatment of SA31, Bit 4: Bus A failure, Bit 5: Bus B failure.
MIMPTR (r/w)	9E 13C	RT-23	MIMPTR is an offset to a 64-word table arranged by RT number. Each entry of the table is two words. The bits of an entry correspond to a particular mode command. A set bit indicates that the ABI will generate a MIM interrupt upon receipt of a mode command (corresponding to the RT associated with that set bit).
RT VARIABLE STATUS RESPONSE GAPS			
RSPGPA (r/w)	AC 158	RT-24	Use to change the maximum allowable status response gap time: *RSPGPA = (time_in_microseconds - 2) * gap_count* (time_in_microseconds = desired gap time, must be > 2) (gap_count = MIP rating of ABI) Accurate to within five microseconds of desired gap time.
RSPGPS (r/w)	AD 15A	RT-24	Use to change the actual RT status response gap time: *RSPGPS = (time_in_microseconds - 4) * gap_count* Accurate to within five microseconds of desired gap time.
DMA PROCESSING QUEUE			
DMAERR (ro)	B5 16A	OVW-21	DMA error reporting word. If this register contains a non-zero value, an error has occurred during a DMA transfer. The most common error is "overflow"; ie., more transfers were requested by the user than could be accomplished.
DMAQPT (wo)	B6 16C	OVW-21	DMA Queue Pointer word. Points to a DMA processing queue that contains DMA transfers requested but not yet performed. This queue is allocated in Control Register memory by default with a length of four but may be reallocated in Data Structure memory by the user.
DMAQLN (wo)	B7 16E	OVW-21	DMA Queue Length. This register contains the length of the DMA processing queue. This length defaults to four unless the user defines a larger queue in Data Structure memory.
LEGEND: * Entry required for proper microcode operation. r/w = read/write, ro = read only, wo = write only Word offset locations between 80h and 3FFh that are not mentioned here are reserved. Accessing these locations will produce unpredictable results.			

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Key Hardware Registers

Control and Status Register (CSR)

This is the only hardware register (memory between 0000 and 003Fh) always accessible to the host software. The user can read or write to this register because the RAM arbiter always has direct access to the internal microcomputer register 0000. This register is key to proper initialization and operations of the ABI. Figure OVW-3 and Table OVW-2 detail the bit definitions for the CSR register. Carefully read the bit descriptions because undesired operations may result from inadvertent reads to and writes from this register. Note that host access to registers 0001-003F can be disabled through bit 8.

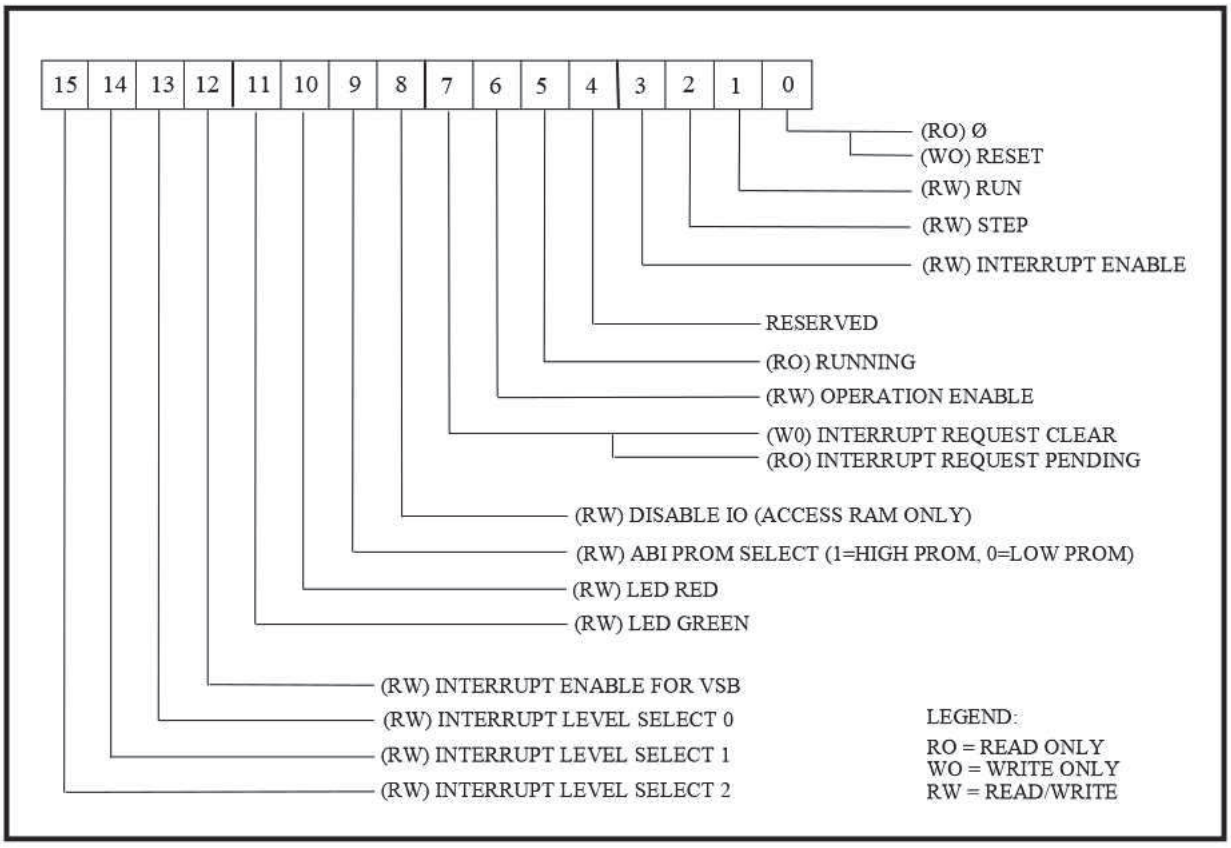


Figure OVW-3 CSR Bits

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Table OVW-2 Control Status Register Bit Definitions		
BIT #	**NAME**	**DESCRIPTION**
0	RESET	Set this bit to "1" to clear the interface. This will set all CSR bits, including the RESET bit, to "0" (except for LED GREEN).
1	RUN	Set this bit to "1" to cause the processor on the ABI to begin execution. Set this bit to "0" to stop all processing.
2	STEP	Set this bit in conjunction with the RUN bit to single-step the ABI microcode. **This function is for microcode development purposes only.**
3	INT ENA	Set this bit to "1" to cause interrupts generated by the ABI to be passed to the host bus.
4	RESERVED	Do not change this bit. (When writing to the CSR, **this bit must be "0"**.)
5	RUNNING	This is a status discrete bit which indicates that the ABI processor is running. When the RUN bit is set to "1" by the host, the ABI microcode will begin execution and will set this bit to "1"; when the RUN bit is set to "0" the microcode will set this bit to "0" .
6	OP ENA	Operation enable is an output discrete bit. When this bit is set to "0", it sets the internal instruction register of the processor to "0". It must be set to "0" prior to restarting a new microprogram and must be set to "1" when the RUN bit is set to "1". **It must not be set to "0" while the ABI processor is running.**
7	INT REQ	This bit has two functions: It is read as an Interrupt Request Pending bit and is written to as an Interrupt Clear bit. If this bit is set to "1" when read, an interrupt request is pending. If a "1" is written to this bit, it resets this pending interrupt. **VME board:** This bit and the pending interrupt will be set to "0" by the hardware interrupt acknowledge cycle. **Clear (set to "0") this bit once at initialization and never again unless polling is used.** **PC board:** Each time interrupts are serviced, the interrupt handler must clear the pending interrupt.
8	DISABLE I/O	Set this bit to "1" to disable access to the ABI I/O registers 01h through 3Fh. The region 01-3Fh will appear as normal RAM. The CSR is still accessible. It is a good idea to set this bit to "1" after the MAP register has been loaded with the desired microprogram number. **This bit must be "0" to load the map register.**
9	PROM SEL	Set this bit to "1" to select the upper half of PROM for use; set to "0" to select the lower half.
10	LED RED	This bit controls the PROG LED on the front panel of the ABI. Set to "1" to turn the LED red.
11	LED GREEN	This bit controls the PROG LED on the front panel of the ABI. Set to "1" to turn the LED green.
12	VSB INT ENA	Set this bit to "1" to cause interrupts generated by the ABI to be passed to the host VSB bus.
13	INTR LEV 0	Least significant bit of the three-bit binary value that selects the VME interrupt level to be used by the ABI. *This interrupt level is for normal 1553 event interrupts, not DMA interrupts.*

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Table OVW-2 Control Status Register Bit Definitions		
BIT #	**NAME**	**DESCRIPTION**
14	INTR LEV 1	Middle bit of the binary value that selects the VME interrupt level to be used by the ABI. *This interrupt level is for normal 1553 event interrupts, not DMA interrupts.*
15	INTR LEV 2	Most significant bit of the binary value that selects the VME interrupt level to be used by the ABI. *This interrupt level is for normal 1553 event interrupts, not DMA interrupts.*

Host DMA Channel Registers (DMA CNTL, ABI ADDH, ABI ADDL, VME ADDH, VME ADDL, WORD CNT)

The host may initiate a DMA transfer operation by programming these six registers directly at any time. Figure OVW-4 and Table OVW-3 define the bit values for HOST DMA CNTL (VMEbus Direct Memory Access Control Word). Descriptions for the remaining five registers follow Table OVW-3.

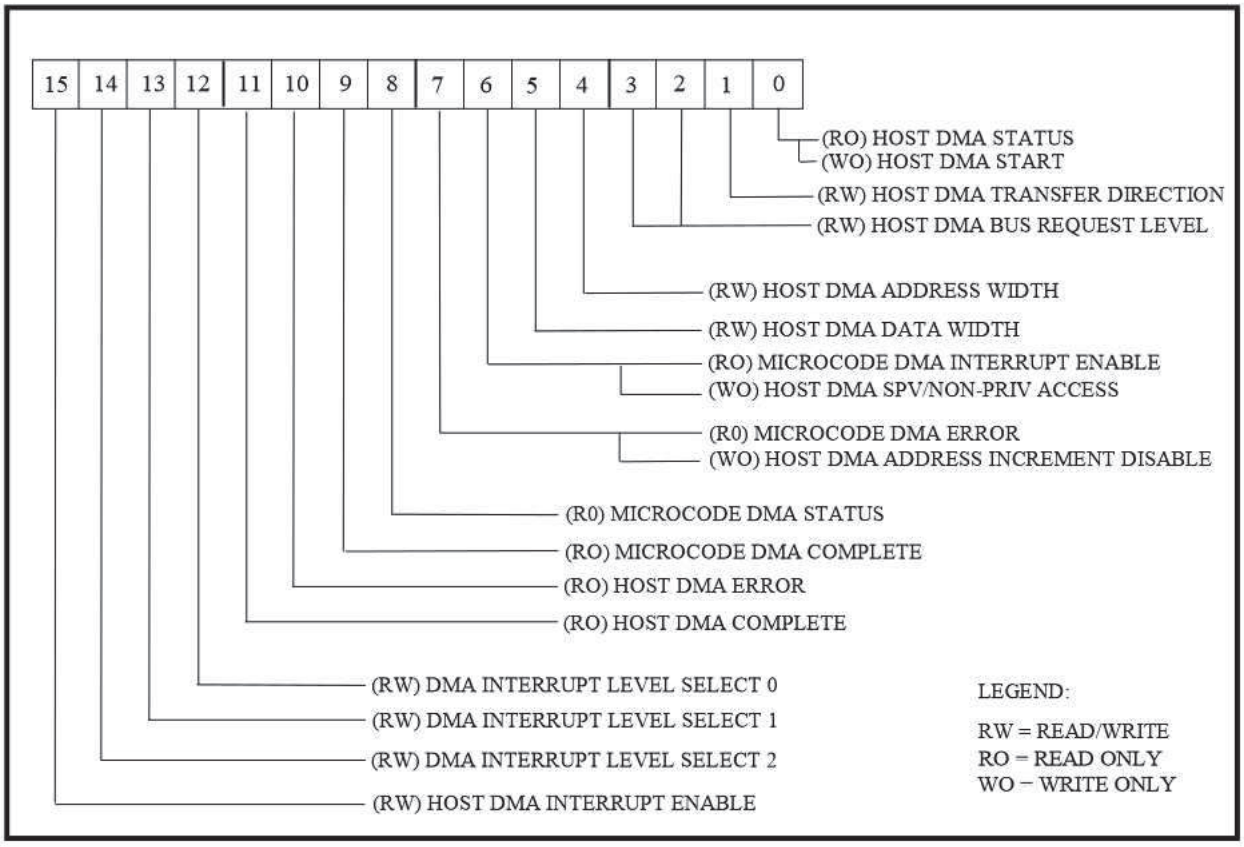


Figure OVW-4 HOST DMA CNTL Word Bits

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Table OVW-3 HOST DMA CONTROL WORD
Bit 0 is right-most bit and least-significant.

BIT(s)/NAME	Bit Values	Comment
Bit 0 Host DMA Status/ Host DMA Start	**As read:** 1 = DMA Transfer in Progress **As written:** 1 = Start DMA Transfer	Write a "1" to this bit to start a Host DMA transfer. The bit value will remain "1" until the DMA transfer is complete.
Bit 1 Host DMA Transfer Direction	0 = Transfer from ABI to VME 1 = Transfer from VME to ABI	This bit controls the direction of master transfers by the ABI. Set to "0" to cause the ABI to transfer data from ABI ADDH/L to VME ADDH/L. Set to "1" to cause the ABI to perform a master transfer from VME ADDH/L memory to ABI ADDH/L.
Bits 2,3 Host DMA Bus Request Level	00 = Bus Request Level 0 01 = Bus Request Level 1 10 = Bus Request Level 2 11 = Bus Request Level 3	These bits control the bus level for the VME transfer. "11" is typically the highest, but this setting is dependent on the bus control settings/protocol of the slot 0 VME arbiter.
Bit 4 Host DMA Address Width	0 = A32 1 = A24	This bit selects either a 32 or 24 bit address width for the VME transfer. The VME address corresponds to the 32 or 24 least significant bits of VME ADDH/L, respectively.
Bit 5 Host DMA Data Width	0 = D32 1 = D64	This bit controls the width of data transfers to/from VMEbus memory. The WORD CNT value is in increments of this bit setting - i.e., if bit 5 is set to "0" and WORD CNT is 16, then 16 32-bit transfers will occur.
Bit 6 Microcode DMA Interrupt Enable/ Host DMA Spv/Non-Priv Access	**As read:** 1 = Interrupt after Microcode DMA **As written:** 0 = Non Privileged (NORMAL) 1 = Supervisory	This bit has two functions. **As read**, it contains the state of the Microcode DMA Interrupt Enable bit. **As written**, it controls memory address modifiers. The ABI-V4 responds to either mode.
Bit 7 Microcode DMA Error/ Host DMA Address Increment Disable	**As read:** 1 = Error in Microcode DMA **As written:** 0 = Increment VME Address 1 = No Address Increment	This bit has two functions. **As read**, it indicates whether an error occurred during a Microcode DMA Transfer. **As written**, it controls automatic VME address increments for ABI block transfers. In short, this bit allows for transfers to/from regular memory or FIFOs. The amount the address is incremented depends on the setting of bit 5; a D32 transfer increments the VME address by 4 and a D64 transfer increments the address by 8.
Bit 8 Microcode DMA Status	**As read:** 1 = Microcode DMA in progress **As written:** Reserved - Set to "0"	When read, this bit indicates whether a Microcode DMA Transfer is in progress. Set this bit to "0" when writing to this register.

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Table OVW-3 HOST DMA CONTROL WORD Bit 0 is right-most bit and least-significant.		
BIT(s)/NAME	**Bit Values**	**Comment**
Bit 9 Microcode DMA Complete	**As read:** 1 = Microcode DMA Complete **As written:** Reserved - Set to "0"	When read, this bit indicates whether a Microcode DMA Transfer has completed. This bit is automatically cleared after being read. Set this bit to "0" when writing to this register.
Bit 10 Host DMA Error	0 = Host DMA Transfer completed successfully 1 = Error occurred during Host DMA Transfer	When read, this bit indicates whether an error occurred during a Host DMA Transfer. This bit is automatically cleared after being read.
Bit 11 Host DMA Complete	1 = Host DMA Transfer has completed	When read, this bit contains the state of the Host DMA Complete bit. This bit is automatically cleared after being read.
Bits 12,13,14 DMA Interrupt Level	000 = Interrupt Level 0 | 111 = Interrupt Level 7	These bits control the interrupt level for both Host and Microcode initiated DMA transfers. "111" is the highest level.
Bit 15 Host DMA Interrupt Enable	0 = Disable Interrupt after DMA 1 = Enable Interrupt after DMA	This bit enables/disables an interrupt by the ABI to the VMEbus after a block (DMA) transfer has completed. This feature allows the ABI to notify the host processor that a DMA transfer has completed for synchronization.

ABI ADDL, ABI ADDH

ABI ADDL and **ABI ADDH** (ABI Source Address Low and High) define the ABI source address for DMA operation to the VME bus. These two words combine to make up a 21-bit ABI address (includes all bits of ABI ADDL and bits 0-4 of ABI ADDH); bits 5-31 of ABI ADDH are not used and should be set to zero. The source address can be any ABI local address. (ABI addresses are in words, not bytes.)

VME ADDL, VME ADDH

VME ADDL and **VME ADDH** (VMEbus Address Low and High) combine to make the VMEbus destination address words (24 or 32 bits as defined by bit 4 of DMA CNTL). VME memory, as with ABI memory, is big-endian oriented. Most VMEbus processor or reflective memory modules are byte oriented; thus, D32 or D64 transfers must start on a four byte or eight byte boundary.

WORD CNT

WORD CNT is the number of transfers to be performed over the VME bus, minus one. The count value is for either D64 or D32 words, as designated by bit 5 of the DMA CNTL word. For example, if WORD CNT is 127 and bit 5 is set to "1" (selecting D64), 128 64-bit words will be transferred. Thus, the word count is not a byte count, but a VME transfer count. The minimum transfer value is zero and the maximum is 65535.

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Host Initiated DMA Transfer

Complete the following steps to initiate a Host DMA Transfer.

1. Write a control value to HOST DMA CNTL (offset 0001h), setting bit 0 to "0".
2. Write the lower 16 bits of the ABI internal address to ABI ADDL (offset 0002h).
3. Write the upper 8 bits of the ABI internal address to ABI ADDH (offset 0003h).
4. Write the lower 16 bits of the VMEbus address to VME ADDL (offset 0004h).
5. Write the upper 16 bits of the VMEbus address to VME ADDH (offset 0005h).
6. Write the length of the transfer minus one to WORD CNT (offset 0006h).
7. If using interrupts, write a VMEbus Interrupt Vector to INTV_DMA (offset 0007h).
8. Write the control value written in step 1 logically OR'd with "1" to HOST DMA CNTL. This sets bit 0 to "1", causing the Master interface to start the Bus Request cycle and transfer data to or from the VMEbus.

VMEbus Interrupt Level and Vector Programming (CSR, DMA CNTL, INTV_DMA, INTV_1553)

Four registers are used to set interrupt levels and vectors. For normal 1553 event interrupts, program bits 13, 14, and 15 of the CSR register to set the interrupt level (see Table OVW-2). Program bits 0-7 of INTV_1553 to set the interrupt vector for normal 1553 interrupts. For DMA interrupts, program bits 8, 9, and 10 of the DMA CNTL register to set the interrupt level (see Table OVW-3) and bits 0-7 of INTV_DMA to set the interrupt vector.

MAP control register

Write the microcode starting address to this register prior to execution. There are a variety of legal microcode starting address locations that correspond to ABI Built-In Test (BIT) routines, utility microcode programs, and the main body of 1553 microcode programs.

PSTEP control register

Write any value to this register to cause a "pipestep" instruction to occur. This instruction latches the microcode and is necessary for proper startup. Access to this register other than for initialization is not recommended.

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Timing Hardware Registers

The **ITCR**, **ITDRL, ITDRM** and **ITDRH** registers configure the 48-bit hardware timer used for 1553 message time stamping in ABI Sequential Monitoring. This timer may be read, reset, or preset as desired by the host software. The ABI timer may be driven from an internal clock or from an external source (auxiliary front panel connector - or the P2 connector for version 03 boards only).

ITCR (Internal Timer Control Register)

This register defines the mode of operation of the timer and contains eight bits, described below.

Bit 0 - Clock Enable/Disable
Set this bit to "1" to enable the internal clock. Default for this bit is "1" or enabled.

Bit 1 - Reserved

Bit 2 - Timer Clear
This signal is used to clear the timer from software. To clear the timer to a count of zero, set bit 2 to "1" and hold at "1" for the entire clock period (one microsecond). The timer will remain cleared until bit 2 is cleared and the timer is enabled.

Bit 3 - External Clock Select
Set this bit to "1" to use an external clock.

Bit 4 - External Enable Output
Set this bit to "1" to activate the external enable output.

Bit 5 - External Clock Master Enable
Set this bit to "1" to configure this ABI as the master clock. When multiple ABIs are in use, only one module may act as the master clock.

Bit 6 - External Enable Input
This is a **read only** bit which indicates whether the external enable signal is activated (1 = enabled, 0 = disabled).

Bit 7 - Internal/External Clears
This is a **read only** bit which indicates whether any one of five internal/external signals is cleared (if any signals are set to "1", this bit will be "1").

NOTE: The state of the Timer Clear bit should only be changed when the timer is disabled.

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ITDRL, ITDRM, ITDRH (Internal Timer Data Registers)

These registers are used to preset or read the 48-bit timer used for time stamping 1553 messages. ITDRL holds the lower 16 bits, ITDRM holds the middle 16 bits, and ITDRH holds the upper 16 bits of the 48-bit timer. Perform the following steps to write to these registers:

1. Clear bit 0 of the ITCR to disable the timer.

2. Write the desired values to ITDRH, ITDRM, and ITDRL, in that order.

3. Set bit 0 of the ITCR to enable the timer.

When bit 0 of the ITCR is enabled, the hardware will load the 48-bit internal timer with the programmed values. This function can be performed with internal or external timer configurations.

Perform the following steps to read these registers:

1. Read ITDRL, latching the upper 32 bits of the timer.

2. Read ITDRM and ITDRH. Because the timer is latched, it may be read anytime in the future using only ITDRM and ITDRH, as long as ITDRL is not re-read.

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VVDR (Variable Voltage DAC Register)

This register (offset 001Fh) controls the amplitude of ABI transmitted 1553 signals (during BC or RT simulation). By writing to this register, the host software can set the ABI output voltage levels from 0 to 21.5V (peak-to-peak). Table OVW-4 provides typical output voltages for given register values. The actual output voltage may be affected by bus loading (the number of terminals, length of bus, etc.). The microcode 1553 main body initializes this register to 00F0h (about 21.5 volts). The BIT 6 routine and Send Utility microcode programs require this register to be programmed for proper operations.

Table OVW-4 Variable Voltage DAC Register

DAC Value	Nominal 1553 Bus Voltage (peak-to-peak)
F0 h	21.5
E0 h	20
D0 h	19
C0 h	17.5
B0 h	15.5
A0 h	14
90 h	12.5
80 h	10.5
70 h	9
60 h	7.5
50 h	6.5
40 h	4.5
30 h	2.9
20 h	1.1
10 h	0.4
00 h	0

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DMAERR, DMAQPT, DMAQLN (DMA Processing Queue Registers)

If a DMA transfer request occurs while a DMA transfer is in progress, the ABI microcode places the request in a processing queue. DMA transfer requests stored in this queue are processed in the order they are received. The default location for the queue is word address 01E0h, pointed to by **DMAQPT**. The queue length, having a default value of 0004h, is stored in **DMAQLN**. If the number of pending DMA transfer requests exceeds the value stored in DMAQLN, an overflow error will occur, resulting in a non-zero value in **DMAERR**.

The size of the queue at word address 01E0h is limited to four words; however, a larger queue may be allocated in Data Structure memory (word addresses above 0400h) if desired. To define a larger queue, program the new word address in DMAQPT and the new length in DMAQLN.

Error Table

The Error Table is a region in RAM used by the microcode to store information on 45 possible errors. Each entry in the table, shown in Table OVW-5, consists of two words and is identified by the address of the first word. The first word provides information (such as a pointer offset to a BC data structure) about the error. The second word is an error counter which indicates the number of times the error has occurred.

Table OVW-5 ABI Error Table

Word Address	Byte Address	Class	Description
100h	200h	H	This error indicates an initialization failure of some of the internal logic after power up.
102h	204h	H/P	This error results either from a hardware failure or from severely distorted transmissions on the bus. It indicates that a data word was not received after detection of bus activity.
104h	208h	M	This error indicates that the microcode has entered an invalid state.
106h	20Ch	P	A word that did not have a command sync was received after a transmit command.
108h	210h	P	A word with a data sync was received when expecting a status word for a receive command.
10Ah	214h	P	This error typically results from other errors on the bus. It occurs when the microcode is waiting for a new command. Any word received that is not a command sync causes this entry to be updated. The microcode was expecting a command sync, but received a data sync.

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Table OVW-5 ABI Error Table

Word Address	Byte Address	Class	Description
10Ch	218h	H/P	This error results either from a hardware failure during a transmit command or from severely distorted transmissions on the bus. It occurs when bus activity is detected through a command sync but a completed transmit command is not received. The microcode receives a SARDY discrete, but never receives the required DRDY discrete.
10Eh	21Ch	P	An apparent transmit command was partially received, but contained a parity error when completed and was not processed.
110h	220h	I	A transmit command has been received for an simulated or real-time monitored RT, and no buffer has been defined in the buffer pointer table for the indicated subaddress.
112h	224h		Undefined
114h	228h	H/P	This error results either from a hardware failure during a transmit command or from severely distorted transmissions on the bus. It occurs when bus activity is detected through a command sync but a completed transmit command is not received. The microcode receives a SARDY discrete, but never receives the required DRDY discrete.
116h	22Ch	P	An apparent receive command was partially received, but contained a parity error when completed and was not processed.
118h	230h	P	A receive command was received when only a transmit command is valid (that is, the second command in an RT-RT message sequence).
11Ah	234h		Undefined
11Ch	238h	H/M	This error indicates that the microcode has entered an invalid state.
11Eh	23Ch	H/P	An apparent data word was received, but it contained a parity error.
120h	**240h**	**P**	**An unexpected gap has occurred in a message. This situation may result from too few data words in a message or from non-contiguous data. This error may also indicate a "no response" condition of an RT. This is the most common error condition.**
122h	244h		Undefined
124h	248h	M	This error indicates that the microcode has entered an invalid state.
126h	24Ch	H/P	This error results either from a hardware failure or from severely distorted transmissions on the bus. It indicates that an expected receive command was not received after detection of bus activity on the second RT-RT command
128h	250h	P	A gap was detected on the bus after a receive command. The receive command should have been followed by a transmit command or by data with no gap.
12Ah	254h	I	A receive command has been received for an simulated or real-time monitored RT, and no buffer has been defined in the table of buffer pointers for the indicated subaddress.

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