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Find the *Abaco Systems / SBS ABI-V5-2* at our website: ***Click HERE***

ABI-V5

MIL-STD-1553 Interface

I/O & Communications

Features

1 or 2 dual redundant 1553 channels featuring 100% concurrent and independent operation as a:

- Bus Controller
- 31 Remote Terminals
- Dual Function Bus Monitor
- Advanced VMEbus and Memory Models

Bus Controller

- Programmable frame lists
- BC-RT, RT-BC, RT-RT
- Mode codes, broadcasts, and time delays

RT Functionality

- RT level protocol selection
- RT definition tables
- Programmable response time

Bus Monitor

- Map monitoring
- Sequential monitoring
- Time stamped
- Double buffered
- Optional IRIG time decoding
- Error tables
- Definable monitoring

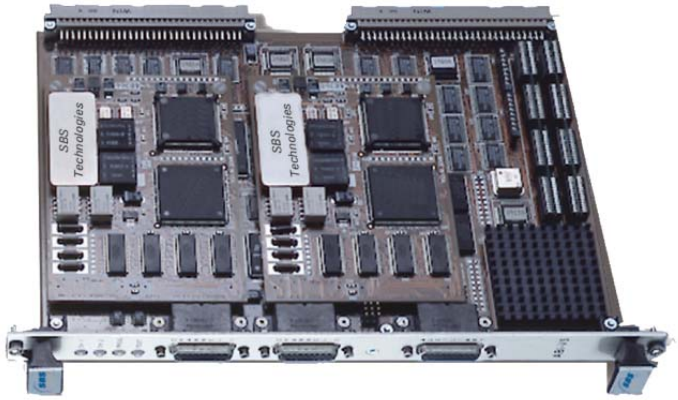
Architecture

- On-the-fly data structures
- BC and RT linked lists
- High-speed DSP
- Flexible memory structure
- Variable voltage 1553 transceivers
- 512 kB or 2 MB memory models

Software Support

- Complimentary drivers for most operating systems
- Integrated Avionics Library, including source code

Optional NASA Box-car and B-2 Models Available



ABI-V5 interface provides a flexible, multi-channel, dual redundant MIL-STD-1553 Master/Slave interface to the VMEbus backplane. The advanced VMEbus master/slave interface provides automated buffer transfers to and from host memory. DMA transfers free the host processor from time consuming polling or interrupt-handling functions. The ABI-V5 interface equips the VMEbus system with a complete 1553 interface. This includes 1553A/1553B selections, pointer-driven transmit and receive buffers and extensive programmable event interrupts.

BC simulation structures consist of linked lists of 1553 command messages: BC-to-RT, RT-to-BC, RT-to-RT, mode code, broadcast and time delay block transmissions. We define RT simulation as a simple series of pointers to RT definition tables. The RT definition tables in turn point to control data buffers. We define the bus activity we want to monitor in both the Map and Sequential monitoring modes. This provides user defined linked lists of data buffers and sequential 1553 activity. The user can time stamp and/or double buffer the 1553 activity. Both monitoring modes perform broad error monitoring. They also provide a comprehensive error table that the host processor can read at any time.

Hardware Overview

SBS bases the ABI interface upon an advanced high speed RISC and DSP, programmable logic and dual port RAM. It delivers a highly reliable hardware platform that is feature rich and user friendly. Through the 512 kB of dual port RAM (2 kB available), the host processor has access to set up, monitor, and change the 1553 interface data structures at any time. Link-list memory architecture allows the user to structure interface memory usage for the maximum in flexibility and usefulness. The ABI-V5 provides storage for on-board firmware via Flash Memory.

Software Support Overview

SBS distributed software includes host processor device drivers to the dual port control and data structures as well as an application layer to these structures. SBS also provides low-level drivers for most operating systems, and the Integrated Avionics Library with source code, with the interface at no additional cost.

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ABI-V5

Configurations

Model Number	Configuration
ABI-V5-1	Single Channel 1553 to VME interface
ABI-V5-2	Dual Channel 1553 to VME interface
IRIG	IRIG B Time Receiver (add /IRIG to product number)
MEM	2 Mbytes SRAM (add /MEM to product number)
	Consult Factory for NASA and B2 options

Specifications

ABI Functionality:
Bus Controller (BC)

- BC retry
- Minor frame timing and message scheduling
- Programmable intermessage gap
- Programmable delay gaps and null BC blocks
- Multiple BC data buffers in a linked list structure
- Error injection

Remote Terminals (RTs)

- 31 RTs and all subaddresses supported
- Transmit/Receive buffers for each subaddress
- Multiple RT data buffers in a linked list structure
- Programmable RT response time, no-response selection and no-response time-out
- Error injection

Map Monitoring

- Multiple linked buffers for each transmit/receive subaddress
- Mapped buffers read by host processor as time permits
- Number of buffers per transmit/receive subaddress is programmable or user definable to account for various host speeds

Sequential Monitoring

- 100% independent
- Host driver selected messages are double buffered
- Messages time stamped with a 1 µs 32-bit clock or optional 48-bit IRIG-B clock
- Standard firmware performs broad error monitoring
- Comprehensive error labeling

Self Test

- Power-up test with status register report
- BIT-RAM and encoder/decoder test
- Run-time health status register
- Unit Test application for 1553 bus functionality

Inputs/Outputs

- Bi-directional external trigger
- IRIG clock input (optional)
- Variable voltage 1553 outputs: 0-22 V p-p
- External TTL/RS-422 system clock input

VME Functionality

- VMEbus system
- D16/D32 single cycle transfers
- D32/D64 block transfers
- A24/A32 addressing
- D08 interrupts
- Memory mapped
- Selectable interrupt requests
- DMA bus master capability

Interface Connections

- $DB26_F$ to $BJ77_F$ coupling harness - Cable assembly: CA-2097 (provided at no cost)
- Coupling harness to bus and I/O connectors
- $DB15_F$ I/O connector

Interface Card Specifications

- Maximum power consumption:
  Single channel
  5 V @ 2.6 A, 12 V @ 250 mA
  Dual channel
  5 V @ 2.8 A, 12 V @ 500 mA
- Standard commercial operating temperature:
  0° C to +55° C
  ≤ 95% rH non-condensing
- Mechanical - single channel or dual channel:
  Standard 6u x 160 mm size

Software and Documentation Support

- Low-level drivers for most operating systems
- Integrated Avionics Library with source code
- Borland and Microsoft® C Compiler compatible
- Hardware and Integrated Avionics Library documentation included on CD. Hard copies of the documentation are available upon request.

Customer Support

- Two-year warranty
- Extended warranties available
- Driver and library upgrades
- Over 18 operating systems supported on various platforms

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