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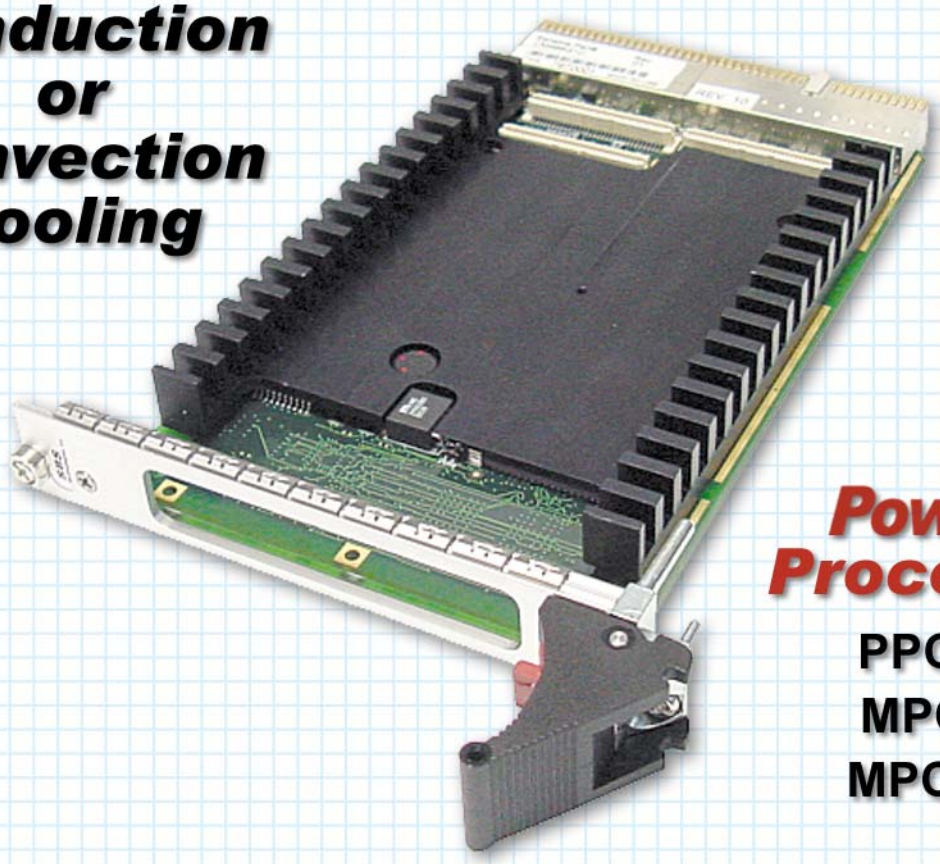
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SBS Technologies

CM4
Single Board Computer

Conduction or Convection Cooling



PowerPC™ Processors

PPC 750
MPC755
MPC7410

User's Guide

Rev F

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CM4 User's Manual - Rev. F

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Document #:70000340-800 Rev. E and 70000345-800 Rev. E

Conventions

The following conventions are used in this user’s guide:

- Signal names are designated with all capital letters (e.g. SYSEN#)
- Signal names followed by the pound sign (#) are active-low (e.g. SYSEN#)
- Data addresses written in hexadecimal are designated with the prefix 0x (e.g. 0xF000_0000)

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Chapter 1: Introduction

1.1 Overview

The CM4 is a 3U CompactPCI Single Board Computer (SBC) designed for network switching, routing, and front-end processing applications. It is available with multiple processor options and offers the flexibility of functioning as a system controller or peripheral card. The CM4 is available in configurations for convection-cooled or conduction-cooled environments.

The CM4 offers two PowerPC Reduced Instruction Set Computer (RISC) processor options:

- MPC755—400MHz
- MPC7410—500MHz

Each processor includes 32KB L1 instruction and 32KB L1data caches. The MPC755 comes with 1MB of backside L2 cache; the MPC7410 processor comes with 2MB of backside L2 cache.

The CM4 implements the Tsi107 Host Bridge (replacing the MPC107 PCI Bridge chip) that includes a 64-bit 100MHz system bus interface, a memory controller with a 64-bit 100MHz memory interface, and a 32-bit 33MHz PCI interface. The memory interface accesses up to four 16M x 16 SDRAM chips for a total on-board system memory of 128MB to 512MB. Error Checking and Correction (ECC) is also included. It also accesses four 64Mb StrataFlash devices for a total on-board flash memory of 64MB. The memory bus also connects with the X-bus to access the 8MB StrataFlash boot flash, 32KB NVSRAM, Real Time Clock, and Decoder CPLD.

The Tsi107 Host Bridge also provides a 32-bit PCI bus interface that connects with the 10/100Mbps 82559ER Ethernet Controller, PCI 6254 PCI Bridge, and a single PMC site.

The 82559ER Ethernet Controller with integrated Medial Access Control (MAC) and physical layer (PHY) provides a 10Base-T and 100Base-TX network communications interface through the cPCI P7202 (P2) connector to the backplane or an optional CM4 Transition Module (TM), which provides either a RJ-45 connector mounted on a rear panel or a surface-mounted connector.

The CM4 includes two ST16C2550 Dual Channel UART Transceivers that provide two RS-232 serial ports and two RS-422/485 serial ports. All four channels operate in full-duplex mode and include 16 bytes of FIFO transmit and 16 bytes of FIFO receive memory.

In addition to serial and Ethernet I/O, the CM4 offers four programmable digital I/O channels that can be used for manufacturing process control lines.

The PCI 6254 PCI Bridge connects the PCI bus (bus 0) to the cPCI backplane (bus1). Because the CM4 can function as a system controller or a peripheral card, the PCI 6254 PCI Bridge (formerly

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HB6) must change how it handles data and PCI signals according to the mode in which the CM4 is operating. When the CM4 is a system controller, the PCI 6254 is in transparent mode, which means the PCI host—the Tsi107 Host Bridge—looks through the PCI 6254 to the backplane, to the PCI devices on other peripheral cards throughout the system. When the CM4 is a peripheral card, the PCI 6254 PCI Bridge is in non-transparent mode, which means that it sees the Tsi107 Host Bridge as PCI device, but cannot look past it to the backplane. This affects how the PCI 6254 handles interrupts and reset signals.

The CM4 incorporates additional flexibility with a PMC site for adding additional I/O capability with over 30 user-defined I/O lines.

The CM4 offers configurations for either convection-cooled or conduction-cooled environment.

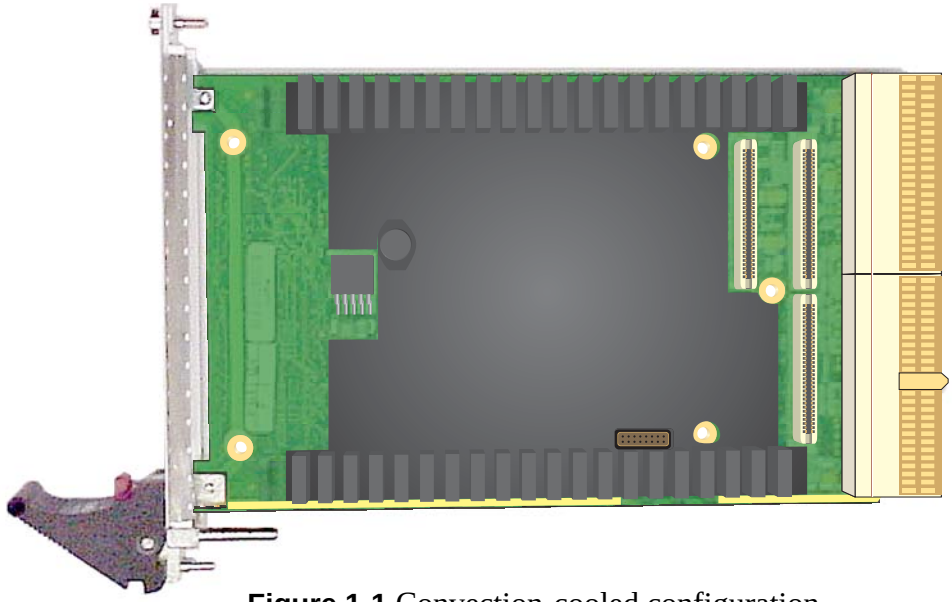


Figure 1-1 Convection-cooled configuration

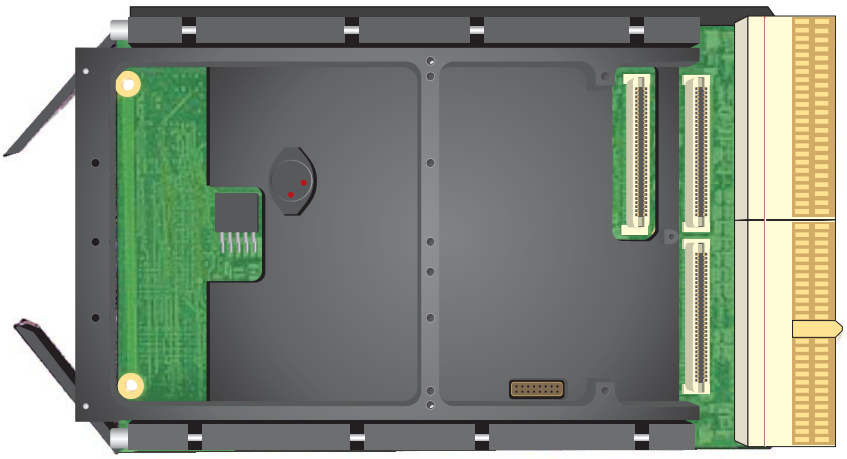


Figure 1-2 Conduction-cooled configuration

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1.2 Specification

Processor

- MPC755 (400MHz)
- MPC7410 (500MHz)
- On-chip L1 cache (32KB instruction, 32KB data, all processors)

L2 Cache

- MPC755—1MB
- MPC7410—2MB

Tsi107 Host Bridge

- 64-bit 100MHz system bus interface
- 32-bit 33MHz PCI bus interface
- Memory controller with 64-bit 100MHz memory interface
- 2 DMA controllers

Memory

- 72-bit (w/ECC)100MHz SDRAM
  128–512MB supported
- 64-bit 64MB flash memory
- 8-bit 8MB boot flash
- 32kB non-volatile SRAM
  automatic data transfer to and from EEPROM

Communications

- Serial ports—asynchronous
  full-duplex 16550-compatible UARTs
  2 RS-232 ports
  2 RS-422/485 ports
- Fast Ethernet—82559ER
  10Base-T
  100Base-TX
  Auto-negotiation
- Digital I/O
  4 register-controlled ports

Power Requirements

- +3.3V
- +5V
- ±12V (for installed PMC only)

Software

- BSP with VxWorks O/S

Environmental Requirements*

- Operating temperature

  Standard: 0° to +70°C
  Extended: -40° to +85°C

- Storage temperature:

  Standard: -40° to +85°C
  Extended: -55° to +105°C

- Humidity: 5–95% @40°C
- Altitude:

  Operating: 15,000 ft. (4.5Km)
  Storage: 40,000 ft. (12Km)

- Shock:

  C-style: 12g/6ms
  R-style: 20g/6ms
  N-style: 100g/6ms

- Vibration:

  C-style: 2g rms/5 to 100Hz
  R-style: 2g rms/5 to 2KHz
  N-style: 14g rms/5 to 2KHz (N-style: 30 minutes each axis)

* All values under typical conditions w/o PMC module installed.

Warranty

- Two year warranty

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1.3 Block Diagram

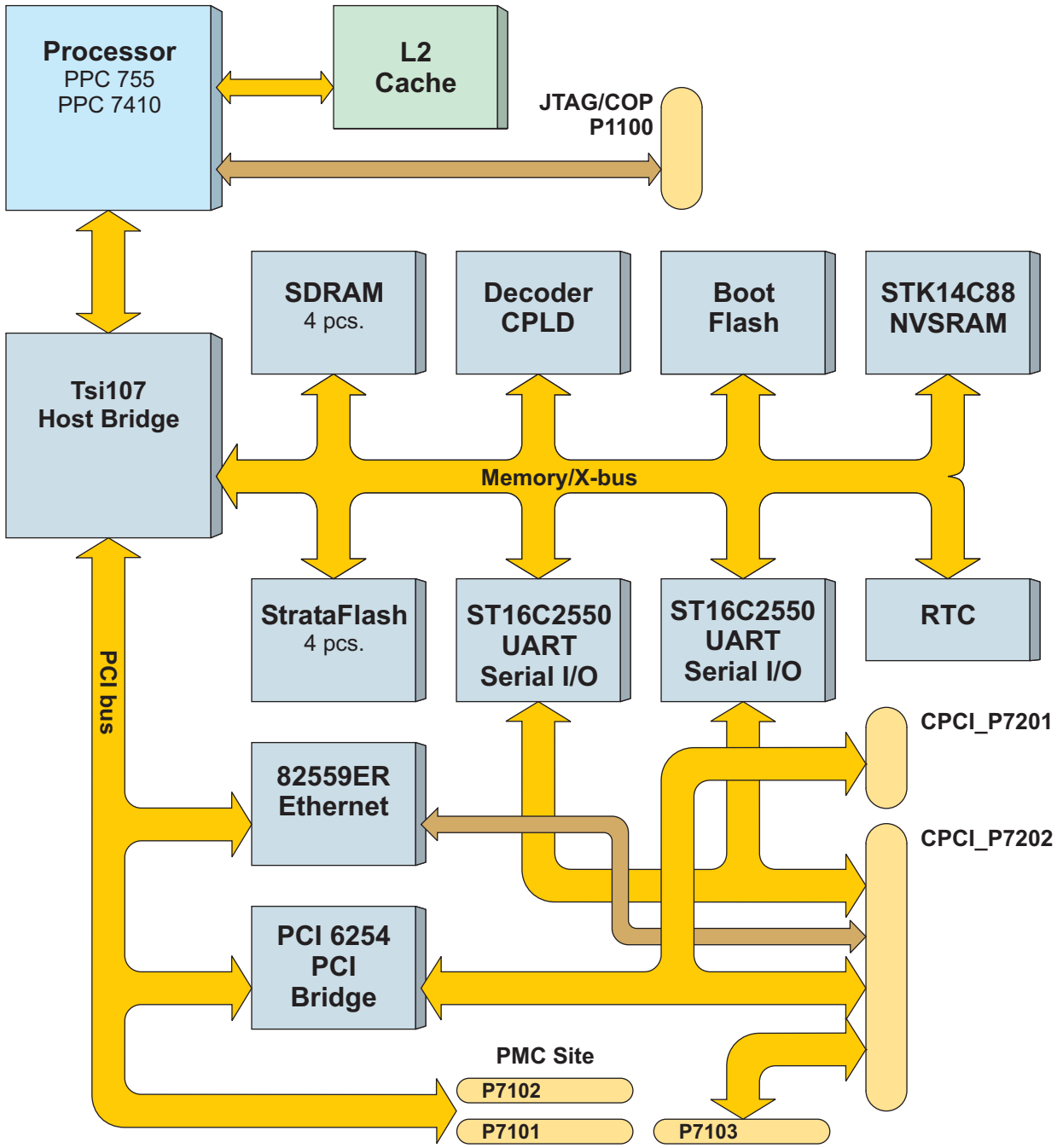


Figure 1-3 CM4 Block diagram

NOTE: The Memory/X-bus represents a network of buses shown in greater detail in “Memory/X-bus” on page 3-8.

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1.4 Technical Support

Most issues can be resolved by referring to this manual. If any problems cannot be resolved, please contact SBS Technical Support by:

- E-mail: support.sbc@sbs.com
- Telephone: (919) 851-1101 (ask for technical support)
- Fax.: (919) 851-2844

For more information, refer to “Customer Service” on page 6-2.

1.5 Related Documents

For more information on CM4 components, refer to the following documents:

Components

- MPC755 RISC Processor Hardware Specification—Motorola, Inc., MPC750EC/D Rev. 6, September 2002
- MPC7410 RISC Microprocessor Hardware Specification—Motorola, Inc., MPC7410EC/D Rev. 0.3, April 2001
- MPC107 PCI Bridge/Memory Controller User’s Manual—Motorola, Inc., MPC107UM/D Rev. 0, November 2000
- Tsi107™ PowerPC™ Host Bridge User’s Manual—Tundra Semiconductor Corporation,80C2000_MA001_03, January 2004
- PCI 6254 (HB6) Dual Mode Universal PCI-to-PCI Bridge DataBook—PLX Technology, Inc., Version 2.0, May 2003
- 3Volt Synchronous Intel StrataFlash® Memory Data Sheet—Intel® Corporation, Order number 290737-004, February 2002
- 82559ER Fast Ethernet PCI Controller Data Sheet—Intel® Corporation, Order number 714682-002, Revision 1.3, March 2001
- XC95144XL High Performance CPLD—Xilinx, Inc., Preliminary Production Specification - Version 1.2, November 1998
- STK14C88 32K x 8 AutoStore™ nvSRAM QuantumTrap™ CMOS Nonvolatile Static RAM—Simtek Corporation, Document Control # ML0014 rev. 0.0, December 2002
- ST16C2550 3.3V and 5V DUART with 16-bit FIFO—EXAR Corporation, Rev. 4.1, March 2002
- DS1685/DS1687 3V/5V Real-Time Clock—Dallas Semiconductor Corporation, DS1685/DX1687

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Specifications

- PowerPC Reference Platform Specification—IBM Corporation, Version 1.1
- PICMG 2.0 CompactPCI Specification—Rev 3.0, October 1999
- PICMG 2.3 PMC on CompactPCI—Rev. 1.0, August 1998
- PCI Local Bus Specification—PCI Special Interest Group, Revision 3.0
- Draft Standard for Common Mezzanine Card Family—CMC, IEEE Standards Department, P1386/Draft 2.0
- Draft Standard Physical and Environmental layers for PCI Mezzanine Cards—PMC, IEEE Standards Department, P1386/Rev 1.0

1. PICMG Specifications are available to PICMG members only. SBS Technologies is not authorized to distribute copies of these specifications. More information can be found at http://www.picmg.org.
2. Data sheets from hardware components can be downloaded from individual vendors web sites.

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Chapter 2: Getting Started

2.1 What is included

The CM4 is shipped with the following items:

- CM4 SBC printed circuit board

2.2 Equipment Needed

The following items are needed to install and operate the CM4:

- Host computer with terminal/console program
- CompactPCI-compatible chassis with system controller card installed
- CM4 Transition Module (optional) (recommended for convection-cooled applications)
- Ethernet cable
- 1:1 Serial cable



Caution! Always use proper Electrostatic Discharge (ESD) protection when handling printed circuit boards to avoid seriously damaging components. Product handlers must always be properly grounded.

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2.3 Power

The CM4 is designed for +3.3V operation but will tolerate +5V. The MIC2903 DC/DC Converter taps the +3.3V rail to provide a +2.5V line. The LTC1727 Power Monitor monitors the +3.3V and +2.5V line.

Caution! Processor manufacturers recommend the following power restrictions for long term product reliability.To comply with these power restrictions, it is recommended the CompactPCI chassis use a dual power supply that complies with the ATX Power Supply Design Guide, Version 1.2.

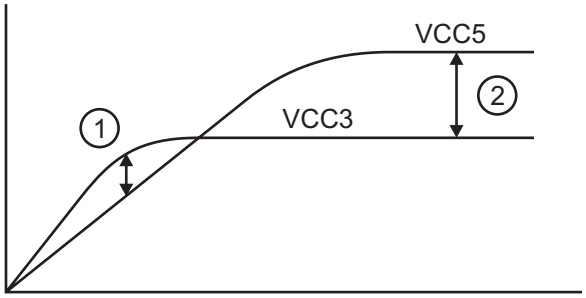


Figure 2-1 Power regulation recommendations

NOTES:

1. VCC3 (+3.3V) must not exceed VCC (+5V) by more than +0.6V for more than 20ms at any time including power-up and power-down.
2. VCC5 (+5V) must not exceed VCC3 (+3.3V) by more than +3.6V for more than 20ms at any time including power-up and power-down.

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2.4 Installation

This installation procedure is a sample bootup scheme that assumes the CM4 will boot from a CM4 BSP VxWorks image located on a network or host computer.

1. Copy the BSP from the CD ROM to a permanent storage location either on a network or the host computer.

   At a minimum the VxWorks image must be available in an FTP server location for the CM4 during bootup.
2. Remove the CM4 from the static-safe envelope.
3. Install the CM4 in a 3U 32-bit CompactPCI-compliant chassis.



Caution! The CM4 is not compatible with a 64-bit backplane.

Convection-cooled Configuration

4. Slide the CM4 into the slot guide, applying even pressure to the front panel and lower ejector handle. Be careful not to bend connector pins.
5. Push up on the lower extraction handle to seat the CompactPCI connectors in the backplane connectors. The red tab on the extraction handle should “click” when the board is locked into the chassis.
6. Tighten the large screw on the front panel, then tighten the smaller screw embedded in the extraction handle to secure the CM4 to the chassis.

Conduction-cooled Configuration

7. Slide the CM4 into the slot guide, applying even pressure to the upper and lower extraction levers. Be careful not to bend connector pins.
8. Use a 3/32-inch hex torque driver to tighten the top and bottom hex screws to 117-inch ounces (0.8-newton meters).

All Configurations

9. When the CM4 has been installed in the chassis, install a serial cable from the host computer to the CM4 through either the optional CM4 Transition Module or other serial port connected to the backplane.
10. Install a Ethernet cable from the host computer or network connection to the CM4 through either the optional CM4 Transition Module or other Ethernet port connected to the backplane.
11. Apply power to the chassis.

NOTE: CM4 can be installed in a system controller or peripheral slot. If the CM4 is not installed in a system slot, a system controller card must be installed in the system slot to supply a PCI reference clock to CM4.

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Figure 2-2 Conduction-cooled configuration



Figure 2-3 Convection-cooled configuration

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Chapter 3: Board Description

3.1 Physical Description

Height:	100mm (3.9 inches)
Length:	160mm (6.3 inches)
Operating temperature:	-40° to 85° C (ambient)*
Storage temperature:	-40° to 85° C (N-style: -55° C to 105° C)
Humidity:	10% to 95% (non-condensing)
Cooling:	Forced air 200 LFM (min.)
Power (+3.3VDC ±5%):	normal—1.3A (4.29W)
Power (+5VDC ±5%):	normal—1.9A (9.5W)

* Highest achievable operating temperature depends on processor type, speed, and ambient conditions (card edge temperature). Also, all temperature values are typical conditions without PMC module installed.

3.2 Power

The CM4 inputs two voltage rails: +5V and +3.3V (*see "Caution" on page 2-2*). A linear regulator taps the +3.3V line and outputs a +2.5V line. VI/O is taken from either the +3.3V for the MPC755 processors or +2.5V for the MPC7410 processor. The LTC1727 power monitor tracks these voltages (+3.3V and +2.5V) within a specified range. If the +3.3V supply drifts above or below its specified range, the power monitor will assert an interrupt (INT3V) to the Decoder CPLD. If it is out of range for longer than 50µs, the power monitor asserts the reset output (BOARD_RST#), which resets the CM4. If the +2.5V supply drifts outside its specified range, the power monitor will assert the VCC2.5OK signal that disables the LM2636 Buck Controller, which provides the processor core voltages. If the +2.5V supply is out of specification for longer than 50µs, the power monitor will assert the reset output (BOARD_RST#), which resets the CM4. BOARD_RST# will remain asserted for 200ms even if the +3.3V or +2.5V supply returns to the specified range.

Table 3-1 Processor voltages

Processor	Core Voltage
MPC755	+2.0V
MPC7410	+1.8V

Configuration resistors on the input of the LM2636 Buck Controller set processor core voltages (VCCP) according to the installed processor as listed in Table 3-1.

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3.3 Connector Locations

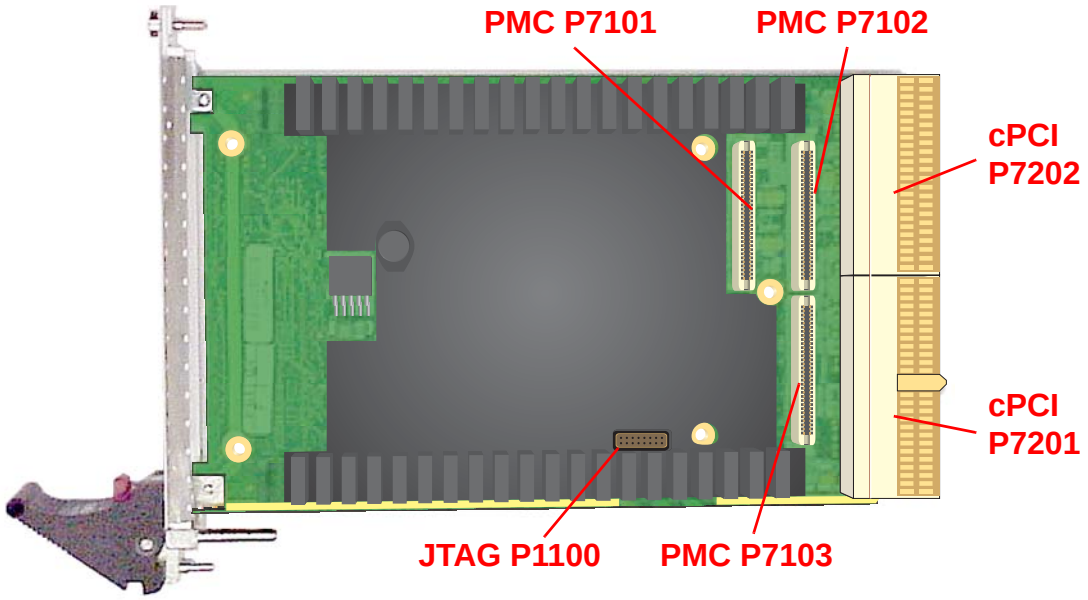


Figure 3-1 Connector locations (convection-cooling version)

3.4 Front Panel

The CM4 front panel (convection-cooled configuration only) provides access to a PMC module front panel. It also includes a locking extraction handle at the bottom of the front panel and two screws: a large screw at the top and a smaller screw embedded in the extraction handle, to secure the CM4 to the chassis.

The conduction-cooled configuration of the CM4 has two extraction levers with no front panel (*see Figure 2-2 on page 2.4*).



Figure 3-2 Front panel (convection-cooled configuration)

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3.5 Connectors

3.5.1 CompactPCI Connectors



Caution! The CM4 is not compatible with a 64-bit backplane.

Table 3-2 CompactPCI connector P7201 pin assignments

Pin	A	B	C	D	E	F
J1-25	+5V	N/C	S_ENUM#	+3.3V	+5V	DGND
J1-24	S_AD01	+5V	VI/O	S_AD00	ACK64#	DGND
J1-23	+3.3V	S_AD04	S_AD03	+5V	AD02	DGND
J1-22	S_AD07	GND	+3.3V	S_AD06	AD05	DGND
J1-21	+3.3V	S_AD09	S_AD08	S_M66EN	C/BE[0]#	DGND
J1-20	S_AD12	GND	VI/O	S_AD11	AD10	DGND
J1-19	+3.3V	S_AD15	S_AD14	GND	AD13	DGND
J1-18	S_SERR#	GND	+3.3V	S_PAR	C/BE[1]#	DGND
J1-17	+3.3V	N/C	N/C	GND	PERR#	DGND
J1-16	S_DEVSEL#	GND	S_VI/O	S_STOP#	LOCK#	DGND
J1-15	+3.3V	S_FRAME#	S_IRDY#	GND	TRDY#	DGND
J1-12 to 14						
J1-11	S_AD18	S_AD17	S_AD16	GND	S_C/BE[2]#	DGND
J1-10	S_AD21	GND	+3.3V	S_AD20	S_AD19	DGND
J1-9	S_C/BE[3]#	S_IDSEL	S_AD23	GND	S_AD22	DGND
J1-8	S_AD26	GND	S_VI/O	S_AD25	S_AD24	DGND
J1-7	S_AD30	S_AD29	S_AD28	GND	S_AD27	DGND
J1-6	S_REQ0#	GND	+3.3V	S_CLK0	S_AD31	DGND
J1-5	N/C	N/C	S__RST#	GND	S_GNT0#	DGND
J1-4	N/C	GND	S_VI/O	N/C	N/C	DGND
J1-3	S_INTA#	S_INTB#	S_INTC#	+5V	S_INTD#	DGND
J1-2	N/C	+5V	N/C	N/C	N/C	DGND
J1-1	+5V	-12V	N/C	+12	+5V	DGND

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Table 3-3 CompactPCI connector P7202 pin assignments

Pin	A	B	C	D	E	F
J2-22	GA4	GA3	GA2	GA1	GA0	DGND
J2-21	SCLK6	GND	PMCI/O_24	ETX+	ERX+	DGND
J2-20	SCLK5	GND	PMCI/O_23	ETC	ERC	DGND
J2-19	GND	GND	PMCI/O_27	ETX-	ERX-	DGND
J2-18	PMCI/O_25	PMCI/O_26	PMCI/O_22	PMCI/O_28	BATT+	DGND
J2-17	PMCI/O_12	PMCI/O_10	RST_BUT#	S_REQ6#	S_GNT6#	DGND
J2-16	PMCI/O_38	PMCI/O_36	DEG#*	GND	PMCI/O_33	DGND
J2-15	PMCI/O_52	PMCI/O_50	FAL3*	S_REQ5#	S_GNT5#	DGND
J2-14	PMCI/O_18	PMCI/O_16	PMCI/O_19	PMCI/O_21	PMCI/O_20	DGND
J2-13	S2_TXD	DI/O_00	PMCI/O_17	S4_CTS-	S4_CTS+	DGND
J2-12	S2_RXD	PMCI/O_13	PMCI/O_14	PMCI/O_15	S4_RTS-	DGND
J2-11	PMCI/O_11	DI/O_02	PMCI/O_30	S4_TXD+	S4_RTS+	DGND
J2-10	PMCI/O_08	PMCI/O_09	BIT_OK	PMCI/O_29	S4_TXD-	DGND
J2-9	PMCI/O_06	DI/O_03	PMCI/O_07	S4_RXD-	S4_RXD+	DGND
J2-8	PMCI/O_03	PMCI/O_04	S3_RXD+	PMCI/O_05	S3_CTS+	DGND
J2-7	DI/O_06	DI/O_04	PMCI/O_02	S3-RTS+	S3_CTS-	DGND
J2-6	S1_TXD	S1_RXD	S3_RXD-	PMCI/O_01	S3_RTS-	DGND
J2-5	DI/O_07	DI/O_01	WDG_REL	S3_TXD-	S3_TXD+	DGND
J2-4	S_VI/O	DI/O_05	A_DI/O	BOOTSEL	B_DI/O	DGND
J2-3	SCLK4	GND	S_GNT3#	S_REQ4#	S_GNT4#	DGND
J2-2	SCLK2	SCLK3	S_SYSEN#	S_GNT2#	S_REQ3#	DGND
J2-1	SCLK1	GND	S_REQ1#	S_GNT1#	S_REQ2#	DGND

* Unused—pulled up to Vcc.

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3.5.2 PMC Connectors

Table 3-4 PMC connectors P7101 and P7102 pin assignments.

PMC P7101				PMC P7102			
Pin	Assignment	Pin	Assignment	Pin	Assignment	Pin	Assignment
1	N/C	2	-12V	1	+12V	2	N/C
3	GND	4	INTD#	3	N/C	4	N/C
5	INTA#	6	INTB#	5	N/C	6	GND
7	N/C	8	+5V	7	GND	8	N/C
9	INTC#	10	N/C	9	N/C	10	N/C
11	GND	12	N/C	11	+5V	12	+3.3V
13	PCLK_PMC	14	GND	13	PCI_RST#	14	GND
15	GND	16	PGNT2#	15	+3.3V	16	GND
17	PREQ2#	18	+5V	17	N/C	18	GND
19	LVDD	20	AD31	19	AD30	20	AD29
21	AD28	22	AD27	21	GND	22	AD26
23	AD25	24	GND	23	AD24	24	+3.3V
25	GND	26	C/BE[3]#	25	AD14	26	AD23
27	AD22	28	AD21	27	+3.3V	28	AD20
29	AD19	30	+5V	29	AD18	30	GND
31	LVDD	32	AD17	31	AD16	32	C/BE[2]#
33	FRAME#	34	GND	33	GND	34	RSVD
35	GND	36	IRDY#	35	TRDY#	36	+3.3V
37	DEVSEL#	38	+5V	37	GND	38	STOP#
39	GND	40	LOCK#	39	PERR#	40	GND
41	SDONE# *	42	SBO# *	41	+3.3V	42	SERR#
43	PAR	44	GND	43	C/BE[1]#	44	GND
45	LVDD	46	AD15	45	AD14	46	AD13
47	AD12	48	AD11	47	GND	48	AD10
49	AD09	50	+5V	49	AD08	50	+3.3V
51	GND	52	C/BE[0]#	51	AD07	52	RSVD
53	AD06	54	AD05	53	+3.3V	54	RSVD
55	AD04	56	GND	55	RSVD	56	GND
57	LVDD	58	AD03	57	RSVD	58	RSVD
59	AD02	60	AD01	59	GND	60	RSVD
61	AD00	62	+5V	61	ACK64# *	62	+3.3V
63	GND	64	REQ64# *	63	GND	64	RSVD

* Not used—pulled up to Vcc.

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Table 3-5 PMC-P7103 pin assignments

PMC P7103

Pin	Assignment	Pin	Assignment
1	PMCI/O_01	2	PMCI/O_02
3	PMCI/O_03	4	PMCI/O_04
5	PMCI/O_05	6	PMCI/O_06
7	PMCI/O_07	8	PMCI/O_08
9	PMCI/O_09	10	PMCI/O_10
11	PMCI/O_11	12	PMCI/O_12
13	PMCI/O_13	14	PMCI/O_14
15	PMCI/O_15	16	PMCI/O_16
17	PMCI/O_17	18	PMCI/O_18
19	PMCI/O_19	20	PMCI/O_20
21	PMCI/O_21	22	PMCI/O_22
23	PMCI/O_23	24	PMCI/O_24
25	PMCI/O_25	26	PMCI/O_26
27	PMCI/O_27	28	PMCI/O_28
29	PMCI/O_29	30	PMCI/O_30
31	N/C	32	N/C
33	PMCI/O_01	34	N/C
35	N/C	36	PMCI/O_36
37	N/C	38	PMCI/O_38
39	N/C	40	N/C
41	N/C	42	N/C
43	N/C	44	N/C
45	N/C	46	N/C
47	N/C	48	N/C
49	N/C	50	PMCI/O_50
51	N/C	52	PMCI/O_52
53	N/C	54	N/C
55	N/C	56	N/C
57	N/C	58	N/C
59	N/C	60	N/C
61	N/C	62	N/C
63	N/C	64	N/C

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3.5.3 JTAG/COP Port (P1100)

CM4 provides a JTAG/COP port (P1100) attached to the processor for single-stepping through code on the processor. The JTAG/COP port is fully functional with EST VisionProbe II emulators.

Table 3-6 JTAG/COP port pin assignments

Pin	Assignment	Pin	Assignment
1	COP_TDO	2	COP_QACK#
3	COP_TDI	4	COP_RST#
5	QREQ#	6	BVDD
7	COP_TCK	8	N/C
9	COP_TMS	10	N/C
11	COP_SRST#	12	N/C
13	COP_HRST#	14	N/C
15	CKSTP_OUT#	16	GND

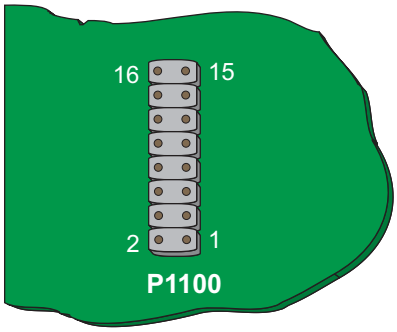


Figure 3-3 JTAG/COP port (P1100)

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3.6 Memory/X-bus

The Memory/X-bus shown in the block diagram (*see Figure 1-3 on page 1-4*) represents a network of memory data, address, and parity buses and an X-bus as shown in Figure 3-4 on page 3-9.

Memory Data Buses

The MCP107 Host Bridge provides a memory controller with a 64-bit memory (data) bus interface. The memory data interface is divided into two 32-bit sections: high data and low data. The 32-bit high data bus transports data to and from two 16-bit SDRAM chips and two 16-bit extended flash memory chips. The 32-bit low data bus transports data to and from the remaining two 16-bit SDRAM chips and 16-bit extended flash memory chips.

The high data bus also provides an 8-bit data bus that connects to the X-bus through a 16-bit bus transceiver.

Address Bus

The 14-bit address bus provides addressing for the SDRAM and ECC devices. It also sends addressing information to a 16-bit bus transceiver, which sends the addressing information to the RA bus.

Parity Bus

The 8-bit parity bus transports parity bits between the Tsi107 Host Bridge and the SDRAM Error Checking and Correction (ECC) device. It also connects to the RA bus.

RA Bus

The 24-bit RA bus carries address and parity information from two 16-bit bus transceivers to the four extended flash devices, Decoder CPLD, NVSRAM, Boot flash, and two UART Transceivers.

X-Bus

The 8-bit X-bus connects the Decoder CPLD, NVSRAM, Boot flash, RTC, or two UART Transceivers to Tsi107PCI Bridge through a 16-bit bus switch. The 16-bit bus switch changes the direction of data flow between read and write cycles.

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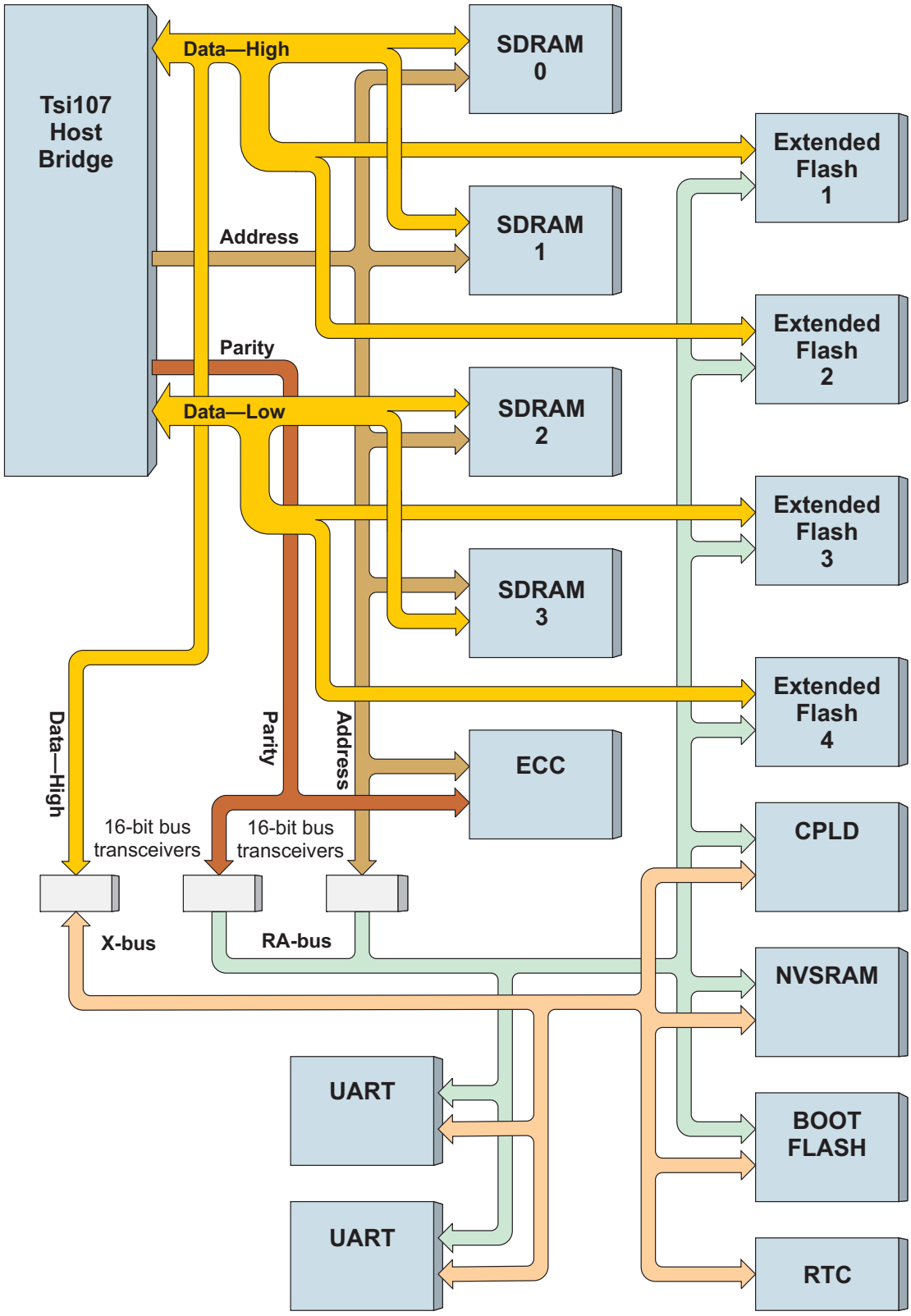


Figure 3-4 Memory/X-bus network

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3.7 Memory Map

The Tsi107 Host Bridge supports two memory maps: Memory Map A and Memory Map B. Memory Map A conforms to the now-obsolete PowerPC Reference Platform (PReP) specification. Memory Map B conforms to the PowerPC microprocessor Common Hardware Reference Platform (CHRP) specification. At power-up or reset, CM4 selects Memory Map B as default.

The memory map can be viewed from two perspectives:

- Processor view
- PCI bus master view

Table 3-7 lists the memory map as seen from the processor point of view; Table 3-8 lists the memory map as seen from the PCI bus master point of view.

Table 3-7 Tsi107 memory map—processor view

Processor Range	PCI Address Range	Description
0x0000_000 to 0x3FFF_FFFF	No PCI cycle	Local memory space[1, 2]
0x4000_0000 to 0x77FF_FFFF	Reserved	Reserved
0x7800_0000 to 0x7FFF_FFFF	No PCI cycle	Extended ROM space[3]
0x8000_0000 to 0xFCFF_FFFF	0x8000_0000 to 0xFCFF_FFFF	PCI memory space
0xFD00_0000 to 0xFDFF_FFFF	0x0000_0000 to 0x00FF_FFFF	PCI memory space (16MB ISA)
0xFE00_0000 to 0xFEBF_FFFF	0x0000_0000 to 0x000B_FFFF	PCI I/O space
0xFEC0_0000 to 0xFEDF_FFEF		Configuration Address register[4]
0xFEE0_0000 to 0xFEEF_FFFF		Configuration Data register
0xFEF0_0000 to 0xFEFF_FFFF	0xFEF0_0000 to 0xFEFF_FFFF	PCI Interrupt Acknowledge
0xFF00_0000 to 0xFF7F_FFFF	No PCI cycle	Board I/O devices[5]
0xFF80_0000 to 0xFFFF_FFFF	No PCI cycle	Base ROM space[6]

NOTES:

1. A PC compatibility gap exists from address 0x0000_A000 to 0x0000_FFFF. A configuration register can set this memory space to either to PCI memory or system memory.
2. Maximum memory space is 512MB (0x1FFF_FFFF).
3. Maximum extended flash memory is 64MB from addresses 0x7C00_0000 to 7FFF_FFF.
4. Maximum extended flash is located from address 0x7C00_0000 to 0x77FFF_FFFF.
5. Location of board-specific I/O devices.
6. 8MB of ROM located from 0xFF80_0000 to 0xFFFF_FFFF.

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Table 3-8 Tsi107 memory map—PCI bus master view

Transactions Address Range	Processor Address Range	Definition
I/O Transactions		
0x0000_0000 to 0x0000_FFFF	No local memory cycle	PCI—I/O space
0x0001_0000 to 0x007F_FFFF	No local memory cycle	Reserved
0x0080_0000 to 0x00BF_FFFF	No local memory cycle	PCI—I/O space
0x00C0_0000 to 0xFFFF_FFFF	No local memory cycle	Reserved
Memory Transactions		
0x0000_0000 to 0x3FFF_FFFF	0x0000_0000 to 0x7FFF_FFFF	System memory
0x4000_0000 to 0x77FF_FFFF	No local memory cycle	Reserved
0x7800_0000 to 0x7FFF_FFFF	0x7800_0000 to 0x7FFF_FFFF	Extended flash/ROM space
0x8000_0000 to 0xFDFF_FFFF		PCI memory space
0xFE00_0000 to 0xFEFF_FFFF		Reserved
0xFF00_0000 to 0xFF7F_FFFF	0xFF00_0000 to 0xFF7F_FFFF	Board I/O device space
0xFF80_0000 to 0xFFFF_FFFF	0xFF80_0000 to 0xFFFF_FFFF	Flash/ROM space

3.7.1 I/O Devices

The Tsi107 Host Bridge provides memory mapping for the devices listed in Table 3-9 through the X-bus.

Table 3-9 X-bus I/O address map

X-bus I/O Address Range	Function
0xFF00_0000 to 0xFF00_7FFF	32kB STK14C88 NVSRAM
0xFF00_8000 to 0xFF00_8002	Watchdog and MCP counter registers
0xFF00_8010 to 0xFF00_8013	Interrupt control registers
0xFF00_8020 to 0xFF00_802F	ST16C2550 UART Serial controller—ports 1 and 2
0xFF00_8030 to 0xFF00_803F	ST16C2550 UART Serial controller—ports 3 and 4
0xFF00_8040 to 0xFF00_8041	DS1285 Real-Time Clock
0xFF00_8050 to 0xFF00_8052	Status Input and Status Output port
0xFF00_8060 to 0xFF00_8063	Digital I/O register

3.8 PCI Arbitration

The Tsi107 provides bus arbitration for PCI devices on the PCI bus listed in Table 3-10.

Table 3-10 PCI bus arbitration

PCI Bus Request	PCI Master
CPU (internal)	Tsi107 Host Bridge
REQ/GND 0	PCI 6254 PCI bridge
REQ/GND 1	82559ER Ethernet controller
REQ/GND 2	PMC site

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3.9 PCI IDSEL

Each PCI device requires a unique PCI address connected to the IDSEL line. Table 3-11 lists the IDSEL for each PCI device and address for the associated configuration registers.

Table 3-11 PCI IDSEL configuration registers

IDSEL	PCI Config. Register	Device
AD12	0x8000_60nn	PCI 6254 PCI bridge
AD13	0x8000_68nn	82599ER Ethernet controller
AD14	0x8000_70nn	PMC slot
* "nn" represents the address of the configuration register		

3.10 Serial I/O Communications

The CM4 includes four asynchronous serial ports: two RS-232 and two RS-422/485, implemented in two dual ST16C2550 UARTS. The UARTs are fully NS16450 and NS16550-compatible. Each UART includes a separate interrupt and a programmable baud generator capable of 50–1.5M baud.

Each UART communicates with the Tsi107 Host Bridge through the X-bus. Each UART channel is memory-mapped to locations listed in Table 3-12. Figure 3-5 on page 3-13 shows the serial communications circuitry.

Table 3-12 Serial port addresses

Serial Port	Address
COM1	0xFF00_8020 to 0xFF00_8027
COM2	0xFF00_8028 to 0xFF00_802F
COM3	0xFF00_8030 to 0xFF00_8037
COM4	0xFF00_8038 to 0xFF00_803F

NOTE: The COM3 and COM4 TXD+/- and RTS+/- drivers are disabled after bootup. These drivers can be enabled through the Data Terminal Ready (DTR) output of the COM3 and COM4 controllers.

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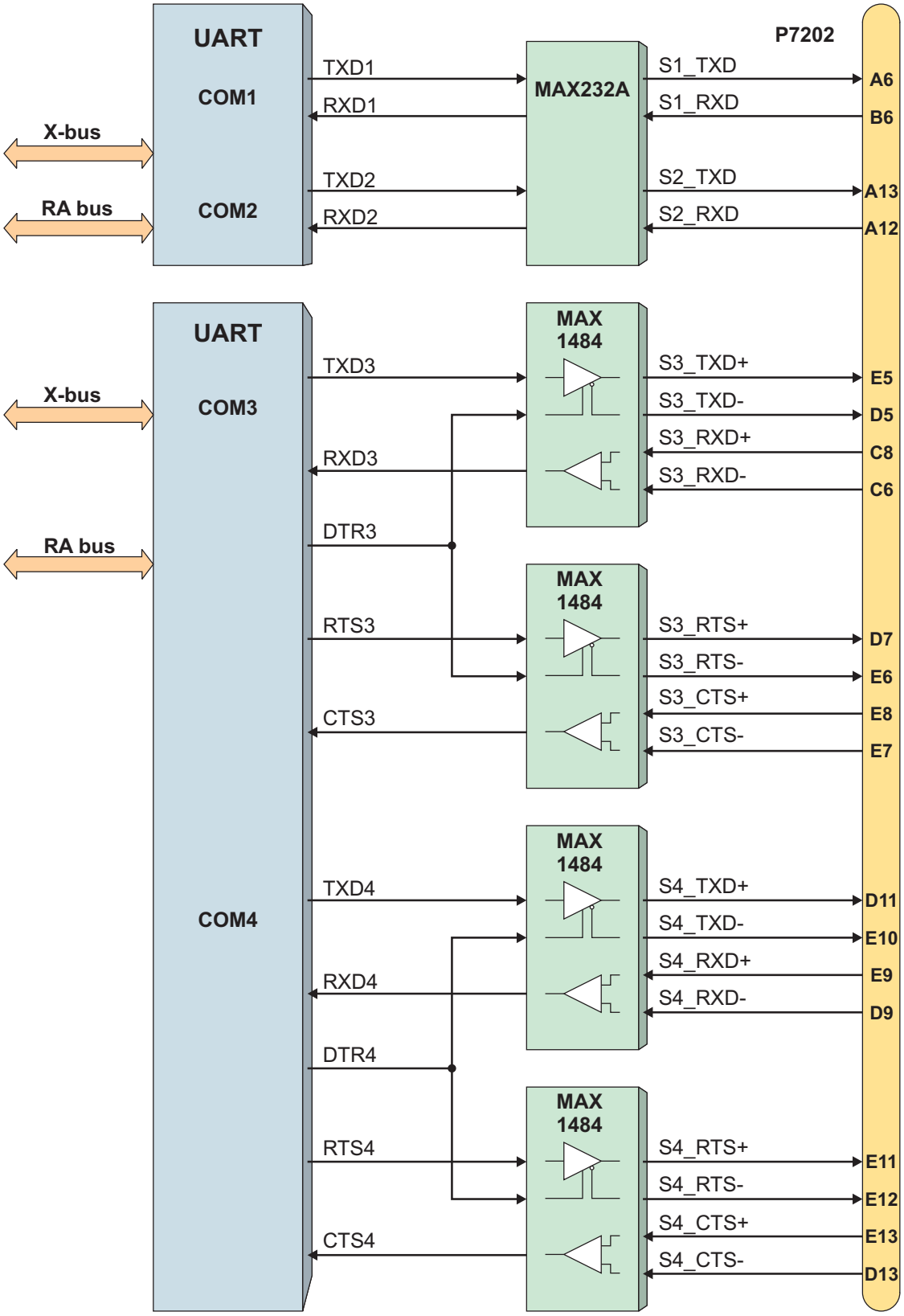


Figure 3-5 Serial port circuitry

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3.11 Digital I/O Communications

The CM4 provides five digital control I/O ports for users to control external process functions. A set of CPLD registers enables the software applications to separately control the direction and usage of each port. Figure 3-6 on page 3-15 shows the circuitry for digital I/O port 0. Each register uses five bits (6, 3:0), one for each port (*see "Digital I/O Registers" on page 5-7*).

The CPLD's DOUTEN register provides five bits to control whether each port is an input or an output. The reset value for this register sets all ports to be inputs. Input ports are readable and have edge-detection circuitry that drives a maskable interrupt function. A port set to be an output is still readable, but its edge-detection circuitry is disabled. The level on output ports is directly controlled by application software.

Input ports have edge-detection circuits which require a minimum input pulse width of 100ns. Pulses less than 100ns may not be detected. Once an edge in either direction is detected, a bit is set in the DI/O Interrupt Status Register. If the corresponding bit in the DI/O Interrupt Mask Register is set, the status register bit causes the assertion of an interrupt. Software can disable the interrupt source by masking it, or by writing a (1) to the bit in the DI/O Interrupt Status Register to clear it. The DINQ register is provided to allow software to read the state of the DI/O ports. Software must read the current state of a DI/O input to determine the direction of an edge that was detected. Therefore, software must consider the fact that a short pulse on an input port could cause the wrong conclusion to be drawn.

Output ports are directly controlled by the values of the five software-controlled bits in the DOUT register. The corresponding bit in the DOUTEN register must be set by software to make a port an output port since they default at reset to input ports. Both of these registers are write-only registers due to resource constraints in the CPLD.

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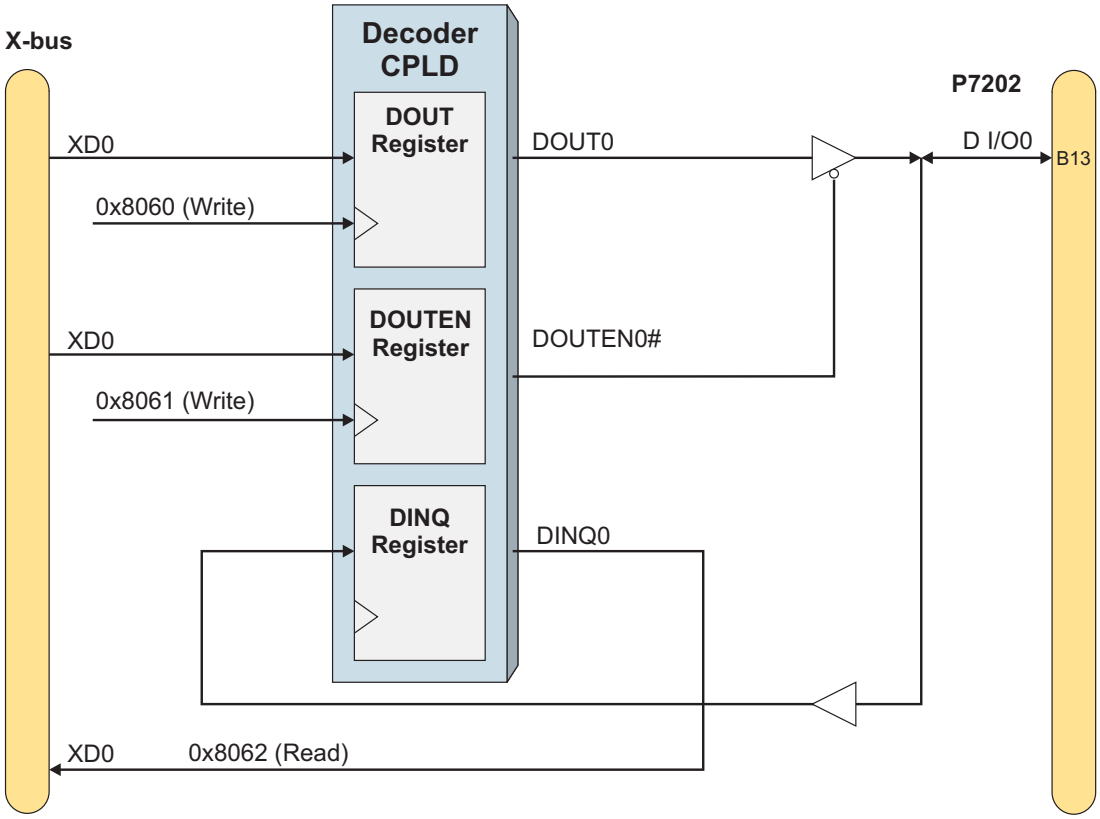


Figure 3-6 Digital I/O circuit (digital port 0)

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3.12 Ethernet I/O Communications

The CM4 includes a 82559ER Fast Ethernet Controller that provides either 10Base-T or 100Base-TX Ethernet through the CompactPCI backplane. The 82559ER Controller includes both a Media Access Controller (MAC), and a physical layer (PHY) that interfaces with the Ethernet transformer. The 82559ER can operate in either full-duplex or half-duplex mode.

The 82559ER Controller is a PCI peripheral that includes a PCI interface. It also includes a 4-bit EEPROM interface. The serial EEPROM contains power-on initialization as well as configuration information.

The 82559ER chip auto-negotiates for the fastest possible connection.

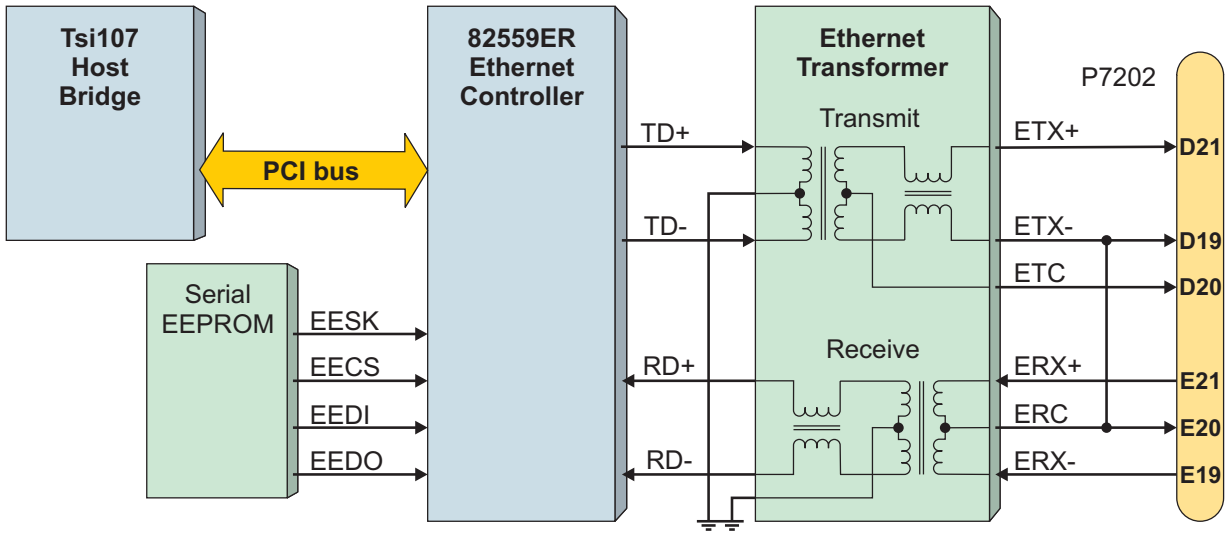


Figure 3-7 Ethernet circuitry

3.13 System Controller vs. Peripheral Operation

It is important to be aware, as it relates to the following sections, that the PCI 6254 handles reset and interrupt signals differently when the CM4 is installed in a system slot, than when the CM4 is installed in a peripheral slot as shown in Figure 3-8 on page 3-17.

When the CM4 is functioning as a system controller, the PCI 6254 PCI bridge is in *transparent mode*, meaning it is effectively transparent to PCI reset signals sent from the Tsi107 Host Bridge out to the PCI backplane and interrupts received from the backplane to the Tsi107.

When the CM4 is functioning as a peripheral, the PCI 6254 PCI Bridge is in *non-transparent mode*, which means that it appears to the Tsi107 as a PCI device on the PCI bus. The function of the MCP107 Host Bridge as PCI host does not change whether the CM4 is functioning as a system controller or peripheral.

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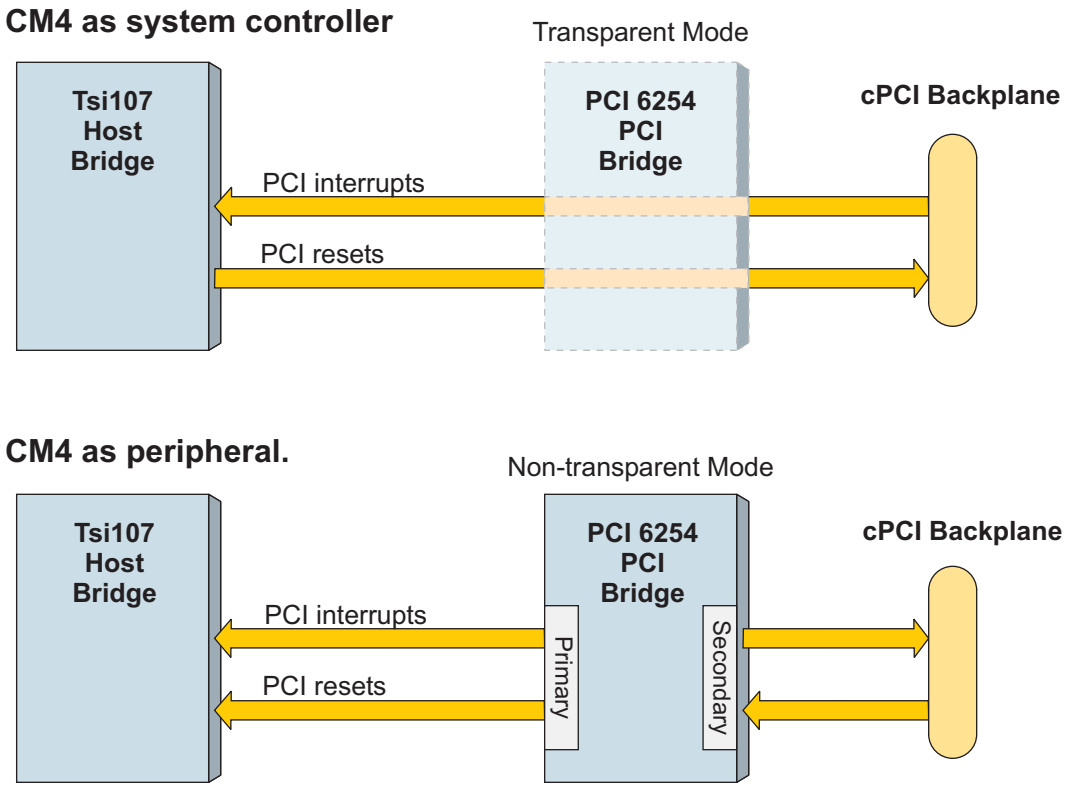


Figure 3-8 PCI 6254 PCI Bridge in transparent and non-transparent mode

3.14 Reset Circuitry

The CM4 reset circuitry consists of hard and soft resets. Hard resets are asserted during power-up or by a voltage drifting out of a specified range, a manual reset, or a PCI reset from the Compact-PCI backplane (discussed separately from hard resets). Soft resets are triggered by application or test and evaluation software.

3.14.1 Hard Resets

The Decoder CPLD receives hard resets from the following sources:

- Power monitor reset (BOARD_RST#)
- Manual reset button (RST_BUT#)
- External emulator reset—P1100 (COP_HRST# and COP_TRST#)

Power Monitor Reset

After power-up or manual reset, when the processor core voltages (VCCP) has been established to the processor, the LM2636 Buck Controller de-asserts the PWRGOOD# signal to the LTC1727 Power Monitor. The LM2636 asserts the PWRGOOD# signal when the processor core voltage (*see Table 3-1 on page 3-1*) goes outside a 10% window and de-asserts it when the core voltage travels back into an 8% window for at least 10ms.

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The LTC1727 Power Monitor tracks the +3.3V and +2.5V lines as well as the PWRGOOD# signal. If the +3.3V or +2.5V drift out of a 1.5% window for more than 50µs or if PWRGOOD# is asserted, the LTC1727 asserts the BOARD_RST# output to the Decoder CPLD and extended flash devices as shown in Figure 3-9. The watchdog timer output (WD_RESET) from the Decoder CPLD can also assert the PWRGOOD# line.

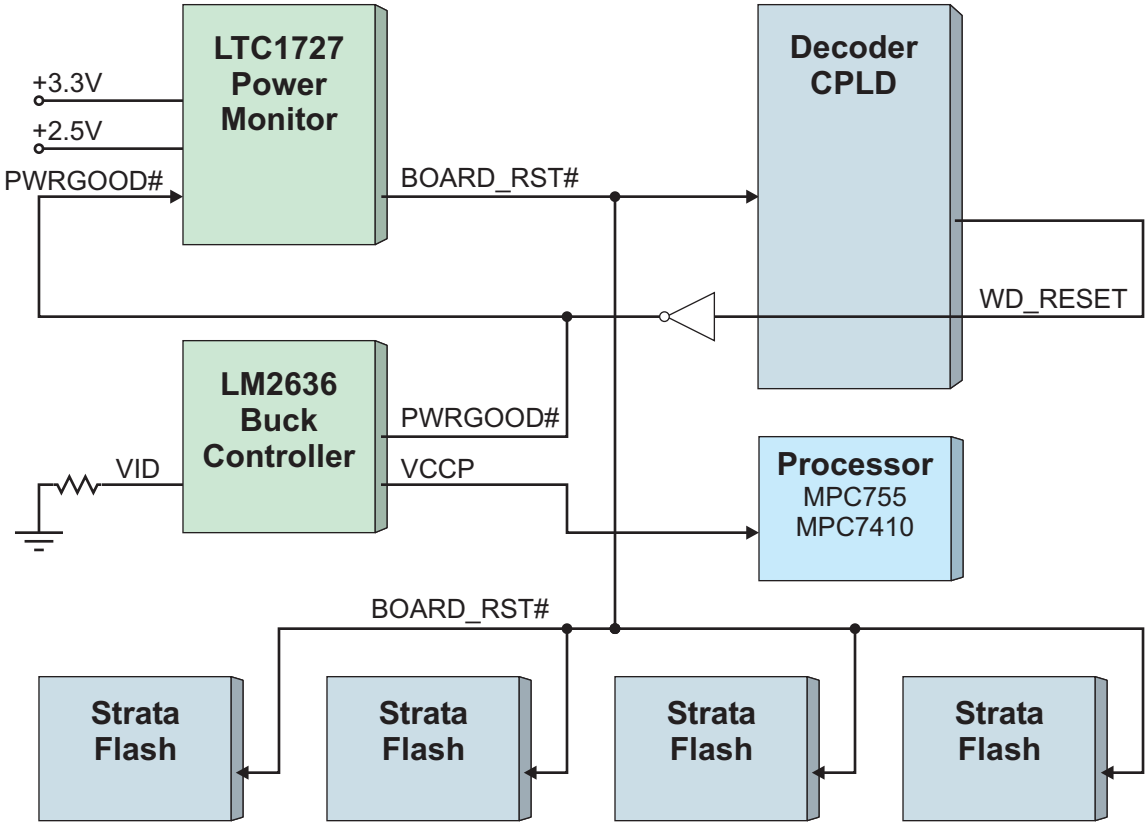


Figure 3-9 Power-up reset circuitry

Manual Reset Button

The CM4 does not include a physical reset button, however, it provides for an external manual reset through the RST_BUT# signal available at CompactPCI connector P7202 (*see Figure 3-10 on page 3-19*). When the RST_BUT# signal is asserted, the Decoder CPLD inputs the RST_BUT# to a logical OR gate with the BOARD_RST# and COP_HRESET# signal to assert the 107_HRESET# line to the Tsi107PCI Bridge. The Tsi107 then asserts the 107_CPUHRST# signal that passes through the Decoder CPLD to reset the processor.

Inside the Decoder CPLD, the 107_CPUHRST# signal is also connected through a logical OR gate with the BOARD_RST# to assert the PCI_RST#. The PCI_RST# signal resets all PCI devices on the CM4 (*see "PCI Resets" on page 3-20*).

SBS Technologies offers a CM4 Transition Module that includes a reset switch on a rear panel or a RST_BUT# pin in the 26-pin Miscellaneous connector.

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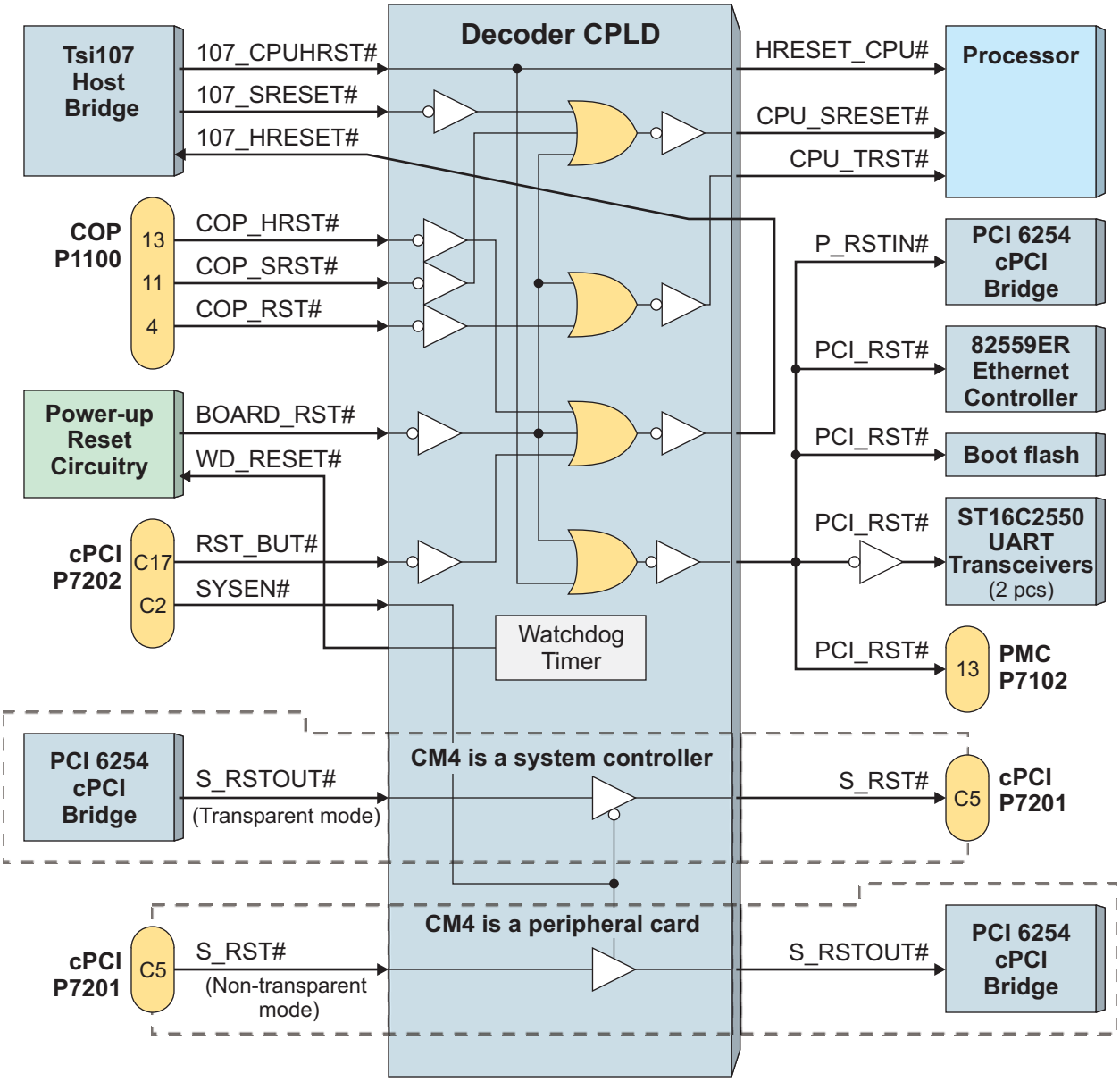


Figure 3-10 Reset circuitry

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Emulator Reset

The CM4 provides a JTAG/COP port (P1100) for board test and evaluation. The COP port provides these reset signals: Hard reset (COP_HRST#), and Test reset (COP_RST#)

These reset signals are generated by test software downloaded to the CM4 through a emulator. They allow the test software to perform hard resets (complete system resets) and test resets.

3.14.2 Soft Resets

The CM4 reset circuit includes two soft reset lines:

- 107_SRESET#
- COP_SRESET#

The Tsi107 Host Bridge outputs the 107_SRESET# to the Decoder CPLD where it is ORed with the COP_SRESET# from the COP port. The 107_SRESET# signal is triggered by application software. The COP_SRESET# is triggered by an emulator (typically test software) attached to the P1100 JTAG/COP port. If one of these reset lines is asserted, the CPU_SRESET# line is asserted causing the processor to perform a soft reset that resets the processor internal logic but does not directly affect the states of output signals.

3.14.3 PCI Resets

When the CM4 is installed in a system slot, it can send PCI resets to peripheral cards in the system through the CompactPCI backplane but cannot receive PCI resets. When the CM4 is installed in a non-system controller slot, it can receive a PCI reset from the system controller but cannot send PCI resets out to the system. This dual mode capability is made possible through the transparent/non-transparent modes of the PCI 6254 PCI Bridge as previously discussed (*see “System Controller vs. Peripheral Operation” on page 3-16*) and the SYSEN# signal, which is asserted when the CM4 is installed in a system slot.

CM4 is a System Controller

When the CM4 is functioning as a system controller and it receives a hard reset, the Decoder CPLD asserts the 107_HRESET# signal to reset the Tsi107 Host Bridge and processor (*see Figure 3-10 on page 3-19*). The Decoder CPLD also asserts the PCI reset output, which resets the following PCI devices on the CM4:

- PCI 6254 PCI Bridge (primary interface)
- 82559ER Ethernet Controller
- StrataFlash boot flash
- Two ST16C2550 UART Transceivers
- PMC site

When the CM4 is the system controller, the PCI 6254 PCI Bridge operates in transparent mode. In transparent mode, the PCI 6254 receives the PCI reset signal on the primary PCI interface reset input (P_RSTIN#) input. When P_RSTIN# is asserted in transparent mode, the secondary PCI interface reset output (S_RSTOUT#) is asserted. The S_RSTOUT# line goes back to the Decoder CPLD where the asserted SYSEN# signal enables an output buffer that drives the reset onto the cPCI backplane as shown in Figure 3-11 on page 3-21.

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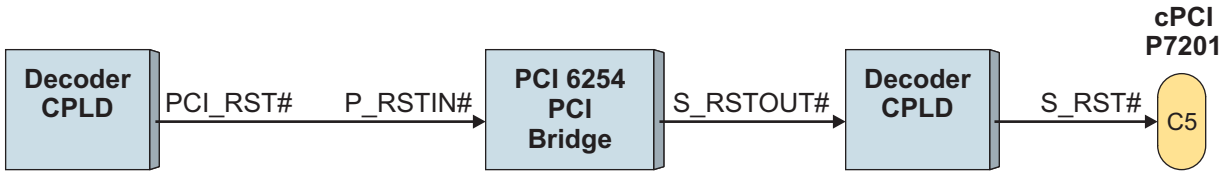


Figure 3-11 PCI reset when CM4 is a system controller

The PCI reset signal is the only signal affected by whether the CM4 is a system controller or peripheral card.

CM4 is a Peripheral Card

When the CM4 is installed in a non-system controller slot, the PCI 6254 PCI Bridge changes to non-transparent mode. In non-transparent mode, the PCI 6254 appears as just another PCI device on the PCI bus. The PCI 6254 receives the P_RSTIN# reset which resets the primary PCI interface but it does not pass the reset on to the secondary PCI interface.

In non-transparent mode, the secondary PCI interface reset output (S_RSTOUT#) becomes an input for system resets from the system controller. When the CM4 is a peripheral card, a PCI reset (S_RST#) is received through the CompactPCI connector P7201, and is routed through the Decoder CPLD. An input buffer enabled by the de-asserted SYSEN# signal drives the PCI reset to the PCI 6254 secondary PCI interface on the S_RSTOUT# line. The PCI reset asserted on the PCI 6254 secondary interface, resets secondary PCI interface configuration registers as shown in Figure 3-12.

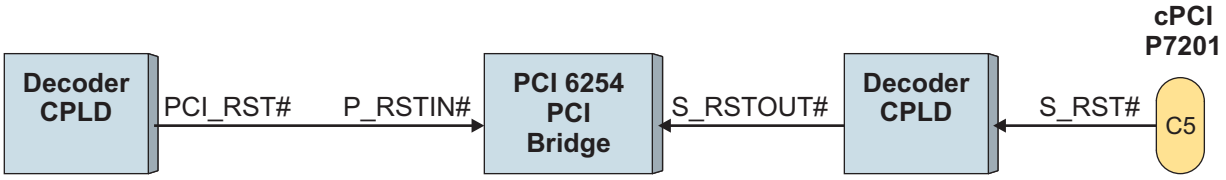


Figure 3-12 PCI reset when CM4 is a peripheral card

3.14.4 Watchdog Timer

The Decoder CPLD includes an integrated watchdog timer that can reset the processor if development application software forces the processor into an unstable condition. After power-up or reset, the watchdog timer is disabled. A write to the Watchdog Control Register WD_ON bit (b0) (*see "Watchdog Control Register" on page 5-1*) enables the watchdog timer. After the watchdog timer is enabled, it counts down—duration of the count is 0.5 seconds. To reset the watchdog timer, the application software must read the Watchdog Control Register before the count expires.

If the watchdog timer count expires, it sends a hard reset signal (WD_RESET#) to the LTC1727 Power Monitor, which then asserts BOARD_RST# as shown in Figure 3-10 on page 3-19.

The application software can determine if a reset was triggered by the watchdog timer or some other cause by reading the Watchdog Control Register.

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3.15 Interrupt Circuitry

The CM4 processor services interrupts generated from several on-board devices, as well as external interrupts from an installed PMC module or from the CompactPCI backplane when the CM4 is installed in a system slot. The Tsi107 Host Bridge includes an Embedded Programmable Interrupt Controller (EPIC) that provides five hardwire interrupt inputs. The CM4 uses four of these interrupt inputs to implement external PCI interrupts from the PCI backplane (CM4 functioning as a system controller) or from an installed PMC module (CM4 functioning either as system controller or peripheral card). The Tsi107 uses the fifth interrupt line for a combined interrupt from the on-board devices.

3.15.1 PCI Interrupts

CM4 is a System Controller

When the CM4 is functioning as a system controller, the Tsi107 Host Bridge can receive up to four PCI interrupts (C_INT[A…D]#) from the CompactPCI backplane through cPCI connector P1701. In the Decoder CPLD, these four interrupts are ANDed with the system enable signal (SYSEN#) to enable open-collector outputs—INT[A…D]# to the Tsi107 EPIC unit as shown in Figure 3-14 on page 3-24. The SYSEN# signal is asserted when the CM4 is installed in a system slot.

CM4 is a Peripheral Card

When the CM4 is a peripheral card, inputs C_ INT[B…D]# are disabled in the Decoder CPLD and input C_INTA# becomes an output from the Decoder CPLD, driven by the PCI 6254 PCI Bridge secondary PCI interface (P6254_SINTA#). The INTA# output from the Decoder CPLD to the Tsi107 EPIC unit is driven by the PCI 6254 primary interface interrupt signal (P6254_PINTA#). The output is enabled by the de-asserted SYSEN#.

PMC PCI Interrupts

If a PMC module is installed on the CM4, it can output four PCI interrupts to the Tsi107 Host Bridge through interrupt outputs (INT[A…D]# regardless of whether CM4 is functioning as system controller or peripheral card as shown in Figure 3-16 on page 3-26. The PMC PCI outputs are rotated so that PMC INTA# is connected to PCI INTD# from the Decoder CPLD as listed in Table 3-13, This is done to reduce interrupt PMC INTA# having to share an interrupt with the busier PCI interrupt INTA#.

Table 3-13 Rotated PMC interrupt connections

PMC PCI Interrupts	PCI Interrupts
INTA#	INTD#
INTB#	INTA#
INTC#	INTC#
INTD#	INTC#

The 82559ER Ethernet controller can also output an interrupt connected to INTB# to the Tsi107 Host Bridge. The Tsi107 Host Bridge interrupt controller accepts interrupts on the four PCI interrupt lines and asserts the CPU_INT# lines as shown in Figure 3-16 on page 3-26.

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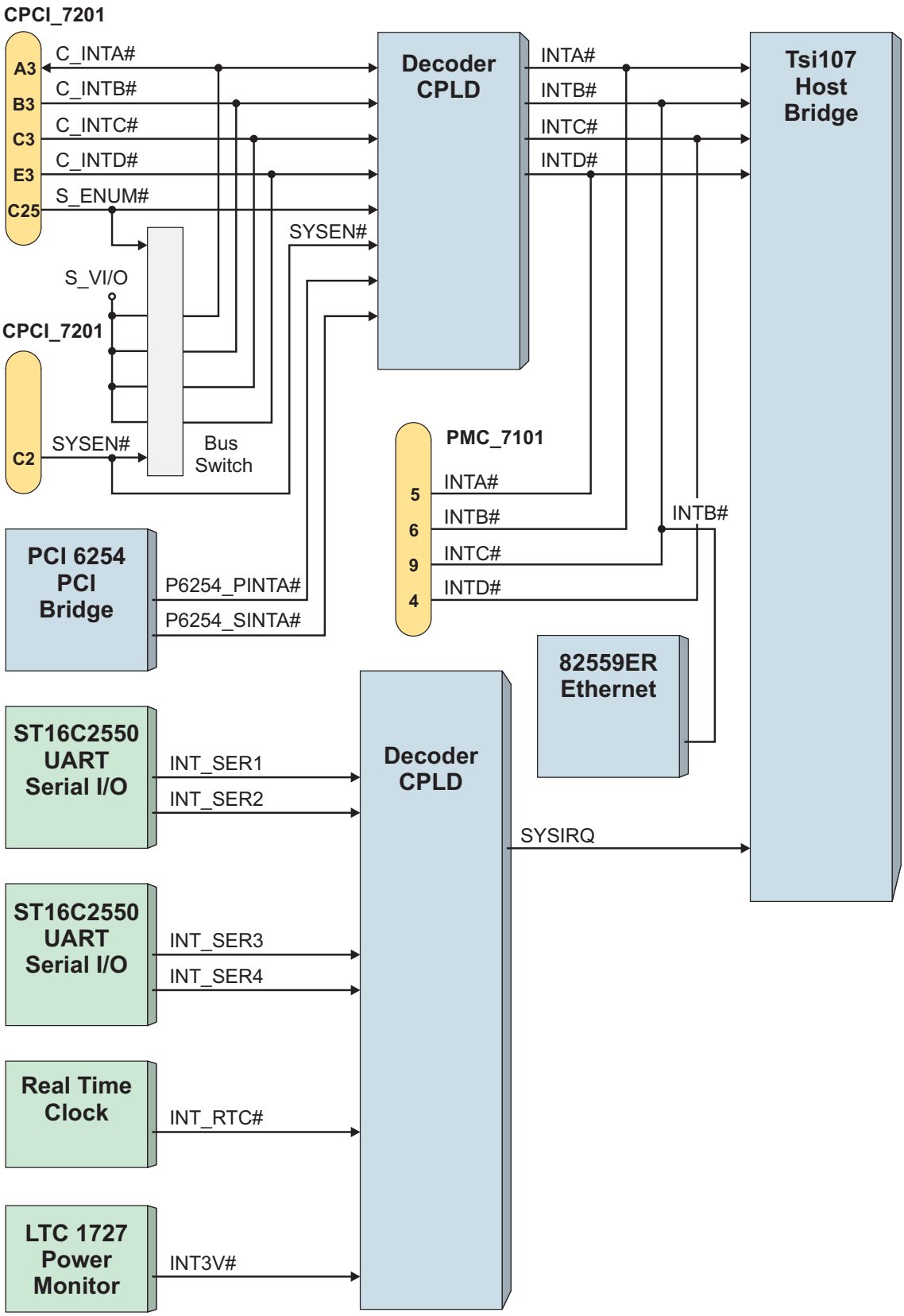


Figure 3-13 Interrupt circuitry

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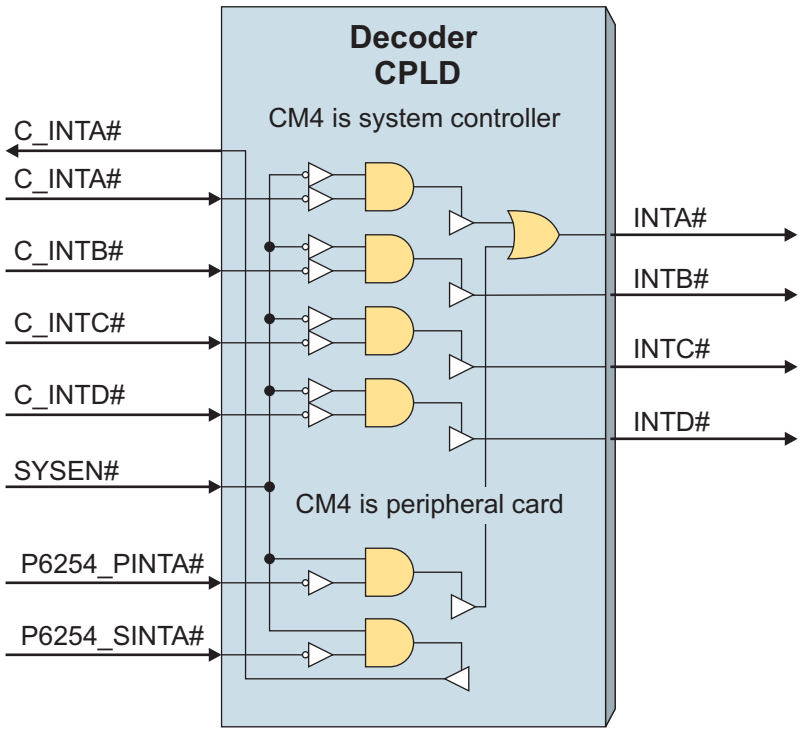


Figure 3-14 Decoder CPLD PCI interrupt circuitry

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3.15.2 On-board Interrupts

The CM4 employs the Decoder CPLD to combine the interrupts from several on-board devices into one interrupt signal—SYSIRQ as shown in Figure 3-13 on page 3-23. The Decoder CPLD receives inputs from the following on-board devices:

- Two Dual ST16C2550 UART serial transceivers
- Real-Time Clock
- LTC 1727 power monitor
- PCI 6254 PCI Bridge

The Decoder CPLD provides the capability of masking any of these device interrupts through the Interrupt Mask register as shown in Figure 3-15.

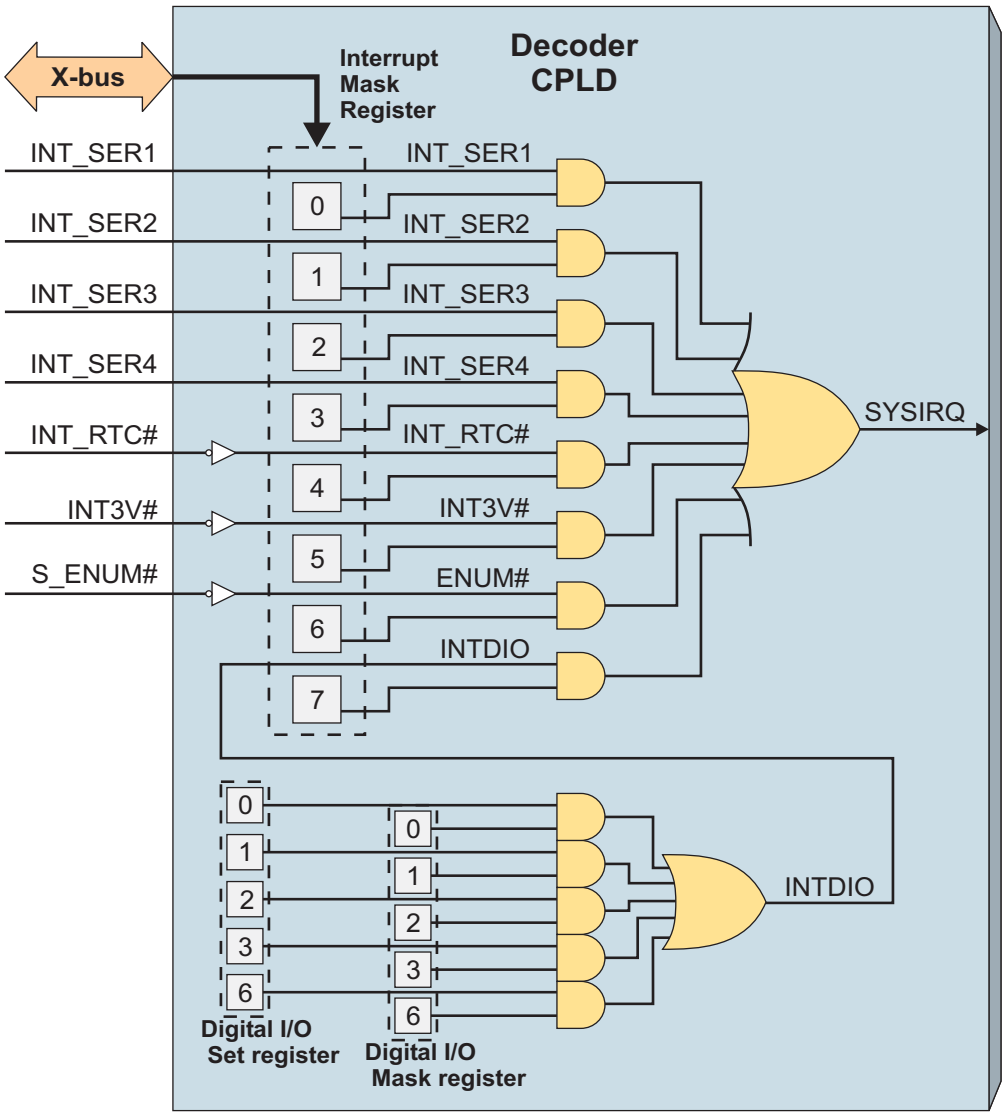


Figure 3-15 Decoder CPLD interrupt circuitry

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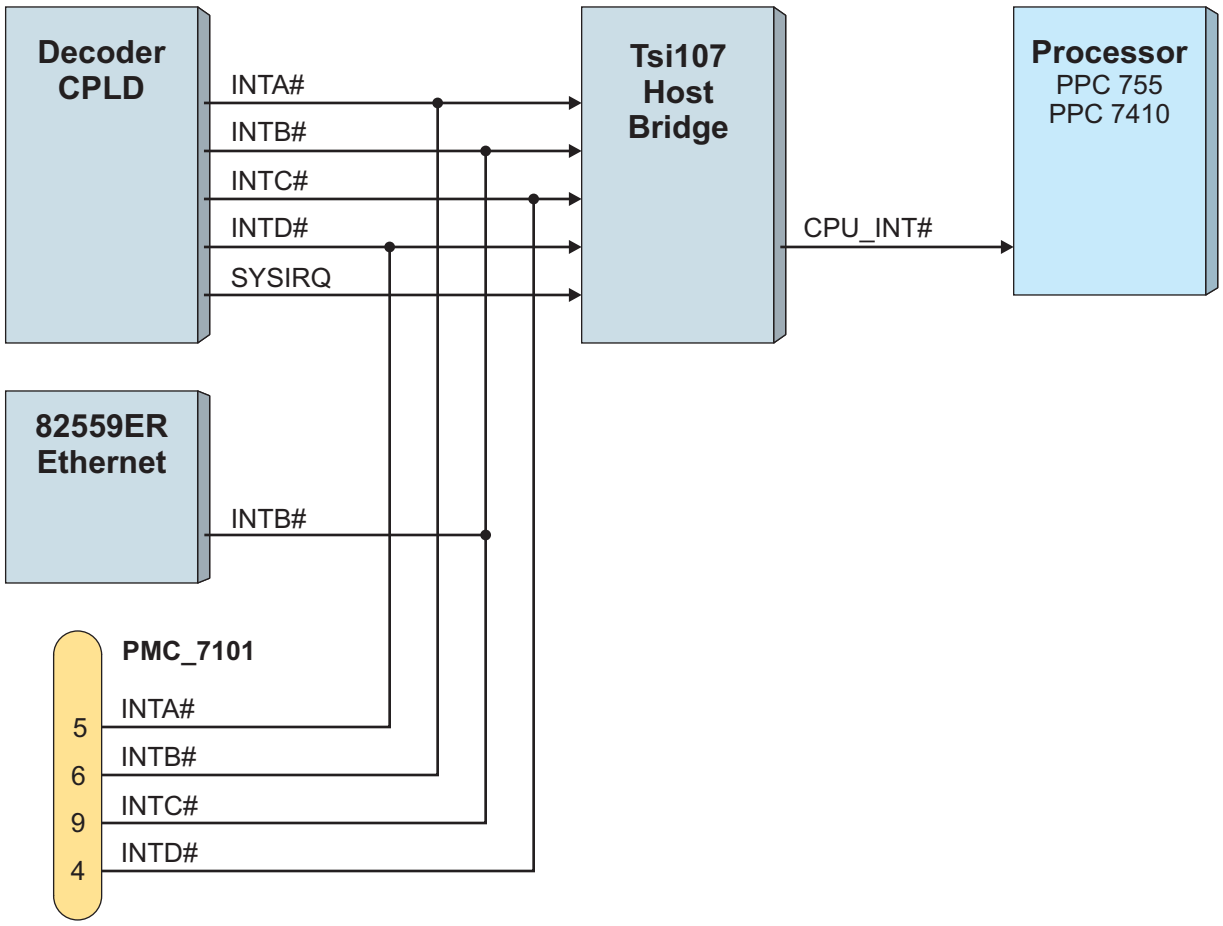


Figure 3-16 CPU interrupt circuitry

3.16 Clock Circuitry

The CM4 clock circuitry begins with one oscillator—14.318MHz input to the ICS9159C-02 clock generator. The ICS9159C-02 clock generator uses the 14.318MHz clock as the main reference clock to generate three clock outputs: 33MHz, 24MHz, and 14.318MHz as shown in Figure 3-17 on page 3-27.

3.16.1 24MHz and 14.318MHz Clocks

The ICS9159C-02 clock generator supplies a 24MHz clock to the two ST16C2550 Dual UART serial transceivers for the programmable baud rate generators. The 14.318MHz clock provides timing to the Decoder CPLD.

3.16.2 Real-Time Clock

The DS1685 Real-Time Clock (RTC) requires and external oscillator to maintain time-of-day clock and memory status. This is provided with a 32.768KHz oscillator.

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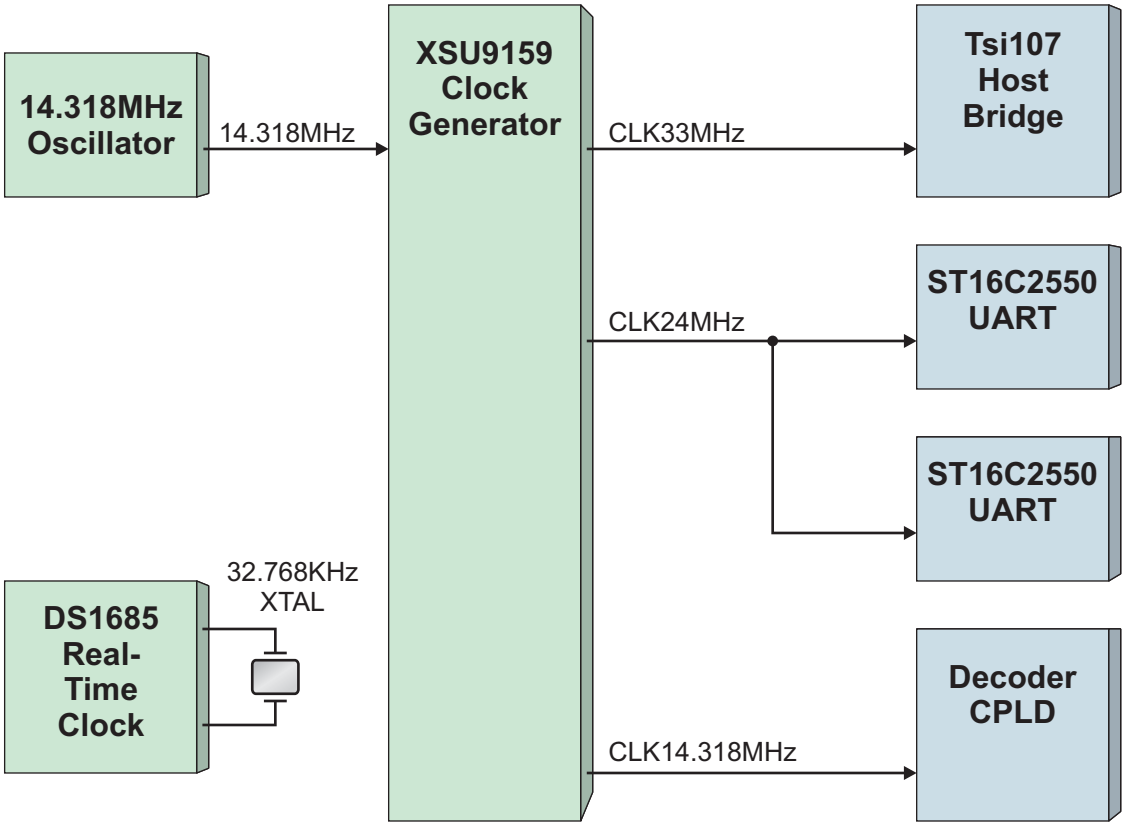


Figure 3-17 Primary clock circuitry

3.16.3 Tsi107 Clock Distribution

Table 3-14 Processor system clocks

Processor	Processor Clock
MPC755	400MHz
MPC7410	500MHz

The 33MHz output from the clock generator provides clocks to most of the other major CM4 components through the Tsi107 Host Bridge. The Tsi107 supplies a 100MHz system clock to the processor (CPU_CLK) and SDRAM. The processor uses the reference clock combined with the Phase-Locked Loop (PLL) configuration settings to determine the processor clock. The processor clocks are listed in Table 3-14. The processor provides timing for on-board L2 cache. The L2 cache runs at 200MHz for all processors.

The Tsi107 distributes the 33MHz clocks through a PCI clock fanout buffer. The CPU and SDRAM clocks go through a Delay-Locked Loop (DLL) buffer to minimize trace-delay effects. The 33MHz clocks are output to the following CM4 devices as shown in Figure 3-18 on page 3-28:

- PCI 6254 PCI bridge
- 82559ER Ethernet controller
- PMC module through P7101connector

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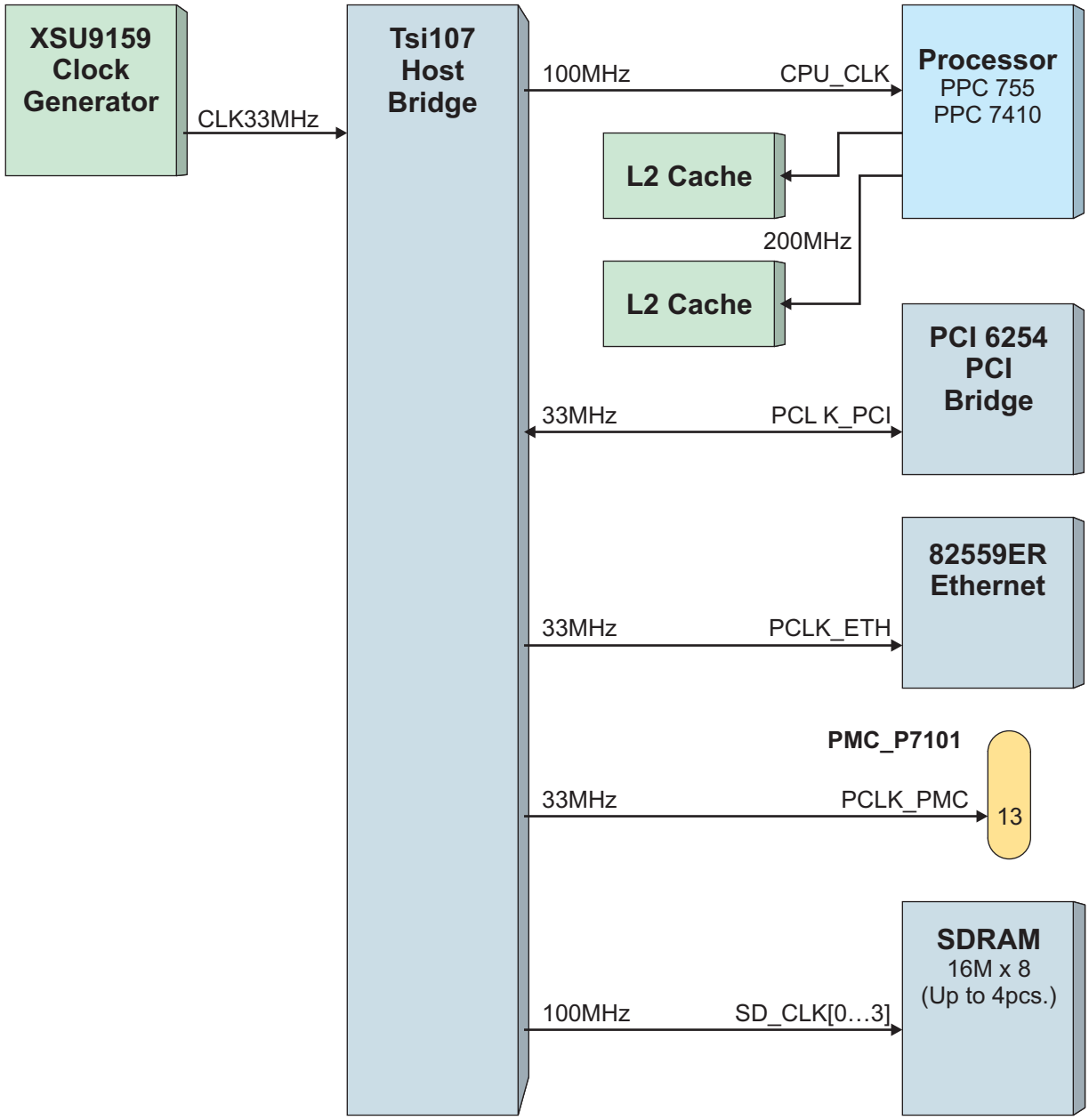


Figure 3-18 PCI clock circuitry

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3.16.4 PCI 6254 PCI Bridge Clock Operation—Transparent Mode

When the CM4 is functioning as a system controller—the CM4 is installed in a system slot and the SYSEN# signal is asserted on the S_CLKOFF input—the PCI 6254 PCI Bridge functions in the transparent mode. The Tsi107 Host Bridge provides a 33MHz PCI clock to the PCI 6254 PCI Bridge. The PCI 6254 receives the PCI clock from the Tsi107 through its primary PCI interface clock input—PCLK_PCI. In transparent mode, the 33MHz PCI input clock at the PCLK_PCI input supplies eight 33MHz clock outputs on the PCI 6254 secondary PCI interface. These eight SCLK clock outputs are enabled by the asserted SYSEN# signal on the S_CLKOFF input. The secondary clock output—SCLK9 provides the PCI clock to the secondary interface through the secondary PCI clock input—S_CLK. Six clock outputs—SCLK[1…6]—are routed to the PCI backplane through CompactPCI connector—P7202; SCLK0 is routed through CompactPCI connector—P7201 as shown in Figure 3-19 on page 3-30.

3.16.5 PCI 6254 PCI Bridge Clock Operation—Non-Transparent Mode

When the CM4 is functioning as a peripheral board—the CM4 is installed in a peripheral slot and the SYSEN# signal is not asserted on S_CLKOFF input—the PCI 6254 PCI Bridge functions in non-transparent mode. In non-transparent mode, the PCI 6254 receives the PCI clock from the SCLK0 input on the secondary PCI interface—seven of the eight SCLK outputs are disabled and SCLK0 becomes an input for the PCI clock from the backplane through CompactPCI connector—P7201. In non-transparent mode, the secondary interface receives its timing from the SCLK0 input and the secondary interface clock input—S_CLK is ignored.

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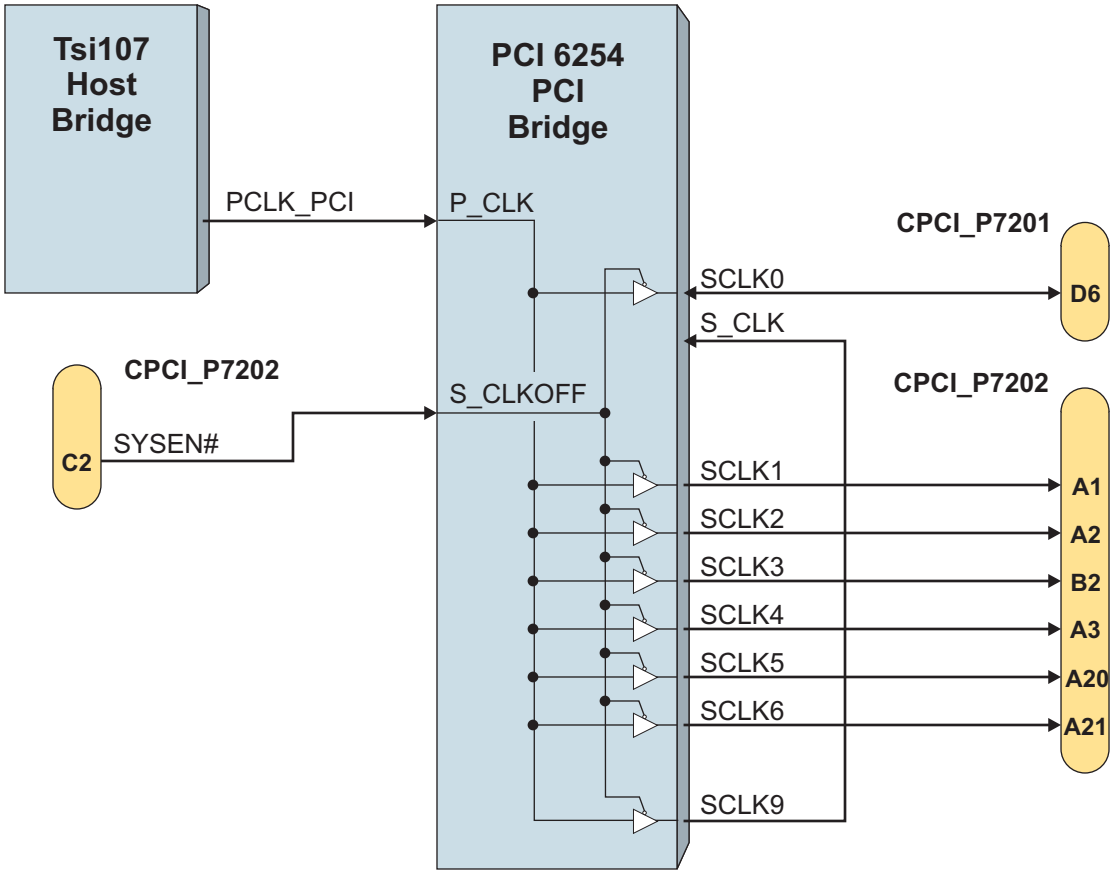


Figure 3-19 cPCI clock circuitry

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Chapter 4: Components

4.1 Component Location

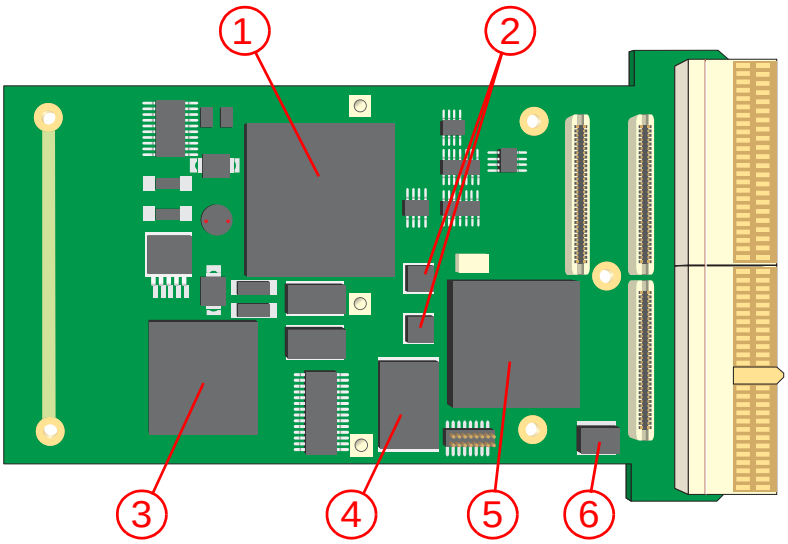


Figure 4-1 CM4 components (front view)

1. Tsi107 Host Bridge (replacing the MPC107 PCI Bridge)
2. Two Dual NS16550 UARTs
3. MPC755 or MPC7410 processor
4. 8MB Boot flash memory
5. PCI 6254 PCI bridge
6. Real-Time Clock

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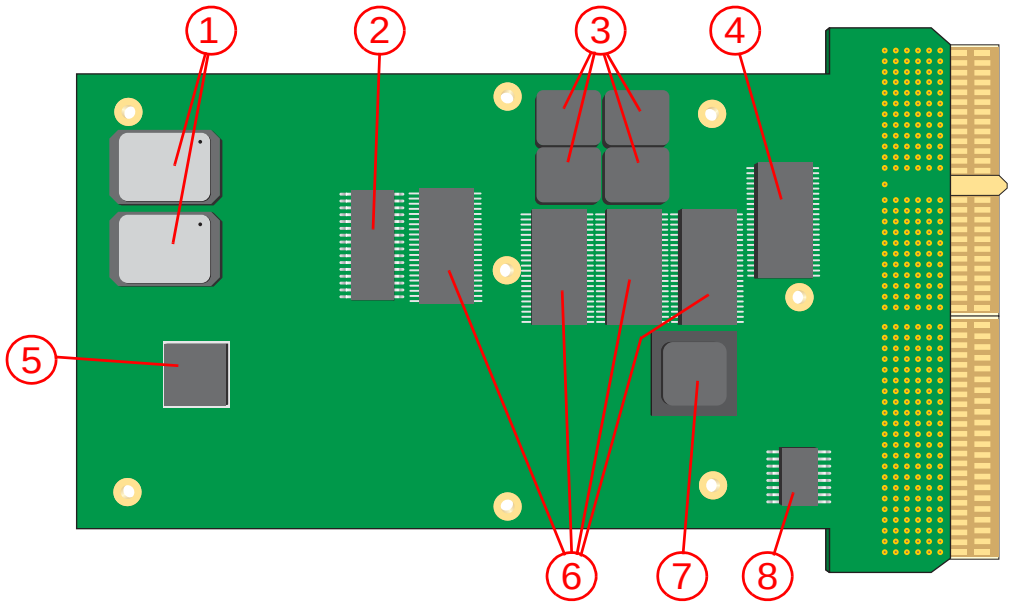


Figure 4-2 CM4 components (back side)

1. L2 Cache
2. NVSRAM
3. Extended StrataFlash memory
4. SDRAM ECC
5. Decoder CPLD
6. SDRAM
7. 82559ER Ethernet controller
8. Ethernet transformer

4.2 Processors

The CM4 offers two processor options: MPC755, and MPC7410. Table 4-1 compares the parameters of each of the processor options.

Table 4-1 Processor parameters

Features	MPC755	MPC7410
System bus interface	60x (100MHz)	60x/MPX (100MHz)
System address bus	32-bit	32-bit
System data bus	64-bit	64-bit
System clock	400MHz	500MHz
L1 Data cache	32KB	32KB
L1 Instruction cache	32KB	32KB
L2 cache support	1MB	2MB
L2 clock speed	200MHz	200MHz

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4.3 Tsi107 Host Bridge

The CM4 features the Tsi107 Host Bridge device that provides the following functions:

- 100MHz 60x system bus interface
- 100MHz memory interface
- Memory controller
- PCI bus interface
- Interrupt controller
- Two-channel DMA controller

NOTE: The Motorola® MPC107 PCI Bridge chip has been replaced by the Tundra® Tsi107 Host Bridge chip.

4.3.1 System Bus Interface

The Tsi107 system bus interface include a 32-bit 100MHz address bus and 64-bit data bus. The system bus conforms to a subset of the 60x bus protocol that support the single-beat and burst-data transfers. The address and data bus are decoupled to support pipelined transactions.

4.3.2 Memory Controller and Bus Interface

The Tsi107 memory controller handles memory transactions between the 16M x 16 SDRAM devices, the processor and the PCI bus. Memory transactions are routed through the 100MHz, 64-bit memory interface and memory buses. The memory data bus is separated into two 32-bit buses: Data high and data low, (*see“Memory/X-bus” on page 3-8*). The high and low memory buses also access the 64Mb extended flash devices.

One 8-bit data bus taps the high data bus and connects to the X-bus through a 16-bit bus transceiver. The X-bus carries data to and from the Decoder CPLD, NVSRAM, Boot flash, RTC, and two serial ST16C2550 UART Transceivers.

4.3.3 PCI Bus Interface

The 32-bit 33MHz PCI bus interface connects the Tsi107 with the 82559ER Ethernet Controller and PCI 6254 PCI Bridge, which connects the Tsi107 to the PCI backplane through P7201 and P7202. It also connects to an installed PMC module through connectors P7101 and P7102.

4.3.4 Interrupt Controller

The Tsi107 includes an Embedded Programmable Interrupt Controller (EPIC) that integrates five hardwire interrupt lines. The CM4 uses these interrupt lines to implement four PCI interrupts (INTA#, INTB#, INTC#, and INTD#) and one combined interrupt (SYSIRQ#) from the on-board devices. The four PCI interrupts are input lines when the CM4 is functioning as a system controller. When the CM4 is a peripheral card, three of the PCI interrupts (INTB#, INTC#, and INTD#) are disabled and the INTA# becomes an output to the cPCI backplane through the Decoder CPLD.

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4.4 PCI 6254 PCI Bridge

The PCI 6254 PCI Bridge provides isolation and connection between the PCI local bus and the cPCI bus. The PCI 6254 PCI Bridge changes how it handles the connections between these two buses according to whether the CM4 is a system controller or peripheral card. When the CM4 is a system controller, the PCI 6254 operates in “transparent” mode, which means that it passes PCI interrupt, reset, and clock signals from the local PCI bus to the cPCI backplane as though it were transparent. When the CM4 is a peripheral card, the PCI 6254 operates in “non-transparent” mode, which means that it appears as a PCI device to the Tsi107 Host Bridge and does not pass PCI resets, interrupts, and clocks from the PCI local bus to the cPCI backplane.

4.5 SDRAM

The CM4 offers one bank of 16M x 16 SDRAM chips (up to four devices) for a total on-board system memory from 128MB to 512MB of SDRAM with a single 8-bit ECC device providing single-bit error correction and double-bit error detection. The memory reside on a 72-bit 100MHz memory bus. The Tsi107 Host Bridge provides the memory controller and interface.

4.6 Flash Memory

The CM4 includes one 8M x 8 E28F640J3A-120 StrataFlash device for boot flash and four 64Mb RC28F640J3A-120 StrataFlash for a total of 64MB of extended flash memory.

4.6.1 Boot Flash

The CM4 boot flash consists of one 8M x 8 E28F640J3A-120 StrataFlash device. It is located on the 8-bit X-bus and is memory-mapped to a fixed address range from 0xFF80_0000 to 0xFFFF_FFFF in the Tsi107 Host Bridge. The CM4 is shipped with a boot loader pre-installed in boot flash. SBS Technologies offers a CM4 Board Support Package (BSP), which includes a boot image for the CM4. To implement a custom boot image, an external boot jumper (not included on CM4) installed on the BOOTSEL pin can redirect the boot process to a different location in boot flash. The BOOTSEL signal is available on the P7202 D4.

The boot flash programming is disabled after CM4 power-up, however, it can be enabled by writing a (1) to the VPEN_BOOT bit (b0) in the Status Output Port register (*see“Status Output Port Register” on page 5-6*).

4.6.2 Extended Flash

The CM4 extended flash consists of one bank of four 64Mb RC28F640J3A-120 StrataFlash devices for a total of 64MB on-board extended flash memory. The extended flash is located on the memory bus and is memory-mapped from 0x7C00_0000 to 0x7FFF_FFFF in the Tsi107 Host Bridge.

The extended flash programming is disabled after CM4 power-up, however, it can be enabled by writing a (1) to the VPEN_FLASH bit (b1) in the Status Output Port register (*see“Status Output Port Register” on page 5-6*)

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4.7 Decoder CPLD

The XC95144XL Decoder CPLD, located on the X-bus, provides the CM4 with discrete programmable logic and registers for the following CM4 circuity:

- Reset
- Interrupt
- Digital I/O

The Decoder also provides control, status, and masking registers as detailed in Chapter 5: CPLD Registers. It also provides logic for many write protect/enable and chip select functions as well as timer/counters such as the watchdog timer and MCP counter.

4.8 82559ER Ethernet Controller

The CM4 provides LAN network communications through the 10/100 fast 82559ER Ethernet Controller. The 82559ER controller provides IEEE 802.3 compatibility at both 10Mb and 100Mb data rates and includes an integrated Physical Layer (PHY) unit with auto-negotiation for full and half duplex at both 10 and 100Mbps data rates The 82559ER Controller includes Media Access Control (MAC), which includes a PCI interface with PCI reset. A 1KB EEPROM attached to the 82559ER Controller provides configuration data storage. The Ethernet signals are routed to the cPCI backplane through cPCI connector P7202.

SBS Technologies offers a CM4 Transition Module that provides 10/100 Ethernet connection through either a rear-panel RJ-45 connector or a surface-mounted connector.

4.9 ST16C2550 Dual Channel UARTs

The CM4 includes two ST16C2550 Dual Channel UARTs for serial communications. Each UART device consists of two NS16450 and NS16550-compliant UART Transceivers. The CM4 implements these channels as two full-duplex RS-232 transceivers and two RS-422/485 transceivers. Each device includes 16 bytes of transmit FIFO memory and 16 bytes of receive FIFO memory, which extends the overall service interval required by the processor. Each UART channel includes a separate chip select and interrupt line.

NOTE: With the external 24MHz clock, each channel is capable of data rates up to 1.5Mbps, however drivers provided by the optional CM4 BSP only support a maximum baud rate to 38400 Baud.

Each ST16C2550 UART device is connected to the Tsi107 Host Bridge through the X-bus and is connected to the cPCI backplane through cPCI connector P7202.

SBS Technologies offers a CM4 Transition Module that provides serial port COM1 connection through a rear-panel DB9 connector or a surface-mounted connector. The remaining serial ports (COM2, COM3, and COM4) are implemented in surface-mounted connectors.

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4.10 STK14C88 NVSRAM

The CM4 provides 32KB of non-volatile static RAM with an AutoStore™ feature. The STK14C88 NVSRAM is located on the X-bus and is memory-mapped from 0xFF00_0000 to 0xFF00_7FFFF in the Tsi107 Host Bridge I/O space.

The STK14C88 NVSRAM has two modes of operation: SRAM mode and non-volatile mode. Each SRAM memory cell has a non-volatile element built into it. In SRAM mode, the NVSRAM operates as a fast static RAM device. In non-volatile mode, data stored in static RAM is transferred to the non-volatile elements or data stored in the non-volatile elements is transferred to the static RAM.

A capacitor attached to the STK14C88 NVSRAM is charged to +5V. This capacitor stores enough power to perform one ‘store’ operation where data in the 32KB static RAM is transferred to the non-volatile elements if supplied power suddenly fails. When power is restored, the device performs a recall operation and the stored data in the non-volatile elements is transferred back to the static RAM.

4.11 DS1685 Real-Time Clock

The CM4 provides a 100-year calendar including a century register, a data alarm register, a timer with periodic interrupt and 242 bytes of user-defined non-volatile RAM. The periodic interrupt is software-controlled. The DS1685 RTC is connected to the Tsi107 Host Bridge through the X-bus and is memory-mapped to the I/O space at 0xFF00_0040 (index register) and 0xFF00_0041 (data register). Table 4-2 on page 4-7 provides the address offsets for internal time, calendar, and alarm data registers for the DS1685 RTC.

The CM4 does not provide battery backup for the DS1685 RTC so when the CM4 is not powered on, the DS1685 RTC requires an external power source. A power can be applied through the BATT+ line available on the cPCI backplane through cPCI connector P7202. The DS1685 RTC is capable of +5V or +3.3V operation.

A 32.768KHz crystal oscillator provides timing to maintain the time-of-day clock and memory status when the CM4 is powered off.

SBS Technologies offers a CM4 Transition Module that provides connection to the BATT+ line through the Miscellaneous connector, a 26-pin surface-mounted connector.

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Table 4-2 Real-Time Clock time, calendar and alarm data modes

Address	Function	Decimal Range	Data Mode Range	
			Binary	BCD
0x01	Seconds	0 to 59	00 to 3B	00 to 59
0x02	Seconds Alarm	0 to 59	00 to 3B	00 to 59
0x03	Minutes	0 to 59	00 to 3B	00 to 59
0x04	Minutes Alarm	0 to 59	00 to 3B	00 to 59
0x05	Hours 12-hour mode	1 to 12	01 to 0C AM 81 to 8C PM	01 to 12 AM 81 to 92 PM
	Hours 24-hour mode	0 to 23	00 to 17	00 to 23
0x06	Hours Alarm 12-hour mode	1 to 12	01 to 0C AM 81 to 8C PM	01 to 12 AM 81 to 92 PM
	Hours Alarm 24-hour mode	0 to 23	00 to 17	00 to 23
0x07	Day of Week (Sunday = 1)		01 to 07	01 to 07
0x08	Date of Month	1 to 31	01 to 1F	01 to 31
0x09	Month	1 to 12	01 to 0C	01 to 12
0x0A	Year	0 to 99	00 to 63	00 to 99
	Century	0 to 99	00 to 63	00 to 99
	Data Alarm	1 to 31	01 to 1F	01 to 31

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Chapter 5: CPLD Registers

5.1 Watchdog Control Register

The CPLD includes watchdog timer circuitry that can reset the processor if development application software forces the hardware into an unstable state. The Watchdog Control register is an 8-bit read/write register that enables and controls the watchdog timer. CM4 BSP firmware writes a (1) to the WD_ON bit (b0) to enable the watchdog timer. The watchdog timer has a 0.5 second time-out. Optional CM4 BSP firmware can read the Watchdog Control Register to reset the count. If the BSP firmware does not reset the count and it expires, the watchdog circuitry issues a reset signal to the processor.

Address offset: 0xFF00_8000

Access: Read/write

Bit(s)	Field	Default	Description
7 to 3	RSVD	N/A	Reserved—always read as (0).
2	WD_EXP	b0	Watchdog timer Expired—indicates the watchdog timer has expired. 0 = timer has not expired 1 = timer has expired **NOTE:** Writing a (1) to this bit clears the bit.
1	WD_SET	b0	Watchdog timer—forces the WD_REL signal, at the P7202 connector, to (1). 0 = WDG_REL is set if watchdog is expired 1 = WDG_REL is always set
0	WD_ON	b0	Watchdog timer Enable—enables the watchdog timer. 0 = disable 1 = enable

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5.2 MCP Ticker Control Register

The MCP Ticker Control register is an 8-bit read/write register that sets the duration of the reset timer and provides the ability to read the status of the Non-Maskable Interrupt (NMI). The NMI is held de-asserted when the T_SEL bits (b2–0) are (000).

Address offset: 0xFF00_8001

Access: Read/write

Bit(s)	Field	Default	Description
7 to 4	RSVD	N/A	Reserved—always reads as (0).
3	NMI (read-only)	b0	Non-Maskable Interrupt—provides the status of the NMI signal. 0 = NMI disabled 1 = NMI enabled
2 to 0	T_SEL	b000	Time Select—sets the interval for the MCP timer. 000 = timer disabled 001 = 0.29ms 010 = 0.58ms 011 = 1.17ms 100 = 2.34ms 101 = 4.67ms 110 = 9.34ms 111 = 18.69ms

5.3 MCP Ticker Reset Register

The MCP Reset register is an a 8-bit write-only register that, when written to, resets the NMI input to the MCP107 Host Bridge. The data written can be any value.

Address offset: 0xFF00_8002

Access: Write-only

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5.4 Interrupt Status Register

The Interrupt Status register is an 8-bit read-only register that provides status indications for interrupt signals from various CM4 components.

Address offset: 0xFF00_8010

Access: Read-only

Bit	Field	Default	Description
7	DI/O_INT		Digital I/O Interrupt 0 = interrupt de-asserted 1 = interrupt asserted
6	ENUM		ENUM Interrupt 0 = interrupt de-asserted 1 = interrupt asserted
5	INT3V		+3.3V Interrupt 0 = interrupt de-asserted 1 = interrupt asserted
4	RTC_INT		Real Time Clock Interrupt 0 = interrupt de-asserted 1 = interrupt asserted
3	SER_INT4		Serial port COM4 Interrupt 0 = interrupt de-asserted 1 = interrupt asserted
2	SER_INT3		Serial port COM3 Interrupt 0 = interrupt de-asserted 1 = interrupt asserted
1	SER_INT2		Serial port COM2 Interrupt 0 = interrupt de-asserted 1 = interrupt asserted
0	SER_INT1		Serial port COM1 Interrupt 0 = interrupt de-asserted 1 = interrupt asserted

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5.5 Interrupt Mask Register

The Interrupt Mask register is an 8-bit read/write registers that provides the capability of masking or inhibiting interrupt signals from various interrupt sources such as the two ST16C2550 Dual Channel UART Transceivers, Real-Time Clock, and digital I/O circuitry.

Address offset: 0xFF00_8011

Access: Read/write

Bit	Field	Default	Description
7	DI/O_INT_MSK	b0	Digital I/O Interrupt Mask 0 = disable mask 1 = enable mask
6	ENUM_MSK	b0	ENUM Interrupt Mask 0 = disable mask 1 = enable mask
5	INT3V_MSK	b0	+3.3V Interrupt Mask 0 = disable mask 1 = enable mask
	NOTE: Writing a (0) to the INT3V_MSK bit also clears the corresponding interrupt if the +3.3V monitor circuit is no longer detecting an error.		
4	RTC_INT_MSK	b0	Real Time Clock Interrupt Mask 0 = disable mask 1 = enable mask
3	SER_INT4_MSK (write-only—always reads (0))	b0	Serial port COM4 Interrupt Mask 0 = disable mask 1 = enable mask
2	SER_INT3_MSK (write-only—always reads (0))	b0	Serial port COM3 Interrupt Mask 0 = disable mask 1 = enable mask
1	SER_INT2_MSK (write-only—always reads (0))	b0	Serial port COM2 Interrupt Mask 0 = disable mask 1 = enable mask
0	SER_INT1_MSK (write-only—always reads (0))	b0	Serial port COM1 Interrupt Mask 0 = disable mask 1 = enable mask

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5.6 Status Input Port Register

The Status Input Port register is an 8-bit read-only register that provides a status indication for the PCI bus frequency (always set to 33MHz), Flash EEPROM status, and an optional external boot select jumper that allows a custom boot image to be loaded into the boot flash. This register is external to the CPLD but is controlled by the CPLD.

Address offset: 0xFF00_8050

Access: Read-only

Bit(s)	Field	Description
7	PCI_BUS_FREQ	Master PCI Bus Frequency 1 = 33MHz
6	FLASH_EEPROM_STS	Flash EEPROM Status 0 = programming or erase function in progress 1 = data available
5	BOOTSEL	BOOTSEL signal status—indicates the status of the BOOT-SEL signal. 0 = jumper installed 1 = jumper not installed
	NOTE: CM4 does not include an on-board BOOTSEL jumper, however, an external jumper may be attached to this signal.	
4 to 0	GA4 to GA0	Geographical Address—connects to GA pins on cPCI 7202 connector.

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5.7 Status Output Port Register

The Status Output Port register is an 8-bit read/write register that controls the outputs for an optional external BITOK LED, the Serial Presence Detect EEPROM, and the write protection for boot and extended flash memory.

Address offset: 0xFF00_8051

Access: Read/write

Bit(s)	Field	Default	Description
7 to 4	RSVD	N/A	Reserved—always reads as (0).
3	BITOK	b0	BITOK Status LED—drives an open-drain output that can control an off-board LED. 0 = LED is off 1 = LED is on **NOTE:** After reset, the BITOK bit is cleared (0).
2	WP_SPD	b0	SPD Serial EEPROM Write Protect 0 = write protect enabled 1 = write protect disabled **NOTE:** After reset, the WP_SPD bit is cleared (0).
1	VPEN_FLASH	b0	VPEN Extended Flash Write Protect 0 = write protect enabled 1 = write protect disabled **NOTE:** After reset, the VPEN_FLASH bit is cleared (0).
0	VPEN_BOOT	b0	Boot Flash Write Protect 0 = write protect enabled 1 = write protect disabled **NOTE:** After reset, the VPEN_BOOT bit is cleared (0).

5.8 CPLD Version Register

The CPLD Version register is an 8-bit read-only register that provides the CPLD version number.

Address offset: 0xFF00_8053

Access: Read-only

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5.9 Digital I/O Registers

The Digital I/O interface consists of four registers that direct the flow of digital control signals. Each digital I/O register uses bits 4–0 and bit 6.

5.9.1 DOUT Register

The DOUT register is an 8-bit write-only register that, when enabled, contains the digital output values to be sent to the cPCI bus.

Address offset: 0xFF00_8060

Access: Write-only

Bit(s)	Field	Default	Description
7	RSVD	N/A	Reserved—always reads (0).
6	DIG_OUT_6	b0	Digital Output 6
5 to 4	RSVD	N/A	Reserved—always reads (0).
3	DIG_OUT_3	b0	Digital Output 3
2	DIG_OUT_2	b0	Digital Output 2
1	DIG_OUT_1	b0	Digital Output 1
0	DIG_OUT_0	b0	Digital Output 0

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5.9.2 DOUTEN Register

The DOUTEN register is an 8-bit write-only register that enables buffers for the digital output lines to the cPCI bus.

Address offset: 0xFF00_8061

Access: Write-only

Bit(s)	Field	Default	Description
7	RSVD	N/A	Reserved—always reads (0).
6	DIG_OUTEN_6	b0	Digital Output Enable 3—enables output buffer for port 6.
5 to 4	RSVD	N/A	Reserved—always reads (0).
3	DIG_OUTEN_3	b0	Digital Output Enable 3—enables output buffer for port 3.
2	DIG_OUTEN_2	b0	Digital Output Enable 2—enables output buffer for port 2.
1	DIG_OUTEN_1	b0	Digital Output Enable 1—enables output buffer for port 1.
0	DIG_OUTEN_0	b0	Digital Output Enable 0—enables output buffer for port 0.

5.9.3 DINQ Register

The DINQ register is an 8-bit read-only register that contains the input values sampled from the cPCI bus.

Address offset: 0xFF00_8062

Access: Read-only

Bit(s)	Field	Default	Description
7	RSVD	N/A	Reserved—always reads (0).
6	DIG_INPUT_6	b0	Digital Input6
5 to 4	RSVD	N/A	Reserved—always reads (0).
3	DIG_INPUT_3	b0	Digital Input3
2	DIG_INPUT_2	b0	Digital Input 2
1	DIG_INPUT_1	b0	Digital Input 1
0	DIG_INPUT_0	b0	Digital Input 0

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5.10 DI/O Interrupt Status Register

The DI/O Interrupt Status register is an 8-bit read/write register that provides status indications for digital I/O interrupts. A bit set in this register indicates a transition edge was detected on the corresponding signal. The DI/O Interrupt Mask register (*see page 5-10*) does not prevent bits from appearing to be set in this register. Writing a (1) to a bit in this register clears the bit and the corresponding interrupt.

NOTE: Bits in this register may be set during board reset, but they will not assert the interrupt since the reset will assert the associated mask bits. Application software should clear the five digital I/O interrupt bits before using this function after any reset.

Address offset: 0xFF00_8012

Access: Read/write

Bit	Field	Default	Description
7	RSVD	-	Reserved—always reads as (0).
6	DI/O6_INT	x	Digital I/O_6 Interrupt 0 = interrupt de-asserted 1 = interrupt asserted
5 to 4	RSVD	-	Reserved—always reads as (0).
3	DI/O3_INT	x	Digital I/O_3 Interrupt 0 = interrupt de-asserted 1 = interrupt asserted
2	DI/O2_INT	x	Digital I/O_2 Interrupt 0 = interrupt de-asserted 1 = interrupt asserted
1	DI/O1_INT	x	Digital I/O_1 Interrupt 0 = interrupt de-asserted 1 = interrupt asserted
0	DI/O0_INT	x	Digital I/O_0 Interrupt 0 = interrupt de-asserted 1 = interrupt asserted

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5.11 DI/O Interrupt Mask Register

The DI/O Interrupt Mask register is an 8-bit read/write register that provides the capability of masking the digital I/O interrupts. Setting a bit (1) allows the corresponding signal to assert the interrupt.

Address offset: 0xFF00_8013

Access: Read/write

Bit	Field	Default	Description
7	RSVD	N/A	Reserved—always reads as (0).
6	DI/O6_INT_MSK	b0	Digital I/O_6 Interrupt Mask 0 = disable mask 1 = enable mask
5 to 4	RSVD	N/A	Reserved—always reads as (0).
3	DI/O3_INT_MSK	b0	Digital I/O_3 Interrupt Mask 0 = disable mask 1 = enable mask
2	DI/O2_INT_MSK	b0	Digital I/O_2 Interrupt Mask 0 = disable mask 1 = enable mask
1	DI/O1_INT_MSK	b0	Digital I/O_1 Interrupt Mask 0 = disable mask 1 = enable mask
0	DI/O0_INT_MSK	b0	Digital I/O_0 Interrupt Mask 0 = disable mask 1 = enable mask

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Chapter 6: Customer Service

6.1 Introduction

This chapter provides forms and information for requesting product service or repair. The following information is included:

- Contact information for technical support service and repair
- Product warranty information
- Return Material Authorization (RMA) information
- Documentation Feedback form

Returned product will not be accepted without a properly authorized RMA number. An RMA number can be authorized by contacting SBS Technologies Customer Service Department (*see"Customer Service" on page 6-2*). To avoid applicable charges, the customer should make every effort to resolve issues including consulting the technical sections of this manual and contacting Technical Support before securing an RMA.

SBS Technologies makes every effort to include all the information needed to properly install, set up and operate our products in our User's Guides. However, if information is needed that cannot be found in the manual, please include relevant comments, suggestions and constructive criticisms in the Documentation Feedback Form and return it to SBS Technologies.

6.2 Updated User Guides and Data Sheets

The latest revisions of product documentation including User's Guides and Data Sheets are available in PDF format from the SBS web site. PDF documents can be viewed using Adobe® Acrobat Reader, which is available for downloading from the Adobe web site (www.adobe.com) at no charge.

All product documentation can be requested through SBS Technologies Customer Service Department (*see"Customer Service" on page 6-2*).

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6.3 Customer Service

The following is contact information for SBS Technologies Customer Service Department:

E-mail: support.sbc@sbs.com
Telephone: (919) 851-1101
Fax.: (919) 851-2844
Mail: SBS Technologies
6301 Chapel Hill Rd.
Raleigh, N.C. 27607-5115

6.4 Warranty Information

SBS Technologies provides a two-year product warranty. Included in the warranty are specific stipulations concerning application and use of the product. Please review the warranty before requesting service.

6.4.1 Warranty

All Single Board Computer (SBC) products manufactured and sold by SBS Technologies, Inc. include a two-year warranty for defects in workmanship and materials for hardware, unless otherwise stated in an Original Equipment Manufacturer (OEM) agreement or contract with SBS Technologies. Software is warranted to be readable and functional upon receipt. This warranty shall not apply to equipment that has been repaired or altered outside of SBS facilities in any way as to, in the judgement of SBS, affect its reliability. Nor will it apply: if the equipment has been used in a manner exceeding its specifications, if the serial number has been removed, or if the equipment has been subject to accident, disaster, improper or inadequate maintenance, or electrical or physical misuse, misapplication, or abuse.

SBS will, at its option, repair or replace the defective item at its factory under the terms of this warranty, subject to the provisions and specific exclusions listed herein.

SBS does not assume any liability for consequential damages as a result of the use of its products. Under no circumstances shall the liability of SBS exceed the original selling price of the equipment.

The equipment warranty shall constitute the sole and exclusive remedy of any buyer of SBS equipment and the sole and exclusive liability of SBS, its affiliates, successors or assigns, in connection with equipment purchased and in lieu of all other warranties expressed, implied, or statutory, including, but not limited to, any implied warranty of merchant ability or fitness for a particular purpose and all other obligations or liabilities of SBS, its affiliates, successors, or assigns.

The equipment must be returned securely packaged in anti-static bags and labeled with a Return Material Authorization (RMA) number written on the outside of the package. The package must be insured, and the shipping cost must be paid. SBS will repair or replace failed parts within the limits of the warranty statement referenced above and return the item at no charge. Standard

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repair charges may apply if: there is a lack of proof of the date of purchase, modifications have been performed, the unit has been operated outside its specifications, and /or if the warranty period has expired.

This description of SBS' limited warranty is only a summary; please review the terms of the product warranty for specific coverage and exclusions.

6.4.2 Non-Warranty Terms and Conditions

Payment for all out-of-warranty repairs must be prearranged through a purchase order or credit card information before a RMA number can be issued. SBS Technologies charges a firm, fixed price for repair of non-warranty boards. Third party products purchased through SBS and returned for repair will follow the warranty schedule for that manufacturer. Non-warranty repairs require a purchase order upon receipt of a repair quote and prior to any work being performed.

6.5 Return Material Authorization (RMA)

Important! An RMA number must be issued before product can be returned

To receive an RMA number:

1. Contact the SBS Single Board Computer Technical Support through the RMA Coordinator.

   Phone: (919) 851-1101 (choose the Technical Support option, then choose RMA option)
   Fax.: (919) 851-2844
   Email: rma.sbc@sbs.com

   Please provide the following information:

   Company name
   Contact person
   Telephone
   Email
   Name of product

2. The RMA Coordinator will contact you and issue an RMA number. The following information will be needed:

   Name of product
   Serial number
   Purchase order number (if out of warranty)
   Description of problem

Important! The RMA Coordinator will determine if warranty applies.

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3. When an RMA number is received, attach the RMA number to the product and ship to:

   SBS Technologies
   Attn.: (*insert RMA number here*)
   6301 Chapel Hill Rd.
   Raleigh, N.C. 27607-5115

4. The product must be securely packaged in an anti-static envelope and placed in a cushioned, corrugated carton (use the original shipping carton if possible).



Caution! Always use proper Electrostatic Discharge (ESD) protection when handling printed circuit boards to avoid seriously damaging components. Product handlers must always be properly grounded.

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6.6 Documentation Feedback Form

The object of a user's guides is to communicate technical information concerning the product's setup and operation from the people who designed the product to the people who will use the product. In our continuous attempt to improve the usefulness of the manuals that accompany our products, we provide this form to give customers and end-users the opportunity to feedback comments, suggestions and constructive criticisms to SBS Technologies concerning the accuracy and usability of product manuals.

This feedback should include:

- Additional information that would be helpful to set up and operate the product
- Missing information
- Information that is incomplete, inaccurate, or misleading
- Information that is difficult to understand and needs further clarification
- Information that was beneficial or that made the manual easier to use

Print the form below, fill it out, and fax it to SBS Technologies (919 851-2844).

Section	Page(s)	Comments
Chapter 1: Introduction		
Chapter 2: Getting Started		
Chapter 3 Board Description		
Chapter 4 Components		
Chapter 5 CPLD Registers		
Chapter 6: Customer Service		
Index		
Other Comments and Suggestions		

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Document No. 70000340-300 and 70000345-300
Revision F

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