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cPRO3
Technical Manual

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SBS Technologies, Inc.

cPRO3

3U CompactPCI Single Board Computer

Technical Manual

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cPRO3 Technical Manual
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This manual applies to the cPRO3 CompactPCI PC, revision 10 and above, until superceded.

Revision Date	By	Comments
09-22-1999	jev	Initial release
02-07-2001	jev	Update text, correct for typo's, heatsink, etc.
11-08-2002	jev	Corrected keyboard/mouse connector drawings on page 3-2.

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This manual uses some generally accepted conventions for clarity and accuracy. These include:

- The use of an 'H' suffix before a number indicates hexadecimal (base sixteen) notation.
- The use of a '-' (minus) suffix to a signal name indicates an active low signal. The signal is either true when it is at a logic zero level or the signal initiates actions on a high-to-low transition.
- Text in `Courier` Font indicates a command entry or output from an SBS embedded PC product using its built-in character set.

This manual is designed to provide information regarding the general use and application of the cPRO3 CompactPCI computer, as well as detail the hardware design. Software methods and programming information are also provided in Chapter 6 of this manual.

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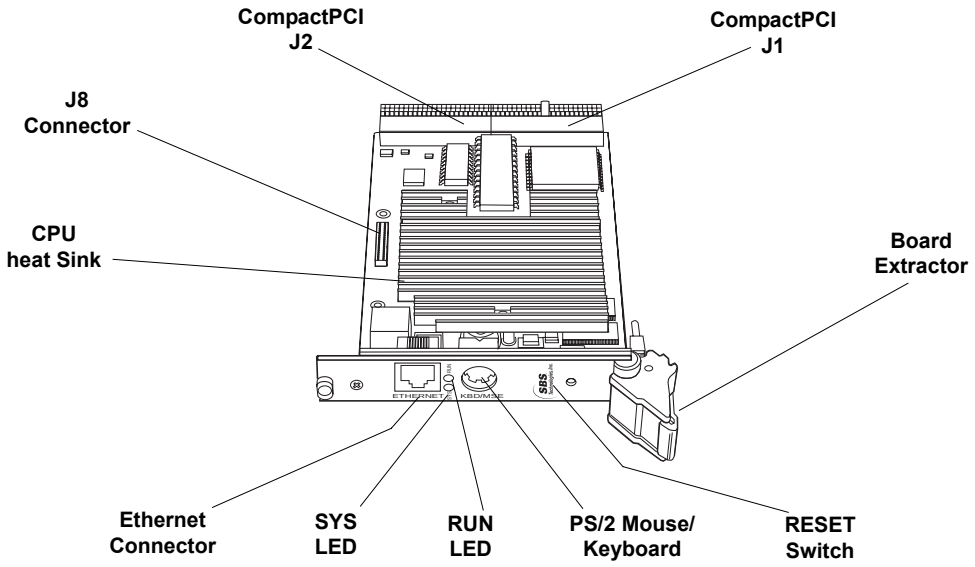
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CHAPTER 1 Introduction



Chapter Scope

This chapter describes the features, capabilities and compatibilities of the cPRO3 CompactPCI Computer. The cPRO3 supports the Intel Pentium MMX or AMD K6-2 processor, and is designed for embedded application.

IBM PC/AT Compatibility Features

CompactPCI Specification

The cPRO3 is an extension of the Proteus family of embedded computers from SBS Technologies, intentionally designed without excessive overhead to facilitate customizing for specific requirements. The cPRO3 is based on the CompactPCI Specification of the PCI Industrial Computers Manufacturing Group (PICMG). The CompactPCI specification is an electrical "superset" of desktop PCI, that uses the Eurocard form factor popularized by the VMEbus. The backplane connector has 47 rows of 5 pins per row, for a total of 220 pins (3 rows of 5 pins are lost to the keying area). The connector is divided into 2 halves; the lower half (110 pins) called J1 and the upper half (110 pins) called J2. The cPRO3's 3U physical size of 3.94 in. x 6.30 in. (100 x 160 mm) and electrical characteristics are compliant with the specification standard. Most I/O is through the backplane connectors, but KBD, Mouse and Ethernet connectors are also provided on the front panel.

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The cPRO3 provides interface for the most common peripherals such as keyboard and mouse ports, parallel port, serial ports (COM1/COM2), USB, Ethernet, floppy and IDE. Continuous video capability is not an operational necessity, and is thus left to be enabled by the addition of a cPCI video card. Various cards are available, so the video capabilities can be readily tailored to the individual situation.

Intel Pentium Microprocessors

The cPRO3 is available from the factory with an Intel Pentium processor at a variety of speeds. The 133MHz to 233MHz Pentium MMX processors are currently supported, and support for future Pentium processors is provided. The 266MHz to 333MHz AMD K6-2 processors are currently supported. Each processor will run standard software written for the PC/AT. They provide the capability of running 8-bit (8086), 16-bit (80286), as well as full 32-bit (80386) software and operating systems. This choice of processors allows you to select a cPRO3 with the performance best suited to your application.

Compatible ROM BIOS

The cPRO3 uses an Award BIOS in a Flash ROM to allow future BIOS upgrades to be programmed on-site. The BIOS provides low-level machine dependent software functions, therefore relieving MS-DOS or any other common operating system from dealing with the hardware directly. Since a great many software programs use calls to the BIOS rather than to MS-DOS, it is important to have a BIOS that functions exactly like the original PC/AT BIOS.

Compatible I/O

The cPRO3 incorporates the I/O capabilities of a complete PC/AT by using the Aladdin M1543 Super I/O controller. These capabilities include two RS-232 serial communications ports, a parallel printer port, 2 Universal Serial Bus (USB) ports, and a keyboard / mouse port. Ethernet is also available at the front panel or at the backplane via the TB-cPRO3 transition board. COM1 and COM2 are at TTL levels out of J2. The COM2 serial port is enhanced for jumper selectable RS-422 or RS-485 operation using the TB-cPRO3 transition board.

System Memory

The cPRO3 is available from the factory with EDO RAM memory of 32 Megabytes (MB).

Floppy Controller

The M1543 also includes a fully PC/AT compatible floppy disk controller onboard the cPRO3. It can control two separate 3.5” 1.44M floppy disk drives. The floppy control signals are provided through connector J8. An optional Transition Board (TB-IDE) is available to enable simple connection to an external disk drive using a standard PC ribbon cable.

Integrated Drive Electronics (IDE) Controller

The onboard **E**nhanced **I**ntegrated **D**rive **E**lectronics (EIDE) controller provided through the ALI chip set is an industry standard IDE interface for a “hard” disk drive or other peripheral. The Primary IDE control signal is provided through connector J4. The TB-IDE Transition Board also enables simple connection to an external hard disk drive using a standard PC ribbon cable.

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CHAPTER 2

Unpacking, Inspection, and Initial Operation

Chapter Scope



ATTENTION
Static Sensitive Devices
Handle only at Static Safe Work Stations

This chapter covers the suggested inspection and preparation considerations and background information necessary prior to using the cPRO3. Unpacking, initial inspection, and first-time operation of the cPRO3 are covered. Following the procedures given in the chapter is recommended, since they will verify proper operation after shipping and before the product is integrated into your computer system.

Electrostatic Discharge Notice

The discharge of static electricity, known as electrostatic discharge or ESD, is a major cause of electronic component failure. The cPRO3 has been packaged in a static-safe bag which protects the board from ESD while the board is in the bag. Before removing the cPRO3 or any other electronic product from its static-safe bag, be prepared to handle it in a static-safe environment.

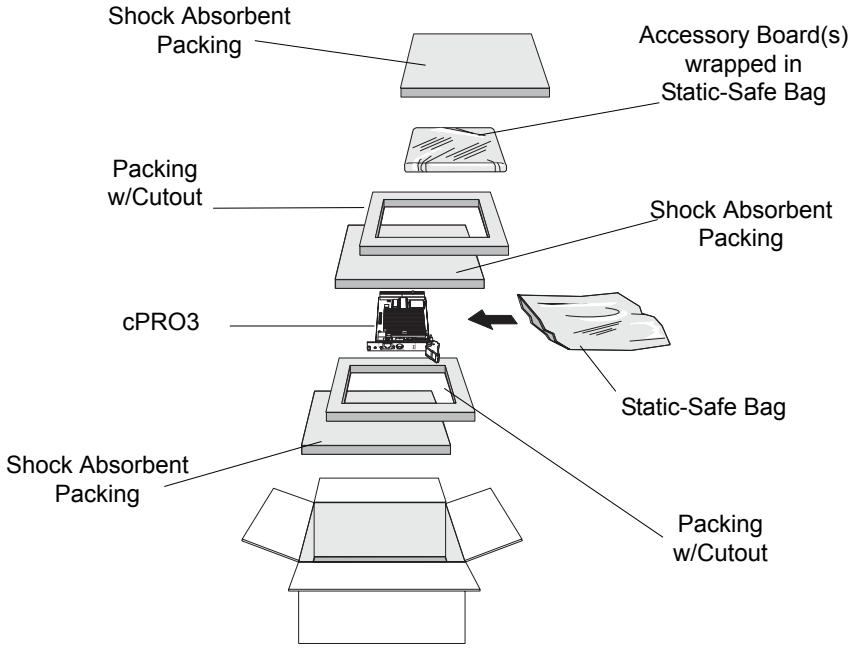
You should wear a properly-functioning antistatic strap and ensure you are fully grounded. Any surface upon which you place the unprotected cPRO3 should be static-safe, usually facilitated by the use of antistatic mats. From the time the board is removed from the antistatic bag until it is in its card cage and functioning properly, extreme care should be taken to avoid “zapping” the board with ESD. You should be aware that you could “zap” the board without your knowing it; a small discharge, imperceptible to the eye and touch, is enough to damage electronic components. Extra caution should be taken in cold and dry weather when static easily builds up.

Unpacking and Handling

The cPRO3 has been carefully packaged to ensure adequate protection from the rigors of shipping. However, the possibility exists that shipping damage can occur. Close inspection of the shipping carton should reveal some information about how the package was handled by the shipping service. If evidence of damage or excessively rough handling is found, you should notify the shipping service and SBS Embedded Computers as soon as possible.

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Only after ensuring that both you and the surrounding area are protected from ESD, carefully remove the cPRO3 from the shipping carton. Place the board, in its anti-static bag, flat down on a suitable surface. You may then remove the board from the anti-static bag by tearing the ESD warning labels. Again place the board flat down on the work surface.



Retain all packing materials in case of future need for storage, relocation or the possibility of return for repairs.

Initial Inspection

Once the cPRO3 has been unpacked, it is suggested you inspect it for visible damage which could have occurred during shipping or unpacking. If there is visible damage, usually in the form of bent component leads or loose socketed components, contact SBS Embedded Computers for additional instructions. Depending on the severity of the damage, it may need to be sent back to the factory to be repaired. DO NOT apply power to the board if it has visible damage. Doing so may cause further, possibly irreparable damage, as well as introduce a fire or shock hazard. Since the cPRO3 may incorporate a number of socketed components, including the CPU, these should be inspected to make sure that they are seated fully in their sockets.

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Included Items

Table 2-1 lists accessories which are included with each cPRO3. You may want to make sure that you have the items shown in the event that you need them during installation or configuration.

Qty.	Item	Purpose
1	Cable Adapter	PC Keyboard Adapter
1	Kbd/Mouse "Y" Adapter	Allows simultaneous connection and operation keyboard and Mouse.

Table 2-1 Included Items

Minimum System Requirements

As shipped, the cPRO3 has been thoroughly tested and burned-in, and is nearly ready for use in your system. In order to verify cPRO3 operation for the first time, it is suggested that you only configure a minimal system. It is not necessary to have disk drives or other accessories connected in order to perform the cPRO3 confidence tests. The following items are all that are required:

Power Supply

You will need a standard CompactPCI backplane wired into a regulated power supply capable of providing stable low noise +5 volt and +3.3 volt sources. The standard CompactPCI backplane also provides +12 volt and -12 volt sources, but they are not used by the cPRO3. Make sure that the supply is capable of meeting the total power requirements of the cPRO3. Please refer to chapter 7 for the cPRO3 Specifications. Initially, you may plug the cPRO3 into any available 3U slot of your CompactPCI backplane. Later you will need to select the proper slot for your particular application. Please make sure that you do not have the power supply turned ON when the cPRO3 is plugged into your backplane.

> ***As a reminder, you must never install or remove any computer card while power is applied unless it is certified for hot-insertion (the cPRO3 is not).***

Keyboard and Mouse

You should have an IBM PC/AT or compatible keyboard for initial system operation. Depending on your application, this keyboard may be a standard full-travel keyboard, or one which utilizes membrane switches for harsh environments. Note that some keyboards have a switch which selects either PC and PC/XT compatibility or PC/AT compatibility. If your keyboard is equipped with such a switch, make sure it is set for PC/AT compatibility. The miniature DIN keyboard connector is located on the front and is directly compatible with IBM PS2-type keyboards. If your keyboard has the normal IBM PC-type keyboard connector you will need to use the supplied cable adapter.

NOTE: The cPRO3 has a single connector defined for both the keyboard and mouse. The definition is such that without an SBS adapter, only the keyboard is available. With the SBS adapter, keyboard and mouse port access are provided.

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Plug your adapter into the keyed front panel connector labeled 'KBD/MSE', then plug the keyboard and mouse into the adapter before power is applied. Plugging and unplugging the keyboard while power is applied is not recommended and can cause a software failure or damage to the keyboard or the onboard circuitry.

NOTE:

The SBS "Y" Adapter is marked reverse of the standard IBM laptop "Y" Adapter.

Initial Power-On Operation

Since the cPRO3 is designed without excessive overhead, there is no onboard video driver. In order to provide visual indication of BIOS operation, particularly for verification of initial operation "out-of-the-carton", ASCII video is provided through the COM2 port of the cPRO3. This ASCII video can be viewed with any VT220 compliant terminal. The serial settings are 9600 Baud, 8 bit, 1 Stop bit, and No Parity. The text will display the results of the initial BIOS operation and enable setting up the BIOS for individual preferences. A cPCI video card may be purchased and plugged into one of the slots on the CompactPCI backplane to provide full video and graphic output display.

With Video

A few seconds after power is applied, the cPRO3 System Award BIOS banner information will be displayed.

The memory test will begin. From the factory, the board is configured to do a very thorough memory test. As such, the test will proceed slowly. Once you have configured your board for the first time, the board will execute a much faster memory test on subsequent startups.

If you have seen all the messages to this point, you can be confident that the board is running properly and is ready to be installed and setup for your application. You may now shut off power to the board and begin setup and configuration as described in Chapter 3.

If the board did not perform as described above, some damage may have occurred in shipping or the board is not installed or setup properly. Contact SBS technical support as described in Chapter 8 for further instructions.

Without Video

Allow up to 120 seconds for the board to perform its initial power-on sequence of tests. VT100 display will begin just before the system configuration banners are posted.

Text only interface is provided. Currently, the VT100 keyboard function is disabled and keyboard I/O must be accomplished through the cPRO3 front panel.

Special Note:
Holding the <ALT> key down during the power-on sequence will cause the system to switch to VT-100 mode and disable video.

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CHAPTER 3 Installation and Interfacing

Chapter Scope

This chapter covers installing the cPRO3 in a computer system and interfacing the cPRO3 to external devices and peripherals.

Installation Requirements

The following paragraphs describe requirements which your system must meet in order to install and successfully integrate the cPRO3. If you are uncertain about any requirements, be sure to contact SBS Embedded Computers Technical Support before installing your cPRO3.

Power Requirements

cPRO3 Power Requirements

Power is supplied to the cPRO3 via the CompactPCI P1 connector as shown in Table 3-1. USB Power and USB Ground, as well as additional V(IO) and Ground are supplied through P2 as shown in table 3-2.

Signal	Location on CompactPCI P1
+5 Volts	Row A; Pins 1 and 25
	Row B; Pins 2 and 24
	Row D; Pins 3 and 23
	Row E; Pins 1 and 25
+3.3 Volts	Row A; Pins 15,17,19,21, and 23
	Row C; Pins 6,10,18 and 22
	Row D; Pin 25
Ground	Row B; Pins 4, 6, 8, 10, 16, 18, 20 and 22
	Row D; Pins 5, 7, 9, 11, 15, 17, 19 and 21
V(IO)	Row C; Pins 4, 8, 16, 20 and 24

Table 3-1 P1 Connector Pins

Signal	Location on CompactPCI P2
V(IO)	Row A; Pin 4
	Row C; Pins 5, 7, 9, 11 and 13
Ground	Row A; Pin 19
	Row B; Pins 1,3,5,7,9,11,13,15,17,19,20 and 21
	Row D; Pins 4,6,8,10,12,14,16 and 20
USB +5 Volts	Row C; Pin 14
USB Ground	Row C; Pin 17

Table 3-2 P2 Connector Pins

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Cooling Requirements

The cPRO3 integrates a large number of high-performance components in the small space of a single card. These components generate a lot of heat. To prevent damage to the board and to ensure reliable operation, the cPRO3 MUST be cooled with forced air. A 100LFM fan is recommended.

Interfacing the cPRO3 to External Devices

Front panel connectors, onboard connector J4 and the backplane connector of the cPRO3 are used to establish an electrical interconnection to external devices. The normal PC keyboard/mouse and Ethernet connectors are provided on the front of the board. COM1, COM2, parallel port, Ethernet and USB port connections are provided via the backplane connector. These features may be easily accessed through an optional TB-cPRO3 board which plugs onto the other side of the backplane connector. In addition, the COM-2 port has jumper selectable RS-422 and RS-485 modes.

Keyboard / Mouse Interface

The keyboard/mouse interface consists of six electrical connections provided on a 6-pin circular mini-DIN connector (PS/2-style). Two connections are for communication between the keyboard and the keyboard interface port. Two similar connections are for communication between the mouse and the mouse interface port. All four of these signals are CMOS compatible. The two remaining connections provide power for the mouse and keyboard's operation. The keyboard/mouse connector with pin assignments as viewed from the front of the cPRO3 are shown in Figure 3-1. Keyboard/mouse signal definitions are given in Table 3-3.

A keyboard alone will work plugged into the keyboard/mouse connector, but a mouse alone will not function. The mouse operation requires a mini-DIN "Y" adapter, supplied with the cPRO3. The bottom part of the "Y" connects to the cPRO3 keyboard/mouse port with two sections splitting to form a separate keyboard and mouse connecting point.

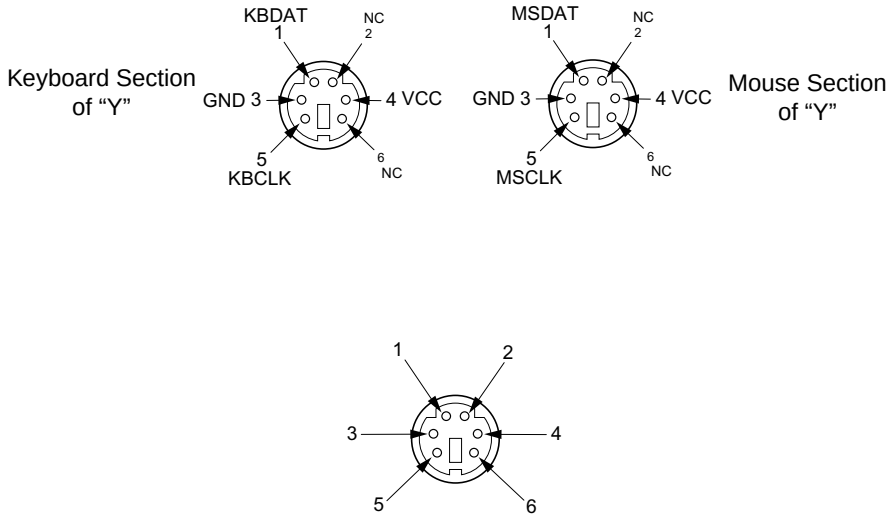


Figure 3-1 Mouse / Keyboard Interface

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Pin	Signal	Function
1	KBDAT	Bidirectional serial data to/from keyboard
2	MSDAT	Bidirectional serial data to/from mouse
3	GND	Digital Ground (0 volt) reference to keyboard
4	VCC	+5 volt power to the keyboard
5	KBCLK	Bidirectional data clock to/from keyboard
6	MSCLK	Bidirectional data clock to/from mouse

Table 3-3 Keyboard / Mouse Interface Signals

This connector accepts any manufacturer's keyboard which is designed with a standard PC/AT interface; however, a PC/AT to PS/2 adapter is required. Such an adapter is supplied with the board. Note that many keyboard manufacturers provide keyboards which will work with either the IBM PC or PC/AT. Most of these have a switch which the user must set to match the type of computer that its used with. For the cPRO3, make sure that the switch is set for PC/AT operation, not for PC or PC/XT operation.

When plugging a keyboard into the cPRO3 keyboard connector, it is recommended that the system power be switched OFF. Plugging a keyboard into a powered-up system may cause improper initialization of the keyboard. If there is a static charge on the keyboard, it may cause damage to the cPRO3 keyboard controller circuitry or to the keyboard circuitry itself.

Serial Ports

The cPRO3 is equipped with two serial ports (COM1 and COM2) which are provided through the backplane J2 connector at TTL levels. If the TB-cPRO3 option board is used, the signals are defined for industry standard interfacing using RS-232 compatible signal levels. See Chapter 7, "Option Board Accessories", for more information on the COM ports.

Parallel Port

The cPRO3 parallel port is available through the backplane, or if the TB-cPRO3 option board is used, by a labled 26 pin connector. In its normal operating mode, the port functions exactly as does a standard IBM PC parallel printer port. In this mode of operation, it will interface with printers using the industry standard Centronics parallel interface. Figure 3-2 indicates the TB-cPRO3 connector pins and signals are defined in Table 3-7.

Operation of the printer port is accomplished with routines built into the ROM BIOS supplied with the cPRO3. Therefore, standard MS-DOS printer functions will work with a printer attached as the "PRN" device.

Under software control, the parallel port supports optional PS/2 type bidirectional parallel port (SPP), Enhanced Parallel Port (EPP), and Extended Capabilities Port (ECP) modes.

The cPRO3 has two USB ports (designated USB1 and USB2) available through the backplane, or if the TB-cPRO3 Option Board is used, through a 10-Pin labled connector. Refer to Chapter 7 for additional information on the USB Ports.

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Ethernet Interface

The Pro3 contains a high performance DEChip 21143 Ethernet controller, and comes with a Twisted Pair (10/100BaseT) interface with an RJ45 connector through the front panel. Ethernet is also provided through the backplane J2. Table 3-11 shows the pin assignments for the RJ45.

Pin	Signal
1	Transmit Data Positive
2	Transmit Data negative
3	Receive Data Positive
4	No connection
5	No connection
6	Receive Data Negative
7	No connection
8	No connection

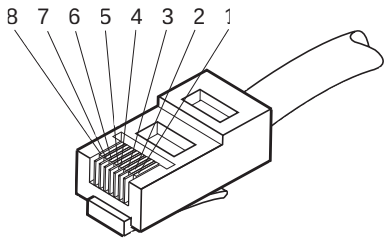


Table 3-4 Ethernet, 10/100BaseT, RJ45 Pin Assignments

IDE Interface

The cPRO3 IDE interface connection is through connector J4, or the Transition Board (TB-IDE) if used. Like the USB capability, the IDE is a PCI slave facilitated by the M1543 chip. The IDE interface supports Ultra 33 Synchronus DMA mode (up to 33Mbytes/sec transfers). The user must supply a 40-pin ribbon cable with mating connectors to connect the IDE interface to an IDE drive. See Section 7, Option Board Accessories, for additional information the IDE Interface. Page 3-6 shows the Pin-outs for connector J4.

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Pin	Row A	Row B	Row C	Row D	Row E	
22	UD1	UD6	UD13	UD15	UD17	P2 / J2 Connector
21	CLK6	GND13	ETHTXF+	ETHTXF-	ETHR45	
20	CLK5	GND11	UD12	GND22	ETHR78	
19	GND1	GND12	UD11	ETHRXF+	ETHRXF-	
18	LPT-STP	LPT-PE	UD10	UD14	UD16	
17	LPT-AFD	GND10	USB GND	REQ6-	GNT6-	
16	LPT-D0	LPT-ACK	USB1D+	GND21	UBAT	
15	LPT-ERR	GND9	USB1D-	REQ5-	GNT5-	
14	LPT-D1	LPT-SLCT	USB VCC	GND20	RI1	
13	LPT-INIT	GND8	VIOB	DTR1	CTS1	
12	LPT-D2	UD5	USB2D+	GND19	TXD1	
11	LPT-SLIN	GND7	VIO5	RTS1	RXD1	
10	LPT-D3	UD4	USB2D-	GND18	DSR1	
9	LPT-D4	GND6	VIO4	DCD1	R12	
8	LPT-D5	UD3	FDENSEL	GND17	DTR2	
7	LPT-BUSY	GND5	VIO3	CTS2	TXD2	
6	LPT-D6	UD2	UD9	GND16	RTS2	
5	LPT-D7	GND4	VIO2	RXD2	DSR2	
4	VIO1	STCLK-	UD8	GND15	DCD2	
3	CLK4	GND3	GNT3-	REQ4-	GNT4-	
2	CLK2	CLK3	UD7	GNT2-	REQ3-	
1	CLK1	GND2	REQ1-	GNT1-	REQ2-	
25	5V2	REQ64-	ENUM-	3.3V10	5V8	P1 / J1 Connector
24	AD01	5V4	VIO5	AD00	ACK64-	
23	3.3V5	AD04	AD03	5V6	AD02	
22	AD07	GND8	3.3V9	AD06	AD05	
21	3.3V4	AD09	AD08	M66EN/GND	CBE0-	
20	AD12	GND7	VIO4	AD11	AD10	
19	3.3V3	AD15	AD14	GND15	AD13	
18	SERR	GND6	3.3V8	PAR	CBE1-	
17	3.3V2	SDONE	SBO-	GND14	PERR-	
16	DEVSEL	GND5	VIO3	STOP-	LOCK-	
15	3.3V1	FRAME-	IRDY-	GND13	TRDY-	
12-14			Key Area			
11	AD18	AD17	AD16	GND12	CBE2-	
10	AD21	GND4	3.3V7	AD20	AD19	
9	CBE3	IDSEL	AD23	GND11	AD22	
8	AD2B	GND3	VIO2	AD25	AD24	
7	AD3D	AD29	AD28	GND10	AD27	
6	REQ-	GND2	3.3V6	CLK	AD31	
5	BRSRVA5	BRSRVB5	RST-	GND9	GNT-	
4	BRSRVA4	GND1	VIO1	INTP	INTS	
3	INTA-	INTB-	INTC-	5V5	INTD-	
2	TCK	5V3	TMS	TD0	TD1	
1	5V1	-12V	TRST-	+12v	5V7	

Table 3-5 Compact PCI J1/J2 Connectors

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Pin	Pin Name	Type	Description
1	PIDE07	2	+5V
3	+5V	4	PIDE15
5	PIDE06	6	+5V
7	+5V	8	PIDE14
9	PIDE05	10	+5V
11	+5V	12	PIDE13
13	PIDE04	14	+5V
15	GND	16	PIDE12
17	PIDE03	18	GND
19	GND	20	PIDE11
21	PIDE02	22	GND
23	GND	24	PIDE10
25	PIDE01	26	GND
27	GND	28	PIDE09
29	PIDE00	30	GND
31	GND	32	PIDE08
33	RSTDRV-	34	PIDECS0-
35	PIDE10W-	36	PIDECS1-
37	PHDMRO	38	PIDEA0
39	PIDE10R-	40	PIDEA1
41	PHDIORDY	42	PIDEA2
43	PIDEDMACK	44	PIDEIRQ
45	FMT0-	46	FWP-
47	FMT1-	48	FWE-
49	FSTEP-	50	FDENSEL-
51	FDS1-	52	FHS-
53	FDS2-	54	FDSKCHG-
55	FINDEX-	56	FRD-
57	FDIRC-	58	GND
59	FTK0-	60	FWD-

Table 3-6 J4 Connector Signals

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CHAPTER 4 Booting and Operation

Starting Setup

This section describes the Award Software BIOS Setup program. The Setup program allows you to modify basic system configuration settings. The settings are stored in a dedicated battery-backed memory, called CMOS RAM, that retains the information when the power is turned off.

The Award Software BIOS is immediately activated when you first turn on the computer. The BIOS reads system configuration information in CMOS RAM and begins the process of checking out the system and configuring it through the Power-On Self Test (POST). The BIOS then seeks an operating system on one of the data storage devices (hard drive, floppy drive, etc.). The BIOS launches the operating system and hands control of system operations to it. You can enter the Setup program by pressing <DEL> immediately after switching the system on.

In Case of Problems

If you should discover that your computer is no longer able to boot after making and saving system changes with Setup, the BIOS supports an override to the CMOS settings that resets your system to its default configuration. You can invoke this override by immediately pressing Insert when you restart your computer. You can restart by either using the ON/OFF switch, the RESET button, or by pressing Ctrl-Alt-Del.

It is recommended that you only alter settings that you thoroughly understand. Especially do not change settings in the Chipset screen without a good reason. The Chipset defaults were carefully chosen by Award Software and SBS Embedded Computers for best performance and reliability. Even an apparently insignificant change to the Chipset setup may cause the system to become unstable.

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Setup Key Commands

The following keys may be used to operate the Setup program:

Arrow Keys	The arrow keys are used to move around the Setup screen. The up and down arrows move you through the previous and the next options respectively. The right arrow moves the cursor into the right side of the screen. The left arrow moves the cursor into the left side of the screen.
ESC	In the Main Menu, pressing the escape key exits the Setup program without saving changes. In other screens, it will exit current page and return to main menu.
PgUp or +	Increase the numeric value, or make changes.
PgDn or **-**	Decrease the numeric value, or make changes.
F1	General help only for Status page and Option page Setup Menu.
F2	Change color from total 16 colors. F2 to select Shift-F2 color forward, Shift-F2 color backward.
F5	Restores the previous CMOS value from CMOS, only for Option Page Setup Menu..
F6	Loads Default BIOS values. (Option Page Setup Menu)
F7	Loads Default Test Setup values.
F10	Saves all CMOS changes. (Main Menu only)

Main Setup Menu

```
ROM PCI/ISA BIOS (2A5KFU80)
CMOS SETUP UTILITY
AWARD SOFTWARE, INC.
```

```
STANDARD CMOS SETUP              INTEGRATED PERIPHERALS
BIOS FEATURES SETUP              SUPERVISOR PASSWORD
CHIPSET FEATURES SETUP           USER PASSWORD
POWER MANAGEMENT SETUP           IDE HDD AUTO DETECTION
PNP/PCI CONFIGURATION            SAVE & EXIT SETUP
LOAD SETUP DEFAULTS              EXIT WITHOUT SAVING

ESC  :  Quit                     ←↑→↓ Move      :   Select Item
F10  :  Save & Exit Setup        (Shift) F2     :   Change Color

                Description of Selected Function above
```


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Standard CMOS	Options in the original PC AT compatible BIOS.
BIOS features	Award Software enhanced BIOS features.
Chipset Features	Options specific to your system chipset.
Power Management	Advanced Power management (APM) options.
PNP/PCI Configuration	Local bus configuration options.
Load Setup Defaults	Factory settings for optimal performance of system operations.
Integrated Peripherals	Settings for HDD, controllers, serial ports and other peripheral devices.
Password Setting	Change, set, or disable a password. Only the supervisor password allows access to Setup. The User password only allows power-on access.
IDD Auto Detection	Automatically detect and configure IDE hard disk parameters.
Save and Exit Setup	Save settings in non-volatile CMOS RAM and exit Setup.
Exit Without Save	Abandon all changes and exit Setup.

The following screens detail additional options available with the respective selections from the Main Menu screen.

Standard CMOS Setup

```
                ROM PCI/ISA BIOS (2A5KFU80)
                  STANDARD CMOS SETUP
                AWARD SOFTWARE, INC.

Date  (mm:dd:yy)  : Fri, Aug 7 1998
Time  (hh:mm:ss)  : 11:10:26

Hard Disks         TYPE   SIZE  CYLS  HEAD   PRECOMP LANDZ  SECTOR  MODE

Primary Master    : AUTO   0     0     0      0       0      0       Auto
Primary Slave     : AUTO   0     0     0      0       0      0       Auto
Secondary Master  : AUTO   0     0     0      0       0      0       Auto
Secondary Slave   : AUTO   0     0     0      0       0      0       Auto

Drive A             : 1.44M, 3.5 in.
Drive B             : None
Floppy 3 Mode Support : Disabled

Video   : EGA/VGA
HaltOn  : All, But Keyboard

Base Memory       :  640K
Extended Memory   :  31,744K
Other Memory      :  384K

Total memory      :  32,768K

ESC : Quit               ←↑→↓ Move  : Select Item     PU/PD/+/- : Modify
F10 : Save & Exit Setup   (Shift) F2 : Change Color
```


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Date This field is for information only.

Time Time format is based on the 24-hour military clock. For example, 1 pm is 13:00. Pres right or left arrow to to move to desired fileds. Press PgUp or PgDn to increment the setting, or type in the desired value.

Hard Disks The BIOS supports up to four IDE drives. This section does not show information about other IDE drives, such as a CD ROM drive, or other hard drive types, such as SCSI drives. It is recommended that you select type AUTO for all drives. The BIOS cna automatically detect the specifications and optimal mode for almost all IDE hard drives. When you select type AUTO for a hard drive, the BIOS detects its specifications during POST, each time the system boots. If you do not want to select type AUTO here, you may do one of the following:

1.) Match the specifications of your IDE hard drive(s) with the preprogrammed values for types 1 thru 45.
2.) Select USER and enter values directly into each drive parameter field.
3.) Use the IDE HDD Auto Detection funtion in Setup.

Drive A, Drive B Select the correct specifications for the diskette drive(s) installed in your system.

Video Select the type of primary video subsytem in your computer. The BIOS usually detects the correct video type automatically.

Halt ON During the power-on self-test (POST), the computer stops if the BIOS detects a hardware error. You can tell the BIOS to ignore certain errors during POST and continue the boot process. These error selections are:

No Errors POST does not stop for any errors.

All Errors If the BIOS detects any non-fatal errors, POST stops and prompts you to take corrective action.

All But Keyboard POST does not stop for a keyboard error, but stops for all other errors.

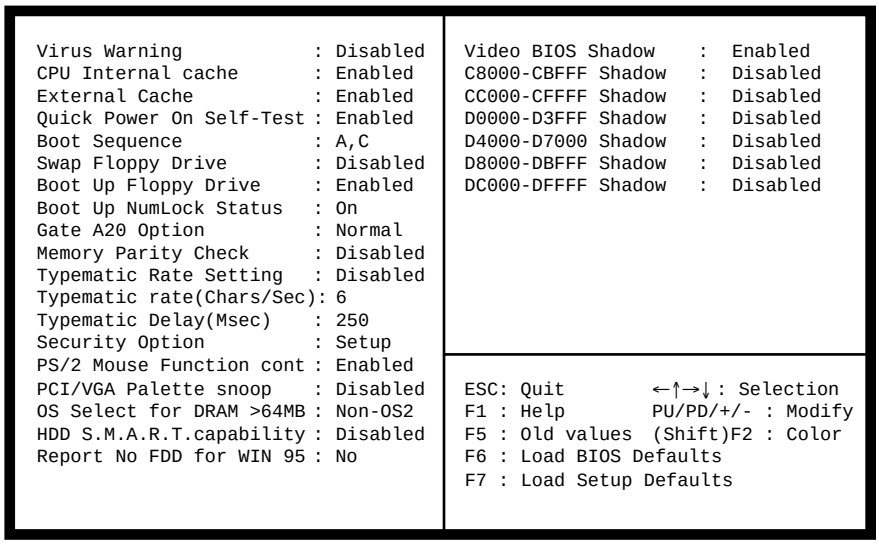
All But Diskette POST does not stop for diskette drive errors, but stops for all other errors.

All But Disk/Key POST does not stop for a keyboard or disk error, but stops for all other errors.

Memory You cannot change any values in the Memory fields. They are there for information only.

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BIOS Features Setup



Virus Warning

When enabled, you receive a warning message if a program (specifically, a virus) attempts to write to the boot sector or the partition table of the hard disk drive. You should then run an anti-virus program. This only protects the boot sector, not the entire hard drive.
NOTE: *Many disk diagnostic programs that access the boot sector table can trigger the virus warning message. If you plan to run such a program, it is recommended that you disable the virus warning first.*

CPU Internal Cache /External Cache

Cache memory is additional memory that is much faster than conventional DRAM (system memory). When the CPU requests data, the system transfers the requested data from the main DRAM into cache memory, for even faster access by the CPU.

Quick Power On Self-Test

Select enabled to to reduce the amount of time required to run the power-on self-test (POST). A quick POST skips certain steps. It is recommended that you normally disable Quick POST. It is better to find a problem during POST than lose data during your work.

Boot Sequence

The original IBM PCs loaded the DOS fromdrive A (floppy disk), so IBM PC-compatible systems are designed to search for an operating system first on drive A, and then on drive C (hard disk). Most modern computers load the operating system from the hard drive, and may even load it from a CD ROM drive. The options are: A,C C,A C,CDROM,A CDROM,A,A C only, LS120,C

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Swap Floppy Drive	This field is effective only in systems with two floppy drives. Selecting ENABLED assigns physical drive B to logical drive A, and physical drive A to to logical drive B.
Boot Up Floppy Seek	When enabled, the BIOS tests (seeks) floppy drives to determine whether they have 40 or 80 tracks. Only 360k drives have 40 tracks. 720k, 1.2M, and 1.44M drives all have 80 tracks. Because very few modern PCs have 40-track drives, it is recommended that you set this field to DISABLED to save time.
Boot Up NumLock Status	Toggle between ON and OFF to control the state of the NumLock key when the system boots. When toggled On, the numeric keypad generates numbers instead of controlling cursor operations.
Gate A20 Option	Gate A20 refers to the way the system addresses memory above 1 MB (extended memory). When set to FAST, the system chipset controls Gate A20. When set to NORMAL, a pin in the keyboard controller controls Gate A20. FAST improves system speed.
Typematic Rate Setting	When DISABLED, Typematic Rate and Typematic Delay are irrelevant. Keyboard repeats at a rate determined by the keyboard controller in your system. When this is ENABLED, you can select Typmatic Rate and Delay.
Typematic Rate (Chars/Sec)	When the Typematic Rate setting is ENABLED, you can select a typematic rate (the rate at which a character repeats when you hold down a key) of 6, 8, 10, 12, 15, 20, 24,or 30 characters per second.
Typematic Delay (msec)	When the Typematic Rate setting is ENABLED, you can select a typematic delay (the delay before key strokes begin to repeat)of 250, 500, 750, or 1000 milliseconds.
Security Option	If you have set a Password, select whether the password is required every time the System boots, or only when you enter Setup.
PS/2 Mouse Function Control	Enables or Disables PS/2 Mouse function control.
PCI/VGA Palette Snoop	If present, leave this field DISABLED.
OS/2 Select for DRAM >64MB	Options are OS/2 or NON OS/2
HDD S.M.A.R.T. Capability	Options are ENABLED or DISABLED.
Report No FDD For WIN 95	Select YES to release IRQ6 when system contains no floppy drive, for compatibility with Windows 95 logo certification. In the Integrated Peripherals screen, select DISABLED for the Onboard FDC Controller field.

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Shadow

Software residing in a Read-Only Memory (ROM) is called Firmware. The Award Software BIOS permits *Shadowing* of firmware such as system BIOS, video BIOS and similar operating instructions that come with some expansion peripherals such as a SCSI adapter. Shadowing copies from ROM into system RAM, where the CPU can read it through the 16-bit or 32-bit DRAM bus. Firmware not shadowed must be read by the system through the 8-bit X-bus. Shadowing improves the performance of the system BIOS and similar ROM firmware for expansion peripherals, but it also reduces the amount of high memory (640kb to 1Mb) available for loading device drivers, etc.

ENABLE shadowing into each section of memory separately.

Video BIOS shadows into memory area C0000-C7FFF. The remaining areas shown on the BIOS features Setup screen may be occupied by other expansion card firmware. If an expansion peripheral in your system contains ROM-based firmware, you need to know the address range the ROM occupies to shadow it into the correct of RAM.

Chipset Features Setup

```
ROM PCI/ISA BIOS (2A5KFU80)
CHIPSET FEATURES SETUP
AWARD SOFTWARE, INC.
```

Auto Configuration	: Enabled	Passive Release	: Enabled
AT Bus Clock	: CLK2/4	ISA Line Buffer	: Enabled
DRAM Write WS	: X-2-2-2	Delay Transaction	: Disabled
Page Mode Read WS	: X-2-2-2		
RAS Precharge Period	: 3T		
Ras-To-CAS Delay Time	: 3T		
EDO Read WS	: X-2-2-2		
DRAM Speculative Read	: Disabled		
SDRAM CAS Latency	: 3		
SDRAM Access Timing	: 3-4-7		
SDRAM Speculative Read	: Disabled		
Pipelined Function	: Enabled		
DRAM refresh Period (us)	: 60		
DRAM Data Integrity Mode	: Disabled		
Memory Hole At 15-16M	: Disabled		
Primary Frame Buffer	: 2 Mb	ESC: Quit	←↑→↓ : Selection
VGA Frame Buffer	: Enabled	F1 : Help	PU/PD/+/- : Modify
Data Merge	: Disabled	F5 : Old values	(Shift)F2 : Color
Byte Merge	: Disabled	F6 : Load BIOS Defaults	
Fast Back-to-Back	: Disabled	F7 : Load Setup Defaults	

The parameters in this screen are for system designers, service personnel and technically competent users only. Do not reset these values unless you understand the consequences of your changes.

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Auto Configuration	Auto configuration selects predetermined optimal values of chipset parameters. When DISABLED, chipset parameters revert to setup information stored in CMOS. Many fields in this screen are not available when Auto Configuration is ENABLED.
AT-BUS Clock	You can set the speed of the AT bus in terms of a fraction of the CPU clock speed, or at the fixed speed of 7.16MHz.
DRAM Write Wait State	The system board designer may elect to insert a wait state into the DRAM write cycle, if necessary. The options are X-2-2-2, X-3-3-3
Page Mode Read Wait State	Select the correct cycle timing combination for the system board design and Page Mode DRAM specifications. Options are X-3-3-3, X-4-4-4
RAS Precharge Period	The RAS Precharge time is the number of cycles it takes for the RAS to accumulate its charge before the DRAM refresh. If sufficient time is allowed, refresh may be incomplete and the DRAM may fail to retain data. Options are: 3T and 4T.
RAS To CAS Delay Time	When DRAM is refreshed, both rows and columns are addressed separately. This setup item allows you to determine the timing of the transition from Row Address Strobe (RAS) to Column Address Strobe (CAS).
EDO Read WS	Select the correct timing cycle combination for the system board design and EDO RAM specifications.
DRAM Speculative Read	The Chipset can "speculate" on a DRAM read address thus reducing read latencies. The CPU issues a read request containing the data memory address. The DRAM controller receives the request. When this field is ENABLED, the controller issues the read command slightly before it has finished decoding the data address.
SDRAM CAS Latency	When synchronus DRAM is installed, the number of clock cycles of CAS latency depends on the DRAM timing. ***DO NOT reset this field from the default value specified by the system designer.***
SDRAM Access Timing	*DO NOT reset this field from the default value specified by the system designer.*
SDRAM Speculative Read	This function is the same as DRAM Speculative Read but is used for Synchronus DRAM.
Pipelined Function	When ENABLED, the controller signals the CPU for a new memory address before all data transfers for the current cycles are complete, resulting in faster performance. Options are ENABLED, DISABLED and TURBO..

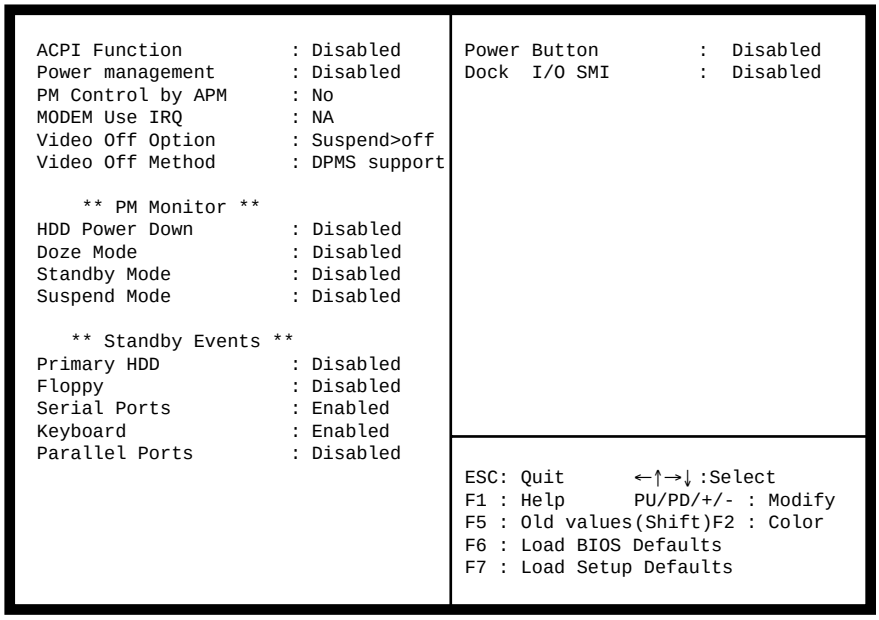
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DRAM Refresh Period (us)	Select the period required to refresh the DRAMs, according to DRAM specifications. Options are 15, 30, 60, 120, 256.
DRAM Data Integrity Mode	Select PARITY or DISABLED according to the type of installed DRAM.
Memory Hole At 15-16M	You can reserve this area of system memory for ISA adapter ROM. When this area is reserved it cannot be cached. The user information of peripherals that need to use this area of system memory usually discusses their memory requirements.
Primary Frame Buffer	Select a size for the Primary Frame Buffer. The size of the buffer should not impinge on local memory.
VGA Frame Buffer	When ENABLED, a fixed VGA Frame Buffer from A000h to BFFFh and a CPU-to-PCI write buffer are implemented.
Data Merge	ENABLES, or DISABLES data merging.
Byte Merge	This field controls the byte-merge feature for frame buffer cycles. When ENABLED, the controller checks the eight CPU Byte Enable signals to determine if data bytes read from the PCI bus by the CPU can be merged.
Fast Back-To-Back	When ENABLED, consecutive write cycles targeted to the same slave become fast back-to-back on the PCI bus.
Passive Release	When ENABLED, CPU to PCI bus accesses are allowed during passive release. Otherwise, the arbiter only accepts another PCI master access to local DRAM.
ISA Line Buffer	The PCI to ISA bridge has an 8-byte bidirectional line buffer for ISA or DMA bus master memory reads from or writes to the PCI bus. When ENABLED, an ISA or DMA bus master can preftech two doublewords to the line buffer for a read cycle.
Delay Transaction	The Chipset has an embedded 32-bit posted write buffer to support delay transaction cycles. Select ENABLED to support compliance with PCI specification version 2.1.

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Power Management

```
ROM PCI/ISA BIOS (2A5KFU80)
POWER MANAGEMENT SETUP
AWARD SOFTWARE, INC.
```



ACPI Function Always leave DISABLED. Selecting ENABLED allows ACPI device node reporting from the BIOS to the operating system.

Power Management Leave DISABLED. Power management capability is either ENABLED or DISABLED with this option.

PM Control By APM Always leave selection as NO. Selection of YES is for the Advanced Power Management (APM) function, not supported by the cPRO3.

MODEM Use Option This is Not Applicable to the cPRO3.

Video OFF Option Select the power saving modes during which the monitor goes blank. Options are:
ALWAYS ON
SUSPEND-->OFF (monitor blanked when system enters suspend mode)
SUSP,STBY-->OFF (monitor blanked when system enters suspend mode)
ALL MODES OFF (monitor blanked when system enters any power saving mode)

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Video Off Method	Determines the manner in which the monitor is blanked. V/H SYNC+BLANK (System turns off vertical and horizontal synchronization ports and writes blanks to the video buffer. DPMS SUPPORT (Select this option if your monitor supports the Display Power Management Signaling (DPMS) standard of the Video Electronics Standards Association (VESA). Use the software supplied for your video subsystem to select video power management values.) BLANK SCREEN (System only writes to the video buffer.)
**** PM Monitor ****	
HDD Power Down	After the selected period of inactivity, the hard disk drive powers down while all other devices remain active. Control of this mode is independent of the power management mode selected previously.
Doze Mode	After the selected period of system inactivity, the CPU clock runs at slower speed while all other devices still operate at full speed.
Standby Mode	After the selected period of system inactivity, the the fixed disk drive and the video shut off while all other devices still operate at full speed.
Suspend Mode	After the selected period of system inactivity, all devices except the CPU shut off.
**** Standby Events ****	
	You may disable activity monitoring of some common I/O events and interrupt requests so they do not wake up the system. The default wake-up event is keyboard activity. When ENABLED, any activity from one of the system peripheral devices listed below wakes up the system. Primary HDD, Floppy, Serial Ports, Keyboard , or parallel Ports.
Power Button	Always leave this function DISABLED.
Dock I/O SMI	Always leave this function DISABLED.

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PnP/PCI Configuration

```
ROM PCI/ISA BIOS (2A5KFU80)
PNP/PCI CONFIGURATION
AWARD SOFTWARE, INC.
```

```
PnP Installed             : No          PCI IDE 2nd Channel  :  Disabled
Resources Controlled by   : Auto        PCI IRQ Activated by :  Level
Reset Configuration Date  : Disabled    PCI IDE IRQ Map to   :  ISA
```

```
ESC: Quit      ←↑→↓ :Select
F1 : Help      PU/PD/+/- : Modify
F5 : Old values(Shift)F2 : Color
F6 : Load BIOS Defaults
F7 : Load Setup Defaults
```

PnP OS Installed Select YES if the system operating environment is Plug and Play aware.

```
PnP Installed             : No          PCI IDE 2nd Channel  :  Disabled
Resources Controlled by :Manual         PCI IRQ Activated by :  Level
Reset Configuration Data:Disabled       PCI IDE IRQ Map to   :  ISA

IRQ-3 Assigned To       :Disabled
IRQ-4 Assigned To       :PCI/ISA PnP
IRQ-5 Assigned To       :PCI/ISA PnP
IRQ-7 Assigned To       :PCI/ISA PnP
IRQ-9 Assigned To       :PCI/ISA PnP
IRQ-10 Assigned To      :PCI/ISA PnP
IRQ-11 Assigned To      :PCI/ISA PnP
IRQ-12 Assigned To      :PCI/ISA PnP
IRQ-14 Assigned To      :PCI/ISA PnP
IRQ-15 Assigned To      :PCI/ISA PnP
DMA-0 Assigned To       :PCI/ISA PnP
DMA-1 Assigned To       :PCI/ISA PnP
DMA-2 Assigned To       :PCI/ISA PnP
DMA-3 Assigned To       :PCI/ISA PnP
DMA-4 Assigned To       :PCI/ISA PnP
DMA-5 Assigned To       :PCI/ISA PnP
DMA-6 Assigned To       :PCI/ISA PnP
DMA-7 Assigned To       :PCI/ISA PnP
```

```
ESC: Quit        ←↑→↓ :Select
F1 : Help        PU/PD/+/- : Modify
F5 : Old values  (Shift)F2 : Color
F6 : Load BIOS Defaults
F7 : Load Setup Defaults
```

Resources Controlled By The Award plug and play BIOS can automatically configure plug-and-play devices. AUTO selection displays the screen as above. MANUAL introduces additional options as indicated below. These additional options are automatically handled in AUTO selection.

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Reset Configuration Data

This is normally left DISABLED. Select ENABLED to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system re-configuration has caused such a serious conflict that the operating system cannot boot.

IRQ x Assigned To

When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt:

LEGACY ISA:

Devices compliant with the original PC AT bus specification, requiring a specific interrupt (such as IRQ4 for serial port 1).

PCI/ISA PnP:

Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

DMA x Assigned To

When resources are controlled manually, assign each system DMA channel as one of the following types:

LEGACY ISA:

Devices compliant with the original PC AT bus specification, requiring a specific DMA channel.

PCI/ISA PnP:

Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

PCI IDE 2nd Channel

Since your chipset supports a second IDE channel, you can use this selection to ENABLE or DISABLE the second channel. The second channel may connect to a CD ROM.

PCI IRQ Activated By

Leave the IRQ trigger set at LEVEL unless the PCI device assigned to the interrupt requires Edge-triggered interrupts.

PCI IDE IRQ Map To

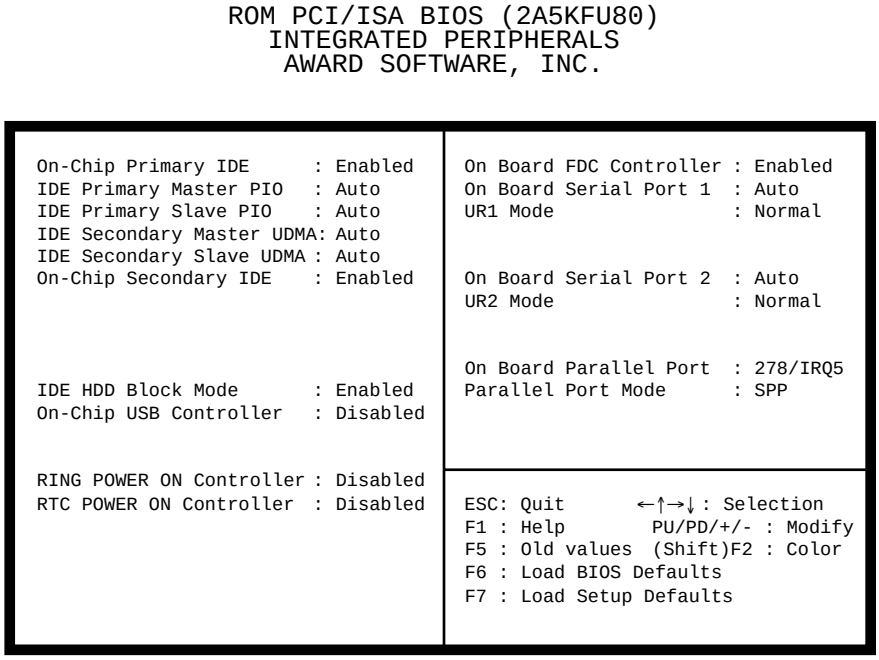
This field lets you select PCI IDE IRQ mapping or PCI AT (ISA) interrupts. If your system does not have one or two PCI IDE connectors on the system board, select values according to the type of IDE interface(s) installed in your system (PCI or ISA). Standard ISA interrupts for IDE channels are IRQ14 for primary and IRQ15 for secondary. Options are ISA, PCI-Slot1, PCI-Slot2, PCI-Slot3, PCI-Slot4, and PCI-AUTO. With any option other than ISA, the Primary & Secondary IDE INT# options below are enabled.

Primary And Secondary IDE INT#

Each PCI peripheral connection is capable of activating up to four interrupts: INT# A, INT# B, INT# C, and INT# D. By default, a PCI connection is assigned INT# A. Assigning INT# B has no meaning unless the peripheral device requires two interrupt services rather than just one. Because the PCI IDE interface in the chipset has two channels, it requires two interrupt services. The primary and secondary IDE INT# fields default to values appropriate for two PCI IDE channels, with the primary PCI IDE channel having a lower interrupt than the secondary.

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Integrated Peripherals



On-Chip Primary IDE Controller The integrated peripheral controller contains an IDE interface with support for two IDE channels. Select ENABLED to activate the IDE interface.

IDE Primary/ Master/Slave PIO The IDE PIO (Programmed Input/Output fields) let you set a PIO mode (0-4) for each of the IDE devices that the onboard IDE interface supports. Modes 0 through 4 provide successively increased performance. In AUTO mode, the system automatically determines the best mode for each device.

IDE Secondary Master/Slave UDMA Ultra DMA (UDMA) is a DMA data transfer protocol that utilizes ATA commands and the ATA bus to allow DMA commands to transfer data at a maximum burst rate of 33 Mb/s. When you select AUTO in the IDE DMA fields, (for each of the IDE devices that the internal PCI IDE interface supports), the system automatically determines the optimal data transfer rate for each IDE device.

IDE HDD Block Mode Block mode is also called block transfer, multiple commands, or multiple sector read/write. If your IDE drive supports block mode (most new drives do), select ENABLED for automatic detection of the optimal number of block read/writes per sector the drive can support.

On-Chip USB Controller The options are ENABLED or DISABLED. This option determines the status of the USB port function.

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Ring Power On & RTC Power On	Both of these options must be left DISABLED as their functions are not supported by the cPRO3.
Onboard FDC Controller	Select ENABLED if your system has a floppy disk controller (FDC) installed on the system board and you wish to use it. If you install an add-in FDC or the system has no floppy drive, select DISABLED in this field.
Onboard Serial Ports (1/2, A/B)	Select a logical COM port name and matching address for the first and second serial ports. Select an address and corresponding interrupt for the first and second serial ports. Options are: AUTO, COM1/3F8, COM2/2F8, COM3/3E8, COM4/2E8, and DISABLED.
UR1 & UR2 Mode	Both of these options must be set to NORMAL. Other functions are not supported by the cPRO3.
Onboard Parallel Port	Select a logical LPT port address and corresponding interrupt for the physical parallel port. Options are: DISABLED, 278/IRQ5, 3BC/IRQ7, and 378/IRQ7.
Parallel Port Mode	Leave set to SPP.

Password Settings

When you select this function, a message appears at the center of the screen:

```
ENTER PASSWORD:
```

Type the password, (up to eight characters) and press Enter. Typing a password will clear any previously entered password from CMOS memory. The message now changes to:

```
CONFIRM PASSWORD:
```

Again, type the password and press Enter.

To abort the process at any time, press Esc.

In the Security Option item in the BIOS Features Setup screen, select either SYSTEM, or SETUP:

SYSTEM	Enter a password each time the system boots and anytime you enter Setup.
SETUP	Enter a password every time you enter Setup.

NOTE: To clear the password, simply press Enter when asked to enter a password. Then the password function is disabled.

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CHAPTER 5 Board Resources

Chapter Scope

This chapter describes the software- and hardware-configurable options of the cPRO3, as well as interrupts, DMA channels, and non-AT registers.

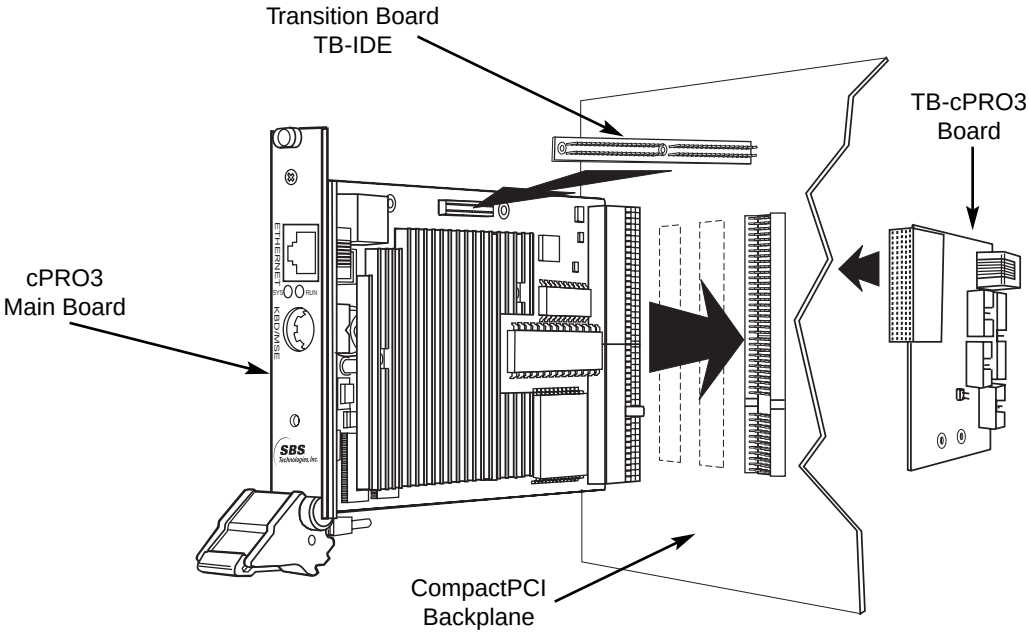
cPRO3 Options

Processor Type & Speed

The cPRO3 is designed to accommodate several Pentium processors at a variety of speeds.

DRAM Size

The cPRO3 can accommodate 32 Megabytes of EDO memory.



cPRO3 with Backplane, Transition Board and TB-cPRO3 Board

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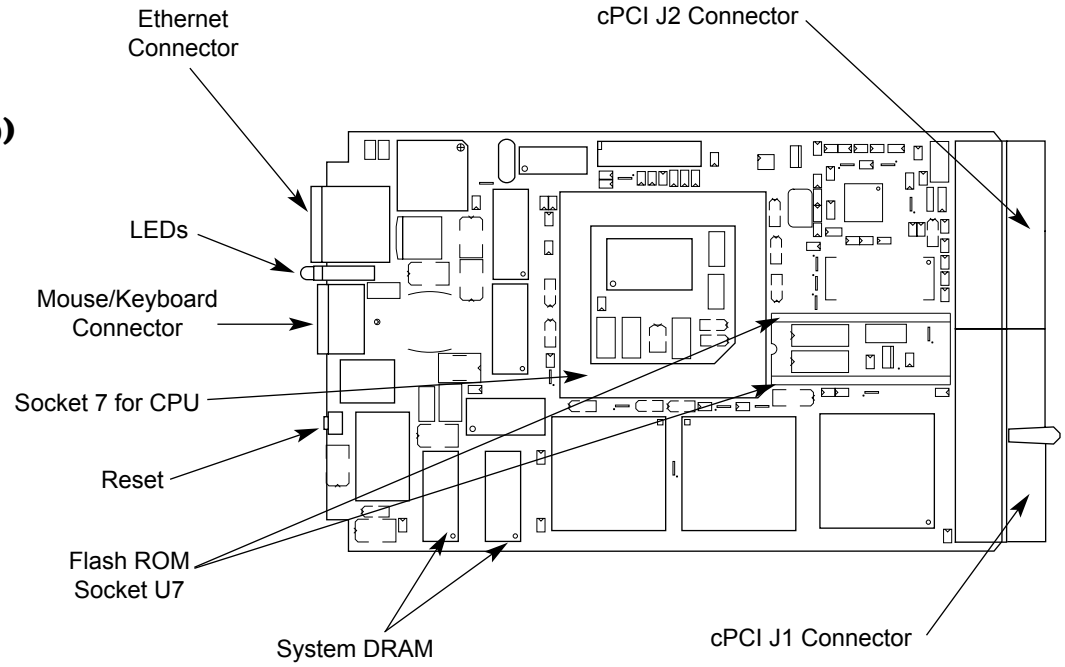
Front Panel LEDs

On the front panel of the cPRO3 there are two LEDs which provide important information regarding the status of the board. These LEDs are, from top to bottom:

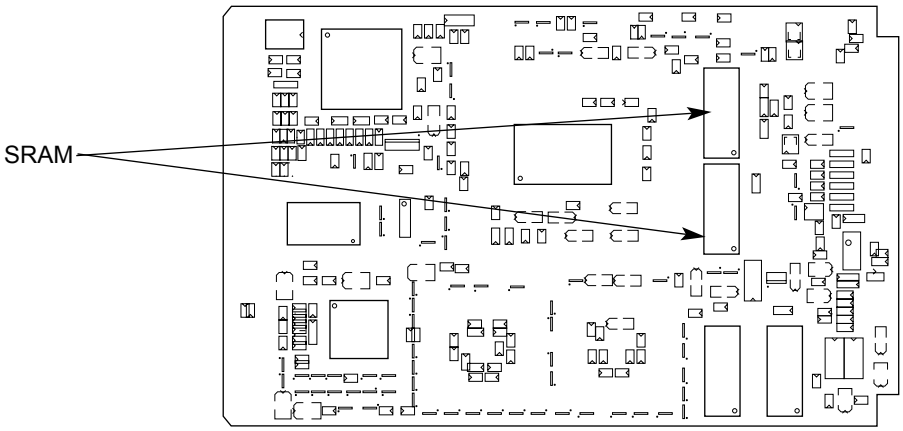
RUN This LED indicates that the processor is active. This LED may flicker as other devices occupy the local bus, but extended outage could indicate that the board is locked up.

SYSFAIL/USR This LED is user-defined and under user software control through the User Register.

PCB (Top)



PCB (Bottom)



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PC Interrupts

The 17 PC interrupts (including NMI) are allocated as shown in Table 5-1. Note that these are the default allocations, some can be changed. The PCI Interrupt is selectable between IRQ5, IRQ10, IRQ11, and IRQ15. IRQ11 is the default.

Interrupt	Interrupt Number	Description/Use
NMI	N/A	Parity Error
IRQ0	8	Timer
IRQ1	9	Keyboard
IRQ2	A	Chain to Interrupts 8–15
IRQ3	B	COM2
IRQ4	C	COM1
IRQ5	D	Available; Selectable as PCI Interrupt**
IRQ6	E	Floppy Disk*
IRQ7	F	Not Used
IRQ8	70	Real Time Clock
IRQ9	71	Re-Directed to IRQ2
IRQ10	72	Not Used
IRQ11	73	Not Used
IRQ12	74	Bus Mouse
IRQ13	75	Coprocessor
IRQ14	76	IDE Hard Disk*
IRQ15	77	Available; Selectable as PCI Interrupt**

Table 5-1 PC Interrupt Allocation

* These devices can be disabled to free the occupied interrupt.

** The PCI Interrupt is configurable as PC interrupt IRQ5, IRQ10, IRQ11, or IRQ15. IRQ11 is the default setting for INTA and IRQ10 is the default for INTB. Any of these PC interrupts to which the PCI Interrupt is not assigned can be considered available for other uses.

DMA Channels

The eight PC DMA channels are allocated as shown in Table 5-2. These are the default allocations, some can be changed. With all onboard devices enabled, six DMA channels are available for use by peripheral cards. Disabling the Floppy Disk will free DMA channel 2.

DMA Channel	Description/Use
0	Memory Refresh
1	Unassigned, Available
2	Floppy Disk*
3	Unassigned, Available
4	Unassigned, Available
5	Unassigned, Available
6	Unassigned, Available
7	Unassigned, Available

Table 5-2 DMA Channel Allocation

* These devices can be disabled to free the occupied DMA channel.

cPRO3 Registers

The cPRO3 has several non-AT registers such as Reset Control Register and two Serial EEPROMs which allow complete control of the hardware by software. These registers are fully documented in the Programming section.

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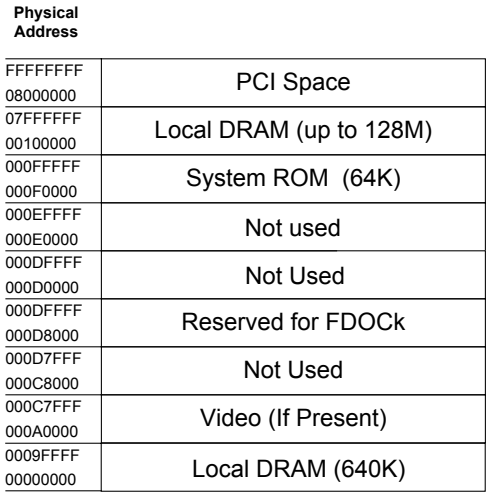


Figure 5-1 cPRO3 Memory Map

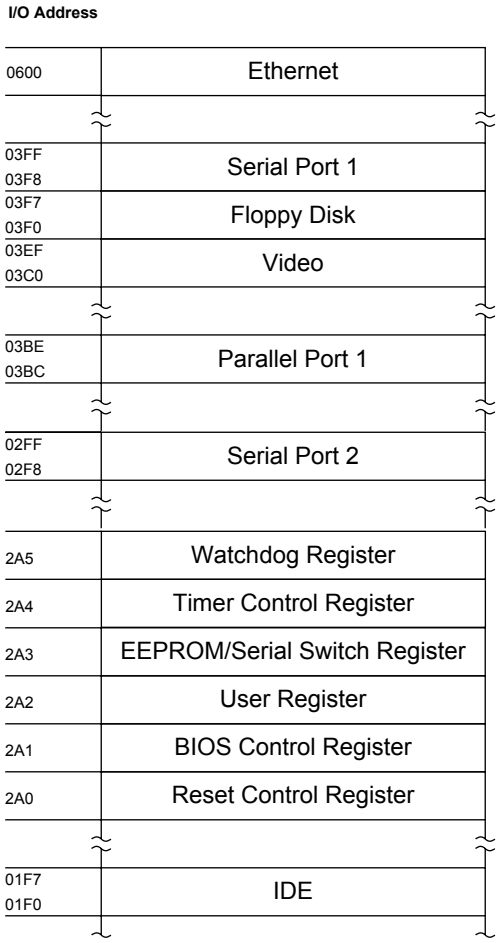
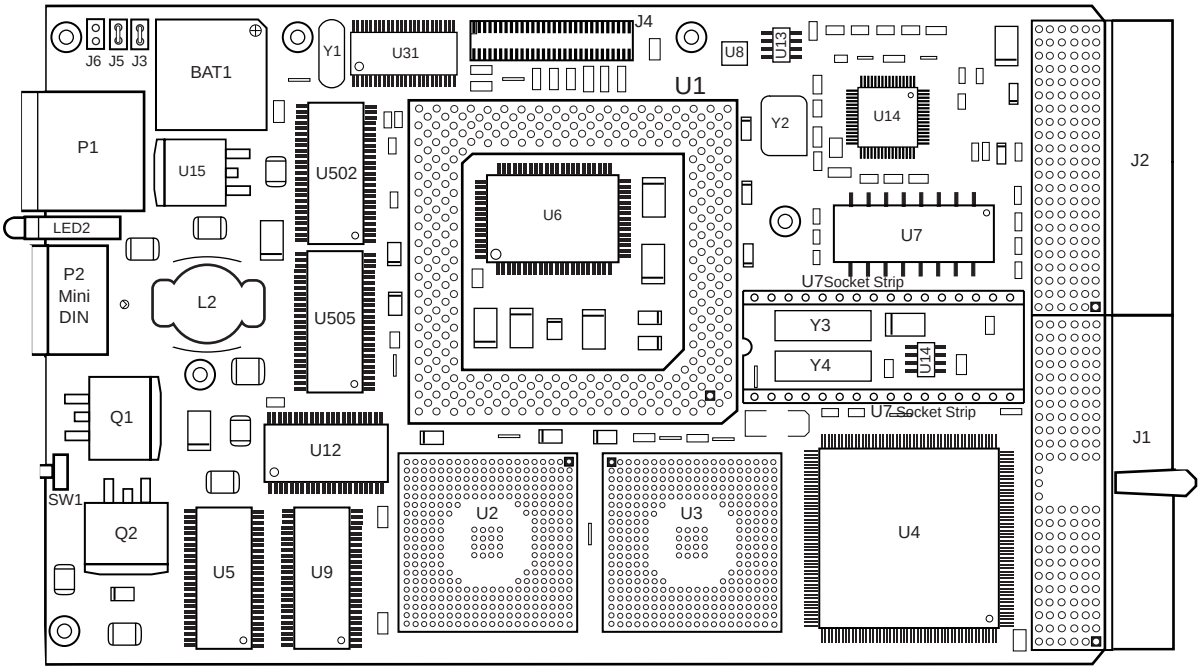


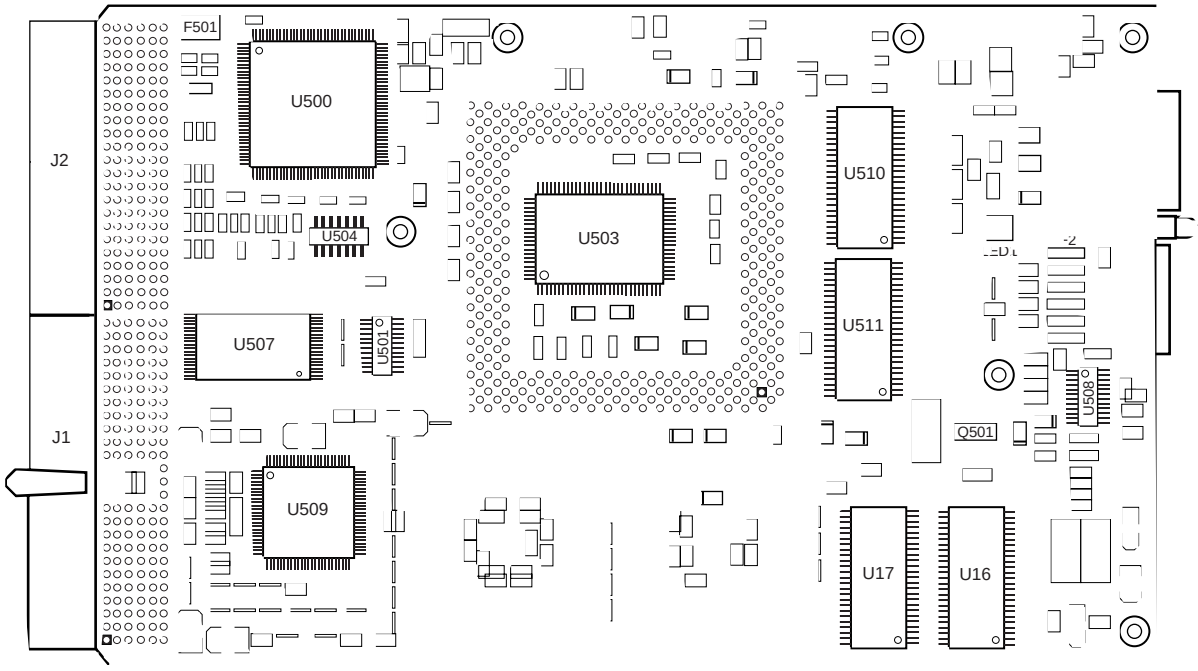
Figure 5-2 cPRO3 I/O Map

Note that Local DRAM entries are dependent on the amount of DRAM installed. Also, some devices such as Floppy can be disabled, freeing space in the I/O map.

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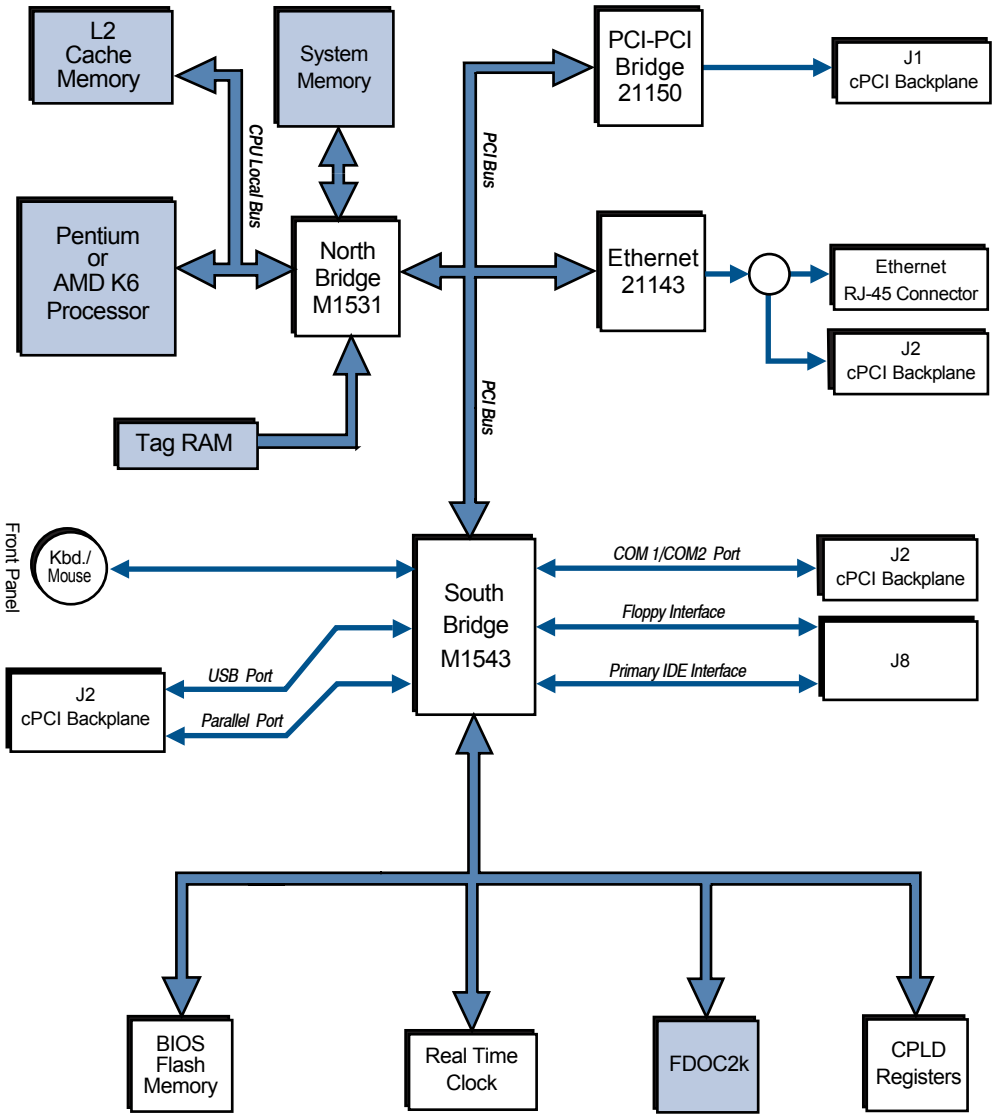
cPRO3 PCB Layout, Top View



cPRO3 PCB Layout, Bottom View

Figure 5-3

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cPRO3 Block Diagram

Figure 5-4

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CHAPTER 6

PC/AT Devices Programming

Chapter Scope

This chapter describes programming the PC/AT devices of the cPRO3. The basic peripherals such as the serial ports, the parallel port, and the keyboard port are covered generally, as are the more advanced controllers for the video, floppy disk, and hard disk interfaces. Devices not usually found on a standard desktop PC/AT, such as onboard Ethernet and advanced SVGA video, are covered in more detail.

Note that it is beyond the scope of this manual to provide the programming details associated with the IBM PC/AT compatible hardware, MS-DOS software, and the ROM BIOS. Rather, it is suggested that one of the many good programming reference books for the PC/AT architecture be consulted. We highly recommend that you obtain a copy of *Advanced MS-DOS* which is published by Microsoft Press. It presents the details of the software environment of MS-DOS and the associated calls to the ROM BIOS. If you are planning to program in 80x86 assembler or a high-level language such as 'C' and need to access system resources directly, you will find this book absolutely essential.

PC/AT Compatible ROM BIOS

The ROM BIOS is a firmware (installed in ROM) resident set of routines which is used to interface the particular system hardware to the MS-DOS operating system, and subsequently to MS-DOS applications. The use of a ROM BIOS in the original IBM PC/AT design has allowed programs to be developed specifically for the operating system environment without concern for the underlying hardware. Programs developed using the AT BIOS can be run on a variety of PC/AT compatible computers without modification. The BIOS provides a very rigid interface between the operating system and applications, and the hardware devices of the system. MS-DOS accesses devices through BIOS calls. These routines must perform their functions and return to the operating system after completion, without disturbing other system functions.

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The cPRO3 CompactPCI Computer uses Award Software BIOS for complete compatibility with IBM's BIOS, without infringing on IBM's copyright. Since the BIOS is completely compatible in operation with the original, we can assure you that programs developed correctly will run, unmodified on the cPRO3.

In order to use the routines contained in the AT ROM BIOS you will need to know how to make BIOS calls through software interrupts. This is described in detail in *Advanced MS-DOS*.

Serial Communications Interface

The NS16450/16550-compatible UART serial controllers within the M1543 fully implement both the standard PC/AT COM1 and COM2 serial ports. These devices normally appear at the standard addresses of 3F8H–3FFH for COM1 and 2F8H–2FFH for COM2. These addresses are software configurable. Standard input and output with the COM ports is accomplished with BIOS calls through interrupt 14H. These calls are fully described in Section 3 of *Advanced MS-DOS*.

Parallel Port

The parallel port is also provided by the M1543 and is typically used for interfacing to Centronics-compatible parallel printers. MS-DOS defines the device, PRN, as the normal printer output device of the system. Therefore, the programmer should not require access to the parallel port directly. Rather, printer services available through the AT BIOS at interrupt 17H should be used. AT BIOS services are fully described in Section 3 of Advanced MS-DOS. Also, be aware that the parallel port of the cPRO3 is capable of SPP, ECP and EPP modes.

Keyboard Port

The keyboard interface is provided by the M1543 which is fully compatible with the keyboard used on the IBM PC/AT. Built into the AT BIOS are calls for keyboard services using interrupt 16H. Section 3 of Advanced MS-DOS describes these calls in detail.

Real Time Clock

The Real-Time Clock of the cPRO3 is equivalent to the Motorola 146818A and is contained in the BQ3285E IC. The RTC occupies 3FH indexed locations and contains registers for clock timekeeping and control, as well as 16 bytes of scratchpad RAM (reserved for use by AT Setup). As long as battery power is provided, the clock will continue updating the date and time registers as well as preserve the contents of the scratchpad RAM.

Accessing the RTC is accomplished by first writing the index address to I/O port address 70H. The valid index address range is 0-7FH. The first 40H locations are used by the cPRO3, while the remaining 40H are available for general use. The register or RAM data can then either be written or read at I/O port address 71H. The specific use of clock registers is covered in the data sheet on the Motorola 146818A.

Y2K Note

The RTC clock is a 100-year device. No hardware provisions exist to denote the rollover in the year 2000. An attempt to circumvent this problem has been implemented in the BIOS. However, advanced operating systems such as Windows NT do not use the BIOS to interface to the RTC. As such, they may display the year 2000 as the year 1900, etc.

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Non-Volatile RAM

The Non-Volatile RAM is actually the scratchpad RAM of the RTC discussed previously. This RAM is battery-backed and contains data used by AT Setup.

Reset Control Register

The Reset Control Register is used to configure the sources and effects of reset conditions. The register is located at I/O address 2A0H.

RSV	RSV	RSV	IGSR	RSV	RSV	RSV	FPSR
7	6	5	4	3	2	1	0

Figure 6-1 Reset Control Register (I/O 2A0H)

Bit 0: 0 = No Reset passed from PCI to cPCI
Default = 1

Bits 1,2,3: Reserved
These bits are reserved for future use by SBS. Reads are not guaranteed to return any particular value. To avoid incompatibilities with future hardware, it is recommended that you leave these bits unchanged during writes.

Bit 4: 0 = No Reset passed from cPCI to PCI
Default = 0

Bits 5–7: Reserved
These bits are reserved for future use by SBS. Reads are not guaranteed to return any particular value. To avoid incompatibilities with future hardware, it is recommended that you leave these bits unchanged during writes.

BIOS Control Register

The BIOS Control Register controls the write enables to both the onboard FLASH BIOS and the BIOS socket. The register is located at I/O address 2A1H.

BSEL	SBWE	OBWE	UBE	FEN	RSV	RSV	RSV
7	6	5	4	3	2	1	0

Figure 6-2 BIOS Control Register (I/O 2A1H)

Bit 0,1,2: Reserved
Reserved for future use by SBS. Reads not guaranteed to return any particular value. To avoid future incompatibilities , leave these bits unchanged during writes.

Bit 3: FDOCk Enable
When set, this bit enables the FDOCk decode logic.
WARNING: Be certain to write back the same value as read.

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Bit 4: Reserved
Reserved for future use by SBS. Reads not guaranteed to return any particular value. To avoid future incompatibilities, leave this bit unchanged during writes.

Bit 5: Onboard BIOS Write Enable (R/W)
This bit enables programming the onboard FLASH BIOS. For normal operation, this bit should be clear so that the onboard BIOS is a read-only device. It should not be set by user programs.
WARNING: Setting this bit makes the BIOS susceptible to data corruption.

Bit 6: Socketed BIOS Write Enable (R/W)
This bit enables programmingof a FLASH ROM in the BIOS socket. For normal operation, this bit should be clear so that any socketed ROM is a read-only device. It should not be set by user programs. *WARNING: Setting this bit makes a FLASH device in the socket susceptible to data corruption.*

Bit 7: BIOS Select
This bit controls the location of the chip select line for the bios. Setting this bit enables the chip select for the on board flash device, disabling the socketed chip select line. Clearing this bit enables the socketed flash chip select line while disabling the on board chip select line. NOTE: This bits status is controlled by jumper J1 at reset and power-up. This bit is set by an uninstalled jumper and is cleared by an installed jumper. Be sure that a valid BIOS is in the socket before installing the jumper or else board failure will result.

User Register

The User Register provides a bit for controlling the SYS LED on the front panel. The purpose of this LED is user-defined.

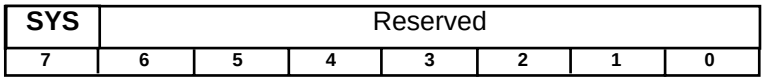


Figure 6-3 User Register (I/O 2A2H)

Bits 0–6: Reserved
Reserved for future use by SBS. Reads not guaranteed to return any particular value. To avoid future incompatibilities , leave these unchanged during writes.

Bit 7: SYS LED Control (R/W)
This bit, when set, illuminates the SYS LED on the front panel of the cPRO3. The purpose of this inidcator is completely user-defined. Note that readbacks of this bit will return the opposite value of the value written.

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Serial EEPROM Register

The Serial EEPROM Register provides a direct interface to the program, data, and clock lines of the serially-programmable EEPROM (see Serial EEPROM below). Programming of this device requires knowledge of device-specific timing requirements, and should be done cautiously. Refer to the National Semiconductor*NM93C46 User's Manual* if you need to access this part directly.

The Serial EPROM Register is an eight-bit register at I/O address 2A3H. The bits are defined as follows:

RSV	OEECS	EEDIN	RSV	RSV	RSV	SDO	CLK
7	6	5	4	3	2	1	0

Figure 6-4 Serial EEPROM Register (I/O 2A3H)

Bit 0: Serial Clock (R/W)
This bit is directly connected to the SK Serial Data Clock line of the NM93C66 Serial EEPROM. It is used for clocking serial data transfers to and from the Serial EEPROM.

Bit 1: Serial Data Out (R/W)
This bit is directly connected to the DI pin of the NM93C66. It is used to send data to the Serial EEPROM.

Bist 2,3,4: Reserved
Reserved for future use by SBS. Reads not guaranteed to return any particular value. To avoid future incompatibilities , leave these unchanged during writes.

Bit 5: Serial EEPROM Data In (R)
This bit is directly connected to the DO pin of the NM93C64 during reads. It is used to receive serial data from the serial EEPROM.

Bit 6: On-Board Serial EEPROM Chip Select (R/W)
This bit is directly connected to the CS pin of the Onboard NM93C66. It selects the NM93C66 chip, making it active and ready for read or write cycles.

Bit 7: Reserved
Reserved for future use by SBS. Reads not guaranteed to return any particular value. To avoid future incompatibilities , leave this bit unchanged during writes.

Serial EEPROM

The cPRO3 incorporates a 128x16 bit serially-accessed Electrically Erasable Programmable Read Only Memory, or EEPROM. This part is the National Semiconductor NM93C66, and is used for storing board setup and configuration data for SETcPRO3 and the VME BIOS. Programming the EEPROM is facilitated through the Serial EPROM Register (see Serial EPROM Register above). However, user programs should make use of the EEPROM only under special circumstances. SBS Embedded Computers can provide you with more information about programming the EEPROM, as well as the dangers of doing so.

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The EEPROM is 64 words in size. The first 43 words are used for VME setup values and board setup information. The remaining 21 words are available for general use.

Note: Like most EEPROM devices, the NM93C66 has a limited lifetime for write cycles. For the NM93C66, the average device life is 10^6 write cycles. Conservative use of the EEPROM will ensure that it lasts the life of the board.

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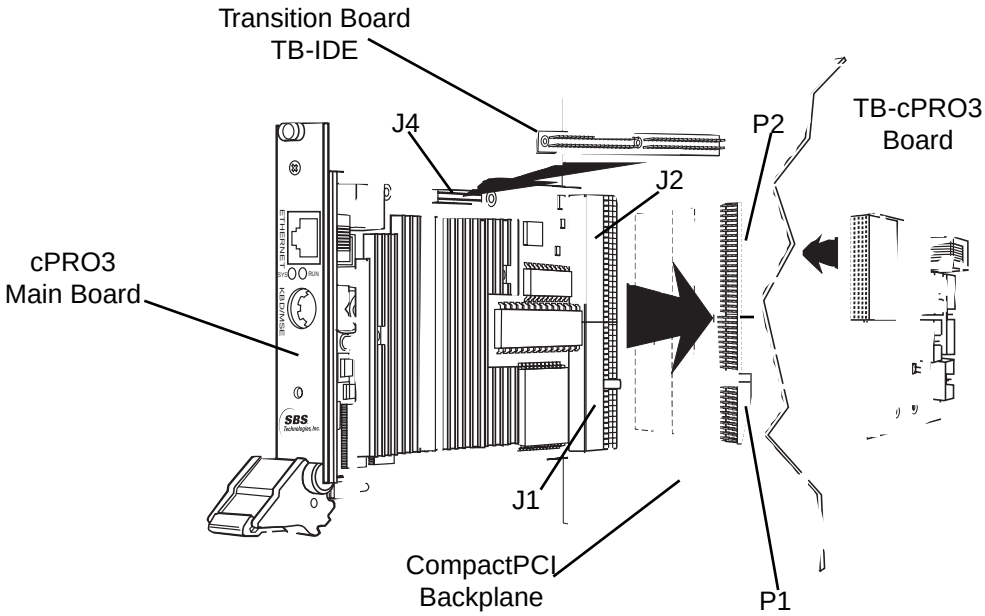
CHAPTER 7

Option Board Accessories

Chapter Scope

In the interests of compactness and user versatility, the cPRO3 provides floppy disk and IDE control functions through onboard connector J4. The pinouts for connector J4 are in Chapter 3: Installation and Interfacing, page 3-6. Two RS-232 protocol serial communications ports, two Universal Serial Bus (USB) ports, a parallel printer port, and Ethernet are all provided at the Compact PCI J2 connector on the rear of the cPRO3 board. The COM1 and COM2 serial ports are at TTL levels out of J2. Ethernet is also available at the RJ45 connector on the front panel, but both ethernet options can not be used simultaneously. The pinouts for connector J2 are in Chapter 3: Installation and Interfacing, page 3-5.

In order to provide simple user access for standard I/O fixtures, two Transition Boards, (TB-IDE and TB-cPRO3) are used with the cPRO3 board. The TB-IDE board comes with the cPRO3. Contact Sales at SBS Embedded Computers or email ***sales@sbs-ec.com*** for information on ordering the TB-cPRO3 Board.



cPRO3 with Backplane, Transition Board and TB-cPRO3 Board

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Serial Ports

The TB-cPRO3 transition board connects to J2 on the rear of the PCI back-plane. The TB-cPRO3 serial ports are defined for industry standard interfacing using RS-232 compatible signal levels. Pin 1 is identified in Figure 7-1. Table 7-1 defines the signals present on the pins of the TB-cPRO3 COM1 and COM2 port connectors, their intended function and their direction. If COM1 or COM2 on the TB-cPRO3 are used, a User supplied +5V must be connected to Pin 4 on the AT style Power Connector on the TB-cPRO3 (GND is Pin 3).

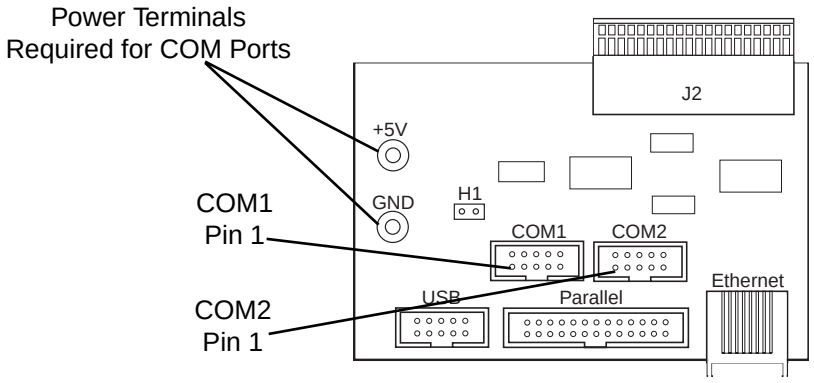


Figure 7-1 TB_cPRO3 Board; Serial Communications (COM1 and COM2) Ports

Extended COM2 Funcionality

The TB-cPRO3 board allows the COM2 serial port of the cPRO3 to provide functionality beyond that of a standard PC/AT. Under Jumper H1 control, COM2 can be configured for RS-422 or RS-485 operation in place of standard RS-232. Jumper H1 ***ON*** enables RS-422/485, Jumper H1 ***OFF*** enables RS232 operation. RS-422 operation on the cPRO3 is four-wire full duplex. RS-485 operation on the cPRO3 is two-wire half duplex. Table 7-2 shows the COM2 signals for RS-422 operation. Table 7-3 shows the COM2 signals for RS-485 operation.

In RS-422 or RS-485 mode it may be necessary to provide termination at the cPRO3 if it is at either end of a multidrop link. For RS-485 this is done automatically by the cPRO3. For RS-422, terminating resistors must be installed in the external connector shield. The terminating resistors should result in a low impedance of 100 ohms or less.

Pin	Signal	Direction	Function
1	DCD	To cPRO3	Data Carrier Detect, from modem
2	RXD	To cPRO3	Received Data, from modem
3	TXD	From cPRO3	Transmitted Data, to modem
4	DTR	From cPRO3	Data Terminal Ready, to modem
5	SIGND	—	Serial Interface Ground reference
6	DSR	From cPRO3	Data Set Ready, from modem
7	RTS	From cPRO3	Request To Send, to modem
8	CTS	To cPRO3	Clear To Send, from modem
9	RI	To cPRO3	Ring Indicator, from modem
10	NC	—	No Connection

Table 7-1 COM-1 & COM-2 (RS-232 Mode) Pin Assignments

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Pin	Signal	Direction	Function
1	NC	—	No connection
2	RXD-	To cPRO3	Receive data, negative
3	TXD-	From cPRO3	Transmit data, negative
4	TXD+	From cPRO3	Transmit data, positive
5	SIGND	—	Serial Interface Ground reference
6	RXD+	To cPRO3	Receive data, positive
7	NC	—	No connection
8	NC	—	No connection
9	RI	To cPRO3	Ring Indicator, from modem
10	NC	—	No Connection

Table 7-2 COM-2 (RS-422 Mode) Pin Assignments

Pin	Signal	Direction	Function
1	NC	—	No connection
2	TX/RX-	From/To cPRO3	Transmit/receive data, negative
3	NC	—	No connection
4	NC	—	No connection
5	SIGND	—	Serial Interface Ground reference
6	TX/RX+	From/To cPRO3	Transmit/receive data, positive
7	NC	—	No connection
8	NC	—	No connection
9	NC	—	No connection
10	NC	—	No Connection

Table 7-3 COM-2 RS-485 Mode Pin Assignments

Note that the DSR and CTS signals are driven true in RS-422/485 mode which allows DOS drivers and communications software to work properly.

Parallel Port

Using the TB-cPRO3 option board, the cPRO3 parallel port is available through a standard 26 pin connector. In its normal operating mode, the port functions exactly as does a standard IBM PC parallel printer port. In this mode of operation, it will interface with printers using the industry standard Centronics parallel interface. Figure 7-2 indicates the TB-cPRO3 connector pins and signals are defined in Table 7-4.

Operation of the printer port is accomplished with routines built into the ROM BIOS supplied with the cPRO3. Therefore, standard MS-DOS printer functions will work with a printer attached as the “PRN” device.

Under software control, the parallel port supports optional PS/2 type bidirectional parallel port (SPP), Enhanced Parallel Port (EPP), and Extended Capabilities Port (ECP) modes.

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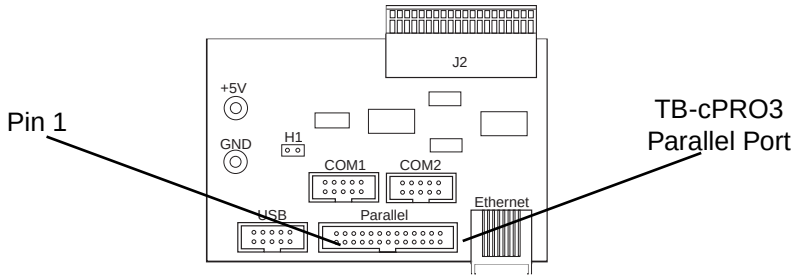


Figure 7-2 TB-cPRO3; Parallel Port Connector

Pin	Signal	Direction	Function
1	STROBE-	Output	Data strobe
2	PD0	I/O	Data bit 0
3	PD1	I/O	Data bit 1
4	PD2	I/O	Data bit 2
5	PD3	I/O	Data bit 3
6	PD4	I/O	Data bit 4
7	PD5	I/O	Data bit 5
8	PD6	I/O	Data bit 6
9	PD7	I/O	Data bit 7
10	ACK-	Input	Data acknowledge
11	BUSY	Input	Printer busy
12	PE	Input	Printer enabled
13	SLCT	Input	Printer selected
14	AUTOFD-	Output	Automatic feed
15	ERROR-	Input	Printer error indicator
16	INIT-	Output	Initialize
17	SLCTIN-	Output	Printer select
18–25	GND	—	Signal Ground
26	NC	—	No Connection

Table 7-4 Parallel Port Pin Assignments

IDE Interface

The TB-IDE Transition Board plugs into connector J4 on the cPRO3. The IDE is a PCI slave facilitated by the M1543 chip. The IDE interface supports Ultra 33 Synchronus DMA mode (up to 33Mbytes/sec transfers). The user must supply a a 40-pin ribbon cable with mating connectors to connect the IDE interface to an IDE drive. The TB-IDE has standard ribbon connectors for Hard drive and Floppy disk. A +5V Power Source with a 1 Amp current limit is also provided by a 4-Pin connector on the TB-IDE board. Page 7-7 shows pin assignments for the IDE interface connector, and page 7-8 shows pin assignments for the Floppy.

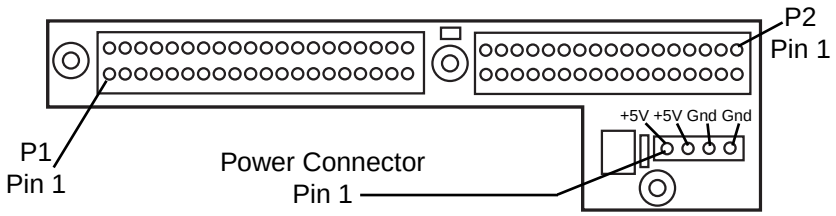
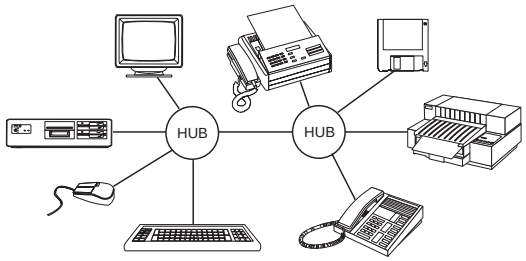


Figure 7-3 ; TB-IDE Transition Board Layout

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USB Ports

Universal Serial Bus (USB) is a new personal computer (PC) interconnect that can support simultaneous attachment of multiple devices. The host serves as master of the bus. Data transfer is serial with two modes of signaling: Full speed mode with a signaling rate of 12 megabits per second (Mbs), and a low speed mode with a signaling rate of 1.5 Mbs. The peripheral devices serve as slaves connected either directly to the host or through hubs which give additional connective capability.



USB System Example

The USB cable consists of four wires. Two wires, D+ and D-, are used for information transfer using differential signaling. The two other wires are used for power: Vbus and Ground. Low-cost unshielded cables are used for the low speed (1.5Mbs) while shielded cables are required for the 12Mbs rate. Essentially the USB protocol is similar to a Token Ring Network. The USB host keeps the bus active by sending a Start Of Frame (SOF) packet every millisecond. The available bus bandwidth is shared between simultaneously connected devices within this 1 millisecond time interval.

Due to the capability of “Hot Swapping”, it is not necessary to power-down to connect or disconnect a USB device. Immediately after a device is attached to the USB host, the host controller is alerted by way of voltage change on the D+ and D- lines. Once the host detects that a device is connected, it determines the exact port it is connected to and enables it. After a reset sequence the host can provide the device with up to 100mA of current through the Vbus/Gnd lines. Of course, self-powered devices do not use the power from the host.

The host uses an interrogation sequence through which it acquires information from the connected device, gives it a unique address, and assigns a configuration value. The system software then either recognizes the device and loads the corresponding device driver, or prompts the user to provide a device driver for the application. After the device driver is loaded, the device performs its intended function until it is detached from the host. Immediately after a device is detached from the USB host port, specific voltage changes on the D+ and D- lines alert the host of the action. The USB system software then acknowledges the removal of the device and frees up any host resources the device was using. For example the host reclaims the bandwidth, and if the device was bus-powered, it reclaims the power and makes it available to other devices.

The cPRO3 has two USB Ports (designated USB1 and USB2) available through the backplane, or if the TB cPRO3 Option Board is used, through a 10-Pin labled connector. The cPRO3 supports both the Full Speed (12Mbs) and Low Speed (1.5Mbs) USB serial transfer. The cPRO3 USB Protocol is facilitated by the USB Controller built into the M1543 chip, which is a PCI master.

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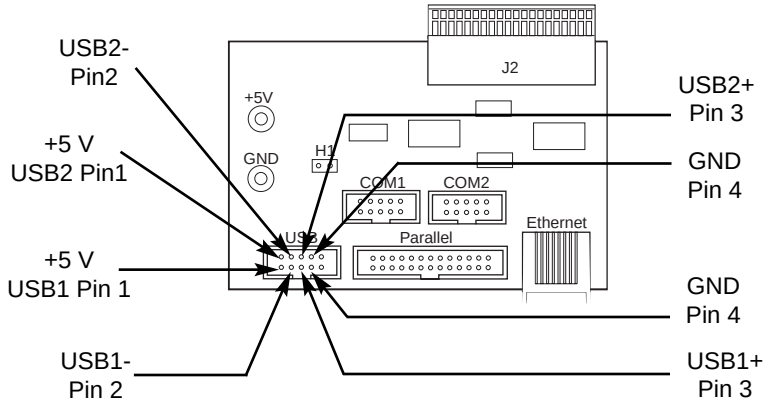


Figure 7-4 TB-cPR03; USB Connector pin outs

Pin	Signal	Function
1	VCC	USB Port Vbus Power Connection*
2	D-	Data - Connection
3	D+	Data + Connection
4	GND	Power Ground

Table 7-5 USB Header Pin Assignments

* This pin is current limited to 750 mA for both USB1 and USB2 through a resettable polyfuse.

NOTE:

Prior to using the SBS BIOS Update Utility, ***"Bios_pgm.exe"*** *it is necessary to temporarily Disable the USB port via the BIOS Setup (See Chapter 4, Booting and Operation, Page 4-14). Failure to do this will corrupt the programming effort and render the board inoperable. The board will then have to be returned to the factory for repair. Following the BIOS update, the USB port can again be Enabled using the BIOS Setup. For further information contact support@sbs-ec.com for assistance.*

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Pin	Pin Name	Type	Description
1	RSTDRV-	O	Reset to IDE drive
2	GND		Digital ground
3	PIDE07	I/O	Primary IDE ATA data bit 07
4	PIDE08	I/O	Primary IDE ATA data bit 08
5	PIDE06	I/O	Primary IDE ATA data bit 06
6	PIDE09	I/O	Primary IDE ATA data bit 09
7	PIDE05	I/O	Primary IDE ATA data bit 05
8	PIDE10	I/O	Primary IDE ATA data bit 10
9	PIDE04	I/O	Primary IDE ATA data bit 04
10	PIDE11	I/O	Primary IDE ATA data bit 11
11	PIDE03	I/O	Primary IDE ATA data bit 03
12	PIDE12	I/O	Primary IDE ATA data bit 12
13	PIDE02	I/O	Primary IDE ATA data bit 02
14	PIDE13	I/O	Primary IDE ATA data bit 13
15	PIDE01	I/O	Primary IDE ATA data bit 01
16	PIDE14	I/O	Primary IDE ATA data bit 14
17	PIDE00	I/O	Primary IDE ATA data bit 00
18	PIDE15	I/O	Primary IDE ATA data bit 15
19	GND		Digital Ground
20	NC		
21	PHDRQ	O	Primary IDE DMA request
22	GND		Digital Ground
23	PIDEIOW	I	Primary IDE IOW command
24	GND		Digital Ground
25	PIDEIOR-	I	Primary IDE IOR command
26	GND		Digital Ground
27	PHDIORDY	O	Primary IDE Ready
28	CSEL	O	Cable Select
29	PIDEACK	I	Primary IDE acknowledge
30	GND		Digital Ground
31	PIDEIRQ	O	Primary IDE interrupt request
32	NC		
33	PIDEA1	I	Primary IDE ATA address 1
34	NC		
35	PIDEA0	I	Primary IDE ATA address 0
36	PIDEA2	I	Primary IDE ATA address 2
37	PIDECSO-	I	Primary IDE chip select 1
38	PIDECS1-	I	Primary IDE chip select 2
39	PDASP-	O	Device active present
40	GND		Digital Ground

Table 7-6 TB-IDE, IDE Connector Signals

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P3 Pin	Signal	Direction	Signal Description
Odd	GND		Signal Ground
2	FRWC-	To Drive	Read/Write Control
4	NC		Not Connected - Unused
6	NC		Not Connected - Unused
8	FINDEX-	From Drive	Index Mark Detected
10	FMT0-	To Drive	Motor On 0
12	FDS2-	To Drive	Drive Select 2
14	FDS1-	To Drive	Drive Select 1
16	FMT1-	To Drive	Motor Control 1
18	FDIRC-	To Drive	Step Motor Direction Control
20	FSTEP-	To Drive	Motor Step Control
22	FWD-	To Drive	Write Data
24	FWE-	To Drive	Write Enable
26	FTK0-	From Drive	Track 0 Position
28	FWP-	From Drive	Floppy is Write Protected
30	FRD-	From Drive	Read Data
32	FHS-	To Drive	Head (Side) Select
34	FDSKCHG-	From Drive	Disk Change Indicator

Table 7-7 TB-IDE, Floppy Drive Interface Signals

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CHAPTER 8 Specifications

General

Model	cPRO3
Description	CompactPCI Single Board Computer

PCI Bus

Controller	ALI Aladdin IV Chipset
Clock Rate	33MHz

USB Port

Controller	ALI Aladdin IV Chipset Low Speed(1.5MB/s) and Full Speed(12MB/s)

Serial Interface

Controller	ALI Aladdin IV Chipset (16550 compatible)
Number	2
Compatibility	IBM PC
Interface Type	COM1: TTL; COM2: TTL
Signals Provided	RxD, TxD, RTS, CTS, DSR, DTR, DCD, RI
Connector	Through Backplane or optional TB-cPRO3 Board for RS-232 & COM2 RS-485

Parallel Interface

Controller	ALI Aladdin IV Chipset
Number	1
Compatibility	Centronics Parallel, PS/2 Bidirectional
Interface	Buffered Parallel
Connector	Through Backplane or optional TB-cPRO3 Board

Mouse / Keyboard Interface

Controller	ALI Aladdin IV Chipset
Compatibility	Microsoft Mouse and PS/2 style keyboard resident in a single 6-pin mini connector, reverse IBM standard. Keyboard Default, Mouse thru adapter
Connector	6-pin Circular Mini-DIN

Disk Drive Interface

Floppy Disk	ALI Aladdin IV Chipset provided through J8 or optional TB-cPRO3
Hard Disk	Primary PCI IDE provided through J8 or optional TB-cPRO3

Ethernet Interface

Type	IEEE 802.3 10/100BaseT (Twisted Pair) provided through RJ45 connector
Controller	DEC 21143 or optional thru TB-cPRO3

Electrical

Power	+5VDC @ 5–10A (memory & CPU dependent) +3.3VDC @ 400mA

Physical

Size	100mm × 160mm (3.94 in. x 6.30 in.), 3U×4HP
Construction	Multi-Layer Printed Circuit

Environmental

Temperature	0 to 55° Celsius Inlet Air, Operating (Extended temperature versions available on request. Contact factory for more information). -40 to 85° Celsius, Non-Operating
Cooling	Forced Air, 100LFM Fan Recommended
Humidity	10 to 95% Relative Humidity, Non-Condensing
Shock	6G Max. Operating, 10G Max. Non-Operating

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CHAPTER 9

Support, Service, and Warranty

Chapter Scope

The following sections describe SBS Technologies product support program. It states our product warranty terms and provides details about what action to take if you experience a problem with the product.

Warranty Statement

SBS Technologies CPU products come with a “return-to-factory” warranty that covers defects in materials and workmanship for a period of two years from the date of product shipment to the customer (original purchaser), provided the product is unmodified and has been subject to normal and proper use. This warranty applies to all standard board-level products which do not incorporate disk drives. Products which incorporate floppy or hard disk drives are also warranted for two years with the exception of the drives themselves. The drives will be warranted for a period of ninety days, according to the normal period for electromechanical components. SBS Technologies makes no warranty or representation, express or implied, with respect to software, its performance, quality, or fitness for a particular purpose. This does not include the media on which the software is distributed, which carries a warranty covering defects in materials and workmanship for a period of ninety days.

If You Have a Problem with an SBS Product

Technical support is available by phone, fax or email. Telephone suppport is available during the following Eastern Time hours:

Monday through Friday 8:30 am - 5:30 pm.

You can reach technical support at:

(919) 851-1101 (voice)
(919) 851-2844 (fax)
support@sbs.com (email)

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Product Repairs

To expedite assistance for problems, be able to provide the following:

- Your Name, Phone and Company.
- Product with which you are having trouble.
- Serial Number and Revision.
- Operating system you are running.
- Detailed description of your problem and any error messages that have appeared on the screen.

Depending on the circumstances of the problem, it may be deemed necessary to return the product to SBS Technologies for repair. In order to return the product for repair, the following steps are necessary:

1. Obtain a Return Material Authorization number (RMA#) from SBS Customer Support.

2. Ship the product prepaid to the designated repair point.

3. Provide a written description of the claimed defect with the product.

Obtaining an RMA Number

To obtain a product return authorization number (RMA#), you should call our Customer Service department through our main number.

Shipping the Product

Any product returned to SBS should be in its original shipping carton if possible. Otherwise the product should be carefully packaged in a conductive packing material and placed in a cushioned corrugated carton suitable for shipping. Please mark the shipping label with the RMA number and return it to:

Customer Service Department
Att: RMA# *(put RMA number here)*
SBS Technologies, Inc.
6301 Chapel Hill Road
Raleigh, NC 27607

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Providing a Product Defect Report

When you are returning a product for repair, it is very important to include a written report which details the nature of the problem in order to expedite the repair. Please make sure that the following information is included:

- RMA Number
- Product:
- Serial Number
- Contact:
- Phone
- Description of the Problem/Defect

Warranty Repairs

Any product returned and found to be under warranty will be repaired or replaced at the discretion of SBS Technologies.

Non-Warranty Repairs

If a product is found not to be under warranty, we will notify you of the non-warranty situation and provide you with a fixed cost and a schedule for the repair. Non-warranty repairs generally require that a purchase order be issued to SBS Technologies Inc. for the amount of the repair before repairs are undertaken.



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APPENDIX A cPRO3 Register Summary

Appendix Scope

This appendix gives a summary of the cPRO3 board-specific registers which are not standard PC/AT, or peripheral device registers. The register layout and location are given, as are the bit mneumonics and names. Read or write capability for each bit is also shown.

RSV	RSV	RSV	IGSR	RSV	RSV	RSV	FPSR
7	6	5	4	3	2	1	0

Reset Control Register
I/O 2A0H

Bit	Description
0	0 = No Reset passed from PCI to cPCI. Default = 1
4	0 = No Reset passed from cPCI to PCI. Default = 0

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BSEL	SBWE	OBWE	RSV	FEN	RSV	RSV	RSV
7	6	5	4	3	2	1	0

BIOS Control Register
I/O 2A1H

Bit	Description
5	Onboard BIOS Write Enable (R/W)
6	Socketed BIOS Write Enable (R/W)

SYS	Reserved						
7	6	5	4	3	2	1	0

User Register
I/O 2A2H

Bit	Description
7	SYS LED Control (R/W)

RSV	OEECS	EEDIN	RSV	RSV	RSV	SDO	CLK
7	6	5	4	3	2	1	0

Serial EEPROM Register
I/O 2A3H

Bit	Description
0	Serial Clock (R/W)
1	Serial Data Out (R/W)
2	Reserved
3	Reserved
4	Reserved
5	EEPROM Data In (R/W)
6	EEPROM Chip Select (R/W)

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