IP-OCTALPLUS232
IP-OCTALPLUS422
IP-OCTALPLUSTTL
IP-OCTPL232-ET
IP-OCTPL422-ET
IP-OCTPLTTL-ET

8 Channels of Serial Interface

User Manual

Subject to change without notice.

Part Number: 89010400 Rev. 1.0

20030423

IP-OCTALPLUSxxx

IP-OCTPLxxx-ET

8 Channels of Serial Interface

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1 Product Description

The IP-OCTALPLUSxxx and IP-OCTPLxxx-ET are IndustryPack® compatible modules providing eight channels of high performance serial interface.

Six variations of the IPs are available:

- IP-OCTALPLUS232 provides RS232 interfaces
- IP-OCTPL232-ET provides RS232 interfaces and supports operation in an extended temperature range
- IP-OCTALPLUSTTL provides TTL level interfaces
- IP-OCTPLTTL-ET provides TTL level interfaces and supports operation in an extended temperature range
- IP-OCTALPLUS422 provides RS422 interfaces
- IP-OCTPL422-ET provides RS422 interfaces and supports operation in an extended temperature range

Each channel has a 64 byte transmit FIFO and a 64 byte receive FIFO to significantly reduce the overhead required to provide data to and get data from the transmitters and receivers. The FIFO trigger levels are programmable.

The IP-OCTALPLUS232/TTL and IP-OCTPL232/TTL-ET support RxD, TxD, RTS, CTS and GND for each of the eight RS232 / TTL channels. The IP-OCTALPLUS422 and IP-OCTPL422-ET support RxD+/-, TxD+/- and GND for each of the eight RS422 channels.

The baud rate is individually programmable for up to 115.2kbaud for the 232 interface cards and up to 460.8kbaud for the TTL and 422 interface cards.

The 232 and 422 interface cards provide ESD protected transceivers (up to +/-15KV according to IEC 1000-4-2).

Several transition modules for I/O cabling are available:

- XM-OCTAL-6U-D provides 8 DB-25 connectors mounted in a 6U 8TE front panel
- XM-OCTAL-6U-RJ8 provides 8 RJ45 connectors mounted in a 6U 4TE front panel
- XM-OCTAL6URJ16 provides 16 4-pin RJ connectors mounted in a 6U 4TE front panel.

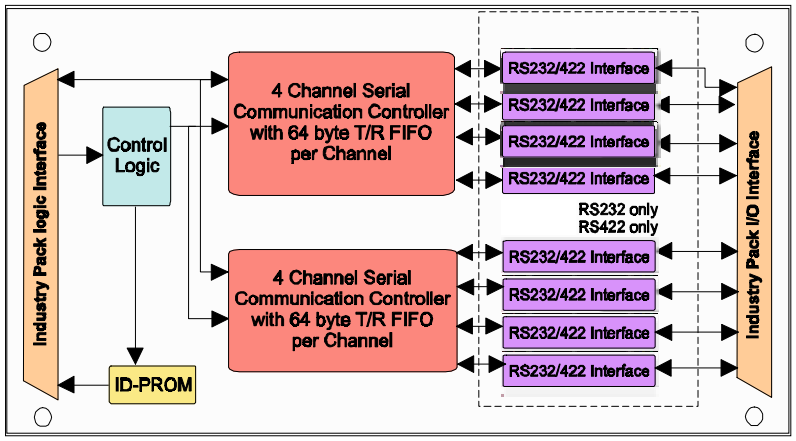


Figure 1-1 : Block Diagram

2 Technical Specification

IP Interface	Single Size IndustryPack® Logic Interface compliant to ANSI/VITA 4-1995 8MHz	
Wait States	No wait states	
Interrupts	Vectored interrupts IP_INTREQ0# for I/O channels 1-4 IP_INTREQ1# for I/O channels 5-8	
Number of Serial Channels	8	
Serial Controller	Two ST16C654 (Quad UART)	
FIFO	64 byte transmit FIFO, 64 byte receive FIFO per channel	
I/O Signals	IP-OCTALPLUS232/TTL and IP-OCTPL232/TTL-ET (RS232) / - (TTL) : TxD, RTS, RxD, CTS, GND DTR, DSR, DCD, RI additionally for channel 1 and channel 2 IP-OCTALPLUS422 and IP-OCTPL422-ET (RS422) : TxD+/-, RxD+/-, GND	
I/O Line Termination	120ohms on board between RxD+ and RxD- for IP-OCTALPLUS422 and IP-OCTPL422-ET	
Baud Rates	Each channel individually programmable : IP-OCTALPLUS232 and IP-OCTPL232 -ET up to 115.2 Kbaud IP-OCTALPLUS422/TTL and IP-OCTPL422/TTL-ET up to 460.8 Kbaud	
I/O Interface Connector	50-conductor flat cable	
ESD Protection	RS232/422 Transmitter : +/-6kV IEC1000-4-2, contact discharge +/-15kV IEC1000-4-2, air gap discharge RS232/422 Receiver : +/-8kV IEC1000-4-2, contact discharge +/-15kV IEC1000-4-2, air gap discharge	
Power Requirements	40mA typical @ +5V DC (no serial channel connected) 1mA typical @ - 12V DC (no serial channel connected) 1mA typical @ + 12V DC (no serial channel connected)	
Temperature Range	Operating Storage	0 °C to +70 °C -40°C to +125°C
MTBF	IP-OCTALPLUS232 and IP-OCTPL232-ET : 714778 h IP-OCTALPLUS422 and IP-OCTPL422-ET : 667498 h	
Humidity	5 – 95 % non-condensing	

Figure 2-1 : Technical Specification

3 ID Prom Contents

Address	Function	Contents
0x01	ASCII ‘I’	0x49
0x03	ASCII ‘P’	0x50
0x05	ASCII ‘A’	0x41
0x07	ASCII ‘C’	0x43
0x09	Manufacturer ID	0xB3
0x0B	Model Number	0x2F
0x0D	Revision	0x10
0x0F	Reserved	0x00
0x11	Driver-ID Low - Byte	0x00
0x13	Driver-ID High - Byte	0x00
0x15	Number of bytes used	0x0D
0x17	CRC	232 : 0x07 TTL : 0x26 422 : 0xF8
0x19	IP-OCTALPLUS and IP-OCTPL Board Option	232 : 0x0A TTL : 0x0B 422 : 0x14
0x1B	Not used	0x00
…	...	...
0x3F	Not used	0x00

Figure 3-1 : ID PROM Contents

4 IP Addressing

All registers for the eight serial channels and three special registers of the IP-OCTALPLUS and IP-OCTPL-ET are accessible in the IP I/O space:

Register	Address Offset in IP I/O Space
Channel 1 Register Set	0x00 to 0x0F
Channel 2 Register Set	0x10 to 0x1F
Channel 3 Register Set	0x20 to 0x2F
Channel 4 Register Set	0x30 to 0x3F
Channel 5 Register Set	0x40 to 0x4F
Channel 6 Register Set	0x50 to 0x5F
Channel 7 Register Set	0x60 to 0x6F
Channel 8 Register Set	0x70 to 0x7F
INTVEC	0x0F
FIFORDY1	0x1F
FIFORDY2	0x5F

Figure 4-1 : I/O Space Address Map

The three special registers INTVEC, FIFORDY1 and FIFORDY2 are located within the register sets of channels 1, 2 and 6.

4.1 Channel Register Sets

Each of the eight I/O channels is controlled by two register sets (register set 1 and register set 2) mapped to the Quad-UART ST16C654 registers.

The Line Control Register (LCR) is common to both register sets of a channel. Bit 7 of the Line Control Register is used to select the actual register set (1 or 2) for a channel.

For more details on the ST16C654 registers and programming please see the ST16C654 Data Sheet.

4.1.1 Channel 1 Register Set

After reset Register Set 1 is selected.

Register Set 1 is accessible if Bit7 of the Line Control Register (LCR) (Offset 0x07) is set to ’0’.

The special register INTVEC is accessible within this register set.

Offset in IP I/O Space	Read Mode	Write Mode	Size (Bit)
0x01	Receive Holding Register (RHR)	Transmit Holding Register (THR)	8
0x03	Interrupt Enable Register (IER)	Interrupt Enable Register (IER)	8
0x05	Interrupt Status Register (ISR)	FIFO Control Register (FCR)	8
0x07	Line Control Register (LCR)	Line Control Register (LCR)	8
0x09	Modem Control Register (MCR)	Modem Control Register (MCR)	8
0x0B	Line Status Register (LSR)	-	8
0x0D	Modem Status Register (MSR)	-	8
0x0F	Interrupt Vector Register (INTVEC)	Interrupt Vector Register (INTVEC)	8

Figure 4-2 : Channel 1 Register Set 1

Register Set 2 is accessible if Bit7 of the Line Control Register (LCR) (Offset 0x07) is set to ’1’.

The Enhance Feature Register, Xon-1/-2 and Xoff-1/-2 registers are only accessible when the Line Control Register is set to 0xBF.

Offset in IP I/O Space	Read / Write	Size (Bit)	Comment
0x01	LSB of Divisor Latch	8	LCR bit-7 set to ‘1’
0x03	MSB of Divisor Latch	8	LCR bit-7 set to ‘1’
0x05	Enhanced Feature Register (EFR)	8	LCR set to 0xBF
0x07	Line Control Register (LCR)	8	Always accessible
0x09	Xon-1 Word	8	LCR set to 0xBF
0x0B	Xon-2 Word	8	LCR set to 0xBF
0x0D	Xoff-1 Word	8	LCR set to 0xBF
0x0F	Xoff-2 Word	8	LCR set to 0xBF

Figure 4-3 : Channel 1 Register Set 2

4.1.2 Channel 2 Register Set

After reset Register Set 1 is selected.

Register Set 1 is accessible if Bit7 of the Line Control Register (LCR) (Offset 0x17) is set to ’0’.

The special register FIFORDY1 is accessible within this register set.

Offset in IP I/O Space	Read Mode	Write Mode	Size (Bit)
0x11	Receive Holding Register (RHR)	Transmit Holding Register (THR)	8
0x13	Interrupt Enable Register (IER)	Interrupt Enable Register (IER)	8
0x15	Interrupt Status Register (ISR)	FIFO Control Register (FCR)	8
0x17	Line Control Register (LCR)	Line Control Register (LCR)	8
0x19	Modem Control Register (MCR)	Modem Control Register (MCR)	8
0x1B	Line Status Register (LSR)	-	8
0x1D	Modem Status Register (MSR)	-	8
0x1F	FIFORDY1 Register	FIFORDY1 Register	8

Figure 4-4 : Channel 2 Register Set 1

Register Set 2 is accessible if Bit7 of the Line Control Register (LCR) (Offset 0x17) is set to ’1’.

The Enhance Feature Register, Xon-1/-2 and Xoff-1/-2 registers are only accessible when LCR is set to 0xBF.

Offset in IP I/O Space	Read / Write	Size (Bit)	Comment
0x11	LSB of Divisor Latch	8	LCR bit-7 set to ‘1’
0x13	MSB of Divisor Latch	8	LCR bit-7 set to ‘1’
0x15	Enhanced Feature Register (EFR)	8	LCR set to 0xBF
0x17	Line Control Register (LCR)	8	Always accessible
0x19	Xon-1 Word	8	LCR set to 0xBF
0x1B	Xon-2 Word	8	LCR set to 0xBF
0x1D	Xoff-1 Word	8	LCR set to 0xBF
0x1F	Xoff-2 Word	8	LCR set to 0xBF

Figure 4-5 : Channel 2 Register Set 2

4.1.3 Channel 3 Register Set

After reset Register Set 1 is selected.

Register Set 1 is accessible if Bit7 of the Line Control Register (LCR) (Offset 0x27) is set to ’0’.

Offset in IP I/O Space	Read Mode	Write Mode	Size (Bit)
0x21	Receive Holding Register (RHR)	Transmit Holding Register (THR)	8
0x23	Interrupt Enable Register (IER)	Interrupt Enable Register (IER)	8
0x25	Interrupt Status Register (ISR)	FIFO Control Register (FCR)	8
0x27	Line Control Register (LCR)	Line Control Register (LCR)	8
0x29	Modem Control Register (MCR)	Modem Control Register (MCR)	8
0x2B	Line Status Register (LSR)	-	8
0x2D	Modem Status Register (MSR)	-	8
0x2F	Not used	Not used	8

Figure 4-6 : Channel 3 Register Set 1

Register Set 2 is accessible if Bit7 of the Line Control Register (LCR) (Offset 0x27) is set to ’1’.

The Enhance Feature Register, Xon-1/-2 and Xoff-1/-2 registers are accessible only when LCR is set to 0xBF.

Offset in IP I/O Space	Read / Write	Size (Bit)	Comment
0x21	LSB of Divisor Latch	8	LCR bit-7 set to ‘1’
0x23	MSB of Divisor Latch	8	LCR bit-7 set to ‘1’
0x25	Enhanced Feature Register (EFR)	8	LCR set to 0xBF
0x27	Line Control Register (LCR)	8	Always accessible
0x29	Xon-1 Word	8	LCR set to 0xBF
0x2B	Xon-2 Word	8	LCR set to 0xBF
0x2D	Xoff-1 Word	8	LCR set to 0xBF
0x2F	Xoff-2 Word	8	LCR set to 0xBF

Figure 4-7 : Channel 3 Register Set 2

4.1.4 Channel 4 Register Set

After reset Register Set 1 is selected.

Register Set 1 is accessible if Bit7 of the Line Control Register (LCR) (Offset 0x37) is set to ’0’.

Offset in IP I/O Space	Read Mode	Write Mode	Size (Bit)
0x31	Receive Holding Register (RHR)	Transmit Holding Register (THR)	8
0x33	Interrupt Enable Register (IER)	Interrupt Enable Register (IER)	8
0x35	Interrupt Status Register (ISR)	FIFO Control Register (FCR)	8
0x37	Line Control Register (LCR)	Line Control Register (LCR)	8
0x39	Modem Control Register (MCR)	Modem Control Register (MCR)	8
0x3B	Line Status Register (LSR)	-	8
0x3D	Modem Status Register (MSR)	-	8
0x3F	Not used	Not used	8

Figure 4-8 : Channel 4 Register Set 1

Register Set 2 is accessible if Bit7 of the Line Control Register (LCR) (Offset 0x37) is set to ’1’.

The Enhance Feature Register, Xon-1/-2 and Xoff-1/-2 registers are accessible only when LCR is set to 0xBF.

Offset in IP I/O Space	Read / Write	Size (Bit)	Comment
0x31	LSB of Divisor Latch	8	LCR bit-7 set to ‘1’
0x33	MSB of Divisor Latch	8	LCR bit-7 set to ‘1’
0x35	Enhanced Feature Register (EFR)	8	LCR set to 0xBF
0x37	Line Control Register (LCR)	8	Always accessible
0x39	Xon-1 Word	8	LCR set to 0xBF
0x3B	Xon-2 Word	8	LCR set to 0xBF
0x3D	Xoff-1 Word	8	LCR set to 0xBF
0x3F	Xoff-2 Word	8	LCR set to 0xBF

Figure 4-9 : Channel 4 Register Set 2

4.1.5 Channel 5 Register Set

After reset Register Set 1 is selected.

Register Set 1 is accessible if Bit7 of the Line Control Register (LCR) (Offset 0x47) is set to ’0’.

Offset in IP I/O Space	Read Mode	Write Mode	Size (Bit)
0x41	Receive Holding Register (RHR)	Transmit Holding Register (THR)	8
0x43	Interrupt Enable Register (IER)	Interrupt Enable Register (IER)	8
0x45	Interrupt Status Register (ISR)	FIFO Control Register (FCR)	8
0x47	Line Control Register (LCR)	Line Control Register (LCR)	8
0x49	Modem Control Register (MCR)	Modem Control Register (MCR)	8
0x4B	Line Status Register (LSR)	-	8
0x4D	Modem Status Register (MSR)	-	8
0x4F	Not used	Not used	8

Figure 4-10: Channel 5 Register Set 1

Register Set 2 is accessible if Bit7 of the Line Control Register (LCR) (Offset 0x47) is set to ’1’.

The Enhance Feature Register, Xon-1/-2 and Xoff-1/-2 registers are accessible only when LCR is set to 0xBF.

Offset in IP I/O Space	Read / Write	Size (Bit)	Comment
0x41	LSB of Divisor Latch	8	LCR bit-7 set to ‘1’
0x43	MSB of Divisor Latch	8	LCR bit-7 set to ‘1’
0x45	Enhanced Feature Register (EFR)	8	LCR set to 0xBF
0x47	Line Control Register (LCR)	8	Always accessible
0x49	Xon-1 Word	8	LCR set to 0xBF
0x4B	Xon-2 Word	8	LCR set to 0xBF
0x4D	Xoff-1 Word	8	LCR set to 0xBF
0x4F	Xoff-2 Word	8	LCR set to 0xBF

Figure 4-11: Channel 5 Register Set 2

4.1.6 Channel 6 Register Set

After reset Register Set 1 is selected.

Register Set 1 is accessible if Bit7 of the Line Control Register (LCR) (Offset 0x57) is set to ’0’.

The special register FIFORDY2 is accessible within this register set.

Offset in IP I/O Space	Read Mode	Write Mode	Size (Bit)
0x51	Receive Holding Register (RHR)	Transmit Holding Register (THR)	8
0x53	Interrupt Enable Register (IER)	Interrupt Enable Register (IER)	8
0x55	Interrupt Status Register (ISR)	FIFO Control Register (FCR)	8
0x57	Line Control Register (LCR)	Line Control Register (LCR)	8
0x59	Modem Control Register (MCR)	Modem Control Register (MCR)	8
0x5B	Line Status Register (LSR)	-	8
0x5D	Modem Status Register (MSR)	-	8
0x5F	FIFORDY2	FIFORDY2	8

Figure 4-12: Channel 6 Register Set 1

Register Set 2 is accessible if Bit7 of the Line Control Register (LCR) (Offset 0x57) is set to ’1’.

The Enhance Feature Register, Xon-1/-2 and Xoff-1/-2 registers are accessible only when LCR is set to 0xBF.

Offset in IP I/O Space	Read / Write	Size (Bit)	Comment
0x51	LSB of Divisor Latch	8	LCR bit-7 set to ‘1’
0x53	MSB of Divisor Latch	8	LCR bit-7 set to ‘1’
0x55	Enhanced Feature Register (EFR)	8	LCR set to 0xBF
0x57	Line Control Register (LCR)	8	Always accessible
0x59	Xon-1 Word	8	LCR set to 0xBF
0x5B	Xon-2 Word	8	LCR set to 0xBF
0x5D	Xoff-1 Word	8	LCR set to 0xBF
0x5F	Xoff-2 Word	8	LCR set to 0xBF

Figure 4-13: Channel 6 Register Set 2

4.1.7 Channel 7 Register Set

After reset Register Set 1 is selected.

Register Set 1 is accessible if Bit7 of the Line Control Register (LCR) (Offset 0x67) is set to ’0’.

Offset in IP I/O Space	Read Mode	Write Mode	Size (Bit)
0x61	Receive Holding Register (RHR)	Transmit Holding Register (THR)	8
0x63	Interrupt Enable Register (IER)	Interrupt Enable Register (IER)	8
0x65	Interrupt Status Register (ISR)	FIFO Control Register (FCR)	8
0x67	Line Control Register (LCR)	Line Control Register (LCR)	8
0x69	Modem Control Register (MCR)	Modem Control Register (MCR)	8
0x6B	Line Status Register (LSR)	-	8
0x6D	Modem Status Register (MSR)	-	8
0x6F	Not used	Not used	8

Figure 4-14: Channel 7 Register Set 1

Register Set 2 is accessible if Bit7 of the Line Control Register (LCR) (Offset 0x67) is set to ’1’.

The Enhance Feature Register, Xon-1/-2 and Xoff-1/-2 registers are accessible only when LCR is set to 0xBF.

Offset in IP I/O Space	Read / Write	Size (Bit)	Comment
0x61	LSB of Divisor Latch	8	LCR bit-7 set to ‘1’
0x63	MSB of Divisor Latch	8	LCR bit-7 set to ‘1’
0x65	Enhanced Feature Register (EFR)	8	LCR set to 0xBF
0x67	Line Control Register (LCR)	8	Always accessible
0x69	Xon-1 Word	8	LCR set to 0xBF
0x6B	Xon-2 Word	8	LCR set to 0xBF
0x6D	Xoff-1 Word	8	LCR set to 0xBF
0x6F	Xoff-2 Word	8	LCR set to 0xBF

Figure 4-15: Channel 7 Register Set 2

4.1.8 Channel 8 Register Set

After reset Register Set 1 is selected.

Register Set 1 is accessible if Bit7 of the Line Control Register (LCR) (Offset 0x77) is set to ’0’.

Offset in IP I/O Space	Read Mode	Write Mode	Size (Bit)
0x71	Receive Holding Register (RHR)	Transmit Holding Register (THR)	8
0x73	Interrupt Enable Register (IER)	Interrupt Enable Register (IER)	8
0x75	Interrupt Status Register (ISR)	FIFO Control Register (FCR)	8
0x77	Line Control Register (LCR)	Line Control Register (LCR)	8
0x79	Modem Control Register (MCR)	Modem Control Register (MCR)	8
0x7B	Line Status Register (LSR)	-	8
0x7D	Modem Status Register (MSR)	-	8
0x7F	Not used	Not used	8

Figure 4-16: Channel 8 Register Set 1

Register Set 2 is accessible if Bit7 of the Line Control Register (LCR) (Offset 0x77) is set to ’1’.

The Enhance Feature Register, Xon-1/-2 and Xoff-1/-2 registers are accessible only when LCR is set to 0xBF.

Offset in IP I/O Space	Read / Write	Size (Bit)	Comment
0x71	LSB of Divisor Latch	8	LCR bit-7 set to ‘1’
0x73	MSB of Divisor Latch	8	LCR bit-7 set to ‘1’
0x75	Enhanced Feature Register (EFR)	8	LCR set to 0xBF
0x77	Line Control Register (LCR)	8	Always accessible
0x79	Xon-1 Word	8	LCR set to 0xBF
0x7B	Xon-2 Word	8	LCR set to 0xBF
0x7D	Xoff-1 Word	8	LCR set to 0xBF
0x7F	Xoff-2 Word	8	LCR set to 0xBF

Figure 4-17: Channel 8 Register Set 2

4.2 Special Registers

4.2.1 Interrupt Vector Register (Offset 0x0F)

The Interrupt Vector Register INTVEC is a byte wide read/write register. It is located within the Register Set 1 of Channel 1.

Each Quad-UART controller generates an individual interrupt (Quad-UART Controller 1 for channel 1-4 and Quad-UART Controller 2 for channel 5-8). The Interrupt Vector Register is shared between both interrupt sources.

Bit	Symbol	Description	Access	Reset Value
7:1		Interrupt vector (loaded by software)	R/W	all 0
0		In I/O space always read as '1'. For INT vector cycle : Read as '0' for an interrupt from controller 1 (channel 1-4) Read as '1' for an interrupt from controller 2 (channel 5-8) Example : INTVEC loaded with 0x60 Controller 1 will create interrupt vector 0x60 Controller 2 will create interrupt vector 0x61	R	

Figure 4-18: Interrupt Vector Register INTVEC

Quad-UART Controller 1 (channels 1-4) generates interrupts on IP interrupt request line INTREQ0#.

Quad-UART Controller 2 (channels 5-8) generates interrupts on IP interrupt request line INTREQ1#.

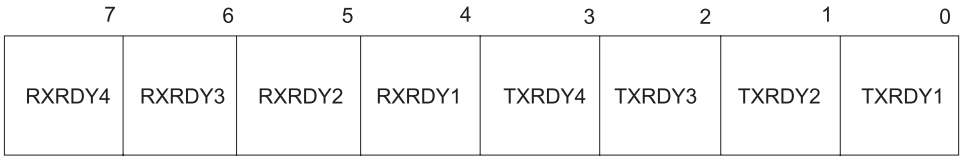
4.2.2 FIFO Ready Status Register 1 (Channel 1-4) (Offset 0x1F)

The FIFO Ready Status Register 1 (FIFORDY1) is a byte wide read only register. It is located within Register Set 1 of Channel 2.

FIFORDY1 covers the FIFO status for Quad-UART Controller 1 (Channels 1-4).

If a serial channel is in FIFO mode (FIFO Control Register bit 0 set to '1') and bit 3 of the FIFO Control Register is set to '1', the corresponding TxRdy-bit of the FIFORDY1 register will be read as '1' if the transmit FIFO is completely full. It will be read as '0' if one or more transmit FIFO locations are empty.
The corresponding RxRdy-bit of the FIFORDY1 register will become '0' when the FIFO trigger level has been reached. The RxRdy-bit of the FIFORDY1 register will be read as '1' when there are no more characters in the receive FIFO.

If a serial channel is in FIFO mode (FIFO Control Register bit 0 set to '1') and bit 3 of the FIFO Control Register is set to '0' or if the FIFO mode is disabled, the TxRdy-bit of the FIFORDY1 register will be read as '0' when there are no characters in the transmit FIFO or transmit holding register. The TxRdy-bit of the FIFORDY1 register will be read as '1' after the first character is loaded into the transmit register.
The corresponding RxRdy-bit of the FIFORDY1 register will be read as '0' when there is at least 1 character in the receive FIFO. The RxRdy-bit of the FIFORDY1 register will be read as '1' when there are no more characters in the receiver.



Bit	Symbol	Description	Access	Reset Value
7	RXRDY4	RXRDY Channel 1-4	R	1111
6	RXRDY3			
5	RXRDY2			
4	RXRDY1			
3	TXRDY4	TXRDY Channel 1-4	R	0000
2	TXRDY3			
1	TXRDY2			
0	TXRDY1			

Figure 4-19: FIFO Ready Status Register 1 (FIFORDY1)

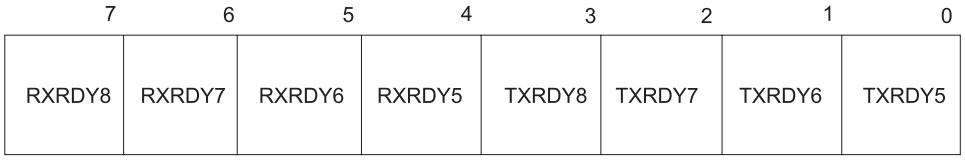
4.2.3 FIFO Ready Status Register 2 (Channel 5-8) (Offset 0x5F)

The FIFO Ready Status Register 2 (FIFORDY2) is a byte wide read only register. It is located within Register Set 1 of Channel 6.

FIFORDY2 covers the FIFO status for Quad-UART Controller 2 (Channels 5-8).

If a serial channel is in FIFO mode (FIFO Control Register bit 0 set to '1') and bit 3 of the FIFO Control Register is set to '1', the corresponding TxRdy-bit of the FIFORDY2 register will be read as '1' if the transmit FIFO is completely full. It will be read as '0' if one or more transmit FIFO locations are empty.
The corresponding RxRdy-bit of the FIFORDY2 register will become '0' when the FIFO trigger level has been reached. The RxRdy-bit of the FIFORDY2 register will be read as '1' when there are no more characters in the receive FIFO.

If a serial channel is in FIFO mode (FIFO Control Register bit 0 set to '1') and bit 3 of the FIFO Control Register is set to '0' or if the FIFO mode is disabled, the TxRdy-bit of the FIFORDY2 register will be read as '0' when there are no characters in the transmit FIFO or transmit holding register. The TxRdy-bit of the FIFORDY2 register will be read as '1' after the first character is loaded into the transmit register.
The corresponding RxRdy-bit of the FIFORDY2 register will be read as '0' when there is at least 1 character in the receive FIFO. The RxRdy-bit of the FIFORDY2 register will be read as '1' when there are no more characters in the receiver.



Bit	Symbol	Description	Access	Reset Value
7	RXRDY8	RXRDY Channel 5-8	R	1111
6	RXRDY7			
5	RXRDY6			
4	RXRDY5			
3	TXRDY8	TXRDY Channel 5-8	R	0000
2	TXRDY7			
1	TXRDY6			
0	TXRDY5			

Figure 4-20: FIFO Ready Status Register 2 (FIFORDY2)

5 Baud Rate Programming

The basic formula of baud rate programming is:

$$BaudRate = 7.3728MHz \div \left((16 \times DIVISOR) \times (1 + 3 \times MCR\_Bit7)\right)$$

The baud rate is programmable individually for each channel.

The divisor value is programmed into the MSB and LSB Divisor Latch Register (Register Set 2 of each channel).

See the note below for programming the MCR (Modem Control Register) Bit 7.

After reset for each channel the MCR Bit7 defaults to '1' and the value of the MSB and LSB Divisor Latch Registers results in a divisor value of 0xFFFF.

Baud Rate MCR Bit 7 = 1	Baud Rate MCR Bit 7 = 0	Divisor
50	200	0x0900
75	300	0x0600
150	600	0x0300
300	1200	0x0180
600	2400	0x00C0
1200	4800	0x0060
2400	9600	0x0030
4800	19.2K	0x0018
7200	28.8K	0x0010
9600	38.4K	0x000C
14.4K	57.6K	0x0008
28.8K	115.2K	0x0004
38.4K	153.6K	0x0003
57.6K	230.4K	0x0002
115.2K	460.8K	0x0001

Figure 5-1 : Baud Rate Programming Table

The highest data rate of the TIP866-10 is 115.2Kbaud because of the used RS232 Line Drivers and Receivers.

For data rates higher than 115.2Kbaud, MCR bit 7 must be set to ‘0’ (422 and TTL versions only).

The MCR (Modem Control Register) Bits 5-7 must be enabled for modifying by setting EFR (Enhanced Feature Register) Bit 4.

These steps should be used to modify MCR Bit 7:

- **Write 0xBF to LCR register (Enable access to EFR register)**
- **Set EFR register Bit 4 to '1' (Enable modification of MCR Bits 5-7)**
- **Modify MCR Bit 7**
- **Set EFR register Bit 4 to '0' (Latch MCR setting)**
- **Write normal operation byte value to LCR register**

6 Pin Assignment – I/O Connector

6.1 50 pin I/O connector 232 and 422 IPs

Pin	Signal 232 Signal TTL	Comment 232	Comment TTL
1	GND	Signal Ground	Signal Ground
2	TXD1	Active low	Active high
3	RXD1	Active low	Active high
4	RTS1	Active high	Active low
5	CTS1	Active high	Active low
6	GND	Signal Ground	Signal Ground
7	TXD2	Active low	Active high
8	RXD2	Active low	Active high
9	RTS2	Active high	Active low
10	CTS2	Active high	Active low
11	GND	Signal Ground	Signal Ground
12	TXD3	Active low	Active high
13	RXD3	Active low	Active high
14	RTS3	Active high	Active low
15	CTS3	Active high	Active low
16	GND	Signal Ground	Signal Ground
17	TXD4	Active low	Active high
18	RXD4	Active low	Active high
19	RTS4	Active high	Active low
20	CTS4	Active high	Active low
21	GND	Signal Ground	Signal Ground
22	TXD5	Active low	Active high
23	RXD5	Active low	Active high
24	RTS5	Active high	Active low
25	CTS5	Active high	Active low
26	GND	Signal Ground	Signal Ground
27	TXD6	Active low	Active high
28	RXD6	Active low	Active high
29	RTS6	Active high	Active low
30	CTS6	Active high	Active low
31	GND	Signal Ground	Signal Ground
32	TXD7	Active low	Active high
33	RXD7	Active low	Active high
34	RTS7	Active high	Active low
35	CTS7	Active high	Active low
36	GND	Signal Ground	Signal Ground
37	TXD8	Active low	Active high

Pin	Signal 232 Signal TTL	Comment 232	Comment TTL
38	RXD8	Active low	Active high
39	RTS8	Active high	Active low
40	CTS8	Active high	Active low
41	GND	Supply for Transition Module	Supply for Transition Module
42	+5V	Supply for Transition Module	Supply for Transition Module
43	DCD1	Active high	Active low
44	DTR1	Active high	Active low
45	RI1	Active high	Active low
46	DSR1	Active high	Active low
47	DCD2	Active high	Active low
48	DTR2	Active high	Active low
49	RI2	Active high	Active low
50	DSR2	Active high	Active low

Figure 6-1 : Pin Assignment I/O Connector 232 and TTL IPs

6.2 50 pin I/O connector 422 IPs

Pin	Signal 422	Comment
1	GND	Signal Ground
2	TxD1-	RS422-
3	TxD1+	RS422+
4	RxD1-	RS422-
5	RxD1+	RS422+
6	GND	Signal Ground
7	TxD2-	RS422-
8	TxD2+	RS422+
9	RxD2-	RS422-
10	RxD2+	RS422+
11	GND	Signal Ground
12	TxD3-	RS422-
13	TxD3+	RS422+
14	RxD3-	RS422-
15	RxD3+	RS422+
16	GND	Signal Ground
17	TxD4-	RS422-
18	TxD4+	RS422+
19	RxD4-	RS422-
20	RxD4+	RS422+
21	GND	Signal Ground
22	TxD5-	RS422-
23	TxD5+	RS422+
24	RxD5-	RS422-
25	RxD5+	RS422+
26	GND	Signal Ground
27	TxD6-	RS422-
28	TxD6+	RS422+
29	RxD6-	RS422-
30	RxD6+	RS422+
31	GND	Signal Ground
32	TxD7-	RS422-
33	TxD7+	RS422+
34	RxD7-	RS422-
35	RxD7+	RS422+
36	GND	Signal Ground
37	TxD8-	RS422-
38	TxD8+	RS422+
39	RxD8-	RS422-
40	RxD8+	RS422+

Pin	Signal 422	Comment
41	GND	Signal Ground
42-50	N.C.	No connection

Figure 6-2 : Pin Assignment I/O Connector 422 IPs

On board signal termination between RxD+ and RxD- is 120 ohms for each channel.