IP-Opto Interrupter

Eight optically isolated, digitally filtered,
programmable input/interrupt channels
IndustryPack®

User Manual

Revision v
Corresponding Hardware: Revision A

IP-Opto Interrupter

Eight optically isolated, digitally filtered, programmable input and interrupt channels IndustryPack®

The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

GreenSpring's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of GreenSpring Computers, Inc.

This product has been designed to operate with IndustryPack carriers and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.

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Product Description

IP-Opto Interrupter provides eight identical digital input channels. Each channel provides independent optical isolation and digital filtering. The input channels may be read directly, or they may be programmed to generate an interrupt.

Typical inputs are mechanical switches, optical switches, or external voltages. IP-Opto Interrupter is ideally suited to critical inputs, such as emergency off switches, mechanical limit detectors, and deadman switches. It can directly detect the presence of external power supplies or monitor digital safety sensors, such as pressure sensors or tension gauges.

IP-Opto Interrupter is designed to provide a particularly effective and uniform way for external events to interrupt the host. The IP is programmed via six byte-wide registers. With the exception of the vector register, each bit of each register corresponds directly with the associated input channel. This uniform programming interface simplifies application software. Any number of channels may be programmed simultaneously. Single, simultaneous, or overlapped input interrupts are easily handled.

A block diagram of the IP-Opto Interrupter is shown in Figure 1 below.

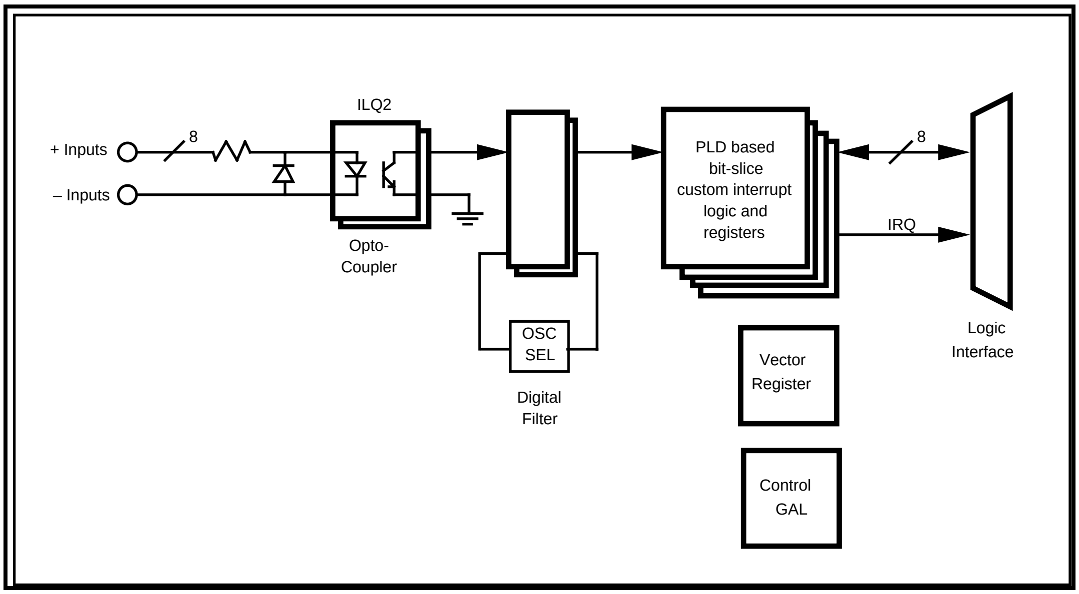

Figure 1 Simplified Block Diagram of IP-Opto Interrupter

Input channels may be individually masked (to not produce an interrupt) or programmed to interrupt on either the rising or falling edge. Two levels of interrupt latch logic are used to prevent any possible occurrence of "lost" interrupts. Input transitions may occur before, during or after an interrupt service routine without danger of losing an interrupt. Similarly, input conditions may be steady state (DC), slow edges, or short pulses. The programmer does not need to know the pulse width (beyond the debounce time) to properly program the IP-Opto Interrupter. Examples of programs are shown later in this manual.

All registers are readable as well as writable to further simplify programming. Bit set and bit clear instructions may be executed directly to affect only a single channel, if desired. Readable registers simplify debugging as well as the interrupt routines themselves.

Optical Isolation

Eight independent optical isolation circuits isolate each input channel from the host's digital logic and from each other. Each channel has a positive and negative input connection. The input circuitry detects a current of the proper polarity. Input resistors are provided on the IP to convert external voltages to the required current to drive the opto-coupler.

Order Options are available for input ranges from 2.2 to 32 volts, plus RS-422 compatible input Higher voltages may be supported with external resistors. Five different input voltage ranges are offered. Order Options and the usable operating ranges are shown below in Figure 2.

Order Option	Typical Input	Maximum OFF Input	Minimum ON Input	Maximum Continuous Input
–RS422	RS-422 driver	0.6 V	1.6 V	40 mA
–Logic	3.5 V	0.9 V	2.2 V	11 V
–STD	5 V	1.0 V	3.0 V	15 V
–12V	12 V	1.6 V	7 V	22 V
–24V	24 V	2.1 V	9 V	32 V

Note: –STD is the factory default if no order option is specified.

Figure 2 Input Range Options

The usable input voltage ranges of the different order options overlap. Selecting the correct order option is primarily a matter of optimizing the noise immunity and minimizing the power dissipation. The "–RS422" range should be specified for compatibility with direct connection to RS-422 or RS-485 drivers.

The optical isolation circuit may be connected to mechanical or optical switches, TTL or CMOS level digital sensors, relays, digital RS-422 drivers, or power supplies. Switches require an external power supply. Digital circuits, drivers and sensors power the input circuit directly. See the section below, User Wiring, for more information.

Digital Filtering

A digital filter stage is provided for input switch debouncing. Three debounce times are pin (shunt) selectable in groups of four channels. The available debounce times are two milliseconds, 20 milliseconds, and 25 microseconds. Two milliseconds is standard. 20 millisecond debounce time is suitable for large mechanical switches such as train sensors or crane limit switches. The 25 microsecond time is provided for cases where minimum delay from the external event to the interrupt is desired and no mechanical contact debouncing is required.

Digital debouncing is accomplished by provided four consecutive flip-flop stages, each clocked by a local oscillator. All four stages must be at the same binary level for the output of the debounce circuit to change. The digital filtering provides significant noise immunity as well as providing the switch debounce function. More information about the digital filtering is available in the IP-Opto Interrupter Engineering Kit.

Interrupt Logic

Input and interrupt logic is implemented in CMOS programmable logic devices (PLDs). The implementation uses four identically programmed parts organized as four two-bit "slices." The PLDs implement all the registers except the vector register.

All host to IP communication is byte-wide. Six registers are used to read, program and respond to interrupts.

For detailed information refer to the Addressing and Programming sections below.

VMEbus Addressing

IP-Opto Interrupter implements six byte-wide registers. These registers, their access modes, addresses, and reset values are shown below in Figure 3. See the next section for Nubus addressing.

Register Name	Access Modes	Address (hex)	Value after Reset
Data	read only	01	
Interrupt Polarity	read/write	03	Reset to FF
Interrupt Disable	read/write	05	Reset to FF
Clear Interrupt	write only	07	
Pending Interrupt	read only	09	Reset to 00
Vector	read/write	0B	Reset to FF

Figure 3 VMEbus Register Map

See the Programming section below for more information on register usage.

NuBus Addressing

IP-Opto Interrupter implements six byte-wide registers. These registers, their access modes, addresses, and reset values are shown below in Figure 4. See the previous section for VMEbus addressing.

Register Name	Access Modes	RM1260 Address (hex)	RM1270 Address (hex)	Reset Value
Data	read only	01	03	
Interrupt Polarity	read/write	05	07	Reset to FF
Interrupt Disable	read/write	09	0B	Reset to FF
Clear Interrupt	write only	0D	0F	
Pending Interrupt	read only	11	13	Reset to 00
Vector	read/write	15	17	Reset to FF

Figure 4 NuBus Register Map

See the Programming section below for more information on register usage.

I/O Wiring

This section gives the pin assignments and wiring recommendations for IP-Interrupter.

The pin numbers given in Figure 5 below correspond to numbers on the 50-pin IndustryPack I/O connector, to the wires on a 50-pin flat cable plugged into a standard IP carrier board, and to the screw terminal numbers on the IP-Terminal block.

P IN Number	Signal
1	+ IN1
2	– IN1
3	+ IN2
4	– IN2
5	+ IN3
6	– IN3
7	+ IN4
8	– IN4
9	+ IN5
10	– IN5
11	+ IN6
12	– IN6
13	+ IN7
14	– IN7
15	+ IN8
16	– IN8
17 – 48	no connection
49	+5 via 100Ω
50	GND

Figure 5 I/O Pin Assignment

Each input pair is optically isolated from the logic circuitry. Each input pair is independent of the other pairs.

The positive polarity pin (shown as a + in Figure 5) should be more positive than the negative polarity pin (shown as a – in Figure 5). The shown polarity must be observed to receive a logic one (ON) signal. Reverse polarity of voltages up to the maximum continuous input voltage will not damage the IndustryPack, but the input will be read as logic zero (OFF). RS-422 drivers could be directly connected, + to + and – to –.

Maximum permitted differential voltage between any two pins on the interface and also between any pin on the interface and the logic ground is 60 volts. This limitation is due to trace separation on the IndustryPack PCB.

Figure 6 on the next page shows the input resistors used for each of the five available order options. The usable input voltage ranges overlap considerably. Multiple ranges are offered to maximize noise immunity and minimize local power dissipation. Standard 8-pin four resistor networks are used. Users may substitute alternate value resistors for special applications. Higher voltages may be used by adding external series resistors.

Order Option	Typical Input	Series Resistance ohms
–RS422	RS422 driver	100 Ω
–Logic	3.5 V	750 Ω
–STD	5 V	1500 Ω
–12V	12 V	4700 Ω
–24V	24 V	8200 Ω

Figure 6 Input Range Resistor Values

The 100**Ω** series resistor is well matched to a typical RS-422 driver This presents and AC termination of close to 100**Ω**, with a typical V_{low} of 0.5 volt and V_{high} of 2.5 volt, and typical driver current of about 10 mA. No other termination resistor should be used. In the case of option-RS422 IP-Opto Interrupters being connected to RS-422 drivers, the user need not be concerned with checking minimum or maximum voltages for assured compatibility.

The optical couplers are current mode devices. The input resistors convert an external voltage to a current. Figure 7 below shows the current characteristics of the optical couplers as implemented. These parameters may be used to compute alternate or external resistor values.

Maximum OFF input current	200 µA
Minimum ON input current	1 mA
Maximum continuous per channel power	125 mW (all channels driven)

Figure 7 Input Characteristics

To guarantee that the IP-Opto Coupler detects inputs as OFF, either the input voltage must be below the "maximum OFF" shown in Figure 8 on the next page, or the input current must be below the "maximum OFF" shown in Figure 7 above. The voltage number is typically used when interfacing to voltage output circuits. The current number should be checked against leakage current specifications when interfacing to electronic switches or pass transistors.

The maximum continuous per channel power is 125 mW. This is the specification that limits the maximum continuous voltage applied to the inputs. The maximum continuous power per channel if only one channel is driven is 250 mW. The maximum instantaneous power per channel is 1000 mW. The maximum applied voltage across any input pair should never exceed 60 volts. Users may exceed the maximum input voltages given in Figure 8 on the next page only if they observe all power and voltage limitations given in this paragraph. Exceeding the maximum continuous voltage rating is not recommended however, since it is difficult to determine in advance what changes may occur in the field or what failure modes of external wiring or sensors may occur.

Order Option	Typical Input	Maximum OFF Input	Minimum ON Input	Maximum Continuous Input
–RS422	RS-422 driver	0.6 V	1.6 V	40 mA
–Logic	3.5 V	0.9 V	2.2 V	11 V
–STD	5 V	1.0 V	3.0 V	15 V
–12V	12 V	1.6 V	7 V	22 V
–24V	24 V	2.1 V	9 V	32 V

Note: –STD is the factory default if no order option is specified.

Figure 8 Input Voltage Ranges

See also your User Manual for your IP Carrier board for more information about cabling.

Applications

Five basic wiring examples are shown in Figure 9 on the next page.

A logic level input may be applied directly to the + input, as shown in Plan A in Figure 9. Note that the "–Logic" order option is required in this configuration.

A preferred wiring arrangement is shown in Plan B. In this case the logic level of the input is read inverted by the IP-Opto Interrupter. Most logic families have more sink current capability and more voltage accuracy when driving low than when driving high. Plan B takes advantage of this fact to deliver better noise immunity. The "–STD" IP-Opto Interrupter may be used in Plan B, in place of the "–Logic" order option, if desired.

Plan C shows typical wiring for a mechanical or optical switch. If a voltage higher than the 5 volts shown is used, then other input range options may be preferable.

Plan D shows direct monitoring of positive voltage sources. Negative voltages may be similarly monitored by connecting the external GND to the + input, and the negative voltage to the – input.

Plan E shows direct connection to an RS-422 driver. The IP-Opto Interrupter provides convenient, fully isolated monitoring of remote digital information. A reverse polarity diode on each input (not shown) provides for current conduction through the 100Ω resistor when the RS-422 driver is in the opposite state. This provides for symmetric and balanced signaling. RS-422 drivers are reliable at distances at up to 2000 feet.

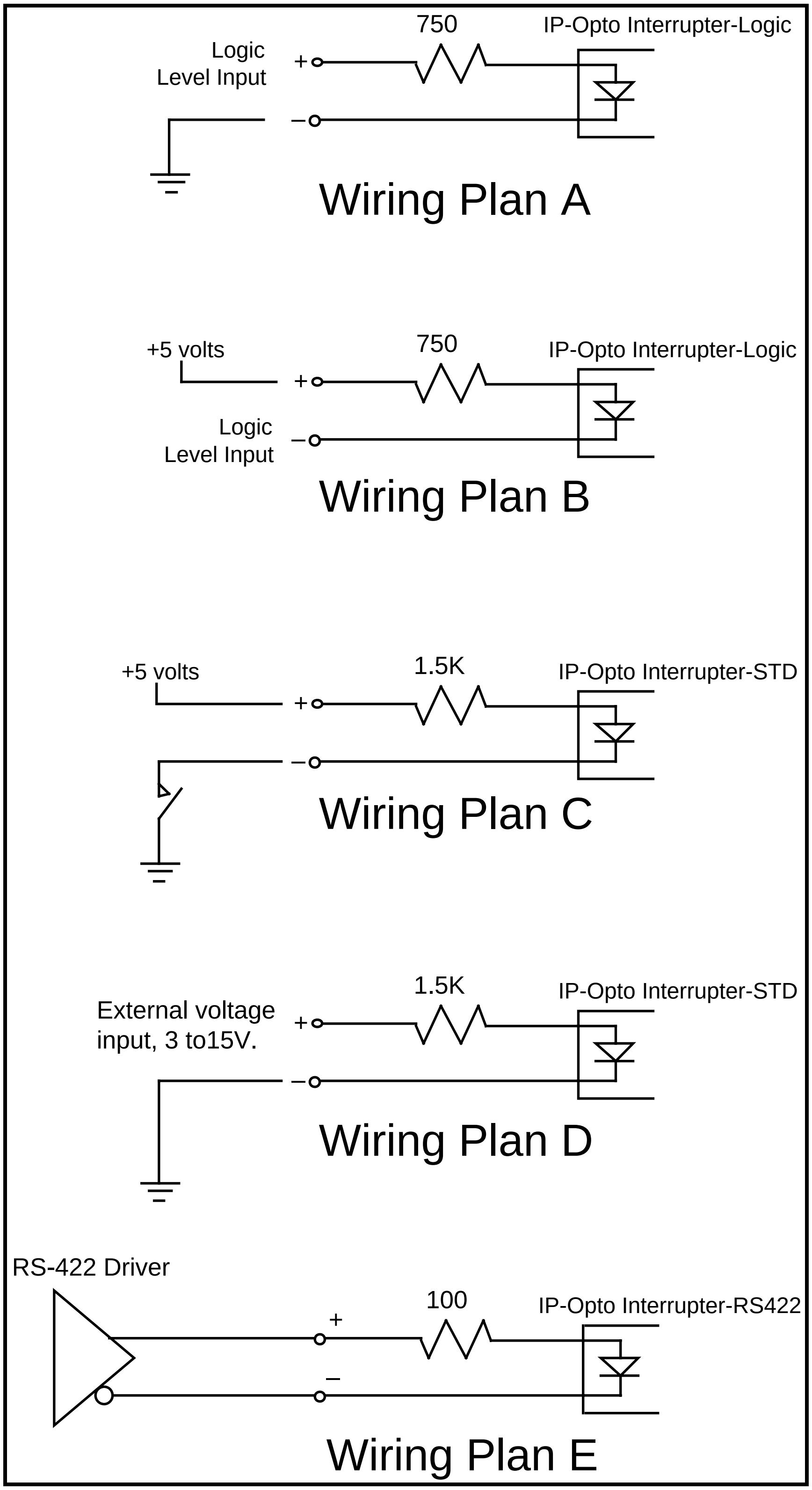

Figure 9 Basic Wiring Options

External resistors or zener diodes may be added to detect special conditions. A simple series zener diode, shown below in Figure 10, may be used to monitor a power supply. For example, with a 24 volt power supply and an 18 volt zener, a logic zero will be received by the IndustryPack when the power supply falls below 19 volts.

The IP-Opto Interrupter may be programmed to generate an interrupt on a logic one to zero transition. In this way the hardware continuously monitors the power supply with no additional software intervention, generating an interrupt (which may be a non-maskable interrupt) should the power supply begin to fail.

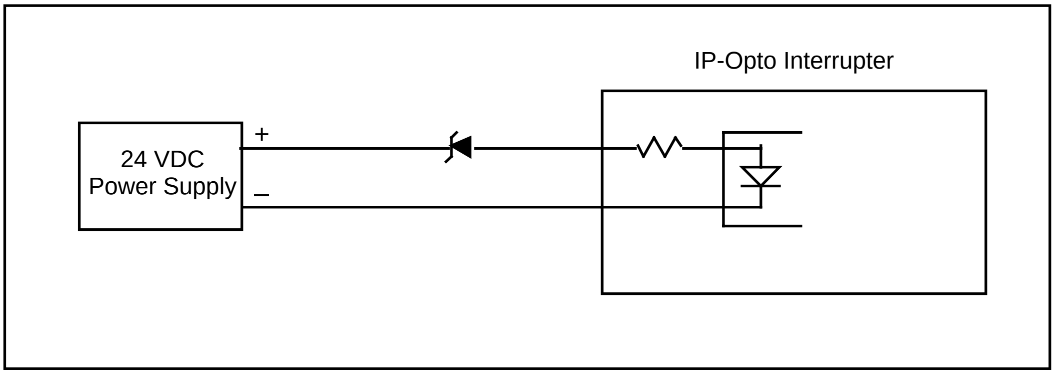

Figure 10 Power Supply Monitoring

Several external components might be used to implement an extremely reliable switch input circuit as shown on the next page in Figure 11. This example circuit detects normal switch operation. It also detects cable shorts or opens. This circuit is desirable in applications such as deadman throttles and safety interlocks. Conventional cable shorting techniques that may be applied to circumvent safety interlocks are detected directly. Intermittent wiring is similarly detected directly. The IP-Opto Interrupter may be programmed to generate interrupts for any combination of state changes.

The various input states are shown following in Figure 12.

GreenSpring Computers cannot assume any liability from the use of the described circuits.

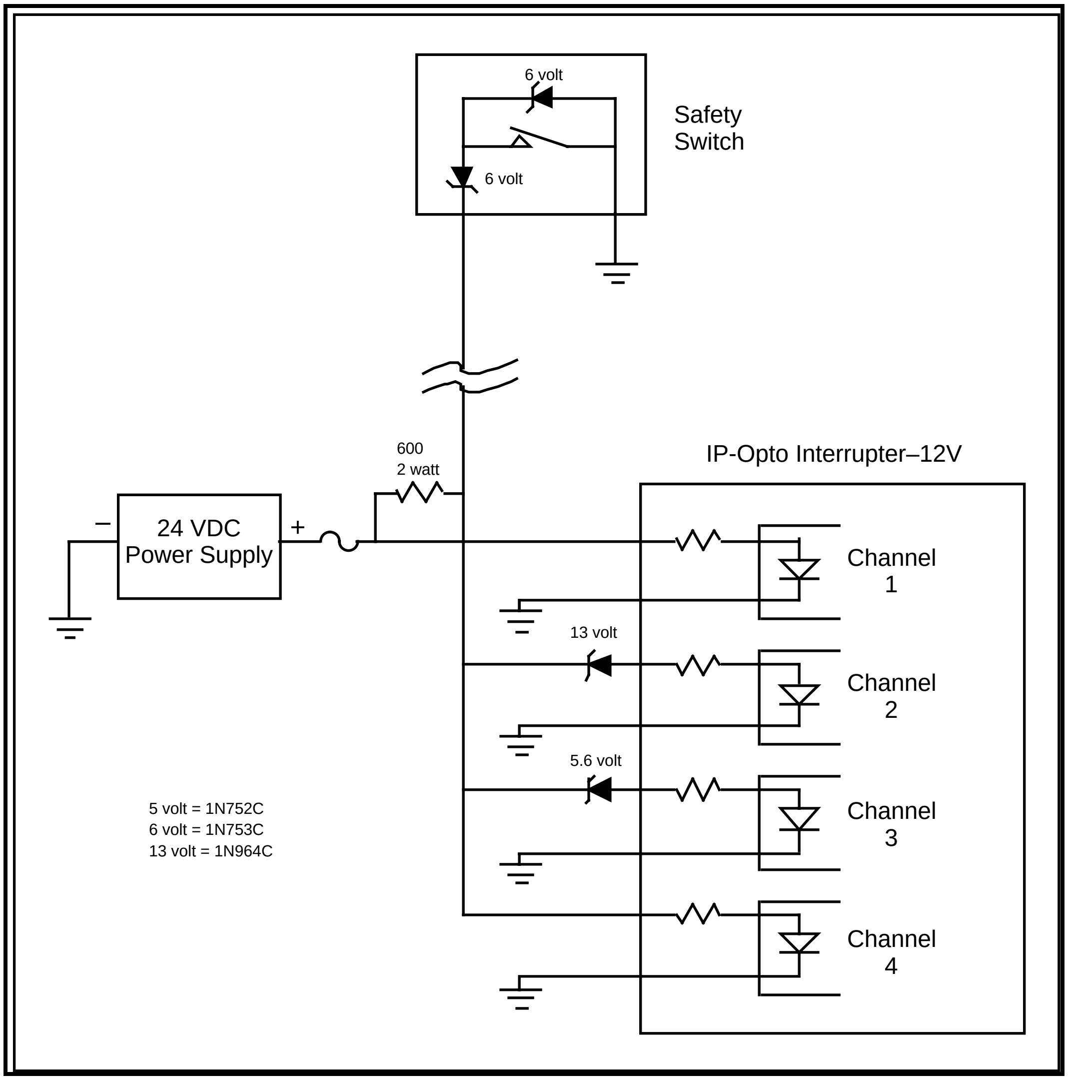

Figure 11 Safety Circuit

Channel 1	Channel 2	Channel 3	Channel 4	Condition
zero	X	X	X	Power Fail/ Fuse Blown
one	one	one	one	Open Cable
one	zero	one	one	Switch Open
one	zero	zero	one	Switch Closed
one	zero	zero	zero	Ground Fault/ Cable Shorted

Figure 12 Input States

IndustryPack Logic Interface Pin Assignment

Figure 13 below gives the pin assignments for the IndustryPack Logic Interface on the IP-Opto Interrupter. Pins marked n/c below are defined by the specification, but not used on IP-Opto Interrupter. See also your User Manual for your IP Carrier board for more information.

GND	GND	1	26
CLK	+5V	2	27
Reset*	R/W*	3	28
D0 IDSel*	4	29	
D1 n/c	5 30		
D2 n/c	6	31	
D3 n/c	7 32		
D4 INTSel*	8	33	
D5 n/c	9 34		
D6 IOSel*	10	35	
D7 n/c	11 36		
n/c	A1	12	37
n/c	n/c	13	38
n/c	A2	14	39
n/c	n/c	15	40
n/c	A3	16	41
n/c	INTReq0*	17	42
n/c	A4	18	43
n/c	n/c	19	44
n/c	A5	20	45
n/c	n/c	21	46
n/c	n/c	22	47
n/c	Ack*	23	48
+5V	n/c	24	49
GND	GND	25	50

Note 1: The no-connect (n/c) signals above are defined by the IndustryPack Logic Interface Specification, but not used by this IP. See the Specification for more information.

Note 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IndustryPack.

Figure 13 Logic Interface Pin Assignment

Programming

IP-Opto Interrupter implements six byte-wide registers. These registers, their access modes, addresses, and reset values were shown previously in Figures 3 and 4. The VMEbus map in Figure 3 is reproduced below as Figure 14 for convenience.

Register Name	Access Modes	Address (hex)	Value after Reset
Data	read only	01	
Interrupt Polarity	read/write	03	Reset to FF
Interrupt Disable	read/write	05	Reset to FF
Clear Interrupt	write only	07	
Pending Interrupt	read only	09	Reset to 00
Vector	read/write	0B	Reset to FF

Figure 14 VMEbus Register Map

Data Register

The map showing correspondence between the bits in the register and the input channels is shown below in Figure 15. This map is used for all registers except the vector register.

Register Bit	Channel Number
0 LSB	1
1	2
2	3
3	4
4	5
5	6
6	7
7 MSB	8

Figure 15 Bit Correspondence to Channels

The data inputs are read after the debounce logic. A logic one corresponds to current flowing in the input channel. A logic zero corresponds to no current flowing in the input channel. No connection to a channel reads as logic zero.

Because of skew in the optical couplers and in the debouncers simultaneous transitions at the IndustryPack's input pins may not necessarily result in simultaneous data or simultaneous interrupts to the host.

Interrupt Polarity Register

The 8-bit Interrupt Polarity Register is used set the polarity of the transition which is to generate an interrupt. Programming any bit to a one sets the polarity to generate an interrupt when the input data changes to logic one. Programming any bit to a zero sets the polarity to generate an interrupt when the input data changes to logic zero. For the IP to actually request an interrupt, the corresponding bit in the Interrupt Disable Register must be zero.

The Interrupt Polarity Register is set to all ones on reset. This is a read/write register. When an interrupt is generated, the host software may wish to read this register to determine whether a rising edge or falling edge just occurred.

The IP's logic monitors writing to this register. If a bit in this register is changed, and the static input on the corresponding channel matches the programmed bit, then the latent interrupt flip-flop for that channel is set. This feature is critical in order to never "lose" an interrupt due to a channel transition that might occur during an interrupt service routine.

(Example: the software reads an input, determines that it is zero, then enables that channel to generate an interrupt on a zero-to-one transition. Between the read and the write, however, the input changed to one. With this special logic, an interrupt is immediately generated—or generated at the end of the current routine if it has interrupts masked. Without this special logic, the input transition would have been lost.)

If the software does not care what the current state of the input channels are and does not wish to get any immediate interrupts, then the procedure is (i) disable interrupts in the processor, (ii) program the IP's Polarity Register, (iii) write to all channels of the Clear Pending Interrupts Register, (iv) enable interrupts in the processor.

Inverting a bit in this register each time the corresponding bit generates an interrupt will result in an interrupt for both rising and trailing edges.

Interrupt Disable Register

The 8-bit Interrupt Disable Register is used to enable or disable interrupts from individual bits. Any number or any combination of channels may be programmed in a single byte write. Programming any bit to a one disables an interrupt from the corresponding input channel. Programming any bit to a zero enables an interrupt from the corresponding input channel.

For the IP to actually request an interrupt, an edge or level must be been for the corresponding channel. Since the IP-Opto Interrupter has a "latent interrupt" latch it is possible to get an interrupt immediately upon clearing any bit in this register.

The Interrupt Disable Register is set to all ones on reset. Thus all channels are disabled from generating interrupts on reset.

Clear Interrupt Register
Pending Interrupt Register

These two 8-bit registers are used to detect and clear pending interrupts from any combination of channels. These two registers both access the same eight pending- interrupt flip-flops. They are arranged as one read-only register—the Pending Interrupt Register, and one write-only register—the Clear Interrupt Register.

The flip-flops that make up these two registers may be set only by a transition on an input channel of the programmed polarity. They may be cleared only by the software by writing to the Clear Interrupt Register.

Reading a one in the Pending Interrupt Register means that the corresponding channel has either an interrupt pending if that channel is enabled, or a "latent" interrupt if that channel is disabled. The difference between a pending and a latent interrupt is that pending interrupts are driving the IP's interrupt request line active. A latent interrupt will become a pending interrupt the moment that the corresponding bit in the Interrupt Disable Register is cleared.

Both pending and latent interrupts are cleared for any channel by writing a one to the corresponding bit position in the Clear Interrupt Register. In general, only channels that have been detected as pending by a read of the Pending Interrupt Register should be cleared. This is because it is possible that a new interrupt could arrive between the read and write. (For example, if the write to the Clear Interrupt Register were to be all ones, then the new interrupt would be lost.) Writing a zero to any bit in the Clear Interrupt Register has no affect on the corresponding channel.

Note that for simplicity the host software need only read the Pending Interrupt Register then immediately write the same byte to the Clear Interrupt Register. Then the software may interrogate the bits in that byte, taking whatever actions are required by the one or more channels recognized to need service. (In addition, the polarity of any input that generated an interrupt may be easily checked by masking the Interrupt Polarity Register with the byte just read.)

If the software wishes to clear all pending or latent interrupts, it writes all ones to the Clear Interrupt Register. This register is cleared on reset, which effectively clears any pending or latent interrupts.

Vector Register

An eight bit read/write vector register is provided. All IP interrupts must be vectored.

All interrupts from one IP-Opto Interrupter use the same vector. The Pending Interrupt Register is used to determine what combination of channels need service.

A single vector is a higher performance implementation than a vector which indicates which (highest priority) channel is requesting service. In the latter case only a single interrupt can be serviced at once. By using a single vector the IP-Opto Interrupter can have any number of equally-weighted channels handled in a single interrupt.

This resister is set to all ones on reset.

Examples

Example 1. Channel 1 interrupts on rising edge (off to on transition):

```
Initialization:
     $FE -> Interrupt Disable Register

Interrupt Handler:
     $01 -> Clear Interrupt Register
                                   ; perform some action
     Return From Exception
```

Example 2. All Channels interrupt on both rising and falling edges:

```
Initialization:
     Data Register XOR $FF -> Polarity Register
     $00 -> Interrupt Disable Register

Interrupt Handler:
     Pending Interrupt Register -> A
     A ->  Clear Interrupt Register
                                   ; now invert interrupt polarity
     Polarity Register XOR A -> Polarity Register
                                   ; perform some actions
     Return From Exception
```

User Options

Debounce Time

Two three-pin shunt groups on IP-Opto Interrupter provide for pin-selectable input switch debounce time. Figure 16 below shows the shunt positions for the three times. The shunt positions are shown in Figure 18 near the end of this manual.

		Channels 1 to 4	
Shunt E2	**Minimum**	**Nominal**	**Maximum**
1-2	2 mS	2.7 mS	3.5 mS
2-3	20 mS	27 mS	35 mS
OUT	4 µS	25 µS	125 µS

		Channels 5 to 8	
Shunt E1	**Minimum**	**Nominal**	**Maximum**
1-2	2 mS	2.7 mS	3.5 mS
2-3	20 mS	27 mS	35 mS
OUT	4 µS	25 µS	125 µS

Figure 16 Switch Debounce Time Selection

The two millisecond time is standard. The longer, 20 millisecond time may be desirable for large mechanical switches.

The third option, with the shunt removed, is for applications where the minimum delay from an external event to the interrupt is desired and mechanical switch debouncing is not required. The range of delay for this option is due primarily to the range in delay of the optical isolator. This delay is primarily a function of the input current. Higher input current results in a smaller delay.

The digital debounce logic also functions as a noise filter. Noise spikes of duration less than the minimum times shown above in Figure 16 are removed by the logic. Note that even with the shunts removed, some noise filtering is still present.

Because of skew in the optical couplers and in the debouncers simultaneous transitions at the IndustryPack's input pins may not necessarily result in simultaneous data or simultaneous interrupts to the host.

Input Resistors

Five values of input resistors are available when the IP-Opto Interrupter is ordered. These values were shown in Figure 6 in the section above, I/O Wiring. Users may substitute other values for special applications. Standard 8-pin four resistor single-in-line (SIP) networks are used. RP2 is used for channels 1 to 4, and RP1 for channels 5 to 8. The locations of RP1 and RP2 are shown in figure 18. Users must be careful not to exceed the power handling capability of the resistor networks. Higher power resistors may be used externally to handle higher voltages.

Refer to the Schematics in the IP-Opto Interrupter Engineering Kit for more information.

ID PROM

Every IP contains an IP PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires that a particular revision be present, it may check for it directly.

Standard data in the ID PROM on the IP-Opto Interrupter is shown in Figure 17 below.
For more information on IP ID PROMs refer to the IndustryPack Logic Interface Specification, available from GreenSpring Computers.

The location of the ID PROM in the host's address space is dependent on which carrier is used. Normally for VMEbus carriers the ID PROM space is directly above the IP's I/O space, or at IP-base + $80. Macintosh drivers use the ID PROM automatically. RM1260 address may be derived from Figure 17 below by multiplying the addresses given by two, then subtracting one. RM1270 addresses may be derived by multiplying the addresses given by two, then adding one.

The ID PROM used is an AMD 27LS19A or equivalent.

3F 19	(available for user)	
17	CRC	
15	No of bytes used	(0B)
13	Driver ID, high byte	
11	Driver ID, low byte	
0F	reserved	(00)
0D	Revision	(A1)
0B	Model No IP-Opto Interrupter	(28)
09	Manufacturer ID GreenSpring	(F0)
07	ASCII "C"	(43)
05	ASCII "A"	(41)
03	ASCII "P"	(50)
01	ASCII "I"	(49)

Figure 17 ID PROM Data (hex)

Construction and Reliability

IndustryPacks were conceived and engineered for rugged industrial environments. The IP-Opto Interrupter is constructed out of 0.062 inch thick FR4 material. The six copper layers consist of two signal layers on the component and solder sides, two internal signal layers, and two internal planes for power and ground.

Through hole and surface mounting of components is used. IC sockets are screw-machined pins, gold plated. High insertion and removal forces are required, which assists in keeping components in place. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the four corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IndustryPack connectors are keyed, shrouded and gold plated on both contacts and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured to the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications they are not required.

The IndustryPack provides a low temperature coefficient of 0.89 W/°C for uniform heat. This is based on the temperature coefficient of the base FR4 material of .31 W/m-°C, and taking into account the thickness and area of the IP. This coefficient means that if 0.89 Watts is applied uniformly on the component side, that the temperature difference between the component and the solder side is one degree Celsius.

Warranty and Repair

GreenSpring Computer warrants this product to be free from defects in workmanship and materials under normal use and service and in its original, unmodified condition, for a period of one year from the time of purchase. If the product is found to be defective within the terms of this warranty, GreenSpring Computer's sole responsibility shall be to repair, or at GreenSpring Computer's sole option to replace, the defective product. The product must be returned by the original customer, insured, and shipped prepaid to GreenSpring Computers. All replaced products become the sole property of GreenSpring Computers.

GreenSpring Computer's warranty of and liability for defective products is limited to that set forth herein. GreenSpring Computers disclaims and excludes all other product warranties and product liability, expressed or implied, including but not limited to any implied warranties of merchandisability or fitness for a particular purpose or use, liability for negligence in manufacture or shipment of product, liability for injury to persons or property, or for any incidental or consequential damages.

GreenSpring's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of GreenSpring Computers, Inc.

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. GreenSpring Computers will not be responsible for damages due to improper packaging of returned items. For service on GreenSpring Products not purchased directly from GreenSpring Computers contact your reseller. Products returned to GreenSpring Computers for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
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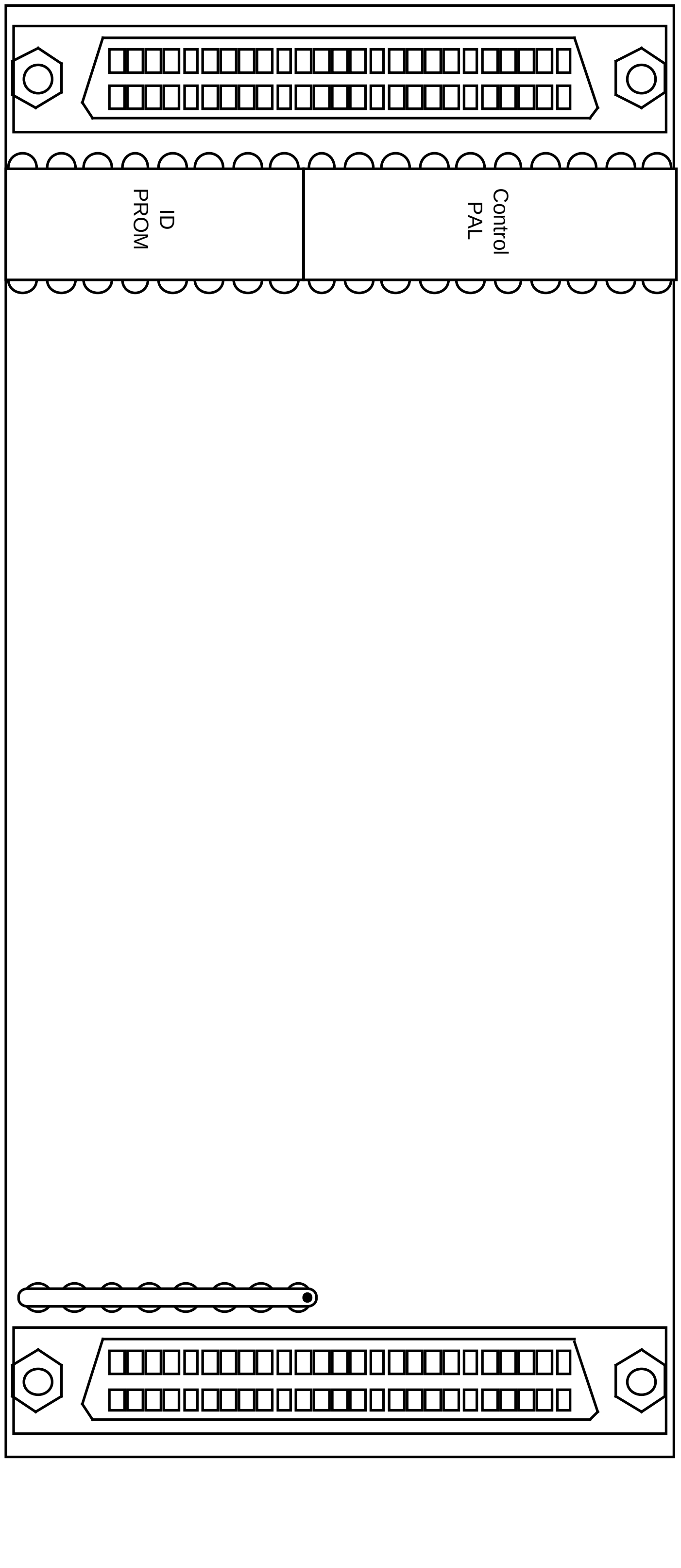
Component Locations

Shown on the next page in Figure 18 is a diagram of the major components of the IP-Opto Interrupter. A comprehensive assembly diagram is available in the IP-Opto Interrupter Engineering Kit, which is recommended for first time buyers.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