IP-UD-E

24 Line Input/Output with LineSafe^{tm} ESD Protection IndustryPack®

User Manual

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IP-UD-E
24 Line Input/Output with
LineSafe ESD Protection
IndustryPack®

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Product Description

The IP-UD-E is part of the IndustryPack™ family of modular I/O components. It provides 24 lines of digital I/O, each with SBS' unique LineSafe™ electrostatic discharge (ESD) protection circuit for increased ruggedness. Each line may be dynamically and individually configured for either input or output. Outputs may be double buffered, making it possible to synchronize multiple IPs. Both internal read back and direct read registers are provided for ease of software development. 16-bit word and 8-bit byte operations are supported.

The IP-UD-E conforms to the IndustryPack Interface Specification. This guarantees compatibility with multiple Support Modules. Because the IPs may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one Support Module with final system implementation on a different one.

The IP-UD-E is pin and software compatible with the IP-UD, a buffered version with 64 mA open collector output drivers and inputs which will handle +15V to –5V. Other products in the UniDig line that share common software but have different output drives are the IP-UD-D with differential I/O, and the IP-UD-HV-16I8O with 100V inputs and high current output switches.

The industry standard 50-pin interface cable may be terminated in a screw terminal block, an OPTO-22™ Direct I/O Interface Module, or user-determined hardware. Alternate grounds on this cable assure reliable signals.

Writing a one to any line turns off the output driver, allowing a passive pull up resistor to set the line to a logic high. Writing a zero to any line turns on the driver, driving the line to a logic low. For input use, a one is written to the corresponding line - this is the power up default. For output use, the binary value desired is written to the corresponding line.

Input and output lines may be double buffered by setting a bit in the Control Register. When this bit is set, the user must provide an external clock of up to 1 MHz. Another bit in the Control Register selects the polarity of this clock, allowing inputs and outputs to be latched on either the rising or falling clock edge.

Two separate locations in I/O space are provided for each signal line. The first location is used to set the output state and also to read back the written value at the internal latch. This read back function is valuable to support bit operations (which are implemented by processors as read-modify-write cycles). It is also useful in debugging, making it possible to observe directly the last value written to the port. The second location is the direct read port, which is always used for reading input values. This register may also be used to verify the correct logic signal is actually on the interface cable.

The IP can function in a Master/Slave Mode for synchronizing multiple IPs. In this mode, the Master IP re-drives the external clock source out I/O line 23. This line becomes the Master Clock that should be wired to I/O line 24 on the Master and all Slave IPs. Wiring in this way prevents excessive loading of the external clock source while ensuring all I/O latches are clocked with minimal skew.

Figure 1 shows a block diagram of the IP-UD-E.

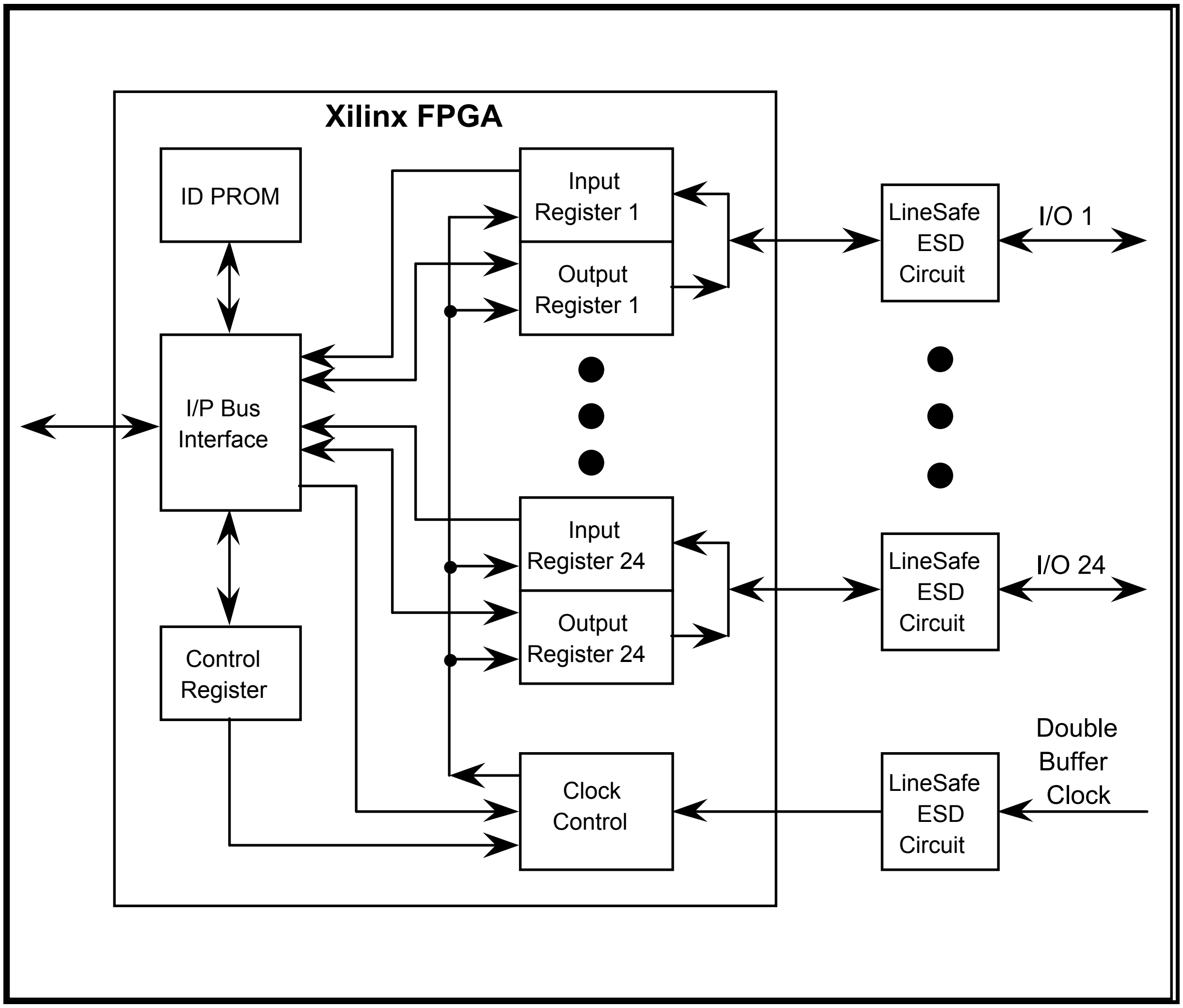

Figure 1 IP-UD-E Block Diagram

VMEbus Addressing

IP-UD-E normally is accessed one word at a time in the host's I/O space. Alternatively, byte or long word accesses may be used. If long words are used, the host (or support module) must map 32-bit long words into two 16-bit cycles. This is common for 68020 and 68030 implementation of the I/O space.

Standard Word Access, I/O Space

base + $0	word	write	Output lines 1—16
base + $2	word	write	Output lines 17—24
base + $0	word	read	Read Back lines 1—16
base + $2	word	read	Read Back lines 17—24
base + $4	word	read	Direct Read lines 1—16
base + $6	word	read	Direct Read lines 17—24
base + $C	word	read/write	Control Register

Figure 2 Word Access VME Address Map

Bit map of words at base + $0 and base + $4

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I/O Line:	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

Bit map of words at base + $2 and base + $6

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I/O Line:	-	-	-	-	-	-	-	-	24	23	22	21	20	19	18	17

Note: data in bits 15 through 8 are ignored in writes, read as "0"s.

Bit map of word at base + $C

Data Bit #	[15:4]	3	2	1	0
Write:	-	Master Select	Mode Enable	Clock Polarity	Dbl. Buffer En.
Read:	0	Master Select	Mode Enable	Clock Polarity	Dbl. Buffer En.

Alternate Byte Access, I/O Space

base + $0	byte	write	Output lines 9—16
base + $1	byte	write	Output lines 1—8
base + $3	byte	write	Output lines 17—24
base + $0	byte	read	Read Back lines 9—16
base + $1	byte	read	Read Back lines 1—8
base + $3	byte	read	Read Back lines 17—24
base + $4	byte	read	Direct Read lines 9—16
base + $5	byte	read	Direct Read lines 1—8
base + $7	byte	read	Direct Read lines 17—24
base + $D	byte	read/write	Control Register

Figure 3 Byte Access VME Address Map

Bit map of bytes at base + $1 and base + $5

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	8	7	6	5	4	3	2	1

Bit map of bytes at base + $0 and base + $4

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	16	15	14	13	12	11	10	9

Bit map of bytes at base + $3 and base + $7

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	24	23	22	21	20	19	18	17

Bit map of byte at base + $D

Data Bit #	[7:4]	3	2	1	0
Write:	-	Master Select	Mode Enable	Clock Polarity	Dbl. Buffer En.
Read:	0	Master Select	Mode Enable	Clock Polarity	Dbl. Buffer En.

Alternate Long Word Access, I/O Space

base + $0	long	write	Output lines 1—24
base + $0	long	read	Read Back lines 1—24
base + $4	long	read	Direct Read lines 1—24
base + $C	long	read/write	Control Register

Figure 4 Long Word Access VME Address Map

Bit map of long words at base + $0 and base + $4

Data Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I/O Line:	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I/O Line:	-	-	-	-	-	-	-	-	24	23	22	21	20	19	18	17

Note: data in bits 15 through 8 are ignored in writes, read as "0"s.

Bit map of long word at base + $C

Data Bit #	[31:20]	19	18	17	16	[15:0]
Write:	-	Master Select	Mode Enable	Clock Polarity	Dbl. Buffer En.	-
Read:	0	Master Select	Mode Enable	Clock Polarity	Dbl. Buffer En.	0

NuBus Addressing

NuBus addressing requires computing the address from the byte addresses given above under VMEbus Addressing. The formula is:

NuBus byte address = (VMEbus byte address * 2) – 1

All byte data is still transferred on data lines D7..D0.

Word addresses on the NuBus are the same as for VME. Word data is transferred on data lines D15..D0.

ISA (IBM PC-AT) Addressing

IP-UD-E normally is accessed one word at a time in the host's I/O space. Alternatively, byte accesses may be used. The actual application will depend on the carrier board. See the carrier board manual for details.

Standard Word Access, I/O Space

base + $0	word	write	Output lines 1—16
base + $2	word	write	Output lines 17—24
base + $0	word	read	Read Back lines 1—16
base + $2	word	read	Read Back lines 17—24
base + $4	word	read	Direct Read lines 1—16
base + $6	word	read	Direct Read lines 17—24
base + $C	word	read/write	Control Register

Figure 5 Word Access ISA Address Map

Bit map of words at base + 0 and base + 4

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I/O Line:	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

Bit map of words at base + 2 and base + 6

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I/O Line:	-	-	-	-	-	-	-	-	24	23	22	21	20	19	18	17

Note: data in bits 15 through 8 are ignored in writes, read as "0"s.

Bit map of word at base + $C

Data Bit #	[15:4]	3	2	1	0
Write:	-	Master Select	Mode Enable	Clock Polarity	Dbl. Buffer En.
Read:	0	Master Select	Mode Enable	Clock Polarity	Dbl. Buffer En.

Alternative Byte Access, I/O Space

base + $0	byte	write	Output lines 1—8
base + $1	byte	write	Output lines 9—16
base + $2	byte	write	Output lines 17—24
base + $0	byte	read	Read-back lines 1—8
base + $1	byte	read	Read-back lines 9—16
base + $2	byte	read	Read-back lines 17—24
base + $4	byte	read	Direct Read lines 1—8
base + $5	byte	read	Direct Read lines 9—16
base + $6	byte	read	Direct Read lines 17—24
base + $C	byte	read	Control Register

Figure 6 Byte Access ISA Address Map

Bit map of bytes at base + $0 and base + $4

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	8	7	6	5	4	3	2	1

Bit map of bytes at base + $1 and base + $5

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	16	15	14	13	12	11	10	9

Bit map of bytes at base + $2 and base + $6

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	24	23	22	21	20	19	18	17

Bit map of byte at base + $C

Data Bit #	[7:4]	3	2	1	0
Write:	-	Master Select	Mode Enable	Clock Polarity	Dbl. Buffer En.
Read:	0	Master Select	Mode Enable	Clock Polarity	Dbl. Buffer En.

I/O Pin Wiring

This section gives the pin assignments and wiring recommendations for IP-UD-E.

The pin numbers given in Figure 7 below correspond to numbers on the 50-pin IndustryPack I/O connector, to the wires on a 50-pin flat cable plugged into a standard IP carrier board, and to the screw terminal numbers on the IP-Terminal block.

I/O 1	1	GND	2
I/O 2	3	GND	4
I/O 3	5	GND	6
I/O 4	7	GND	8
I/O 5	9	GND	10
I/O 6	11	GND	12
I/O 7	13	GND	14
I/O 8	15	GND	16
I/O 9	17	GND	18
I/O 10	19	GND	20
I/O 11	21	GND	22
I/O 12	23	GND	24
I/O 13	25	GND	26
I/O 14	27	GND	28
I/O 15	29	GND	30
I/O 16	31	GND	32
I/O 17	33	GND	34
I/O 18	35	GND	36
I/O 19	37	GND	38
I/O 20	39	GND	40
I/O 21	41	GND	42
I/O 22	43	GND	44
I/O 23/Master Clk Out	45	GND	46
I/O 24/Slave Clk In	47	GND	48
Double Buffer Clk	49	GND	50

Figure 7 I/O Pin Assignment

Caution

Note that when the IP-UD-E is used to directly connect with OPTO 22, Allen Bradley, Grayhill or similar compatible parallel opto-isolation panels that these panels number their channels starting with pin 47. Thus the IP-UD-E line number ordering and the OPTO Panel line number ordering are *reversed*.

IndustryPack Logic Interface Pin Assignment

Figure 8 below gives the pin assignments for the IndustryPack Logic Interface on the IP-UD-E. Pins marked n/c below are defined by the specification, but are not used on IP-UD-E. Also see the User Manual for your IP Carrier board for more information.

GND	GND	1	26	
CLK	+5V	2	27	
Reset*	R/W*	3	28	
D0	IDSel*	4	29	
D1	n/c	5	30	
D2	n/c	6	31	
D3	n/c	7	32	
D4	INTSel*	8	33	
D5	n/c	9	34	
D6	IOSel*	10	35	
D7	n/c	11	36	
D8	A1	12	37	
D9	n/c	13	38	
D10	A2	14	39	
D11	n/c	15	40	
D12	A3	16	41	
D13	n/c	17	42	
D14	A4	18	43	
D15	n/c	19	44	
BS0*	A5	20	45	
BS1*	n/c	21	46	
–12V	A6	22	47	
+12V	Ack*	23	48	
+5V	n/c	24	49	
GND	GND	25	50	

Note 1: The no-connect (n/c) signals above are defined by the IndustryPack Logic Interface Specification, but not used by this IP. See the Specification for more information.

Note 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IndustryPack.

Figure 8 Logic Interface Pin Assignment

Programming

Programming the IP requires only the ability to read and write data in the host's I/O space. The base address is determined by the IP Support Module. This document refers to this address as "base".

After power on reset or VME system reset, the IP requires a minimum delay of 300 milliseconds before any accesses are made by the host system. This is to allow the Xilinx FPGA to configured itself. Any accesses during this time will result in a bus error. Reset sets all lines to be inputs and clears all bits in the Control Register.

Each of the 24 bits may be individually set as input or output. To set a bit to be input, write a "1" to the I/O bit location. This is the default.

To write a zero on the I/O signal line, write a "0" to the I/O bit location. To write a one on the I/O signal line, write a "1" to the I/O bit location. Writing a one and setting the signal line to input mode is the same. Passive pull-up resistors are used with tri-state drivers to implement the interface.

Using word access, up to 16 bits may be programmed at once. The IP implements a read back register at the same address used for writing to the signal line I/O bits. This permits "set bit" and "clear bit" instructions to be used in programming, which are implemented by the host hardware as read-modify-write cycles. Thus, single bits at well as bit fields may be accessed.

The IP may also be accessed using byte or long word accesses. If long word accesses are used from a 68020, 68030, or 68040 host, the I/O space must be mapped into "D16". 68000 and 68010 hosts internally map all long word accesses into 16 bits, so no special precaution is necessary.

The IP uses a Control Register to enable double buffering and control the polarity of the Double Buffer Clock. It also is used to enable Master/Slave Mode and define the Master IP in a multiple IP system using an external clock source to synchronize inputs and outputs.

Bit #	Definition	Access
0	Double Buffer Enable	Read/Write
1	Double Buffer Clock Polarity Select	Read/Write
2	Mode Enable	Read/Write
3	Master Select	Read/Write
4 - 7	Reserved	Read as "0"

Figure 9 Control Register Bit Definitions

Control Register Bit Definitions:

Bit [0] = D0 LSB Double Buffer Enable
Double Buffer Enable bit. This bit enables double buffering. If this bit is set to a "1", the user must provide a clock on either the Double Buffer Clock, pin 49, or the Slave Clock, pin 45, depending on how bit[3] is set. This clock may be up to 1 MHz and must have an edge rate faster than 60 ns. Writing a "0" disables double buffering. This is the default.

Bit [1] = D1 Double Buffer Clock Polarity Select

Double Buffer Clock Polarity Select bit. This bit controls the Double Buffer Clock polarity. Writing a "1" will cause output data to be latched out of the IP and input data to be latched into the IP on the falling edge of the Double Buffer Clock. Writing a "0" will cause data to be latched on the rising edge of the Double Buffer Clock. This is the default.

Bit [2] = D2 Master/Slave Mode Enable

Master/Slave Mode Enable bit. This bit determines which pin on the I/O connector is the source for the Double Buffer Clock. Writing a "1" puts the IP in Master/Slave mode and makes pin 47 (I/O 24) the source for the Double Buffer Clock. In this mode, I/O 24 must be set to "1" to make it an input. **This I/O line must be set up prior to putting the IP in Master Mode.** Writing a "0" to the Master/Slave Mode Enable bit puts the IP in normal mode and makes pin 49 (Double Buffer Clock) the source for the Double Buffer Clock. In this mode, all 24 I/O lines are available for use. This is the default mode.

Bit [3] = D3 Master Select

Master Select bit. This bit determines whether the IP is a master or slave. Writing a "1" makes the IP a master. When it is a master, the IP re-drives the Double Buffer Clock (pin 49) out I/O line 23 (pin 45). This clock should then be wired externally to I/O line 24 (pin 47) on this IP and all slave IPs. This minimizes the clock skew between the master and all slaves. When this bit is set, I/O line 23 must be set to "0" and I/O line 24 must be set to "1". **These I/O lines must be set up prior to putting the IP in Master Mode.** If more than three IPs will be connected as master and slaves, the 10 KΩ pullup resistors on all the clock pins except the last in the chain should be removed. Without eliminating them, the pullup resistors will add up to a greater load than the outputs can drive. Before removing a resistor network, note which direction pin 1 is facing (pin 1 has a small dot marked on the resistor network body above the pin). To remove a pullup resistor, remove the resistor network, and cut off the lead on the pin corresponding to the I/O line, then replace the resistor network. The Master IP should have pins 8 and 9 of RN2 cut, while all Slave IPs except the one farthest from the Master should have pin 9 of RN2 cut.

Writing a "0" to the Master Select bit makes the IP a slave with its clock source I/O line 24 if Bit [2] is set to a "1", or normal operation with its Double Buffer Clock source from pin 49 (Double Buffer Clock). This is the default. See Figure 12 in the Theory of Operation section later in this manual for a diagram of how to wire a master and slave IP.

Bit [7..4] = D7..D4

These bits are reserved for future use and will be read as "0".

Double Buffering

Double buffering is a feature that allows all the inputs and outputs to be latched at the same time, whether on a single IP or a system with multiple IPs. This is useful for systems that require many inputs and outputs to be updated simultaneously. To use double buffering, an external TTL or CMOS level clock with an edge rate faster than 60 ns must be provided on Pin 49, the Double Buffer Clock Input pin. Alternatively, a Slave Clock must be provided on Pin 47, the Slave Clock Input pin if the IP is put into Master/Slave Mode. Regardless of which pin the Double Buffer Clock comes from, the Double Buffer Enable bit, Bit [0], in the Control Register must be set. The Double Buffer Clock polarity is programmable via the Double Buffer Clock Polarity bit, Bit [1], in the Control Register. Setting this bit to a "0" will cause the input and outputs to be latched on the rising edge of the Double Buffer Clock, while setting the bit to "1" will latch the inputs and outputs on the falling edge.

ID PROM

Every IP contains an IP PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires a particular revision IP, it may check for it directly.

Standard data in the ID PROM on the IP-UD-E is shown in Figure 10 below. For more information on IP ID PROMs refer to the IndustryPack Logic Interface Specification, available from SBS Technologies. The ID PROM on the IP-UD-E is implemented in the Xilinx FPGA device.

The location of the ID PROM in the host's address space is dependent on the carrier board used. For most VMEbus carriers the ID PROM space is directly above the IP's I/O space, or at IP-base + $80. Macintosh drivers use the ID PROM automatically. RM1260 address may be derived from Figure 10 below by multiplying the addresses given by two, then subtracting one. RM1270 addresses may be derived by multiplying the addresses given by two, then adding one.

3F 19	(available for user)	
17	CRC for bytes used	(C3)
15	No of bytes used	(0C)
13	Driver ID, high byte	(00)
11	Driver ID, low byte	(00)
0F	reserved	(00)
0D	Revision	(A1)
0B	Model No IP-UD-E	(51)
09	Manufacturer ID SBS	(F0)
07	ASCII "C"	(43)
05	ASCII "A"	(41)
03	ASCII "P"	(50)
01	ASCII "I"	(49)

Figure 10 ID PROM Data (hex)

Theory of Operation

IndustryPack Standards

The IP-UD-E is part of the IndustryPack™ family of modular I/O products. It meets the IndustryPack Logic Specification. (Contact SBS Technologies for a copy of this Specification.) It is assumed the reader is at least casually familiar with both this document and 68000 processor architecture.

Control Logic

All control logic is contained within a single Xilinx FPGA. It is clocked by the 8 MHz IP Logic clock from the Support Module. The IP responds to I/O and ID selects. It does not respond to memory selects, however the MEMSel* line is routed to the FPGA, enabling easy modification for special needs.

The IP does not require wait states for either read or write cycles. Thus, the FPGA generates Ack* on the clock cycle following either I/O or ID Select. Hold cycles (from the Support Module) are supported for both read and write cycles by extending Ack* as required. If no hold cycles are requested by the Support Module, the IP is capable of supporting the full 8 MByte per second data transfer rate of the IP Logic Interface Specification.

I/O Data Lines

All input and output latches and buffers are contained within the Xilinx FPGA. Each I/O line has SBS' unique LineSafe™ ESD protection circuit for added ruggedness. This circuit puts a 33Ω resistor in series and the equivalent of a 1100 pF capacitor to ground on each I/O line. Standard ESD handling precautions should still be used as the IP Logic Interface lines are unprotected. Additionally, external voltage should not be applied when the IP is unpowered. This will damage the Xilinx FPGA. Turning on and off all power supplies at the same time will eliminate this problem.

Outputs use active low tri-state buffers that are controlled by the individual output lines. In this manner, they implement an open drain connection, being enabled when the output is low and disabled when the output is high. Three 10 KΩ, resistor networks pull up the I/O lines to +5V when the outputs are disabled. RN1 pulls up I/O Lines 9—16, RN2 pulls up I/O Lines 17—24, and RN3 pulls up I/O Lines 1—8. These resistors may be replaced with other values, as long as the total sink current necessary to drive the pullup and load on each line low is less than the four milliamps specified for each pin of the Xilinx chip. Individual pullup resistors may be removed by cutting the pin off the network corresponding to the desired I/O line.

Data Output

Each output has two latches associated with it. If double buffering is enabled, the Double Buffer Latch is clocked by the Double Buffer Clock. Without double buffering, this latch is clocked on the falling edge of the IP Clock. Figure 6 shows a block diagram. Outputs from the Double Buffer Latch directly drive the I/O output lines. Data is latched into the internal latch on the rising edge of the IP Clock after the IOSel* line is driven low.

Double buffering is enabled by setting the Double Buffer Enable Bit (bit [0]) in the Control Register to a "1". A TTL compatible signal must be provided on the External Clock, pin 49. This signal must have an edge rate faster than 60 ns. If double buffering is enabled, the Double Buffer Clock Polarity Bit (bit [1]) in the Control Register is used to set the Double Buffer Clock polarity. Setting the Double Buffer Clock Polarity Bit to a "0" will latch data on the rising edge and setting it to a "1" will latch data on the falling edge. The power up default is "0" for both these bits.

Data Input

The data may be read from two sets of address locations. The first set of locations, base + 0 and base + 2 for word operations, function as the Internal Read Back Register. The data latched in the Internal Output Latch is read from these addresses. They support processor bit operations implemented as read-modify-write cycles, and are also useful for debugging purposes.

The second set of locations, base + 4 and base + 6 for word operations, is the Direct Read Register. Data is latched into Input Register with the same clock that latches the Double Buffer Latch. Figure 11 shows a block diagram.

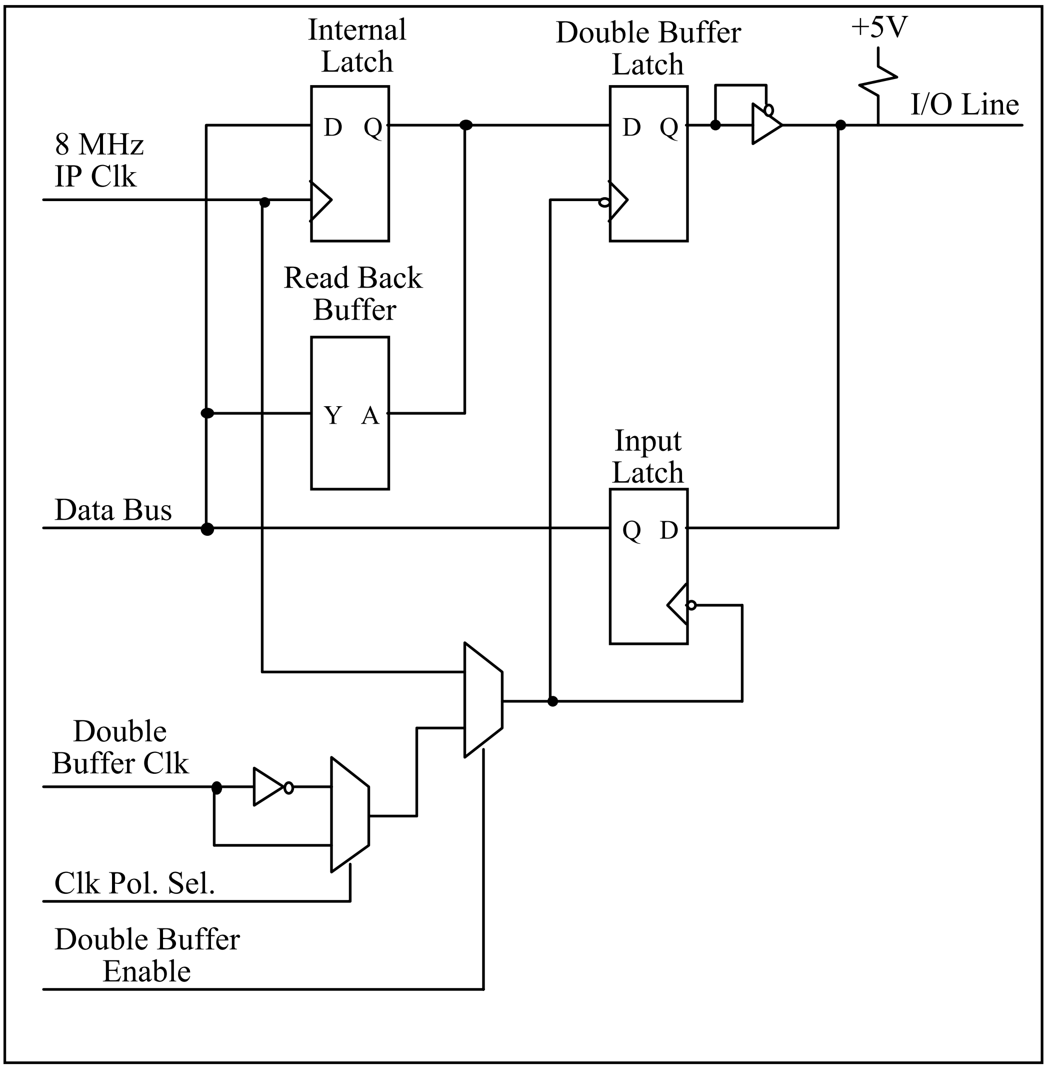

Figure 11 I/O Line Block Diagram

Master/Slave Mode

Master/Slave Mode is provided for multiple IP systems using a single external clock to synchronize inputs and outputs. If this clock does not have sufficient drive capability for driving all the IPs in the system, it may be wired to the Master IP to be re-driven to all the Slave IPs. Figure 12 shows a block diagram of two IPs in Master/Slave Mode while Figure 13 shows a diagram of how to wire a Master and Slave IP.

An IP is configured to be a Master by first making I/O Line 23 an output by writing a "0" to it and I/O Line 24 an input by writing a "1" to it. It is critical this be done before the Control Register is changed to allow the I/O lines to be clocked by the internal clock. Next, set both the Master/Slave Mode Bit and the Master Select Bit (bit [2] and bit [3]) to a "1" in the Control Register. The desired clock polarity is set by the Clock Polarity Select Bit (bit [1]). Writing a "0" to this bit will latch data on the rising edge, writing a "1" will latch data on the falling edge. The external clock is wired to the Double Buffer Clk pin 49. The Master Clk Out pin 45 is then wired to the Slave Clk In pin 47 on all the IPs, including the Master IP.

Slave IPs are configured by setting the Master/Slave Mode Bit (bit [2]) to a "1" and the Master Select Bit (bit [3]) to a "0" in the Control Register. The desired clock polarity is set by the Clock Polarity Select Bit (bit [1]). I/O Line 24 is set to be an input by writing a "1" to it. The Master Clk Out signal from the Master IP is wired to the Slave Clk In pin 47.

If more than three IPs will be connected as master and slaves, the 10 KΩ pullup resistors on all the clock pins except the last in the chain should be removed. Without eliminating them, the pullup resistors will add up to a greater load than the Master Clock Output can drive. Before removing a resistor network, note which direction pin 1 is facing (pin 1 has a small dot marked on the resistor network body above the pin). To remove a pullup resistor, remove the resistor network, and cut off the lead on the pin corresponding to the I/O line, then replace the resistor network, maintaining the proper orientation. Pin 1 on the board has a square around it and is on the same end as the label. The Master IP should have pins 8 and 9 of RN2 cut, while all Slave IPs except the one farthest from the Master should have pin 9 of RN2 cut.

If an IP is changed from a Slave to a Master, it must be first taken out of Double Buffer Mode to set I/O Lines 23 and 24 correctly before re-enabling Double Buffer Mode.

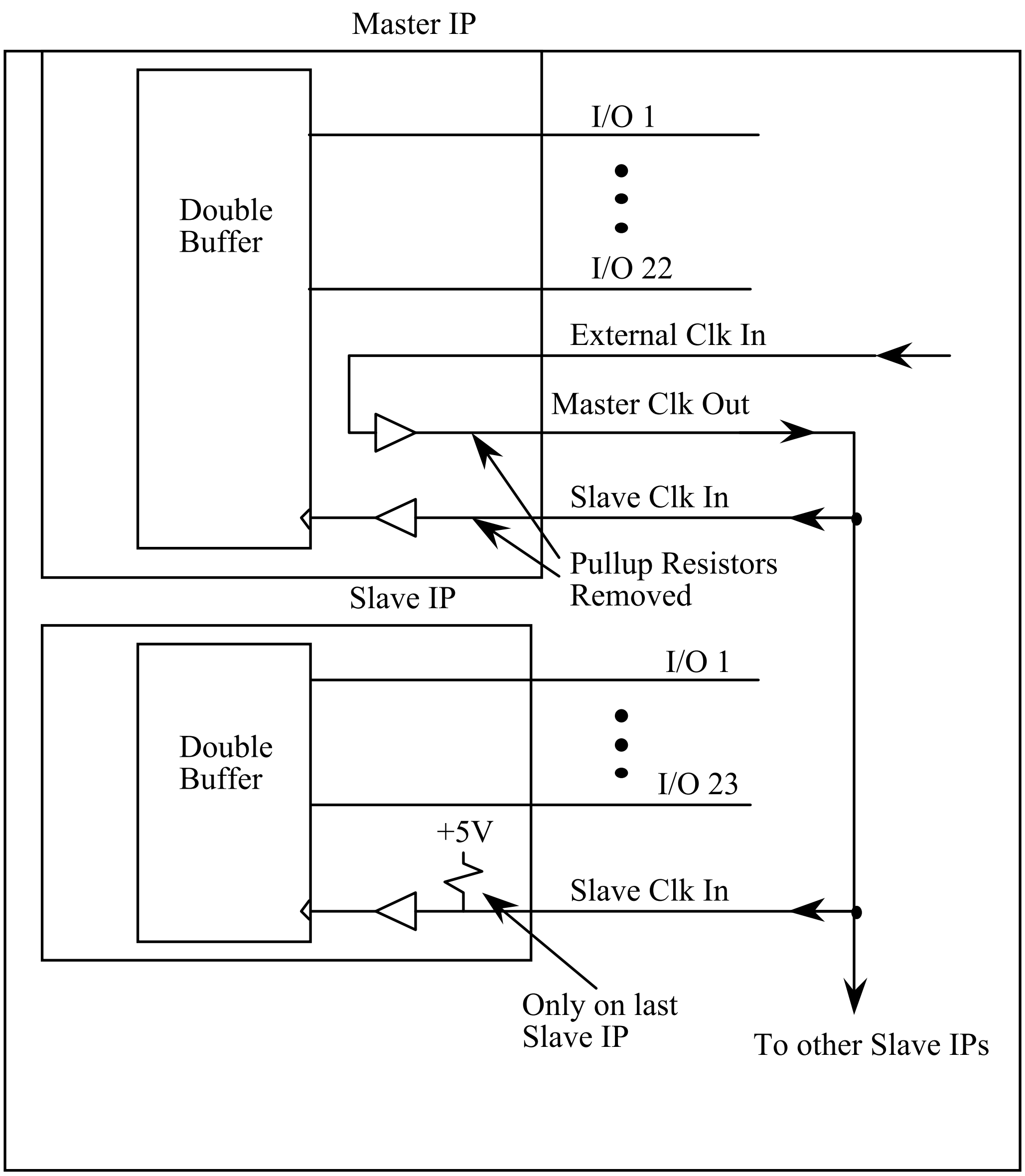

Figure 12 Master and Slave Configuration

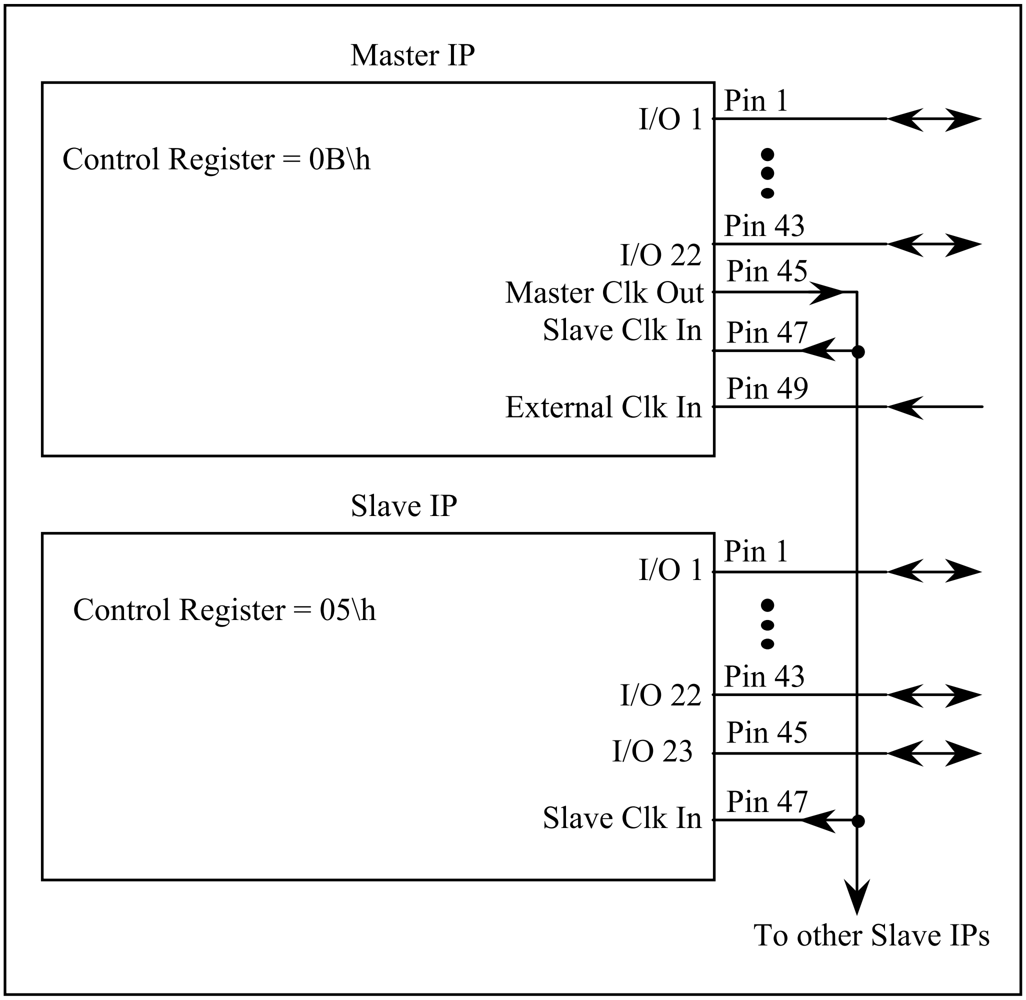

Figure 13   Master and Slave Wiring Diagram

Construction and Reliability

IndustryPacks were conceived and engineered for rugged industrial environments. The IP-UD-E is constructed out of 0.062 inch thick FR4 V0 material. The four copper layers consist of two signal layers on the top and bottom, and two internal power and ground plane layers.

Through hole and surface mounting of components are used. IC sockets use gold plated screw-machine pins. High insertion and removal forces are required, which assists in keeping components in place. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the four corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IndustryPack connectors are keyed, shrouded and have gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured to the carrier with four M2 metric stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration and incomplete insertion. For most applications they are not required.

The IndustryPack provides a low temperature coefficient of 0.89 W/°C for uniform heat. This is based on the temperature coefficient of the base FR4 material of 0.31 W/m-°C, taking into account the thickness and area of the IP. This coefficient means that if 0.89 Watts is applied uniformly on the component side, then the temperature difference between the component and the solder side is one degree Celsius.

Repair

Service Policy

Before returning a product for repair, verify as soon as possible that the suspected unit is at fault; then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if it is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include the return address and telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. SBS Technologies will not be responsible for damages due to improper packaging of returned items. For service of SBS Technologies products not purchased directly from SBS Technologies, contact your reseller. Products returned to SBS Technologies for repair by other than the original customer will be treated as out-of-warranty.

For service, contact:

SBS Technologies, Inc.
1284 Corporate Center Drive
St. Paul, MN 55121-1245
Tel: (651) 905-4700
FAX: (651) 905-4701
Email: support.commercial@sbs.com

Specifications

Logic Interface	IndustryPack Logic Interface
Digital Interface	24 digital signal lines with double buffered outputs and latched inputs Each line is either an input or an output Alternate grounds on the interface cable
Interface Level	TTL Tri-state with 10 K Ohm pull up resistor standard 4 mA current sink
Software Interface	The 24 I/O lines are read and written to with either word or byte accesses. There is an 8-bit Control register
Initialization	300 millisecond delay from reset Forces all lines to be inputs Disables double buffering
Access Mode	Byte or word in I/O Space Byte or word in ID Space
Wait States	Zero
Transfer Rate	8 Mbytes/second maximum, continuous
Onboard Options	All options are software programmable
Dimensions	Standard Single High IndustryPack width and length 1.8 x 3.9 inches
Construction	Conformal Coated FR4 4 layer Printed Circuit Surface mounted components
Temperature Coefficient	0.89 W/°C for uniform heat across IP
Power Requirements	+5.0 VDC, 30mA typical