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IP-E1

E1 and ISDN IndustryPack®

User's Manual

Manual Revision: 2 7/27/99 Hardware Revision: A

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IP-E1

E1 and ISDN IndustryPack®

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Product Description

The IP-E1 implements full E1 and ISDN protocol in a single-size IndustryPack. IP-E1 is designed for demanding applications in data communication and custom voice+networks. When linked to a host processor such as an MVME162, powerful modular data communication functions and networks are easily implemented that are fully compatible with telco equipment and hardware.

The LSI devices on the IP-E1 are Brooktree BtP9170 Intelligent E1 Controller, Brooktree Bt8071A HDLC Controller, Brooktree Bt8069B Line Interface Unit, 256-byte FIFO, one MB SRAM, and Xilinx FPGA.

The BtP9170 Intelligent E1 Controller is a microprocessor (MPU) controlled device that implements the 2048 Kbits/s transceiver functions of an E1 (European 1st order) digital interface. It offers programmable control modes, per-channel trunk and signaling forced-data substitution, per-channel trunk and signaling conditioning, received signaling storage, performance monitoring and reporting, alarm handling, transmit/receive channelization and synchronization, in addition to framer functions applicable to PCM30 and CEPT for digital exchange, multiplex, or terminal equipment.

The Bt8071A HDLC Controller multiplexes/demultiplexes up to 32 high speed data channels to support HDLC and ISDN implementations. ISDN implementation is based on E1 primary rate carrier. It provides 32 full duplex channels with HDLC/SDLC protocol formatting/deformatting, and fully programmable channel configuration including hyperchannels. All four DMI B channel data options are implemented covering 64 kbps clear channel, 64 kbps virtual circuit service, 19.2 kbps asynchronous or synchronous, and 56 kbps synchronous. Signaling options support both bit-oriented (BOS) and message-oriented (MOS).

The 256-byte FIFO is a companion device to Bt8071A for channel number and buffer status storage.

Local memory consists of up to one MB of high speed dual-port SRAM directly addressable in the IndustryPack memory address space. The SRAM is shared between the IndustryPack host and the Bt8071A HDLC Controller for reception and transmission of data packets over the E1 communication link.

The Bt8069B Line Interface Unit interfaces the BtP9170 to the CEPT PCM30 transmission medium. The Bt8069B physically interfaces to standard E1 cabling via on-board transformers.

The Xilinx field programmable gate array (FPGA) implements the logic interface between the host and all the on-board LSI devices.

IP-E1 can generates two distinct interrupt levels to the host. One of the interrupts is generated by the BtP9170 upon conditions such as bipolar violation and framing error. The other interrupt is generated by the Bt8071A HDLC Controller through the FIFO. Host programmable interrupt vector register associated with each interrupt is supported.

The information contained in this user manual is specific to implementation of E1 communication link on IP-E1. For a full detailed description of functions and capabilities of the BtP9170, Bt8071A, and Bt8069B, please refer to their respective Brooktree data sheets included in the Engineering Kit.

GreenSpring Computers offers some example source C-code such as transmit/receive local and external loopback for the IP-E1. Contact factory for more information.

Key Features:

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- Single-high size, Type II (components on back)
- Brooktree BtP9170 as Intelligent E1 Controller
- Brooktree Bt8071A as 32-Channel HDLC Controller with interrupt capability
- Brooktree Bt8069B Line Interface Unit.
- 256-byte FIFO stores channel number and buffer status with interrupt capability
- Receive and transmit cable interface transformers
- Support 75? and 120? line impedance interface
- One MB high speed dual port SRAM as buffer memory
- All surface-mount components for maximum reliability
- CMOS technology for minimum power consumption

BtP9170 Intelligent E1 Controller Detailed Features:

- Intelligent Single-Chip E1 Transceiver (2048 Kbits/s)
- Support for Multiple PCM30 Framing Formats:
    - Channel Associated Signaling (CAS)
    - Clear Channel Without Signaling
    - Common Channel Signaling (CCS)
- Adheres to CCITT Blue Book Recommendations:
    - G.704 Synchronous Frame Structures
    - G.706 Frame Alignment and CRC Procedures
    - G.732 Channel Associated Signaling
- Provides Facility Management Functions:
    - Near-End Performance Monitoring
    - Far-End Performance Data Reporting
    - Extraction of 4 Kbits/s Link Data
- Independent Transmit and Receive Functions, Each with a Separate Timebase
- User-Maskable Interrupt Request Generated on Specified Alarm and Error Conditions
- On-Chip CRC-4 Generation and Checking
- Off-Line Framer "Flywheel Timebase" Option
- Independent Transmit and Receive Per Channel Controls
    - Automatic Conditioning of Receive Trunk and Signaling Data During a Fault Condition
    - Unconditional Replacement of Transmit or Receive Trunk and Signaling Data
- Ones Density Options: HDB3 or Transparent
- Alarm Generation and Detection

Bt8071A 32-Channel HDLC Controller Detailed Features:

- Simplifies ISDN/DMI Implementation
- Provides up to 32-Full-Duplex Channels with DHLC/SDLC Protocol Formatting
- Provides Fully Programmable Hyperchannel Configuration
- Supports All Four DMI B-Channel Data Options:
    - Mode 0 (Clear Channel 64 kbps Synchronous)
    - Mode 1 (56 kbps Synchronous Data With or Without HDLC Protocol)
    - Mode 2 (up to 19.2 kbps Synchronous or Asynchronous)
    - Mode 3 (64 kbps Virtual Circuit Service)
- Supports Both DMI D-Channel Signaling Options:
    - Bit-Oriented Signaling (BOS)
    - Message-Oriented Signaling (MOS)
- Compatible With 2.048 Mbps CEPT PCM-30 Carrier Format
- Supports Both Flag Stuffing (I.462, DMI mode 2) and RA2 Intermediate Rate Adaption (I.460, X.30, V.110, or ECMA-102)
- Compatible With HDLC, SNA SDLC, X.25, X.75, LAPB, and LAPD Protocols

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• Provides CRC-16 Generation and Checking, Automatic Flag Detection and Transmission, and Zero-bit Insertion and Deletion

Bt8069B Line Interface Unit Detailed Features:

• Compatible with E1 PCM30 (2.048 Mbps) standard
• Meets CCITT Recommendation G.703 for PCM30
• Meets jitter requirements specified in CCITT Recommendation G.823 for PCM30
• Phase Locked Loop for loop timing applications
• Incorporates a frequency discriminator in PLL circuitry to enhance frequency training and locking
• Accommodates pulse shape requirement for 120? and 75? lines in PCM30 applications
• Intrinsic jitter less than 0.05UI
• Jitter attenuation roll off starts at 2 Hz
• Jitter tolerance above 0.4 UI for jitter frequency from 20KHz to 100 KHz
• 8-bit transmitter (TX) elastic store for system-provided timing alignment
• 44-bit receiver (RX) elastic store for input jitter and wander accommodation
• Provision to bypass RX elastic store
• Master/slave timing option
• Local and remote loopback modes with automatic RCLK switching
• AIS (Blue Alarm) generation and detection
• Bipolar violation detector
• Automatic detection of external line-rate clock (EXCLK)
• Automatic centering of phase-lock loop when timing reference is absent
• On-chip line drivers, pulse shaping, and TX equalizer

Figure 1 provides the block diagram of IP-E1.

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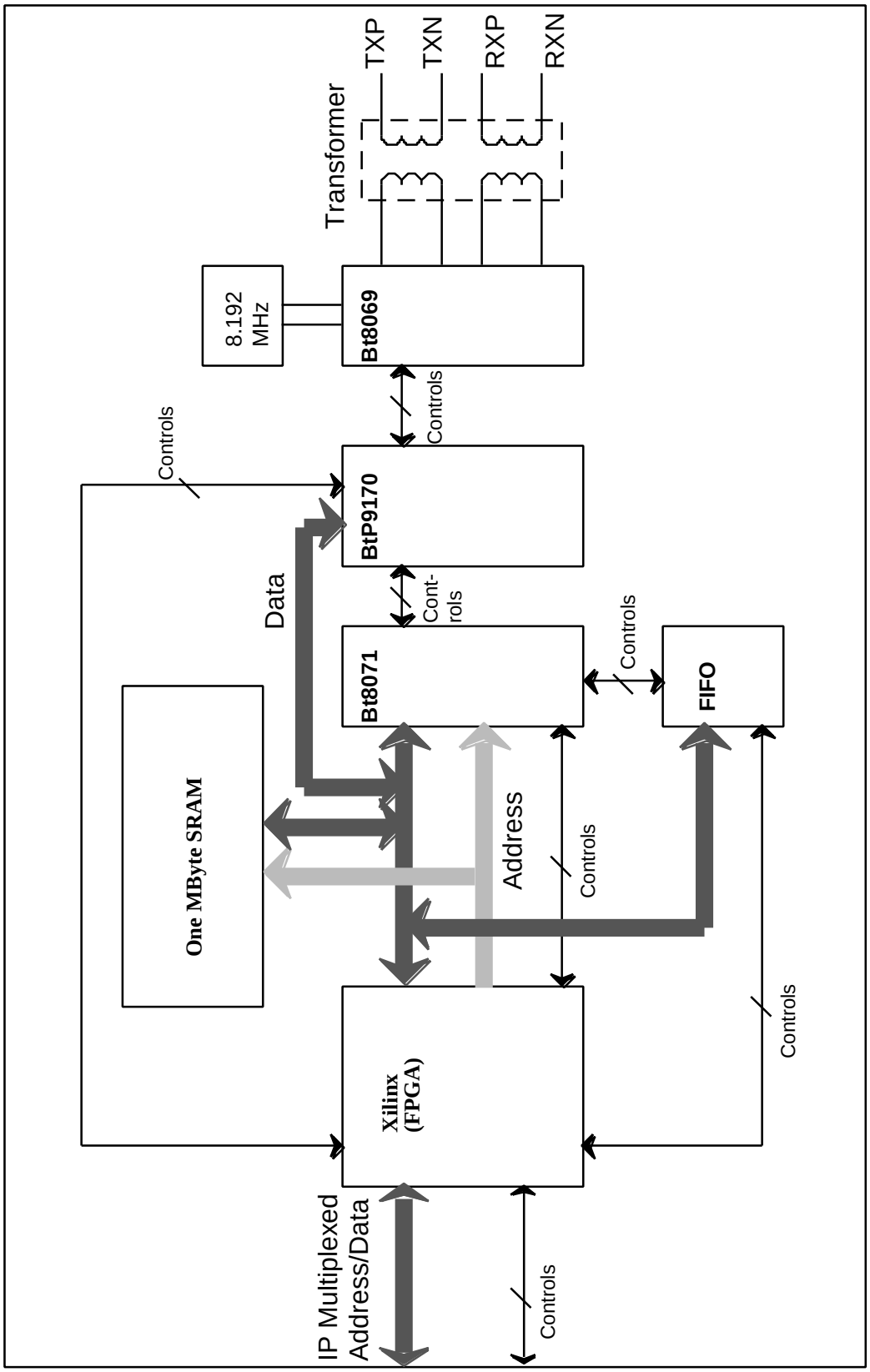


Figure 1Simplified Block Diagram Of IP-E1

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VMEbus Addressing

The IP-E1 registers and SRAM are mapped in a two megabyte IP memory address space. The following address offsets are relative to the IP-E1 memory base address.

$00 0000 through $0F FFFF	IP-E1 Registers
$10 0000 through $1F FFFF	IP-E1 SRAM

The registers are byte-wide only and located on data lines D7..D0. This byte is the odd byte in Motorola 68K host architecture. Any access to registers on data lines D15..D8 is ignored.

The host may access SRAM as byte- or word-wide. Odd byte accesses to SRAM are on data lines D7..D0, even bytes on D15..D8, and even words on D15..D0.

The registers are grouped into two categories: 1) Brooktree BtP9170 internal registers 2) IP-E1 registers specific to hardware.

Shown below in Figure 2 are the BtP9170 internal registers as found in the BtP9170 data sheet. The Address column provides the VME addressing required from the host..

Addr (Hex)	**Reg Lable**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
000001	MR0	FEBE	AISDET	LOST	CRCS	BPVS	FERR	RYEL	COFA
000003	MR1	SLIP	RMYEL	RMRED	T16AIS	SRED	MS3	MS2	MS1
000005	MR2	TXN	PDV	ES1	ES0	EN8071	EN8069	CB	IntReq0
000007	TS0MR	NBOK	NBCH	NBUSE	SA4	SA5	SA6	SA7	SA8
000009	TS0CR	USESA	SA4L	DISYEL	TX4	TX5	TX6	TX7	TX8
00000B	CR0	REDMD 1	REDMD 0	SYS1	SYS0	CRCDIS	SMFENA	ACE1	ACE0
00000D	CR1	RZSD	TZSD	ABIEN	Note1	Note1	Note1	FAS8	SL
00000F	CR2	RESET	RFSR	TS16L	OLFRE	Note1	Note1	TCE	CGA
000011	CR3	E1	E2	EBFRCE	PADE	EN8071	EN8069	CB	0
000013	CR4	TYEL	SAIS	ADS	MODE	LOOP	ELS3	ELS2	ELS1
000015	CR5	MASTR	ETNRZ	TS16BY	YBYPAS	NBYPAS	FBYPS	SBYPAS	CBYPA
000017	IREG	IREG1	IREG2	IREG3	IREG4	IREG5	IREG6	IREG7	IREG8
000019	DSR	Note1	D2A	D4B	D4A	D16D	D16C	D16B	D16A
00001B	AER	FEBE	AISDT	LOST	CRCS	BPVS	FERR	RYEL	COFA
00001D	IER	NEPER M	FRED	CASRED	CRCRED	RXSIG	ALARM	0	ITST
00001F	ICR	NEPER M	FRED	CASRED	CRCRED	RXSIG	ALARM	0	ITST
000021	CR6	PLOOP	0	0	SAS2	SAS1	SAS0	LOSMD	INTPE R
000023	MR3	NOCRC4	0	0	0	0	0	0	0
000041	PCCR1	P	Q	X	E	D	C	B	A
000043	PCCR2	P	Q	X	E	D	C	B	A
000045	PCCR3	P	Q	X	E	D	C	B	A
000047	PCCR4	P	Q	X	E	D	C	B	A
000049	PCCR5	P	Q	X	E	D	C	B	A
00004B	PCCR6	P	Q	X	E	D	C	B	A
00004D	PCCR7	P	Q	X	E	D	C	B	A
00004F	PCCR8	P	Q	X	E	D	C	B	A

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000051	PCCR9	P	Q	X	E	D	C	B	A
000053	PCCR10	P	Q	X	E	D	C	B	A
000055	PCCR11	P	Q	X	E	D	C	B	A
000057	PCCR12	P	Q	X	E	D	C	B	A
000059	PCCR13	P	Q	X	E	D	C	B	A
00005B	PCCR14	P	Q	X	E	D	C	B	A
00005D	PCCR15	P	Q	X	E	D	C	B	A
00005F	PCCR16	P	Q	X	E	D	C	B	A
000061	PCCR17	P	Q	X	E	D	C	B	A
000063	PCCR18	P	Q	X	E	D	C	B	A
000065	PCCR19	P	Q	X	E	D	C	B	A
000067	PCCR20	P	Q	X	E	D	C	B	A
000069	PCCR21	P	Q	X	E	D	C	B	A
00006B	PCCR22	P	Q	X	E	D	C	B	A
00006D	PCCR23	P	Q	X	E	D	C	B	A
00006F	PCCR24	P	Q	X	E	D	C	B	A
000071	PCCR25	P	Q	X	E	D	C	B	A
000073	PCCR26	P	Q	X	E	D	C	B	A
000075	PCCR27	P	Q	X	E	D	C	B	A
000077	PCCR28	P	Q	X	E	D	C	B	A
000079	PCCR29	P	Q	X	E	D	C	B	A
00007B	PCCR30	P	Q	X	E	D	C	B	A
00007D	PCCR31	P	Q	X	E	D	C	B	A
000081	RSR1	CH8	CH7	CH6	CH5	CG4	CH3	CH2	CH1
000083	RSR2	TS16 1	CH15	CH14	CH13	CH12	CH11	CH10	CH9
000085	RSR3	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16
000087	RSR4	TS16 5	CH30	CH29	CH28	CH27	CH26	CH25	CH24
000089	RSR5	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
00008B	RSR6	TS16 2	CH15	CH14	CH13	CH12	CH11	CH10	CH9
00008D	RSR7	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16
00008F	RSR8	TS16 6	CH30	CH29	CH28	CH27	CH26	CH25	CH24
000091	RSR9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
000093	RSR10	TS16 3	CH15	CH14	CH13	CH12	CH11	CH10	CH9
000095	RSR11	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16
000097	RSR12	TS16 7	CH30	CH29	CH28	CH27	CH26	CH25	CH24
000099	RSR13	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
00009B	RSR14	TS16 4	CH15	CH14	CH13	CH12	CH11	CH10	CH9
00009D	RSR15	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16
00009F	RSR16	TS16 8	CH30	CH29	CH28	CH27	CH26	CH25	CH24
0000A1	NEMR1	CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0
0000A3	NEMR2	0	0	0	0	0	0	CRC9	CRC8
0000A5	NEMR3	FAS7	FAS6	FAS5	FAS4	FAS3	FAS2	FAS1	FAS0
0000A7	NEMR4	SEF1	SEF0	0	0	FAS11	FAS10	FAS9	FAS8
0000A9	NEMR5	BPV7	BPV6	BPV5	BPV4	BPV3	BPV2	BPV1	BPV0
0000AB	NEMR6	0	0	0	0	BPV11	BPV10	BPV9	BPV8
0000AD	FEPR1	FEBE7	BEFE6	FEBE5	FEBE4	FEBE3	FEBE2	FEBE1	FEBE0
0000AF	FEPR2	0	0	0	0	0	0	FEBE9	FEBE8

Figure 2 VMEbus Address Map -BtP9170

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Shown below in Figure 3 is the VMEbus address map for the IP-E1 hardware specific registers.

Addr (Hex)	Reg Lable	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
000201	FIFO	UNOV	IVBA	RX/TX	CH4	CH3	CH2	CH1	CH0
000203	MODE	ATTN	HYPER	EN9170	ENFIFO	T1/E1	MDFS	HCS1	HCS0
000205	IVECT0	user	user	user	user	user	user	user	user
000207	IVECT1	user	user	user	user	user	user	user	user

Figure 3 VMEbus Address Map -IP-E1 Hardware Specific Registers

See the Programming section and the BtP9170 data sheet included in the IP-E1 Engineering Kit for register definition details.

Note1: Reserved for factory test; must remain zero.

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ISA [PC-AT] Bus Addressing

ISAbus addressing requires computing the address from the byte addresses given above under VMEbus Addressing. The formula is:

ISAbus byte address = VMEbus byte address - 1

All registers byte data is transferred on data lines D7..D0. This byte is the even byte in Intel family host architecture. Any access to registers on data lines D15..D8 is ignored.

Even byte accesses to SRAM are on data lines D7..D0, odd bytes on D15..D8, and even words on D15..D0.

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NuBus Addressing

NuBus addressing requires computing the address from the byte addresses given above under VMEbus Addressing. The formula is:

ISAbus byte address = (VMEbus byte address * 2) - 1

All registers byte data is transferred on data lines D7..D0. Any access to registers on data lines D15..D8 is ignored.

Words addresses on the NuBus are the same as for VME. Word data is transferred on data lines D15..D0.

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Programming

This section provides the description of registers and programming details specific to the implementation of the BtP9170, Bt8071A and Bt8069B on the IP-E1. For a detailed functional description of the BtP9170, Bt8071A, and Bt8069B, refer to their respective data sheets included in the Engineering Kit. An understanding of the corresponding data sheets is prerequisite to an understanding of this section and beyond.

Intelligent E1 Controller- BtP9170

Figure 2 provides the VMEbus address map for the BtP9170 registers. All the register definition and functions as outlined in the data sheet is applicable on IP-E1. In addition, the peripheral I/O pins (PIO1*, PIO2*, PIO3* and PIO4*) are connected to monitor the Bt8071A channel status interrupt signal (IntReq0*), to control the Bt8071A RESET Signal and to control the Bt8069B CB and RESET signals. PIO3*, PIO2* and PIO1* pins have external pull-up resistors.

As described in the BtP9170 data sheet, the four low-order register bits of MR2 monitor the status of the peripheral I/O signals. Note that the PADE bit and the low-order bit of CR3 must be set to 0 to allow the low-order bit of this register to function as an input. These bits are used as follows:

PRD3 is EN8071 Enable Bt8071A. This bit monitors the corresponding bit in register CR3

PRD2 is EN8069 Enable Bt8069B. This bit monitors the corresponding bit in register CR3

PRD1 is CB Center/Bypass Elastic Store. This it monitors the corresponding bit in CR3

PRD0 is IntReq0 IP Interrupt Request 0. This bit monitors the interrupt status of the Bt8071A channel status FIFO

0 = No interrupt pending, FIFO is empty
1 = Interrupt pending, FIFO is not empty

The following bit setting in the CR3 register is a requirement of the hardware implementation:

PADE Peripheral Active Drive Enable. This bit must be 0

0 = PIOx signals are open drain, bidirectional

The four low-order bits in the CR3 register control the outputs of the peripheral I/O signals. When CR3 bit PADE is 0, the outputs are open drain (pulled high by pull-up resistors). These bits are set as follows:

PTD3 is EN8071 Enable Bt8071A. This bit controls the run/reset status of the Bt8071A

0 = Reset (default upon power-up)
1 = Bt8071A enabled

PTD2 is EN8069 Enable Bt8069B. This bit controls the run/reset status of the Bt8069B

0 = Reset (default upon power-up)
1 = Bt8069B enabled

PTD1 is CB Center/Bypass Elastic Store. This bit controls the Bt8069B CB signal (note inverted polarity)

0 = RX elastic store is bypassed (default upon power-up)

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1/0 = Elastic store is centered when this bit is changed from 1 to 0

PT1D0 is Bit 0 — This bit must be zero (default upon power-up)

32-Channel HDLC Controller- Bt8071A

The Bt8071A is controlled via the Mode register , and is interfaced to a status FIFO as well as shared SRAM for command/status buffer. The Mode register is explained in Mode subsection of this section.

The Bt8071A signal UAEN* is tied to logic 0, forcing the first 256 bytes of SRAM as System Memory. The table in figure 4 outlines the SRAM partitioning for channel allocation.

The SRAM is dual-ported between the Bt8071A and the IP host CPU. Only one master at a time can access the SRAM. The access to SRAM is arbitrated by the on-board logic. The host accesses the SRAM in three IP clocks (375 nsec) unless there is an access already in progress by the Bt8071A. Depending on the timing of assertion of Bt8071A bus request signal DMND, there is a possibility of wait states being imposed on the host CPU. This is due to higher arbitration priority of Bt8071A over the host CPU. The host finishes its SRAM access in its normal three IP clocks if its memory cycle precedes the DMND assertion by at least one IP clock, otherwise the host will be put in wait state till DMND is negated and then finishes its cycle in three IP clocks. IP clock running at 8 MHz has a period of 125 nano seconds. The IP clock is not synchronized to the Bt8071A TCLK signal, therefore there are no phase relationship between the two. The timing of Bt8071A access to the SRAM, including DMND is the same as Bt8071A data sheet timing figures. It is recommended to system integrators to run their application software in the actual system to measure an accurate throughput access to the SRAM by both masters.

The access to the SRAM by the Bt8071A is byte- wide, and the host CPU at byte- or word-wide. Obviously the host access at word-wide yield higher data throughput.

Mode Register

The Mode register is one of the IP-E1 hardware specific registers and participates in controlling the Bt8071A, the BtP9170, and the FIFO. See Figure 3 for VMEbus addressing of this register. The Mode register bits are used as follows:

Bit]7] ATTN [R/W]
Bt8071 Attention. When set to 1, the Bt8071A fetches the Channel Activation Byte and Channel Buffer Pointers from shared SRAM (segment 0). When the Bt8071A is finished, it asserts ATACK, which resets this bit. Reading the Mode register bit 7 will reflect the current status of the Bt8071A ATTN signal.

Bit[6] HYPER [R/W]
Hyperchannel SRAM Address Mode. See SRAM access table in Figure 4.
0 = Disable Hyperchannel Address Mode
1 = Enable Hyperchannel Address Mode

Bit[5] EN9170 [R/W]
Enable BtP9170. This bit directly controls the BtP9170 PUP* pin.
0 = Reset BtP9170
1 = Enable BtP9170

Bit[4] ENFIFO [R/W]
Enable Bt8071A Status FIFO

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0 = Reset FIFO
1 = Enable FIFO

Bit[3] T1/E1 [R]
Bt8071A T1/E1 Framing Select
0 = E1 Framing Mode selected

Bit[2] MDFS [R/W]
Bt8071A Memory Data Format Select.
0 = Select Intel 8086 Data Format
1 = select Motorola 68K Data Format
This bit must be set to 1 for Motorola 68K IP host CPU, and set to 0 for Intel 8086 host CPU.

Bit[1..0] HCS1, HCS0 [R/W]
Bt8071A Hyperchannel Select. See the Bt8071A data sheet for these signals.

The power-up or the reset default value of this register is $08.

Line Interface Controller- Bt8069B

The Bt8069B frequency standard is an external 8.192 MHz, parallel resonant crystal as described in the data sheet. Control for the Bt8069B line equalization, mode and status is provided through the appropriate interface signals and register bits in the BtP9170.

FIFO

The 256-byte FIFO is a companion device to the Bt8071A. The Bt8071A queues the channel number and its current buffer status into the FIFO as described in the data sheet. The FIFO Empty Flag drives the IP interrupt request 0 as long as it has data in its queue. The inverted state of this flag can be read by general purpose line PIO0* of the BtP9170. The Empty Flag is set to 1 when not empty. The FIFO may be set at any time under the Mode register control. The default status of Empty Flag upon reset or power-up is 0.

The host may read the FIFO content by reading the FIFO register. See Figure 3 for VMEbus address of this register. The FIFO content should be ignored when it is empty. The FIFO register bits are used as follows:

Bit[7] UNOV [R]

Bit[6] IVBA [R]

Bit[5] RX/TX [R]

Bit[4..0] Channel 4..0 [R]

Refer to the Bt8071A data sheet for description of these bits.

SRAM

The one MByte SRAM is divided into 16 segments of 64 kilobytes each. Memory segments are shared between channels as listed in the Figure 4 below. The Bt8071A system access is made from the first 256 bytes of segment 0. The Bt8071A addresses memory segments in either Normal Address Mode or Hyperchannel Address Mode.

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Hyperchannel Address Mode also uses the RX/TX signal for memory segment selection. A Bt8071A channel access selects memory segments via its CH0-CH4 signals for Normal Address Mode and via the RX/TX and CH0-CH4 signals for the Hyperchannel Address Mode. Address bits A0-A15 select a byte displacement within the selected 64 Kbyte segment.

Hyperchannel Address Mode is enabled by the HYPER bit in the Mode register. Segments containing multiple channels in the selected Figure 4 entry, must be shared among the channels listed.

Address Hex Offset	**Segment**	**Normal Address Mode Channel Allocation** (Shared TX/RX Channels)	**Hyperchannel Address Mode Channel Allocation** (Separate TX/TX Channels)
10 0000	0	1 & Bt8071A sys access	1-3 TX
11 0000	1	2 & 3	1-3 RX
12 0000	2	4 & 5	4-7 TX
13 0000	3	6 & 7	4-7 RX
14 0000	4	8 & 9	8-11 TX
15 0000	5	10 & 11	8-11 RX
16 0000	6	12 & 13	12-15 TX
17 0000	7	14 & 15	12-15 RX
18 0000	8	TS16 & 16	TS16-18 TX
19 0000	9	17 & 18	TS16-18 RX
1A 0000	10	19 & 20	19-22 TX
1B 0000	11	21 & 22	19-22 RX
1C 0000	12	23 & 24	23-26 TX
1D 0000	13	25 & 26	23-26 RX
1E 0000	14	27 & 28	27-30 TX
1F 0000	15	29 & 30	27-30 RX

Figure 4 SRAM Channel Allocation

The Bt8071A RX/TX buffers should be allocated on even byte boundaries in order to facilitate word length parameters in buffer headers as well as data transfers on the IP bus. Note that according to the data sheet, the Bt8071A buffers can not begin at the first byte of a segment. (The resulting buffer pointer is null and the Bt8071A ignores the buffer.)

Interrupts

The FIFO Empty Flag directly drives the IP interrupt request 0 through an inverter. The IP Intreq 0 signal is asserted as long as it has data in its queue.

The BtP9170 INTR* signal directly drives the IP interrupt request 1. See the BtP9170 data sheet for causes of assertion of this signal

The IVECT0 and IVECT1 are byte-wide, read/write registers containing the interrupt vectors which are transferred to the IP host CPU during interrupt acknowledge cycles. IVECT0 and IVECT1 are interrupt vector registers for the FIFO and the BtP9170 respectively. See Figure 3 for VMEbus address map for these registers.

The power-up or the reset value of these registers are $00. These registers must be initialized to appropriate vectors before any interrupts are allowed to occur.

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Xilinx FPGA

The Xilinx FPGA includes the IP host interface to the SRAM, BtP9170, Bt8071A, SRAM arbitration, data transceivers, address latches, ID PROM, and four registers as shown in Figure 3. With the exception of the registers, all the FPGA functions are just hardware implementation and totally transparent to the programmer. The Figure 3 registers are described in the above paragraphs.

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ID PROM

Every IP contains an IP PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto-configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires a particular revision IP, it may check for it directly.

Standard data in the ID PROM on the IP-E1 is shown in Figure 5 below.
For more information on IP ID PROMs refer to the IndustryPack Logic Interface Specification, available from GreenSpring Computers. The ID PROM is implemented in the Xilinx FPGA.

The location of the ID PROM in the host's address space is dependent on the carrier used. Normally for VMEbus carriers the ID PROM space is directly above the IP's I/O space, or at IP-base + $80. Macintosh drivers use the ID PROM automatically. RM1260 address may be derived from Figure below by multiplying the addresses given by two, then subtracting one. RM1270 addresses may be derived by multiplying the addresses given by two, then adding one.

3F 2D	(available for user)	
17	CRC for bytes used	(81)
15	No of bytes used	(0C)
13	Driver ID, high byte	(00)
11	Driver ID, low byte	(00)
0F	reserved	(00)
0D	Revision	(A5)
0B	Model NoIP-E1	(80)
09	Manufacturer ID GreenSpring	(F0)
07	ASCII "C"	(43)
05	ASCII "A"	(41)
03	ASCII "P"	(50)
01	ASCII "I"	(49)

Figure 5 ID PROM Data (hex)

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I/O Pin Wiring

This section gives the I/O pin assignment for the IP-E1

The pin numbers given in Figure 6 correspond to numbers on the 50-pin IndustryPack I/O connector, to the wires on a 50-pin flat cable plugged into a standard IP carrier board, and to the screw terminal numbers on the IP-Terminal block.

I/O Cable Pin No.	Signal	I/O Cable Pin No.	Signal
1	GND	26	N/C
2	TXP	27	N/C
3	GND	28	N/C
4	TXN	29	N/C
5	GND	30	N/C
6	GND	31	N/C
7	RXN	32	N/C
8	GND	33	N/C
9	RXP	34	N/C
10	GND	35	N/C
11	N/C	36	N/C
12	N/C	37	N/C
13	N/C	38	N/C
14	N/C	39	N/C
15	N/C	40	N/C
16	N/C	41	N/C
17	N/C	42	N/C
18	N/C	43	N/C
19	N/C	44	N/C
20	N/C	45	N/C
21	N/C	46	N/C
22	N/C	47	N/C
23	N/C	48	N/C
24	N/C	49	N/C
25	N/C	50	N/C

Figure 6 IP-E1 I/O Pin Assignment

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Figure 7 details the Bt8069B Line Interface Unit interface to the E1 cable through individual transformers. The standard values are 75? and 120? for R15, and 0? for R18. These values correspond to 75? and 120? line impedance interface. Other line impedances may be accommodated by substituting R15 and R18 values, as shown in the Bt8069B data sheet.

Customer special interface circuitry may be placed on an external transition board by omitting R15, and replacing the transformers with jumpers.

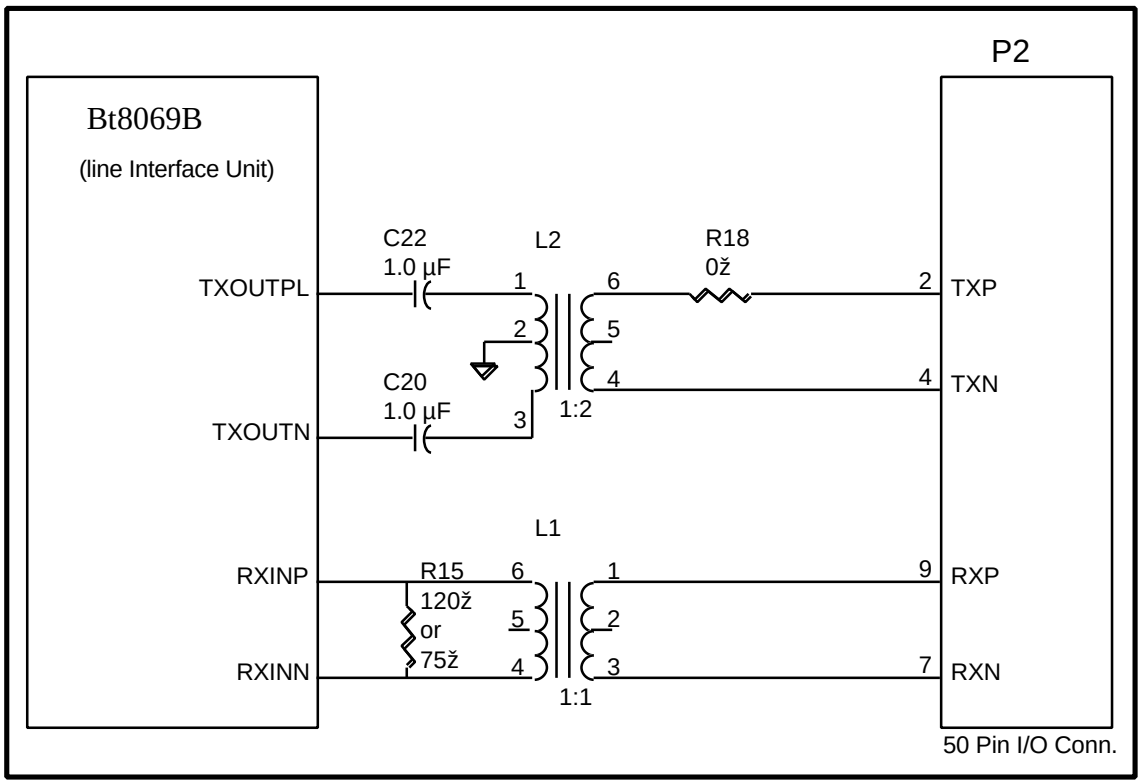


Figure 7 IP-E1 Line Interface Unit

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IndustryPack Logic Interface Pin Assignment

Figure 8 below gives the pin assignments for the IndustryPack Logic Interface on the IP-E1. Pins marked n/c below are defined by the specification, but not used on IP-T1. Also see the User Manual for your IP Carrier board for more information.

GND	GND	1	26	
CLK	+5V		2	27
Reset*	R/W*	3	28	
D0	IDSel*		4	29
D1	n/c	5	30	
D2	MEMSel*		6	31
D3	n/c	7	32	
D4	INTSel*		8	33
D5	n/c	9	34	
D6	n/c		10	35
D7	n/c	11	36	
D8	A1		12	37
D9	n/c	13	38	
D10	A2		14	39
D11	n/c	15	40	
D12	A3		16	41
D13	IntReq0*	17	42	
D14	A4		18	43
D15	IntReq1*	19	44	
BS0*	A5		20	45
BS1*	n/c	21	46	
n/c	A6		22	47
n/c	Ack*	23	48	
+5V	n/c		24	49
GND	GND	25	50	

Note 1: The no-connect (n/c) signals above are defined by the IndustryPack Logic Interface Specification, but not used by this IP. See the Specification for more information.

Note 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IndustryPack.

Figure 8 Logic Interface Pin Assignment

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Construction and Reliability

IndustryPacks were conceived and engineered for rugged industrial environments. The IP-E1 is constructed out of 0.062 inch thick FR4 V0 material. The six copper layers consist of two signal layers on the top and bottom, and four internal layers. Two internal layers are dedicated to power and ground planes. Two additional layers are used for signal wiring.

The IndustryPack connectors are keyed, shrouded and gold plated on both contacts and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured to the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications they are not required.

The IndustryPack provides a low temperature coefficient of 0.89 W/°C for uniform heat. This is based on the temperature coefficient of the base FR4 material of .31 W/m-°C, and taking into account the thickness and area of the IP. This coefficient means that if 0.89 Watts is applied uniformly on the component side, that the temperature difference between the component and the solder side is one degree Celsius.

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For Service Contact:

Customer Service Department
GreenSpring Computers
1204 O Brien Drive
Menlo Park, CA 94025
(415) 327-1200
(415) 327-3808 fax
InterNet Address support@gspring.com

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Specifications

This section gives the technical specification for the IP-E1

LSI Chip	Brooktree BtP9170 Intelligent E1 Controller Brooktree Bt8071A 32-Channel HDLC Controller Brooktree Bt8069B Line Interface Unit
Crystal Frequency	8.192 MHz provided to Bt8069B- parallel resonant @ -18 dB third harmonic
FIFO	Integrated Devices IDT7200, 256 Bytes
Memory	High-speed one Mbyte volatile Dual-Port SRAM
Logic Interface	Xilinx Field Programmable Gate Array (FPGA)
I/O Interface	Direct interface to standard E1 cable via transformers. 120? (standard) and 75? (optional) line impedance interface is supported.
Protocols	E1, ISDN, HDLC, SDLC, X.25, X.75, LAPB, LAPD
Initialization	Hardware Reset initializes on-board logic and LSI chips. Software reset through control registers.
Access Modes	Byte or word in memory space Byte in ID Space Vectored interrupt
Wait States	Depends on access type. Host SRAM access at one wait state typ. See Programming Section
Interrupt	IP Interrupt Request on Levels 0 and 1 Independent vector registers provided
Onboard Options	All Options are Software Programmable
IndustryPack Specification	Logic Interface Specification Revision 0.7.1 Type II (components on the back)
Dimensions	Standard Single IndustryPack width and length. 1.8 x 3.9 inches Maximum component height on the back at 0.0625 Inches (type II)
Construction	6 Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed.
Temperature Coefficient	.89 W/°C for uniform heat across IP

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Test conditions	20°C, typical
Power Requirements	+5 VDC, 250 mA typ +12 VDC, 0 mA typ –12 VDC, 0 mA typ
Environmental	Operating temperature: 0 to 70°C Humidity: 5 - 95% non-condensing Storage temperature: –10 to +85°C

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