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Find the *Abaco Systems / SBS / Greenspring IP-FASTDAC-8* at our website: *Click HERE*

IP-FASTDAC

8 channel 16 bit 2uS Digital to Ananlog Converter
With 4 Quadrant Multiplier
Industry Pack Module

REFERENCE MANUAL

801-10-000-4000
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ALPHI TECHNOLOGY CORPORATION

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TABLE OF CONTENTS

1. GENERAL DESCRIPTION ***1***

1.1 INTRODUCTION **1**

1.2 FUNCTIONAL DESCRIPTION **1**

2. INTERNAL ORGANIZATION ***2***

2.1 IP INTERFACE **2**

2.1.1 IDSPACE 2

2.1.2 IOSPACE 3

2.1.3 INTSPACE 4

2.1.4 Memory space 4

2.2 ANALOG OUTPUT **4**

3. JUMPER SETTINGS ***6***

4. JUMPER LOCATION ***6***

5. Vref BLOCK DIAGRAM ***6***

6. OUTPUT CONNECTOR ***7***

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1. GENERAL DESCRIPTION

1.1 INTRODUCTION

The **IP-FASTDAC** is a high performance DIGITAL TO ANALOG module. The **IP-FASTDAC** digitizes 8 channels with 16 bits of resolution at a maximum conversion rate of 2 μS.

The primary features of the **IP-FASTDAC** are as follows:

- Eight channels-16 bit - 2 μS D/A converters with on-chip 4-quadrant multiplication resistors for accurate +/-10V bipolar conversion.
- Individual buffer for each output.
- +/-10 volt outputs.

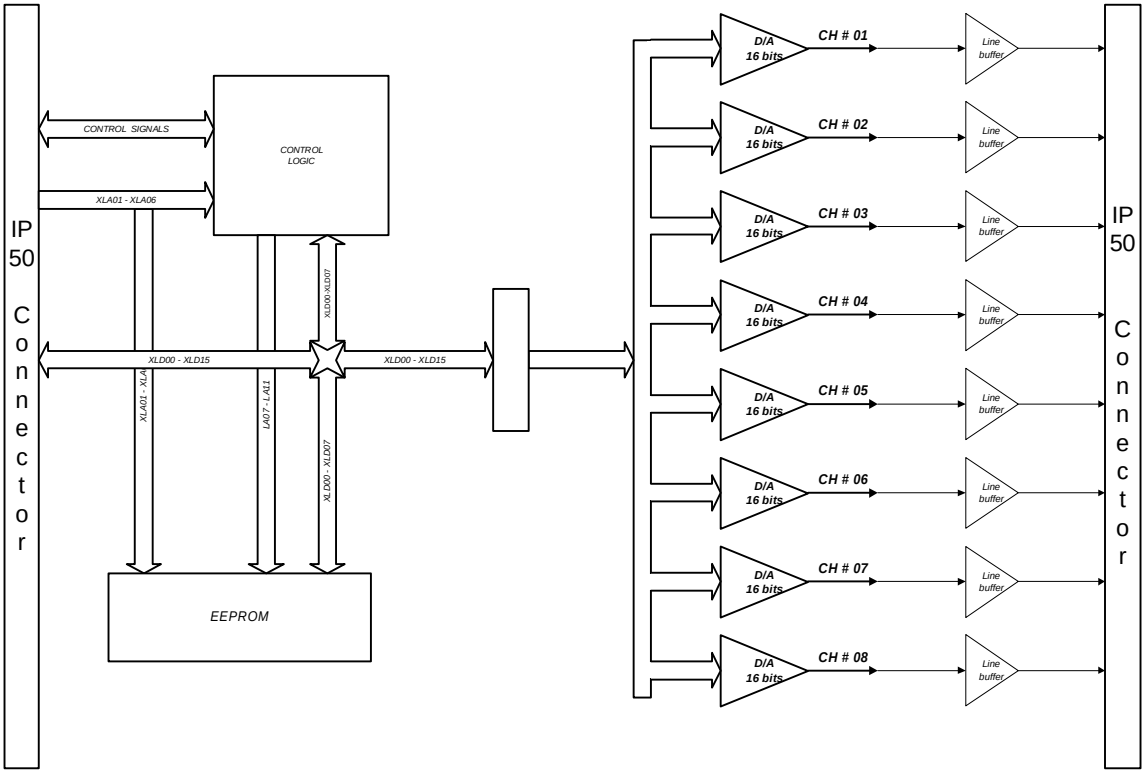
1.2 FUNCTIONAL DESCRIPTION

A functional block diagram of the **IP-FASTDAC** is presented below in Figure 1-1.

The **IP-FASTDAC** operates as a slave that is managed by the host processor on the IP bus.

The **IP-FASTDAC** is supported by ALPHI Technology under *Windows NT* by a **Board Support Package** which is supplied with the card. Other documentation supplied with the card will describe this support in full detail.

Figure 1.1: Block Diagram



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2. INTERNAL ORGANIZATION

The **IP-FASTDAC** card is divided into different sections. Each section and its relationship to other sections will be discussed. The **IP-FASTDAC** sections are:

- IP interface
- Analog Output

2.1 IP INTERFACE

2.1.1 IDSPACE

An EEPROM memory that occupies 2 Kbytes of address space is for providing information about the module to the user. The lower address contains data related to the type of module, revision, etc...

The Upper space can be used to store information. Only the ODD address is valid. Each IP conforms to the IP Bus Specification and has 32 bytes of EEPROM that can be read by the local Host to identify the IP module Manufacturer, type, revision, etc.

Left over memory (2K-32 byte) is available to the user to store information related to the module offset gain error for eventual software correction

ID space address	Description	Value
$01	ASCII “I”	$49
$03	ASCII “P”	$50
$05	ASCII “A”	$41
$07	ASCII “H”	$48
$09	Manufacturer identification	$11
$0B	Module type	$17
$0D	Revision module	$0B
$0F	Reserved	
$11	Driver ID,low byte	
$13	Driver ID,high byte	
$15	Number of bytes used	$0A
$17	CRC	
$19-$3F	User space	

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Table 2-1 FLASH byte content

Address $01-$07 identifies “IPAH”. Also this identifies the EEprom beginning.

2.1.2 IOSPACE

2.1.2.1 LOCAL REGISTERS

The IP-FASTDAC module uses 8 - LTC1821 Ultra precise fast setting V-out D/A converters from Linear Technology. A double buffered interface is used to transfer incoming data to the output. The first 8 ($00 - $0E) addresses are used to pre-load data into the first stage of each D/A converter. A write to the address $10 – DAC-OUT will transfer the data to the outputs in a synchronous manner. The Next 8 ($20 - $2E) addresses are used to transfer data directly to the output. The eight registers associated, one for each channel are located in the I/O space.. See I/O memory map below for more details.

Offset	Register Name	Function
$00	Ch # 1	First register stage pre-load of D/A # 1
$02	Ch # 2	First register stage pre-load of D/A # 2
$04	Ch # 3	First register stage pre-load of D/A # 3
$06	Ch # 4	First register stage pre-load of D/A # 4
$08	Ch # 5	First register stage pre-load of D/A # 5
$0A	Ch # 6	First register stage pre-load of D/A # 6
$0C	Ch # 7	First register stage pre-load of D/A # 7
$0E	Ch # 8	First register stage pre-load of D/A # 8
$10	DAC_OUT	Analog Output update of all D/A’s
$18	DAC_RST	D/A reset
$1A	8/32Mhz	$1 = 8Mhz / $0 = 32Mhz IP-Clock
$20	Ch # 1	Direct transfer of Data to Output D/A # 1
$22	Ch # 2	Direct transfer of Data to Output D/A # 2
$24	Ch # 3	Direct transfer of Data to Output D/A # 3
$26	Ch # 4	Direct transfer of Data to Output D/A # 4
$28	Ch # 5	Direct transfer of Data to Output D/A # 5
$2A	Ch # 6	Direct transfer of Data to Output D/A # 6
$2C	Ch # 7	Direct transfer of Data to Output D/A # 7
$2E	Ch # 8	Direct transfer of Data to Output D/A # 8

Table 2.1: Registers

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8/32Mhz register

This IP is designed to run at 32Mhz default, the register address $1A can allow 8Mhz functionality by writing a $1 to the register. See chart below for each functions wait state.

IP-Clock	DAC FUNCTION	Wait States
32Mhz	Stage Pre-Load	2
32Mhz	Analog Output Update	3
32Mhz	Direct Transfer	5
8Mhz	Stage Pre-Load	2
8Mhz	Analog Output Update	3
8Mhz	Direct Transfer	1

2.1.3 INTSPACE

Not Used.

2.1.4 Memory space

The on board EEPROM provides 2K – 32bytes space available for the user.

2.2 ANALOG OUTPUT

The **IP-FASTDAC** has eight analog outputs each with its own buffer.

The outputs are +/- 10 Volts.

DAC

LTC 1821 (16bit Ultra Precise, Fast Settling Vout DAC)

+/-10Volt Bipolar Offset

Input code - Binary only

2us Settling to 0.0015% for 10volt step.

1LSB Max DNL and INL over Industrial Temp range

Low Glitch Impulse: 2nV * s

Low Noise 13nV

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+/-10Volt Bipolar Offset Code table

Digital Input Binary Number In DAC Register	Analog Output Vout
MSB LSB	
1111 1111 1111 1111	Vref (32,767/32,768)
1000 0000 0000 0001	Vref (1/32,768)
1000 0000 0000 0000	0 volt
0111 1111 1111 1111	-Vref (1/32,768)
0000 0000 0000 0000	- Vref

OUTPUT BUFFER

IP-FASTDAC can be configured with either a high speed, high output current (BUF634) or High speed, low offset voltage (OPA132) input buffers. The specs are below for each device.

BUF634 (250mA High-Speed Input Buffer)

High Output Current : 250mA

Slew Rate : 2000V/us

Wide Bandwidth mode : 180Mhz

Input offset: Typ. = +/- 30 mV

OPA132 (High Speed OP-AMP)

Output Current : 4.8 mA

Slew Rate : 20V/us

Bandwidth : 8Mhz

Input offset : Typ = +/-0.25mV

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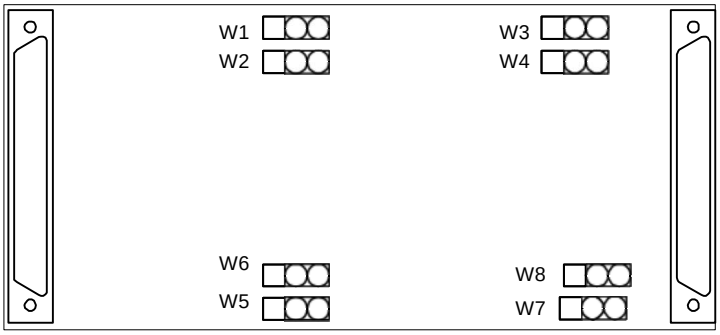
3. JUMPER SETTINGS

The IP-FASTDAC allows the possible of configuring each DAC channel for internal or external Vref supply. See chart below for configuration possibility. Factory default for Vref is internal +10 volts. A +5volt internal Vref can be accommodated upon request.

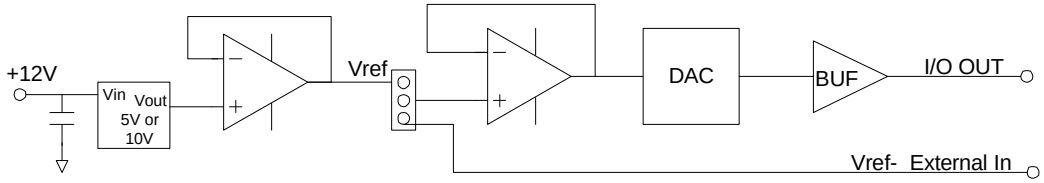
DAC Channel	Internal Vref supply +10v	External Voltage supply
DAC1	W8 = 1-2	W8 = 2-3
DAC2	W7 = 1-2	W7 = 2-3
DAC3	W6 = 1-2	W6 = 2-3
DAC4	W5 = 1-2	W5 = 2-3
DAC5	W4 = 1-2	W4 = 2-3
DAC6	W3 = 1-2	W3 = 2-3
DAC7	W2 = 1-2	W2 = 2-3
DAC8	W1 = 1-2	W1 = 2-3

4. JUMPER LOCATION

Square pad on PCB is pin 1.



5. Vref BLOCK DIAGRAM



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6. OUTPUT CONNECTOR

Pin	Signal	Pin	Signal
1		26	
2		27	AGND
3	DAC # 1	28	AGND
4	AGND	29	AGND
5	DAC # 2	30	AGND
6	AGND	31	
7	VREFX1	32	VREFX2
8		33	AGND
9	DAC # 3	34	AGND
10	AGND	35	AGND
11	DAC # 4	36	AGND
12	AGND	37	VREFX4
13	VREFX3	38	VREFX6
14	VREFX5	39	AGND
15	DAC # 5	40	AGND
16	AGND	41	AGND
17	DAC # 6	42	AGND
18	AGND	43	
19	VREFX7	44	VREFX8
20		45	AGND
21	DAC # 7	46	AGND
22	AGND	47	AGND
23	DAC # 8	48	AGND
24	AGND	49	
25		50	

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