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Installation and User's Guide

VxWorks Edition

Rev B

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SBS Technologies, Inc. Communications Products *Installation and User's Guide* for the K2 PowerPC 750/7400 embedded computer.

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Hardware

The SBS CompactPCI Development Chassis and K2 Single Board Computer (SBC) are both available from SBS Communications Products.

- E-mail: www.sbscomm.com
- Call: 888-SBS-COMM
- Fax: 760-438-6904

Software

VxWorks Tornado II V5.4 BSP is available from SBS Communications Products.

- E-mail: www.sbscomm.com
- Call: 888-SBS-COMM
- Fax: 760-438-6904

Printed and on-line Information

A K2 Data Sheet is available in Acrobat PDF format on the worldwide web at www.sbs-comm.com.

Printed copies of the *K2 Installation and User's Guide* are available from SBS by calling 888-SBS-COMM.

Advice

If you are unable to resolve questions from the information available on the web, please call Customer Service at 760-438-6900.

Service

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Chapter 1: Quick Start

These items are needed to set up and operate K2:

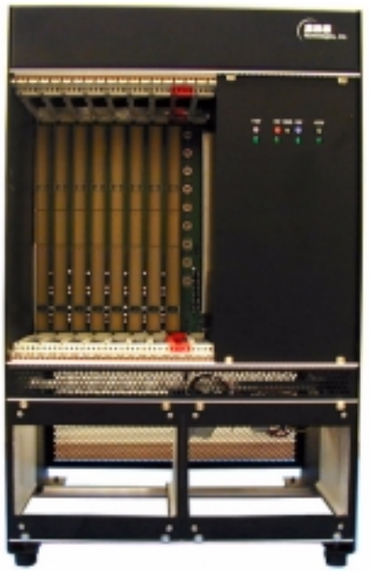
- K2 single board computer (SBC).
- A host computer.
- A CompactPCI chassis.
- An Ethernet cable.
- A serial cable.
- VxWorks Tornado II and appropriate VxWorks V5.4 Board Support Package (BSP).

> **Warning:** Always use proper Electrostatic discharge (ESD) protection when handling computer components to avoid seriously damaging them. Make certain you are properly grounded.

1.1 Hardware Setup

Shown below is a development CompactPCI chassis. K2 should be inserted into a similar chassis.

Figure 1-1, The SBS CompactPCI Development Chassis



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Important: The CompactPCI chassis may be either right or left justified. Therefore, the System slot, or slot one controller, will be either on the right or left side. With some CompactPCI chassis, the slot one controller may also be found in the middle. You may identify the controller slot by looking inside the CompactPCI chassis just above the J5 connectors. You will typically find that a diamond or triangle has been embossed over one slot. This diamond indicates the position of the slot one controller.

1.2 System Capability

1.2.1 Adjusting System Capability—J2 Jumper

The System slot is also called slot one. A CompactPCI system must have a System controller in slot one to provide clock and arbitration. K2 can be either a System or non-System controller. The board is designed to auto-sense it s location in the CompactPCI chassis and to configure accordingly.

If you plug K2 into slot one, it will configure itself as the System controller.

If you plug K2 into any other slot, it will configure itself as a non-System controller.

If the board is not placed in the System slot, it may still be forced to act as the System controller board simply by jumpering JP2.

If you remove the jumper on JP2, K2 will auto sense its location and configure itself accordingly as either a System controller or a peripheral board.

The JP2 jumper is located in the upper corner of K2, near the card edge connectors. See Figure 3-3, J6—JTAG Diagnostic Connector Pinouts, on page 3-4.

1.3 K2 Components

Photographs of K2 board and its components are shown in Figure 3-2, K2 Hot Swap CompactPCI Board, on page 3-3.

K2 is a CompactPCI single board PowerPC 750/7400 based computer. It has a PowerPC device that resides beneath the heat sink.

1.4 Hardware Installation and Setup

1. Ensure that JP2 is NOT jumpered.
2. Place K2 in Slot one the system Controller slot and lock it in place.
3. Connect the cables to communicate between the single board computer and your host computer as well as through the Ethernet.
   - Connect the host serial cable to K2's Com 1 port. Use Null modem if necessary. (COM 1 is configured as DTE.)
   - Connect the Ethernet cable to the Ethernet port. There are two ways to connect the cable. If connecting to a LAN through a gateway, use a standard Ethernet cable. If making a direct connection from a host computer to the system, use a loopback or crossover cable.

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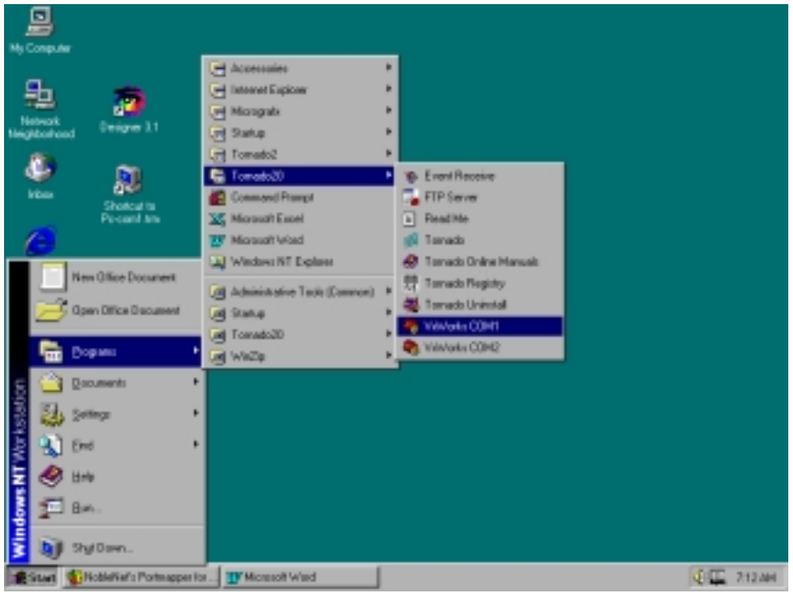
1.5 Software Setup

Tornado II software may be operated in Windows 95, 98, NT or any UNIX type environment. K2 requires both Tornado II and K2 Board Support Packages (BSPs) installed on the host computer. For the purpose of demonstration, this manual was written from a Windows perspective. The procedure involves:

1. Setting up a terminal/console.
2. Setting up an FTP server.
3. Configuring and booting K2.

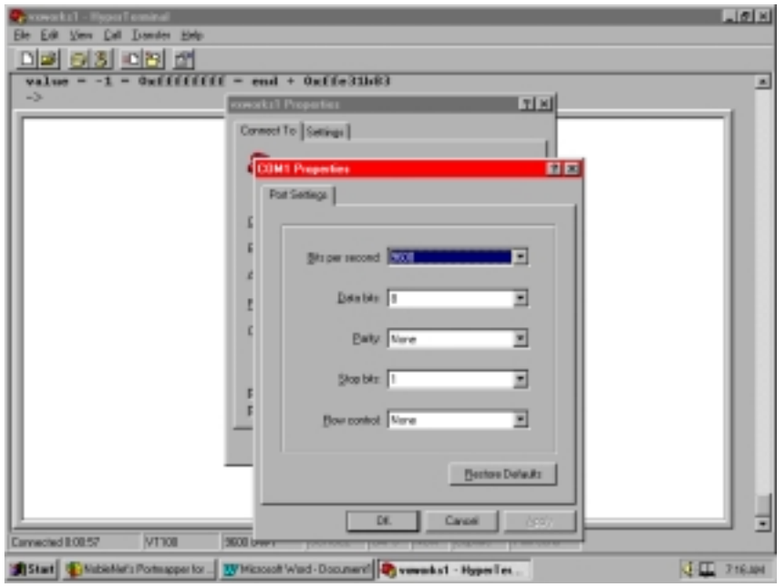
1.5.1 Procedure

1. Obtain the host IP address and, if necessary, gateway address.
2. Invoke Start > Programs > Tornado2 > Com1 to open a terminal/console window.
   (This assumes that the serial cable is plugged into COM1 of the host computer.)



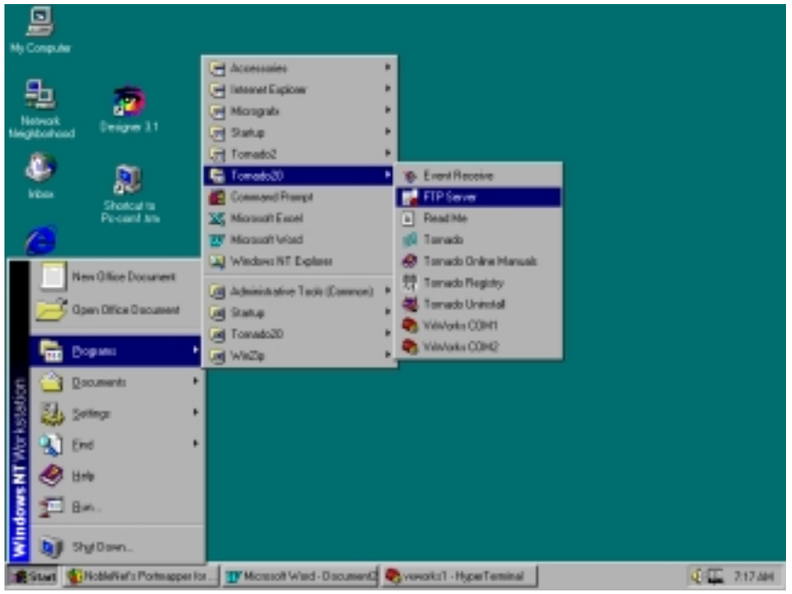
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3. Configure the serial port parameters. The default configuration is 9600, 8N1.



4. Invoke Start > Programs > Tornado2 > FTP Server.

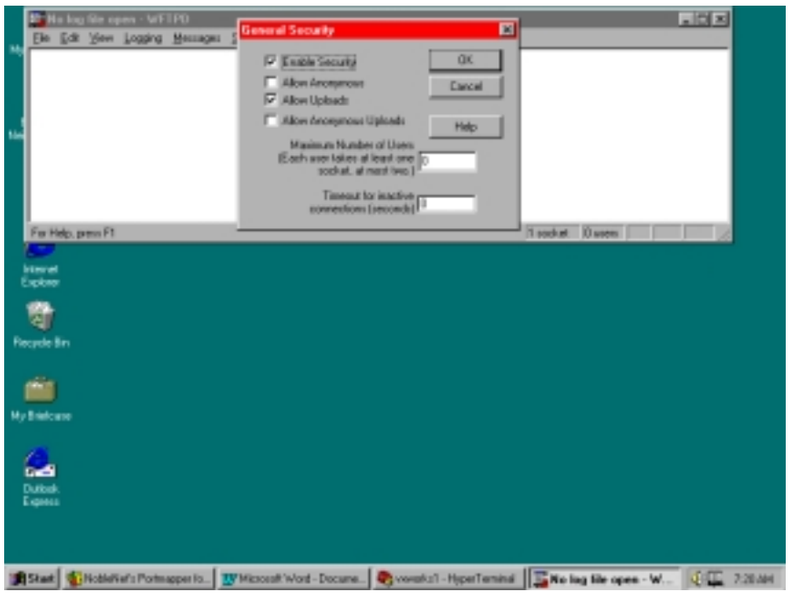
   An FTP server is necessary to pass files between the host and SBC.



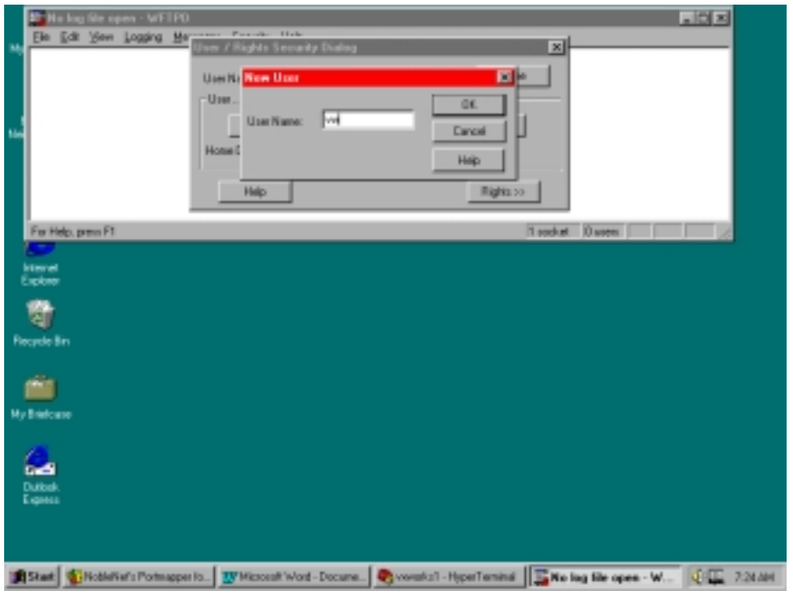
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5. Configure the FTP server as follows:

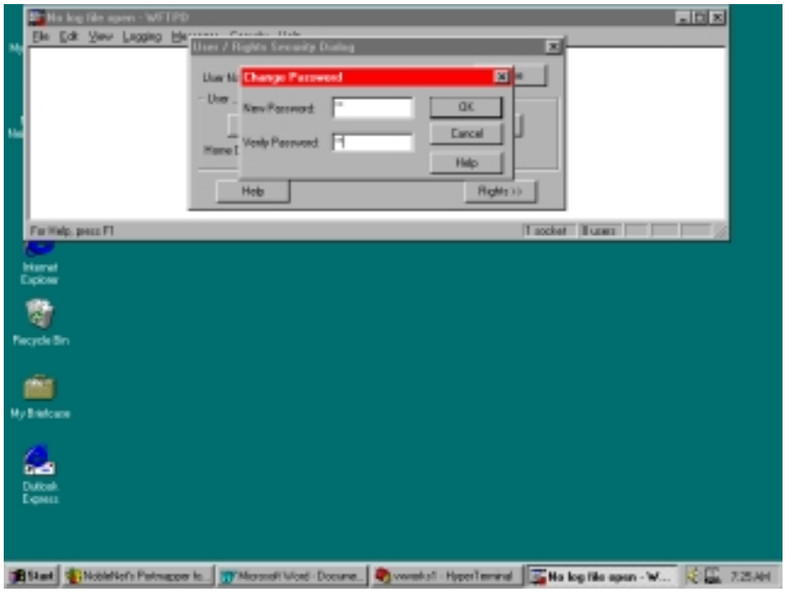
   Security > General



For user s rights: Security > Users/rights > New User



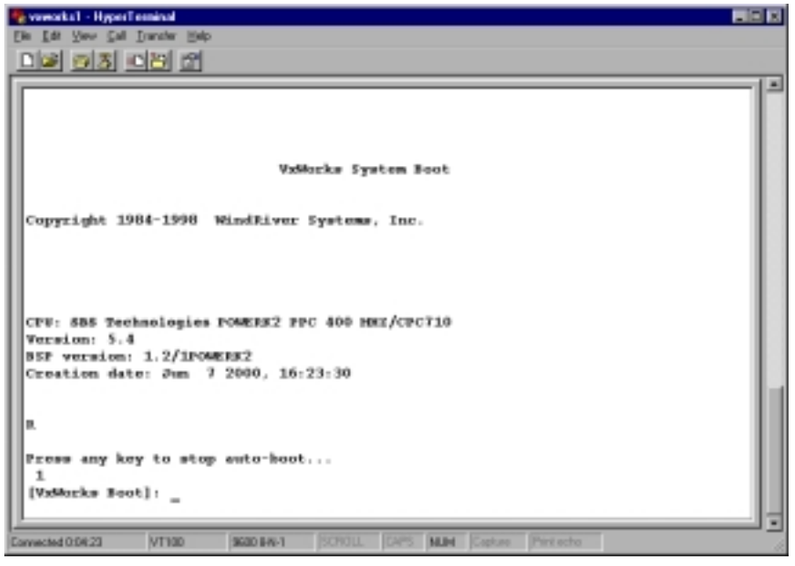
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The FTP server should be running.

1.5.2 Invoke Boot

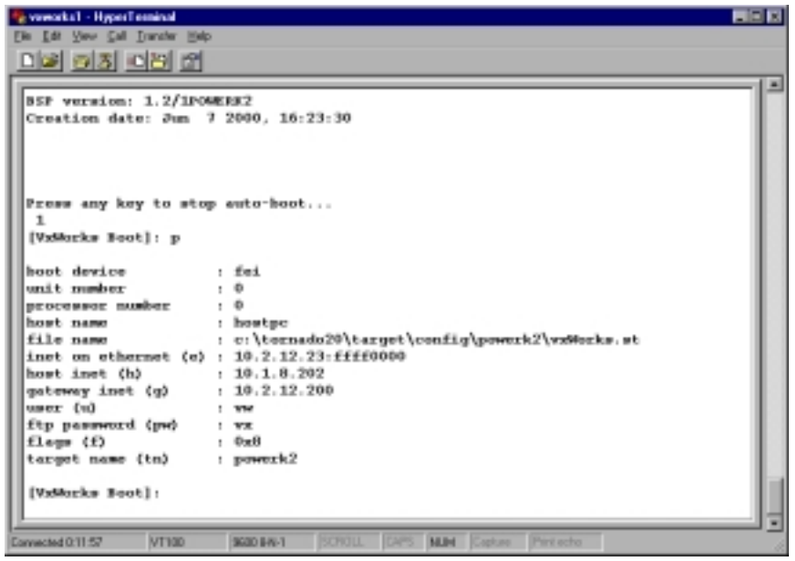
1. Turn power on to the CompactPCI chassis. The monitor port should display output through the Com 1 connection.



2. As the data begins to scrolls, press any key to halt the auto boot process.

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3. Press [p] to view pre-configured boot parameters.



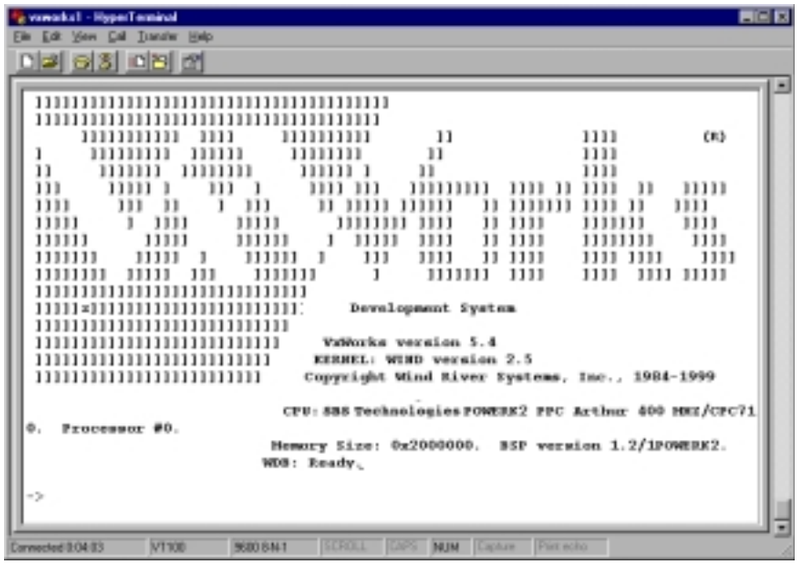
4. Press [c] to change individual boot parameters.
5. Enter new boot parameters followed by <Enter> to advance to the next field.

> **Tip:** Entering '.' clears a field.
>
> '_' goes to previous field.
>
> ^D quits.
>
> Refer to Tornado 2 user's manual for more information on VxWorks commands.

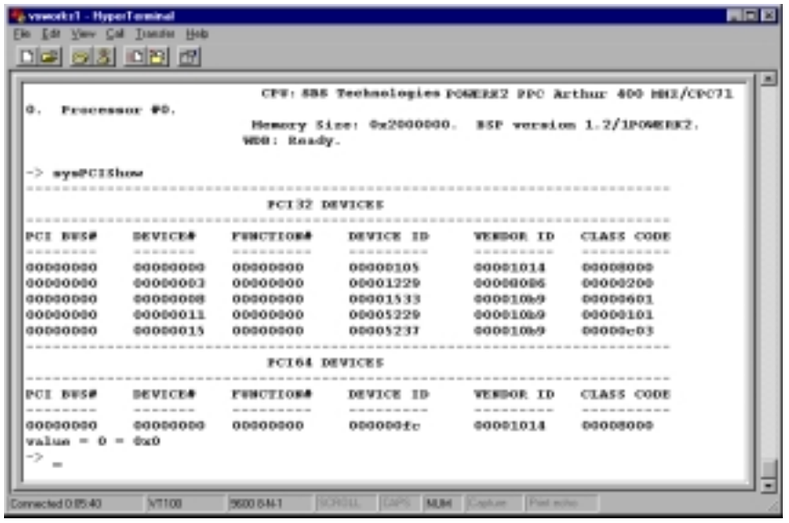
6. Press <Shift> @ when finished changing parameters to load.

   The VxWorks banner is now displayed.

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7. Try a few BSP utility commands to verify proper operation.
8. Enter at the boot prompt —> sysPCIShow



Five PCI devices on the **local bus** (PCI32) should be displayed; one PCI device on the CompactPCI (PCI64) should be displayed.

Application code may now be ported to K2.

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Chapter 2: Introduction

2.1 PowerPC 750 Hot Swap CompactPCI Features

- IBM PowerPC PPC750 to 500MHz, low power
- 1 MB IBM L2 cache
- IBM CPC710 PPC/PCI Bridge offers two independent buses
- Two PMC expansion slots for T1/E1, T3/E3, ATM and other communication I/O modules.
- Full hot swap per PICMG 2.1 R1.0
- 128 MB to 1 GB SDRAM
- 8 MB flash
- 100MHz system bus
- IDE interface
- 10/100 baseTX Ethernet
- Two debug ports (RS-232)
- Watchdog timer
- Sysslot or non-sysslot
- VxWorks and Linux drivers

K2 is a high performance, 6U CompactPCI single board computer. It is designed for use in a wide variety of computing applications including network switching and routing and front-end processing. The latest IBM PowerPC 750 is available in frequency options to 500MHz, features with 1 MB of L2 cache (running at 250MHz), 128 MB to 1 GB of SDRAM, 8 MB of flash memory and 512 KB of boot flash. To highlight it s flexibility, K2 has two PMC slots for the addition of LAN, WAN, graphics, or other I/O functions readily available from SBS and other third-party suppliers.

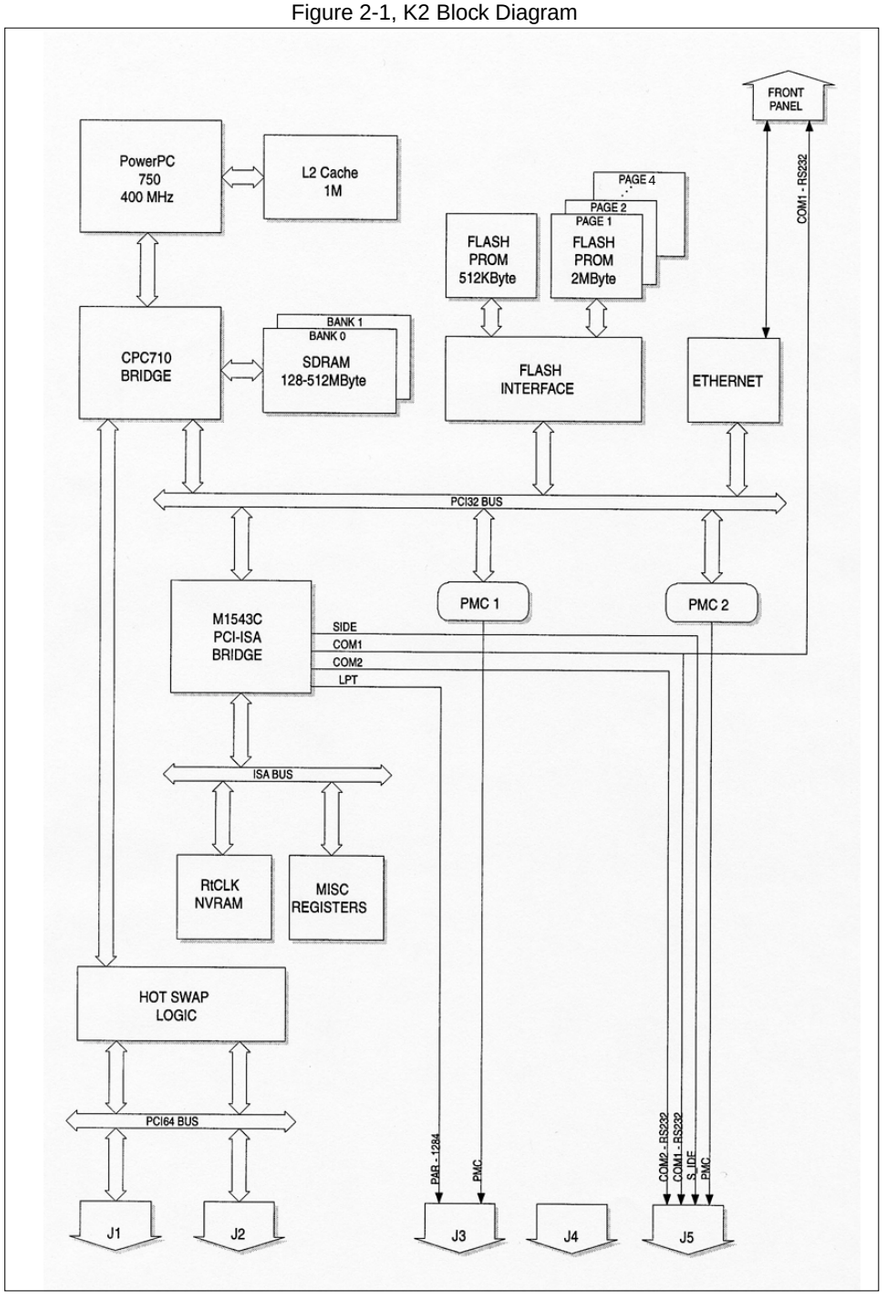
The system bus operates at 100MHz, and has a 64-bit interface between the processor, system memory and the CompactPCI bus. The card also features 10/100 Ethernet, two RS-232 debug ports, an IDE port, a parallel port, a real time clock, and a watchdog timer.

Using the industry standard CompactPCI 6U form factor, K2 occupies a single slot. The board is capable of operating as a System slot or non-system slot controller. K2 supports full hot swap modes as defined by PICMG 2.1 R1.0.

K2 is supported with the VxWorks Operating System. In addition, Linux has been ported for open system applications like high speed web servers and internet related firewalls or routers.

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Figure 2-1, K2 Block Diagram



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2.2 Specifications

IBM 750 PowerPC Processor
- 400MHz, 450MHz, 500MHz
- On-chip cache, 32K/32K

L2 Cache
- 1 MB
- 1/2 speed of the processor

IBM CPC710 Avignon Dual Bridge and Memory Ctlr
- 144-bit data path to memory, interleaved
- 32-bit PCI peripheral bus
- 64-bit, 33MHz CompactPCI bus

Memory
- 128 MB to 1 GB SDRAM, ECC
- 8 MB flash, organized as four 2 MB pages
- 512 KB socketed boot flash
- 32 KB NVRAM

PCI Interface Controllers
- 33MHz PCI bus clock
- 3.3V/5V

PMC Interface
- Two slots, 32-bit
- Conforms to IEEE P1386 and P1386.1
- Front panel and rear J5/J3 I/O
-

Ethernet
- Intel 82559
- 10/100BaseTX
- RJ-45 on front panel

See Figure 3-1, K2 Hot Swap CompactPCI Front Panel, on page 3-2.

IDE Interface
- Acer 1543C
- Secondary on J5

Serial Interface
- Two 16550 compatible ports
- RS232 to 115Kbps
- One port front panel or J5, one port J5
-

Ethernet
- Intel 82559
- 10/100BaseTX
- RJ-45 on front panel
- See Figure 3-1, K2 Hot Swap CompactPCI Front Panel, on page 3-2.

IDE Interface
- Acer 1543C
- Secondary on J5

Serial Interface
- Two 16550 compatible ports
- RS232 to 115Kbps
- One port front panel or J5, one port J5

Parallel Port
- Acer 1543C
- IEEE 1284 compliant on J3

Counters/Timers
- Three 16-bit timers
- SGS-Thompson M48T37Y Real Time Clock
- Watchdog timer

Full Hot Swap

Software
- VxWorks
- Linux

Operating temperature
- 0 to +55 degrees C ambient

Storage Temperature
- -40 to +85 degrees C

Humidity
- 10% to 95% (non-condensing)

Cooling
- Forced air 200 LFM (minimum)

Physical characteristics
- Single slot 6U CompactPCI
- Length: 233.5mm (9.18")
- Width: 160mm (6.29")

Warranty
- Three years

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2.3 Related Documents

For information on K2 components, refer to the following documents:

PPC750 Processor, IBM Corp.

http://www.chips.ibm.com/techlib/products/powerpc/datasheets.html

CPC710 Processor, IBM Corp.

http://www.fr.ibm.com/france/cdlab/avi.htm

RISC Microprocessor User s Manual, IBM Corp.

http://www.ibm.com/search?q=RISC+Microprocessor+User%27s+Manual&realm=ibm&v=10&lang=en&cc=us&Go.x=11&Go.y=13AMD 29LV040B data sheet, AMD publication # 21354, Rev. C.*

AMD 29LV040B data sheet, AMD publication #21354, Rev. C.*

http://www.amd.com/products/nvd/techdocs/techdocs.html

Intel Word-wide FlashFile, 28F640J3A data sheet, order # 290667-001.*

http://developer.intel.com/design/flcomp/SPECUPDT/298130.htm

Intel Fast Ethernet Multifunction PCI/Cardbus Controller Datasheet, Revision 2.0, order # 743892-002.

http://developer.intel.com/design/network/datashts/index.htm

M1543C Preliminary Data Sheet V1.10, Acer Labs*

http://www.acerlabs.com/eng/product/core/m1543c.htm

M48T37, 32K x 8 TIMEKEEPER SRAM, April 1998 Data Sheet, SGS-THOMSON.*

http://wwwgen.uni-paderborn.de/gbt/static_data/supplier/sgst/stonline/books/pdf/alpha/ds/m.htmDraft Supplement to 1993 version of ANSI/IEEE Document # 802.3u/d2

Draft Standard for a Common Mezzanine Card Family: CMC, IEEE Standards Department, P1386/Draft 2.0.

http://standards.ieee.org/catalog/drafts.html

Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC, IEEE Standards Department, P1386.1/Draft 2.0.

http://standards.ieee.org/catalog/drafts.html

Compact PCI Specification, Revision 1.0

https://www.picmg.org/gspecorderformsec.htm

PICMG 2.3 R1.0, PMC on CompactPCI®

https://www.picmg.org/gspecorderformsec.htm

*Some of these documents are available in Adobe Acrobat (PDF) format on the SBS web site while others are available through their respective vendor web sites.

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Chapter 3: K2 Components

3.1 CPU – IBM 750

K2 has an IBM PPC 750 CPU. The CPU is located beneath the heat sink. See Figure 3-2, “K2 Hot Swap CompactPCI Board,” on page 2-3. The PowerPC 750 SYSCLK is driven at 100 MHz. A range of SYSCLK to CPU core speed multipliers is supported as follows:

Table 3-1: SYSCLK to CPU Core Speed Multipliers

PLL_CFG 0:3	Core Speed
1000	300 MHz
1110	350 MHz
1010	400 MHz
0111	450 MHz
1011	500 MHz

The PLL_CFG bits can be read in the HID1 register in the PPC 750.

For further information about the PowerPC 740/750 dd 3.2, refer to Chapter 2.3 “Related Documents,” on page 2-4, or access their web site at .

3.2 Level 2 Cache

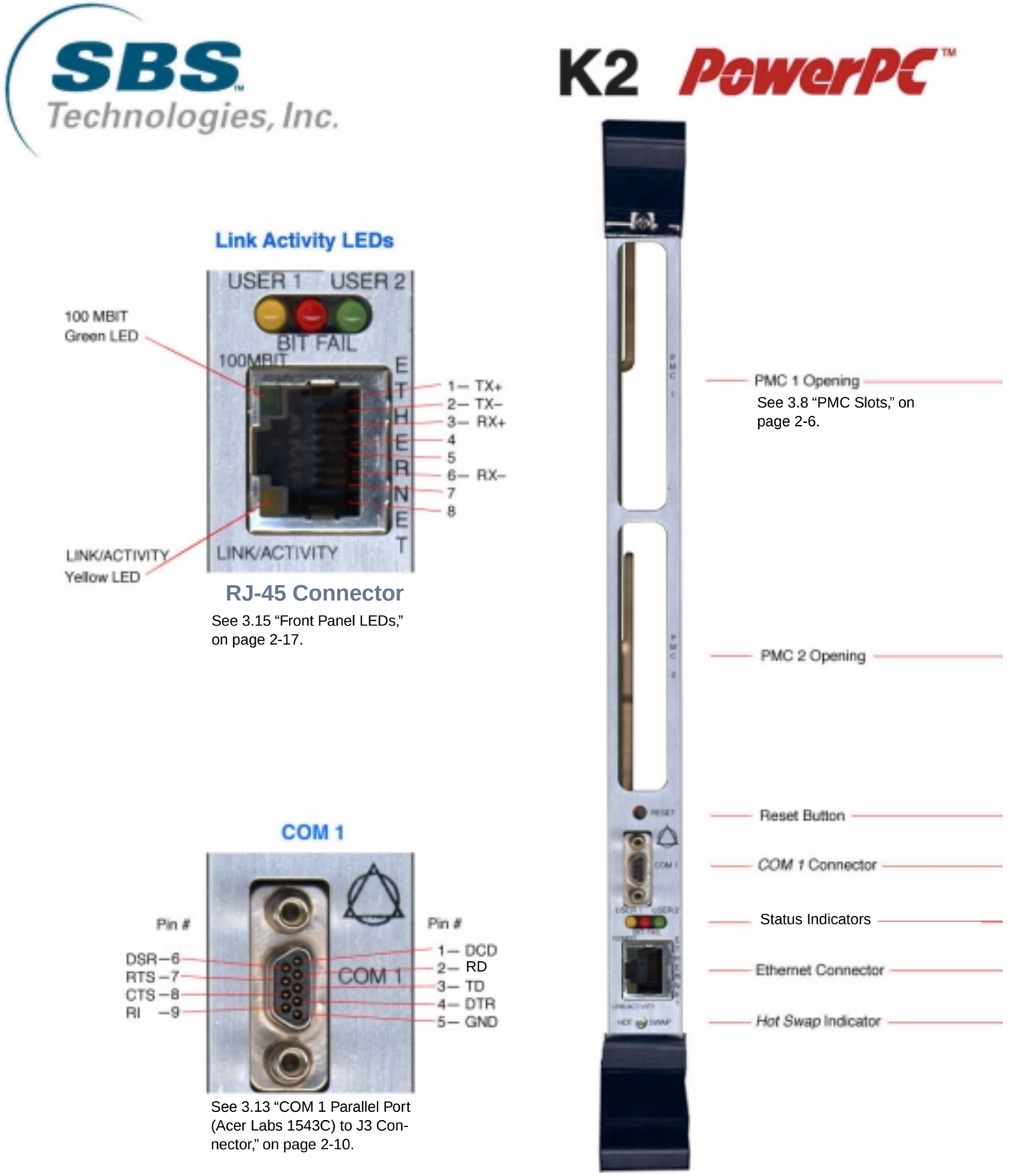
The PPC 750 includes an integrated L2 cache controller with TAG RAM for up to 1M bytes of L2 cache. Two (2) devices provide a 256k x 72 (64 bits plus parity/ECC) Level 2 cache. The L2 cache runs at one half the CPU core speed. K2 has an IBM CPC710 PPC/PCI Bridge. Refer to Figure 2-1, “K2 Block Diagram,” on page 2-2.

3.3 PPC/PCI Bridge—IBM CPC710

The IBM CPC710 PowerPC to PCI bridge used on K2 incorporates a fully interleaved memory controller (144 bit data path to memory), and two (2) completely independent PCI busses. One PCI bus is 32 bits wide and, on K2, this bus is used for on-board peripherals including Ethernet, PCI to ISA bridge and two (2) PMC slots. The other PCI bus is 64 bits wide and capable of 33 or 66 MHz operation. On K2, this bus is connected to the CompactPCI bus and will run at 33 MHz.

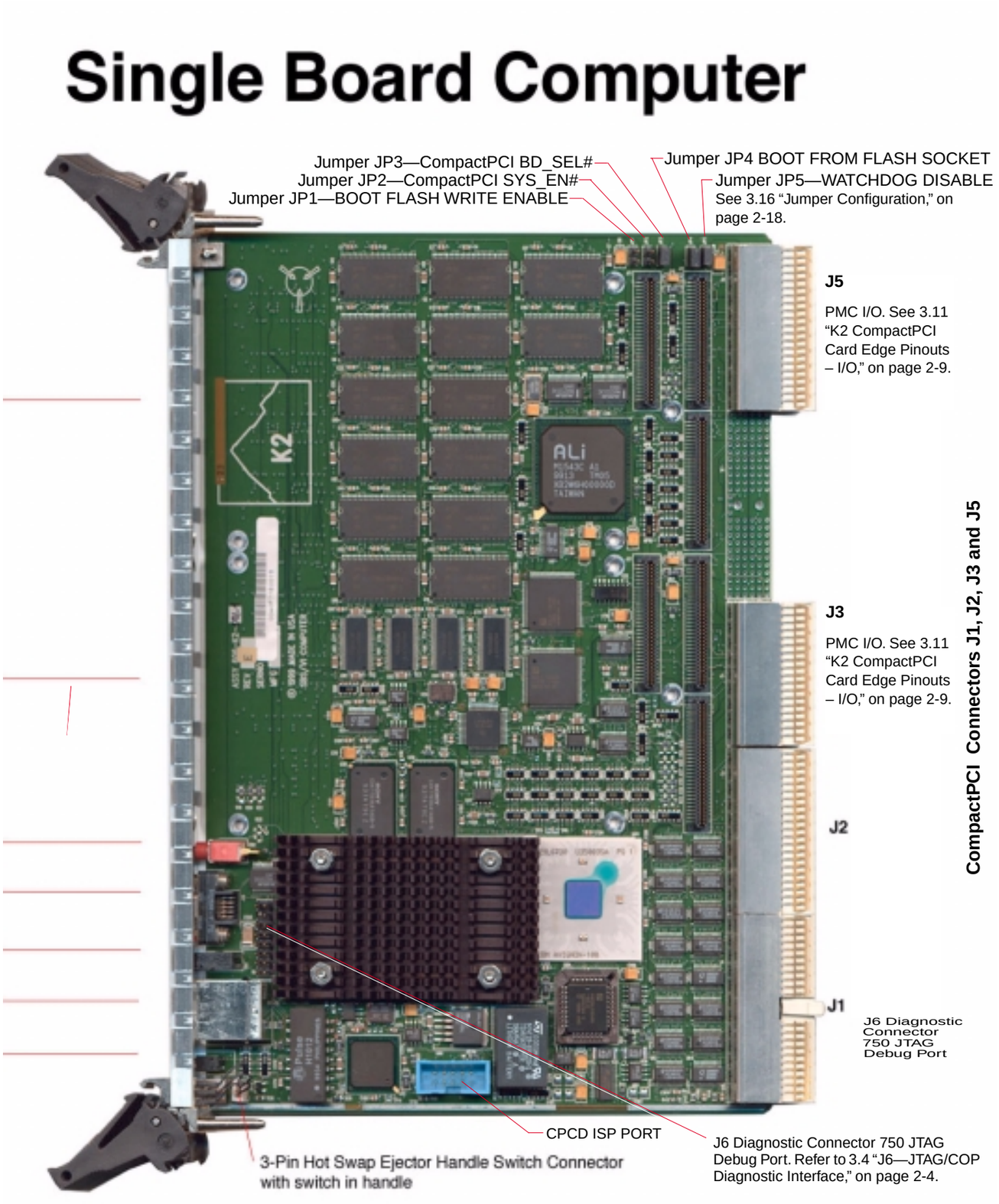
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Figure 3-1, K2 Hot Swap CompactPCI Front Panel



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Figure 3-2, K2 Hot Swap CompactPCI Board

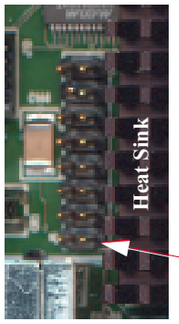


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3.4 J6—JTAG/COP Diagnostic Interface

Figure 3-3, J6–JTAG Diagnostic Connector Pinouts

Pin	Signal	Function
16	GND	DC ground
14	N/C	Key position
12	GND	Ground
10	N/C	No connect
8	N/C	No connect
6	VDD	Processor supply voltage (3.3 Vdc)
4	/RST	Test reset
2	/QACK	Quiescent acknowledge



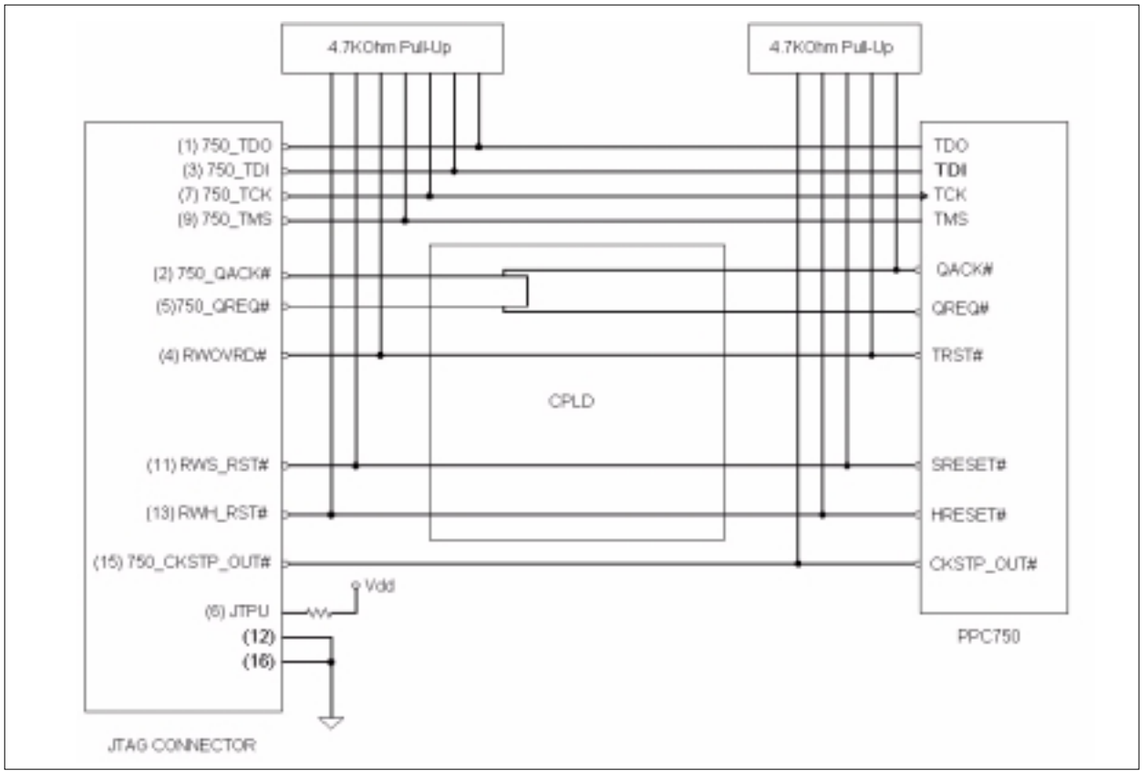
Pin	Signal	Function
15	/CKSTOP	Checkstop output
13	/HRST	Hardware reset
11	/SRST	Software reset
9	S	Test mode select
7	TCLK	Test clock input
5	/QREQ	Quiescent request
3	TDI	Test data input
1	TDO	Test data output

See Figure 3-2, K2 Hot Swap CompactPCI Board, on page 2-3

The 750 has extensive on-chip test capability including Debug control/observation (COP).

SBS has implemented a JTAG port. The JTAG port has been tested and is fully functional with the EST VisionProbe2 emulators. Detailed discussion of the 750 test functions is beyond the scope of this document. Sufficient information, however, has been provided to allow the system designer to disable the test functions that would impede normal operation.

Figure 3-4, JTAG Diagnostic Signal Connections



For more information, refer to *IEEE Standard Test Access Port and Boundary Scan Architecture IEEE STD 1149-1a-1993*.

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3.5 SDRAM – Generic 8M x 8, 16M x 8 or 32M x 8

The memory controller on K2 operates in interleaved mode. This requires memory to be provided in 144 bit wide odd and even banks (128 + parity/ECC). The result is a minimum memory size for each memory bank of 128M bytes using 8M x 8 SDRAM devices. Populating the memory locations with 16M x 8 or 32M x 8 devices results in a bank size of 256M or 512M bytes respectively. K2 is available with 1 or 2 banks of memory. This allows for total memory sizes of 128M – 1G. The memory will run at 100 MHz.

The first bank of memory uses CS0 and CS1 (chip select 0). The second bank, if installed, uses CS2 and CS3. While the memory controller allows any bank to be mapped to any address, it is necessary for one bank to be mapped to address 0 for the exception handlers. In general, bank0 (CS0 and CS1) will be mapped to 0 for accesses from 0 - 07FFFFFFh, for 128M base board memory size.

Memory controller programming information is provided below.

3.6 Executable Flash Memory – Intel 28F640J3A and AMD 29LV040B

K2 contains two (2) flash devices which support direct code execution. The Intel 28F640J3A is permanently soldered in place and provides 8M bytes of storage organized as four 2M byte pages. These pages are selected by using the general purpose output register of the CPC710. Each page is mapped to the uppermost 2M bytes of the PPC750 address space at FFE00000 – FFFFFFFF. The AMD 29LV040B is socketed and provides 512K of storage. It is only accessible when jumper JP1 is installed. With JP1 installed, the 512K flash device will be mapped to the lower 512K bytes of the upper 1M of the PPC750 address space, overlaying the memory of the Intel 28F640J3A device on page 0. The overlap is required due to the 2M byte limitation of the CPC710 memory controller's flash address space. A summary of the flash mapping is provided in the table below:

Table 3-2: Flash Mapping Summary

Jumper JP4	Socketed device (U54)	Soldered device (U101)	Boot Device
Installed	FFF00000 – FFF7FFFF	FFE00000 – FFEFFFFF	Socketed device
Not Installed	Not visible	FFE00000 – FFFFFFFF	Soldered device

JP4, is used to control the write protect mode of the flash. When JP4 is not installed, neither flash device can be written to. Installing JP4 enables writes to either device.

Table 3-3: JP1 Flash Write Protect Mode

Jumper JP1	Socketed device (U?)	Soldered device (U?)
Installed	Writes enabled	Writes enabled
Not Installed	Write protected	Write protected

For more information on the boot flash devices refer to *AMD 29LV040B data sheet, AMD publication # 21354, Rev. C. and Intel Word-wide FlashFile, 28F64073A data sheet, order # 290667-001*

3.7 Ethernet Interface – Intel 82559

The Intel 82559 Fast Ethernet controller provides the 100BaseTX interface on K2. It includes an integrated transceiver, which allows use of both 10Mbit and 100Mbit Ethernet through the same cable connection.

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The transceiver connections are terminated, filtered, and isolated on K2 and are then brought out to a RJ-45 connector on the front panel.

The 82559 is a PCI peripheral, and as such, it contains several PCI configuration registers. It also contains registers for controlling the Ethernet operation, known as *command and status registers* (CSR). The CSRs are accessible via the PCI memory and I/O spaces.

The PCI signals specific to the 82559 are shown below:

Table 3-4: 82559 PCI Signals

Intel 82559 Signal	PCI Connection
IDSEL	AD13
IRQ/	INTA#
REQ/	REQ0#
GNT/	GNT0#

On K2, two (2) LEDs are connected to the 82559. One LED is used for both Link and Activity indication. This LED is connected across the ACTLED and LILED pins so that a valid Link will turn on the LED and Ethernet activity will turn off the LED. In normal use this LED will remain on when no activity is present and will flash when activity is detected. The other LED is connected to the SPEEDLED pin. This LED will turn on when the 82559 is operating in 100Mbit mode.Refer to Figure 3-1, “K2 Hot Swap CompactPCI Front Panel,” on page 2-2.

For further information on the 82559, refer to Intel Fast Ethernet Multifunction PCI/Cardbus Controller Data Sheet, Revision 2.0, order # 743892-002.

3.8 PMC Slots

K2 contains two (2) PMC slots. These slots conform to IEEE draft standards P1386 and P1386.1. These slots accept either two single width expansion boards, or one double width 3.3V or 5V expansion board. The board(s) may be plugged into the K2 32-bit PCI bus via the P11, P12 and P21, P22 connectors.

P14 and P24 are provided to route PMC I/O to the Compact PCI card edge connectors in the manner described below. The pinouts are a combination of Tables 2 and 3 of the PMC on CompactPCI specification (PICMG 2.3 R1.0).

Table 3-5: PMC Slot #1 J5 Signal Routing

Connector	Position	Row F	Row E	Row D	Row C	Row B	Row A
J5	22	GND	P14-1	P14-2	P14-3	P14-4	P14-5
J5	21	GND	P14-6	P14-7	P14-8	P14-9	P14-10
J5	20	GND	P14-11	P14-12	P14-13	P14-14	P14-15
J5	19	GND	P14-16	P14-17	P14-18	P14-19	P14-20
J5	18	GND	P14-21	P14-22	P14-23	P14-24	P14-25
J5	17	GND	P14-26	P14-27	P14-28	P14-29	P14-30
J5	16	GND	P14-31	P14-32	P14-33	P14-34	P14-35
J5	15	GND	P14-36	P14-37	P14-38	P14-39	P14-40
J5	14	GND	P14-41	P14-43	P14-43	P14-44	P14-45
J5	13	GND	P14-46	P14-47	P14-48	P14-49	P14-50
J5	12	GND	P14-51	P14-52	P14-53	P14-54	P14-55
J5	11	GND	P14-56	P14-57	P14-58	P14-59	P14-60
J5	10	GND	P14-61	P14-62	P14-63	P14-64	VI/O

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Table 3-6: PMC Slot #2 J3 Signal Routing

Connector	Position	Row F	Row E	Row D	Row C	Row B	Row A
J3	14	GND	+5V	+5V	+3.3V	+3.3V	+3.3V
J3	13	GND	P24-1	P24-2	P24-3	P24-4	P24-5
J3	12	GND	P24-6	P22-7	P24-8	P24-9	P24-10
J3	11	GND	P24-11	P24-12	P24-13	P24-14	P24-15
J3	10	GND	P24-16	P24-17	P24-18	P24-19	P24-20
J3	9	GND	P24-21	P24-22	P24-23	P24-24	P24-25
J3	8	GND	P24-26	P24-27	P24-28	P24-29	P24-30
J3	7	GND	P24-31	P24-32	P24-33	P24-34	P24-35
J3	6	GND	P24-36	P24-37	P24-38	P24-39	P24-40
J3	5	GND	P24-41	P24-43	P24-43	P24-44	P24-45
J3	4	GND	P24-46	P24-47	P24-48	P24-49	P24-50
J3	3	GND	P24-51	P24-52	P24-53	P24-54	P24-55
J3	2	GND	P24-56	P24-57	P24-58	P24-59	P24-60
J3	1	GND	P24-61	P24-62	P24-63	P24-64	VI/O

K2's front panel contains two openings to accept the PMC front bezels.

The PCI signals specific to the PMC Slots are shown below:

Table 3-7: PCI Signals Specific to PMC Slots

PMC Slot #1 Signal	PMC Slot #2 Signal	PCI Connection
	IDSEL	AD15
	IRQ/	INTD#
	REQ/	REQ3#
	GNT/	GNT3#
IDSEL		AD14
IRQ/		INTC#
REQ/		REQ2#
GNT/		GNT2#

For further information on the PMC specification, refer to *PCI Local Bus Specification, Revision 2.1*, PCI Special Interest Group, *Draft Standard for a Common Mezzanine Card Family: CMC*, IEEE Standards Deparent, P1386/Draft 2.0, and *Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC*, IEEE Standards Deparent, P1386.1/Draft 2.0.

3.9 PCI/ISA Bus Bridge – Acer Labs 1543C

The Acer 1543C integrates the functionality of two standard 82C37 ISA DMA controllers (with 32-bit addressing), a 82C54 timer chip, two 82C59 programmable interrupt controllers (PICs), two independent Integrated Drive Electronics (IDE) interfaces, two 16550 compatible Universal Asynchronous Receiver Transmitters (UARTs) and an IEEE 1284 compliant parallel port. It also maps Peripheral Connect Interconnect (PCI) interrupts to Industry Standard Architecture (ISA) interrupts and decodes the addresses for several standard peripherals.

The ISA bridge of the 1543C is a PCI peripheral; and therefore, it contains several PCI configuration registers. It also contains many registers for controlling the various integrated ISA peripherals. The ISA peripheral registers are accessible via the ISA I/O space, which is at the bottom of the PCI I/O space.

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The PCI signals specific to the 1543C are shown below:

Table 3-8: 1543C PCI Signals

1543C - Device	PCI Connection to IDSEL
ISA Bridge	AD18
IDE Master	AD27
USB (not used on K2)	AD31
PMU (not used on K2)	AD28

The 1543C PCI bus arbitration request/grant and interrupt signals are connected to the various PCI peripherals as shown below:

Table 3-9: PCI Arbitration Assignments

CPC710	Peripheral Connection
PCI Bus Request/Grant 0	82559
PCI Bus Request/Grant 1	Not used
PCI Bus Request/Grant 2	PMC Slot #2
PCI Bus Request/Grant 3	PMC Slot #1
PCI Bus Request/Grant 5	1543C
PCI Interrupt Request A	82559
PCI Interrupt Request B	Not used
PCI Interrupt Request C	PMC Slot #2
PCI Interrupt Request D	PMC Slot #1

See 3.10 “IDE Interfaces – Acer Labs 1543C,” on page 2-8, for information on how to program the 1543C registers.

For further information on the 1543C, refer to *M1543C Preliminary Data Sheet V1.10, Acer Labs*

3.10 IDE Interfaces – Acer Labs 1543C

The Acer 1543C contains two (2) independent IDE channels with dedicated pins for each ATA interface. The Direct Memory Access (DMA) channels support Programmed Input/Output (PIO) modes 0 – 4 and Ultra 33 DMA modes 0-2. CTRL to facilitate hot swapping of IDE devices. The primary IDE interface is not used.

The Secondary IDE interface is routed to the card edge connector as shown below:

Table 3-10: IDE Routing to J3 Connector

Connector	Pos	Row F	Row E	Row D	Row C	Row B	Row A
J5	9	GND	IDE_RESET	IDE_DD7	IDE_DD8	IDE_DD6	IDE_DD9
J5	8	GND	IDE_DD5	IDE_DD10	IDE_DD4	IDE_DD11	IDE_DD3
J5	7	GND	IDE_DD12	IDE_DD2	IDE_DD13	IDE_DD1	IDE_DD14
J5	6	GND	IDE_DD0	IDE_DD15	IDE_DMARQ	IDE_IOW#	IDE_IOR#
J5	5	GND	IDE_IORDY	IDE_DMACK#	IDE_INTRQ	IDE_IOCS16#	IDE_DA1
J5	4	GND	IDE_DA0	IDE_DA2	IDE_CS0#	IDE_CS1#	IDE_DASP#

The IDE Master interface of the 1543C is a PCI peripheral. It therefore contains several PCI configuration registers. The PCI signals specific to the 1543C are shown in Table 3-8: “1543C PCI Signals,” on page 2-8.

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3.11 K2 CompactPCI Card Edge Pinouts – I/O

K2's I/O pinouts are routed as described below:

J1 and J2 have no I/O.

J4 is not used for I/O because, per the Computer Telephony Specification (PICMG 2.5 R1.0), most of these pins are busses on telecom backplanes.

This leaves J3 and J5.

CompactPCI specifications recommended two methods of mapping dual PMCs. K2 does not apply these methods because they either use J4 or they don't provide access to all of the 64 PMC I/O pins for each PMC slot.

Table 3-11: "J3 I/O Mapping," on page 2-9, and Table 3-14: "J5 I/O Mapping," on page 2-10, provide the single PMC mapping that was instead applied.

The rest of the I/O (COM ports, parallel port, IDE) were routed to the remaining free pins.

3.12 J3 Pinouts

Table 3-11: J3 I/O Mapping

Connector	Position	Row F	Row E	Row D	Row C	Row B	Row A
J3	19	GND	Reserved	Reserved	Reserved	Reserved	Reserved
J3	18	GND	P_STB#	P_ALF	P_D0	P_ERR	P_D1
J3	17	GND	P_INIT#	P_D2	P_SLIN#	P_D3	P_D4
J3	16	GND	P_D5	P_D6	P_D7	P_ACK#	P_BUSY
J3	15	GND	P_PE#	P_SCLT	Reserved	Reserved	Reserved
J3	14	GND	+5V	+5V	+3.3V	+3.3V	+3.3V
J3	13	GND	P24-1	P24-2	P24-3	P24-4	P24-5
J3	12	GND	P24-6	P22-7	P24-8	P24-9	P24-10
J3	11	GND	P24-11	P24-12	P24-13	P24-14	P24-15
J3	10	GND	P24-16	P24-17	P24-18	P24-19	P24-20
J3	9	GND	P24-21	P24-22	P24-23	P24-24	P24-25
J3	8	GND	P24-26	P24-27	P24-28	P24-29	P24-30
J3	7	GND	P24-31	P24-32	P24-33	P24-34	P24-35
J3	6	GND	P24-36	P24-37	P24-38	P24-39	P24-40
J3	5	GND	P24-41	P24-43	P24-43	P24-44	P24-45
J3	4	GND	P24-46	P24-47	P24-48	P24-49	P24-50
J3	3	GND	P24-51	P24-52	P24-53	P24-54	P24-55
J3	2	GND	P24-56	P24-57	P24-58	P24-59	P24-60
J3	1	GND	P24-61	P24-62	P24-63	P24-64	VI/O

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3.13 COM 1 Parallel Port (Acer Labs 1543C) to J3 Connector

The Acer Labs 1543C includes an IEEE 1284 compliant parallel port. The Signals are routed to J3 as shown below:

Table 3-12: Parallel Port Connections to J3

Connector	Pos	Row F	Row E	Row D	Row C	Row B	Row A
J3	18	GND	P_STB#	P_ALF	P_D0	P_ERR	P_D1
J3	17	GND	P_INIT#	P_D2	P_SLIN#	P_D3	P_D4
J3	16	GND	P_D5	P_D6	P_D7	P_ACK#	P_BUSY
J3	15	GND	P_PE#	P_SCLT	Reserved	Reserved	Reserved

The Parallel port is an ISA peripheral. Its registers are accessed via the ISA I/O space, which is at the bottom of the PCI I/O space. The actual address used by the parallel port is programmable but at power up it will be set as follows:

The default ISA I/O addresses specific to the Parallel Port are shown below:

Table 3-13: Parallel Port ISA I/O Addresses

Parallel Port	ISA I/O Address
Standard Mode Registers	378-37F
Enhanced Mode Registers	778-77F

3.13.1 J5 Pinouts

Table 3-14: J5 I/O Mapping

Connector	Position	Row F	Row E	Row D	Row C	Row B	Row A
J5	22	GND	P14-1	P14-2	P14-3	P14-4	P14-5
J5	21	GND	P14-6	P14-7	P14-8	P14-9	P14-10
J5	20	GND	P14-11	P14-12	P14-13	P14-14	P14-15
J5	19	GND	P14-16	P14-17	P14-18	P14-19	P14-20
J5	18	GND	P14-21	P14-22	P14-23	P14-24	P14-25
J5	17	GND	P14-26	P14-27	P14-28	P14-29	P14-30
J5	16	GND	P14-31	P14-32	P14-33	P14-34	P14-35
J5	15	GND	P14-36	P14-37	P14-38	P14-39	P14-40
J5	14	GND	P14-41	P14-43	P14-43	P14-44	P14-45
J5	13	GND	P14-46	P14-47	P14-48	P14-49	P14-50
J5	12	GND	P14-51	P14-52	P14-53	P14-54	P14-55
J5	11	GND	P14-56	P14-57	P14-58	P14-59	P14-60
J5	10	GND	P14-61	P14-62	P14-63	P14-64	VI/O
J5	9	GND	IDE_RESET	IDE_DD7	IDE_DD8	IDE_DD6	IDE_DD9
J5	8	GND	IDE_DD5	IDE_DD10	IDE_DD4	IDE_DD11	IDE_DD3
J5	7	GND	IDE_DD12	IDE_DD2	IDE_DD13	IDE_DD1	IDE_DD14
J5	6	GND	IDE_DD0	IDE_DD15	IDE_DMARQ	IDE_IOW#	IDE_IOR#
J5	5	GND	IDE_IORDY	IDE_DMACK#	IDE_INTRQ	IDE_IOCS16#	IDE_DA1
J5	4	GND	IDE_DA0	IDE_DA2	IDE_CS0#	IDE_CS1#	IDE_DASP#
J5	3	GND	SIN2	CTS2	DSR2	DCD2	RI2
J5	2	GND	SOUT2	RTS2	DTR2	SIN1	CTS1
J5	1	GND	DSR1	DCD1	SOUT1	RTS1	DTR1

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3.13.2 COM2 Serial Ports (16550, Acer 1543C) to J5 Connector

The Acer Labs 1543C device includes two (2) ports—16550 compatible UARTs—Com1 and Com2.

COM1 is routed to the front panel and the CompactPCI card edge connector. Refer to Figure 3-1, “K2 Hot Swap CompactPCI Front Panel,” on page 2-2.

COM2 is routed only to the Compact PCI card edge connector as shown below in Table 3-15: “COM Port Connections to J5,” on page 2-11.

Table 3-15: COM Port Connections to J5

Connector	Pos	Row F	Row E	Row D	Row C	Row B	Row A
J5	3	GND	SIN2	CTS2	DSR2	DCD2	RI2
J5	2	GND	SOUT2	RTS2	DTR2	SIN1	CTS1
J5	1	GND	DSR1	DCD1	SOUT1	RTS1	DTR1

The MISC register (see section 4.1 “Software Configuration,” on page 2-1) is used to select whether COM1 is routed to the front panel or to the J5 connector. On power-up, the register is cleared and COM1 is routed to the front panel. When the register is set, COM1 goes to the J5 connector as shown in the table below:

Table 3-16: COM1 Routing Register xxx

MISC Register bit 5	COM1 Connected To
0	Front Panel
1	J5 Connector

The UARTs are ISA peripherals so their registers are accessed via the ISA I/O space, which is at the bottom of the PCI I/O space. The actual addresses used by the COM ports are programmable but at power up they will be set as follows:

The default ISA I/O addresses specific to the UARTs are shown below:

Table 3-17: UART ISA I/O Addresses

16550 Register	ISA I/O Address
COM1 Registers	3F8 – 3FF
COM2 Registers	3E8 – 3FF

*For information on programming the UARTs refer to M1543C Preliminary Data Sheet V1.10, Acer Labs**

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3.14 Timers/Counters

The Acer Labs 1543C includes the equivalent of an 82C54 timer. It provides three 16-bit counter/timers.

On K2, the clock source for the timers is 100 KHz. This allows the 16-bit timer/counters to count with a resolution of 10 µS for a duration of up to 655,350 mS. The 1543 routes the output of timer 0 to IRQ0.

Timer 1 has no external connections.

Timer 2 is connected to the SPKROUT pin on the 1543C. This pin is a no-connect.

In addition to the three timers in the 1543C there are the decrementer and time-of-day counter/timers in the CPU and the periodic and watchdog timers in the RTC.

3.15 Interrupt Logic – 82C59s, Acer Labs 1543C

The 1543C contains the equivalent of a pair of cascaded 82C59 interrupt controllers. Some of the interrupt sources are fixed:

- IRQ0 for timer 0.
- IRQ2 for 8259 cascade.
- IRQ8 for external pin.
- IRQ13 for external pin.

Most of the interrupts, however—including IRQs 1,3,4,5,6,7,9,10,11,12,14,15—can be sourced either from on-board devices or from external pins via software.

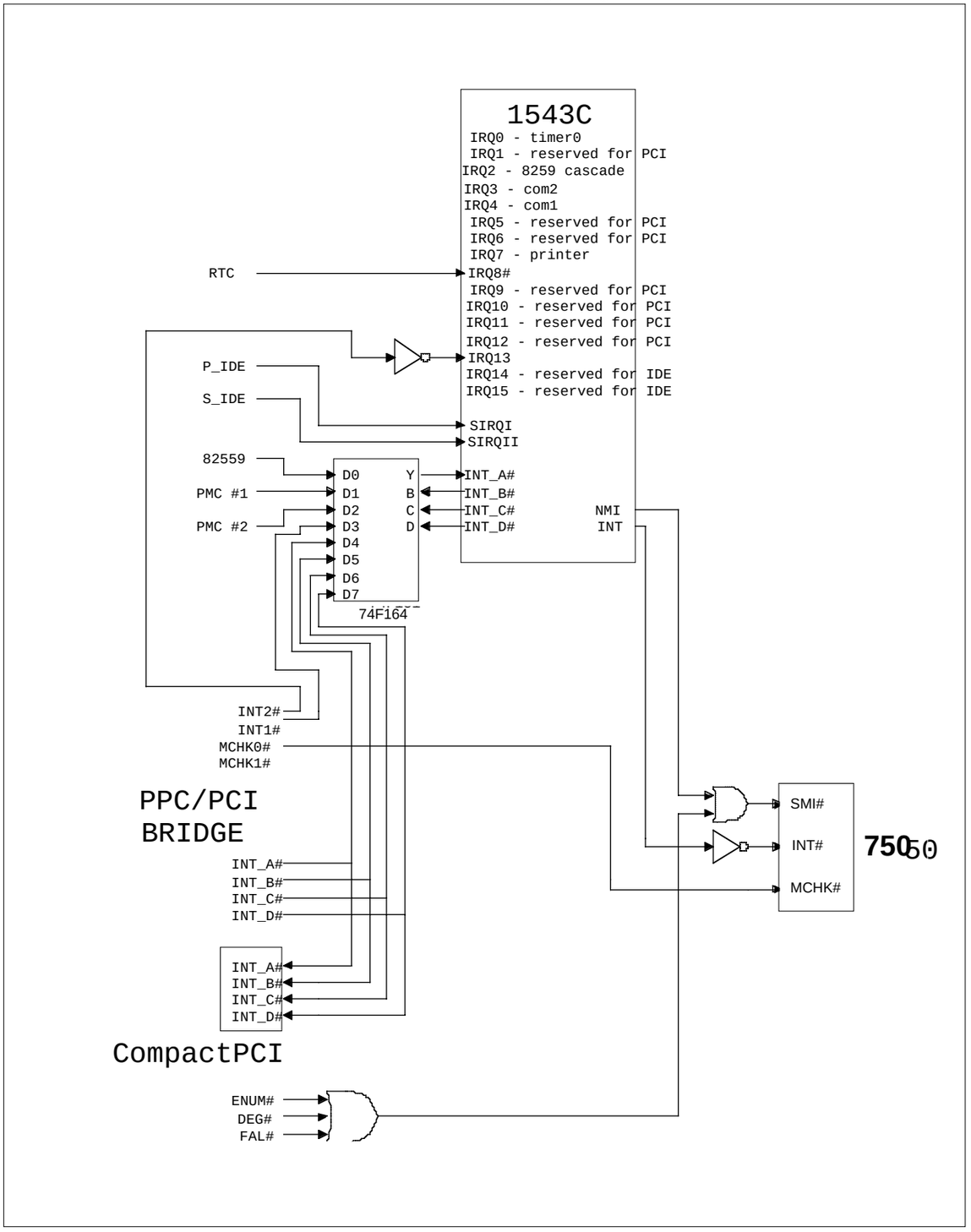
To maximize the flexibility of interrupt assignments, K2 utilizes an additional feature of the 1543C for PCI interrupt routing. This feature, called “PCI Interrupt Polling Mode,” allows an external 3 to 8 decoder to be connected to the normal four PCI interrupts resulting in a total of eight PCI interrupts that can be routed to any of the twelve routable interrupt levels of the 82C59 devices.

From a software standpoint, PCI interrupt polling looks just like normal mode. The cost for using this mode is an extra latency on the PCI interrupts of up to 240 nS. This is the time it takes for the polling circuitry to cycle through the eight PCI interrupts.

A diagram of K2’s interrupt logic is shown below in Figure 3-5, “K2 Interrupt Logic Diagram,” on page 2-13.

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Figure 3-5, K2 Interrupt Logic Diagram



For further information on the PCI/ISA interrupt mapping, refer to *M1543C Preliminary Data Sheet V1.10, Acer Labs*

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3.16 NVRAM – SGS-Thomson M48T37Y

K2 contains 32K bytes (actually 32K X 16 bytes) of battery backed, non-volatile SRAM. The NVRAM is implemented with the M48T37Y SGS-Thomson CMOS Timekeeper SRAM part and is physically located on the ISA bus. The chip select for the NVRAM is derived from the 1543C ROMKBCS# pin which is controlled with the 1543C BCSC (BIOS Chip Select Control) register. It is recommended that this register be programmed to the default of 00h (40h for write protecting the NVRAM) which puts the NVRAM at F0000 – F7FEF in ISA memory space. This translates to 000F0000 – 000F7FEF in PCI memory space. Mapping from the CPU point of view will depend on how the PPC to PCI bridge (CPC710) is configured.

The NVRAM device is a byte wide device. The part, however, may be accessed with 8, 16, or 32 bit wide reads or writes. The 1543C performs gathering or scattering as required so that 8-bit devices can be accessed with 32-bit instructions. The SGS-Thomson M48T37Y has a replaceable, snappable top hat that contains a battery cell and a crystal. Plastic tabs hold the top hat securely to the main body of the part.

For more information regarding K2 NVRAM refer to *M48T37, 32K x 8 TIMEKEEPER SRAM, April 1998 Data Sheet* , SGS-THOMSON.

3.17 REAL TIME CLOCK – SGS-Thomson M48T37Y

K2 contains a realtime clock and calendar with battery back up. The realtime clock is implemented with the M48T37Y SGS-Thomson CMOS Timekeeper SRAM part and is physically located on the ISA bus. As with the NVRAM, access to the RTC is controlled via the 1543C register. With this register set to its default of 00h, the RTC is accessed from F7FF0 – F7FFF in ISA memory space. PCI access is from PCI memory space, addresses 000F7FF8 to 000F7FFF. The realtime Clock is a byte wide device. The part, however, may be accessed with 8, 16, or 32 bit wide reads or writes. The 1543C ISA bridge performs gathering or scattering as required. As mentioned above, the SGS-Thomson M48T37Y has a replaceable, snappable top hat that contains a battery cell and a crystal. Plastic tabs hold the top hat securely to the main body of the part.

The SGS-Thomson M48T37 contains century, year, month, day of month, day of week, hour, minute, and seconds in binary coded decimal registers. Corrections for leap year are performed automatically. Table 3-18: “Real Time Clock Registers,” on page 2-14, below, itemizes the Real Time Clock registers.

Table 3-18: Real Time Clock Registers

PCI ADDRESS	FUNCTION	BCD RANGE	D7 D6 D5 D4	D3 D2 D1 D0
000F7FFF	YEAR	00 to 99	10 YEARS	YEAR
000F7FFE	MONTH	01 to 12	0 0 0 10 M.	MONTH
000F7FFD	DATE	01 to 31	0 0 10 DATE	DATE
000F7FFC	DAY	01 to 07	0 0 0 0	0 DAY
000F7FFB	HOUR	00 to 23	0 0 10 HOURS	HOURS
000F7FFA	MINUTE	00 to 59	0 10 MINUTES	MINUTES
000F7FF9	SECOND	00 to 59	0 10 SECONDS	SECONDS
000F7FF8	CONTROL		W R S Cal.	Calibration
000F7FF7	WATCHDOG		WDS BMB4 BMB3 BMB2	BMB1 BMB0 RB1 RB0
000F7FF6	INTERRUPTS		AFE 0 ABE 0	0 0 0 0
000F7FF5	ALARM DATE	01 to 31	RPT4 0 AL. 10 DATE	AL. DATE
000F7FF4	ALARM HOURS	00 to 23	RPT3 0 AL. 10 HOURS	AL. HOURS
000F7FF3	ALARM MINUTES	00 to 59	RPT2 AL. 10 MINUTES	AL. MINUTES
000F7FF2	ALARM SECONDS	00 to 59	RPT1 AL. 10 SECONDS	AL. SECONDS
000F7FF1	CENTURY	00 to 99	1000 YEARS	100 YEARS
000F7FF0	FLAGS		WDF AF Z BL	Z Z Z Z

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All reads and writes to the Real Time Clock must be coordinated through use of the control register (000F7FF8). Before reading a Real Time Clock register , first the “R” bit of the control register must be set. That freezes the current copy of time in an internal buffer in the M48T37 (the internal clock remains counting). Then the clock buffer registers can be read (000F7FF9 to 000F7FFF). Note, the clock register buffers will not be updated again until the “R” bit is reset to zero. When any of the real time clock time settings are to be modified, first the “W” bit of the control register must be set. After setting the “W” bit, any or all of the clock buffer registers can be written (000F7FF9 to 000F7FFF). Note, the actual update to the clock time settings do not occur until the “W” bit is reset to zero. **Also note, when the “W” bit is reset to zero, all of the buffer registers are updated to the actual Real Time Clock internal counters (not just the buffers that were written).** For more information, refer to *M48T37, 32K x 8 TIMEKEEPER SRAM, April 1998 Data Sheet* , SGS-THOMSON.

3.18 Watchdog Timer – SGS-Thomson M48T37

The SGS-Thomson contains a built-in watchdog timer. On power-up, the watchdog timer is disabled. Once it is enabled by software, it can be disabled by writing 00h to the watchdog register. It can be set for a timeout interval of _ to 124 seconds.

The watchdog can be used to generate IRQ8, or a hardware reset. Selection of the various timeout events is made as follows. The M48T37 has two (2) methods of indicating a watchdog timeout. One is with a reset pin and the other is with an interrupt pin. Software which configures the watchdog selects one or the other of these timeout indications. The reset output is connected to the hardware the same as the push button reset, so watchdog timeouts using the reset pin will behave just like a front panel push button reset. The interrupt pin is routed to IRQ8 of the 1543C’s 8259. Refer to Figure 3-6, “Watchdog Timer Reset Logic,” on page 2-16.

For debugging, jumper JP5 can be used to disable the watchdog timer. When JP5 is installed, the watchdog timer must receive a clock on its STROBE pin to prevent it from timing out. This is useful when software modifications inadvertently result in watchdog timeouts. When this happens, the developer can install the jumper and proceed with software testing without having to start over with the watchdog software removed.

Table 3-19: Watchdog Timer Jumper JP5

Jumper JP5	Watchdog Timer
Installed	Disabled
Not Installed	Enabled

For more information on the watchdog timer, refer to *M48T37, 32K x 8 TIMEKEEPER SRAM, April 1998 Data Sheet* , SGS-THOMSON.

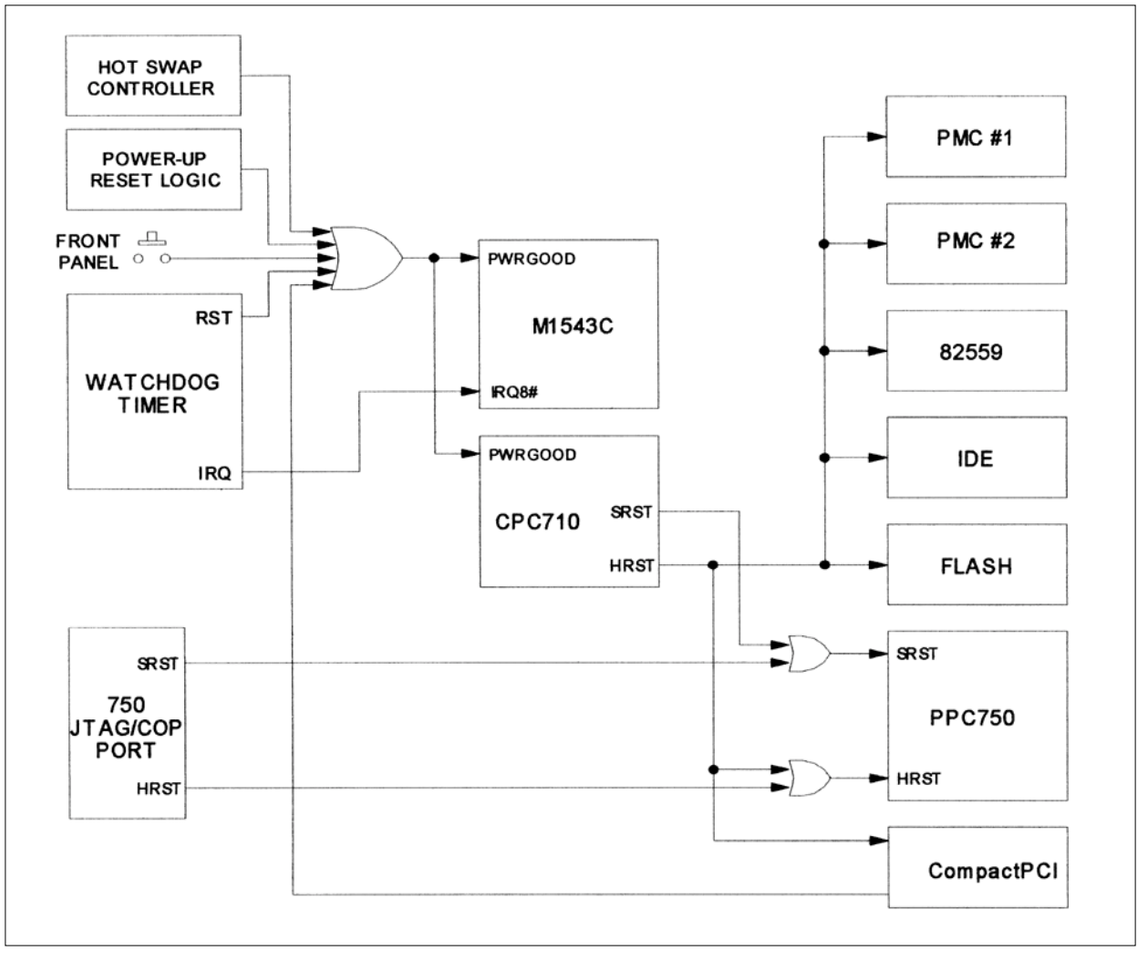
3.13.1 Reset Logic

K2 can be reset from multiple sources as shown below in Figure 3-6, “Watchdog Timer Reset Logic,” on page 2-16. There are five sources which can affect a reset of the K2 module:

- Power-up circuitry.
- Front panel pushbutton switch.
- Hot Swap controller.
- Watchdog timer.
- JTAG interface.

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Figure 3-6, Watchdog Timer Reset Logic



3.14 Clock Circuitry

A Motorola MPC9724 clock chip satisfies the majority of K2's clock requirements. This chip takes a 33.3 Mhz input and generates both 100 Mhz and 33.3 MHz outputs.

A zero delay PLL clock buffer distributes the 100 MHz clocks to the SDRAM chips. The 33 MHz is used for PCI devices.

A 25 MHz oscillator provides the clock for the Ethernet controller.

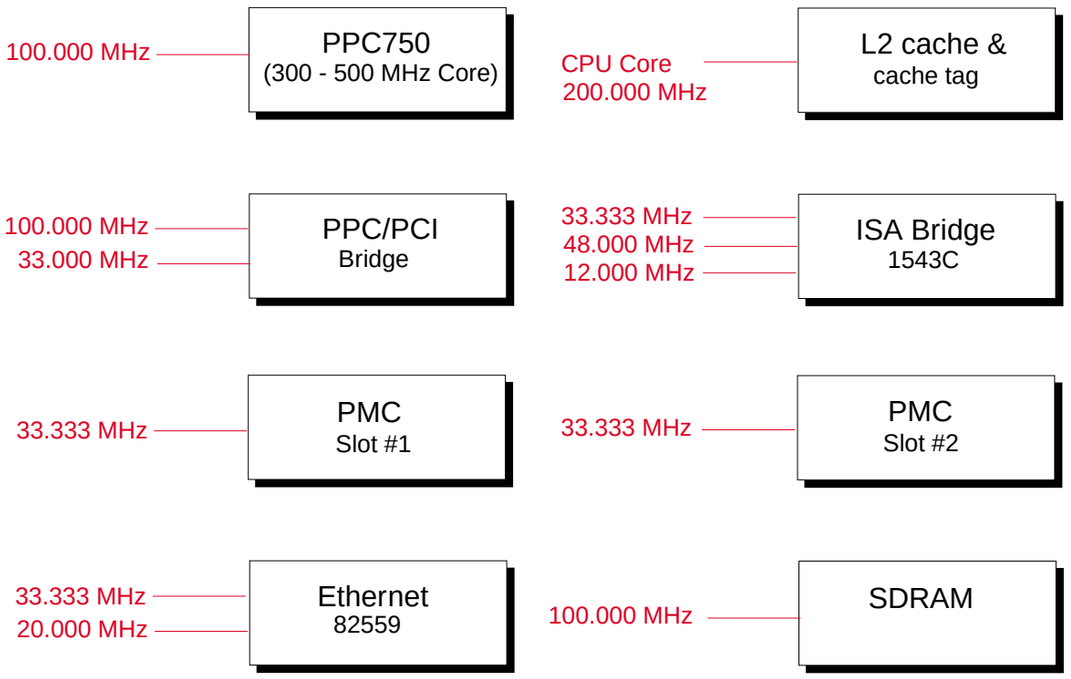
A 48 MHz oscillator provides the clock for the various SIO peripherals within the 1543C ISA bridge, including the UARTS. This clock is divided down to provide 12 MHz to the 82C54 within the 1543C ISA bridge.

The clock for the L2 cache comes from the CPU and is half the core frequency.

The different clocks are distributed as shown below:

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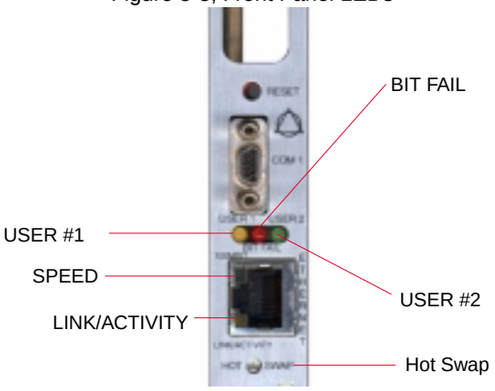
Figure 3-7, Clock Distribution



3.15 Front Panel LEDs

The front panel LEDs are shown below:

Figure 3-8, Front Panel LEDs



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Table 3-20: LED Assignments

LED	Color	Signal
1	Blue	Hot Swap
2	Yellow	Ethernet Link/Activity
3	Green	Ethernet Speed
4	Yellow	User 2
5	Green	User 1
6	Red	Bit Fail

3.16 Jumper Configuration

There are five (5) end user jumpers on K2. They are JP1, JP2, JP3, JP4 and JP5. Their locations are shown below.

WARNING **DO NOT USE JP2 IF K2 IS INSTALLED IN A NON-SYSTEM SLOT.** This can result in permanent damage. Before installing JP2, make certain that the K2 is plugged in to a slot which is safe for SYS functionality.

WARNING **IF JP3 IS INSTALLED, YOU MUST TURN OFF CHASSIS POWER BEFORE INSERTING OR EXTRACTING K2.** The Use of JP3 will affect the operation of the On-Board Hot Swap controller. Application of backend power, prematurely applied, may result in permanent damage to the board.

Figure 3-9, Jumpers JP1 through JP5

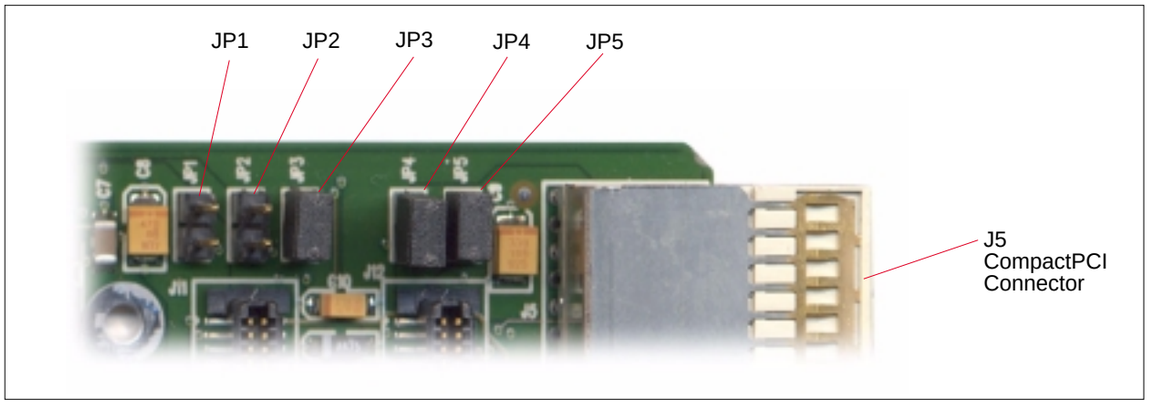


Table 3-21: Jumper Definitions

JUMPER	NAME	INSTALLED	REMOVED
JP1	Boot Flash Write Enable	Writes to boot flash are enabled	Writes to boot flash are disabled
JP2	CompactPCI SYSEN#	Grounds SYS_EN# pin	Pulls SYS_EN# pin high
JP3	CompactPCI BD_SEL#	Grounds BD_SEL# pin	Pulls BD_SEL# pin high
JP4	Boot Flash Select	Boot to socketed device	Boot to soldered device
JP5	Watchdog Disable	Disable watchdog timer	Enable watchdog timer

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3.13.1 Jumper JP1

Jumper JP1 is used to enable or disable writes to the flash devices. When JP1 is **NOT** installed, there are no chip enables generated for write cycles to the boot flash devices.

3.13.2 Jumper JP2

Jumper JP2 is used to ground the CompactPCI SYSEN# pin to force SYSSLOT mode in the event that the chassis does not do so. When JP2 is installed, K2 will enter SYSSLOT mode regardless of which slot into which it is plugged. If K2 is not placed in the System slot, it may still be forced to act as the System controller board simply by jumpering JP2. If you remove the jumper on JP2, K2 will auto sense its locations and configure itself accordingly as either a System controller or a peripheral board, depending on where it is placed in the chassis.

3.13.3 Jumper JP3

Jumper JP3 is used to ground the CompactPCI BD_SEL# pin in case the chassis does not do so. When JP3 is installed, K2 will remained powered up regardless of the state of the BD_SEL# pin on the backplane.

3.13.4 Jumper JP4

Jumper JP4 is used to select which flash device the board boots from. When JP1 is installed, the board boots from the socketed device. When JP1 is removed, booting will take place from the soldered device. See section 3.6 “Executable Flash Memory – Intel 28F640J3A and AMD 29LV040B,” on page 2-5, for more information on the boot flash.

3.13.5 Jumper JP5

Jumper JP5 is used to disable the watchdog timer for debugging purposes. When JP5 is installed, a clock pulse is driven onto the strobe pin (pin 14) of the NVRAM/CLOCK chip (U65). This prevents a watchdog interrupt or reset from occurring.

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Chapter 4: Internal Registers

4.1 Software Configuration

For additional information regarding the PowerPC 750 and CPC710 configurations, please refer to “Related Documents” on page 2-4.

This manual defines all registers used in the CPC710. Registers which have K2 configuration dependencies are defined below.

4.2 Table of K2 Registers

Table 4-1: K2 Registers

ISAI/O ADDR	Name	Description	Type	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	reset value
0800	Board ID	see below	R	PT3	PT2	PT1	PT0	BS1	BS0	CS1	CS0	01100010
0802	L2CNTL	See below	R	X	X	X	X	X	X	X	L2CLK	00000001
0804	MISC	see below	R/W	NDLK	C1_J5	C1_FP	C2_EN	CP_SYS (1)	ULED2	BITF	ULED1	0010c010
0808	MSIZ/Slot ID	see below	R	MSIZ0	MSIZ1	MSIZ2	GA4	GA3	GA2	GA1	GA0	ccc111cc
080B	Interrupt CTRL/Status	see below	R/W	SMI Mask	EIIM Mask	ENUM STAT(1)	SUPPLY FAIL(1)	SUPPLY DEGRD(1)	EJECTOR STAT(1)	MCP Mask	1543 NMI(1)	11cccc1c
080C	Hot Swap	see below	R/W	INS	EXT	x	x	LOO	x	EIM	x	cccccccc
080E	PLD 2 Rev	See below	R	PLDH3	PLDH2	PLDH1	PLDH0	PLDL3	PLDL2	PLDL1	PLDL0	cccccccc
080F	PLD 3 Rev	see below	R	PLDH3	PLDH2	PLDH1	PLDH0	PLDL3	PLDL2	PLDL1	PLDL0	cccccccc

(1)-bit is read only

x - bit value doesn’t matter, reads as 0, writes have no effect.

c - bit value depends on board configuration or status.

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4.2.1 Board ID Register

Address Offset: 0x800

Access:Read Only

Reset Value: x62

Table 4-2: K2 Board ID Register

Bit(s)	Name	Reset Value	Function
7-4	PT[3..0]	b0110	Processor Type: b0001 - Reserved b0010 - Reserved b0011 - Reserved b0100 - Reserved b0101 - Reserved b0110- PPC750 b0111 0 PPC7400 (Future capability) b1xxx - Reserved
3-2	BS[1..0]	b00	Bus Speed: b00 - 100 MHz b01 - Reserved b10 - Reserved b11 - 66.6 MHz
1-0	CS[1..0]	b10	L2 Cache Size: b00 - Reserved b01 - Reserved b10 - 1 MB b11 - No L2 Cache

4.2.2 Miscellaneous Register

Address Offset: 0x804

Access:Read/Write

Reset Value: x21

Table 4-3: K2 Miscellaneous Register

Bit(s)	Name	Reset Value	Function
7	NDLK	b0	CP710 Deadlock Control: 1 - enable; 0 = disable
6	COM1_J3	b0	COM 1 Control: 1 = enable to backplane J3; 0 - disable to backplane J3
5	COM1_FP	b1	COM 1 Control: 1 = enable to front panel; 0 - disable to front panel
4	COM2_J3	b0	COM 2 Control: 1 = enable to backplane J3; 0 - disable to backplane J3
3	SKFL_EN	b1	Socketed Flash PROM Control: 1 = enable; 0 = disable
2	ULED2	b0	User LED 2 (Yellow) Control: 1 = LED on; 0 = LED off
1	BITFLED	b1	BitFail LED (Red) Control: 1 = LED on; 0 = LED off
0	ULED1	b0	User LED 1 (Green Control: 1 = LED on; 0 = LED off

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4.2.3 L2 Cache Configuration Register

Address Offset: 0x802

Access:Read Only

Reset Value: Dependent on board revision

Table 4-4: K2 L2 Cache Configuration Register

Bit(s)	Name	Reset Value	Function
7-1			Reserved
3-0	L2 CLK	c	L2 Cache Clock Configuration: 1 = single ended clocks, 0 - differential clocks

4.2.4 Memory Size/Slot ID Register

Address Offset: 0x808

Access:Read Only

Reset Value: xcc

Table 4-5: K2 Memory Size/Slot ID Register

Bit(s)	Name	Reset Value	Function
7-5	MEM_SIZ[2..0]	ccc	SDRAM Memory Size: b111: 128 MB x 1 Bank b110: 128 MB x 2 Banks b101: 256 MB x 1 Bank b100: 256 MB x 2 Banks b011: 512 MB x 1 Bank b010: 512 MB x 2 Banks b001: Reserved b000: Reserved
4-0	GA[4..0]	cc	Slot Identification: b00000: slot 0 (reserved for future use per CompactPCI specification) b00001: slot 1 b00010: slot 2 b00011: slot 3 . . b11111: slot 31

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4.2.5 Interrupt Control and Status Register

Address Offset: 0x80B

Access:Read/Write (write zero to bits 0, 2, or 3 to clear specific interrupts)

Reset Value: xF2

Table 4-6: Interrupt Control and Status Register

Bit(s)	Name	Reset Value	Function
7	SMI MASK	b1	System management interrupt mask: 1 = mask interrupt; 0 = enable interrupt
6	EIIM MASK	b1	ENUM interrupt input signal mask: 1 = mask signal; 0 = enable signal
5	ENUM STAT	b0	ENUM interrupt input status (read only): 1 = ENUM inactive; 0 = ENUM active
4	SUPPLY FAIL	b1	Power supply status (sys controller only): 1 = supply ok; 0 = supply fail
3	SUPPLY DEG	b1	Power supply status (sys controller only): 1 = supply ok; 0 = supply degrade
2	EJSW	c	Ejector Switch Status: 1 = ejector closed; 0 = ejector open
1	MCP MASK	b1	MCP Mask (PPC750 machine check): 1 = mask MCP; 0 = Enable MCP
0	a543NMI	b0	M1543C Non-maskable Interrupt: 1 = interrupt asserted; 0 = no interrupt

4.2.6 Hot Swap Control Register

Address Offset: 0x80C

Access:Read/Write

Reset Value: x88

Table 4-7: Hot Swap Control Register

Bit(s)	Name	Reset Value	Function
7	INS	b1	Insertion ENUM status: 1 = ENUM asserted; 0 = ENUM not asserted
6	EXT	b0	Extraction ENUM status: 1 = ENUM asserted; 0 = ENUM not asserted
5			Reserved
4			Reserved
3	LOO	b1	Blue LED Status: 1 = LED on; 0 = LED off
2			Reserved
1	EIM	b0	ENUM Signal Mask: 1 = mask ENUM; 0 = enable ENUM
0			Reserved

4.2.7 CPLD 2 Revision Register

Address Offset: 0x80E

Access:Read Only

Reset Value: Dependent on board revision

Table 4-8: CPLD 2 Revision Register

Bit(s)	Name	Reset Value	Function
7-4	PLD2H[3..0]	c	CPLD 2 revision, upper bits, represents ‘ones’ place of revision
3-0	PLD2L[3..0]	c	CPLD 2 revision, upper bits, represents ‘tenths’ place of revision

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4.2.8 CPLD 3 Revision Register

Address Offset: 0x80F

Access:Read Only

Reset Value: Dependent on board revision

Table 4-9: CPLD 2 Revision Register

Bit(s)	Name	Reset Value	Function
7-4	PLD3H[3..0]	c	CPLD3 revision, upper bits, represents ‘ones’ place of revision
3-0	PLD3L[3..0]	c	CPLD 3 revision, upper bits, represents ‘tenths’ place of revision

4.2.9 Address Offset

Table 4-10: PT Bit Definition

PT3	PT2	PT1	PT0	Meaning
0	0	0	1	PPC601
0	0	1	0	PPC602
0	0	1	1	PPC603
0	1	0	0	PPC604
0	1	0	1	PPC740
0	1	1	0	PPC750
0	1	1	1	reserved
1	x	x	x	reserved

Table 4-11: BS Bit Definition

BS1	BS0	Meaning
0	0	100.0 MHz
0	1	83.3 MHz
1	0	75.0 MHz
1	1	66.6 MHz

Table 4-12: CS Bit Definition

CS1	CS0	Meaning
0	0	512K
0	1	256K
1	0	1M
1	1	no cache

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Table 4-13: Memory Configuration Bit Definition

MSIZ0 (GPIO0)	MSIZ1 (GPIO1)	MSIZ2 (GPIO2)	BANK SIZE	NO. OF BANKS	TOTAL MEMORY
1	1	1	128 MB	1	128 MB
1	1	0	128 MB	2	256 MB
1	0	1	256 MB	1	256 MB
1	0	0	256 MB	2	512 MB
0	1	1	512 MB	1	512 MB
0	1	0	512 MB	2	1 GB
0	0	1	reserved	reserved	Reserved
0	0	0	reserved	reserved	Reserved

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Chapter 5: Software

5.1 K2 PPC750 Initialization Sequence

1. Disable Caches
2. Disable data and instruction translation
3. Disable IBAT registers
4. Disable DBAT registers
5. Initialize L2 Cache
6. Perform L2 Global Invalidate
7. Wait for invalidation to complete
8. Enable L2 Cache operation
9. Cache functions

5.1.1 CPC710 Initialization

Initialize Standard System Register Space

RSTR(0xff000010): write 0xf0000000

SIOC(0xff001020): write 0x00000000

PIDR(0xff000008): write 0x00000000

UCTL(0xff001000): write 0x00780080

ABCNTL(0xff001030): write 0x70000000

SRST(0xff001040): write 0x00000000

ERRC(0xff001050): write 0x00000000

SESR(0xff001060): write 0x00000000

SEAR(0xff001070): write 0x00000000

PGCHP(0xff001100): write 0x000000e0

GPDIR(0xff001130): write 0x00000000

ATAS(0xff001160): write 0x709c2508

AVDG(0xff001170): write 0x00000000

MESR(0xff001220): write 0x00000000

MEAR(0xff001230): write 0x00000000

MCER0(0xff001300): write 0x800080c0

MCER1(0xff001310): write 0x808080c0

MCCR(0xff001200): write 0xf3b0e400

Wait for MCCR bit 2 to be set (mem init complete)

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5.1.2 Enable PCI64 Configuration Space

CNFR(0xff00000c): write 0x80000003 *setup for pci64 config*
BAR(0xff200018): write 0xff400000
PCIENB(0xff201000): write 0x80000000 *enable pci configuration access*
CNFR(0xff00000c): write 0x00000000

5.1.3 Enable PCI32 Configuration Space

CNFR(0xff00000c): write 0x80000002 *setup for pci32 config*
BAR(0xff200018): write 0xff500000
PCIENB(0xff201000): write 0x80000000 *enable pci configuration access*
CNFR(0xff00000c): write 0x00000000

5.1.4 Initialize PCI64 Configuration Space

CFGA(0xff4f8000): write 0x08000080 *little endian format*
CFGD(0xff4f8010): read PCI64 revision ID

CFGA(0xff4f8000): write 0x04000080 *little endian format*
CFGD(0xff4f8010): write 0x0701 *pci64 command register, little endian format*

CFGA(0xff4f8000): write 0x06000080 *little endian format*
CFGD(0xff4f8010): write 0xffff *pci64 status register, little endian format*

5.1.5 Initialize PCI32 Configuration Space

CFGA(0xff5f8000): write 0x08000080 *little endian format*
CFGD(0xff5f8010): read PC32 revision ID

CFGA(0xff5f8000): write 0x04000080 *little endian format*
CFGD(0xff5f8010): write 0x0701 *pci32 command register, little endian format*

CFGA(0xff5f8000): write 0x06000080 *little endian format*
CFGD(0xff5f8010): write 0xffff *pci32 status register, little endian format*

CFGA(0xff5f8000): write 0x68000080 *little endian format*
CFGD(0xff5f8010): write 0xffff *pci32 intrpt register, little endian format*

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5.1.6 Initialize PCI32 Bridge Registers

PSEA(0xff5f6110): write 0x00000000

PCIDG(0xff5f6120): write 0x40000000

PIBAR(0xff5f7800): write 0x80000000

PMBAR(0xff5f7810): write 0x00000000

PR(0xff5f7f20): write 0xa000e000

ACR(0xff5f7f30): write 0xfc000000

MSIZE(0xff5f7f40): write 0xf0000000

IOSIZE(0xff5f7f60): write 0xfc000000

SMBAR(0xff5f7f80): write 0xe0000000

SIBAR(0xff5f7fc0): write 0xf0000000

CTLRW(0xff5f7fd0): write 0x00000000

PSSIZE(0xff5f8100): write 0x00000000

PPSIZE(0xff5f8110): write 0x00000000

BARPS(0xff5f8120): write 0x00000000

BARPP(0xff5f8130): write 0x00000000

PSBAR(0xff5f8140): write 0x00000000

PPBAR(0xff5f8150): write 0x00000000

BPMDLK(0xff5f8200): write 0x00000000

PDLK(0xff5f8210): write 0x00000000

BIODLK(0xff5f8220): write 0x00000000

TIODLK(0xff5f8230): write 0x00000000

5.1.7 Initialize PCI64 Bridge Registers

PSEA(0xff4f6110): write 0x00000000

PCIDG(0xff4f6120): write 0xc0000000

PIBAR(0xff4f7800): write 0x80000000

PMBAR(0xff4f7810): write 0x00000000

PR(0xff4f7f20): write 0x8000a000

ACR(0xff4f7f30): write 0xfc000000

MSIZE(0xff4f7f40): write 0xc0000000

IOSIZE(0xff4f7f60): write 0xfc000000

SMBAR(0xff4f7f80): write 0x40000000

SIBAR(0xff4f7fc0): write 0xc0000000

CTLRW(0xff4f7fd0): write 0x02000000

PSSIZE(0xff4f8100): write 0x00000000

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PPSIZE(0xff4f8110): write 0x00000000

BARPS(0xff4f8120): write 0x00000000

BARPP(0xff4f8130): write 0x00000000

INT_SET(0xff4f8310): write 0x00000000

5.2 M1543C (AcerLabs) Initialization

> **Note:** This part contains a PCI to ISA bridge, IDE interface, printer port, and serial ports. The configuration accesses below are used to configure the ISA bridge.

5.2.1 Initialize ISA Bridge Registers

CFGA(0xff4f8000): write 0x40180080 *little endian format*

CFGD(0xff4f8010): write 0x304a007f *little endian format*

CFGA(0xff4f8000): write 0x50180080 *little endian format*

CFGD(0xff4f8010): write 0x40008900 *little endian format*

CFGA(0xff4f8000): write 0x54180080 *little endian format*

CFGD(0xff4f8010): write 0x00080300 *little endian format*

CFGA(0xff4f8000): write 0x58180080 *little endian format*

CFGD(0xff4f8010): write 0x030e0d4c *little endian format*

CFGA(0xff4f8000): write 0x5c180080 *little endian format*

CFGD(0xff4f8010): write 0xfc010000 *little endian format*

CFGA(0xff4f8000): write 0x70180080 *little endian format*

CFGD(0xff4f8010): write 0x00000000 *little endian format*

CFGA(0xff4f8000): write 0x78180080 *little endian format*

CFGD(0xff4f8010): write 0x00000002 *little endian format*

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5.3 Memory Map

Memory mapping on K2 is extremely flexible. The memory controller imposes only two restrictions.

- At least 1M byte of system memory must be mapped to address 0.
- The upper 16 Megabytes of the CPU address space are reserved for PROM and other system devices.

The only other restrictions imposed by the system are interoperability issues. PCI specifications allow PCI devices to be located anywhere in the PCI address space.

The PCI memory and I/O spaces can be located anywhere within the CPU memory space. The ISA I/O devices can be located anywhere within the first 64K of PCI I/O space.

Since PCI peripherals are mapped into the PCI memory and I/O spaces during system configuration, it is only relevant to list the PCI address/data lines connected to IDSEL lines of the PCI peripherals.

The following device ID selects are used within the PCI configuration space:

Table 5-1: Device ID Selects

ID Select	I/O Device	Device Part_Number
AD18	PCI/ISA Bridge	Acer Labs 1543C
AD12	none	N/A
AD13	Ethernet	Intel 82559
AD14	PMC Slot #1	Connector P12
AD15	PMC Slot #2	Connector P22

During boot up, the open boot firmware or VxWorks operating system will map these devices into PCI memory space.

The PCI device default I/O addresses are shown below:

Table 5-2: PCI Device Default Addresses

Device	PCI Memory Address	PCI I/O Address
ACER	0X01000000	0X01000000
Ethernet	0X01010000	0X01010000
PMC1	0X04000000	0X01040000
PMC2	0X08000000	0X01080000

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The ISA power-on default I/O addresses for peripherals are shown below:

Table 5-3: ISA Peripherals Power-On Default I/O Addresses

ISA Peripheral	ISA Memory Address	ISA I/O Address
COM1 Registers		3F8 - 3FF
COM2 Registers		3E8 - 3EF
Parallel Port, standard mode		378 – 37F
Parallel Port, enhanced mode		778 – 77F
On Board Registers (See Table 5-4: “750 DBAT MMU Configuration” on page 2-12		800 – 80F
M48T37 NVRAM	90000 – 97FEF	
M48T37 RTC	97FF0 – 97FFF	

This table does not include the ISA peripherals contained within the 1543C. For full details on these ISA peripherals, refer to M1543C Preliminary Data Sheet V1.10, Acer Labs*

5.4 L2CNTL

L2CLK — L2 Clock Type

1 — Single Ended

0 — Differential

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5.5 VxWorks 5.4 Architecture Specific Reference

This supplement to WindRiver's VxWorks documentation describes the drivers specific to the K2 board.

5.5.1 Memory Configuration

K2 is designed with either one or two banks of memory. Minimum memory depends on the kind of chips installed. A bank may be equiped with either 128 MB (8M x 8), 256MB (16M x 8) or 512MB (32M x 8).

This BSP version supports the dynamic determination of memory size at both boot and kernel initialization time. Using this feature, the VxWorks kernel determines dynamically how much memory is on the system, then configures the Memory Management Unit (MMU) to reflect the size. As a result, only one kernel image is necessary for all possible board configurations.

With configurations larger than 32MB, however, VxWorks will have trouble loading either executable objects or data files into memory. The error, "Relocation value does not fit in 24 bits," will appear. This is due to the design of VxWorks on the PowerPC platform.

The BSP implements a partial work-around for this problem but, when the memory configuration is larger than 32MB, the VxWorks kernel requires further reconfiguration by the user application.

When a module is loaded, it is placed in high memory, and memory is consumed from the end towards the beginning. However, some PowerPC instructions limit branch calls to within a 32MB of any instruction location. As a result, a module that is loaded, regardless of whether it is program or data, must be within the lowest 32MB of memory in order for the kernel to (potentially) execute its content.

By default, the kernel manages only the first 32MB of memory when it initializes and configures. Change this by defining the C macro **LOCAL_MEM_AUTOSIZE ("#define LOCAL_MEM_AUTOSIZE")** at the beginning of **config.h**. This enables the dynamic configuration of the memory that VxWorks will manage based upon the size of DRAM on the board. With this flag **excluded**, loading of any modules into lower memory can be performed. Once all modules are loaded, the user can choose to have VxWorks manage the remainder of memory by making a call to the routine memAddToPool(char *memPtr, int memSize). For the Power•K2 board the call would be in the form of

```
memAddToPool(0x2000000, sysLocalMemSize() - 0x2000000)
```

where **sysLocalMemSize()** returns the total size of memory on the board.

> **Note**: All modules must loaded before call to memAddToPool() is made or the load error, *Relocation value does not fit in 24 bits,* will occur:

5.5.2 Determining Memory Size

- When system is first started, the VxWorks banner and the function **sysMemTop()** indicates the memory size, less any user reserved memory (**USER_RESERVED_MEM**).
- After start up, call **memShow()** to determine how much memory the system is currently managing.
- Use the function **sysLocalMemSize()** to obtain the total DRAM size of the board.
- By default **LOCAL_MEM_AUTOSIZE** is not defined.

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5.5.3 Determining L2 Cache Configuration

Determine L2 cache configuration in a similar fashion. The ROM resident VxWorks boot loader determines whether L2 cache is present and, if so, its size—256K, 512K, or 1MB. The cache is then automatically configured and initialized at boot time. L2 is not enabled by the BSP.

This L2 cache function initializes the L2 Control Register in the 750 L2 Cache Control Register. This routine takes into account the PLL setting to be used for the L2 clock constant ration by reading the 750 HiD1 register. Each bits are ored and written to the L2 Cache Control Register with L2 enable bit cleared.

5.5.3.1 SysL2CacheEnable

This L2 cache function enables the L2 interface by setting L2 enable bit 0 in the 750 L2 Cache Control Register. This routine takes into account the PLL setting to be used for the L2 clock constant ratio by reading the 750 HiD1 register. Each bits are ored and written to the L2 Cache Control Register with L2 enable bit set. The routine samples the L2 Global Invalidate In Progress Bit until it is cleared.

5.5.3.2 SysL2CacheDisable

This L2 cache function disable L2 by clearing bit 0 of the 750 L2 Cache Control Register.

5.5.4 Memory Management Unit (MMU) Configuration

With respect to CPU mappings, the VxWorks configuration follows a virtual-to-physical translation by default. This is based upon the PowerPC microprocessor *Common Hardware Reference Platform* (CHRP) which has superseded the **P**owerPC **RE**ference **P**latform (PreP). As a result, any physical address detailed in the PreP specification has the same processor address interpretation from the perspective of VxWorks.

Two MMU facilities are utilized in the processor to support the functions of the BSP. The Block Address Translation (BAT) table is used to map to large regions of memory and is used to access areas such as the Peripheral Component Interconnect (PCI) memory. For smaller regions of memory, such as SDRAM and PCI configuration register, the Page Address Translation (PAT) table is used for mapping. Use the BAT when there is need to set up access to a large region of memory with the same caching characteristics. Use the PAT when accessing small regions, especially when fine control over the caching characteristics of many different regions is required.

BAT table mapping always takes precedence over the PAT table. Whenever there is an address translation, the BAT is conferred with first. If a match is not found, the PAT table is then checked. Refer to the PowerPC Microprocessor Family: The Programming Environments from IBM Microelectronics and IBM Corporation for more details.

5.5.4.1 BAT Table

There are eight processor register entries in the BAT table for processors that are newer than the PowerPC 4XX/601 series. Eight entries are used to map to regions of memory, four to where instructions are stored and four to where data is stored.

In the BSP file sysLib.c, the structure **sysBatTable[]** contains the entries for the BAT table. The kernel uses this at initialization time to set up the BAT registers for operation in the processor. This structure is shown below:

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```
UINT32 sysBatDesc [2 * (_MMU_NUM_IBAT + _MMU_NUM_DBAT)] =
    {
    /* I BAT 0 */
    ((ROM_BASE_ADRS & _MMU_UBAT_BEPI_MASK) | _MMU_UBAT_BL_512K |
    _MMU_UBAT_VS | _MMU_UBAT_VP),
    ((ROM_BASE_ADRS & _MMU_LBAT_BRPN_MASK) | _MMU_LBAT_PP_RW |
    _MMU_LBAT_CACHE_INHIBIT | _MMU_LBAT_GUARDED),

    /* I BAT 1 */
    (((ROM_BASE_ADRS | 0x80000) & _MMU_UBAT_BEPI_MASK) | _MMU_UBAT_BL_256K |
    _MMU_UBAT_VS | _MMU_UBAT_VP),
    (((ROM_BASE_ADRS | 0x80000) & _MMU_LBAT_BRPN_MASK) | _MMU_LBAT_PP_RW |
    _MMU_LBAT_CACHE_INHIBIT | _MMU_LBAT_GUARDED),

    /* I BAT 2 */
    (((ROM_BASE_ADRS | 0xC0000) & _MMU_UBAT_BEPI_MASK) | _MMU_UBAT_BL_128K |
    _MMU_UBAT_VS | _MMU_UBAT_VP),
    (((ROM_BASE_ADRS | 0xC0000) & _MMU_LBAT_BRPN_MASK) | _MMU_LBAT_PP_RW |
    _MMU_LBAT_CACHE_INHIBIT | _MMU_LBAT_GUARDED),


    /* I BAT 3 */
    (((ROM_BASE_ADRS | 0xE0000) & _MMU_UBAT_BEPI_MASK) | _MMU_UBAT_BL_128K |
    _MMU_UBAT_VS | _MMU_UBAT_VP),
    (((ROM_BASE_ADRS | 0xE0000) & _MMU_LBAT_BRPN_MASK) | _MMU_LBAT_PP_RW |
    _MMU_LBAT_CACHE_INHIBIT | _MMU_LBAT_GUARDED),

    /* D BAT 0 */
    ((((unsigned int)CPU_PCI_ISA_MEM_ADRS + 0*MEM_256MB) &
   _MMU_UBAT_BEPI_MASK)
    | _MMU_UBAT_BL_256M |
    _MMU_UBAT_VS | _MMU_UBAT_VP),
    ((((unsigned int)CPU_PCI_ISA_MEM_ADRS + 0*MEM_256MB)  &
   _MMU_LBAT_BRPN_MASK) | _MMU_LBAT_PP_RW |
    _MMU_LBAT_CACHE_INHIBIT | _MMU_LBAT_GUARDED),

    /* D BAT 1 */
    ((((unsigned int)CPU_PCI_ISA_MEM_ADRS + 1*MEM_256MB) &
   _MMU_UBAT_BEPI_MASK)
    | _MMU_UBAT_BL_256M |
    _MMU_UBAT_VS | _MMU_UBAT_VP),
    ((((unsigned int)CPU_PCI_ISA_MEM_ADRS + 1*MEM_256MB)  &
   _MMU_LBAT_BRPN_MASK) | _MMU_LBAT_PP_RW |
    _MMU_LBAT_CACHE_INHIBIT | _MMU_LBAT_GUARDED),

    /* D BAT 2 */
    ((((unsigned int)CPU_PCI_ISA_MEM_ADRS + 2*MEM_256MB) &
   _MMU_UBAT_BEPI_MASK)
    | _MMU_UBAT_BL_256M |
    _MMU_UBAT_VS | _MMU_UBAT_VP),
    ((((unsigned int)CPU_PCI_ISA_MEM_ADRS + 2*MEM_256MB) &
   _MMU_LBAT_BRPN_MASK)
    | _MMU_LBAT_PP_RW |
    _MMU_LBAT_CACHE_INHIBIT | _MMU_LBAT_GUARDED),
```


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```
 /* D BAT 3 */
 ((((unsigned int)CPU_PCI_ISA_MEM_ADRS + 3*MEM_256MB) &
_MMU_UBAT_BEPI_MASK)
 | _MMU_UBAT_BL_256M |
 _MMU_UBAT_VS | _MMU_UBAT_VP),
 ((((unsigned int)CPU_PCI_ISA_MEM_ADRS + 3*MEM_256MB) &
_MMU_LBAT_BRPN_MASK)
 | _MMU_LBAT_PP_RW |
 _MMU_LBAT_CACHE_INHIBIT | _MMU_LBAT_GUARDED),
 };
```

The DBAT for the 750 processor is mapped differently during the hardware initialization process:

```
/* D BAT 0 - Local Memory (0x0000_0000 to 0x1000_0000)  256MB */

BATRegs[4].LBAT =

((LOCAL_MEM_LOCAL_ADRS & _MMU_LBAT_BRPN_MASK) | _MMU_LBAT_PP_RW |

_MMU_LBAT_CACHE_INHIBIT | _MMU_LBAT_GUARDED);

BATRegs[4].UBAT =

((LOCAL_MEM_LOCAL_ADRS & _MMU_UBAT_BEPI_MASK) | _MMU_UBAT_BL_256M |

_MMU_UBAT_VS | _MMU_UBAT_VP);


/* D BAT 1 -  ROM Space, PCI_ISA_IO and PCI_ISA_MEM space,

-- PCI_IO space, PCI_CNFG_ADDR, PCI_CNFG_DATA registers

-- PCI_INT_ACK, ROM SPACE (0xfd00_0000 to 0xffff_ffff)

-- NOTE: PCI memory space 0xf000_0000 to 0xfcff_ffff

-- (0xf000_0000 to 0xffff_ffff) - 256 MB */

 BATRegs[5].LBAT =

     ((MAP_B_PCI_ROM_BASE_ADRS & _MMU_LBAT_BRPN_MASK) |
_MMU_LBAT_PP_RW |

     _MMU_LBAT_CACHE_INHIBIT | _MMU_LBAT_GUARDED);

BATRegs[5].UBAT =

     ((MAP_B_PCI_ROM_BASE_ADRS & _MMU_UBAT_BEPI_MASK) |_MMU_UBAT_BL_256M |

     _MMU_UBAT_VS | _MMU_UBAT_VP);
```


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```
/* D BAT 2 - PCI Memory Space (0x8000_0000 to 0x8fff_ffff) */
BATRegs[6].LBAT =
     ((CPU_PCI_MEM_ADRS & _MMU_LBAT_BRPN_MASK) | _MMU_LBAT_PP_RW |
     _MMU_LBAT_CACHE_INHIBIT | _MMU_LBAT_GUARDED);
BATRegs[6].UBAT =
     ((CPU_PCI_MEM_ADRS & _MMU_UBAT_BEPI_MASK) | _MMU_UBAT_BL_256M |
     _MMU_UBAT_VS | _MMU_UBAT_VP);
/* D BAT 3 -  PCI Memory Space (0x9000_0000 to 9fff_ffff) */
      BATRegs[7].LBAT =
     ((CPU_PCI_MEM2_ADRS & _MMU_LBAT_BRPN_MASK) | _MMU_LBAT_PP_RW |
     _MMU_LBAT_CACHE_INHIBIT | _MMU_LBAT_GUARDED);
BATRegs[7].UBAT =
     ((CPU_PCI_MEM2_ADRS & _MMU_UBAT_BEPI_MASK) | _MMU_UBAT_BL_256M |
     _MMU_UBAT_VS | _MMU_UBAT_VP);
```


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Table 5-4: 750 DBAT MMU Configuration

BAT DESCRIPTION	ADDRESS RANGE	ADDRESS DESCRIPTION
DBAT0	0x00000000 0x10000000	LOCAL MEMORY SPACE
DBAT1	0xF0000000 0xFFFFFFF	PCI I/O, PCI config/data register, PCI Int Ack, ROM, Peripherals Registers
DBAT2	0x80000000 0x8FFFFFFF	CPU to PCI MEM SPACE
DBAT3	0x7FC00000 0x7FFFFFFF	CPLD Registers
DBAT3	0x90000000 0x9FFFFFFF	CPU to PCI MEM SPACE

The default configuration sets the four entries of the instruction BAT (IBAT) to map to the region of memory where the ROM devices reside. It is set up as cache inhibited. This region is the area where the VxWorks boot ROM code resides. If this is modified, the new setting should ensure access to at least one MB starting at **ROM_BASE_ADRS**. All of the data BAT (DBAT) entries are used to enable access to addresses starting in the PCI Memory Space.

5.5.4.2 Page Address Translation Table

The BAT has dedicate registers in the processor for use in address translations, but the page tables are set up using system memory. Using the BAT may save memory because table sizes vary depending on the number of mapping entries. Using the page tables requires a fixed 32 bytes of system memory to map every 4 KB of memory, a factor of 8 to 1.

In the BSP file sysLib.c, the structure **sysPhysMemDesc[]** contains the entries for the page table. At initialization, the kernel uses this to set up the operation page table entries. Part of the structure is shown below:

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```
PHYS_MEM_DESC sysPhysMemDesc [] =

    {

    {

    (void *) LOCAL_MEM_LOCAL_ADRS,

    (void *) LOCAL_MEM_LOCAL_ADRS,

     LOCAL_MEM_SIZE_DEF,

     VM_STATE_MASK_VALID | VM_STATE_MASK_WRITABLE |
VM_STATE_MASK_CACHEABLE,

    VM_STATE_VALID      | VM_STATE_WRITABLE      | VM_STATE_CACHEABLE

    },


{

    (void *) CPU_PCI_ISA_IO_ADRS,

    (void *) CPU_PCI_ISA_IO_ADRS,

    CPU_PCI_ISA_IO_SIZE,

    VM_STATE_MASK_VALID | VM_STATE_MASK_WRITABLE | VM_STATE_MASK_CACHEABLE,

    VM_STATE_VALID      | VM_STATE_WRITABLE      | VM_STATE_CACHEABLE_NOT

    },
/* added CPU_ISA_MEM_SPACE */


    {

    (void *) CPU_PCI_ISA_MEM_ADRS,

    (void *) CPU_PCI_ISA_MEM_ADRS,

    CPU_PCI_ISA_MEM_SIZE,

    VM_STATE_MASK_VALID | VM_STATE_MASK_WRITABLE | VM_STATE_MASK_CACHEABLE,

    VM_STATE_VALID      | VM_STATE_WRITABLE      | VM_STATE_CACHEABLE_NOT

    },


    {

    (void *) CPU_PCI_IO_ADRS,

    (void *) CPU_PCI_IO_ADRS,
```


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```
    CPU_PCI_IO_SIZE,
    VM_STATE_MASK_VALID | VM_STATE_MASK_WRITABLE | VM_STATE_MASK_CACHEABLE,
    VM_STATE_VALID      | VM_STATE_WRITABLE      | VM_STATE_CACHEABLE_NOT
    },


    /* Map in Flash ROM addresses to support the flash programming utili-
ties */
   /* The BAT may have already map this area in but we do it again just in
*/
    /* case the BAT is needed for other purposes
*/
    {
    (void *) 0xFF000000,
    (void *) 0xFF000000,
    0x01000000,                                 /* 16 meg */
    VM_STATE_MASK_VALID | VM_STATE_MASK_WRITABLE | VM_STATE_MASK_CACHEABLE,
    VM_STATE_VALID      | VM_STATE_WRITABLE      | VM_STATE_CACHEABLE_NOT
    }
    };
```


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5.6 Interrupts

K2 has several sources for interrupts. All interrupts are ultimately routed to one interrupt condition on the processor, the PowerPC External/ Interrupt condition. This interrupt event is also shared with the Decrementor timer interrupt event. Once it is determined that an external interrupt has occurred, the processor will decode to one of fifteen possible interrupt conditions by polling the Acer M1543C PCI-to-ISA bus bridge. This chip, besides being the interface to the ISA bus, also serves to route all interrupts to the processor. Using a pair of onboard 8259 interrupt controllers, the M1543C is set up to handle the fifteen distinct interrupt conditions. It then reports the conditions to the processor via the polling process to an interrupt acknowledge register. The fifteen different conditions, as defined for K2, are shown in Table 5-5: ISA Interrupt Levels, on page 2-15, below. These interrupts are referred to as ISA interrupts because they are handled by the M1543C.

Table 5-5: ISA Interrupt Levels

Interrupt Level	Device	Interrupt Vector	Configuration Macro
0	Onboard Timer	PIT_INT_VEC	PIT_INT_LVL
1	INTEL 82559 Ethernet Controller	LN_INT_VEC	LN_INT_LVL
2	Reserved	N/A	N/A
3	Serial Port 2	COM2_INT_VEC	COM2_INT_LVL
4	Serial Port 1 (Console)	COM1_INT_VEC	COM1_INT_LVL
5	PMC/PCI Interrupt 1	PMC1_INT_VEC	PMC1_INT_LVL
6	PMC/PCI Interrupt 2	PMC2_INT_VEC	PMC2_INT_LVL
7	Parallel Port	PP_INT_VEC	PP_INT_LVL
8	Real Time Clock	RTC_INT_VEC	RTC_INT_LVL
9	CPCI INT A	CPCI_INTA_VEC	CPCI_INTA_LVL
10	CPCI INT B	CPCI_INTB_VEC	CPCI_INTB_LVL
11	CPCI INT C	CPCI_INTC_VEC	CPCI_INTC_LVL
12	CPCI INT D	CPCI_INTD_VEC	CPCI_INTD_LVL
13		DMA_ASSERTED_VEC	DMA_ASSERTED_LVL
14	Primary IDE	P_IDE_VEC	P_IDE_LVL
15	Secondary IDE	S_IDE_VEC	S_IDE_LVL

VxWorks provides the routines intConnect (VOIDFUNCPTR *vector, VOIDFUNCPTR routine, int parameter), intDisable (int), and intEnable (int), which facilitates connection and enabling of an interrupt level. For instance, to connect a user defined interrupt handler for the Real Time Clock the sequence would be

```
intConnect(INUM_TO_IVEC(RTC_INT_VEC), (VOIDFUNCTR)myFunc, myArg)
```

INUM_TO_IVEC is a system defined macro that should be used on all intConnect calls. To Enable/Disable the interrupt use:

```
intEnable(RTC_INT_LVL) or intDisable(RTC_INT_LVL)
```

In addition to each of the fifteen interrupt levels, a device may have multiple conditions associated with it. For instance, a PMC device supplied by a third-party vendor may have status as to a particular interrupt that has occurred that caused the PCM interrupt event.

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5.7 PCI Bus Devices

K2's local bus is implemented using the PCI standard as its main interface. The bus conforms to the standards of PCI Specification 2.1, and as such supports PCI Configuration, I/O, and Memory cycles. In conjunction with the PowerPC micropressor Common Hardware Reference Platform (CHRP) specification the local bus implements the mapping from CPU to PCI as show in the Table 5-6: Processor to PCI Translation, on page 2-16 below:

Table 5-6: Processor to PCI Translation

Processor Address Range	PCI32 Address Range	PCI64 Address Range	Definition
00000000 03FFFFFF	No PCI32 Cycle	No PCI64 Cycle	System memory space (64M)
80000000 81000000	00000000 01000000	NA	PCI32 ISA IO Space
C0000000 C1000000	00000000 01000000	NA	PCI32 ISA Memory Space
810000000 8FFFFFFF	01000000 01FFFFFF	NA	PCI32 IO Space
C10000000 CFFFFFFF	01000000 01FFFFFF	NA	PCI32 Memory Space
90000000 94000000	NA	00000000 04000000	PCI64 IO Space
A0000000 C0000000	NA	40000000 60000000	PCI64 Memory Space
FF508000	PCI CNFG ADDR		PCI32 Configuration Address Register
FF508010	PCI CNFG DATA		PCI32 Configuration Data Register
FF408000		PCI CNFG ADDR	PCI64 Configuration Address Register
FF408100		PCI CNFG DATA	PCI64 Configuration Data Register
FFE00000 FFFFFFFF	No PCI32 Cycle	No PCI64 Cycle	ROM space

From the PCI I/O address space, the address ranges are as shown below. The processor memory cannot be accessed for this space.

Table 5-7: PCI I/O to Processor Translation

PCI I/O Transactions	Processor Address Range	Definition
00000000 - IOSIZE	No local memory cycle.	PCI I/O space.

The IOSIZE is defined by the CPC710 IOSIZE Register in the CPC710 Specification.Refer to 2.3 Related Documents, on page 2-4.

The PCI Memory address space address ranges are shown below.

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Table 5-8: PCI Memory to Processor Translation

PCI Memory Transactions	Processor Address Range	Definition
40000000 - MSIZE	No local memory cycle	PCI Memory Space

Table 5-9: PCI Memory to Processor Translation

PCI Memory Transactions	Processor Address Range	Definition
80000000 FFFFFFFF	00000000 80000000	Local Memory space.

Note: Refer to CPC710-100 Databook for further details on memory addressing.

5.8 PCI Devices

The are four PCI devices attached to the PCI32 bus of the K2 board:

- PMC1
- PMC2
- Ethernet
- PCI/ISA bridge devices

Within the PCI/ISA bridge chip, there are four additional PCI agents:

- ISA interrupt controller
- IDE
- PMU
- USB devices

In addition, the AMD and INTEL Flash devices are also attached to the bus.

5.9 PCI Configuration Cycles

This method uses the Type 1 configuration cycle of the PCI specification. The Direct method will not work if code is migrated to another PReP compatible hardware platform, but Type 1 will still function.

5.9.1 Type 0/1 Configuration Cycles

Type 0/1 Configurations Cycles always involves two separate I/O operations.

The first operation writes the requested address to the PCICFGADR register.

The second operation reads or writes the PCICFGDATA register.

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For this type of cycle, the address for the Ethernet chip would be 0x80001800.

Notes:

The CPC710 specific PCI Registers are accessible using the type 1 configuration method.

Type 1 Configuration Cycles can be used to probe either the local PCI bus or subordinate/ secondary buses (by setting bits 16-23 for the bus number).

5.9.2 CPC710 Address and Data Register Locations

Table 5-10: CPC710 Definition Address and Data Register Locations

BUS	PCICFGADR Register Location	PCICFGDATA Register Location
PCI32	0xFF508000	0xFF508010
PCI64	0xFF408000	0xFF408010

The format of the PCICFGADR register, in general, is show below:

31 30 24 23 16 15 11 10 8 7 2 1 0

E	0000000	Bus Number	Device Number	Function	Register	00

E - Enable Configuration Cycle (1 = enable, 0 = disable).

Bus Number - Selection of bus number to access. For local devices this should be 0x00.

Device Number - Selection of the device number on the bus.

Function - Selection of function for the device. This is used most often for devices with multiple sets of configuration registers, one for each major function of the device.

Register - Selection of register of the device.

The register sysPokePCI() and sysPeekPCI() can be used to for Type 1 Configuration Cycles. Refer to Sections 5.18.2 sysPeekPCI(), on page 2-56 and 5.18.3 sysPokePCI(), on page 2-57 for a description of these functions. For example, to read the device/vendor ID register of the Ethernet chip use the following sequence:

sysPokePCI(0xFF508000, 0x80001800)

sysPeekPCI(0xFF508010)

To write a value to the Ethernet configuration register at offset 0x40 use the following:

sysPokePCI(0xFF508000, 0x80001840)

sysPokePCI(0xFF508010, val)

Reading or writing of the PCI devices requires that data is byte swapped before being written to the registers. The PCI utility functions performs this.

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5.9.3 PCI I/O Cycles

In the CPC710 map configuration for VxWorks the PCI I/O space is in the range **0x01000000 - 0x01FFFFFF (0x81000000 - 0x81FFFFFF** as seen from the CPU).

> **Notes :**
>
> - The CPC710 decodes the above range.
> - The Configuration Macro used to define the PCI I/O addresses can be found in *powerk2.h***.**

Use the functions sysPokePCI() and sysPeekPCI() to access the I/O space. Refer to Sections 5.18.2 sysPeekPCI(), on page 2-56, and 5.18.3 sysPokePCI(), on page 2-57, for a description of these functions.

For example, to read the device/vendor register of a PCI device, with an assigned address of **0x01020000** I/O, use the following:

sysPeekPCI(0x81020000)

To write a value to the same PCI device register at offset 0x40, use the following:

sysPokePCI(0x81020040, val)

Reading or writing a PCI device requires that data is byte swapped before being written to the registers. The PCI utility functions perform this.

5.9.3.1 PCI Memory Cycles

In the CPC710 map configuration for VxWorks, PCI Memory space is in the range **0x01000000 - 0x1FFFFFFF** (**0xC1000000 - 0xD1000000** as seen from the CPU). VxWorks sets up the MMU to access the PCI Memory. By default, no devices occupy PCI Memory space on K2.

To set up a device to respond to an available Memory region, simply set its Base Address and Command Registers in the Configuration Space. This is hardware specific and each PCI device may have a unique implementation for the Base Address Register.

5.9.4 Adding PMC Devices

Use the information provided in the previous section to configure devices across the PMC expansion from K2. Take these steps.:

- Set up VxWorks to probe for the PMC device.
- Provide PCI I/O and/or PCI Memory addresses to program the Base Address Registers.
- Provide a driver initialization function to perform any additional setup of the device.
- Connect an interrupt handler for the PMC and enabling interrupts.

Setting up a PMC device is logically no different than setting up a standard PCI device. In fact, a PMC device may be considered just another PCI device. For this reason, a DEC21140 will be used as an example. A user PMC device may be set up in the exactly the same manner.

5.9.5 Probing the PMC

To set up VxWorks to automatically probe the PMC slot, use the function sysPciDevProbe(), a standard system call. Refer to the WindRiver Reference Manual for the exact definition of this function. This function is located in the file **powerk2/pci/pciLocalBusIn.c**. A summary of the function is shown below.

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```
STATUS sysPciDevProbeIndirect (
ULONG pciCnfgBaseAdrs,          /* PCI configuration base address */
ULONG pciVndrDevId,             /* PCI vendor device ID */
ULONG *pPciDevCnfgAdrs          /* PCI device config addr returned */
BOOL   bPCIBus                  /* PCI32 or PCI64 Architecture          )
```

pciCnfgBaseAdrs is the base Configuration address to start probing for PCI devices. This is defined in the macro **CPU_PCI32_CNFG_ADRS** or **CPU_PCI64_CNFG_ADRS**. This is an Indirect Configuration address. The VxWorks default is direct and uses the files under **powerk2/pci/pciLocalBus.c**.

pciVndrDevId is the device specific Device and Vendor ID as found in all PCI configuration registers. It has base address zero. For example, a DEC21140 Ethernet chip has a Device ID of 0x0009 and Vendor ID of 0x1011 so the value for pciVndrDevId is 0x00091011. The variable pPciDevCnfgAdrs will be set to the exact base address of the configuration registers of the device if the function has probed successfully. The returned address will be 0x80802000.

Probing for the PCI devices is performed in the function sysHwInit(), located in the file **sysLib.c**. The case for an Ethernet is shown below.

```
/* configure PCI LANCE device */

if (sysPciDevProbeIndirect (CPU_PCI_CNFG_ADRS, PCI_ID_LN_DEC, &pciDevCnf-
gAdrs, PCI32BUS)

        == OK)

   {

   IO_SYNC;

   sysPciDevConfigIndirect (

              CNFG_LN_ADRS,

              PCI_IO_LN_ADRS,

              NULL,

              (CSR_BM_EN | CSR_IO_EN),


  PCIBUS32,

              NULL,

              NONE,

              NONE

              );

}
```


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5.9.6 Programming Base Addresses

Referring to the code in Section 5.9.5 Probing the PMC, on page 2-19, if the probe for the device is successful, an attempt will be made to program the PCI I/O and/or Memory address into the register using the function sysPciDevCnfg(). The declaration of the function is show below.

```
STATUS sysPciDevConfigIndirect
  (
  ULONG     devPciCnfgAdrs,     /* device PCI config space addrs */
  ULONG     devIoBaseAdrs,      /* device IO base address */
  ULONG     devMemBaseAdrs,     /* device memory base address */
  ULONG     command,            /* command to load in command reg */
  BOOL bPCIBus                  /* PCI 32 or PCI64 Architecture */
  FUNCPTR   devPciRoutine,      /* device specific function */
  ULONG     devPciArg1,         /* device specific function argument */
  ULONG     devPciArg2          /* device specific function argument */
  )
```

devPciCnfgAdrs is the variable pciDevCnfgAdrs returned from sysPciDevProbe(), devIoBaseAdrs is the PCI I/O address to program into the I/O Base Address register of the device, and devMemBaseAdrs is the PCI Memory address to program into the Memory Base Address register of the device. The logic used in sysPciDevConfig to determine which configuration register to program is as follows:

- For PCI I/O address, *sysPciDevConfig* will probe beginning at configuration register 0x04 until it finds a register with bit zero set. This is in accordance to PCI 2.1 Specifications which states that the PCI I/O Base Address Register should always hardwire bit zero to a 1 to indicate an I/O base address.
- For PCI Memory address, *sysPciDevConfig* will begin probing at configuration register 0x04 and continue until it finds a register with bit zero cleared. This is in accordance with PCI 2.1 specifications which state that the PCI Memory Base Address Register should always be hard-wired bit zero to a 0 to indicate a Memory base address.
- Once this criteria is met, the values passed via *devIoBaseAdrs* and *devMemBaseAdrs* will be written to their respective registers.

Using the Ethernet again as an example, an I/O address given by **PCI_IO_LN_ADRS** (0x01020000) is passed to the function call, and a **NULL** is passed for the Memory address, because the Universe does not have a default base address register. Refer to Section 5.9.3 PCI I/O Cycles, on page 2-19 for a description of the assigned PCI I/O addresses.

Based upon the description above, it is assumed that the base address register setups of a PMC device will follow standard PCI convention. If they do not, extra logic may be needed in a driver initialization function (pciDevRoutine) as described in the next section. Write the value, *command*, into the Command register. There may be many characteristics that can be programmed into this register. Refer to the PCI 2.1 Specification for a discussion of most of the bit settings. Of particular importance are the:

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- Bus Master Enable (bit 2)
- PCI Memory Enable (bit 1)
- PCI I/O Enable (bit 0) bits

The Bus Master bit must be set if the PMC device has PCI bus mastering capabilities. The other two bits simply tell the device it can respond to PCI requests that fall within the windows set up with the base addresses. The system macros **CSR_BM_EN, CSR_MEM_EN**, and **CSR_IO_EN** implement these bits respectively. The DEC21140, however, has master capabilities, is set up for I/O space, and cannot respond to Memory space.

The last three arguments to sysPciDevConfig() are the driver initialization function and two arguments that can be passed to it. These are described in the next section.

5.9.6.1 Driver Initialization Function

It is likely that additional initializations will be required beyond those of the VxWorks kernel to completely configure the PMC. Each device will require specific setups and need some type of driver to handle them. This is not unlike any device driver written for a particular hardware. The function sysPciDevConfig() provides a way for the application to supply this needed driver initialization code via the parameters devPciRoutine for the function and devPciArg1 and devPciArg2.

The driver initialization function provided by the user adds most of the extract support and is left to the developer to implement. The interrupt handler, discussed in the next section, may require similar treaent.

5.9.6.2 Connecting an Interrupt Handler

This section describes the general method of connecting interrupt handlers for PMC devices. It is recommended that the interrupt connection call and enable be made in the function **sysHwInit2()**, located in sysLib.c. This will maintain compatibility with future VxWorks releases. The interrupt connection could be done in **sysHwInit()**, but the enable should be put off until **sysHwInit2()**.

For a PMC device that has an interrupt handler myIntHandler(), and argument myArg, the call could be

```
/* connect PMC interrupt */

(void)intConnect (INUM_TO_IVEC(PMC_INT_VEC), myIntHandler, myArg);


 /* interrupts can only be turned on ultimately by the PIC int ctrlr */

 intEnable (PMC_INT_LVL);
```


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5.10 Timers

There are four timers available on the K2 board:

- Decrementor
- Timebase
- Watchdog
- Periodic Timer

The sections below describe these facilities.

5.10.1 Decrementor

The system timer facility is implemented, by default, using the Decrementor facilities of the PowerPC 750 CPU. This provides the kernel rescheduling timer and system clock functions. There is no timer support for the Auxiliary Clock facilities of VxWorks.

5.10.2 Timebase Timer

This is a non-interrupt timer available in the processor. It is most useful for time stamping purposes. The utilities available for this timer are located in section 5.13 Timing Utilities, on page 2-25.

5.10.3 Watchdog Timer

The Watchdog timer provides a method of interrupting the processor on a watchdog timer expiration. This timer is based on a 256msec time period. Upon expiration of the timer an **SRESET** condition is sent to the processor. This causes an unconditional jump by the instruction fetch logic of the processor to either address 0xFFF00100 or 0x100, based upon the setting of the processor Hardware Implementation Dependent 0 (HID0) Register. If asserted while the VxWorks kernel is running the default will be 0x100. Refer to 3.14 Timers/Counters, on page 2-12, for a detailed discussion on the hardware implementation of the watchdog.

5.10.4 Periodic Timer

The Periodic timer provides a method of interrupting the processor upon a periodic timer expiration. This timer is based on a 1KHZ clocking frequency. With an 8 bit resolution of the timer register this translates into a timer period of between 1 msec and .256 sec. Refer to 3.14 Timers/Counters, on page 2-12, for a detailed discussion on the hardware implementation of the periodic timer.

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Table 5-11: Periodic Timer Utilities

Name	Description
STATUS sysPeriodicConnect(FUNCPTR routine, int val)	Connects a user defined handler with the Periodic Timer interrupt.
STATUS sysPeriodicStart()	Start the Periodic Timer at the current count value.
STATUS sysPeriodicStop()	Stop the Periodic Timer. The current count value freezes.
STATUS sysPeriodicSet(count)	Program the <count> value into the counter.
void sysPeriodicEnable ()	Enable interrupt on Periodic Timer completion
void sysPeriodicDisable ()	Disables interrupt on Periodic Timer completion

NOTE: These functions are planned for a future K2 BSP release.

5.11 Serial Devices

K2 has two RS-232 serial ports. They can be configured from 50 to 115.2K baud rate and do not support any modem signals. The default rate set up in the VxWorks boot ROM is 9600.

The serial devices support serial mode debugging as required by VxWorks Tornado debugger.

5.12 BSP Utilities

Several software files/routines have been added to the BSP as part of the delivered distribution. These files are provided to assist in both testing the software/hardware and to provide some programming examples for the various components of the board.

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5.13 Timing Utilities

An additional timer on the PowerPC processor provides a timebase capability to software applications. The following routines provide basic access to the TimeBase Register.

5.13.1 sysTimeBaseInit()

NAME

sysTimeBaseInit() - Initialize the timebase register

SYNOPSIS

void sysTimeBaseInit

(

)

DESCRIPTION

Initializes the timebase register. This should be called before each sequence of calls to sysTimeBaseRead(). This utility is contained in sysLib.c.

RETURNS

N/A

5.13.2 sysTimeBaseRead()

NAME

sysTimeBaseRead() - Get current timebase value

SYNOPSIS

double sysTimeBaseInit
(
)

DESCRIPTION

Returns the number of seconds since the last call to *sysTimeBaseInit()*. This utility is contained in *sysLib.c*.

RETURNS

N/A.

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5.14 Flash Programming Utilities

A flash utility library has been provided with the BSP which supports programming the AMD AM29LV040 flash located in the socket at location U2 as well as the INTEL 28F128 8MB soldered-in flash.

The AM29LV040 provides 512K of erasable programmable flash memory that is located in a removable socket. It appears in the upper 1 Mbyte of the PPC750 at addresses **0xFFF00000-0xFFF7FFFF** if JP4 is installed. The INTEL flash appears at address **0xFFE00000-0xFFFFFFFF** if JP4 is removed.

The utility file **sysFlash.c** is an optional file which can be linked into the kernel to provide a full complement of utility functions for accessing the AMD flash device. A summary of the utilities are shown in Table 5-12: Flash Programming Utilities, on page 2-26**,** below.

Table 5-12: Flash Programming Utilities

Function	Description
PfINTELID	Gets the flash part ID
PfINTELBlkErase	Erases a block of the flash
PfINTELVerifyProgram	Verifies data programmed into flash.
PfINTELVerify	Determines if a region of the flash has been erased.
PfINTELProgram	Programs flash from data in memory
PfINTELProgramFile	Programs the contents of a file into flash memory.
PfINTELProgramBootFile	Programs the contents of a file into the boot-able area of flash memory.
PfINTEL_PAGE_SELECT	Selects one of the 8 pages in the 16MB flash device.
pfAMDVerifyProgram	Verifies data programmed into flash.
PfAMDVerify	Determines if a region of the flash has been erased.
PfAMDProgram	Programs flash from data in memory
pfAMDChipErase	Erases the entire flash parts.
pfAMDProgramFile	Programs the contents of a file into flash memory.
pfAMDProgramBootFile	Programs the contents of a file into the boot-able area of flash memory.

pfFlashInit() should be called before any of the flash utility functions. Failing to do so will yield unpredictable results.

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5.15 Flash Utility Summary

The following sections gives the detailed description of the flash programming utilities described above.

5.15.1 pfINTELID()

NAME

pfINTELID() - Gets flash part ID

SYNOPSIS

STATUS pfINTELID (void)

DESCRIPTION

Prints out the flash vendor ID

RETURNS

OK or **ERROR** if flash is not accessible

SEE ALSO

sysFlash

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5.15.2 pfINTELBlkErase

NAME

pfINTELBlkErase() - Erases a block of the flash part

SYNOPSIS

STATUS pfINTELBlkErase

(

UINT block, /* Block to erase (0-31) */

UINT flag /* Verify erase of flash */

)

DESCRIPTION

This function issues a block erase command to the flash part. Only those blocks not locked will be erased. There are 128 blocks of 128 KB which cover the entire 8MB for flash devices.

The following table shows the addresses that would be erased for each block.

> **CAUTION**: Set <flag> to TRUE for erase verification.

RETURNS

OK or **ERROR** if flash erase fails/not confirmed.

SEE ALSO

sysFlash, pfINTELBulkErase ()

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5.15.3 K2 Flash Architecture

The PowerK2 has 2 (two) available flash devices: The 512K AMD AM29LV040B socketed programming is referenced with “pfAMD.” The 16M INTEL Strataflash directly soldered on-board is referenced with “pfINTEL.”

Due to the limitations of the CPC710 (Avignon), at any given point you are only able to see a 2M window. This forces us to “page” the INTEL flash to be able to see all 16Mbytes.

Jumper JP4 is a jumper which is used as a “bootjumper” – installed and the board loads code from the socketed AMD, removed and the board loads code from the soldered INTEL’s page 1 (one). This feature has its disadvantages since it effectively removes accesses to the INTEL flash in those regions (blocks 8-11, page 1) – see Diagram A. Each consecutive page in INTEL flash memory has the full 2Mbyte access regardless of jumper position.

The following VxWorks commands have function within a VxWorks environment:

pfINTEL_PAGE_SELECT

pfINTELBlkErase

pfINTELProgramBootFile

pfAMD ChipErase

pfAMDProgramFile

“**pfINTEL_PAGE_SELECT**” does just that – selects which 2Mb “page” to access in INTEL flash space. Proper usage of this command would look like:

→ **pfINTEL_PAGE_SELECT *x*** (where *x* = the page you want to access, 1 – 8)

“**pfINTELBlkErase**” is a command that erases a block of information. Proper usage of this command would look like:

→ **pfINTELBlkErase *y*,1** (where *y* = the block you want to erase (0 – 15) and where 1 is the flag validating the erasure sequence)

“**pfINTELProgramBootFile**” is a command that, when executed properly, erases blocks 8 – 11 and programs a specified bootfile in that location. Blocks 8 – 11 range from address FFF00000 – FFF1FFFF which corresponds to PowerPC’s default bootrom address location. Proper uasge of this command would look like:

→ **pfINTELProgramBootFile** “(path&filename)”, (offset, if applicable)

Tornado generated bootrom_uncmp images typically do NOT have offsets built into them, so setting the offset to “0x100” is necessary. For example, suppose you wanted to burn a newly built bootrom image into INTEL flash memory and be able to boot from it. The file is located in the root directory. The command you would type would be:

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→ **pfINTELProgramBootFile** “bootrom_uncmp.raw”, 0x100

“**pfAMDChipErase**” is a command used to erase the AMD flash, preparing it for reprogramming. Jumper JP4 ***MUST*** be installed for ***any*** access to AMD flash. Proper usage of this command would look like:

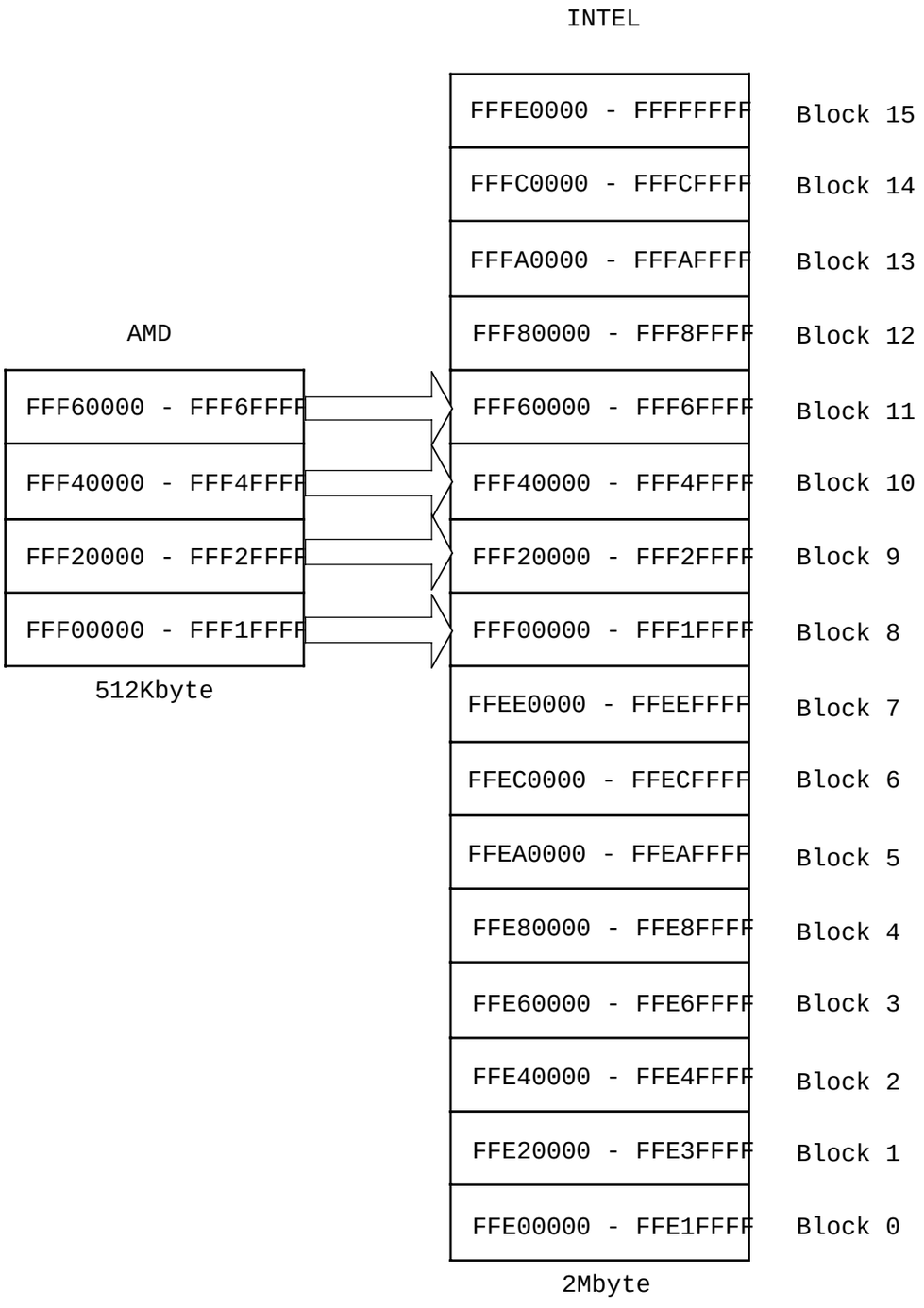
→ **pfAMDChipErase 1** (where 1 is the flag validating the erasure sequence)

“**pfAMDProgramFile**” is a command that writes a specified file into AMD flash space. Jumper JP4 ***MUST*** be installed for ***any*** access to AMD flash. Proper usage of this command would look like:

→ **pfAMDProgramFile** “(path&filename)”, (offset, if applicable)

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Diagram A



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Start	End	Block Number	Page Number
0x00000000	0x0001FFFF	0	PAGE 1
0x00020000	0x0003FFFF	1	
0x00040000	0x0005FFFF	2	
0x00060000	0x0007FFFF	3	
0x00080000	0x0009FFFF	4	
0x000a0000	0x000BFFFF	5	
0x000c0000	0x000DFFFF	6	
0x000e0000	0x000FFFFF	7	
0x00100000	0x0011FFFF	8	
0x00120000	0x0013FFFF	9	
0x00140000	0x0015FFFF	10	
0x00160000	0x0017FFFF	11	
0x00180000	0x0019FFFF	12	
0x001A0000	0x001BFFFF	13	
0x001C0000	0x001DFFFF	14	
0x001E0000	0x001FFFFF	15	
0x00200000	0x003FFFFF	16-31	PAGE 2
0x00400000	0x005FFFFF	32-47	PAGE 3
0x00600000	0x007FFFFF	48-63	PAGE 4
0x00800000	0x009FFFFF	64-79	PAGE 5
0x00A00000	0x00BFFFFF	80-95	PAGE 6
0x00C00000	0x00DFFFFF	96-111	PAGE 7
0x00E00000	0x00FFFFFF	112-127	PAGE 8

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5.15.4 pfINTELVerifyProgram

NAME

pfINTELVerifyProgram() - Verifies data programmed into Flash

SYNOPSIS

STATUS pfINTELVerifyProgram

```
(
UINT        offset,    /* Flash memory offset      */
FLASH_TYPE  *dataPtr,  /* Pointer to data to store */
UINT        len        /* Number of bytes to store */
)
```

DESCRIPTION

This function verifies that a program at address given by <dataPtr> has been properly programmed into the flash device starting at <offset> and is <len> bytes long.

RETURNS

OK or **ERROR** if there is a data mismatch

SEE ALSO

sysFlash, pfINTELVerify()

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5.15.5 pfINTELVerify()

NAME

pfINTELVerifyProgram() - Verifies data programmed into Flash

SYNOPSIS

```
STATUS pfINTELVerifyProgram
  (
  UINT        offset,    /* Flash memory offset      */
  FLASH_TYPE  *dataPtr,  /* Pointer to data to store */
  UINT        len        /* Number of bytes to store */
  )
```

DESCRIPTION

This function verifies that a program at address given by <dataPtr> has been properly programmed into the flash device starting at <offset> and is <len> bytes long.

RETURNS

OK or **ERROR** if there is a data mismatch

SEE ALSO

sysFlash, pfINTELVerifyProgram()

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5.15.6 pfINTELProgram()

NAME

pfINTELProgram() - Program flash from memory

SYNOPSIS

```
STATUS pfINTELProgram
  (
  UINT    offset,    /* Flash memory offset      */
  double  *dataPtr,  /* Pointer to data to store */
  UINT    len        /* Number of bytes to store */
  )
```

DESCRIPTION

This function programs flash memory starting at <offset> with data located at <dataPtr>. <len> bytes are programmed into the flash, rounded to the nearest 8 bytes.

RETURNS

OK or **ERROR** if programmed unsuccessfully

SEE ALSO

sysFlash, pfINTELProgramFile(), pfINTELProgramBootFile()

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5.15.7 pfINTELProgramFile()

NAME

pfINTELProgramFile() - Programs a file into flash memory

SYNOPSIS

STATUS pfINTELProgramFile

(

char *file,

UINT offset

)

DESCRIPTION

This functions programs a file given by the pointer <file> into flash memory beginning at offset <offset>

RETURNS

OK or **ERROR** if programming failed for any reason

SEE ALSO

sysFlash, pfINTELProgram(), pfINTELProgramBootFile()

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5.15.8 pfINTELProgramBootFile()

NAME

pfINTELProgramBootFile() - Programs a file into the boot-able area of the flash

SYNOPSIS

STATUS pfINTELProgramBootFile

(

char *file

)

DESCRIPTION

This function programs a file given by <file> into the region of flash that when enabled to boot, will execute that file

RETURNS

OK or **ERROR** if programming failed for any reason

SEE ALSO

sysFlash, pfINTELProgram(), pfINTELProgramFile()

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5.15.9 pfAMDChipErase()

NAME

pfAMDChipErase() - Erases the entire 512k of the flash

SYNOPSIS

```
STATUS pfAMDChipErase
  (
  UINT  flag  /* Erase verification flag */
  )
```

DESCRIPTION

This function erases the entire 512k of flash

RETURNS

OK or **ERROR** if erase was unsuccessful

SEE ALSO

sysFlash, pfAMDSectorErase()

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5.15.10 pfAMDVerifyProgram()

NAME

pfAMDVerifyProgram() - Verifies data programmed into Flash

SYNOPSIS

```
STATUS pfAMDVerifyProgram
  (
  UINT  offset,    /* Flash memory offset      */
  char  *dataPtr,  /* Pointer to data to store */
  UINT  len        /* Number of bytes to store */
  )
```

DESCRIPTION

This function verifies that a program at address given by <dataPtr> has been properly programmed into the flash device starting at <offset> and is <len> bytes long.

RETURNS

OK or **ERROR** if there is a data mismatch

SEE ALSO

sysFlash, pfAMDVerify()

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5.15.11 pfAMDVerify()

NAME

pfAMDVerify() - Determines if a region of flash has been erased

SYNOPSIS

```
STATUS pfAMDVerify
  (
  UINT  flashOffset,  /* Offset into flash        */
  UINT  len           /* Number of bytes to verify */
  )
```

DESCRIPTION

This function determines whether a region of flash memory has been erased and is ready to by written.

A <flashOffset> into the flash indicates the location to start verification and <len> indicates the number of bytes to be verified.

RETURNS

OK or **ERROR** if flash memory has data written to it

SEE ALSO

sysFlash, pfAMDVerifyProgram()

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5.15.12 pfAMDProgram()

NAME

pfAMDProgram() - Programs the flash part from memory

SYNOPSIS

STATUS pfAMDProgram

(

UINT flashOffset,

UINT from,

UINT len

)

DESCRIPTION

This function programs the flash part beginning at <flashOffset> using data from <from>. The data size is <len> bytes.

RETURNS

OK or **ERROR** if programming was unsuccessful

SEE ALSO

sysFlash, pfAMDProgramFile(), pfAMDProgramBootFile()

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5.15.13 pfAMDProgramFile()

NAME

pfAMDProgramFile() - Programs a file into flash memory

SYNOPSIS

STATUS pfAMDProgramFile

(

char *file,

UINT offset

)

DESCRIPTION

This function programs a file given by the pointer <file> into flash memory beginning at offset <offset>

RETURNS

OK or **ERROR** if programming failed

SEE ALSO

sysFlash, pfAMDProgram(), pfAMDProgramBootFile()

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5.16 Programming VxWorks Bootroms

Use the utilities described in the previous section to program a VxWorks bootrom image in the AMD device. The following sections provide examples.

First, prepare the image to be programmed into flash. Several images can be made for this purpose. The most common images are **bootrom** and **bootrom_uncmp**. Refer to the WindRiver Programming Manual for more information on these images. From these images, a raw binary file is generated using the VxWorks utility **elfToBin** to convert **bootrom** or **bootrom_uncmp** to an absolute binary file appropriate for writing to flash.

For example, to generate a suitable image for **bootrom_uncmp**, do the following in the *powerk2* directory

make bootrom_uncmp

elfToBin < bootrom_uncmp > bootrom_uncmp.raw

bootrom_uncmp.raw is now ready to be programmed into the flash @ offset 0x100.

5.16.1 AMD VxWorks Bootrom

To burn the **bootrom_uncmp.raw** image into the AMD device at a bootable offset, the following sequence should be used:

- Erase the AMD device:

  -> **pfAMDChipErase 1**
- Program the file at the appropriate flash offset location

  -> **pfAMDProgramFile “bootrom_uncmp.raw”, 0x100**

The image file is programmed at offset 0x100. This is required because the K2 process always loads its first instruction at 0x100 from the base address of the flash part. In addition, the utility function *pfAMD-ProgramFile* assumes that I/O services are available to access the file name provided. In most cases, this is provided either by access to a remote file server via the Ethernet or from storage media such as hard disk.

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5.17 PCI Configuration Utilities

Several PCI utility functions have been added to simplify the process of locating PCI bus devices. They are especially useful for probing devices beyond the local bus; that is, devices on the CompactPCI back-plane.

Using combinations of the returns, an application can locate the Configuration Space address for any PCI device given its Device/Vendor ID information. The device information, if found, is passed back in the form of a PCI Bus number, Device number, and Function number. Using this information, the calling application can then locate the base address registers of the devices and program them appropriately.

The functions described in the following sections can be found in the file **sysPCIConfigUtils.c**.

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5.17.1 sysPCIConfigWrite

NAME

sysPCIConfigWrite() - write a value to the PCI device.

SYNOPSIS

```
STATUS sysPCIConfigWrite
  (
  int   busNum,    /* bus number to access (0 - 255)    */
  int   devNum,    /* device number on the bus (0 - 31) */
  int   funcNum,   /* function for the device (0-7)     */
  int   regNum,    /* register of the device (0 - 0xFF) */
  int   dataSize,  /* size of each data (1, 2, or 4)    */
  UINT  devValue   /* value to write to the PCI device  */
  BOOL bPCIBus/* PCI bus 32(0) 64(1)          */
  )
```

DESCRIPTION

This function writes a value to the PCI device base on PCI configuration address. The input values should be bus number to access, <busNum>, device number on the bus, <devNum>, function for the device, <funcNum>, register of the device, <regNum>. The address is written to as 1, 2, or 4 bytes as specified by <dataSize> the value to write to the PCI device is given by <devValue> and <PCIBus> architecture. For example, to write a 32 bit value of 0x4488086 to register 0x3C of the device at bus number 0, device number 13, and function number 0 at PCI bus 32 use:

```
sysPCIConfigWrite 0, 13, 0, 0x3c, 4, 0x04488086,0
```

RETURNS

OK or **ERROR** if the input values is not within the range , or the address can't be probed

SEE ALSO

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5.17.2 sysPCIConfigRead

NAME

sysPCIConfigRead() - read CONFIG_ADDRESS register.

SYNOPSIS

```
STATUS sysPCIConfigRead
  (
  int    busNum,    /* bus number to access (0 - 255)            */
  int    devNum,    /* device number on the bus (0 - 31)         */
  int    funcNum,   /* function for the device (0-7)             */
  int    regNum,    /* register of the device (0 - 0xFF)         */
  int    dataSize,  /* size of each data (1, 2, or 4)            */
  void *  devValue   /* where to return value of device or vendor ID */
  BOOL bPCIBus    /* PCI Bus 32(0) or 64(1) */
  )
```

DESCRIPTION

This function reads CONFIG_ADDRESS register of the PCI Device base on PCI configuration address . The input values should be bus number to access <busNum>, device number on the bus <devNum>, function for the device <funcNum>, register of the device <regNum>, the address is read or written as 1, 2, or 4 bytes, as specified by <dataSize>, and the address where value of device or vendor ID will return. For example, to read 32 bits from bus number 0, device 13, function 0, register 0x3C at PCIBus 64 , use the following command:

Example : sysPCIConfigRead 0, 13, 0, 0x3c, 4, &val, 1

Note that the variable "val" should be initialized to 0 (zero) before the call to the function.

RETURNS

OK or **ERROR** if the input values is not within the range or the address can't be probed.

SEE ALSO

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5.17.3 sysPCIBusProbe

NAME

sysPCIBusProbe() - probe for the Vendor/Device ID.

SYNOPSIS

```
UINT sysPCIBusProbe
  (
  UINT  busNum,   /* bus number to start access    */
  UINT  devNum,   /* device number to start access */
  UINT  devVenID  /* device number on the bus      */
   BOOL bPCIBus   /* PCI Bus 32(0) 64 (1)          */
  )
```

DESCRIPTION

This function probes for the Vendor/Device ID given by <devVenID> beginning at bus <busNum> and <devNum> number at a given <PCIBus> architecture . It will also probe any subordinate buses that is found for the device. If multiple devices are on the bus/subordinate bus then the one nearest to the local bus with a lower device number and a lower function number will always be located. The format of the returned 32-bit value can be used to write to the CONFIG_ADDRESS register (0x80000CF8) for Type 1 Configuration cycles. The format of the 32-bit returned value is shown below :

```
31 30     24 23 16 15     11 10       8  7          2  1  0
 ------------------------------------------------------------
|1|Reserved|Bus #|Device #|Function #|Register #|0|0|
 ------------------------------------------------------------
```

For example, if the device is located at bus number 3, device number 13, and function number 2 the returned 32-bit value would be 0x80036B00.

RETURNS

32 bits CONFIG_ADDRESS register value or ERROR if unsuccessful

SEE ALSO

sysPCIConfigProbe2, sysPCIConfigRead, sysPCIConfigWrite

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5.17.4 sysPCIConfigProbe

NAME

sysPCIConfigProbe() - probe the PCI bus for a device

SYNOPSIS

```
UINT sysPCIConfigProbe
  (
  UINT  devVenID,  /* device number on the bus */
  UINT  *busNum,   /* bus number to access     */
  UINT  *devNum,   /* device number on the bus */
  UINT  *funcNum   /* function for the device  */
  BOOL bPCIBus     /* PCI Bus 32(0) 64(1)     */
  )
```

DESCRIPTION

This function probes the PCI Configuration Space bus to locate the device passed in <devVenID> of the given <PCIBus> architecture. If found the address information for the device is passed back in the <busNum>, <devNum>. and <funcNum> fields. It is also passed back as a 32 bit Type 1 Configuration header appropriate for writing to the PCICFGADR register. If multiple devices are on the bus/subordinate bus then the one nearest to the local bus with a lower device number and a lower function number will always be located.

If <busNum> is set to between 0 and 255 then the probe will begin at that PCI bus number else at 0. If <devNum> is set between 0 and 31 then that is the first device slot probed at the <busNum> else 0. Multi-function devices are always probed starting at function 0.

The format of the returned 32-bit value can be used to write to the PCICFGADR register for Type 1 Configuration cycles. The format of the 32-bit returned value is shown below :

```
   31 30     24 23 16 15     11 10        8 7          2 1 0
 ---------------------------------------------------------------
|1|Reserved|Bus #|Device #|Function #|Register #|0|0|
 ---------------------------------------------------------------
```

For example, if the device is located at bus number 3, device number 13, and function number 2 the returned 32-bit value would be 0x80036B00. bus number 3.

This is functionally equivalent to sysPCIConfigProbe2. It only differs in probing implementation. This is more specific and depends upon knowledge of PCI bridge devices, but takes less time to complete. See **sysPCIBusProbe** function.

RETURNS

32 bits CONFIG_ADDRESS register value or **ERROR** if unsuccessful

SEE ALSO

sysPCIConfigProbe2, sysPCIConfigRead, sysPCIConfigWrite, sysPCIShow

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5.17.5 sysPCIShow

NAME

sysPCIShow() - show all the devices on PCI bus.

SYNOPSIS

void sysPCIShow(Void)

(

Void

)

DESCRIPTION

This function displays a table of all the PCI devices on the specified <PCIBus 32 or 64> architecture and subordinate buses. The output will contain the bus number, device, number, function number, device/ vendor ID, and type of device description. The bus number, device number, and function number can be used in the calls to **sysPCIConfigRead** and **sysPCIConfigWrite**.

RETURNS

N/A

SEE ALSO

sysPCIConfigRead, sysPCIConfigWrite, sysPCIConfigProbe, sysPCIBusProbe

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5.17.6 sysPCIConfigProbe2

NAME

sysPCIConfigProbe2() - probe the PCI bus for a device

SYNOPSIS

```
UINT sysPCIConfigProbe2
  (
  UINT  devVenID,
  UINT  *busID,
  UINT  *devID,
  UINT  *funcID,
   BOOL bPCIBus,
  )
```

DESCRIPTION

This function probes the PCI Configuration Space bus to locate the device passed in <devVenID> at a specified <PCI Bus> architecture. If found the address information for the device is passed back in the <busNum>, <devNum>. and <funcNum> fields. It is also passed back as a 32 bit Type 1 Configuration header appropriate for writing to the PCICFGADR register. If multiple devices are on the bus/subordinate bus then the one nearest to the local bus with a lower device number and a lower function number will always be located.

If <busNum> is set to between 0 and 255 then the probe will begin at that PCI bus number else at 0. If <devNum> is set between 0 and 31 then that is the first device slot probed at the <busNum> else 0. Multi-function devices are always probed starting at function 0.

The format of the returned 32-bit value can be used to write to the PCICFGADR register for Type 1 Configuration cycles. The format of the 32-bit returned value is shown below :

```
31 30      24 23 16 15     11 10        8  7          2 1 0
 ------------------------------------------------------------
|1|Reserved|Bus #|Device #|Function #|Register #|0|0|
 ------------------------------------------------------------
```

For example, if the device is located at bus number 3, device number 13, and function number 2 the returned 32-bit value would be 0x80036B00.

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This function is functionally equivalent to **sysPCIConfigProbe**. It only differs in probing implementation.This is more generic and does not depend upon knowledge of PCI bridge devices but could take longer to complete.

RETURNS

32 bits CONFIG_ADDRESS register value or **ERROR** if unsuccessful

SEE ALSO

sysPCIConfigProbe, sysPCIConfigRead, sysPCIConfigWrite, sysPCIShow

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5.17.7 sysPCIToCNFG

NAME

sysPCIToCNFG() - convert PCI information to a PCICFGADR value

SYNOPSIS

UINT sysPCIToCNFG

(

UINT busNum,

UINT devNum,

UINT funcNum

)

DESCRIPTION

This function converts the <busNum>, <devNum>, and <funcNum> into a value for writing to a PCI PCICFGADR register.

RETURNS

OK or **ERROR**

SEE ALSO

sysPCIConfigProbe, sysPCIConfigRead, sysPCIConfigWrite, sysPCIShow

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5.17.8 sysCNFGToPCI

NAME

sysCNFGToPCI() - convert PCICFGADR to PCI information

SYNOPSIS

```
STATUS sysCNFGToPCI
  (
  UINT  cnfgAddr,
  UINT  *busNum,
  UINT  *devNum,
  UINT  *funcNum
  )
```

DESCRIPTION

This function extracts the bus, device, and function number from a PCICFGADR register definition and returns it in <busNum>, <devNum>, and <funcNum>.

RETURNS

OK or **ERROR**

SEE ALSO

sysPCIConfigProbe, sysPCIConfigRead, sysPCIConfigWrite, sysPCIShow

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5.18 Other Utilities

The following utilities were recently added to the Board Support Package.

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5.18.1 sysDumpCNFGRegs()

NAME

sysDumpCNFGRegs() - Dumps the contents of a PCI device registers.

SYNOPSIS

```
void sysDumpCNFGRegs
  (
  UINT  cnfgAddr  /* Configuration address of PCI device */
  )
```

DESCRIPTION

Displays the contents of a PCI device configuration registers from 0x00 - 0x70* The configuration address of the device is given by <cnfgAddr> and should be an address type appropriate for use in PCI Type 0/1 configuration cycles. Values for <cnfgAddr> corresponding to PCI IDSEL lines are:

IDSEL 11 - 0x80000800

IDESL 12 - 0x80001000

IDSEL 13 - 0x80001800

IDSEL 14 - 0x80002000

IDSEL 15 - 0x80002800

For example, to display a PCI device at IDSEL 12 use :

sysDumpCNFGRegs(0x80001000)

RETURNS

N/A

SEE ALSO

sysLib, sysDumpMPCRegs(), sysDumpUniverseRegs()

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5.18.2 sysPeekPCI()

NAME

sysPeekPCI() - Reads an address on the PCI bus

SYNOPSIS

ULONG sysPeekPCI

(

ULONG address/* PCI address to probe */

)

DESCRIPTION

Reads a PCI address for a 32-bit value. This routine performs any possible byte swapping due to the endian difference between the CPU and PCI bus. This utility is contained in *sysLib.c*.

RETURNS

Value at the PCI address or ERROR if the address can’t be probed.

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5.18.3 sysPokePCI()

NAME

sysPokePCI() - Probe an address on the PCI bus

SYNOPSIS

ULONG sysPokePCI

(

ULONGaddress, /* PCI address to probe */

ULONGdata/* word to write */

)

DESCRIPTION

Writes a PCI address with a 32-bit value. This routine performs any possible byte swapping due to the endian difference between the CPU and PCI bus. This utility is contained in *sysLib.c*.

RETURNS

Value a the PCI address or **ERROR** if the address can't be probed.

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5.19 BSP Distribution

The contents of K2 distribution are shown below. There are some files contained in the distribution that are duplicates of the WindRiver versions. They are generally located under **target/src** or **target/h**. If a duplicate of these files already exists in the VxWorks development tree, do not overwrite them. Overwriting them, however, will not cause any ill effects if the originals were not modified from the standard WindRiver release.

Any driver files delivered in binary format are included in an additional library file, **powerk2Lib.a**. In particular, the serial driver (**pc87332Sio.o**), Ethernet drivers **fei82557.o** and **sysfei82557.o** (to support Ethernet on K2), are contained in the library and are configured to be linked automatically into a kernel built for K2. Serial device driver files are also provided in source format and are located in the directory **powerk2/sio**.

5.20 Installation

This page intentionally left blank.

This section describes the installation procedure for either a UNIX host or PC-based host running Windows 95, 98, 2000 and NT.

If K2's BSP is received on CD media then follow the WindRiver Products Installation Guide for Tornado 2.0. This installation is menu driven under either the Windows 95/NT environment or UNIX host X Windows environment. Included with the CD media is a BSP INSTALLATION KEY sheet which contains the necessary key to enter when prompted.

If the K2 BSP is delivered in **T**ape **AR**chive (**tar**) format via FTP site, it can be installed using the WindRiver utility *installOption*. Refer to the WindRiver documentation for instructions on how to use the install option.

With the updated BSP distribution, the user may also simply **tar** the BSP into the WindRiver tree or any other location. Any board dependent files or modules now have been moved exclusively to K2's BSP directory. The BSP is compatible on both Unix and Windows 95, 98, 2000 and NT platforms.

5.21 Technical Support

Please see Chapter 6, "Service," for RMAs and contact information.

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Chapter 6: Service

6.1 General

Use this chapter to request service or repair.

The following sections cover:

- Contact information for support, service and repair.
- Warranty Information.
- Return Material Authorization (RMA) forms
- Instructions for completing and returning the RMA

Please do not attempt to return the product for service until reviewing all supporting documentation, made every effort to resolve the issue and secured an RMA from our service deparent.

6.2 Acquiring Updated User Manuals and Data Sheets

6.2.1 Data Sheets

To view a current revision of the data sheet in Adobe Acrobat, see www.sbs.com. Adobe Acrobat Reader is available at no charge from www.adobe.com.

6.2.2 User Manuals, Electronic

To view a current revision of this manual in Adobe Acrobat, see www.sbs.com. Again, you may download Acrobat Reader at no charge from www.adobe.com or link from our page.

6.2.3 Manual Revisions, Hard Copy

To request a current hard copy of this manual, call 760-438-6900.

6.3 Contacting Customer Service

6.3.1 E-Mail

Please e-mail customer service at www.sbscomm.com

6.3.2 Toll Free

To call Customer Service, toll free, call 888-SBS-COMM.

6.3.3 Fax

To fax Customer Service, call 760-438-6904.

6.3.4 Mail

Customer Service Deparent
SBS Technologies, Inc.
Communications Products
5791 Van Allen Way
Carlsbad, CA 92008-7321

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6.4 Warranty Information

SBS Technologies, Inc. Communications Products provides a liberal three-year warranty, with specific stipulations concerning application and usage of the product. Please review the Warranty, below, before requesting service.

6.4.1 Warranty

SBS Technologies, Inc., Communications Products, hereinafter called The Company, warrants the product described in this documentation to be free from defects in workmanship and materials when used within the operating specifications set by The Company and in its original, unmodified condition, for a period of three years from its date of shipment. ANY MODIFICATION TO THE PRODUCT VOIDS THIS WARRANTY. An extended warranty may be available for specific product lines.

If the product is found to be defective within the terms of this warranty, The Company's sole responsibility shall be to repair, or at The Company's sole discretion, to replace the defective product. The product must be returned insured and shipped prepaid to The Company after obtaining a Return Material Authorization (RMA) from The Company. All replaced products become the sole property of the The Company.

This warranty is limited to the product described in this manual, and specifically excludes any ancillary products or equipment provided by third parties. The user should seek relief for third party products under any warranties issued by their respective manufacturers.

The Company assumes no liability under the terms of this warranty if repair is impossible due to structural damage to the product as a result of accident, abuse, or misapplication of the product.

The Company does not authorize the use of its components in (a) life support applications where failure or malfunction of the component may result in injury or death, or (b) nuclear control and process applications where failure or malfunction of the component may result in radioactive release, explosions, environmental damage/contamination, personal injury or death. Therefore, the user of The Company components in any and all life support applications or nuclear applications assumes all risk arising out of such use and further agrees to indemnify and hold The Company harmless against any and all claims of whatsoever kind or nature (including claims of culpable conduct [strict liability, negligence or breach of warranty] on the part of the The Company) and for all costs of defending any such claims.

The Company's warranty of, and liability for, defective products is limited to that set forth herein. The Company disclaims and excludes all other warranties and product liability, expressed or implied, including but not limited to any implied warranties of merchantability or fitness for a particular purpose or use, liability for negligence in manufacture or shipment of product, liability for injury to persons or property, or for any incidental, consequential, punitive or exemplary damages.

This limited warranty is in lieu of all other warranties expressed or implied. Faults caused by unauthorized modification or misuse of products are not covered by this warranty. The Company specifically disclaims the implied warranties of merchantability and fitness for a particular purpose.

The warranties provided herein are the buyer's sole and exclusive remedies. In no event shall The Company be liable for indirect, special, incidental, consequential or punitive damages (including but not limited to lost profits, penalties, or damages payable to third parties and damage to goodwill) suffered or incurred, whether based on contract, tort, or any other legal theory, even if The Company has been informed of the possibility of such damages.

This limitation of liability may not be enforceable in certain jurisdictions, therefore the above limitations may not apply. This warranty gives you specific rights. You may also have other rights that vary from jurisdiction to jurisdiction.

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6.5 Request for Return Material Authorization (RMA)

If you have a product that is not performing correctly, and you have exhausted the recommendations in this user's manual, please complete the "Request for Return Material Authorization" below.

After you have filled it out completely, send it to the SBS Technologies Service Deparent. You may make your request in one of three ways:

- Photocopy this page, fill out the form, and fax it to 760-438-6904.
- Complete the on-line version at our web site: www.sbs.com.

An RMA number will be issued upon receipt of this form.

Request for Return Material Form

Fax to:

760-438-6904

Figure 6-1, Request for Return Material Authorization (RMA)

Sales Order Number		E-mail Address	
Your Name		Date	
Your Company		Title (Optional)	
Address 1		Address 2	
City	State	Zip Code +4	Country
Phone Number (AC)		Alternate No. (AC)	
Fax Number (AC)		E-mail Address	

Item	Model No	Serial No	Reported Failure
1			
2			
3			
4			

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Request for Return Material Form

Fax to:

760-438-6904

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6.6 Documentation Feedback Form

You can help us provide you with better documents. Simply photocopy this page, print your comments, and fax or mail to:

Fax: 760-438-6904
SBS Technologies, Inc.
Communications Products
5791 Van Allen Way
Carlsbad, California 92008-7321

Figure 6-2, Document Feedback Form

Section	Key Information Needed	Technical Error	Please describe any errors on the appropriate line.
Cover Page			
Table of Contents			
List of Figures			
List of Tables			
How to Use			
Chapter 1			
Chapter 2			
Chapter 3			
Chapter 4			
Chapter 5			
Acronyms			
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