PCI-60A

Hex IndustryPack®
Carrier for the PCI Bus

User Manual

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PCI-60A
Hex IndustryPack®
Carrier Board For The
PCI Bus

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Product Description

The PCI-60A IndustryPack® carrier board provides six IndustryPack slots on a single desktop or industrial PCI slot card. The PCI-60A-8 provides an 8 MHz clock to all IndustryPack slots. The PCI-60A-8/32 provides a clock that is software-selectable on a per-slot basis and has an overall higher performance level.

The standard 8 MB memory space is available for each IndustryPack site. High-speed 32-bit PCI host address space permits desirable linear mapping and fixed address partitions of memory, I/O, and ID spaces for each IndustryPack module.

The PCI-60A uses a PLX PCI9080 controller as the PCI bus interface chip and Altera FPGA logic, which provides fully configurable PCI interrupt vector space. The PCI bus interface handles 3.3V and 5.0 V signaling levels.

Each IndustryPack site has an adjacent 50-pin I/O connector for exiting the host system through the PCI slot panel. One connector is accessible via the rear-panel. The standard connector allows most of SBS transition modules and terminal blocks to be used.

The PCI-60A meets the PCI specification and conforms to the VITA-4 IndustryPack Logic Interface Specification. This guarantees compatibility with a wide range of IndustryPacks. The PCI-60A is backward compatible with the PCI-40A.

Key Features

- Six IndustryPack slots on a single PCI slot board
- I/O via six 50-pin keyed, shrouded ribbon cable headers
- Switchable 8/32 MHz IndustryPack bus
- LEDs for CPU access and power monitor for each slot
- Filtered power rails and resettable fuses
- Interrupt acknowledge space for retrieving IndustryPack vectors
- Backwards-compatible with the PCI-40A
- Reduced memory-map version available by special order

Address Map

The PCI-60A is mapped into the PCI memory space. PCI I/O space is not used. IndustryPack I/O, ID, memory, and interrupt vector registers are mapped in the PCI memory space. Two address maps are supported: a standard memory map consuming 64 Mbytes of address space and a small memory map consuming 64 Kbytes. Size is an order option.

The PCI bus allocates only one interrupt line to the PCI-60A per the PCI 2.1 Specification. The PCI-60A, however, provides an interrupt status register that quickly identifies that IndustryPack slot generated the interrupt.

I/O Connections

The six IndustryPack positions are referred to as slots and identified by the letters A, B, C, D, E, and F. Five of the slots have upright 50-pin flat cable headers accessible through the rear panel of the PCI-60A for their I/O connections. The sixth slot has a right angle connector available directly from the rear panel. The I/O connectors are mounted directly on the PCI-60A board to provide a modular and reliable cabling system with inherent strain relief. I/O cables may be inserted or removed without removing the PCI-60A from the chassis. IndustryPacks in slots A and B may be installed or removed without interfering with the I/O cabling.

PCI-60A provides protected and filtered +5V, +12V, and -12V supplies to each IndustryPack by means of passive "T" filters, capacitors, and fuses. The three terminal filters provide excellent RF rejection of power supply conducted noise. This permits use of precision analog IndustryPacks together with high-speed digital IndustryPacks in the same PCI-60A. The fuses are self-resetting Positive Temperature Coefficient devices. The IndustryPack slots feature other power handling features such as separated ground planes to reduce conducted noise.

PCI-60A IndustryPack interface is compliant with the ANSI/VITA 4 IndustryPack Module Specification Revision 1.0. This guarantees compatibility with the wide range of IndustryPacks currently available and planned.

Figure 1 is a block diagram of the PCI-60A.

Block Diagram

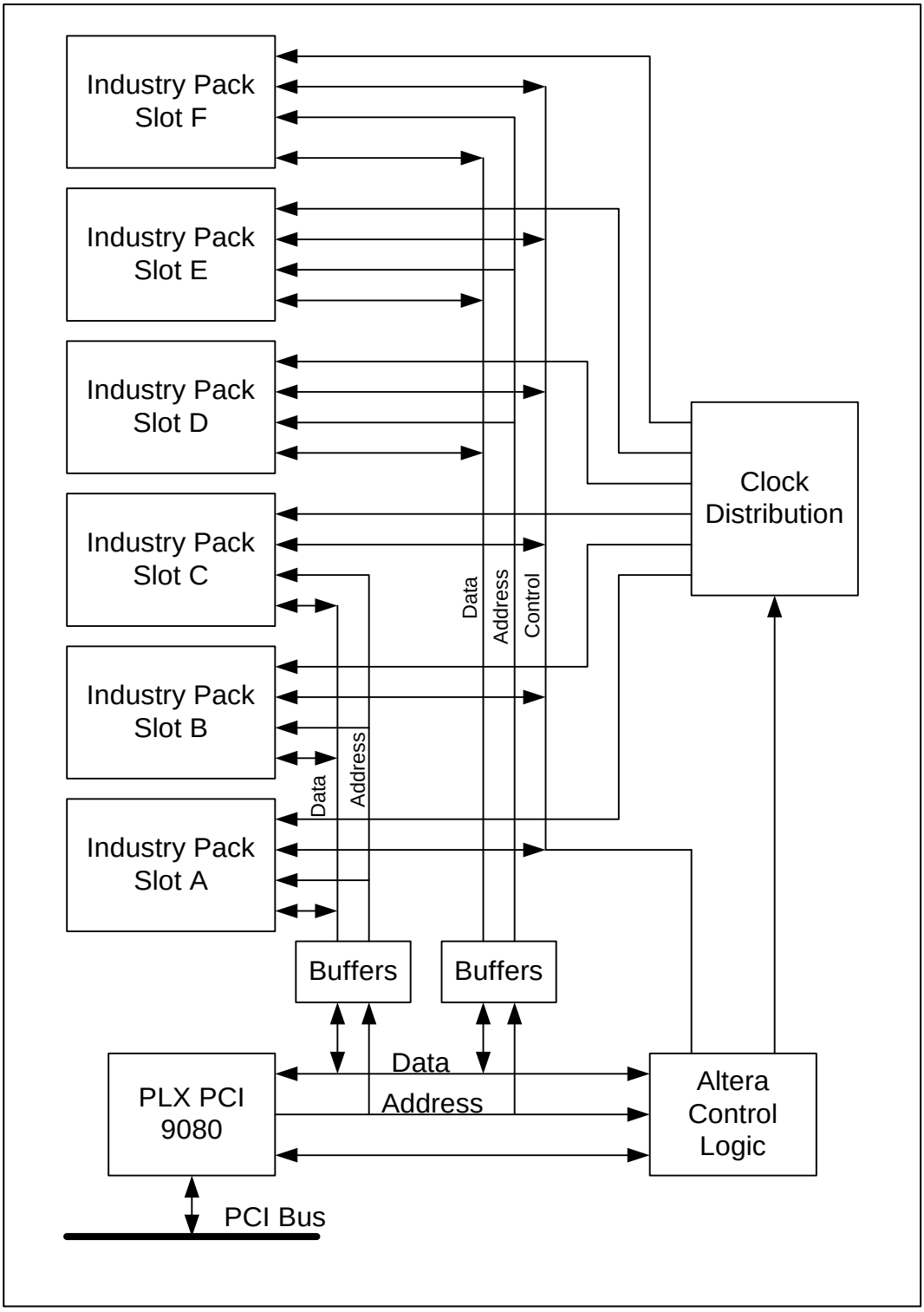

Figure 1. Block Diagram

PCI-60A Hardware Overview

Addressing Overview

IndustryPacks have four separate address spaces across the IndustryPack Logic interface: ID, I/O, memory, and (interrupt) vector. It is the job of the carrier board, the PCI-60A, to map these spaces into the host's address space. The PCI-60A maps all IndustryPack spaces into the PCI bus memory space.

The IndustryPack I/O, ID, and vector spaces are fixed in size. The IndustryPack memory size can vary up to 8 MB per IndustryPack. The PCI-60A supports two address maps: a standard map consuming 64 MB of memory space and a reduced map consuming 64 KB of memory space. Both memory maps provide the I/O, ID, and INT spaces for the six slots plus local register decoding. The reduced map provides an additional 2K of memory space per IndustryPack and the standard map provides an additional 8 MB per IndustryPack.

Selecting the PCI-60A Base Address

The PCI-60A base address and address map are selected through the PCI configuration registers. Unlike VME and ISA systems, the base addresses in PCI systems are set at run time by the BIOS. The BIOS uses PCI configuration cycles to query each slot on the PCI bus. Upon detecting a card, the BIOS writes all Fs to the Base Address Registers (BARs) and then reads them back. The card responds by placing 0s in all the address bits that it uses. The BIOS uses this information to determine how much memory the card is requesting, then assigns an address and writes it back to the BAR.

There are three base address registers for the PCI-60A. The first, BAR0, is the address of the PCI-9080 PCI accessible registers in PCI memory space. The second, BAR1, is the address of the PCI-9080 PCI accessible registers in PCI IO space. The third address, BAR2, is the address to use for accessing the IndustryPacks and PCI-60A Local Control registers in PCI memory space. The PCI-60A does not use the PCI-9080 BAR for local spaces. The addresses depicted in Figures 2 and 3 are relative to contents of BAR2. Please refer to the *Programming* section for more information.

Note that addresses within each IndustryPack's space are specific to that IndustryPack. Refer to each IndustryPack's User Manual for specific addressing information.

Address		**Name**
From	To	
0000 0500	0000 07FF	PCI-60A Local Control
0000 1000	0000 10FF	SlotA I/O
0000 1100	0000 11FF	SlotA ID
0000 1200	0000 12FF	SlotA INT
0000 2000	0000 20FF	SlotB I/O
0000 2100	0000 21FF	SlotB ID
0000 2200	0000 22FF	SlotB INT
0000 3000	0000 30FF	SlotC I/O
0000 3100	0000 31FF	SlotC ID
0000 3200	0000 32FF	SlotC INT
0000 4000	0000 40FF	SlotD I/O
0000 4100	0000 41FF	SlotD ID
0000 4200	0000 42FF	SlotD INT
0000 5000	0000 50FF	SlotE I/O
0000 5100	0000 51FF	SlotE ID
0000 5200	0000 52FF	SlotE INT
0000 6000	0000 60FF	SlotF I/O
0000 6100	0000 61FF	SlotF ID
0000 6200	0000 62FF	SlotF INT
0100 0000	017F FFFF	SlotA MEM
0180 0000	01FF FFFF	SlotB MEM
0200 0000	027F FFFF	SlotC MEM
0280 0000	02FF FFFF	SlotD MEM
0300 0000	037F FFFF	SlotE MEM
0380 0000	03FF FFFF	SlotF MEM

Figure 2. Standard Memory Map - 64 MB

Address		Name
From	To	
0000 0500	0000 07FF	PCI-60A Local Control
0000 5000	0000 57FF	SlotA MEM
0000 5800	0000 5FFF	SlotB MEM
0000 6000	0000 67FF	SlotC MEM
0000 6800	0000 6FFF	SlotD MEM
0000 7000	0000 77FF	SlotE MEM
0000 7800	0000 7FFF	SlotF MEM
0000 9000	0000 90FF	SlotA I/O
0000 9100	0000 91FF	SlotA ID
0000 9200	0000 92FF	SlotA INT
0000 A000	0000 A0FF	SlotB I/O
0000 A100	0000 A1FF	SlotB ID
0000 A200	0000 A2FF	SlotB INT
0000 B000	0000 B0FF	SlotC I/O
0000 B100	0000 B1FF	SlotC ID
0000 B200	0000 B2FF	SlotC INT
0000 C000	0000 C0FF	SlotD I/O
0000 C100	0000 C1FF	SlotD ID
0000 C200	0000 C2FF	SlotD INT
0000 D000	0000 D0FF	SlotE I/O
0000 D100	0000 D1FF	SlotE ID
0000 D200	0000 D2FF	SlotE INT
0000 E000	0000 E0FF	SlotF I/O
0000 E100	0000 E1FF	SlotF ID
0000 E200	0000 E2FF	SlotF INT

Figure 3. Reduced Memory Map - 64 KB

I/O Space

The I/O space on each IndustryPack is fixed at 128, 16-bit words (256 Bytes). (The I/O space above 64 words is for future use.) This occupies a space of $100 Bytes. The six IndustryPack I/O spaces are accessible at fixed offsets from the PCI-60A's Base Address, as shown in Figures 2 and 3. Typically, IndustryPacks do not fully decode their entire 64 long-word space. Some IndustryPacks support both word and byte accesses to I/O space, while others require accesses to be byte-only or word-only. See each IndustryPack's User Manual for details.

***Caution**: An IndustryPack may or may not fully decode its I/O space. Incomplete decoding will often cause IndustryPack registers to appear in multiple places within the 64-word I/O space. IndustryPacks may have different read and write maps. Some IndustryPacks require 16-bit accesses only. If an IndustryPack does not respond to an invalid access, then the PCI-60A bus timer will respond [if enabled] and cause an interrupt to alert the software.*

ID Space

Every IndustryPack must have an ID PROM. The ID space on each IndustryPack is fixed at 128, 16-bit words. *The ID space above 32 Bytes is for future use.* The ID PROM is required by the ANSI/VITA 4 IndustryPack Module Specification 1.0. The ID PROM data is at least 12 Bytes and is found in the lowest byte of the first 12 words. Newer IndustryPacks may support the ID PROM Data Format II that uses 16-bit words instead of 8-bit bytes. The ID PROM provides information about the IndustryPack, which is defined in the IndustryPack Specification and the IndustryPack's User Manual. This information includes the IndustryPack's manufacturer, model code, and manufacturing revision level. It may also include a driver identification code and calibration information.

The figure below lists the required information in each ID PROM. For additional information, see the IndustryPack Specification and the Users Manual for each IndustryPack.

$FF 2A	user space	
2*nn $18	pack specific space	
$16	CRC	
$14	No of bytes used	[= nn]
$12	Driver ID, high byte	
$10	Driver ID, low byte	
$0E	reserved	($00)
$0C	Revision	
$0A	Model No	
$08	Manufacturer ID	
$06	ASCII "C"	($43)
$04	ASCII "A"	($41)
$02	ASCII "P"	($50)
$00	ASCII "I"	($49)

Figure 4. Required IndustryPack ID PROM Information

Memory Space Accesses

The use of IndustryPack memory space is optional, and two sizes are available. Implementation among IndustryPacks varies widely. It may be used for RAM, EPROM, Flash, video frame buffers, communication data buffers, SRAM, local processor space, expanded register space, special functions, or a combination thereof. The memory is generally, but not always, 16-bits wide.

The PCI-60A supports two configurations of IndustryPack memory space. The standard map allocates the full 8 MB of space per IndustryPack. The reduced map configuration allocates a 2 KB partition for each of the six IndustryPacks. This is adequate to service many IndustryPacks that use the memory space as an alternate or expanded register space. It is not sufficient for some IndustryPack designs that implement real memory in

this space. Because this space is within the address decoding of the IndustryPack Memory space, the 2K block will appear at memory address 0 only for slot A. The other slots will be offset from 0 in 2K increments.

Interrupt Space

The PCI-60A maps all interrupt levels to the INTA# signal on the PCI back plane as required for single function devices by the PCI Specification 2.1. Because the PCI interrupts are shared, an interrupt can be from any slot on the back plane or from the motherboard itself. The interrupt service routine (ISR) must first check that the interrupt came from the PCI-60A by reading the CNTL2 register on the PCI-60A. If an IndustryPack is requesting the interrupt, the CNTL1 register can be read to determine which one. Each of the twelve IndustryPack interrupt lines (2 per IndustryPack) has a bit in this register. An interrupt will be generated whenever one of these bits is set and interrupts are enabled. It is up to the ISR to prioritize multiple interrupts if more than one bit is set. Each bit can be cleared only by clearing the interrupt source on the Industry Pack.

The interrupt space of each IndustryPack slot is directly accessible at any time. Typically, the ISR will access the INT space to determine the local cause of the interrupt. A read to the INT space will generate an IndustryPack Interrupt Cycle. During this cycle, the IndustryPack places its interrupt vector on the data lines. Some IndustryPacks may require this access to clear the interrupt. Check the IndustryPack's User Manual for specific details on clearing interrupts.

Please refer to the Control and Status register bit map section for more information.

IndustryPack Bus Time-Out

The PCI-60A has a programmable IndustryPack bus error timer. When enabled, the PCI-60A will time out if the IndustryPack being accessed does not respond. This allows the IndustryPack slots to be interrogated during start up to determine what IndustryPacks are installed in what slots. Without this feature, accessing an IndustryPack slot that does not respond will usually put the PCI bus in an infinite retry loop, essentially locking up the host processor.

When the Bus Error feature is enabled, the hardware will create a “bus reply” for an IndustryPack that does not respond within 3.2 µs. The hardware can also generate an interrupt to the host when the reply is from the timer instead of the IndustryPack. Interrupts may also be disabled and the bus error timer status may be polled. Three bits are used to control the way the bus error timer works. The AUTO_ACK bit in CNTL0 enables the bus error timer. When it is set to “1”, the bus error timer will generate an Ack* whenever an IndustryPack is accessed but does not respond. A status bit in CNTL2, AUTO_INT_SET, will be set if the CLR_AUTO bit in CNTL0 is set to “1”. Once set, the AUTO_ INT_SET bit will stay set until the CLR_AUTO bit is cleared to “0”. The AUTO_ INT_SET bit will generate an interrupt if the INT_EN bit in CNTL0 is set to “1” and the Local Interrupt Enable bit in the PCI 9080 Interrupt Control/Status Register is set to “1”. With the INT_EN bit cleared to “0”, the AUTO_ INT_SET bit may be polled.

The PCI 9080 always posts to its internal write FIFO before actually performing the write to the local bus side (i.e., the IndustryPack or CNTRL register). This leads to problems when a write causes a bus error on the local bus side and the AUTO_ACK feature is not enabled. The write appears to complete with no problems. However, the next access to the PCI-60A puts the PCI bus in an infinite retry loop as the PCI 9080 is still waiting for the previous access to complete. This effectively locks up the host computer.

Please refer to the *Bit Map* section for more information.

Status and Control Register Bit Maps

Three registers reside within the PCI-60A Local Control space as shown in Figures 2 and 3. The relative offsets and bit map definitions follow:

CNTL0: BAR2 offset 0x00000500 = Control Register 0 [CNTL0]

D15	D14	D13	D12	D11	D10	D9	D8
Unused	Unused	Unused	Unused	Unused	Unused	CLKF	CLKE

D7	D6	D5	D4	D3	D2	D1	D0
INTSET	INTEN	AUTO_ACK	CLR_AUTO	CLKD	CLKC	CLKB	CLKA

Bit	Definition
CLKA	0 = 8 MHz, 1 = 32 MHz for IP slot A
CLKB	0 = 8 MHz, 1 = 32 MHz for IP slot B
CLKC	0 = 8 MHz, 1 = 32 MHz for IP slot C
CLKD	0 = 8 MHz, 1 = 32 MHz for IP slot D
CLR_AUTO	0 = clear, 1 = enable AUTO_INT_SET bit in CNTL2
AUTO_ACK	0 = disable, 1 = enable bus error timer
INTEN	0 = disable interrupts, 1 = enable interrupts
INTSET	0 = turn off, 1 = force local interrupt [INTEN = 1]
CLKE	0 = 8 MHz, 1 = 32 MHz for IP slot E
CLKF	0 = 8 MHz, 1 = 32 MHz for IP slot F

Default value = 0x00. Word access and read-writeable.

CLK[A..F]
The CLKx bits control the clock rate for each IndustryPack. The clock to the slot is always at the frequency selected. The State Machine clock is altered to match the slot clock rate for each access automatically. A PLL is used to allow clean switching between frequencies without “glitching”. For the 8 MHz only version, these bits have no affect.

CLR_AUTO
The CLR_AUTO control bit is used to enable and clear the AUTO_INT_SET bit in CNTL2. The AUTO_INT_SET bit is held clear when this bit is “0”. Setting this bit to “1” removes the clear from the AUTO_INT_SET bit, allowing it to be set when the bus error timer expires and an Ack* is generated for an IndustryPack. Once the AUTO_INT_SET bit is set, a “0” must be written to the CLR_AUTO bit to clear the AUTO_INT_SET bit. The CLR_AUTO bit must be set back to “1” to re-enable the AUTO_INT_SET bit. The CLR_AUTO bit defaults to “0” on power-up or after a reset.

AUTO_ACK
The AUTO_ACK bit enables the auto acknowledge feature when set to “1”. When enabled, the PCI-60A creates a response to the PCI bus if an IndustryPack does not respond within 3.2 µsec or is not present. A response will be generated for valid IndustryPack addresses only. Clearing this bit to “0” will disable this function. If the CLR_AUTO, AUTO_ACK, and INTEN are all set to “1”, an interrupt will be generated if the software accesses a location that does not respond. The software must read CNTL2 and, if necessary, CNTL1 to determine the source of the interrupt. AUTO_ACK can be used with INTEN disabled and CLR_AUTO enabled by polling the status after each access. The power-up and reset default is “0”.

INTEN
INTEN enables interrupts from the PCI-60A onto the PCI bus when set to “1”. If cleared to "0", the interrupt remains pending but blocked from the PCI-9080. The PCI-9080 will cause INTA# of the PCI bus to be asserted if INTEN is enabled and an interrupt source is active. The PCI-9080 must also be set up to pass interrupts by having its Local Interrupt Enable bit and the PCI Interrupt Enable bit in the Interrupt Control/Status Register set to “1”s. Only the PCI Interrupt Enable bit defaults to “1” as set by the EEPROM. The power-up and reset default is “0”.

INTSET
The INTSET bit is used with INTEN to create an interrupt. The interrupt source is within the Altera control PLD. With INTEN enabled, setting INTSET to a “1” will generate an interrupt input to the PCI-9050. If interrupts from the local bus are enabled, the PCI bus INTA# will be activated. This is a useful feature for debugging.

CNTL1: BAR2 offset 0x00000600 = control register 1 [CNTL1]

Read

D15	D14	D13	D12	D11	D10	D9	D8
Unused	Unused	Unused	Unused	IRQF1	IRQF0	IRQE1	IRQE0

D7	D6	D5	D4	D3	D2	D1	D0
IRQD1	IRQD0	IRQC1	IRQC0	IRQB1	IRQB0	IRQA1	IRQA0

Bit	Definition [read only]
IRQA0	0 = no interrupt, 1 = interrupt pending
IRQA1	0 = no interrupt, 1 = interrupt pending
IRQB0	0 = no interrupt, 1 = interrupt pending
IRQB1	0 = no interrupt, 1 = interrupt pending
IRQC0	0 = no interrupt, 1 = interrupt pending
IRQC1	0 = no interrupt, 1 = interrupt pending
IRQD0	0 = no interrupt, 1 = interrupt pending
IRQD1	0 = no interrupt, 1 = interrupt pending
IRQE0	0 = no interrupt, 1 = interrupt pending
IRQE1	0 = no interrupt, 1 = interrupt pending
IRQF0	0 = no interrupt, 1 = interrupt pending
IRQF1	0 = no interrupt, 1 = interrupt pending

CNTL1 is read to determine the source of an interrupt request that originates from the IndustryPack Slots. If an interrupt request is processed by the host CPU originating from the PCI-60A, then the CPU should read it and CNTL2 to determine which interrupts are pending. If the IndustryPack requires access in the interrupt space, then a read/write operation can be performed via the Interrupt space (see memory map) to create an INT space access to the IndustryPack slot in question. A1 is set by the address within the space. Access an even word [a1 =0] for INT0 and an odd word for INT1.

CNTL2: BAR2 [read only] offset 0x00000700 = control register 2 [CNTL2]

D15	D14	D13	D12	D11	D10	D9	D8
Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused

D7	D6	D5	D4	D3	D2	D1	D0
LINT	Auto_Int_Set	unused	Unused	Unused	Unused	Unused	Unused

Bit	Definition [read only]
Auto_Int_Set	0 = no bus error time out, 1 = bus error interrupt pending
LINT	0 = no interrupt, 1 = interrupt pending to PLX

Auto_Int_Set
Auto_Int_Set indicates that a bus error has occurred and that Readyi# was asserted to prevent the system from hanging up. Please refer to CNTL0 for the Auto_Int_Set control bits.

LINT
LINT is an active high version of LINT# input to the PCI 9080 and indicates that PCI-60A is requesting an interrupt when read as "1".

IndustryPack Bus Pin Assignments

The six IndustryPack slots have the standard logic connector pinout as defined by VITA 4-1995 and shown below:

Pin	Signal
1	GND
2	CLK
3	Reset*
4	D0
5	D1
6	D2
7	D3
8	D4
9	D5
10	D6
11	D7
12	D8
13	D9
14	D10
15	D11
16	D12
17	D13
18	D14
19	D15
20	BS0*
21	BS1*
22	-12 V
23	+12 V
24	+5 V
25	GND

Pin	Signal
26	GND
27	+5 V
28	R/W*
29	IDSel*
30	DMAReq0*
31	MemSel*
32	DMAReq1*
33	IntSel*
34	DMAck*
35	IOSel*
36	[Reserved]
37	A1
38	DMAEnd*
39	A2
40	[Error*]
41	A3
42	IntReq0*
43	A4
44	IntReq1*
45	A5
46	Strobe*
47	A6
48	Ack*
49	[Reserved]
50	GND

Figure 5. IndustryPack Bus Pin Assignments

Signals shown within square brackets, such as [Reserved], are not connected on the PCI-60A. Signals shown within curly braces, such as {Strobe*}, are connected but not used. All signals except IDSel*, IntSel*, IOSel, MemSel*, IntReq0*, IntReq1*, and Ack* are bused.

IndustryPack I/O Pin Assignments

The six IndustryPack positions are referred to as slots and identified by the letters A, B, C, D, E, and F. Each slot's I/O connections are routed to a separate 50-pin IDC connector which allows the separate ribbon cables to be brought out through the rear panel. Refer to the *I/O Wiring* section for more information.

Power

The PCI-60A provides protected and filtered +5V, +12V, and -12V supplies to each IndustryPack by means of passive "T" filters, capacitors, and fuses. The three terminal filters provide excellent RF rejection of power supply conducted noise. This permits use of precision analog IndustryPacks together with high-speed digital IndustryPacks in the same PCI-60A. The IndustryPack slots feature other power handling features such as separated ground planes to reduce conducted noise. For more information, refer to the Fuse Chart depicted Figure 7 in the *Other Features* section of this manual.

Programming

This section outlines key aspects in programming IndustryPacks installed on the PCI-60A.

The PCI-60A is normally programmed to occupy space above one megabyte. DOS, including Microsoft's MS-DOS and IBM's PC-DOS, cannot access space above one megabyte. "32-bit" operating systems, such as Windows NT, OS-9000, and SCO Unix, can generally access space above one megabyte. Some operating systems may require an intermediate piece of software to gain access to the hardware.

The PCI-60A has a Vendor ID of 0x124B and a Device ID of 0x0040. It has a Subsytem Vendor ID of 0x124B and a Subsystem Device ID of 0. Before use, the PCI-60A must have its Base Address set by the system. This is done via the PCI configuration registers. All accesses to the IndustryPacks on the PCI-60A are then relative to the Base Address. In general, computing an exact address of a register within an IndustryPack requires the addition of three numbers: the PCI-60A Base Address, the Offset of the IndustryPack's appropriate I/O space, and the Register Offset within the IndustryPack. Generally, C structures and C header files are used to perform these additions implicitly. The Offset of the IndustryPack's I/O space is shown in Figure 2 in the *Addressing* section of this manual. The Register Offset is specific to each IndustryPack and is listed in its User Manual.

The base address is determined during start-up by the PCI BIOS. Each device on the PCI bus is interrogated during start-up. The BIOS writes out all ones to the BAR, then reads it back. The card responds with zeroes in all the address bits it decodes. From this, the BIOS determines how much space the device is requesting and assigns it a base address. It then writes this address back to the BAR.

The PCI 9080 used on the PCI-60A for a PCI interface has registers that are tested by the PCI BIOS during initialization. Based upon the results, two memory spaces and one I/O space are allocated to the PCI-60A. The first memory space is contained in BAR0 and is the address of the PCI-9080 PCI accessible registers referred to as the Local Configuration Registers, Runtime Registers, and Messaging Queue Registers in the PCI 9080 Datasheet. The second memory space is contained in BAR2 and is the address to use for accessing the IndustryPacks and PCI-60 as Local Control registers. This is referred to as the Local Address Space 0 in the PCI-9080 Datasheet. The I/O space for the PCI 9080 accessible registers is contained in BAR1. Programming of the PCI 9080 registers from the IO space is not recommended. The PCI-60A does not use the PCI-9080 BAR3 for Local Address Space 0.

The following figure shows a map of the PCI Configuration Registers. Refer to the PCI 2.1 specification and the PLX PCI 9080 Data Sheet for definitions of these registers.

PCI CFG Register Address	To ensure software compatibility with other versions of PCI 9080 family and to ensure compatibility with future enhancements, write 0 to all unused bits.				PCI Writeable	Written by Serial EEPROM
	31 24	23 16	15 8	7 0		
0x00	Device ID		Vendor ID		N	Y
0x04	Status			Command	Y	N
0x 08	Class Code	Revision ID	Local	Y	Y[15:0]	N
0x 0C	BIST	Header Type	PCI Latency Timer	Cache Line Size	Y	N
0x 10	PCI Base Address 0 for Memory Mapped Configuration Registers (BAR0)				Y	N
0x 14	PCI Base Address 1 for I/O Mapped Configuration Registers (BAR1)				Y	N
0x 18	PCI Base Address 2 for Local Address Space 0 (BAR2)				Y	N
0x 1C	PCI Base Address 3 for Local Address Space 1 (BAR3)				Y	N
0x 20	Unused Base Address (BAR4)				N	N
0x 24	Unused Base Address (BAR5)				N	N
0x 28	Cardbus CIS Pointer (Not Supported)				N	N
0x 2C	Subsystem ID Subsystem Vendor ID				N	Y
0x 30	PCI Base Address for Local Expansion ROM				Y	N
0x 34	Reserved				N	N
0x 38	Reserved				N	N
0x 3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	Y [7:0]	Y

Figure 6. PCI Configuration Registers

Programming the PCI 9080 Registers

At power on, or after a PCI bus reset, the PCI 9080 reads a serial EEPROM to determine what responses to give to the BIOS. The EEPROM must be programmed to indicate whether the PCI-60A is an interrupt generator, how much memory should be allocated, and re-mapping of the memory, etc. The following sections describe some of the modes that may be applicable to IndustryPacks. Please refer to the PCI 9080 Data Sheet for a complete description of the registers.

PCI 2.1 Mode

The PCI-9080 chip has two modes of operation, one in which it will hold onto the PCI bus during the entire IndustryPack read access and one in which it will issue an immediate retry on the PCI bus and continue issuing retries until the IndustryPack has responded. This second mode is compliant with the PCI 2.1 specification that requires all targets to respond within sixteen PCI clock cycles. It is the factory default and, for a 33 MHz PCI bus, it is equivalent to 485 ns. It is not possible for the PCI-60A to respond within this time, even with a zero wait state 32 MHz IndustryPack. This mode may slow overall access to the IndustryPack as the master gives up ownership of the bus when it receives the retry and must arbitrate to get it back. In lightly loaded systems, or systems where the

host is the only bus master, performance should not be affected. The 2.1 compliant mode only affects read cycles, as writes are always posted to the PCI-9080's internal write FIFO. The PCI-9080 terminates the PCI bus write cycle, then writes the data out to the local bus.

When not in the 2.1 compliant mode, the PCI-9080 uses a retry delay timer that issues a retry when the timer expires. The factory default setting for the timer is the maximum allowed 128 PCI clock cycles, which is 3.8 µsec for a 33 MHz PCI bus. An IndustryPack must respond within 3.5 µsecs to keep the timer from expiring, taking into account the overhead to translate the access to the IndustryPack bus. Some IndustryPacks may not be able to meet this requirement, particularly those IndustryPacks that read serial EEPROMs. IndustryPacks that have processors with which the IndustryPack control hardware must arbitrate to gain access to the local bus may also have problems meeting this response time. This should not be a problem if it happens infrequently. However, other cards on the PCI bus may suffer due to the loss of PCI bandwidth while the PCI-60A holds onto the bus.

The PCI 2.1 compliant mode is set with bits 24 and 26 in the Mode/Arbitration Register of the PCI 9080 chip. It gets loaded from the configuration EEPROM, but may be changed at run time. See the PLX PCI-9080 data sheet and the EEPROM Programming section for more information.

Read Ahead Mode

The PCI 9080 can operate in a read ahead mode, where it will prefetch the data from the next address on the IndustryPack. On subsequent reads, the data will be read from the PCI 9080's internal FIFO rather than from the IndustryPack. This is incompatible with most IndustryPacks. The default setting is to leave this mode disabled. The bit controlling this feature is the Memory Space 0 Prefetch Disable bit [8] in the Local Address Space 0/Expansion ROM Bus Region Descriptor Register. The Read Prefetch Count Enable bit [10] in the same register must be set to a “1” to disable the prefetch mode. Refer to the PCI 9080 Data Sheet for more information.

Interrupts

The PCI-60A maps all 12 of the IndustryPack interrupts as well as its internal interrupts into the Local Interrupt In pin on the PCI 9080. These are routed in the PCI 9080 to the PCI bus INTA line, per the PCI 2.1 specification for single function devices. To enable interrupts, the INTEN bit, the CNTL0 Bit[6], and both the PCI Interrupt Enable Bit[8] and the PCI Local Interrupt Enable Bit[11] in the PCI 9080 Interrupt Control/Status must be set to one. The PLX Interrupt Control/Status register is located at an offset of 0x68 from the address held in the BAR0. The following is an example of the steps and values to enable the IndustryPacks to interrupt the host CPU.

- Set CNTL0 to 0x007X. This value enables interrupts from the IndustryPacks to reach the PCI 9080, enables bus timeout on an access to an empty IndustryPack slot, and enables the bus timeout interrupt to reach the PCI 9080. The X value should be set to the proper clock speed bits for each IndustryPack slot. CNTL0 is relative to BAR2.
- Set PCI 9080 Interrupt Control/Status Register (INTCSR) to 0x000D0900. This value enables interrupts from the IndustryPacks or the bus timeout to reach the host CPU. INTCSR is relative to BAR0.

All IndustryPacks capable of generating interrupts must also supply an Interrupt Vector during an interrupt acknowledge (IACK) cycle. Since the PCI bus does not have an inherent IACK cycle, the PCI-60A has a separate address space for each IndustryPack that will create an IACK cycle when read. Reading from offset address 0x0 in the Interrupt Space will read the IntReq0* Interrupt Vector. Address 0x2 will read the

IntReq1* Interrupt Vector. The vector will normally be read inside the Interrupt Service Routine. The vector does not have to be read if the IndustryPack does nothing more with an IACK cycle than output the vector. Although this is the case with most IndustryPacks, please verify for each IndustryPack by referring to its documentation. Some IndustryPacks require the vector to be read to clear the interrupt.

Write Posting

The PLX PCI 9080 chip always posts writes to its internal write FIFO regardless of how the PCI 2.1 compliant bit in the Mode/Arbitration Register is set. This keeps the PCI bus access at a minimum, usually taking five PCI clocks, but can cause problems on the PCI-60A if the software is not aware of this feature. A problem can occur when a write is made to an IndustryPack that does not respond or is not present. The PCI bus transaction will complete normally. However, the local bus side of the PCI 9080 will get hung up waiting for the IndustryPack to respond. The next access to the PCI-60A will then put the PCI bus in an infinite retry loop when the PCI 9080 issues a retry for the new access while it waits for the previous access to complete. The easiest way around this problem is to use the Auto Acknowledge feature, which will automatically complete the local bus cycle if the IndustryPack does not respond within 3.2 µsecs. See the *IndustryPack Bus Time-Out* and *Status and Control Register Bit Map* sections of this manual.

Other Features

LED Indicators

There are six green LED indicators on the top long edge of the PCI-60A. These are labeled ACK A, ACK B, ACK C, ACK D, ACK E, and LED F. Each time an IndustryPack is successfully accessed, the corresponding LED will turn on for one third of a second. Accesses more frequent than three times a second will appear as a continuously illuminated indicator.

The LEDs respond to I/O, ID, memory, and interrupt vector ID accesses. The following figure lists the LEDs and their colors and functions.

LED	Color	Function
LED A	green	IP A accessed
LED B	green	IP B accessed
LED C	green	IP C accessed
LED D	green	IP D accessed
LED E	green	IP E accessed
LED F	green	IP F accessed
PWR A	amber	Slot A +12, -12, +5 volt supply OK
PWR B	amber	Slot B +12, -12, +5 volt supply OK
PWR C	amber	Slot C +12, -12, +5 volt supply OK
PWR D	amber	Slot D +12, -12, +5 volt supply OK
PWR E	amber	Slot E +12, -12, +5 volt supply OK
PWR F	amber	Slot F +12, -12, +5 volt supply OK

Figure 7. LED Chart

The LEDs are driven by the acknowledge signal from the IndustryPacks. Thus, if the host software attempts to access an IndustryPack, but selects an unused location to which the IndustryPack does not respond, or a location that is empty, the indicator LED will not flash. The indicators do not show that the PCI-60A is being selected, but rather that the associated IndustryPack has completed an access. Similarly, the indicator LEDs do not show interrupts pending, but do show interrupt vector ID read cycles.

There are six amber LED indicators, one per IndustryPack slot, located on the top edge of the PCI-60A between IndustryPack slots C and D. These are connected to power monitoring circuits that will turn the LED on when the +5, +12, and -12V supplies are all present for that slot. These can be used to determine when a fuse has turned off.

Fuses

Caution: PCI-60A *has self-resetting fuses added on the power inputs to all IndustryPack positions. This is consistent with safety-related requirements of some organizations. Current limitations imposed by these fuses are shown below:*

Supply	Applies To	Current	Fuse[A,B,C,D,E,F]
+5V	Per IP	2.5 A @ 20˚C, 1.25 A @ 70˚C	F3,4,7,10,13,16
+12V	Per IP	2 A @ 20˚C, 1.0 A @ 70˚C	F1,5,9,12,15,18
–12V	Per IP	2 A @ 20˚C, 1.0 A @ 70˚C	F2,6,8,11,14,17

Figure 8. Fuse Chart

The PCI-60A uses Raychem PolySwitch® Resettable Fuses. These fuses are positive temperature coefficient resistors that rapidly increase resistance in response to excessive currents. If the current rises above the rated current, the device's resistance abruptly rises, effectively turning off the power to the IndustryPack. Once the fault condition is removed, the switch cools and returns to its normal resistance, typically 0.05 Ohms.

Installation of IndustryPacks

IndustryPacks are installed on the PCI-60A carrier board by simply snapping them into place. Press the IndustryPack and the carrier board together with your fingers until the two pairs of mating connectors are flush. The connectors are keyed, so the IndustryPack can only be installed correctly. Proper anti-static handling procedures should be followed.

There are six locations for IndustryPacks. These are identified as Industry Pack A – F on the silk screen.

IndustryPacks A, B, C, D, and E mate with straight 50-pin flat cable receptacle connectors for their I/O. Pin 1 for each connector is identified on the silkscreen. Slot F has a 50-pin right angle flat cable receptacle mounted through the rear panel. Route the cables for IndustryPacks A, B, C, D, and E through the rear panel over the IndustryPack slot F connector.

Many connector manufacturers are able to provide suitable receptacles. The following are recommended:

AdamTech	SC-50-B-A
Robinson Nugent	IDS-C50NPK-SR-TG

The following are recommended 50-pin IndustryPack connectors:

AMP	173279-3	Plug (situated on an IndustryPack)
AMP	173280-3	Header (situated on a carrier board)

Cables are available from SBS.

After an IndustryPack has been installed, four stainless steel screws may be used to secure the IndustryPack to the carrier board. This is normally necessary only in high vibration or shock environments. Insert the screw through the IndustryPack and the two connectors. Attach the nut on the solder side of the PCI-60A. Tighten using small tools, taking care to damage neither the IndustryPack nor the support board. The screws used are standard (metric) M2 x 18 stainless slotted flat heads. Screws and nuts are supplied with each IndustryPack.

User I/O Wiring

Each of the 50 pins on each I/O connector for the six IndustryPack slots (A, B, C, D, E, and F) connects to an identically numbered pin on the six corresponding flat cable connectors on the PCI-60A. The IndustryPack I/O connector, the PCI-60A flat cable connectors, and the wires on the ribbon cables are all numbered identically from 1 to 50. Each connector is labeled as IndustryPack Slot A Connector, IndustryPack Slot B Connector, IndustryPack Slot C Connector, IndustryPack Slot D Connector, IndustryPack Slot E Connector, and IndustryPack Slot F Connector on the silkscreen.

Pin 1 on IndustryPack and PCI-60A connectors is marked with a square pad, observable from the solder side of the respective board. Pin 1 is also shown on the silkscreen for each connector.

Caution: *This pin numbering system is not maintained with many mass-terminated connectors. Each type of connector has its own intrinsic pin numbering system. Systems integrators or users making their own cables must be certain which pin corresponds to which signal.*

The pin assignment of the IndustryPack I/O connector is fixed by the connector manufacturer and repeated in the IndustryPack Specification. This assignment is shown in the figure below:

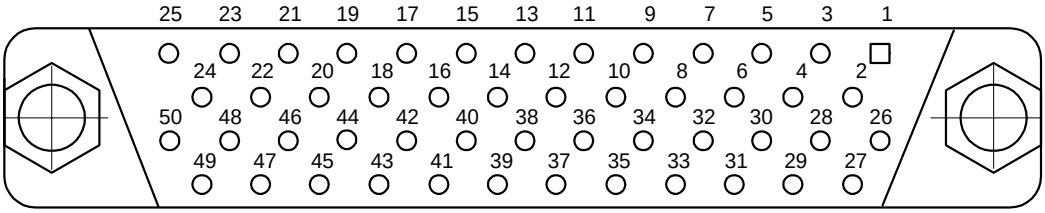

Figure 9. IndustryPack Connector Pin Numbering

Viewed from solder side of PCI-60A

The PCI-60A carrier board connects the mating I/O connector pins to a 50-pin flat cable connector. All pins from the IndustryPack go to identically numbered pins on these connectors. The pin numbering assignment of the four 50-pin front panel connectors is shown in the figure below. The wires in ribbon cables themselves are numbered sequentially across the flat cable starting with a red stripe on pin 1.

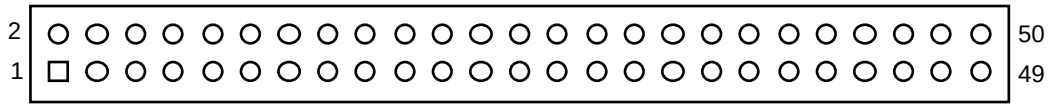

Figure 10. Flat Cable Connector Pin Numbering

Viewed from component side of PCI-60A

SBS Technologies offers cables and terminal blocks.

Interfacing to the outside world - the I/O cabling - remains the responsibility of the system integrator or end-user/engineer.

User Options

The PCI-60A uses a switch for controlling the EEPROM configuration. Settings are described below.

Switch SW1

Position 1 EESEL
Selects the size of the EEPROM. OFF selects the 1K 93CS46 and ON selects the 2K 93CS56 part. Leave in the ON position (factory default).

Position 2 SHORT
The SHORT switch is used by the PCI 9080 to determine the size of the EEPROM. When in the ON position, the PCI 9080 will only read the first five configuration registers and will not request any space for the PCI-60A IndustryPacks. When in the OFF position (factory default), all configuration registers will be read.

Position 3 EEPROM Data Out
This switch connects the EEPROM Data Out pin to the PCI 9080 device. When in the OFF position, the PCI 9080 will power up with its factory defaults. It will not request any space for the IndustryPacks during the PCI BIOS configuration process. When in the ON position (factory default), the PCI 9080 device will read the EEPROM after power up and use that information during the PCI BIOS configuration.

Position 4 EEPROM PE
The EEPROM PE switch and the EEPROM PRE switch are used to enable programming of the EEPROM. When in the OFF position, the EEPROM Program Enable (PE) pin is pulled to VCC by a 4.7K Ohm resistor. This allows programming of the EEPROM. When in the ON position (factory default), the PE pin is tied to GND. This prevents any programming of the EEPROM.

Position 5 EEPROM PRE
The EEPROM PRE switch and the EEPROM PE switch are used to enable programming of the EEPROM. When in the OFF position, the EEPROM Protect Register Enable (PRE) pin is pulled to VCC by a 4.7K Ohm resistor. This allows programming of the EEPROM protect register. When in the ON position (factory default), the PRE switch connects the pin to GND. This enables programming of the EEPROM data area and prevents programming of the protect register.

Positions 6,7,8 NOT USED

E1 - IndustryPack Strobe

Each IndustryPack has one pin on the logic interface labeled "Strobe." This pin may be used for a digital strobe or clock signal related to the IndustryPacks functionality. On the PCI-60A, this pin from each of the six IndustryPack slots is connected to one of the pins on the E1 shunt. Wires may be added to connect combinations of the IndustryPack Strobe lines together. The factory default is to leave all these pins unconnected. The following table lists the connections.

Pin	IP Slot
1	Slot F
2	Slot E
3	Slot D
4	Slot C
5	Slot B
6	Slot A

Construction and Reliability

IndustryPacks and their carriers were conceived and engineered for rugged industrial environments. The PCI-60A is constructed out of 0.062-inch thick FR4 material. The six copper layers consist of a power plane, ground plane, and four signal planes. The power planes significantly reduce conducted and emitted RF noise. They also assist in heat dissipation. Solder mask covers exposed traces on both sides.

Components are a mix of surface-mount and through-hole. Programmable ICs are socketed in low profile gold-plated screw-machine pin sockets. High insertion and removal forces are required, which assists in keeping components in place. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the four corner pins of each socketed component into the socket. The factory can build socket-free boards, as well as extended temperature range boards, on special order.

The IndustryPack connectors are keyed, shrouded and gold-plated on both contacts and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IndustryPack is optionally secured to the carrier board with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IndustryPack. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications, they are not required.

IndustryPacks provide a low temperature coefficient of 0.89 W/°C for uniform heat. This is based on the temperature coefficient of the base FR4 material of .31 W/m-°C, and taking into account the thickness and area of standard IndustryPacks. This coefficient means that if 0.89 Watts is applied uniformly on the component side, the temperature difference between the component and the solder side would be one degree Celsius.

Most of the components on the PCI-60A are CMOS. Many IndustryPacks are also primarily CMOS. Nonetheless, adequate cooling of the host system is strongly recommended.

The PCI-60A features independent three-terminal pi filters on all power lines to the IndustryPacks. This aggressive filtering of high frequency noise allows precision analog and high-speed digital IndustryPacks to be mixed in the same slot. The power line filters both block digital noise from elsewhere in the host system from entering an IndustryPack, and also block noise generated from an IndustryPack from entering the host system.

Specifications

Form Factor	PCI non-standard length
PCI	PCI Specification, Revision 2.1
PCI Controller	PLX 9080
Number of IndustryPack Slots	Six Supports up to three double-wide IndustryPacks
IndustryPack Bus Clock	Switchable 8/32 MHz per IndustryPack slot
IndustryPack Features Supported	I/O space, ID space, memory space, interrupt acknowledge cycles
IndustryPack Memory Size	8 Mbytes per IndustryPack*
Carrier Board Memory Space	64 Mbytes*
IndustryPack Interrupts Supported	Int0* and Int1* for each slot
PCI Bus Interrupts Generated	INTA# only
I/O Access	One 50-pin 0.1” ribbon cable header per IndustryPack slot One connector is rear-panel accessible
Indicators	One green LED for CPU access and one amber LED for power monitor per IndustryPack slot
Fuses	Resettable 2.5A @ 20º C for 5 VDC Resettable 2.0A @ 20º C for +/-12 VDC
Dimensions	4.2” x 13.35” (106.7 mm x 339.1 mm) ISA full-length card
Weight	0.24 kg (0.56 lb)
Power Requirements	+5V VDC, 150 mA typ +12 V DC, 10 mA typ –12 V DC, 10 mA typ Extra power required for IndustryPack modules
Environmental	Operating temperature: 0° to +70° C Humidity: 5% to 95% non-condensing Storage: –40° to +85° C

*A reduced memory map version of the PCI-60A is available by special order. Contact sales for more information.

Appendix A - DOS Extenders

DOS is not recommended with the PCI-60A because its native address space is limited to 1 MByte. Although the PCI-60A can be located within this 1 MByte address space, this configuration has not been tested and is not recommended. The PCI-60A is normally located above the 1 MByte boundary that DOS cannot directly access. If your application requires a DOS environment, then both a DOS Extender and a PC/AT platform with an Intel 386SX/DX, 486SX/DX, or higher processor are required.

A DOS Extender allows a user to access memory beyond the 1 MByte (extended memory) limit of DOS by running any application in the 16-bit protected mode of the Intel 80386, 486, or Pentium microprocessor. With a DOS Extender, an application can directly access up to 16 Mbytes of memory in a PC/AT system running under DOS.

A user may access the extended memory with DOS 5.0 or 6.0 specific utility calls. Implementation of these utilities is beyond the scope of this user manual.

The user may contact the following DOS Extender vendors for any DOS Extender questions and literature:

PHAR LAP SOFTWARE, INC.
60 Aberdeen Avenue
Cambridge, MA 02138
Tel: (617) 661-1510

TENBERRY SOFTWARE, INC. (formerly RATIONAL SYSTEMS, INC.)
P.O. Box 20050
Fountain Hills, AZ 85269-0050
Tel: (480) 767-8868

ERGO COMPUTING, INC.
One Intercontinental Way
Peabody, MA 01960
Tel: (800) 633-1925

Repair

Service Policy

Before returning a product for repair, verify as soon as possible that the suspected unit is at fault; then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if it is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include the return address and telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. SBS Technologies will not be responsible for damages due to improper packaging of returned items. For service of SBS Technologies products not purchased directly from SBS Technologies, contact your reseller. Products returned to SBS Technologies for repair by other than the original customer will be treated as out-of-warranty.

For service, contact:

SBS Technologies, Inc.
1284 Corporate Center Drive
St. Paul, MN 55121-1245
Tel: (651) 905-4700
FAX: (651) 905-4701
Email: support.commercial@sbs.com