Power7E

Technical Manual

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Power7E

PowerPC VMEbus Single Board Computer

Technical Manual

Power7E Technical Manual
Document Number **A-945-MN-04548-01**
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Revision 01

This manual applies to the Power7E Single Board Computer, revision 00 and above, until superceded.

Revision Date	By	Comments
08-27-2001	jev	Current Preliminary Manual
09-24-2001	jev	Updated CPU speed from 500MHz to 533MHz
11-01-2001	jev	Assorted corrections, typos and updates.
02-21-2002	jev	Appendix is updated to account for 3-Row P2 connector.
05-02-2002	jev	Update Specs., and typo corrections.
08-29-2002	jev	Add JTAG/COP to drawing on Page 1-1and Table on Page 2-13.

This manual uses some generally accepted conventions for clarity and accuracy. These include:

- The use of an ‘H’ suffix to a number indicates hexadecimal (base sixteen) notation.
- The use of a ‘-’ (minus) suffix to a signal name indicates an active low signal. The signal is either true when it is at a logic zero level or the signal initiates actions on a high-to-low transition.
- Text in `Courier` Font indicates a command entry or output from an SBS Technologies PC product using its built-in character set.

Contents

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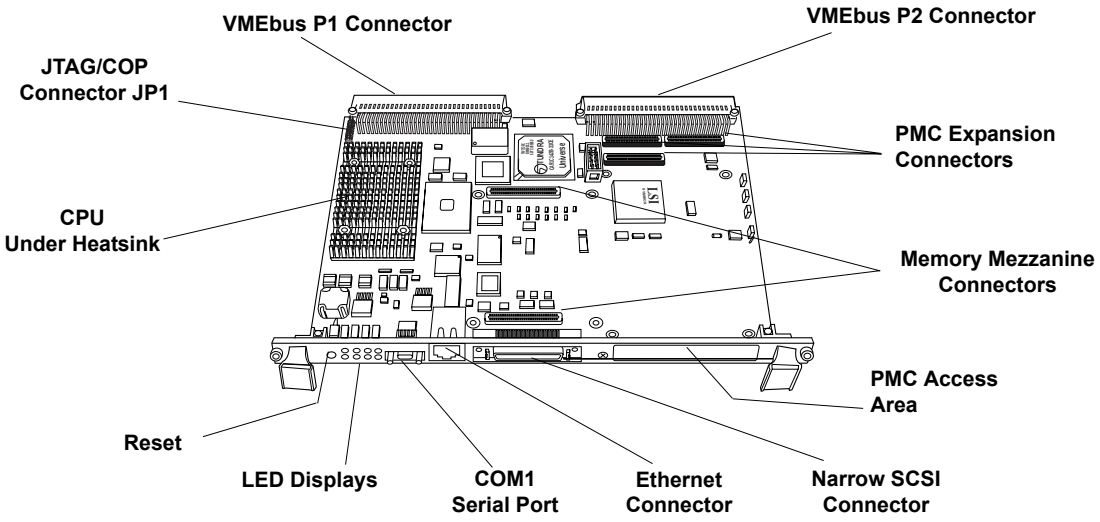
CHAPTER 1 Introduction



Overview

The Power7E is a high performance, 6U VME64 single board computer designed for use in a wide variety of computing applications. It provides everything a user could want in a basic computer including a fast CPU, a large amount of fast SDRAM memory with ECC, a large amount of non-volatile storage and a Fast Ethernet interface. The Power7E does all this in a single slot.

The Power 7E is designed to use the IBM PPC750 CPU. The PowerPC 750 SYSCLK is driven at 66 MHz. A JTAG emulator port is provided by a keyed 2 x 8 header on the PC board.

The Boot ROM socket (U18) provides 512k bytes of flash memory organized as 512k x 8. The socket is a 32-pin PLCC socket.

Features

Key features of the Power7E are:

• IBM PowerPC 750 running at up to 500 MHz

• 1M Byte of level 2 cache running at up to 250 MHz

• 66 MHz system bus

• 64M – 512 MBytes of SDRAM with ECC at 66 MHz
(On board memory up to 256MB, mezzanine memory up to 256MB)

• IBM CPC700 PCI-Bridge/Local Bus/Memory Controller

• Tundra Universe-IIB PCI/VME Bridge

• 512k Byte socketed boot flash memory

• 16MB on-board Strataflash

• A 53C875 providing an Ultra-SCSI port on the P2 Connector & Front Panel

• 10/100BaseTX Ethernet

• Two 16550 compatible UARTs with RS-232 interface supporting up to 115k baud. COM1 on front panel, COM2 rear panel I/O thru P2.

• 32K bytes NVRAM

• Y2K compliant real time clock/calendar

• Watchdog timer supporting interrupt or board/chassis reset

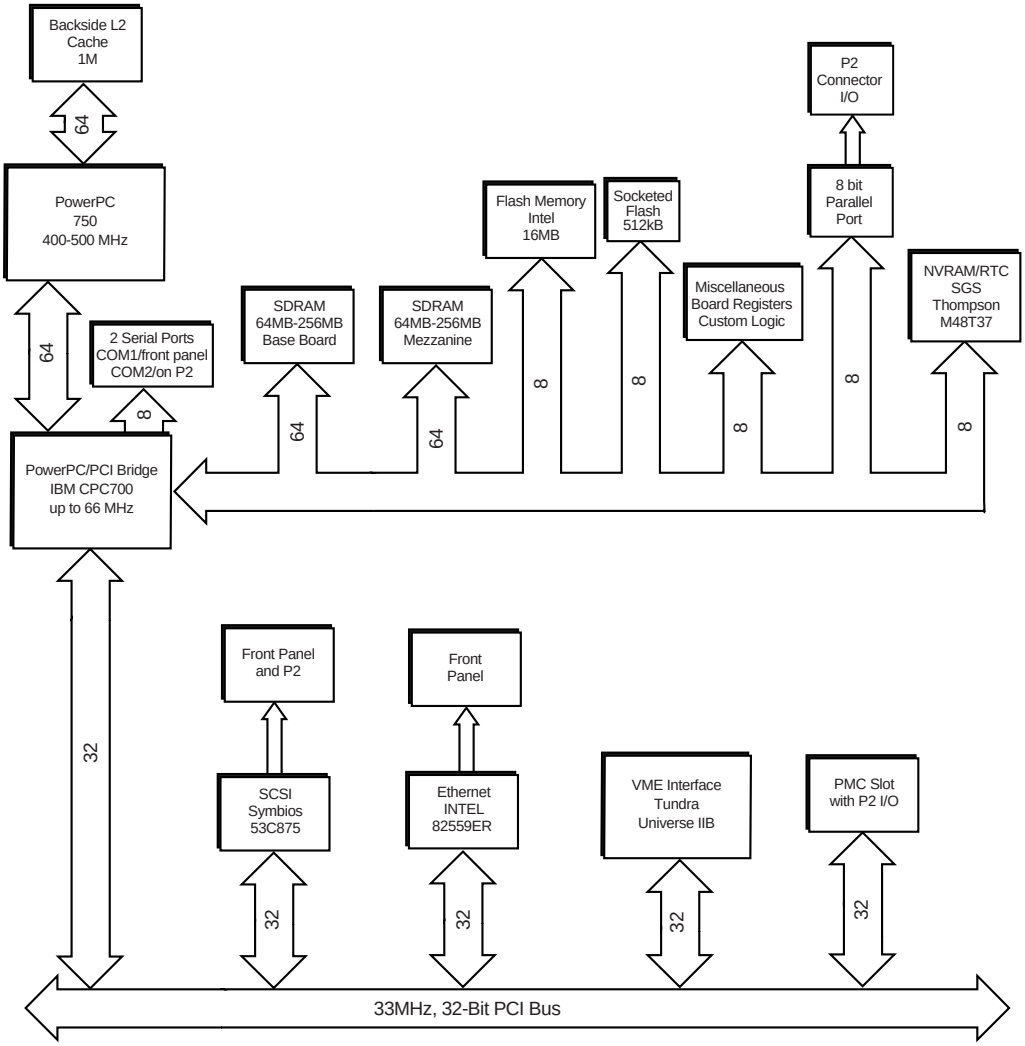
• Occupies a single 6U VME slot

• A PMC expansion slot with PMC I/O routed to the VMEbus backplane connector P2

CHAPTER 2 Detailed Description by Device

Block Diagram

This section describes the Power7E by looking at the individual hardware devices used on the board. A block diagram of the Power7E is shown below:



CPU - IBM PowerPC 750

The Power7e is designed for a PowerPC 750 at 400-500MHz. PowerPC 750 SYSCLOCK is driven at 66MHz. A range of SYSCLK to CPU core speed multipliers is supported as follows:

PLL Bit	Resistor	6x 400MHz	7.5x 500MHz
0	R120	1	0
1	R119	1	0
2	R118	0	0
3	R117	1	1

JTAG Port

A JTAG Emulator port is provided by a keyed 2 x 8 header on the board. JTAG (Joint Test Action Group, IEEE Standard 1149.1) protocol contains commands to read/set the values of the pins (and internal registers) of devices. JTAG facilitates board testing, as signals not visible at the board connector may be read and set. The PLL_CFG bits can be read in the HID1 register in the PPC 750.

For additional information on the PPC750, refer to the MPC750 RISC Microprocessor User's Manual, Motorola, Inc. - Document Number MPC750UM/AD.

Level 2 Cache

The PPC 750 includes an integrated L2 cache controller with TAG RAM with 1M Byte of L2 cache. On the Power7E, two Motorola MCM69R737 devices, or equivalent, provide a 256k x 72 (64 bits plus parity/ECC) Level 2 cache. The L2 cache runs at a ratio of the CPU core speed.

Processor Local/PCI Bridge - CPC700

The CPC700 contains a bridge from the PowerPC processor to the PCI bus, as well as a high speed memory controller, internal peripherals, and control for external ROM and external peripherals. The CPC700 system clock is driven at 33 MHz and is asynchronous with the SDRAM/750 PowerPC 66Mhz bus frequency. The CPC700 supplies the following functions for the Power7E board:

- PowerPC 60x/7xx bus interface operation to 66 MHz
- Synchronous DRAM interface operating at 66 MHz
- External peripheral bus
- PCI Revision 2.1 Compliant Interface
- Interrupt controller supports interrupts from a variety of on and off chip sources
- Programmable Timers
- Two 2-wire 8-bit 16550 compatible UARTS
- Two independent IIC interfaces
- Uses standard type 0 PCI configuration register map(can act like a device or perform host functions)
- A special interface provides for the generation of any PCI command including type 1 configuration cycles
- Support for shared memory locally mapped to the processor's ROM or SDRAM using PCI Base Address Registers
- Buffered PCI writes and supports PCI read pre-fetching from local memory
- Hardware enforced cache coherency
- PCI bus arbitration using a fixed priority arbitration algorithm

The CPC700 incorporates a fixed processor address map that serves the PowerPC family of processors. The address map has provisions for ROM, RAM, and I/O. Mapping can be performed solely from the processor side or from a combination of the processor and PCI side. The address map of the CPC700 is given on the following page.

The CPC700/PowerPC and the CPC700/PCI bus interfaces include the following functions:

1. CPC700 – PowerPC interface.

- Interfaces to PowerPC 750
- One level of processor address pipelining
- Processor Bus Arbiter
- Bus snooping support during PCI access to local memory
- 32 byte write buffer to memory
- Address only cycle support
- Error tracking/status for processor transaction
- Low latency access path to local memory

The CPC700 – PCI interface.

- 32-bit PCI address bus
- PCI bus clock up to 66 MHz (33 MHz synchronous, up to 66 MHz asynchronous)
- Processor to PCI access cycles include:

1. Single-beat PCI I/O reads and writes
2. PCI memory single-beat and prefetch-burst reads and single-beat writes
3. Single beat PCI configuration reads and writes (type 0 and type 1)
4. PCI interrupt acknowledge
5. PCI special cycle – buffered 32 read and write as PCI target and master; PCI master 64 byte read buffer
6. Error tracking and status

The CPC700 memory interface provides support for SDRAM and ROM/Peripherals. Flexible programmable timing is provided on a per bank basis. Up to 5 banks of SDRAM, ROM, or peripherals can be individually programmed. Bank 0 is dedicated to Boot ROM. All other banks are defined in programmable configuration registers. Each bank can have a bus width of 8, 16, 32, or 64 data bits.

CPC700 Address Map

Function	Sub Function	Start Address	End Address	Size
Local Memory/Peripherals		0000_0000	7FFF_FFFF	2GB
PCI Core Space		8000_0000	FF4F_FFFF	2GB – 11MB
	PCI Memory	8000_0000	F800_0000	
	PCI I/O	F800_0000	F800_FFFF	
	Reserved	F801_0000	F87F_FFFF	
	PCI I/O	F880_0000	FBFF_FFFF	
	Reserved	FC00_0000	FEBF_FFFF	
	PCI Config Regs	FEC0_0000	FEC0_0004	
	PCI Interrupt ACK	FED0_0000	FEDF_FFFF	
	Reserved	FEE0_0000	FF3F_FFFF	
	PCI local Config Regs	FF40_0000	FF40_003C	
Device Configuration Register (DCR) Space		FF50_0000	FF5F_FFFF	1MB
	Processor Interface Registers	FF50_0000	FF50_0004	
	Memory Controller Registers	FF50_0008	FF50_000C	
	OPB Macro Registers	FF50_0810	FF50_0818	
	PLB Macro Registers	FF50_0850	FF50_085C	
	Interrupt Controller	FF50_0880	FF50_08A0	
	Clock and Power Management	FF50_0900	FF50_0914	
Internal Peripherals		FF60_0000	FF7F_FFFF	2MB
	UART0	FF60_0300	FF60_0309	
	UART1	FF60_0400	FF60_0409	
	IIC0	FF62_0000	FF62_0010	
	IIC1	FF63_0000	FF63_0010	
	Timers	FF65_0000	FF65_0024	
Local Memory/Peripherals		FF80_0000	FFDF_FFFF	6MB
Boot ROM		FFE0_0000	FFFF_FFFF	2MB

SDRAM

The Power7E contains 64M/128M/256M bytes of on board SDRAM. The ECC function can be tested using ECC control registers contained in the CPC700. Populating the memory locations with 8M x 8 devices results in a baseboard memory size of 64M bytes. An option is available to install a mezzanine board to increase the amount of memory. The mezzanine memory board has a standard SODIMM connector to allow different memory configurations. The mezzanine can either be 64M, 128M, or 256M bytes resulting in a maximum of 512M bytes of SDRAM. The memory runs at 66MHz.

The bank of memory on the baseboard uses CS1 (chip select 1). The mezzanine module(s) will use CS2 – CS4. While the memory controller allows any bank to be mapped to any address, it is necessary for one bank to be mapped to 1 for the exception handlers. In general, bank0 (CS1) will be mapped to 0 for accesses from 0 - 07FF_FFFF for 128M base board memory size. Mapping for the mezzanine module depends on the baseboard size and mezzanine module memory.

Boot Flash Memory

A socket (U18) provides 512K bytes of flash memory organized as 512K x 8. The socket is a 32-pin PLCC socket. The socket can also be used to interface to a ROM emulator.

The 512K byte flash is an AMD 29F040B or equivalent, and resides at FFF0_0000 to FFF7_FFFF when selected as the boot flash (following reset, the processor begins executing at FFF0_0100). When the processor accesses the flash, the memory controller buffers eight accesses before presenting 64 bits of data to the processor. It should be noted that the boot flash memory space is partially decoded so duplicate images of the 512K byte flash device exist in the 2M byte boot space provided by the CPC700 memory controller.

The Power7E also contains an additional 4 – 16MB of soldered-in flash. This flash is an INTEL StrataFlash and can be used as the boot flash by removal of a jumper on the board. When the Strataflash is used as the boot flash, the 512K byte flash chip enable is routed to the on-board location and addresses FF80_0000 – FF87_FFFF (Strataflash) are mapped to FFF0_0000 – FFF7_FFFF. To accomplish this, the two flash devices share chip select signals depending on whether the boot jumper on the board is installed or not. When the jumper is installed, the 512K byte device is the boot device and the Strataflash chip-select is pulled high. When the jumper is not installed the Strataflash device is the boot flash and the 512K byte device chip-select is pulled high.

For more information on the boot flash devices refer to AMD 29LV040B data sheet, AMD publication # 21354, Rev. C. and INTEL StrataFlash data sheet, INTEL publication E28F320J5-100.

UART

The CPC700 contains two UARTs that provide two wire, full duplex serial interfaces to support communications with serial peripheral devices. Each UART is compatible with NS 16550 and includes a 16-byte send and a 16-byte receive FIFO.

Features of the UART include:

- Compatible with the NS 16550
- 16-byte send and 16 byte receive FIFO
- Full duplex operation
- Programmable baud rate generator
- Supports 5-to 8-bit word size, 1/2 stop bits, even/odd/no parity
- Two wire transmit/receive external interface

Timers/Counters

The CPC700 contains a general-purpose timer that includes a time base counter and ten system timers. The time base counter is 32-bit read/write counter and is clocked from the CPC700 system clock (33MHz). The system timers are 32 bits wide, and all are capable of interrupting the PowerPC 750. The general purpose timer is fully programmable through memory mapped registers features include:

- Programmable time base counter
- Maskable time-base comparison support for each compare timer
- Programmable compare timer values
- Enable/disable control of all capture timers
- Enable/disable control of all capture and compare interrupts
- Mask control of interrupt status bits
- Programmable capture event edge detection and synchronization

For further information on the CPC700 Timer/Counter, refer to the CPC700 User's manual given on page 2.2 "JTAG Port" of this document.

PCI/VME Bridge Universe IIB

The VME Interface is implemented with the Tundra Universe IIB chip. The Universe IIB provides a fully compliant, 64 bit, VME bus interface (A32/A24/A16 master & slave, D64/D32/D08 master & slave, MBLT, BLT, RMW, ADOH, LOCK), programmable DMA controller (with independent FIFOs and with linked list support), write post and read prefetch FIFOs, VME interrupter and handler, and VME system controller (with automatic system controller capability).

The Universe IIB chip is a 32-bit PCI peripheral, and as such, it contains several PCI configuration registers (called PCICS -PCI Configuration Space Registers). It also contains registers for controlling VME and PCI operation, known as UCSRs (Universe Control and Status Registers). The UCSRs are accessible via the PCI I/O space (note, the PCICS registers are also a subset of the UCSRs).

Universe power up configuration options is set as follows:

- Automatic system controller detect
- Automatic SYSFAIL# assertion
- PCI register access (UCSRs) set to PCI I/O space
- 32 bit PCI bus width
- BI-mode disabled

The automatic system controller feature works by the Universe monitoring VME signal BGIN3# during SYSRESET# deassertion. A Power7E in slot 1 sees BGIN3# low and it becomes system controller. Logic on the Power7E prevents the BGIN3# signal from propagating to BGOUT3#, thus assuring that no other Power7E boards become system controller.
Note, the BGIN3# method of autosyscon determination is fairly standard; however, care should be taken when other card types co-exist in the same VME chassis. The PCI signals specific to the Universe are shown below:

Universe Signal	PCI Connection
IDSEL	AD14
LINT#	IRQ1#
REQ#	REQ2#
GNT#	GNT2#

For further information on the Universe IIB, refer to Universe IIB User Manual, Tundra Semiconductor Corp, Document Number 8091142.MD300.01. For further information on the VMEbus standard, refer to IEEE Standard for a Versatile Backplane Bus: VME64, ANSI/VITA 1,1994 Standard .

Ethernet Interface

The INTEL 82559ER is an Ethernet LAN controller containing an MII port for connection to 100Mbit transceivers. The 82559ER consists of the Media Access Controller (MAC) and the physical layer (PHY) combined into a single component solution, which allows use of both 10Mbit and 100Mbit (100baseTX) Ethernet through the same cable connection. The transceiver connections are terminated, filtered, and isolated on the Power7E board and are then brought out to an RJ-45 connector on the front panel. A serial EEPROM is used to store the MAC address.

The 82559ER is a PCI peripheral, and as such, it contains several PCI configuration registers. It also contains registers for controlling the Ethernet operation, known as command and status registers (CSRs). CSRs are accessible via the PCI memory and I/O spaces. The PCI signals specific to the 82559ER are shown below:

INTEL 82559 Signal	PCI Connection
IDSEL	AD13
IRQ/	IRQ0#
REQ/	REQ1#
GNT/	GNT1#

For further information on the 82559ER and the MII interface refer to: INTEL 82559ER Fast Ethernet Multifunction PCI/Cardbus Controller Datasheet, INTEL Corp., Document Number 738259-001 Rev 1.0

PMC Slots

The PMC Slot conforms to IEEE draft standards P1386 and P1386.1 as well as being compliant to ProcessorPMC specifications (PPMC). It allows single-width +3.3V expansion boards to be plugged into the Power7E PCI bus via the P11 and P12 connectors. P14 is provided to route PMC I/O to VMEP2 in the manner described below.

The Power7E front panel contains an opening to accept the PMC front bezel. The PCI signals specific to the PMC Slot are shown below:

PMC Slot Signal	PCI Connection
IDSEL	AD15
IRQ/	IRQ2#
REQ/	REQ3#
GNT/	GNT3#

For further information on the PMC specification, refer to PCI Local Bus Specification, Revision 2.1, PCI Special Interest Group, Draft Standard for a Common Mezzanine Card Family: CMC, IEEE Standards Department, P1386/Draft 2.0, and Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC, IEEE Standards Department, P1386.1/Draft 2.0.

SCSI Interface

The Symbios 53C875 provides a SCSI-3 interface capable of transferring 40 MB/sec in Ultra-Wide synchronous mode. The SCSI signals are terminated on the Power7E board using Unitrode UC561DP active terminators, and are then brought out to the VME P2 connector. SCSI peripherals can be plugged into the SCSI interface using an I/O module that plugs into the VMEP2 connector behind the VME backplane, or through a cable that has a mini DB-50 SCSI-2 connector on its front panel. The upper 8 bits of the SCSI data bus are routed to the Z row on P2 so use of Ultra-Wide SCSI requires a 5-row transition module such as the SBS P7E-TM.

The 53C875 is a PCI peripheral, and as such, it contains several PCI configuration registers. It also contains registers for controlling the SCSI operation, known as operating registers. The operating registers are also accessible via the PCI configuration space, as well as the PCI memory and I/O spaces.

The PCI signals specific to the 53C875 are shown below:

NCR 53C875 Signal	PCI Connection
IDSEL	AD12
IRQ/	IRQ3#
REQ/	REQ4#
GNT/	GNT4#

The SCLK frequency provided to the 53C875 is 40 MHz. In order to operate in Ultra SCSI mode the clock doubler on the 53C875 must be enabled.

The SCSI low (8-bit plus control) terminator enable/disable pin is connected to the GPIO0 pin. The high (upper data for wide SCSI) terminator enable/disable pin is connected to the GPIO3 pin. For proper operation, the following 53C875register settings should be used:

NCR 53C875 Parameter	Value
TBD GPCNTL bits 7-0	10x10100
TBD GPREG bits 7-0	xxxx0xx0

For further information on the 53C875, refer to SYM53C875/875E PCI-Ultra SCSI I/O Processor Data Manual Version 4.0, Symbios Logic Inc.

Parallel Port Exar ST78C36CQ64

The ST78C36CQ64 is a monolithic Parallel Port interface. It has a software selectable interrupt and an 8-bit DMA channel.

For further information on the ST78C36CQ64, refer to Exar Corporation — Document Number ST78C36.

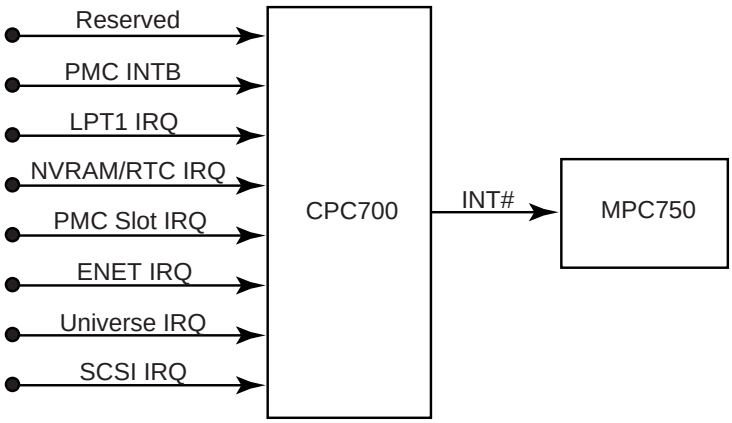
Interrupt Logic

There are two types of interrupts, SMI, and INT:

The processor external interrupt INT can be asserted in two ways:

1. CPC700 internally generated interrupts
2. A specific CPC700 control register is written (and not masked) to cause an interrupt to processor (accessible from the PCI bus).

The interrupt controller in the CPC700 controls interrupts. The CPC700 acts as the PCI master interrupt controller. The CPC700 performs PCI bus arbitration in addition to servicing interrupt requests from PCI slave devices on the bus. All interrupt masking and control is supplied by logic in the CPLD and the CPC700. For a detailed description of CPC700 interrupt processing, refer to the CPC700 User's manual given in section 2 of this document. A block diagram of the interrupt logic for the Power7e board is shown below:



Interrupt Assignments

For further information on the interrupt mapping, refer to the IBM CPC700 User Manual.

NVRAM - SGS Thomson M48T37Y

Power7E contains 32K bytes of battery backed, non-volatile SRAM. The NVRAM is implemented with the ST M48T37Y CMOS Timekeeper SRAM part and is physically located on the ROM bus (CPC700). Processor access to the NVRAM is from addresses FFE8_0000 to FFEF_FFEF. The NVRAM device is a byte wide device, however, the part may be accessed with 8, 16, or 32 bit wide reads or writes. The ST M48T37Y has a replaceable, snappable top hat that contains a battery cell and a crystal; plastic tabs hold the top hat securely to the main body of the part.

For more information regarding the Power7E NVRAM refer to M48T37, 32Kb x 8 TIMEKEEPER SRAM, April 1998 Data Sheet, ST.

Real Time Clock - ST M48T37Y

Power7E contains a battery backed up, real time clock and calendar. The real time clock is implemented with the ST M48T37Y CMOS Timekeeper SRAM part and is physically located on the ROM bus. Processor access to the real time clock is from addresses FFEF_FFF0 to FFEF_FFFF. The Real Time Clock device is a byte wide device, however, the part may be accessed with 8, 16, or 32 bit wide reads or writes. The ST M48T37Y has a replaceable, snappable top hat that contains a battery cell and a crystal; plastic tabs hold the top hat securely to the main body of the part.

The SGS-Thomson M48T37 is Y2K compliant and contains century, year, month, day of month, day of week, hour, minute, and seconds in binary coded decimal registers. Corrections for leap year are performed automatically. The table below itemizes the Real Time Clock registers:

Address	Function	BCD Range	D7	D6	D5	D4	D3	D2	D1	D0
FFEF-FFFF	Year	00 to 99	10 Years				Year			
FFEF-FFFE	Month	01 to 12	0	0	0	10 M.	Month			
FFEF-FFFD	Date	01 to 31	0	0	10Date		Date			
FFEF-FFFC	Day	01 to 07	0	0	0	0	0	Day		
FFEF-FFFB	Hour	00 to 23	0	0	10 Hours		Hours			
FFEF-FFFA	Minute	00 to 59	0	10Minutes			Minutes			
FFEF-FFF9	Second	00 to 59	0	10Seconds			Seconds			
FFEF-FFF8	Control		W	R	S	Cal.	Calibration			
FFEF-FFF7	Watchdog		WDS	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0
FFEF-FFF6	Interrupts		AFE	0	ABE	0	0	0	0	0
FFEF-FFF5	Alarm Date	01 to 31	RPT4	0	Al.	10Date	Al. Date			
FFEF-FFF4	Alarm Hours	00 to 23	RPT3	0	Al.	10Hours	Al. Hours			
FFEF-FFF3	Alarm Minutes	00 to 59	RPT2	Al. 10Seconds			Al. Minutes			
FFEF-FFF2	Alarm Seconds	00 to 59	RPT1	Al. 10Seconds			Al. Seconds			
FFEF-FFF1	Century	00 to 99	1000 Years				100 Years			
FFEF-FFF0	Flags		WDF	AF	Z	`BL	Z	Z	Z	Z

Reads and writes to the Real Time Clock must be coordinated through use of the control register. Before reading a Real Time Clock register, first the “R” bit of the control register must be set. That freezes the current copy of time in an internal buffer in the M48T37 (the internal clock remains counting). Then the clock buffer registers can be read. Note, the clock register buffers will not be updated again until the “R” bit is reset to zero. When any of the real time clock time settings are to be modified, first the “W” bit of the control register must be set. After setting the “W” bit, any or all of the clock buffer registers can be written. Note, the actual update to the clock time settings do not occur until the “W” bit is reset to zero. **Also note, when the “W” bit is reset to zero, all of the buffer registers are updated to the actual Real Time Clock internal counters (not just the buffers that were written).**

For more information, refer to M48T37, 32Kb x 8 TIMEKEEPER SRAM, April 1998 Data Sheet, ST.

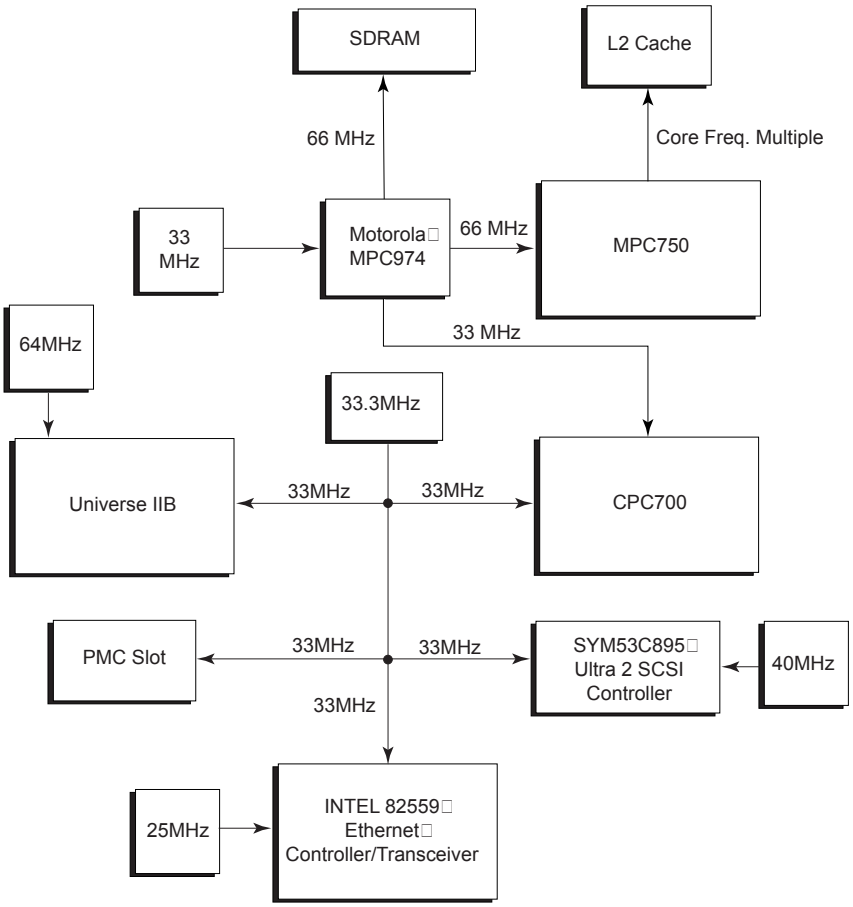
Watchdog Timer ST M48T37Y

The ST M48T37Y contains a built-in watchdog timer. On power-up, the watchdog timer is disabled. Once it is enabled by software, it can be disabled by writing 00h to the watchdog register. It can be set for a timeout interval of ¼ to 124 seconds. The watchdog can be used to generate a system reset.

For more information on the watchdog timer, refer to M48T37, 32Kb x 8 TIMEKEEPER SRAM, April 1998 Data Sheet, ST.

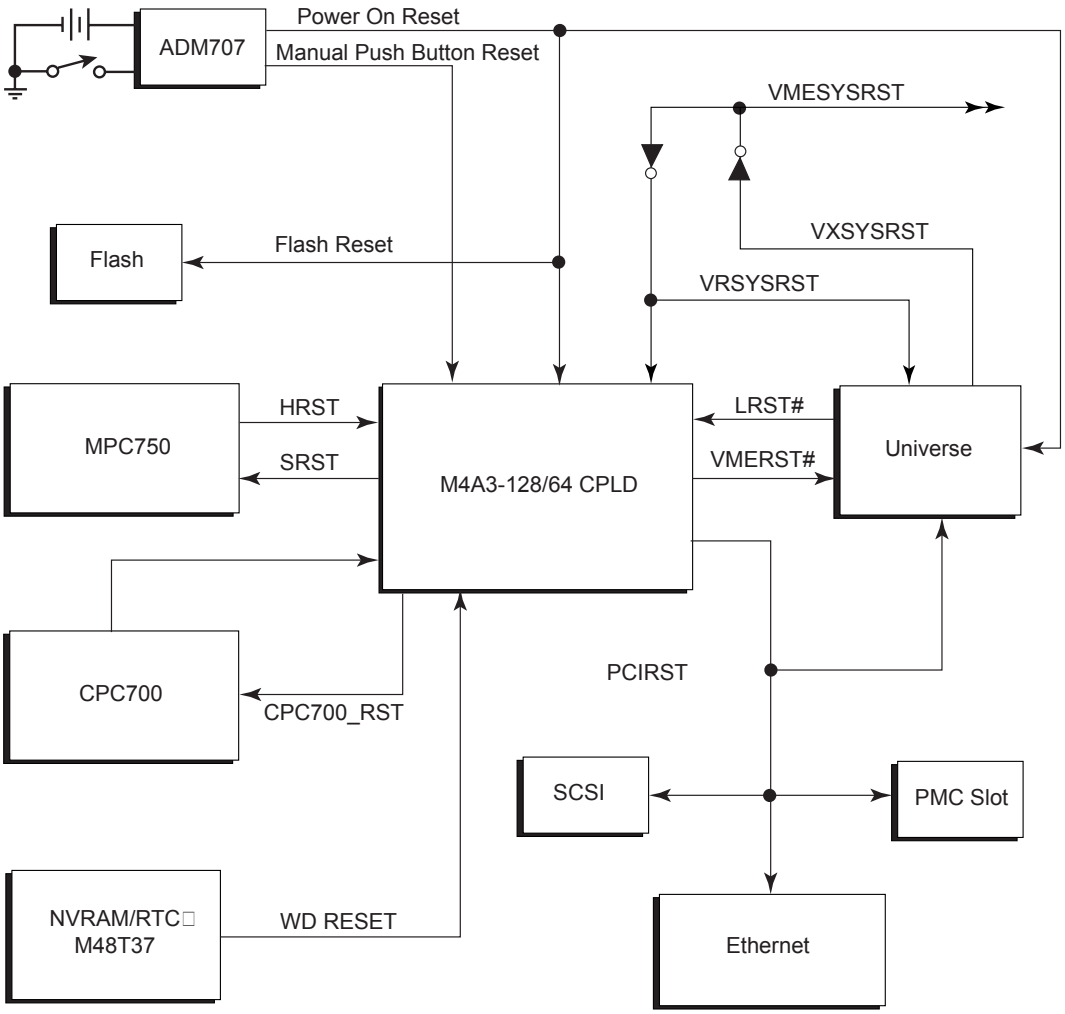
Clock Circuitry

The Power7E uses a Motorola MPC972 clock chip for the majority of the clock requirements. This chip takes a 33 MHz input and generates both 66 MHz and 33 MHz outputs. A Quality Semiconductor 5920 distributes the 66 MHz clocks to the SDRAM chips. A 33 MHz oscillator is used for PCI devices and a 25 MHz oscillator provides the clock for the Ethernet controller/transceiver. An additional 40 MHz oscillator is provided for the SCSI controller as well as a 64 MHz oscillator for the UniverseIIB VME Bridge. The clock for the L2 cache comes from the CPU and is a multiple of the core frequency. The different clocks are distributed as shown below:



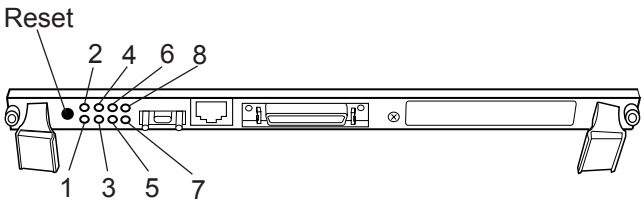
Reset Logic

A diagram of the Power7E reset logic is shown below:



Front Panel LEDs

The Front Panel LEDs are numbered 1 through 8, as illustrated below:



The Front panel LEDs are connected to the following signals:

LED Assignments

Pin	Signal	Function
1	Green	Ethernet Transmit Activity
2	Green	10/100BaseT Link
3	Green	VME System Controller
4	Green	Select 10/100BaseTx
5	Green	User1
6	Green	User2
7	Red	VME System Fail
8	Red	Bit Fail

JTAG/COP Diagnostic Emulator Port

A JTAG/COP emulator interface to 750 processor is provided via JP1, a keyed 2 x 8 header; pinouts of the connector are defined below.

JTAG 2 x 8 Header, Pin Assignments

Pin	Signal	Signal	Pin
1	TDO	QACK_IN#	2
3	TDI	TRST#	4
5	QREQ_OUT#	3.3V(thru 1k Ohm)	6
7	TCK	NC	8
9	TMS	NC	10
11	SRESET#	NC	12
13	HRESET#	Key (No Pin)	14
15	CKSTP_OUT#	GND	16

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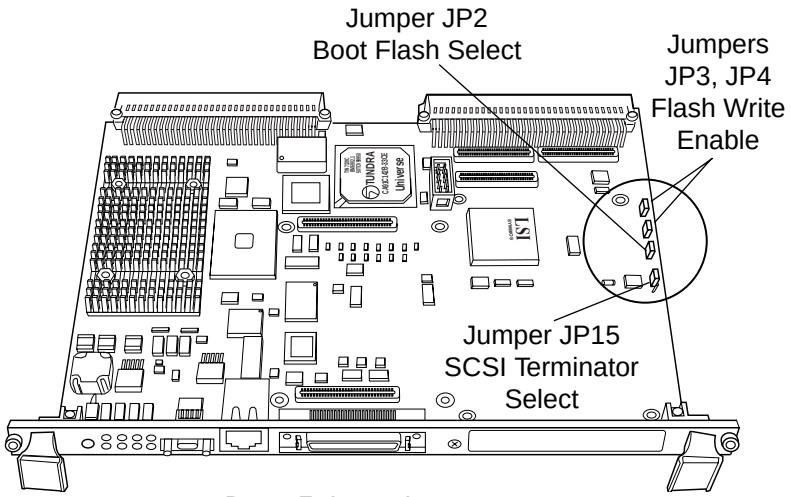
CHAPTER 3 Configuration

Chapter Scope

This chapter provides information regarding configuration options and requirements for the Power7E.

Jumper Configuration



Power7E Jumper Locations

Power7E Jumper Definitions

Jumper	Name	Installed	Removed
JP2	Boot Flash Select	Boot to Socketed Device	Boot to Soldered device
JP3	StrataFlash Write Enable	Writes Allowed	Write Protected
JP4	Boot Flash Write Enable	Writes Allowed	Write Protected
JP15	SCSI Terminator Select	Front Panel (1-2)	VME Connector (2-3)

Jumper JP2 is used to select which flash device the board boots from. When JP2 is installed, the board boots from the socketed device (U18). When JP2 is removed, booting will take place from the soldered device. See page 2-5 for more information on the boot flash.

Jumpers JP3 & JP4 are used to enable or disable writes to the flash devices. When JP3/JP4 is NOT installed, no chip enables are generated for write cycles to the flash devices.

A/B Resistor Configuration

The Power7E is designed with several configuration options selected via the installation location of what are called A/B resistors. These are 0805 style surface mount resistors which can be installed in one of two locations, A or B for a given reference designator (for instance Rx can be installed at A or B). The resistor location is a manufacturing option and is not intended for end user modification. Modifying a resistor location will terminate the warranty unless written consent is given by SBS prior to the modification. The various A/B resistors and their functions are described below:

Resistor	Description	A	B
46	Baseboard ID Bit 1	X	
63	AFREQ		X
64	BFREQ	X	
77	M4-128/64 Enable#		X
92	J12 PMC MONARCH#		X
95	PERR (A) or PMC1042 (B)	X	
117	PPC750 PLL3 Enable	X	
118	PPC750 PLL2 Enable		X
119	PPC750 PLL1 Enable	X	
120	PPC750 PLL0 Enable	X	
121	PPC750 (A) or PPC4700 (B)	X	
122	PCF8594C EEPROM test (A)	X	
133	66MHz (A) or 83MHz (B)	X	
134	ASYNC PCI (A) or SYNC PCI (B)		X
140	TSIZ2 (Used to configure CPC700)	X	
141	TSIZ1 (Used to configure CPC700)	X	
143	PCI ARB EN (A) or Parity EN (B)	X	
144	TSIZ0 (Used to configure CPC700)		X
145	M66EN (Used to configure CPC700)		X
146	Cache Ratio Bit 0	X	
147	Base Board ID Bit 0		X
148	Cache Ratio Bit 2	X	
149	Cache Ratio Bit 1		X
151	SCSI Data 0 (A) or PMCIO2 (B)	X	
152	SCSI Data 1 (A) or PMCIO4 (B)	X	
153	SCSI Data 2 (A) or PMCIO6 (B)	X	
154	SCSI Data 3 (A) or PMCIO8 (B)	X	
155	SCSI Data 4 (A) or PMCIO10 (B)	X	
156	SCSI Data 5 (A) or PMCIO12 (B)	X	
157	SCSI Data 6 (A) or PMCIO14 (B)	X	
158	Printer Strobe (A) or PMCIO15 (B)	X	
159	SCSI Data 7 (A) or PMCIO16 (B)	X	
160	Printer Data Bit 0 (A) or PMCIO17 (B)	X	
162	SCSI DP0 (A) or PMCIO18 (B)	X	
163	Printer Data Bit 1 (A) or PMCIO19 (B)	X	
164	SCSI ATN# (A) or PMCIO20 (B)	X	
165	Printer Data Bit 2 (A) or PMCIO21 (B)	X	

Power7E Jumper Definitions

Power7E A/B Resistor configuration options, continued from previous page

Resistor	Description	A	B
166	SCSI BSY# (A) or PMCIO22 (B)	X	
167	Printer Data Bit 3 (A) or PMCIO23 (B)	X	
168	SCSI ACK# (A) or PMCIO24 (B)	X	
169	Printer Data Bit 4 (A) or PMCIO25 (B)	X	
170	SCSI RST# (A) or PMCIO26 (B)	X	
172	Printer Data Bit 5 (A) or PMCIO27 (B)	X	
173	SCSI MSG# (A) or PMCIO28 (B)	X	
174	Printer Data Bit 6 (A) or PMCIO29 (B)	X	
175	SCSI SEL# (A) or PMCIO30 (B)	X	
176	Printer Data Bit 7 (A) or PMCIO31 (B)	X	
177	Printer INIT# (A) or PMCIO41 (B)	X	
178	Printer SLCT (A) or PMCIO39 (B)	X	
179	SCSI C/D (A) or PMCIO32 (B)	X	
181	Printer ACK# (A) or PMCIO33 (B)	X	
182	SCSI REQ# (A) or PMCIO34(B)	X	
183	Printer BUSY# (A) or PMCIO35 (B)	X	
184	SCSI I/O# (A) or PMCIO36 (B)	X	
185	PPE# (A) or PMCIO37 (B)	X	
197	L2 Cache PPC750 (A) or PPC7400 (B)	X	

Power7E Jumper Definitions

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CHAPTER 4 Memory Map

Chapter Scope

The Power7E memory mapping is extremely flexible. There are only a couple of restrictions imposed by the memory controller.

1. At least 1M byte of system memory must be mapped to address 0.
2. The upper 8M bytes of the CPU address space is reserved for PROM.

Aside from these two requirements, the only restrictions are those imposed by system interoperability issues. The PCI devices can naturally (per PCI spec) be located anywhere in the PCI address space. The PCI memory and I/O spaces can be located anywhere within the CPU memory space. The 8-bit I/O devices can be located anywhere within the first 2M of CPU address space.

Device ID

Since PCI peripherals are mapped into the PCI memory and I/O spaces during system configuration, it is only relevant to list the PCI address/data lines connected to IDSEL lines of the PCI peripherals. Within the PCI configuration space the following device ID selects are used:

Device ID Selects

ID Select	I/O Device	Device Part Number
AD12	SCSI	53C875
AD13	Ethernet	INTEL 82559ER
AD14	VME Bridge	Universe IIb
AD15	PMC Slot	Connector P12
AD16	PMC Slot (IDSELB)	Connector P12

The software will map these devices into PCI memory space at boot time.

Power-On Default 8-Bit Addresses

The power-on default 8-bit I/O addresses for the Power7E 8-bit peripherals are shown below:

8-Bit Peripherals

8-Bit Peripheral	8-Bit Memory Address
M48T37 NVRAM	FFE8_0000 - FFEF_FFEF
M48T37 RTC	FFEF_FFF0 - FFEF_FFFF
Boot Flash	FFF0_0000 - FFF7_FFFF
Parallel Port Standard Mode	FFFF_FD00 - FFFF_FDFF
DRAM Type Register	FFFF_FF00
FlashBank/Miscellaneous Register	FFFF_FF04
Cache Ratio Register	FFFF_FF08
PLD Revision Register	FFFF_FF0C

Miscellaneous Register Map

Miscellaneous Registers

I/O Address	FFFF_FF00	FFFF_FF04	FFFF_FF08	FFFF_FF0C
Name	DRAM Type	FlashBank/Misc.	Cache Ratio	PLDRev
Description	See Below	See Below	See Below	See Below
Type	R/W	R/W	R/W	R/W
Bit 7	BBID1	FB1	X	PLDH3
Bit 6	BBID0	FB0	X	PLDH2
Bit 5	X	X	X	PLDH1
Bit 4	X	SSLOT	X	PLDH0
Bit 3	M2ID1	MISC	X	PLDL3
Bit 2	M2ID0	ULED2	CR2	PLDL2
Bit 1	M1ID1	BITF	CR1	PLDL1
Bit 0	M1ID0	ULED1	CR0	PLDL0
Reset Value	CC00_CCCC	110C_0000	0000_0CCC	CCCC_CCCC

X - bit value doesn't matter, reads as 0.
C - bit value depends on board configuration.

CR2..0 – Cache Ratio, see CR bit definition table 7.
FB1..0 – Flash Bank bits, see FB bit definition table 6.
SSLOT - 1 indicates that board is installed in System Slot. This bit is read only.
MISC – 1 bit R/W register.
BITF - 1 turns on BITFAIL LED, 0 turns it off.
ULED1 - 1 turns on USERLED1, 0 turns it off.
ULED2 - 1 turns on USERLED2, 0 turns it off.
BBID1..0 – Base Board ID bits, see table 5.
M2ID1..0 - Mezzanine #2 ID bits, see table 5.
M1ID1..0 - Mezzanine #1 ID bits, see table 5.
PLDH3..0 – PLD revision, upper bits, represents ones place of revision
PLDL3..0 – PLD revision, lower bits, represents tenths place of revision

DRAM Type

DT (DRAM Type) Baseboard and Mezzanine 1 & 2

BBID1/ M1ID1/ M2ID1	BBID0/ M1ID1/ M2ID0	Meaning
0	0	256M SDRAM
0	1	128M SDRAM
1	0	64M SDRAM
1	1	No SDRAM

FB (FlashBank) Bit Definition

FB1	FB0	Meaning
0	0	FlashBank 4
0	1	FlashBank 3
1	0	FlashBank 2
1	1	FlashBank 1

CR (Cache Ratio) Bit Definition

CR2	CR1	CR0	Meaning
0	0	0	L2 Clk & DLL Disabled
0	0	1	1:1
0	1	0	1.5:1
0	1	1	Reserved
1	0	0	2:1
1	0	1	2.5:1
1	1	0	3:1
1	1	1	Reserved

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CHAPTER 5 Specifications

General

Model	Power7E
Description	VMEbus Single Board Computer
Hardware Compatibility	VMEbus Dual Eurocard, VME64 ANSI/VITA 1-1994

VMEbus

Controller	Tundra Universe IIB
Configuration	DTB Master, Option A32/A24/A16, D32/D16/D08(EO), RMW DTB Slave, Option A32/A24/A16, D32/D16/D08(EO), RMW
Interrupter	Programmable, 1-of-7
Interrupt Handler	Programmable, IH(1-7)
Requester	Programmable, BR(3,2,1,0), Option ROR and RWD
Arbiter	RRS, PRI, SGL
Block Mode Transfer	Master/Slave BLT and MBLT D64/D32/D16

CPU

IBM	PowerPC 750

PCI Bus

Controller	IBM CPC700
Clock Rate	33MHz

Serial Interface

Controller	IBM CPC700
Number	2 RS-232 up to 115 kBaud
Compatibility	IBM PC
Connector	Mini DB9

Parallel Interface

Controller	IBM CPC700
Number	1 Parallel Port
Connector	VME P2 connector I/O

Disk Drive Interface

Hard Disk	Ultrafast SCSI-2 Interface Provided Through Front Panel and VME P2

Ethernet Interface

Type	IEEE 802.3 10/100BaseT (Twisted Pair), Provided Through Front Panel RJ45 connector

Electrical

Power	+5VDC @ 6A with 1MB at 400MHz +12VDC @ 47 mA -12VDC @ 0 mA

Physical

Size	160mm × 233mm (Dual Eurocard), 6U×4HP
Weight	374g
Construction	Multi-Layer Printed Circuit, FR-4 with Flammability rating of 94V-0 by UL recognized manufacturers

Environmental

Temperature	0 to 55° Celsius Inlet Air, Operating -40 to 85° Celsius, Non-Operating
Cooling	Forced Air, 100LFM Fan Recommended
Humidity	10 to 95% Relative Humidity, Non-Condensing
Random Vibration	10 Hz to 500 Hz, 2G
Mechanical Shock	20G, 6mS

CHAPTER 6

Support, Service, and Warranty

Chapter Scope

The following sections describe SBS Technologies product support program. It states our product warranty terms and provides details about what action to take if you experience a problem with the product.

Warranty Statement

SBS Technologies VMEbus products come with a “return-to-factory” warranty that covers defects in materials and workmanship for a period of two years from the date of product shipment to the customer (original purchaser), provided the product is unmodified and has been subject to normal and proper use. This warranty applies to all standard board-level products that do not incorporate disk drives. Products which incorporate floppy or hard disk drives are also warranted for two years with the exception of the drives themselves. The drives will be warranted for a period of ninety days, as is the normal period for electro-mechanical components. SBS Technologies, Inc. makes no warranty or representation, express or implied, with respect to software, its performance, quality, or fitness for a particular purpose. This does not include the media on which the software is distributed, which carries a warranty covering defects in materials and workmanship for a period of ninety days.

If You Have a Problem with an SBS Product

Free technical support is available by phone, fax or email. Telephone suppport is available during the following Eastern Time hours:

Monday through Friday 8:30 am - 5:30 pm.

You can reach technical support at (919) 851-1101 voice, (919) 851-2844 fax or email at support@sbs.com.

Product Repairs

To expedite assistance for problems, be able to provide the following:

- Your Name, Phone number and Company.
- Product with which you are having trouble.
- Serial Number and Revision.
- Operating system you are running.
- Detailed description of your problem and any error messages that have appeared on the screen.

Depending on the circumstances of the problem, it may be deemed necessary to return the product to SBS Technologies for repair. In order to return the product for repair, the following steps are necessary:

1. Obtain a Return Material Authorization number (RMA#) from SBS Customer Support.

2. Ship the product prepaid to the designated repair point.

3. Provide a written description of the claimed defect with the product.

Obtaining an RMA Number

To obtain a product return authorization number (RMA#), you should call our Customer Service department through our main number.

Shipping the Product

Any product returned to SBS should be in its original shipping carton if possible. Otherwise the product should be carefully packaged in a conductive packing material and placed in a cushioned corrugated carton suitable for shipping. Please mark the shipping label with the RMA number and return it to:

Customer Service Department
Att: RMA# *(put RMA number here)*
SBS Technologies, Inc.
6301 Chapel Hill Road
Raleigh, NC 27607

Providing a Product Defect Report

When you are returning a product for repair, it is very important to include a written report which details the nature of the problem in order to expedite the repair. Please make sure that the following information is included:

- RMA Number
- Product:
- Serial Number
- Contact:
- Phone
- Description of the Problem/Defect

Warranty Repairs

Any product returned and found to be under warranty will be repaired or replaced at the discretion of SBS Technologies.

Non-Warranty Repairs

If a product is found not to be under warranty, we will notify you of the non-warranty situation and provide you with a fixed cost and a schedule for the repair. Non-warranty repairs generally require that a purchase order be issued to SBS Technologies, Inc. for the amount of the repair before repairs are undertaken.

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APPENDIX

VME64 I/O Information

VME64 P1 I/O

The following table shows the standard VME64 P1 I/O Mapping

Pin	Row Z	Row A	Row B	Row C	Row D
1	NC	VMED0	VMEBBSY#	VMED8	Vcc
2	GND	VMED1	VMEBCLR#	VMED9	GND
3	NC	VMED2	VMEACFAIL#	VMED10	NC
4	GND	VMED3	VMEBGIN0#	VMED11	NC
5	NC	VMED4	VMEBGOUT0#	VMED12	NC
6	GND	VMED5	VMEBGIN1#	VMED13	NC
7	NC	VMED6	VMEBGOUT1#	VMED14	NC
8	GND	VMED7	VMEBGIN2#	VMED15	NC
9	NC	GND	VMEBGOUT2#	GND	NC
10	GND	VMESYSCLK	VMEBGIN3#	VMESYSFAIL#	NC
11	NC	GND	VMEBGOUT3#	VMEBERR#	NC
12	GND	VMEDS1#	VMEBR0#	VMESYSRST#	NC
13	NC	VMEDS0#	VMEBR1#	VMELWORD#	NC
14	GND	VMEWR#	VMEBR2#	VMEAM5	NC
15	NC	GND	VMEBR3#	VMEA23	NC
16	GND	VMEDTACK#	VMEAM0	VMEA22	NC
17	NC	GND	VMEAM1	VMEA21	NC
18	GND	VMEAS#	VMEAM2	VMEA20	NC
19	NC	GND	VMEAM3	VMEA19	NC
20	GND	VMEIACK#	GND	VMEA18	NC
21	NC	VMEIACKIN#	NC	VMEA17	NC
22	GND	VMEIACKOUT#	NC	VMEA16	NC
23	NC	VMEAM4	GND	VMEA15	NC
24	GND	VMEA7	VMEIRQ7#	VMEA14	NC
25	NC	VMEA6	VMEIRQ6#	VMEA13	NC
26	GND	VMEA5	VMEIRQ5#	VMEA12	NC
27	NC	VMEA4	VMEIRQ4#	VMEA11	NC
28	GND	VMEA3	VMEIRQ3#	VMEA10	NC
29	NC	VMEA2	VMEIRQ2#	VMEA9	NC
30	GND	VMEA1	VMEIRQ1#	VMEA8	NC
31	NC	-12v	NC	+12v	GND
32	GND	Vcc	Vcc	Vcc	Vcc

VME64 P2 I/O

This table shows the standard VME64 P2 I/O Mapping

Pin	Row Z	Row A	Row B	Row C	Row D
1	*PMCIO39	P2_IOA1	Vcc	PMCIO1	*PMCIO2
2	GND	P2_IOA2	GND	PMCIO3	*PMCIO4
3	*PMCIO41	P2_IOA3	NC	PMCIO5	*PMCIO6
4	GND	P2_IOA4	VMEA24	PMCIO7	*PMCIO8
5	PMCIO43	P2_IOA5	VMEA25	PMCIO9	*PMCIO10
6	GND	P2_IOA6	VMEA26	PMCIO11	*PMCIO12
7	SD8#	P2_IOA7	VMEA27	PMCIO13	*PMCIO14
8	GND	P2_IOA8	VMEA28	P2_IOC8	*PMCIO15
9	SD9#	P2_IOA9	VMEA29	P2_IOC9	*PMCIO16
10	GND	P2_IOA10	VMEA30	P2_IOC10	*PMCIO17
11	SD10#	P2_IOA11	VMEA31	P2_IOC11	*PMCIO 18
12	GND	P2_IOA12	GND	P2_IOC12	*PMCI O19
13	SD11#	P2_IOA13	Vcc	P2_IOC13	*PMCI O20
14	GND	P2_IOA14	VMED16	P2_IOC14	*PMCIO21
15	SD12#	P2_IOA15	VMED17	P2_IOC15	*PMCIO 22
16	GND	P2_IOA16	VMED18	P2_IOC16	*PMCIO 23
17	SD13#	P2_IOA17	VMED19	P2_IOC17	*PMCIO 24
18	GND	P2_IOA18	VMED20	P2_IOC18	*PMCIO 25
19	SD14#	PMCIO38	VMED21	P2_IOC19	*PMCIO 26
20	GND	PMCIO40	VMED22	P2_IOC20	*PMCIO27
21	SD15#	*PMCIO42	VMED23	P2_IOC21	*PMCIO 28
22	GND	PMCIO44	GND	P2_IOC22	*PMCIO29
23	SDP1#	PMCIO46	VMED24	PMCIO45	*PMCIO30
24	GND	PMCIO48	VMED25	PMCIO47	*PMCIO31
25	NC	PMCIO50	VMED26	PMCIO49	*PMCIO32
26	GND	PMCIO52	VMED27	PMCIO51	*PMCIO33
27	NC	PMCIO54	VMED28	PMCIO53	*PMCIO34
28	GND	PMCIO56	VMED29	PMCIO55	*PMCIO35
29	UART_T X1	PMCIO58	VMED30	PMCIO57	*PMCIO36
30	GND	PMCIO60	VMED31	PMCIO59	*PMCIO37
31	UART_RX1	PMCIO62	GND	PMCIO61	GND
32	GND	PMCIO64	Vcc	PMCIO63	Vcc

*Asterisks indicate pin connections that depend on the placement of A/B Resistors as indicated on pages 3-2 and 3-3 of this manual.

3-Row P2 I/O

An optional version of the P7E has only three rows of pins (Row A, B and C) on the VME P2 connector. In order to provide COM2 via the P2 connector in this version, UART_TX1 is provided on pin A29 and UART_RX1 is provided on pin A31. Therefore it is necessary to verify you use the correct Transition Module. Both versions of the P7E-TM Transition Module have the 5-Row connector, but the one intended for the 3-Row P7E is modified to accept COM2 I/O on row A.

Pin	Row A	Row B	Row C
1	P2_IOA1	Vcc	PMCIO1
2	P2_IOA2	GND	PMCIO3
3	P2_IOA3	NC	PMCIO5
4	P2_IOA4	VMEA24	PMCIO7
5	P2_IOA5	VMEA25	PMCIO9
6	P2_IOA6	VMEA26	PMCIO11
7	P2_IOA7	VMEA27	PMCIO13
8	P2_IOA8	VMEA28	P2_IOC8
9	P2_IOA9	VMEA29	P2_IOC9
10	P2_IOA10	VMEA30	P2_IOC10
11	P2_IOA11	VMEA31	P2_IOC11
12	P2_IOA12	GND	P2_IOC12
13	P2_IOA13	Vcc	P2_IOC13
14	P2_IOA14	VMED16	P2_IOC14
15	P2_IOA15	VMED17	P2_IOC15
16	P2_IOA16	VMED18	P2_IOC16
17	P2_IOA17	VMED19	P2_IOC17
18	P2_IOA18	VMED20	P2_IOC18
19	PMCIO38	VMED21	P2_IOC19
20	PMCIO40	VMED22	P2_IOC20
21	*PMCIO42	VMED23	P2_IOC21
22	PMCIO44	GND	P2_IOC22
23	PMCIO46	VMED24	PMCIO45
24	PMCIO48	VMED25	PMCIO47
25	PMCIO50	VMED26	PMCIO49
26	PMCIO52	VMED27	PMCIO51
27	PMCIO54	VMED28	PMCIO53
28	PMCIO56	VMED29	PMCIO55
29	UART_TX1	VMED30	PMCIO57
30	PMCIO60	VMED31	PMCIO59
31	UART_RX1	GND	PMCIO61
32	PMCIO64	Vcc	PMCIO63

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