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Px-Octal

PC•MIP Modules with Eight Serial Channels

User Manual

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Px-Octal
PC•MIP Modules with
Eight Serial Channels

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Product Description

The Px-Octal product family provides eight channels of EIA-232, EIA-422, or TTL-compatible (3.3V) asynchronous serial communication on a Type I (flexible I/O) or Type II (front panel I/O) PC•MIP module. The high channel density makes the Px-Octal module ideal for communications applications that require a large number of serial channels in a small space.

Five versions of the Px-Octal family are documented here:

- P1-Octal-TTL is a Type I (flexible I/O) module with TTL-compatible (3.3V) driver support.
- P1-Octal-232 is a Type I (flexible I/O) module with EIA-232 driver support.
- P1-Octal-422 is a Type I (flexible I/O) module with EIA-422 driver support.
- P2-Octal-232 is a Type II (front panel I/O) module with EIA-232 driver support.
- P2-Octal-422 is a Type II (front panel I/O) module with EIA-422 driver support.

In addition to the common core design features of these modules, this manual documents the differences in serial drivers and I/O routing for these products.

The Px-Octal family features two quad UART SCCs with 128 bytes of transmit FIFO and 128 bytes of receive FIFO per channel. Data rates of up to 460.8 kbaud are supported for RS-422 communications, and up to 115.2 kbaud for the RS-232 and TTL (3.3V) communications.

Serial signals for each channel are routed to the flexible I/O connector for rear-panel access. For the RS-232 and RS-422 options, all signals are ESD-protected up to ±15 kV, according to IEC 1000.4.2 specifications.

Baud rate is software-configurable from 50 bps to the maximum rate via the on-board programmable baud rate generator. Interrupts are fully supported per channel with four programmable transmit/receive FIFO interrupt trigger levels. In addition, programmable bit length, parity, and stop bits are provided to support all asynchronous protocols.

A VxWorks 5.3 driver and a Windows NT 4.0 are available. The Px-Octal modules are compatible with the PC•MIP draft specification (ANSI/VITA-29).

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Block Diagrams

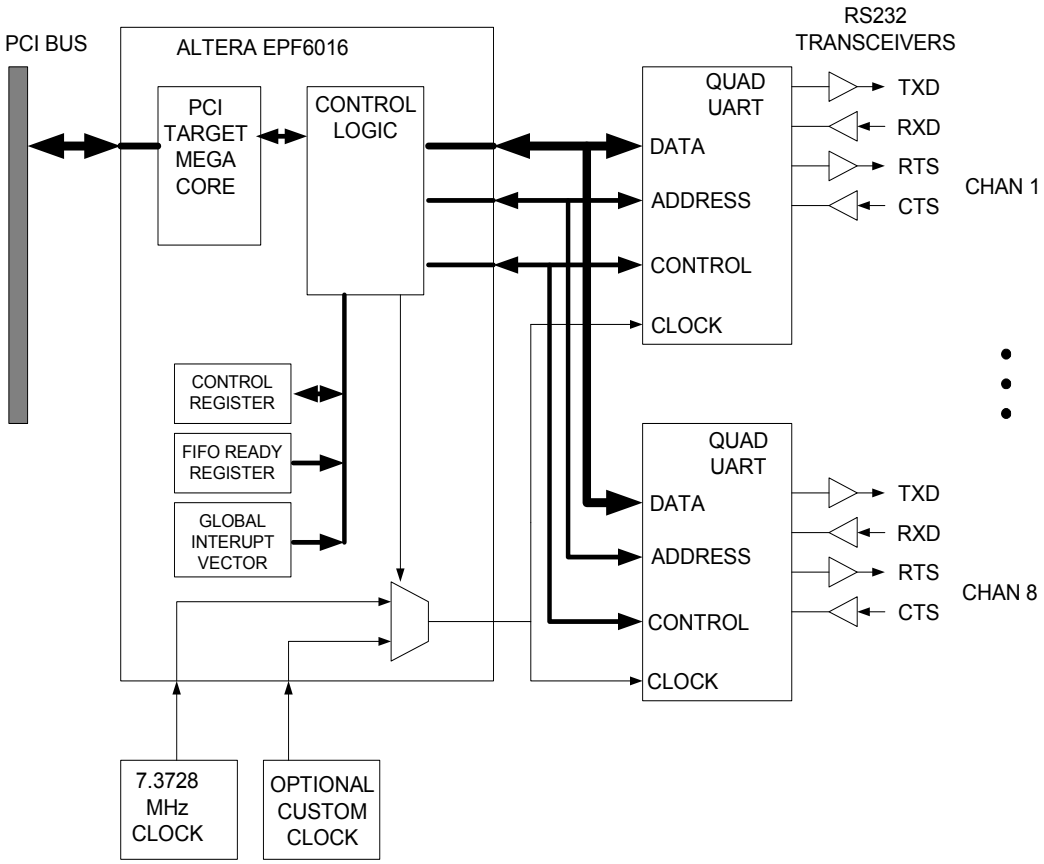


Figure 1. Block Diagram - Version 232

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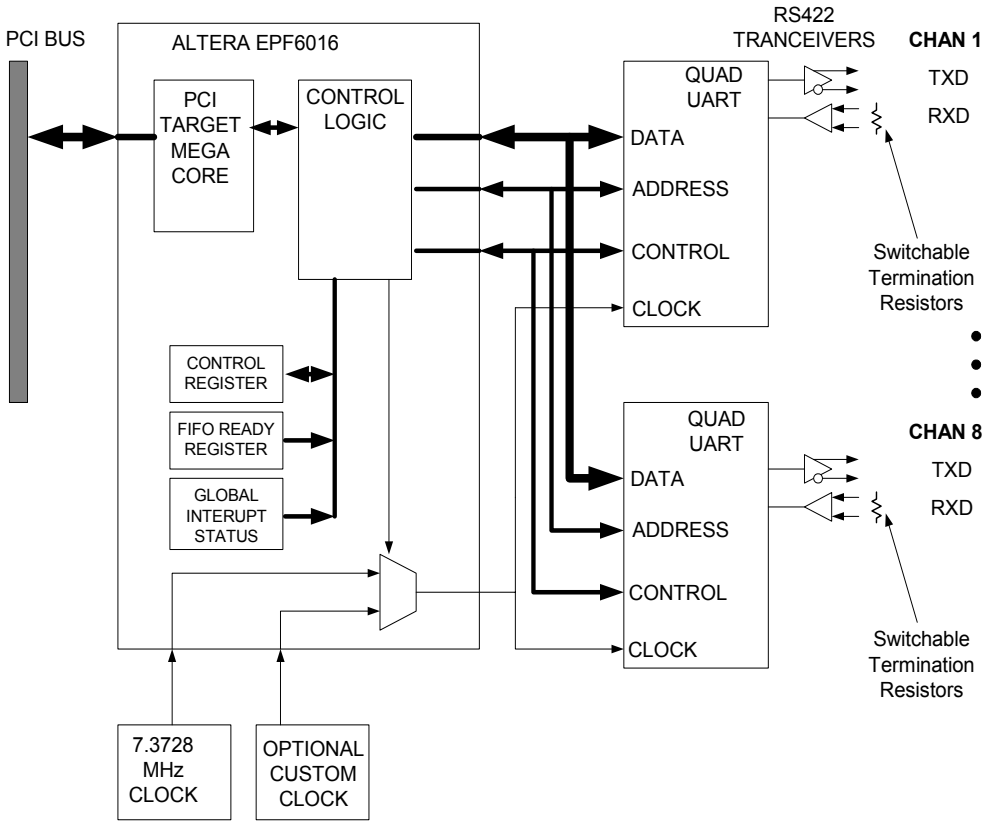


Figure 2. Block Diagram - Version 422

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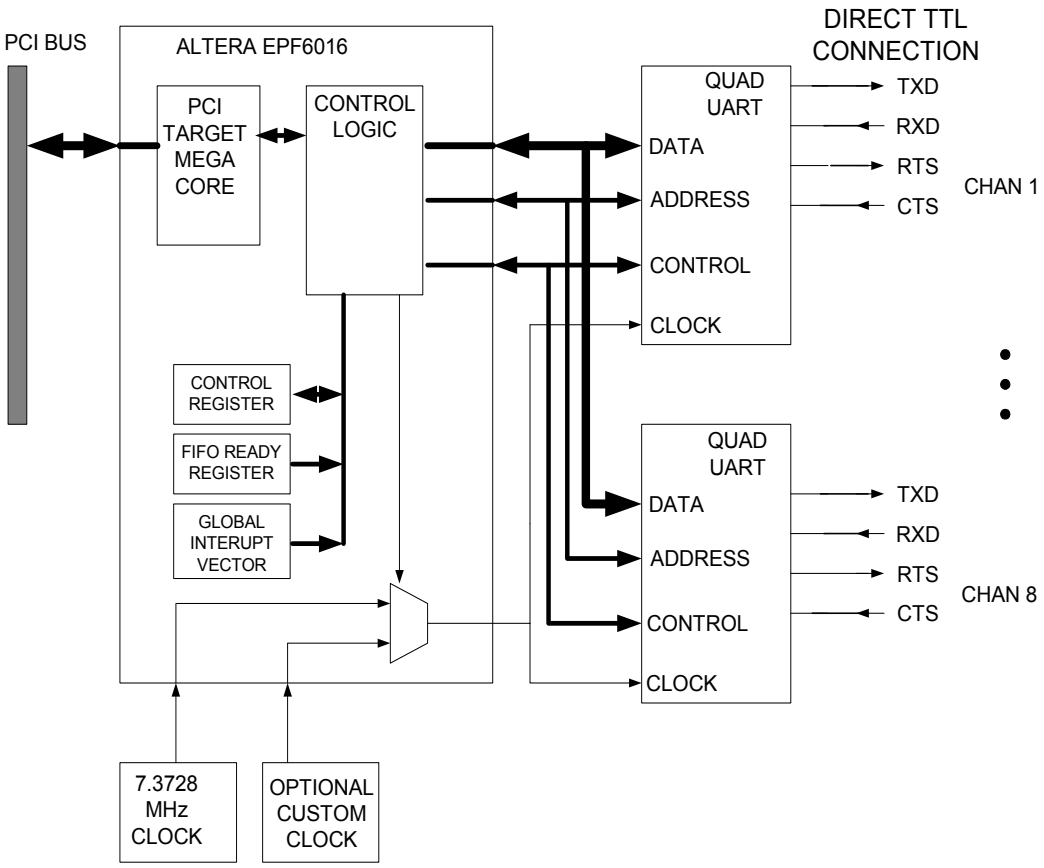


Figure 3. Block Diagram - TTL Version

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Quick Start

Each channel is implemented by a unique set of UART registers but also shares the global control, FIFO ready, and interrupt status registers implemented in the Altera device.

This section illustrates how to:

1. Configure Channel 1 and Channel 8 for 9600 baud rate, 8 data bits, 1 stop bit, and no parity
2. Transmit two bytes from Channel 1
3. Read the two transmitted bytes from Channel 8

All addresses indicate offset from BAR0. To transmit characters from Channel 1 to Channel 8, Channel 1 TxD pin should be connected to Channel 8 RxD pin as illustrated in the figure below:

	Connect From		Connect To	
Board	**Pin**	**Signal**	**Pin**	**Signal**
P1-Octal-232	2	TxD 1	49	RxD 8
P2-Octal-232	2		34	

Figure 4. Quick Start Pin Connections to Transmit Characters - 232 Versions

	Connect From		Connect To	
Board	**Pin**	**Signal**	**Pin**	**Signal**
P1-Octal-422	2	TxD- 1	51	RxD- 8
	3	TxD+ 1	52	RxD+ 8
P2-Octal-422	2	TxD- 1	35	RxD- 8
	3	TxD+ 1	36	RxD+ 8

Figure 5. Quick Start Pin Connections to Transmit Characters - 422 Versions

	Connect From		Connect To	
Board	**Pin**	**Signal**	**Pin**	**Signal**
P1-Octal-TTL	2	TxD 1	49	RxD 8

Figure 6. Quick Start Pin Connections to Transmit Characters - TTL Version

On the P1-Octal versions, the connection is made at the backplane or on the carrier board at a user I/O connector. Be careful to join the correct pins.

UART Reset

- Write 0x10 to offset 0x0500
  Write 0x00 to offset 0x0500
  (This step resets both UARTs. It is recommended to delay 500ms between the two writes.)

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Channel 1 Configuration

1. Write 0x80 to offset 0x0030
   (Enables access to Special Register.)
2. Write 0x0C to offset 0x0000
   Write 0x00 to offset 0x0010
   (Sets baud rate to 9600.)
3. Write 0x03 to offset 0x0030
   (Exits Special Register mode and sets 8 data bits, 1 stop bit, no parity.)
4. Write 0x00 to offset 0x0010
   (Disables all interrupts.)
5. Write 0x01 to offset 0x0020
   (Enables FIFO operation.)

Channel 8 Configuration

1. Write 0x80 to offset 0x1330
   (Enables access to Special Register.)
2. Write 0x0C to offset 0x1300
   Write 0x00 to offset 0x1310
   (Sets baud rate to 9600.)
3. Write 0x03 to offset 0x1330
   (Exits Special Register mode and sets 8 data bits, 1 stop bit, no parity.)
4. Write 0x00 to offset 0x1310
   (Disables all interrupts.)
5. Write 0x01 to offset 0x1320
   (Enables FIFO operation.)

Transmitting and Reading

1. Write 0x11 to offset 0x0000
   Write 0x22 to offset 0x0000
   (Writes two characters to THR register, which transmits them out of Channel 1.)
2. Read from 0x1300
   (Reads from Channel 8 RHR register. Result should be 0x11.)
3. Read from 0x1300
   (Reads from Channel 8 RHR register. Result should be 0x22.)

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Channel Numbering

The Px-Octal uses two quad UARTs (UART 0 and UART 1). Please refer to the Exar ST16C854 Data Sheet for a complete definition of all the UART registers. UART channels are labeled as follows:

Channel Number	UART Number	UART Channel
1	0	A
2		B
3		C
4		D
5	1	A
6		B
7		C
8		D

Figure 7. Channel Numbering

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PCI Configuration Registers

PCI Configuration Registers can be accessed only through PCI Configuration Read and Configuration Write cycles. Px-Octal PCI configuration space follows PCI Local Bus Specification, Revision 2.1, which defines sixteen 32-bit words of block configuration space. The registers within this range identify the device, control PCI bus functions, and indicate PCI bus status. The table below summarizes PCI configuration registers supported by the Px-Octal.

Address Offset (Hex)	Range Reserved (Hex)	Read/Write	Mnemonic	Register Name
00	00-01	Read	ven_id	Vendor ID
02	02-03	Read	dev_id	Device ID
04	04-05	Read/Write	Comd	Command
06	06-07	Read/Write	status	Status
08	08-08	Read	rev_id	Revision ID
09	09-0B	Read	class	Class Code
0E	0E-0E	Read	header	Header type
10	10-13	Read/Write	bar0	Base address register zero
2C	2C-2D	Read	sub_ven_id	Subsystem Vendor ID
2E	2E-2F	Read	sub_id	Subsystem ID
3C	3C-3C	Read/Write	int_ln	Interrupt line
3D	3D-3D	Read	int_pin	Interrupt pin

Note: Unused registers ignore write operations and produce a zero when read.

Figure 8. PCI Configuration Registers

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The following table specifies read-only PCI Configuration register values. For a detailed description of these registers, please refer to PCI Local Bus Specification, Revision 2.1.

Register	Value
Vendor ID	0x124b
Device ID	0x0001
Revision ID	0x0001
Class Code	0x0007
Header Type	0x0000
Subsystem Vendor ID	0x124b
Subsystem ID	0x0308

Figure 9. Read-Only PCI Configuration Register Values – RS-232 Versions

Register	Value
Vendor ID	0x124b
Device ID	0x0001
Revision ID	0x0001
Class Code	0x0007
Header Type	0x0000
Subsystem Vendor ID	0x124b
Subsystem ID	0x0408

Figure 10. Read-Only PCI Configuration Register Values – RS-422 Versions

Register	Value
Vendor ID	0x124b
Device ID	0x0001
Revision ID	0x0001
Class Code	0x0007
Header Type	0x0000
Subsystem Vendor ID	0x124b
Subsystem ID	0x0308

Figure 11. Read-Only PCI Configuration Register Values - TTL Version

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Memory Space

The host system accesses the Px-Octal via a 33 MHz, 32-bit PC•MIP interface that is PCI Specification 2.1 compliant.

The board contains two sets of registers. One set is implemented in the Altera device and consists of the Control Register (CR), FIFO Ready Registers (FRR), and the Global Interrupt Status Register (GISR). The second set of registers is built into the UART and provides access to UART's status and control registers. All are accessible through the PCI BAR0.

The PCI BAR0 is mapped in PCI Memory Space and consumes 8Kbytes of space. The registers are 8 bits wide and 8-, 16-, or 32-bit accessible.

The following table lists the base address offset for all registers accessible from the memory space.

Name	Description	Size (bytes)	Access Type	Address Offset
CB1	Channel 1 Base	0x80	Read/Write	0x0000
CB2	Channel 2 Base	0x80	Read/Write	0x0100
CB3	Channel 3 Base	0x80	Read/Write	0x0200
CB4	Channel 4 Base	0x80	Read/Write	0x0300
CR	Control Register Channels 1-8	0x01	Read/Write	0x0500
FRR14	FIFO Ready Register Channels 1-4	0x01	Read	0x0600
GISR	Global Interrupt Status Register	0x01	Read	0x0700
CB5	Channel 5 Base	0x80	Read/Write	0x1000
CB6	Channel 6 Base	0x80	Read/Write	0x1100
CB7	Channel 7 Base	0x80	Read/Write	0x1200
CB8	Channel 8 Base	0x80	Read/Write	0x1300
	Reserved	---	---	0x1500
FRR58	FIFO Ready Register Channels 5-8	0x01	Read	0x1600
	Reserved	---	---	0x1700

Figure 12. Memory Address Map

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Altera-Implemented Registers

Registers implemented in the Altera device consist of the Control Register (CR), FIFO Ready Registers (FRR), and the Global Interrupt Status Register (GISR).

CR Control Register

7	6	5	4	3	2	1	0	Bit
OSC1_PRSNT	0	0	UART_RESET	OSCSEL	INTENABLE	CLKSEL_1	CLKSEL_0	Read
X	X	X	UART_RESET	OSCSEL	INTENABLE	CLKSEL_1	CLKSEL_0	Write
OSC1_PRSNT	0	0	0	0	0	0	0	Reset

The Control Register controls clock and oscillator selection, enables interrupts, and indicates installation status of a user-supplied oscillator.

7	OSC1_PRSNT	Oscillator 1 Present	R

This bit indicates whether a user-supplied oscillator (OSC1) is installed. Logic one indicates that OSC1 is installed. Logic zero indicates that OSC1 is not installed.

6..5		Reserved	R

These bits are reserved for future use. They are read as zeros and are ignored on writes. Resets to zero.

4	UART_RESET	UART Reset	R/W

Writing a one to this bit places both UARTs in the reset state. Writing a zero discontinues the reset state for both UARTs. Resets to zero.

3	OSCSEL	Oscillator Select	R/W

This bit selects one of two oscillators. A zero value enables Oscillator 2 and a one value enables Oscillator 1. Resets to zero.

2	INTENABLE	Interrupt Enable	R/W

When set to one, this bit enables interrupts. When set to zero, this bit disables interrupts. (Note: interrupts can be further controlled through the IER.) Resets to zero.

1	CLKSEL_1	Clock Select 1	R/W

This bit controls the CLKSEL pin on the UART 1 (Channels 5-8). A one value selects the 1x clock. A zero value selects the 4x clock. Resets to zero.

0	CLKSEL_0	Clock Select 0	R/W

This bit controls the CLKSEL pin on the UART 0 (Channels 1-4). A one value selects the 1x clock. A zero value selects the 4x clock. Resets to zero.

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FRR14 FIFO Ready Channels 1-4

7	6	5	4	3	2	1	0	Bit
C4_RXRDY	C3_RXRDY	C2_RXRDY	C1_RXRDY	C4_TXRDY	C3_TXRDY	C2_TXRDY	C1_TXRDY	Read
X	X	X	X	X	X	X	X	Write
1	1	1	1	0	0	0	0	Reset

FIFO Ready Channels 1-4 reflect the status of Transmit FIFO Channels 1-4 and Receive FIFO Channels 1-4.

7	C4_RXRDY	Channel 4 RXRDY	R

This bit reflects status of the RXRDY pin on Channel 4 of the UART, which in turn indicates status of the Channel 4 Receive FIFO. A zero indicates that the FIFO has either reached the programmed trigger level or a time-out has occurred. A one indicates that the FIFO is below the programmed trigger level. Resets to one.

6	C3_RXRDY	Channel 3 RXRDY	R

This bit reflects status of the RXRDY pin on Channel 3 of the UART, which in turn indicates status of the Channel 3 Receive FIFO. A zero indicates that the FIFO has either reached the programmed trigger level or a time-out has occurred. A one indicates that the FIFO is below the programmed trigger level. Resets to one.

5	C2_RXRDY	Channel 2 RXRDY	R

This bit reflects status of the RXRDY pin on Channel 2 of the UART, which in turn indicates status of the Channel 2 Receive FIFO. A zero indicates that the FIFO has either reached the programmed trigger level or a time-out has occurred. A one indicates that the FIFO is below the programmed trigger level. Resets to zero.

4	C1_RXRDY	Channel 1 RXRDY	R

This bit reflects status of the RXRDY pin on Channel 1 of the UART, which in turn indicates status of the Channel 1 Receive FIFO. A zero indicates that the FIFO has either reached the programmed trigger level or a time-out has occurred. A one indicates that the FIFO is below the programmed trigger level. Resets to one.

3	C4_TXRDY	Channel 4 TXRDY	R

This bit reflects status of the TXRDY pin on Channel 4 of the UART, which in turn indicates status of the Channel 4 Transmit FIFO. A one indicates that the Transmit FIFO trigger level has been reached. A zero indicates that the Transmit FIFO is below the trigger level. Resets to zero.

2	C3_TXRDY	Channel 3 TXRDY	R

This bit reflects status of the TXRDY pin on Channel 3 of the UART, which in turn indicates status of the Channel 3 Transmit FIFO. A one indicates that the Transmit FIFO trigger level has been reached. A zero indicates that the Transmit FIFO is below the trigger level. Resets to zero.

1	C2_TXRDY	Channel 2 TXRDY	R

This bit reflects status of the TXRDY pin on Channel 2 of the UART, which in turn indicates status of the Channel 2 Transmit FIFO. A one indicates that the Transmit FIFO trigger level has been reached. A zero indicates that the Transmit FIFO is below the trigger level. Resets to zero.

0	C1_TXRDY	Channel 1 TXRDY	R

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This bit reflects status of the TXRDY pin on Channel 1 of the UART, which in turn indicates status of the Channel 1 Transmit FIFO. A one indicates that the Transmit FIFO trigger level has been reached. A zero indicates that the Transmit FIFO is below the trigger level. Resets to zero.

Note: For information on setting Receive and Transmit FIFO trigger levels, please refer to the XR16C854 UART data sheet. (The XR16C854 UART data sheet contains a discrepancy in its description of the TXRDY pin. The TXRDY pin does not indicate if at least one empty location is available in Transmit FIFO. Instead, it indicates whether the trigger level is reached as described in the FIFO Ready Register Definition.)

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FRR58 FIFO Ready Channels 5-8

7	6	5	4	3	2	1	0	Bit
C8_RXRDY	C7_RXRDY	C6_RXRDY	C5_RXRDY	C8_TXRDY	C7_TXRDY	C6_TXRDY	C5_TXRDY	Read
X	X	X	X	X	X	X	X	Write
1	1	1	1	0	0	0	0	Reset

FIFO Ready Channels 5-8 reflect the status of Transmit FIFO Channels 5-8 and Receive FIFO Channels 5-8.

7	C8_RXRDY	Channel 8 RXRDY	R

This bit reflects status of the RXRDY pin on Channel 8 of the UART, which in turn indicates status of the Channel 8 Receive FIFO. A zero indicates that the FIFO has reached the programmed trigger level or a time-out has occurred. A one indicates that the FIFO is below the programmed trigger level. Resets to one.

6	C7_RXRDY	Channel 7 RXRDY	R

This bit reflects status of the RXRDY pin on Channel 7 of the UART, which in turn indicates status of the Channel 7 Receive FIFO. A zero indicates that the FIFO has reached the programmed trigger level or a time-out has occurred. A one indicates that the FIFO is below the programmed trigger level. Resets to one.

5	C6_RXRDY	Channel 6 RXRDY	R

This bit reflects status of the RXRDY pin on Channel 6 of the UART, which in turn indicates status of the Channel 6 Receive FIFO. A zero indicates that the FIFO has reached the programmed trigger level or a time-out has occurred. A one indicates that the FIFO is below the programmed trigger level. Resets to one.

4	C5_RXRDY	Channel 5 RXRDY	R

This bit reflects status of the RXRDY pin on Channel 5 of the UART, which in turn indicates status of the Channel 5 Receive FIFO. A zero indicates that the FIFO has reached the programmed trigger level or a time-out has occurred. A one indicates that the FIFO is below the programmed trigger level. Resets to one.

3	C8_TXRDY	Channel 8 TXRDY	R

This bit reflects status of the TXRDY pin on Channel 8 of the UART, which in turn indicates status of the Channel 8 Transmit FIFO. A one indicates that the Transmit FIFO trigger level has been reached. A zero indicates that the Transmit FIFO is below the trigger level. Resets to zero.

2	C7_TXRDY	Channel 7 TXRDY	R

This bit reflects status of the TXRDY pin on Channel 7 of the UART, which in turn indicates status of the Channel 7 Transmit FIFO. A one indicates that the Transmit FIFO trigger level has been reached. A zero indicates that the Transmit FIFO is below the trigger level. Resets to zero.

1	C6_TXRDY	Channel 6 TXRDY	R

This bit reflects status of the TXRDY pin on Channel 6 of the UART, which in turn indicates status of the Channel 6 Transmit FIFO. A one indicates that the Transmit FIFO trigger level has been reached. A zero indicates that the Transmit FIFO is below the trigger level. Resets to zero.

0	C5_TXRDY	Channel 5 TXRDY	R

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This bit reflects status of the TXRDY pin on Channel 5 of the UART, which in turn indicates status of the Channel 5 Transmit FIFO. A one indicates that the Transmit FIFO trigger level has been reached. A zero indicates that the Transmit FIFO is below the trigger level. Resets to zero.

Note: For information on setting Receive and Transmit FIFO trigger levels, please refer to the XR16C854 UART data sheet. (The XR16C854 UART data sheet contains a discrepancy in its description of the TXRDY pin. The TXRDY pin does not indicate if at least one empty location is available in Transmit FIFO. Instead, it indicates whether the trigger level is reached as described in the FIFO Ready Register Definition.)

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GISR Global Interrupt Status Register

7	6	5	4	3	2	1	0	Bit
CH8_IRQ	CH7_IRQ	CH6_IRQ	CH5_IRQ	CH4_IRQ	CH3_IRQ	CH2_IRQ	CH1_IRQ	Read
X	X	X	X	X	X	X	X	Write
0	0	0	0	0	0	0	0	Reset

The Global Interrupt Status Register reflects the interrupt status of Channels 1-8.

Each bit reflects the interrupt status on its respective channel. A one indicates an active interrupt. Resets to zero.

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UART-Implemented Registers

Each UART channel contains a set of 15 registers accessible at the base address offsets of its channel. For additional information regarding UART registers, please refer to the Exar XR16C854 datasheet.

Register Name	Register Size	Access Type	Address Offset
RHR	8 bits	Read	0x0000
THR	8 bits	Write	0x0000
TRG	8 bits	Read/write	0x0000*
DLL	8 bits	Read/Write	0x0000**
IER	8 bits	Write	0x0010
FCTR	8 bits	Read/Write	0x0010*
DLM	8 bits	Read/Write	0x0010**
ISR	8 bits	Read	0x0020
FCR	8 bits	Write	0x0020
EFR	8 bits	Read/Write	0x0020*
LCR	8 bits	Write	0x0030
MCR	8 bits	Write	0x0040
XON-1	8 bits	Write	0x0040*
LSR	8 bits	Read	0x0050
XON-2	8 bits	Write	0x0050*
MSR	8 bits	Read	0x0060
XOFF-1	8 bits	Write	0x0060*
SPR	8 bits	Read/Write	0x0070
EMSR	8 bits	Write	0x0070*
XOFF-2	8 bits	Write	0x0070*

Figure 13. UART Register Map

Addresses followed by " * " comprise the Enhanced Register Set and are accessible only when the LCR is set to 0xBF. Addresses followed by " ** " comprise the Baud Rate Register Set and are accessible only when the LCR bit[7] is set to one.

NOTE: The P-Octal uses TXRDY and RXRDY pins to reflect FIFO status instead of the FIFO Ready Registers on the UART.

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Interrupts

Interrupt Architecture

Each of the two UARTs has four interrupt lines, INT A through D. All eight lines are ORed together in the FPGA, gated with the INTENABLE bit in the Control Register, and output to the PCI bus via INTA#.

Each of the eight UART interrupt lines may be monitored via a bit in the Global Interrupt Status Register.

Enabling Interrupts

Following power-up or reset, each UART holds its four interrupt lines tri-stated. In order to avoid spurious interrupts cause by floating signal, it is important that these signals be properly enabled before use. Follow the steps below:

1. On each channel in each UART, set bit 3 of the MCR to enable the interrupt signals
2. Install interrupt handlers as required by the operating system
3. Clear any unwanted interrupting conditions in the UARTS
4. Enable the PCI interrupt by setting bit 2 (INTENABLE) in the Control Register.

Servicing Interrupts

Interrupts are serviced by removing the interrupting condition in the UARTs. No further action is required.

The Global Interrupt Status Register may be used to determine which channels are interrupting to avoid polling each channel.

Disabling Interrupts

To disable interrupts, simply clear bit 2 (INTENABLE) in the Control Register.

Advanced Interrupt Features

Advanced interrupt features must be specifically enabled if they are to be used. Set bit 4 of the EFR of each channel in each UART to one in order to enable hardware flow control interrupts, FIFO trigger levels, clock selection (bit 7 of the MCR), and other features.

The following example illustrates how to enable this bit on channel 3:

1. Write 0xBF to offset 0x0230
   (Enables access to Enhanced Register Set.)
2. Write 0x10 to offset 0x0220
   (Sets EFR Bit-4 to 1.)
3. Write 0x03 to offset 0x0230
   (Exits Enhanced Register Set and sets 8 data bits, 1 stop bit, no parity.)

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User Options

User-Supplied Oscillator

A user-supplied oscillator may be installed in the User Oscillator Location (OSC1) in order to provide baud rates not supported by the standard 7.3728 MHz oscillator.

The user-supplied oscillator must be a HCMOS/TTL 5.0V D.C. device in a four pin, J-lead, surface mount package and must be less than or equal to 24 MHz with a 10% (or better) duty cycle. The SM-990 series from Monitor Products Company are examples of compatible oscillators

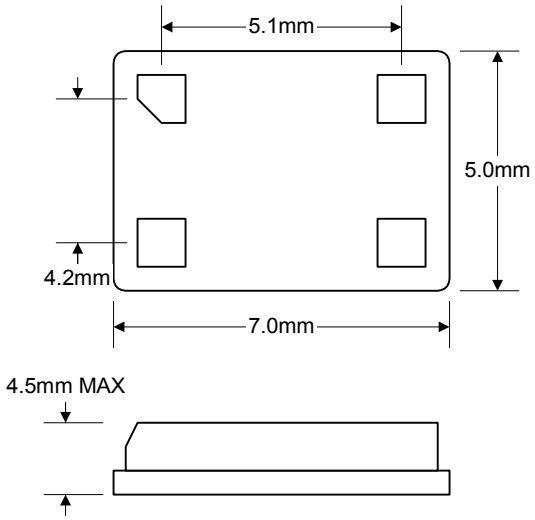


Figure 14. User-Supplied Oscillator Dimensions

User-Switchable Termination Resistors

The Px-Octal-422 contains a user-switchable, 120 Ohm termination resistor network (RN3). The user can connect between positive and negative RxD pins by closing the corresponding SW1 switch. Switch numbers correspond to the channel numbers they terminate.

Note: These resistors are not loaded on the RS-232 and TTL versions.

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Connector Pin Assignments

J1

Connector J1 carries part of the PCI bus to the module. Connector J2 carries the rest of the signals.

J1 Pin	Signal	J1 Pin	Signal
1	Reserved-r	2	Reserved-r
3	Reserved-r	4	Reserved-r
5	–12V	6	TRST#
7	TCK	8	+12V
9	Ground	10	TMS
11	TDO	12	TDI
13	+5V	14	+5V
15	+5V	16	INTA#
17	INTB#	18	INTC#
19	INTD#	20	+5V
21	PRSNT1#	22	Reserved-q
23	Reserved-q	24	+3.3V
25	PRSNT#2	26	Reserved-q
27	Ground	28	Ground
29	Reserved-q	30	Reserved-q
31	Ground	32	RST#
33	CLK	34	+3.3V
35	Ground	36	GNT#
37	REQ#	38	Ground
39	+3.3V	40	Reserved-q
41	AD[31]	42	AD[30]
43	AD[29]	44	+3.3V
45	Ground	46	AD[28]
47	AD[27]	48	AD[26]
49	AD[25]	50	Ground
51	+3.3V	52	AD[24]
53	C/BE[3]#	54	IDSEL
55	AD[23]	56	+3.3V
57	Ground	58	AD[22]
59	AD[21]	60	AD[20]
61	AD[19]	62	Ground
63	+3.3V	64	AD[18]

Figure 15. Connector J1 Pin Assignments

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J2

Connector J2 carries part of the PCI bus to the module. Connector J1 carries the rest of the signals.

J2 Pin	Signal
64	AD[17]
62	C/BE[2]#
60	Ground
58	IRDY#
56	+3.3V
54	DEVSEL#
52	Ground
50	LOCK#
48	PERR#
46	+3.3V
44	SERR#
42	+3.3V
40	C/BE[1]#
38	AD[14]
36	Ground
34	AD[12]
32	AD[10]
30	M66EN
28	Ground
26	AD[08]
24	AD[07]
22	+3.3V
20	AD[05]
18	AD[03]
16	Ground
14	AD[01]
12	+3.3V
10	ACK64#
8	+5V
6	+5V
4	Reserved-r
2	Reserved-r

J2 Pin	Signal
63	AD[16]
61	+3.3V
59	FRAME#
57	Ground
55	TRDY#
53	Ground
51	STOP#
49	+3.3V
47	SDONE
45	SBO#
43	Ground
41	PAR
39	AD[15]
37	+3.3V
35	AD[13]
33	AD[11]
31	Ground
29	AD[09]
27	Ground
25	C/BE[0]#
23	+3.3V
21	AD[06]
19	AD[04]
17	Ground
15	AD[02]
13	AD[00]
11	+3.3V
9	REQ64#
7	+5V
5	+5V
3	Reserved-r
1	Reserved-r

Figure 16. Connector J2 Pin Assignments

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J3

I/O on the P1-Octal-232 is via a flexible I/O Connector J3 as shown in the table below. This connector does not exist on P2-Octal-232. Signal numbers reflect pin assignments when the module is plugged into a carrier board and I/O is accessed via a user connector.

J3 Pin No.	Signal No.	Channel	Direction	Signal
1	1	-	-	GND
2	2	1	Out	TxD
3	3	1	In	RxD
4	4	1	Out	RTS
5	-	-	-	GND
6	5	1	In	CTS
7	6	-	-	GND
8	7	2	Out	TxD
9	8	2	In	RxD
10	-	-	-	GND
11	9	2	Out	RTS
12	10	2	In	CTS
13	-	-	-	GND
14	11	-	-	GND
15	12	3	Out	TxD
16	13	3	In	RxD
17	14	3	Out	RTS
18	-	-	-	GND
19	15	3	In	CTS
20	16	-	-	GND
21	-	-	-	GND
22	17	4	Out	TxD
23	18	4	In	RxD
24	19	4	Out	RTS
25	20	4	In	CTS
26	-	-	-	GND
27	21	-	-	GND
28	22	5	Out	TxD
29	-	-	-	GND
30	23	5	In	RxD
31	24	5	Out	RTS
32	25	5	In	CTS

J3 Pin No.	Signal No.	Channel	Direction	Signal
33	26	-	-	GND
34	-	-	-	GND
35	27	6	Out	TxD
36	28	6	In	RxD
37	-	-	-	GND
38	29	6	Out	RTS
39	30	6	In	CTS
40	31	-	-	GND
41	32	7	Out	TxD
42	-	-	-	GND
43	33	7	In	RxD
44	34	7	Out	RTS
45	-	-	-	GND
46	35	7	In	CTS
47	36	-	-	GND
48	37	8	Out	TxD
49	38	8	In	RxD
50	-	-	-	GND
51	39	8	Out	RTS
52	40	8	In	CTS
53	-	-	-	GND
54	41	-	-	GND
55	42	-	-	+12V
56	43	-	-	NC
57	44	-	-	NC
58	-	-	-	GND
59	45	-	-	NC
60	46	-	-	NC
61	47	-	-	NC
62	48	-	-	NC
63	49	-	-	NC
64	50	-	-	NC

Figure 17. The P1-Octal-232 Flexible I/O Connector J3 Pin Assignments

Pins marked “NC” have no connection.

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I/O on the P1-Octal-422 is via a flexible I/O Connector J3 as shown in the table below. This connector does not exist on P2-Octal-422. Signal numbers reflect pin assignments when the module is plugged into a carrier board and I/O is accessed via a user connector.

J3 Pin No.	Signal No.	Channel	Direction	Signal
1	1	-	-	GND
2	2	1	Out	TxD-
3	3	1	Out	TxD+
4	4	1	In	RxD-
5	-	-	-	GND
6	5	1	In	RxD+
7	6	-	-	GND
8	7	2	Out	TxD-
9	8	2	Out	TxD+
10	-	-	-	GND
11	9	2	In	RxD-
12	10	2	In	RxD+
13	-	-	-	GND
14	11	-	-	GND
15	12	3	Out	TxD-
16	13	3	Out	TxD+
17	14	3	In	RxD-
18	-	-	-	GND
19	15	3	In	RxD+
20	16	-	-	GND
21	-	-	-	GND
22	17	4	Out	TxD-
23	18	4	Out	TxD+
24	19	4	In	RxD-
25	20	4	In	RxD+
26	-	-	-	GND
27	21	-	-	GND
28	22	5	Out	TxD-
29	-	-	-	GND
30	23	5	Out	TxD+
31	24	5	In	RxD-
32	25	5	In	RxD+

J3 Pin No.	Signal No.	Channel	Direction	Signal
33	26	-	-	GND
34	-	-	-	GND
35	27	6	Out	TxD-
36	28	6	Out	TxD+
37	-	-	-	GND
38	29	6	In	RxD-
39	30	6	In	Rxd+
40	31	-	-	GND
41	32	7	Out	TxD-
42	-	-	-	GND
43	33	7	Out	TxD+
44	34	7	In	RxD-
45	-	-	-	GND
46	35	7	In	RxD+
47	36	-	-	GND
48	37	8	Out	TxD-
49	38	8	Out	TxD+
50	-	-	-	GND
51	39	8	In	RxD-
52	40	8	In	RxD+
53	-	-	-	GND
54	41	-	-	GND
55	42	-	-	NC
56	43	-	-	NC
57	44	-	-	NC
58	-	-	-	GND
59	45	-	-	NC
60	46	-	-	NC
61	47	-	-	NC
62	48	-	-	NC
63	49	-	-	NC
64	50	-	-	NC

Figure 18. The P1-Octal-422 Flexible I/O Connector J3 Pin Assignments

Pins marked “NC” have no connection.

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I/O on the P1-Octal-TTL is via a flexible I/O Connector J3 as shown in the table below. Signal numbers reflect pin assignments when the module is plugged into a carrier board and I/O is accessed via a user connector.

J3 Pin No.	Signal No.	Channel	Direction	Signal
1	1	-	-	GND
2	2	1	Out	TxD
3	3	1	In	RxD
4	4	1	Out	RTS
5	-	-	-	GND
6	5	1	In	CTS
7	6	-	-	GND
8	7	2	Out	TxD
9	8	2	In	RxD
10	-	-	-	GND
11	9	2	Out	RTS
12	10	2	In	CTS
13	-	-	-	GND
14	11	-	-	GND
15	12	3	Out	TxD
16	13	3	In	RxD
17	14	3	Out	RTS
18	-	-	-	GND
19	15	3	In	CTS
20	16	-	-	GND
21	-	-	-	GND
22	17	4	Out	TxD
23	18	4	In	RxD
24	19	4	Out	RTS
25	20	4	In	CTS
26	-	-	-	GND
27	21	-	-	GND
28	22	5	Out	TxD
29	-	-	-	GND
30	23	5	In	RxD
31	24	5	Out	RTS
32	25	5	In	CTS

J3 Pin No.	Signal No.	Channel	Direction	Signal
33	26	-	-	GND
34	-	-	-	GND
35	27	6	Out	TxD
36	28	6	In	RxD
37	-	-	-	GND
38	29	6	Out	RTS
39	30	6	In	CTS
40	31	-	-	GND
41	32	7	Out	TxD
42	-	-	-	GND
43	33	7	In	RxD
44	34	7	Out	RTS
45	-	-	-	GND
46	35	7	In	CTS
47	36	-	-	GND
48	37	8	Out	TxD
49	38	8	In	RxD
50	-	-	-	GND
51	39	8	Out	RTS
52	40	8	In	CTS
53	-	-	-	GND
54	41	-	-	GND
55	42	-	-	+12V
56	43	-	-	NC
57	44	-	-	NC
58	-	-	-	GND
59	45	-	-	NC
60	46	-	-	NC
61	47	-	-	NC
62	48	-	-	NC
63	49	-	-	NC
64	50	-	-	NC

Figure 19. The P1-Octal-TTL Flexible I/O Connector J3 Pin Assignments

Pins marked “NC” have no connection.

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J4

I/O on the P2-Octal-232 is via front panel connector, J4. This connector does not exist on P1-Octal-232. The connector is a Champ36 female (AMP 787641-1) with mating part (AMP 787131-2).

Pin No.	Channel	Direction	Function
1	-	-	GND
2	1	Out	TxD
3		In	RxD
4		Out	RTS
5		In	CTS
6	2	Out	TxD
7		In	RxD
8		Out	RTS
9		In	CTS
10	-	-	GND
11	3	Out	TxD
12		In	RxD
13		Out	RTS
14		In	CTS
15	4	Out	TxD
16		In	RxD
17		Out	RTS
18		In	CTS
19	-	-	GND
20	5	Out	TxD
21		In	RxD
22		Out	RTS
23		In	CTS
24	6	Out	TxD
25		In	RxD
26		Out	RTS
27		In	CTS
28	-		GND
29	7	Out	TxD
30		In	RxD
31		Out	RTS
32		In	CTS
33	8	Out	TxD
34		In	RxD
35		Out	RTS
36		In	CTS

Figure 20. The P2-Octal-232 Front Panel Connector J4 Pin Assignments

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I/O on the P2-Octal-422 is via front panel connector, J4. This connector does not exist on P1-Octal-422. The connector is a Champ36 female (AMP 787641-1) with mating part (AMP 787131-2).

Pin No.	Channel	Direction	Signal
1	-	-	GND
2	1	Out	TxD-
3		Out	TxD+
4		In	RxD-
5		In	RxD+
6	2	Out	TxD-
7		Out	TxD+
8		In	RxD-
9		In	RxD+
10	-	-	GND
11	3	Out	TxD-
12		Out	TxD+
13		In	RxD-
14		In	RxD+
15	4	Out	TxD-
16		Out	TxD+
17		In	RxD-
18		In	RxD+
19	-	-	GND
20	5	Out	TxD-
21		Out	TxD+
22		In	RxD-
23		In	RxD+
24	6	Out	TxD-
25		Out	TxD+
26		In	RxD-
27		In	RxD+
28	-		GND
29	7	Out	TxD-
30		Out	TxD+
31		In	RxD-
32		In	RxD+
33	8	Out	TxD-
34		Out	TxD+
35		In	RxD-
36		In	RxD+

Figure 21. The P2-Octal-422 Front Panel Connector J4 Pin Assignments

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P1-Octal-232 Specifications

Form Factor	PC•MIP Type I Single-Wide 8H
PC•MIP Interface	PC•MIP draft specification (ANSI/VITA-29), Revision 0.9
PCI	32-bit, PCI Specification, Revision 2.1
PCI Controller	Altera EPF6016
UART	Two Exar XR16C854
Physical Interface	Texas Instruments SN75C188 and SN75C189
Number of Channels	Eight
Physical Levels Supported	EIA-232
Maximum Data Rate	115 kbaud
Signals Supported	TxD, RxD, CTS and RTS
Protocols Supported	Asynchronous UART
Stop Bits	Programmable to 1, 1.5, and 2
I/O Access	Flexible I/O connector for rear-panel access
FIFO	128 bytes for transmit, 128 bytes for receive per channel
Dimensions	47.0 mm x 90.0 mm
Weight	0.027 kg (0.065 lb)
Power Requirements	+3.3 VDC, 110 mA typ operating +5.0 VDC, 80 mA typ operating +12.0 VDC, 60 mA typ operating -12.0 VDC, 60 mA typ operating
Environmental	Operating temperature: 0° to +70° C Humidity: 5% to 95% non-condensing Storage: -40° to +85° C

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P1-Octal-422 Specifications

Form Factor	PC•MIP Type I Single-Wide 8H
PC•MIP Interface	PC•MIP draft specification (ANSI/VITA-29), Revision 0.9
PCI	32-bit, PCI Specification, Revision 2.1
PCI Controller	Altera EPF6016
UART	Two Exar XR16C854
Physical Interface	Dallas Semiconductor DS26C31, DS26C32A
Number of Channels	Eight
Physical Levels Supported	EIA-422
Maximum Data Rate	460.8 Kbaud
Signals Supported	TxD+, TxD-, RxD+, and RxD-
Protocols Supported	Asynchronous UART
Stop Bits	Programmable to 1, 1.5, and 2
I/O Access	Flexible I/O connector for rear-panel access
FIFO	128 bytes for transmit, 128 bytes for receive per channel
Dimensions	47.0 mm x 90.0 mm
Weight	0.027 kg (0.065 lb)
Power Requirements	+3.3 VDC, 80 mA typ operating +5.0 VDC, 280 mA typ operating
Environmental	Operating temperature: 0° to +70° C Humidity: 5% to 95% non-condensing Storage: -40° to +85° C

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P1-Octal-TTL Specifications

Form Factor	PC•MIP Type I Single-Wide 8H
PC•MIP Interface	PC•MIP draft specification (ANSI/VITA-29), Revision 0.9
PCI	32-bit, PCI Specification, Revision 2.1
PCI Controller	Altera EPF6016
UART	Two Exar XR16C854
Physical Interface	TTL-compatible (3.3V)
Number of Channels	Eight
Physical Levels Supported	TTL-compatible (3.3V)
Maximum Data Rate	115 Kbaud
Signals Supported	TxD, RxD, CTS, and RTS
Protocols Supported	Asynchronous UART
Stop Bits	Programmable to 1, 1.5, and 2
I/O Access	Flexible I/O connector for rear-panel access
FIFO	128 bytes for transmit, 128 bytes for receive per channel
Dimensions	47.0 mm x 90.0 mm
Weight	0.027 kg (0.065 lb)
Power Requirements	+3.3 VDC, 40 mA typ operating +5.0 VDC, 40 mA typ operating
Environmental	Operating temperature: 0° to +70° C Humidity: 5% to 95% non-condensing Storage: -40° to +85° C

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P2-Octal-232 Specifications

Form Factor	PC•MIP Type II Single-Wide 8H
PC•MIP Interface	PC•MIP draft specification (ANSI/VITA-29), Revision 0.9
PCI	32-bit, PCI Specification, Revision 2.1
PCI Controller	Altera EPF6016
UART	Two Exar XR16C854
Physical Interface	Texas Instruments SN75C188 and SN75C189
Number of Channels	Eight
Physical Levels Supported	EIA-232
Maximum Data Rate	115 Kbaud
Signals Supported	TxD, RxD, CTS and RTS
Protocols Supported	Asynchronous UART
Stop Bits	Programmable to 1, 1.5, and 2
I/O Access	36-pin Champ Front Panel I/O connector
FIFO	128 bytes for transmit, 128 bytes for receive per channel
Dimensions	47.0 mm x 99.0 mm
Weight	0.029 kg (0.07 lb)
Power Requirements	+3.3 VDC, 110 mA typ operating +5.0 VDC, 80 mA typ operating +12.0 VDC, 60 mA typ operating -12.0 VDC, 60 mA typ operating
Environmental	Operating temperature: 0° to +70° C Humidity: 5% to 95% non-condensing Storage: -40° to +85° C

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P2-Octal-422 Specifications

Form Factor	PC•MIP Type I Single-Wide 8H
PC•MIP Interface	PC•MIP draft specification (ANSI/VITA-29), Revision 0.9
PCI	32-bit, PCI Specification, Revision 2.1
PCI Controller	Altera EPF6016
UART	Two Exar XR16C854
Physical Interface	Dallas Semiconductor DS26C31, DS26C32A
Number of Channels	Eight
Physical Levels Supported	EIA-422
Maximum Data Rate	460.8 Kbaud
Signals Supported	TxD+, TxD-, RxD+, and RxD-
Protocols Supported	Asynchronous UART
Stop Bits	Programmable to 1, 1.5, and 2
I/O Access	Flexible I/O connector for rear-panel access
FIFO	128 bytes for transmit, 128 bytes for receive per channel
Dimensions	47.0 mm x 90.0 mm
Weight	0.027 kg (0.065 lb)
Power Requirements	+3.3 VDC, 80 mA typ operating +5.0 VDC, 280 mA typ operating
Environmental	Operating temperature: 0° to +70° C Humidity: 5% to 95% non-condensing Storage: -40° to +85° C

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Repair

Service Policy

Before returning a product for repair, verify as soon as possible that the suspected unit is at fault; then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if it is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include the return address and telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. SBS Technologies will not be responsible for damages due to improper packaging of returned items. For service of SBS Technologies products not purchased directly from SBS Technologies, contact your reseller. Products returned to SBS Technologies for repair by other than the original customer will be treated as out-of-warranty.

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