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RL4

PowerPC Single Board Computer

Hardware User's Manual

Revision 1.3

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Revision	By	Date	Section	Comments
V0.0	EH	05/24/2000		First Draft
V0.1	EH	07/12/2000	1.3	add power requirements
			2.1, 2.2	new placement plans
			2.8.3	correct board I/O addresses
			3.7	add physical addresses serial ports
			3.11.2	clarify bit MINT3V description
			3.13	correct port addresses
				add bit BITOK in output port
			3.14.1	delete 3.14.1
			3.14.2	correct MCP time periods
			3.14.3	clarify and correct description
			3.14.3.2	delete paragraph
			3.14.3.3	add bit NMI
				correct MCP timings
			3.14.3.4	insert paragraph
			4.1.1	insert placement plan
V1.0	EH	01/05/2001	1.3	MTBF
			2.1,2.2	new placement plans V1.x
			2.5.2	correct J1001/J1000
			3.1	add differences MPC750/755/7400
			3.7	enable/disable drivers of COM3/4
			3.13.1	add /25MHZ bit
			3.13.3	add paragraph
			3.15	delete COP connector J1160
			4.1.2.1	P1001 is not mounted
			4.1.2.3	VIO not used
			4.1.2.4.3	P1400 not mounted
V1.1	EH	02/12/2001	1.4	Add Paragraph “Thermal Behaviour”
			2.14	rewrite section
			2.5	delete tables and refer to factory settings
			2.5.5	clarify BOOTSEL function
			2.7.1	add warning for 64-bit backplanes
			3.1.3.1	clarify handling of BOOTSEL
			3.16	add PMC power requirements
V1.2	EH	03/13/2001	1.4	750/300MHz Processor added
V1.3	MF	10/28/2002		Caution for battery removed
			1.3	Specification updated
				Error Report Form corrected

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Unpacking and Handling Instructions

1. Please read this manual carefully before unpacking the module or fitting it into your system. This will certainly save time and avoid trouble.
2. Please observe the precautions for electrostatic sensitive modules.
3. If the product contains batteries, please do not place the board on conductive surfaces or anti-static plastic or sponge, which can cause shorts and lead to battery or board trace damage.
4. Please do not exceed the specified operational temperatures. Please note that batteries might have temperature restrictions.
5. Keep all original packaging material for future storage or warranty shipments of the board.

Warning

This is a Class A product. In a domestic environment, this product may cause radio interference in which case the user may be required to take adequate measures.

Notes

Drain static electricity before you install or remove any parts. Installing or removing modules without observing this precaution could result in damage to this and/or other modules in your system.

Installation

Use the following steps to install your SBS Technologies hardware.

General Advisories

1. Before installing or removing any board, please ensure that the system power and external supplies have been turned off.
2. Check that the jumpers and piggybacks are correctly configured for your application.
3. Mount the board/piggyback/transition module very carefully. See also additional advisories for VMEbus and CompactPCI products below.
4. Connect all I/O cables.
5. Once you are certain that all modules are correctly fitted into the system and all connections have been made properly, restore the power.

Advisories for VMEbus products

On a standard VMEbus backplane, remove the jumpers on the IACKIN - IACKOUT interrupt daisy chain (1 jumper) and on the BGxIN - BGxOUT busgrant daisy chains (4 jumpers) for the slot where the board is to be mounted. The daisy chain jumpers on the VMEbus backplane should be mounted on all free slots.

Setting jumpers is not necessary for the SBS Technologies Auto-Daisy-Chain VMEbus backplane (order number: VBUSxxAD). Please read additional advisories within the manual.

A board with system controller functionality must be fitted at slot 1 (for SBS Technologies products, see additional notes within the manual).

Advisories for Compact PCI products

Mount the CPU board carefully on the first CPCIbus slot (called system slot). Note that on some boards connectors are used for I/O purposes which must not be inserted into a CPCIbus backplane. A transition module must be used instead.

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Warranty

SBS Technologies grants the original purchaser of SBS Technologies products a warranty of 12 month from the date of delivery. For details refer to the "Allgemeine Geschäftsbedingungen".

In the event of repair, please return the product together with additional written information about

the kind of defect
is the defect restricted to certain environmental conditions
what was the hardware environment when the defect appeared
were there input signals; if yes which
warranty/no warranty repair

Please use the error report form sheet at the end of this manual and use the original packing material to avoid damage. Otherwise warranty may be lost.

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1 General Information

This manual applies to the RL4 single board computer version 1.0 and above, until superseded.

1.1 Features

Microprocessor	PowerPC 750/755/7400 300MHz – 400 MHz and higher in BGA package
Cache RAM	32 Kbytes instruction + 32 Kbytes data first level cache, 1Mbyte or 2Mbyte second level cache
DRAM	32 - 128 Mbytes onboard soldered SDRAM running at max. 100MHz
Chipset	Motorola MPC107 max. 100MHz Memory and 33MHz PCI bridge Two DMA channels for memory and PCI transfers
Flash ROM	8Mbyte Boot-Flash 8-bit wide 32 or 64 Mbytes 64-bit wide extended Flash memory
nvSRAM	32 kbytes SRAM with STK14C88 device. Automatic data loading and storing on power-up/down
PMC slot	One PCI mezzanine connector for standard PMC as well as for rugged PMC, some of PMC I/O signals available at the rear connector
Fast Ethernet	High speed PCIbus Ethernet controller (Intel 82559ER) with 10BaseT and 100BaseTX interface and integrated FIFO buffer
RTC	114 byte non-volatile RTC, MC146818 compatible RTC with additional feature (Y2K compatible), external battery supply from rear I/O
Serial I/O	Four serial channels with two async. 16550 compatible full duplex RS-232 channels, transfer rates up to 1.5 Mbaud and two async. 16550 compatible full duplex RS-422/485 channels, transfer rates up to 1.5 Mbaud
CPCI	Compact PCI Bus with Texas Instrument PCI2050 PCI-PCI bridge for minimum bus load PICMG 2.0 R3.0 complaint CPCI local bus standard, 32bit interface for up to 7 slots at 25 or 33Mhz.
Watchdog	Watchdog activates reset under software control
JTAG Interface	JTAG interface for processor, chipset, PCI/PCI bridge controller, and PMC slot at rear P1 connector
COP Interface	Processor debug interface for external emulator at rear I/O
LED Indicator	BITOK user LED at rear I/O

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Front Panel	PMC slot
Backpanel I/O	COM1-4, Reset, Watchdog, PMC I/O, Ethernet, Boot Select, JTAG, COP, Transition module RLTM available for compatible connectors
Power	Dual Power Supply 3.3V and 5V
Conduction Cooling	Conduction Cooling available
Conformal Coating	The board is optionally conformal coated to protect against humidity and fungus

1.2 Board Types

Contact SBS Technologies.

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1.3 Specification

- PCB — FR4 Multilayer
- Size — Total size: 1 board : 3U, 4 TE
- Dimensions — PCB: 100 mm x 160 mm x 20 mm
- Weight: — 270g with cooling plate
- Conduction Cooling — The board is optionally conduction cooled with an aluminum alloy cooling plate at top of the devices. See RL4 Thermal Report for calculation. Contact SBS for thermal report.
- Power Requirement — +5V +/-5%, +3.3V +/-5%
- Power Consumption

The table below helps to calculate the power consumption of each RL4 system. For measurement, the RL4 is mounted on a CPCI backplane, without any other I/O interfaces. The power is measured during VxWorks Boot prompt and no application software is running.

	Typical Power +5.0V	Typical Power +3.3V	Typical Overall	Description
RL4	4.0 W	2.0W	6.0 W	PowerPC755 200 MHz, 50 MHz Bus, 32 MB Memory, 1MB Cache
RL4	7.0 W	2.2W	9.2 W	PowerPC755 400 MHz, 100 MHz Bus, 64 MB Memory, 1MB Cache
RL4	8.0W	2.2W	10.2W	PowerPC750 500 MHz, 100 MHz Bus, 64 MB Memory, 1MB Cache

- External Battery Input — input range 2.7 – 4.5 V, max. current (@3.0V) 1µA

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Environment	C-Style	I-Style	N-Style
High Temperature [°C]			
Operating[1]	+70°C	+85°C	+85°C
Storage	+85°C	+85°C	+85 □C

☐ Note 1: Please refer to section 1.4 Thermal Behaviour for more information.

Low Temperature			
Operating	+0°C	-40 □C	-40 □C
Storage	-40°C	-40 □C	-40 □C

Rel. Humidity			
Operating	up to 95% @ 40°C, non-condensing		
Storage	up to 95% @ 40°C, non-condensing		

Altitude			
Operating	4.5 km	4.5 km	vacuum
Storage	12 km	12 km	vacuum

☐ Note: 4.5 km (15,000 ft.), 12 km (40,000 ft.)

Shock			
Amplitude	12g	12g	100g / 40g
Duration	6 ms	6 ms	6 ms / 11 ms

☐ Note: half sine (peak), 3 axis up & down, 5 hits / direction

Vibration (operating)			
Spectrum	5 to 100 Hz	5 to 100 Hz	5 to 2000 Hz
Acceleration	$2g_{rms}$	$2g_{rms}$	$14g_{rms}$

☐ Note: random, 30 min , 3 axis

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1.4 Thermal Behaviour

This section describe in short the thermal behaviour of the RL4 boards. For more detailed information, please check the thermal report document of the RL4 (Doc Ref TR-HW-002).

1.4.1 Thermal Condition C-Style

The thermal condition of the C-Style RL4 is used to be in an airstream cooled environment. This means the maximum ambient temperature can only achieved with sufficient airflow. The table below gives the maximal ambient temperature of the CPU (hottest spot) related to the forced airflow under worst case power condition..

☐ Note: Please notify that the airflow must be valid for the complete board surface (front and backside) to achieve the ambient temperature and a mounted PMC Module changes the thermal behaviour of the RL4 board.

Device	P_{max}	Maximal Ambient Temperature at Airflow							
		0m/s	0,5m/s	1,0m/s	1,5m/s	2,0m/s	2,5m/s	3,0m/s	4,0m/s
Processor MPC750 300	6.1W	58□C	65□C	72□C	76□C	79□C	81□C	83□C	85□C
Processor MPC750 400	8.0W	53□C	61□C	68□C	72□C	76□C	78□C	81□C	82□C
Processor MPC750 500	8.25W	48□C	57□C	64□C*	64□C*	64□C*	64□C*	64□C*	64□C*
Processor MPC755 300	5.4W	58□C	65□C	71□C	76□C	79□C	81□C	83□C	85□C
Processor MPC755 400	7.1W	52□C	60□C	67□C	72□C	75□C	77□C	80□C	81□C
Processor MPC7400 400	12.7W	30□C	42□C	52□C	59□C	64□C	68□C	71□C	74□C

* Junction temperature of MPC750 500MHz is limited to 65□C.

It is not recommended to operate the RL4 system without sufficient airflow. As the thermal situation depends on the actual power consumption and a defined airflow, which may be difficult to determine, we suggest following procedure:

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The hottest spots at the RL4 board are the CPU and devices under the heatsink. Under worstcase power consumption the heatsink surface shall not exceed the specified value, which can be found in the table below.

Device	$T_{case/max}$	$T_{heatsink\ max}$
Processor MPC750 300MHz	105°C	96°C
Processor MPC750 400MHz	105°C	94°C
Processor MPC750 500MHz	65°C	63°C
Processor MPC755 300MHz	105°C	96°C
Processor MPC755 400MHz	105°C	93°C
Processor MPC7400 400MHz	105°C	91°C

To determine the maximum possible ambient temperature (T_{amax}) the user shall take the maximum heatsink temperature from Table above and measure the current ambient temperature (T_{ameas}) and the heatsink surface temperature ($T_{heatsinkmeas}$) under typical application and actual airflow in the system rack. The maximum ambient temperature is then calculated with following formula.

$$T_{amax} < T_{heatsinkmax} - T_{heatsinkmeas} + T_{ameas}$$

Another way to determine the temperature limit is to read the die temperature of the CPU and stay below the 105°C in any circumstances.

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1.4.2 Thermal Condition N-Style

The thermal condition of the N-Style RL4 is used to be in conduction cooling environment. That means the base is not related to the ambient temperature but to the maximum card edge temperature.
The table below gives the maximal junction temperature at 85□C card edge temperature and worst case power condition.

The RL4 with conduction cooling has for all critical components a temperature below the maximum specified values. As all calculation are performed under worst case (mechanical) and worst case (power consumption) conditions, this will give more margins in real life.

□ Note: Please notify that a mounted PMC Module will change the thermal behaviour of the RL4 board.

Device	Part Designator	Tjunction max	Tjunction @ 85□C card edge	Comment
Processor MPC755 200MHz	U1100	105°C	92°C	compliance
Processor MPC750 300MHz	U1100	105°C	95°C	compliance
Processor MPC750 400MHz	U1100	105°C	98°C	compliance
Processor MPC755 300MHz	U1100	105°C	95°C	compliance
Processor MPC755 400MHz	U1100	105°C	98°C	compliance
Processor MPC7400 400MHz	U1100	105°C	104°C	compliance
Chipset MPC107 @ 50MHz	U1300	105°C	92°C	compliance
Chipset MPC107 @ 100MHz	U1300	105°C	96°C	compliance
cPCI Bridge PCI2050	U7200	115°C	98°C	compliance
Ethernet GD82559ER	U5000	105°C	98°C	compliance
2.5V Regulator MIC39100 @ 50MHz	U1240	125°C	104°C	compliance
2.5V Regulator MIC39100@ 100MHz	U1240	125°C	120°C	compliance
Clock PLL ICS9159-14	U1000	105°C	95°C	compliance
nvSRAM STK14C88	U2000	105°C	96°C	compliance

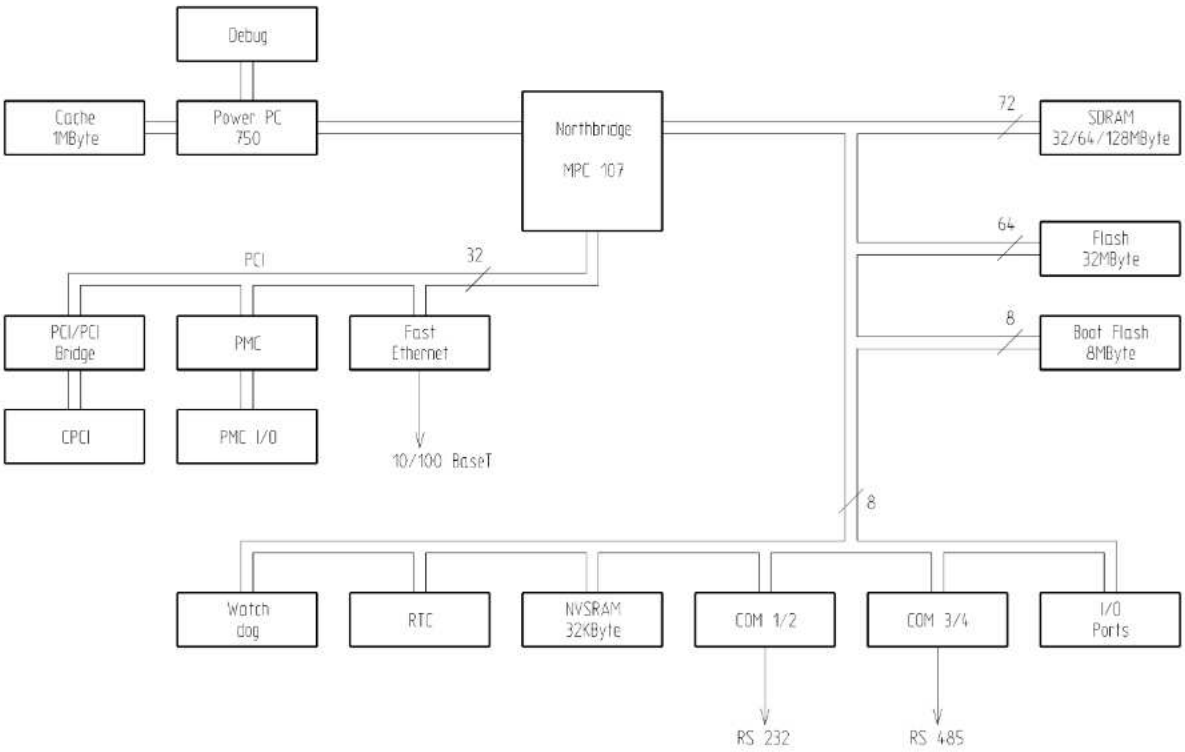
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Strata Flash E28F640J3	U1500	105°C	92°C	compliance
Cache SRAM 80Mhz MCM96P73TQ3.0	U1150, U1151	105°C	99°C	compliance
Cache SRAM 133Mhz MCM96P73TQ3.0	U1150, U1151	105°C	104°C	compliance
SDRAM	U1400 – U1404	105°C	103°C	compliance
PLD Xilinx XC95144XL	U1900	105°C	102°C	compliance
Flash 28F640	U1501-U1503	105°C	97°C	compliance
RS232 Driver MAX232	U2301	105°C	99°C	compliance

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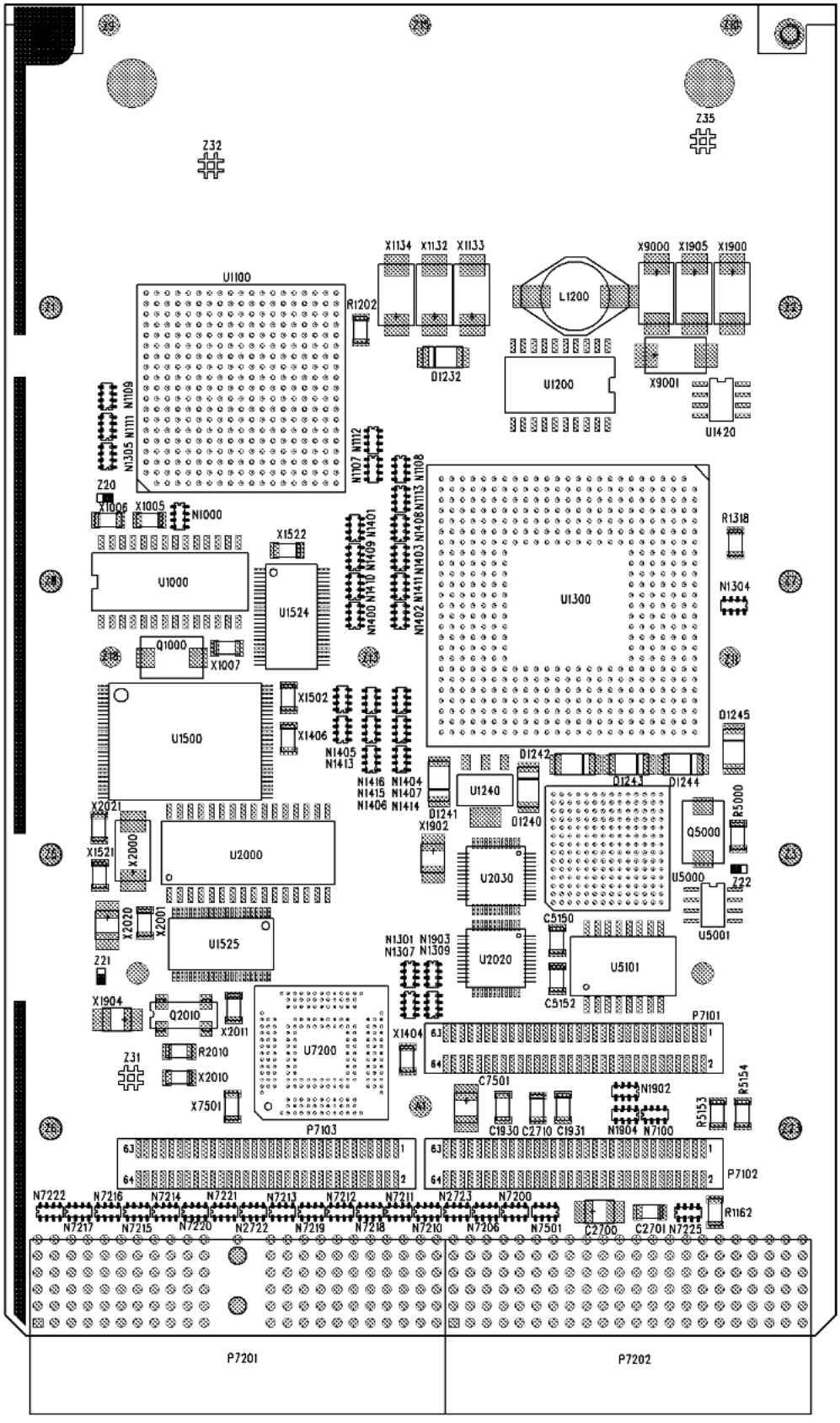
2 Hardware Installation

The RL4 is a single slot CPCI controller using the PowerPC 750 or pin compatible microprocessor like PowerPC 755 or PowerPC 7400. It is equipped with all functions a conventional system controller can only offer with several add-on cards. Extension boards can be connected via the CPCI interface and one PMC interface. The minimized board size and the number of interfaces and functions makes the RL4 suitable for many applications.



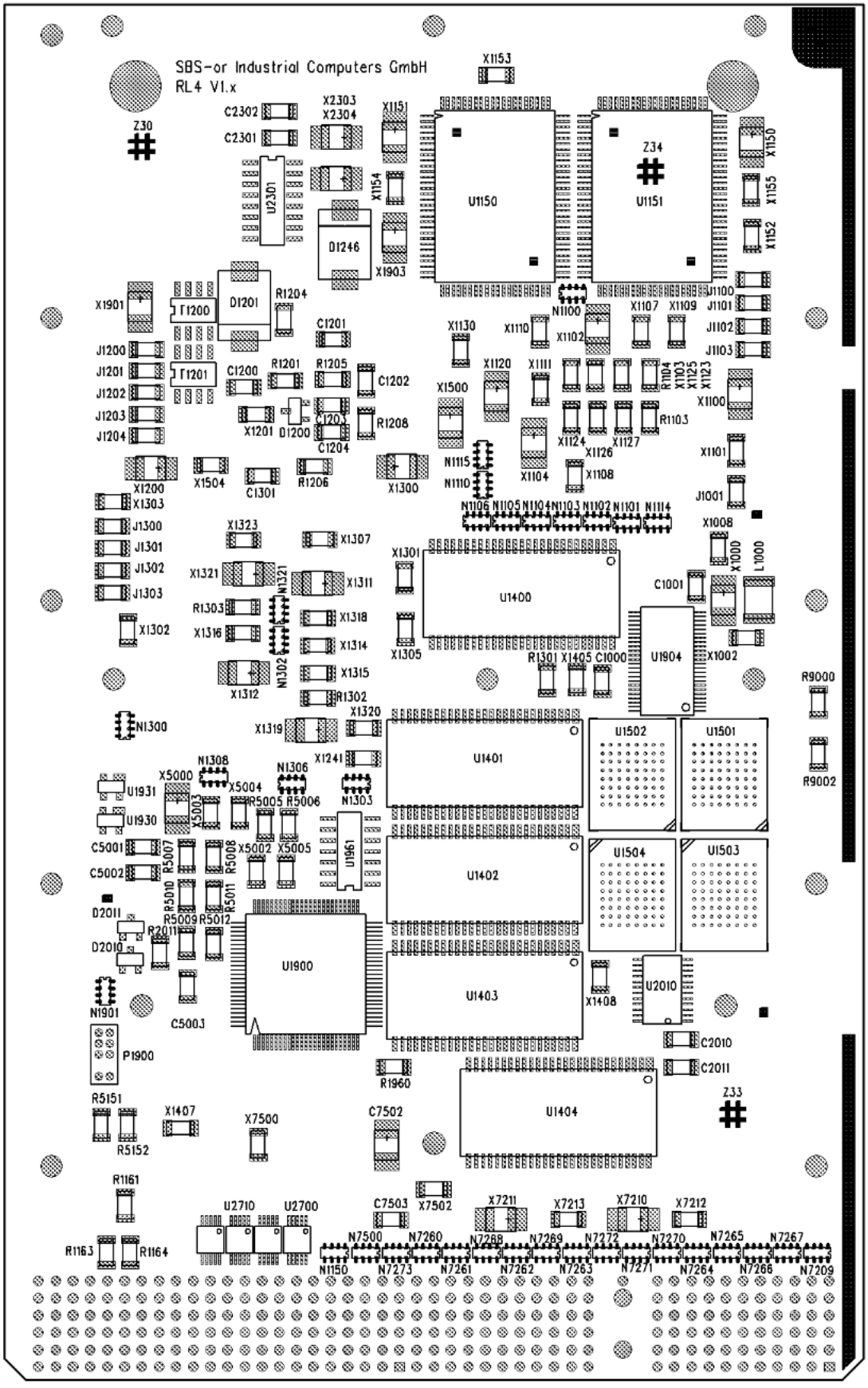
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2.1 Placement Plan Component Side



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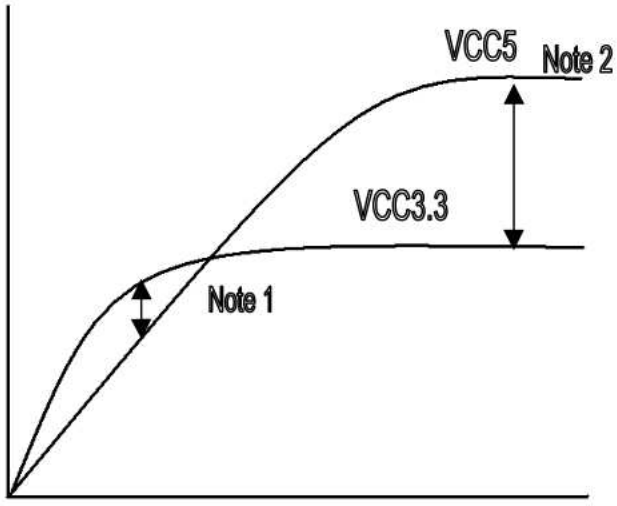
2.2 Placement Plan Solder Side



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2.3 Power Supply

For power supply the RL4 uses two voltage rails 3.3V and 5V from the CPCI bus connector. For power consumption see section 1.3 Specification. Cautions about the sequencing of the external voltages (3.3V and 5V) are necessary for long term reliability of the board.
Diodes in the power supply between 5V and 3.3V may regulate the maximum potential differences.



Note 1: VCC3.3 must not exceed VCC5 by more than 0.6V at any time including power-on/off.
Note 2: VCC5 must not exceed VCC3.3 by more than 3.6V at any time including power-on/off.

The RL4 takes care for the sequencing of internal generated voltages (2.5V and processor core voltage).

2.4 Status BITOK (LED)

The RL4 has provisions for one status LED, which has the function as listed below. It is accessible at P7202 (P2)-C10. The output is able to drive max. 8mA, a serial resistor of 220Wis already implemented on the board.

Signal	Function
BITOK	BITOK Status: This signal is low during reset and high when the reset is inactive, BITOK will be switched low when processor has successful performed the initialization routine. Can be also used for other status indication. See section 3.13.2 Status Output Port for controlling.

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2.5 Socket Installation

Only the BOOTSEL selection configuration is available at the rear I/O. All other options for voltages and clock speed configurations are provided with soldered jumpers (zero Ohm resistors) and are assembled at factory.

2.5.1 Processor Voltage Configuration

This configuration defines the PowerPC CPU core voltage. The CPU core voltage is generated by a DC/DC converted from the 5V power rail. The CPU core voltage depends from vendor and frequency and must be selected according the CPU specification. It is set at factory.

2.5.2 Master/PCI Clock

The master clock can be selected between 25MHz and 33Mhz. The master clock is the base frequency of the RL4 board and the PCI bus. It is set at factory.

The selected frequency can be obtained at bit 7 of the Status Input Port (see section 3.13.1 Status Input Port).

2.5.3 Chipset Frequency

The chipset frequency is a multiple of the master/PCI clock and is used for memory and CPU clock. The clock is set by configuration inputs at reset time.
The selected chipset frequency can be obtained at bit 3..0 at the Status Chipset Frequency input port (see section 3.13.3 Status Chipset Frequency Factor).

2.5.4 CPU Core Frequency

The internal core frequency of the PowerPC is a multiple of the chipset clock and is set by factory set configuration inputs at reset time. The setting can be read from a status register inside the CPU

The table below gives samples of chipset frequencies to core frequencies.

Factor	Core Frequency at				
	25Mhz	50Mhz	75 MHz	83.3Mhz	100Mhz
2			150 MHz	166 MHz	200 MHz
3		150 MHz	225 MHz	250 MHz	300 MHz
3.5		175 MHz	262 MHz	292 MHz	350 MHz
4		200 MHz	300 MHz	333 MHz	400 MHz
4.5		225 MHz	337 MHz	375 MHz	450 MHz
5		250 MHz	375 MHz	417 MHz	500 MHz
5.5		275 MHz	412 MHz	458 MHz	
6	150 MHz	300 MHz	450 MHz	500 MHz	
6.5	162.5 MHz	325 MHz	487 MHz		
7	175 MHz	350 MHz	525 MHz		
7.5	187.5 MHz	325 MHz			
8	200 MHz	400 MHz			
9	225 MHz	450 MHz			
10	250 MHz	500 MHz			

2.5.5 Jumper Configuration

There is one accessible jumper on the rear I/O. The signal BOOTSEL at P7202-d4 selects the booting source. The boot behaviour depends on the software installed in the boot flash. The boot software is responsible for the evaluation of the BOOTSEL jumper.

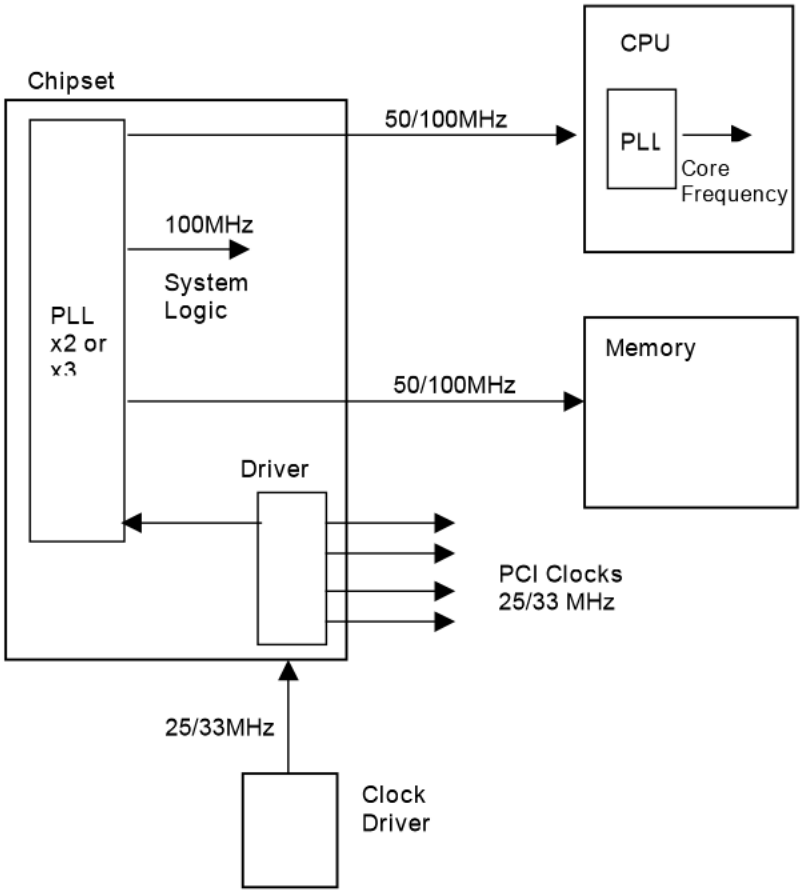
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The value of the signal can be read at Status Input Port Bit 5.

BOOTSEL open	BOOTSEL tied to GND
BOOTSEL is read as a one.	BOOTSEL is read as a zero..

2.6 Clocking

The CPU, chipset, memory and PCI clocks depend on each other. One master clock of 25 or 33MHz is provided by a clock chip. This master clock feeds the chipset and buffered outputs are used for the PCI devices. The chip set PLL synchronizes the PCI clock to the system logic clock. The system logic clock is a multiple of (x1, x1.5, x2, x2.5, x3, x4) of the PCI clock and is set by the factory according to the order number. The system clock is used for CPU and memory clock. The core logic of the CPU is running with a multiple of the CPU clock. The multiple factor is set by the factory according to the used CPU speed.



2.7 Connectors

The connectors P7201 (P1) and P7202 (P2) carry the signals for the CPCI bus as well as all the I/O signals of the RL4. For easy connection of the I/O signals to standard connectors a transition module is available from SBS Technologies. The order number for the transition module is RLTM. See Appendix A for a complete description.

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2.7.1 CPCI bus Connector P1/P2 (P7201, P7202)

The following table lists the pin assignments of connector P7201 (P1) and P7202P1 (P2). The pinning is compliant to PICMG 2.0 R3.0 section "5.3.4 System Slot Rear Panel I/O". Do not use the RL4 board together with a 64-bit connector backplane.

No.	A	B	C	D	E	F
P1-1	+5V	-12V	\JTAG_RST	+12V	+5V	GND
P1-2	JTAG_TCK	+5V	JTAG_TMS	JTAG_TDO	JTAG_TDI	GND
P1-3	\INTA	\INTB	\INTC	+5V	\INTD	GND
P1-4	nc	GND	V_I/O	nc	nc	GND
P1-5	nc	nc	\PCI_RST	GND	\GNT0	GND
P1-6	\REQ0	GND	+3.3V	PCICLK0	AD31	GND
P1-7	AD30	AD29	AD28	GND	AD27	GND
P1-8	AD26	GND	V_I/O	AD25	AD24	GND
P1-9	\C/BE3	GND	AD23	GND	AD22	GND
P1-10	AD21	GND	+3.3V	AD20	AD19	GND
P1-11	AD18	AD17	AD16	GND	\C/BE2	GND
P1-12-14	Key Area					
P1-15	+3.3V	\FRAME	\IRDY	GND	\TRDY	GND
P1-16	\DEVSEL	GND	V_I/O	\STOP	\LOCK	GND
P1-17	+3.3V	nc	nc	GND	\PERR	GND
P1-18	\SERR	GND	+3.3V	PAR	\C/BE1	GND
P1-19	+3.3V	AD15	AD14	GND	AD13	GND
P1-20	AD12	GND	V_I/O	AD11	AD10	GND
P1-21	+3.3V	AD9	AD8	M66EN**	\C/BE0	GND
P1-22	AD7	GND	+3.3V	AD6	AD5	GND
P1-23	+3.3V	AD4	AD3	+5V	AD2	GND
P1-24	AD1	+5V	V_I/O	AD0	\ACK64*	GND
P1-25	+5V	\REQ64 *	\ENUM	+3.3V	+5V	GND
P2-1	PCICLK1	GND	\REQ1	\GNT1	\REQ2	GND
P2-2	PCICLK2	PCICLK3	\SYSEN**	\GNT2	\REQ3	GND
P2-3	PCICLK4	GND	\GNT3	\REQ4	\GNT4	GND
P2-4	V_I/O	COP_TDO	\COP_QACK	BOOTSEL	COP_TDI	GND
P2-5	\COP_RST	\QREQ	WDG_REL	S3_TXD-	S3_TXD+	GND
P2-6	S1_TXD	S1_RXD	S3_RXD-	PMCIO01	S3_RTS-	GND
P2-7	\COP_HRST	COP_TMS	PMCIO02	S3_RTS+	S3_CTS-	GND
P2-8	PMCIO03	PMCIO04	S3_RXD+	PMCIO05	S3_CTS+	GND
P2-9	PMCIO06	COP_TCK	PMCIO07	S4_RXD-	S4_RXD+	GND
P2-10	PMCIO08	PMCIO09	BITOK	PMCIO29	S4_TXD-	GND
P2-11	PMCIO11	\CHKST_OUT	PMCIO30	S4_TXD+	S4_RTS+	GND
P2-12	S2_RXD	PMCIO13	PMCIO14	PMCIO15	S4_RTS-	GND
P2-13	S2_TXD	\COP_SRST	PMCIO17	S4_CTS-	S4_CTS+	GND
P2-14	PMCIO18	PMCIO16	PMCIO19	PMCIO21	PMCIO20	GND
P2-15	PMCIO52	PMCIO50	P.U.	\REQ5	\GNT5	GND
P2-16	PMCIO38	PMCIO36	P.U.	GND	PMCIO33	GND
P2-17	PMCIO12	PMCIO10	\RST_BUT	\REQ6	\GNT6	GND
P2-18	PMCIO25	PMCIO26	PMCIO22	PMCIO28	BATT+	GND
P2-19	GND	GND	PMCIO27	ETX-	ERX-	GND
P2-20	PCICLK5	GND	PMCIO23	ETC	ERC	GND
P2-21	PCICLK6	GND	PMCIO24	ETX+	ERX+	GND
P2-22	GA4	GA3	GA2	GA1	GA0	GND

Notes: * Signals \REQ64 and \ACK64 are tied to pull-up.
** Signals \SYSEN and M66EN are tied to GND.

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Signal groups:	
PMC I/O signals:	PMCIO…
Serial 1, 2, 3, 4 signals:	S1....., S2....., S3....., S4.....
Fast Ethernet signals:	E…
COP Debug Interface:	COP_...

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2.7.2 PMC Connectors (P7101-Pn1, P7102-Pn2, P7103-Pn4)

The following table lists the pin assignments of the PMC connectors.

Pin	P7101 (Pn1)		Pin	Pin	P7102 (Pn2)		Pin
01	JTAG_TCK	-12V	02	01	+12V	/JTAG_TRST	02
03	GND	/INTD	04	03	JTAG_TMS	JTAG_TDO	04
05	/INTA	/INTB	06	05	JTAG_TDI	GND	06
07	N.C.	+5V	08	07	GND	RES.	08
09	/INTC	RES.	10	09	RES.	RES.	10
11	GND	RES.	12	11	+5V	+3.3V	12
13	PCLK_PMC	GND	14	13	/PCIRST	GND	14
15	GND	/GNT***	16	15	+3.3V	GND	16
17	/REQ***	+5V	18	17	RES.	GND	18
19	+5V	AD31	20	19	AD30	AD29	20
21	AD28	AD27	22	21	GND	AD26	22
23	AD25	GND	24	23	AD24	3.3V	24
25	GND	C/BE3	26	25	IDSEL **	AD23	26
27	AD22	AD21	28	27	+3.3V	AD20	28
29	AD19	+5V	30	29	AD18	GND	30
31	+5V	AD17	32	31	AD16	C/BE2	32
33	/FRAME	GND	34	33	GND	RES.	34
35	GND	/IRDY	36	35	/TRDY	3.3V	36
37	/DEVSEL	+5V	38	37	GND	/STOP	38
39	GND	/LOCK	40	39	/PERR	GND	40
41	/SDONE*	/SBO*	42	41	+3.3V	/SERR	42
43	PAR	GND	44	43	C/BE1	GND	44
45	+5V	AD15	46	45	AD14	AD13	46
47	AD12	AD11	48	47	GND	AD10	48
49	AD9	+5V	50	49	AD8	3.3V	50
51	GND	C/BE0	52	51	AD7	RES.	52
53	AD6	AD5	54	53	+3.3V	RES.	54
55	AD4	GND	56	55	RES.	GND	56
57	+5V	AD3	58	57	N.C.	RES.	58
59	AD2	AD1	60	59	GND	RES.	60
61	AD0	+5V	62	61	/ACK64 *	3.3V	62
63	GND	/REQ64 *	64	63	GND	RES.	64

N.C.	Not connected
RES.	Reserved. Do not connect anything
+12V/-12V	Only available if supplied by the CPCI backplane.
*	64-bit PCI and cache signals not used, tied high with pull-ups
**	IDSEL wired to AD14
***	Request and grant connected to REQ/GNT2

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Due to the limited rear I/O pins not all 64 PMCIO signals are routed.

Pin	P7103 (Pn4)		Pin
01	PMCIO01	PMCIO02	02
03	PMCIO03	PMCIO04	04
05	PMCIO05	PMCIO06	06
07	PMCIO07	PMCIO08	08
09	PMCIO09	PMCIO10	10
11	PMCIO11	PMCIO12	12
13	PMCIO13	PMCIO14	14
15	PMCIO15	PMCIO16	16
17	PMCIO17	PMCIO18	18
19	PMCIO19	PMCIO20	20
21	PMCIO21	PMCIO22	22
23	PMCIO23	PMCIO24	24
25	PMCIO25	PMCIO26	26
27	PMCIO27	PMCIO28	28
29	PMCIO29	PMCIO30	30
31	nc	nc	32
33	PMCIO33	nc	34
35	nc	PMCIO36	36
37	nc	PMCIO38	38
39	nc	nc	40
41	nc	nc	42
43	nc	nc	44
45	nc	nc	46
47	nc	nc	48
49	nc	PMCIO50	50
51	nc	PMCIO52	52
53	nc	nc	54
55	nc	nc	56
57	nc	nc	58
59	nc	nc	60
61	nc	nc	62
63	nc	nc	64

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2.7.3 COP Interface

The RL4 provides an interface for COP debugging.
The COP interface signals are available at the P2 connector at the rear I/O. See RL4 transition module description for COP interface connector.

Signal	J7202 (P2)
\COP_RST	A5
COP_TDO	B4
COP_TDI	C4
COP_TCK	B9
COP_TMS	B7
\COP_SRST	B13
\COP_QACK	C4
\COP_HRST	A7
\CHKSTOP	B11
\QREQ	B5

For the COP interface pull-up and pull-down resistors are recommended. The following table lists the used resistor values.

Signal	Resistor Value, pull-up or pull down
\COP_HRST	10kW, pull-up
\COP_SRST	10kW, pull-up
COP_TMS	10kW, pull-up
COP_TCK	10kW, pull-up
\COP_RST	1kW, pull-up
COP_TDI	10kW, pull-up
\COP_QACK	1kW, pull-down
\CHKSTOP	10kW, pull-up

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2.7.4 JTAG Interface

A JTAG interface is available for testing the connected devices according IEEE1149.1. The chain of the devices with JTAG interface is implemented in following order.

1. Northbridge MPC107 U1300
2. PCI/PCI Bridge U7400
3. PMC Module

The JTAG interface signals are available at the P7201 (P1) connector. See RL4 transition module description for JTAG interface connector.

Signal	P7201 (P1)
JTAG_TDI	E2
JTAG_TCK	A2
JTAG_TDO	D2
JTAG_RST	C1
JTAG_TMS	C2

2.7.5 ISP Programming Interface Connector (P1900)

The RL4 has one PLD U1900 for miscellaneous glue logic. The ISP connector (P1900) provides in-system-programming for maintenance and update. This connector is only useful for manufacturing or development updates and therefore not mounted.

Signal	P1900		Signal
TCK	1	2	GND
TDO	3	4	+5V
NC	5	6	TMS
NC	7	8	NC
TDI	9	10	GND

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2.8 Memory Map (Map B)

The two memory maps Map A (PReP-PowerPC Reference Platform) and Map B (CHRP-Common Hardware Reference Platform) are supported by the MPC107 chipset. After power-up/reset Memory Map B is selected as default map and remains in effect until reprogammed by software. The following sections give a general description of the RL4 address organization.
Please refer to "Motorola MPC107 User Manual" for a complete description or using of the two memory maps.

There are two views for the memory address:

- The memory map as viewed by the processor
- The memory map as viewed by PCI local bus masters.

2.8.1 Processor Memory Map (Map B)

Processor Range		PCI Address Range	Definition
0000_0000	3FFF_FFFF	No PCI cycle [1]	Local Memory space [1,2]
4000_0000	77FF_FFFF	RESERVED	RESERVED
7800_0000	7FFF_FFFF	No PCI cycle	extended ROM space [3]
8000_0000	FCFF_FFFF	8000_0000 – FCFF_FFFF	PCI- Memory space
FD00_0000	FDFF_FFFF	0000_0000 – 00FF FFFF	PCI Memory Space 16Mbyte ISA
FE00_0000	FEBF_FFFF	0000_0000 – 000B_FFFF	PCI I/O space
FEC0_0000	FEDF_FFEF		Config Address Register [4]
FEE0_0000	FEEF_FFFF		Config Data Register
FEF0_0000	FEFF_FFFF	FEF0_0000 – FEFF_FFFF	PCI – Interrupt Acknowledge
FF00_0000	FF7F_FFFF	No PCI cycle	board I/O devices [5]
FF80_0000	FFFF_FFFF	No PCI cycle	base ROM space [6]

Notes:

1. There is a PC compatibility hole between 0000_A000 - 0000_FFFF which can be set either to PCI memory or system memory in a configuration register
2. Maximal RL4 memory space is 128Mbyte (07FF_FFFF)
3. The RL4 has max 64Mbytes extended ROM located at 7C00_0000 – 7FFF_FFFF
4. IDSEL 11=8080_08xx, 12=8080_10xx, ..., 18=8084_00xx.
5. Location of RL4 board specific I/O devices
6. The RL4 has 8Mbytes ROM located at FF80_0000 – FFFF_FFFF

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2.8.2 PCI Memory Map

PCI I/O Transactions Address Range		Proc Address Range	Definition
0000_0000	0000_FFFF	no local memory cycle	PCI - I/O space
0001_0000	007F_FFFF	no local memory cycle	RESERVED
0080_0000	00BF_FFFF	no local memory cycle	PCI - I/O space
00C0_0000	FFFF_FFFF	no local memory cycle	RESERVED

PCI Memory Transactions Address Range		Proc Address Range	Definition
0000_0000	3FFF_FFFF	0000_0000 – 3FFF_FFFF	System memory
4000_0000	77FF_FFFF	no local memory cycle	RESERVED
7800_0000	7FFF_FFFF	7800_0000 - 7FFF_FFFF	extended FLASH/ROM space
8000_0000	FDFF_FFFF		PCI Memory space
FE00_0000	FEFF_FFFF		RESERVED
FF00_0000	FF7F_FFFF	FF00_0000 - FF7F_FFFF	board I/O devices space
FF80_0000	FFFF_FFFF	FF80_0000 - FFFF_FFFF	FLASH/ROM space

2.8.3 Board I/O Devices

The board I/O addresses are specific to the RL4. The 8 bit wide port interface of the MPC107 chipset is used for accessing these I/O devices.

I/O Address Range (Hex)	Function
FF00_0000 – FF00_7FFF	32kByte nonvolatile SRAM STK14C88
FF00_8000 – FF00_8002	Watchdog and MCP tick registers
FF00_8010 – FF00_8011	Interrupt Control registers
FF00_8020 – FF00_802F	UART Controller 1 ST16C2550 for serial 1 and 2
FF00_8030 – FF00_803F	UART Controller 2 ST16C2550 for serial 3 and 4
FF00_8040 – FF00_8041	Real Time Clock Controller DS1285
FF00_8050 – FF00_8052	Status Input and Status Output Port

2.9 PCI Arbitration

There are four potential PCI bus masters on the RL4:

- Northbridge Motorola MPC107
- Ethernet Controller Intel 82559ER
- PCI/PCI Bridge Texas Instruments PCI2050
- PMC Slot

The arbitration logic is provided by the Northbridge MPC107.

PCI Bus Request	PCI Master
CPU (Internal)	Northbridge
DRQ/GNT 0	PCI/PCI Bridge Texas Instruments PCI2050
DRQ/GNT 1	Ethernet Controller Intel 82559ER
DRQ/GNT 2	PMC Slot

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2.10 PCI-IDSEL

Each PCI device has an unique PCI address/data signal connected to the IDSEL input. The following table provides the IDSEL on the RL4 board. And the address-data for accessing the PCI configuration registers.

IDSEL	PCI Config. Reg Address Data	Device
AD12	8000_60nn	PCI/PCI Bridge Texas Instruments PCI2050
AD13	8000_68nn	Ethernet Controller Intel 82559ER
AD14	8000_70nn	PMC slot

Note: nn represents the address of the configuration register.

2.11 Interrupts

On the RL4 board two devices perform interrupt handling, these are the MPC107 and a programmable logic device. Sources of interrupts may be any of the following:

- Northbridge MPC107 (Timer, DMA, I2C, memory/transfer error interrupts)

- PCI bus (interrupts from PCI devices)
  INTA: PCIbus Interrupt A
  INTB: PCIbus Interrupt B and Ethernet controller
  INTC: PCIbus Interrupt C
  INTD: PCIbus Interrupt D

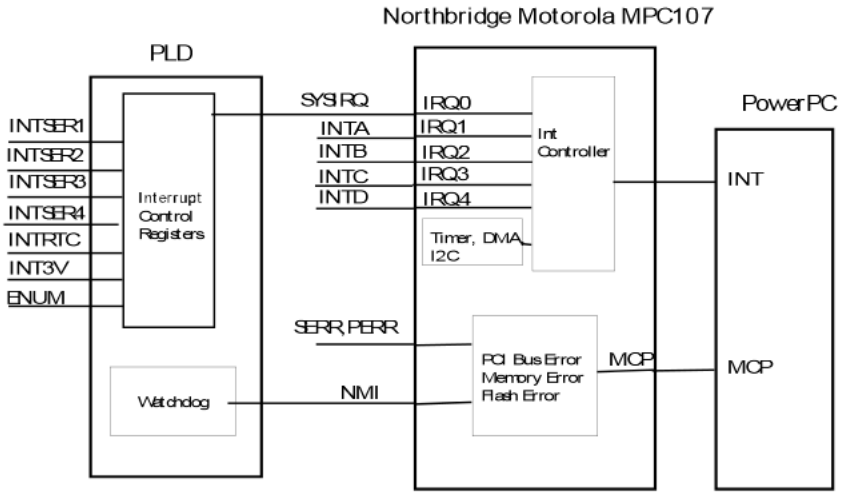
- I/O devices (interrupts from I/O devices and watchdog)

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Interrupt sources from I/O devices:

SERINT1 to SERINT4:	Interrupt from UART devices, indicate receive or transmit data
INTRTC:	Real Time Clock alarm interrupt
INT3V:	Interrupt from power monitor indicates low voltage at the 3.3V power plane (3.3V-10%).
ENUM:	Interrupt from CPCI bus indicates hot swap interrupt
INTA,B,C,D:	PCI interrupts from internal PCI bus, PMC or CPCI bus
NMI:	Watchdog interrupt, which generate an MCP to the CPU
SERR,PERR:	PCI signals, which generate an MCP to the CPU

The following figure shows the interrupt architecture on the RL4.



2.12 DMA

The Northbridge supports two DMA channels for transferring data from local or PCI memory to local or PCI memory. See Motorola MPC107 manual for detail description.

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2.13 Reset

The RL4 has four different sources of reset.

- Power-on reset
- CPCI Reset switch
- Watchdog Timer reset
- Reset from the COP debug interface

The affected devices of the various reset types are listed in the table below:

	Processor	Northbridge	PCI Devices	I/O Devices	CPCIbus
Power-On reset	x	x	x	x	x
CPCI Reset switch	x	x	x	x	x
Watchdog reset	x	x	x	x	x
Reset COP interface	x	x	x	x	x

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2.14 Endian

PowerPC environment is inherently big-endian, but the PCIbus is inherently little-endian. The following section describes some aspects of big- and little-endian bus operations.

Both the processor and the MPC107 chipset support big- and little-endian bit format, but the local processor and the MPC107 should be set for the same endian mode. The current implementation of RL4 is based on the default value of both big-endian. That means the MPC107 maintains the big-endian byte ordering on the PCIbus during the data phase(s) of transactions. The software now must swap the bytes to the correct order for PCIbus transactions. Note that only the bytes in a byte lane are swapped the bit ordering remains unchanged, AD31 is still the most significant bit of the byte in byte lane 3 and AD0 is still the least significant bit of the byte in byte lane 0.

The table below shows the byte lane translation from the big-endian CPU/memory bus to the little-endian PCIbus. No address modification is performed.

Processor Byte Lane	Processor Data Bus Signals	PCI Byte Lane	PCI Address/Data Bits Signals during Data Phase
0	DH(0:7)	0	AD(7:0)
1	DH(8:15)	1	AD(15:8)
2	DH(16:23)	2	AD(23:16)
3	DH(24:31)	3	AD(31:24)
4	DL(0:7)	0	AD(7:0)
5	DL(8:15)	1	AD(15:8)
6	DL(16:23)	2	AD(23:16)
7	DL(24:31)	3	AD(31:24)

Byte transfers are maintained equal for big- and little-endian but for multiple byte data transfer a byte swapping by software must be performed because at a multiple byte data transfer big-endian stores the most significant byte at the lowest numerical address and little-endian the least significant byte at the lowest numerical address.

That means: Big-endian holds the most significant byte at Byte (0).
Little-endian holds the least significant byte at Byte (0).

Example:

Data Type	Memory Location	Big Endian	Little Endian
String "ABCD" Byte-transfer	Byte (0) Byte (1) Byte (2) Byte (3)	'A' 'B' 'C' 'D'	'A' 'B' 'C' 'D'
32 bit integer 12345678	Byte (0) Byte (1) Byte (2) Byte (3)	12 34 56 78	78 56 34 12
Two 16 bit integer 1234 and 5678	Byte (0) Byte (1) Byte (2) Byte (3)	12 34 56 78	34 12 78 56

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3 Function Blocks

3.1 PowerPC Processor

The RL4 board supports the usage of MPC750, MPC755 and MPC7400 PowerPC processors with frequencies from 200MHz to +500MHz and core voltages from 2.5V down to 1.3V.

Major differences between MPC750 and MPC755 visible to programmers and system designer:

- Instruction and data cache locking mechanism added
- Eight additional Block Address Translation registers (BAT)
- Software table search mode added
- Four special-purpose (SPRG) registers added
- Parity generation and detection on L2 address bus added
- Instruction-only mode to L2 cache added
- Private direct map SRAM capability to L2 cache interface added
- PB3-type SRAM support to L2 cache interface added (not used in RL4 design)
- 32-bit data bus mode added
- Bus voltage select (BVSEL) and L2 cache interface voltage select (L2VSEL) added. (not used in RL4 design)

Major differences between MPC750 and MPC7400 visible to programmers and system designer:

- The MPC7400 adds an implementation of the new AltiVec technology instruction set
- Significant improvements in memory subsystem (MSS) bandwidth and offers an optional, high-bandwidth MPX bus interface (not used on RL4 design)
- L2-cache support up to 2 Mbyte
- Implementation of a next generation process technology for core frequency improvement
- Floating-point unit has been improved to make latency equal for double-precision and single-precision operations involving multiplication
- The completion queue has been extended to 8 slots
- Bus voltage select (BVSEL) and L2 cache interface voltage select (L2VSEL) added. (not used in RL4 design)

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3.2 L2 Cache

The L2 cache of 1Mbyte (PowerPC MPC750, 755) or 2Mbyte (PowerPC MPC7400) has a direct interface to the CPU and works with a maximal speed of 200MHz. It consists of Synchronous Pipelined Burst SRAM with an access time <3ns. The L2 cache is parity protected.

3.3 Chipset (Northbridge)

The RL4 uses the MPC107 as chipset, also called Northbridge. The MPC107 provides the memory and PCI interface and integrates additional features, which are controlled by the embedded memory utility block.
PCI and memory configuration registers are accessible by PCI compliant configuration cycles.

Address	Data	Function
FEC0_0000	nn00_0080	PCI configuration address, nn represent the 4 byte aligned address that contains the register address to be accessed
FEE0_0000	xxxx_xxxx	Data transfer read/write to the addressed config register

The embedded utility block provides several features. The registers of these functions are located in a 1Mbyte PCI memory area, which is defined by a configuration register. The power-up routine will set it to FDF0_0000. Following is a list of the embedded utility and the location of the control registers, for complete description see the Motorola MPC107 data manual.

Address	Embedded Function
FDF0_0000 - FDF0_0FFF	Message Unit I2O
FDF0_1000 - FDF0_1FFF	DMA Controller
FDF0_2000 - FDF0_2FFF	Address Translation Unit
FDF0_3000 - FDF0_3FFF	Serial Bus Interface I2C
FDF4_1000 - FDF6_0FFF	EPIC Controller (Timer, Interrupt)
FDFF_F000 – FDFF_FFFF	Watchpoint Monitor

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3.4 DRAM Memory

The RL4 provides 1 bank 72bit wide SDRAM memory with up to 100MHz memory clock. It is controlled by the MPC107 system chip with ECC single-bit error correction and double-bit error detection. The memory uses 4 devices 16bit wide organized SDRAMs and 1 device 8bit wide chip for ECC. The size of the bank can be 32Mbyte, 64Mbyte or 128Mbyte.

3.5 Boot Flash ROM

The RL4 contains an Intel 28F640J3 flash memory device. This provides 8Mbyte of flash memory capacity organized as 8M x 8bit. The Boot Flash ROM is controlled by the MPC107 and is located at FF80_0000 – FFFF_FFFF. On power-up or reset, the PowerPC begins executing code at address FFF0_0100. The address area is fixed and can't be moved so the boot process starts always in the Boot Flash ROM. With the BOOTSEL jumper the Boot program can only determine where the boot program should continue the boot process.

The boot loader program will initialize the RL4 and load the appropriate operating system. For newest version please contact factory.
The Boot Flash ROM programming can be enabled/disabled by an output port VPENBoot. After power on the programming is disabled by the output port. See section 3.13 Status Port for settings. For erasing and reprogramming the Flash device please refer to the software description of the appropriate operating system.

3.6 Extended Flash ROM

The RL4 includes an optional 32/64Mbyte of Flash Memory, which is 64bit wide. The one memory bank consists of 64Mbit Intel 28F640J3 or 128Mbit 28F128J3 Flash Memory. The Extended Flash ROM is controlled by the MCP107 and located at 7C00_0000 – 7FFF_FFFF.
The Extended Flash programming can be enabled/disabled by an output port VPENFlash. After power-on the programming is disabled by the output port. See section 3.13 Status Port for settings For erasing and reprogramming the Flash device please refer to the software description of the appropriate operating system.

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3.7 Asynchronous Serial Ports

The RL4 supports four asynchronous serial ports, which are implemented in two dual UARTs Exar ST16C2550. The UARTs are fully compatible with the NS16450 and NS16550. The UARTs have programmable baud rate generators capable of 50 to 1.5Mbaud. Each UART has an separate interrupt. The UARTs are located at following physical addresses:

UART	Address
COM1	FF00_8020 – FF00_8027
COM2	FF00_8028 – FF00_802F
COM3	FF00_8030 – FF00_8037
COM4	FF00_8038 – FF00_803F

Two of the serial interfaces are buffered through EIA-232-D drivers/receivers and the other two are buffered by RS422/485 drivers/receivers. All signals are routed to the P7202 (P2) connector.

RS232 Serial Interface COM1:

Signal	P7202 (P2)
COM1-TXD	A6
COM1-RXD	B6

RS232 Serial Interface COM2:

Signal	P7202 (P2)
COM2-TXD	A13
COM2-RXD	A12

RS422/485 Serial Interface COM3:

Signal	P7202 (P2)
COM3-TXD+	E5
COM3-TXD-	D5
COM3-RXD+	C8
COM3-RXD-	C6
COM3-CTS+	E8
COM3-CTS-	E7
COM3-RTS+	D7
COM3-RTS-	E6

The drivers for TXD+/- and RTS+/- at COM3 can be enabled/disabled via the Data Terminal Ready output of the COM3 controller. After boot the drivers are disabled.

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RS422/485 Serial Interface COM4:

Signal	P7202 (P2)
COM4-TXD+	D11
COM4-TXD-	E10
COM4-RXD+	E9
COM4-RXD-	D9
COM4-CTS+	E13
COM4-CTS-	D13
COM4-RTS+	E11
COM4-RTS-	E12

The drivers for TXD+/- and RTS+/- of COM4 can be enabled/disabled via the Data Terminal Ready output of the COM4 controller. After boot the drivers are disabled.

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3.8 Counter and Timer

The RL4 has five counters and timers, which can be used for single interrupts, periodic interrupts, and/or polling. Four timers are incorporated in the Motorola MPC107 and one additional timer in the watchdog logic.

Device	Timer	Clock Input	Timer Width	Function
MPC107	Timer 1	1/8 CPUCLK (12.5MHz at 100MHz)	31bit	PCI Interrupt Polling
MPC107	Timer 2	1/8 CPUCLK (12.5MHz at 100MHz)	31bit	PCI Interrupt Polling
MPC107	Timer 3	1/8 CPUCLK (12.5MHz at 100MHz)	31bit	PCI Interrupt Polling
MPC107	Timer 4	1/8 CPUCLK (12.5MHz at 100MHz)	31bit	PCI Interrupt Polling
Watchdog logic	NMI timer	See section 3.14	0.29 ms up to 18 ms	MCP Interrupt

For timer programming please refer to the Motorola MPC107 data manual and Watchdog description section 3.14.1 Watchdog Register Description.

3.9 AutoStore nvSRAM

The RL4 provides 32kbytes non-volatile SRAM with auto store feature on the SIMTEK STK14C88. The nvSRAM can only be accessed via 8 bit operations, accesses with 16bit/23bit/64bit operations will lead to data corruption.
During normal operation, application software just reads and writes the SRAM without special programming algorithm. Upon detection a power down on the +5V supply, an AutoStore cycle is performed and all 32kbytes are automatically transferred from the SRAM to the on-chip EEPROM. The necessary power is stored in an on-board capacitor. At next power-up a recall cycle is performed to transfer the EEPROM content back to the SRAM and normal reads writes can continue. The number of recalls is unlimited the maximum number of store cycles is 1.000.000, and the data retention period is 100 years.
The nvSRAM is physical located at address FF00_0000 to FF00_7FFF.

3.10 Real Time Clock

The RL4 has a Real Time Clock (RTC) Dallas DS1685 chip on-board. It provides a 100-year calendar with century register, alarm function, a timer with periodic interrupt and 242 bytes of general purpose SRAM. The interrupt INTRTC is routed to the interrupt control register in the PLD. In power-off state the RTC must be supplied by a external power at P7202 (P2) e18. This battery supply voltage must be min. 2.7V max. 4.5V. The maximum battery supply current is 1µA (typ 0.5µA).
The RTC has an multiplexed address/data bus.

Address information is written at physical address FF00_8040 (size 8 bit)
Data information can be read/write at physical address FF00_8041 (size 8 bit)

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3.11 Interrupt Control Register

The interrupt controller inside the chipset MPC107 has only five external interrupt request inputs. Four are reserved for PCI interrupts (INTA,B,C,D) and the remaining interrupts must be shared by the SYSIRQ. The RL4 provides interrupt registers in a programmable logic device (PLD) for controlling and masking the interrupt request inputs to the SYSIRQ input.

3.11.1 Interrupt Status Register (ISR)

The interrupt status register reflects the current state of the interrupt request inputs, regardless of the state of the mask register.

Address: FF00_8010

Size: 8 bit

Bit	Name	Write	Read
7	(reserved)	n/a	Undefined
6	ENUM	n/a	1 ENUM int active 0 ENUM int inactive
5	INT3V	n/a	1 Power 3V int latched* 0 Power 3V int inactive
4	RTCINT	n/a	1 RTC int active 0 RTC int inactive
3	SERINT4	n/a	1 COM4 int active 0 COM4 int inactive
2	SERINT3	n/a	1 COM3 int active 0 COM3 int inactive
1	SERINT2	n/a	1 COM2 int active 0 COM2 int inactive
0	SERINT1	n/a	1 COM1 int active 0 COM1 int inactive

Note:
* The interrupt INT3V indicates a low voltage at 3.3V power rail. To detect short power breaks each falling edge of INT3V is latched. To reset the latched interrupt INT3V bit 5 in the mask register (IMR) must be set to 0.

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3.11.2 Interrupt Mask Register (IMR)

The Interrupt Mask Register accomplishes to enable and disable each single interrupt request. A one bit enables the corresponding interrupt request a zero disables the interrupt request.

Address: FF00_8011

Size: 8 bit

Bit	Name	Write	Read	Default
7	(reserved)	Always write as "0"	Undefined	n/a
6	MENUM	1 to enable ENUM interrupt 0 to disable	1 ENUM int enable 0 ENUM int disabled	0
5	MINT3V	1 to enable Power 3V interrupt 0 to disable	1 Power 3V int enable 0 Power 3V int disabled and reset the latched INT3V	0
4	MRTCINT	1 to enable RTC interrupt 0 to disable	1 RTC int enable 0 RTC int disabled	0
3	MSERINT4	1 to enable COM4 Interrupt 0 to disable	1 COM4 int enable 0 COM4 int disabled	0
2	MSERINT3	1 to enable COM3 Interrupt 0 to disable	1 COM3 int enable 0 COM3 int disabled	0
1	MSERINT2	1 to enable COM2 Interrupt 0 to disable	1 COM2 int enable 0 COM2 int disabled	0
0	MSERINT1	1 to enable COM1 Interrupt 1 0 to disable	1 COM1 int enable 0 COM1 int disabled	0

3.12 Power Monitor

The RL4 provides three power monitors.

- +5.0V power monitor: If the +5V power is below +5.0V -10% the RL4 will issue a system reset.
- CPU core voltage: If the CPU core voltage is 10% below or above the selected value the RL4 will issue a system reset.
- +3.3V power monitor: If the +3.3V power is below +3.08V (typ) the INT3V interrupt line is active.

Specification of the Power Monitors:

Power Monitor	Thresholds			Condition
	min	typ	max	
+5V Power Voltage	4.50V	4.63 V	4.75	Ta = -40□C to +85 □C
CPU Core Voltage		+/-10%		Ta = +25 □C
+3.3V Power Voltage	3.00 V	3.08V	3.15V	Ta = -40 □C to +85 □C

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3.13 Status Port

The RL4 has an status input and output port to control miscellaneous functions.

3.13.1 Status Input Port

The Status Input Port is a Read Only 8 bit port.
Address: FF00_8050
Size: 8 bit

Bit	Name	Write	Read	Default
7	/25MHZ	N/A	This bit reflect the selected Master/PCI frequency. If low 25Mhz is selected, if high 33MHz is selected.	n/a
6	STS	N/A	Status of the Extended Flash EPROM's. When zero this bits indicates that a function (program and/or erase) in the flashes is in progress. When this bit is read as one a new function can be started or normal read operation can be performed.	n/a
5	BOOTSEL	N/A	This pin reflects the position of the BOOTSEL The implemented software or boot loader makes the decision how to proceed.	n/a
4	reserved	N/A	not defined	n/a
3	reserved	N/A	not defined	n/a
2	reserved	N/A	not defined	n/a
1	reserved	N/A	not defined	n/a
0	reserved	N/A	not defined	n/a

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3.13.2 Status Output Port

The Status Output Port is a Read/Write register.

Address: FF00_8051
Size: 8 bit

Bit	Name	Write	Read	Default
7-4	(reserved)	N/A	Undefined	n/a
3	BITOK	1 Status LED on 0 Status LED off The Status LED is on during active power-on reset and off when reset is inactive. The LED is then controlled by system boot loader to indicate that the mainboard has started operating. After system boot loader has passed control to the operating system, the Status LED is available for user-defined operations. It is available at the rear connector P2 (P7202-c10).	(last value Written)	0
2	WP_SPD	This bit controls the write protection of the SPD serial EEPROM. When WP_SPD is 1 the content of the serial EEPROM can be overwritten. If the bit is 0 the EEPROM is write protected. After reset this bit is set to 0. It is not recommended to change the content of the SPD EEPROM by the user.	(last value Written)	0
1	VPENFLASH	This bit controls the write protection of the Extended Flash EPROM. When VPEN is 1 the content of the Extended Flash can be overwritten. If the bit is 0 the Extended Flash is write protected. After reset this bit is set to 0.	(last value written)	0
0	VPENBOOT	This bit controls the write protection of the Boot Flash EPROM. When VPEN is 1 the content of the Boot Flash can be overwritten. If the bit is 0 the Extended Flash is write protected. After reset this bit is set to 0.	(last value written)	0

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3.13.3 Status Chipset Frequency Factor

The Status Chipset Frequency Factor Port reflects the setting of the PLL of the MPC107 chipset. This port is read only.

Address: FF00_8052
Size: 8 bit

Bit	Name	Write	Read	Default
7-4	(reserved)	n/a	Undefined	n/a
3-0	PLL107	n/a	Setting of the PLL factor inside the MPC107 chipset. This value depends from the soldered jumpers J1300-J1303 (see section 2.5.3 Chipset Frequency).	-

PLL107[3]	PLL107[2]	PLL107[1]	PLL107[0]	Factor
1	0	0	0	1
1	0	0	1	1.5
0	1	0	0	2
1	0	1	0	2
0	0	1	1	2.5
0	0	0	1	3
0	1	0	1	4

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3.14 Watchdog Monitor and MCP Timer

For security of application software, the RL4 offers a software controlled hardware watchdog capable of issuing a reset signal if its time-out interval has elapsed.
A software programmable interrupt (MCP) timer tick is also available.

3.14.1 Watchdog Register Description

The watchdog issuing a reset signal if the RL4 is running in a time-out due to hardware or application software problem. Since standard software doesn't trigger the watchdog periodically, it is disabled after reset. The watchdog function can be enabled via the Watchdog Control Register WCR. If the watchdog is enabled, it must be reset periodically by reading WCR within 0.5 seconds. Otherwise a reset pulse with a duration of 200 msec is generated to restart the system.
There is also the signal WDG_REL available at P2 (P7202-c5). This signal indicates a watchdog failure to external logic. It is set if the watchdog time is elapsed or it can be set directly by software.

3.14.1.1 Watchdog Control Register (WCR)

Address: FF00_8000

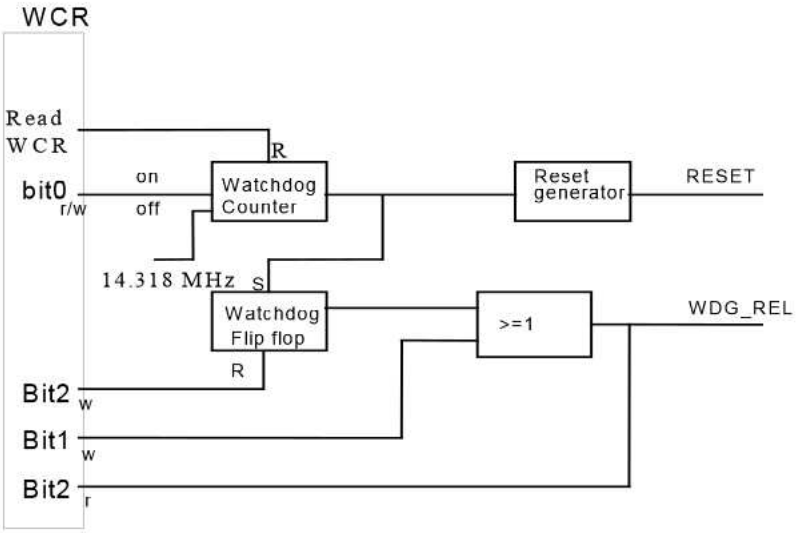
Size: 8 bit

Bit	Name	Write	Read	Default
7-3	(reserved)	Always write as "0"	Undefined	n/a
2	WD_RES	1 Reset Watchdog Flip flop 0 (no effect)	1 Last system reset by Watchdog 0 Last system reset by other cause	n/a
1	WD_SET	1 to set WDG_REL output line 0 to reset WDG_REL output line	1 WDG_REL is set 0 WDG_REL is inactive	0
0	WD_ON	1 to enable Watchdog function 0 to disable	1 Watchdog is enabled 0 Watchdog is disabled	0

Once enabled by setting WD_ON, the Watchdog Timer starts counting down. Software must then read the WCR register in periodic intervals of less than 0.5 seconds. If it fails to do so, the timer expires and a system reset pulse is generated, forcing the system to restart. After a system reboot, software can determine the state of the Watchdog-Reset-Last line WDG_REL (see below diagram) by reading WD_RES whether the system was restarted by the watchdog, or has rebooted (or just booted) within normal operation. The WDG_REL line can be manually set to 1 by writing a 1 to WD_SET.

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The below diagram illustrates WCR operation and watchdog hardware connections.



3.14.2 MCP Timer

The RL4 features a timer, which can trigger a NMI periodically and this will trigger the MCP input of the processor via the MPC107. The timer is programmable in 7 steps from 0.29 ms up to 18 ms. The interrupt MCP must be reset by a dummy write to the MCP Reset Register.
Following periods are programmable via T_SEL[ ] MCPTCR register:

T_SEL2..T_SEL0	MCP period
000	MCP-timer disabled
001	0.286 ms
010	0.572 ms
001	1.144 ms
100	2.289 ms
101	4.577 ms
110	9.154 ms
111	18.309 ms

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3.14.2.1 MCP Ticker Control (MCPTCR)

Address: FF00 8001

Size: 8 bit

Bit	Name	Write	Read	Default
7-4	(reserved)	Always write as "0"	Undefined	n/a
3	NMI	n/a	0- NMI inactive 1- NMI input of MCP107 active	0
2-0	T_SEL	000 to disable MCP Timer 001 for 0.286 ms 010 for 0.572 ms 011 for 1.144 ms 100 for 2.289 ms 101 for 4.577 ms 110 for 9.154 ms 111 for 18.309 ms	(last value written)	000

3.14.2.2 MCP Reset Register

Address: FF00 8002

Size: 8 bit

Bit	Name	Write	Read	Default
7-0	(reserved)	Always write as "0" Reset the NMI input line of the MPC107	Undefined	n/a

3.15 COP Interface

The COP (Common On-chip Processor) interface of the PowerPC processor provides a serial interface for boundary scan and for debug. The COP signals are wired to the P2 connector.

3.16 PMC Interface

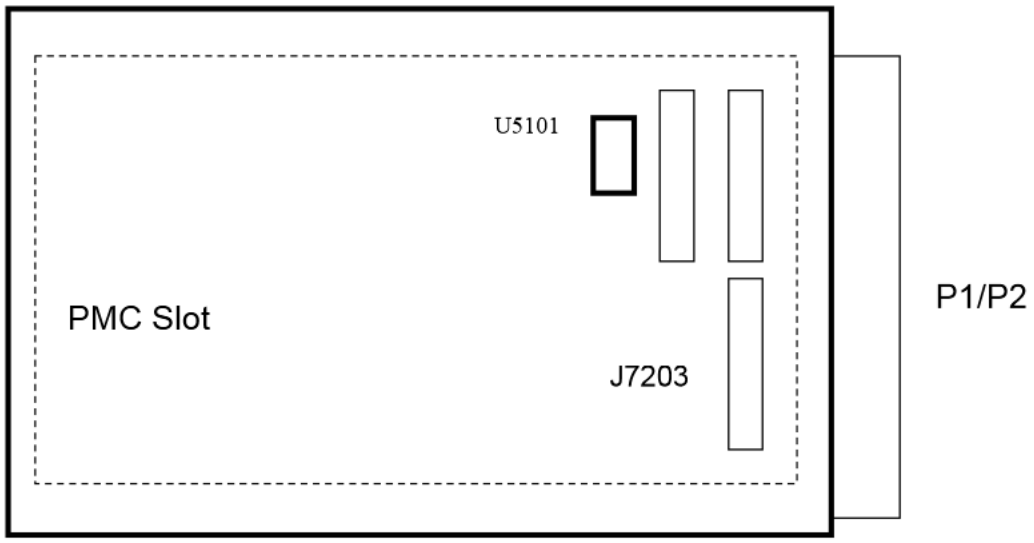
The RL4 allows the installation of one additional PMC module with user defined I/Os on the PMC connector J7103. These PMC I/O signals are routed to P2 connector, but due to the limited signal pins not all PMC I/O are routed.
The PMC bus of the RL4 is +5V/+3.3V signaling tolerant but the PMC are keyed for +5V signaling and VIO of the PMC interface is set to +5V.

Power Requirements:
The RL4 board provides +5V, +3.3V, and +/-12V to the PMC connectors. The +5V and+3.3V are only limited by the max possible power consumption of the PMC module to 15W. The voltage +/-12V are limited by the thickness of the power traces. The cPCI backplane has to provide all voltages.
The maximal current for each voltage is defined in the table below.

Voltage	Max. PMC current
+5V	3A
+3.3V	3A
+12V	0.5A
-12V	0.5A

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☐ Attention: The RL4 is not completely compliant to the mechanical PMC specification. The nominal distance between host side and PMC side surface is 10mm. This is referred to the stacking height. The maximum component height of the host and PMC side is specified to 4.70mm. For thermal and mechanical stiffness reasons the heatsink of the RL4 (N-Style and C-Style) has a height of 4.9mm. This leaves only an air gap of 0.4mm instead of 0.6mm. If a customer uses PMC cards with component heights, which are close to 5mm and conductive materials please contact factory for isolation solutions. Additional one component (the Ethernet transformer U5101) is slightly higher (5.1mm) and can intrude in the PMC component height. See figure below for placement of U5101.



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3.17 CompactPCI Bus

The RL4 provides a PICMG 2.0 R3.0 compliant CPCI local bus standard. For separation to the internal PCI bus a Texas Instrument PCI2050 PCI/PCI bridge is used. The PCI2050 bridge is compliant with the PCI-to-PCI Bridge Specification 1.1. The implementation supports 25 MHz or 33 MHz, 32 bit wide CPCI bus with up to 7 peripheral slots.

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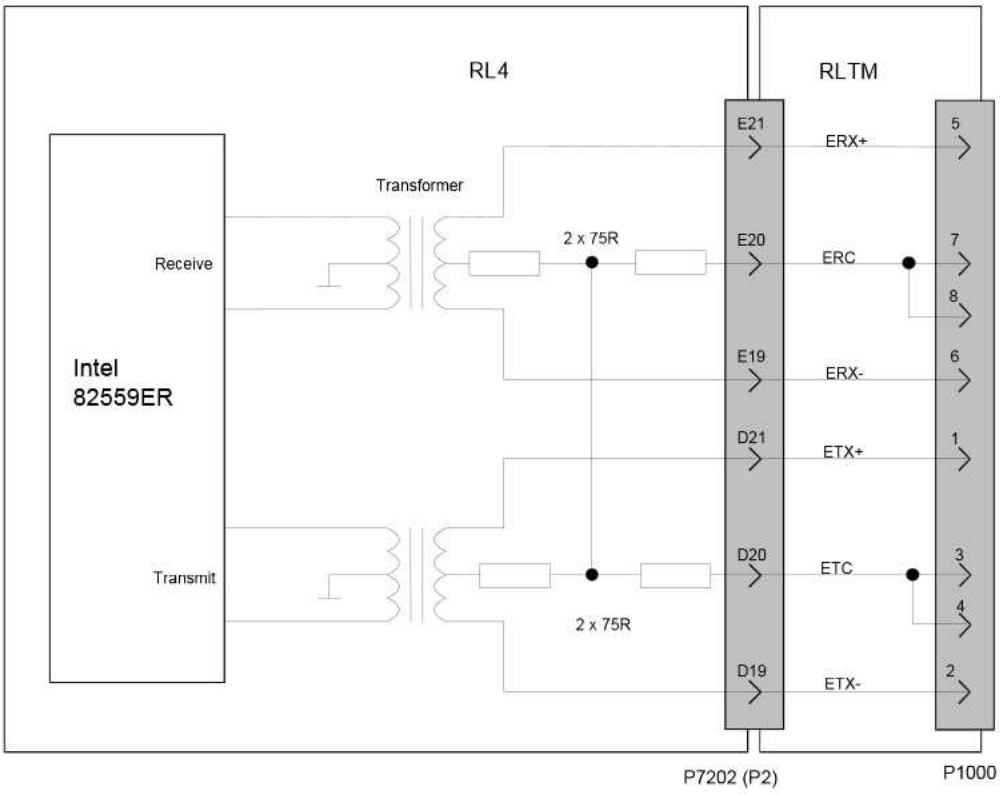
3.18 Ethernet Interface

The Ethernet controller Intel GD82559ER used with the RL4 is a high performance Fast Ethernet PCI controller compatible to the Novell NE2100 and NE1500 standard devices.

For registration and identification of a workstation in a LAN, a unique ID number is assigned to each network card. This Ethernet address resides in a serial EEPROM an is written by the factory. It is strongly recommend not to change the content by the user. The reserved Ethernet address area is:

00 03 EC 46 40 00 to 00 03 EC 46 7F FF

The Ethernet signals are provided at the rear connector P2. If the transition module RLTM is connected to the RL4, the Ethernet signals are routed to the Header P100 as described in the section 4.1.2.4.1 Ethernet Interface P120. For general information please see the sketch below.



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3.19 Additional devices

3.19.1 I2C Bus Device

The RL4 uses a serial 2-wire I2C bus to communicate with the onboard device. The I2C master is the MPC107. For controlling the I2C function please refer to the MPC107 manual.

I2C bus address:

Device	Designator	SMB address
SPD EEprom (*)	U1420	1010000Xb

* The content is written by the factory and it is strongly recommended not to change by the user.

3.19.1.1 SPD EEPROM

For storage of DRAM data a serial EEPROM is implemented on the RL4 board. The 24C04 EEPROM stores the data according the PC SDRAM Serial Presence Detect (SPD) Specification. It is a standard 24C04 type EEPROM with 512 bytes. The SPD EEPROM is protected by a bit in the output port for unintentional writes, see 3.13.2 Status Output Port. More information about writing and reading the contents can be found in the datasheets from the manufacturer (e.g. Microchip Technology, SGS Thomson, Atmel, Catalyst and many others).

3.19.2 Reset Button

A push button, which is connected to P7202 (P2) c17 will issue a hard power-on reset. The reset pin is an open collector type input. The reset signal is active for all subsystems and the complete RL4.

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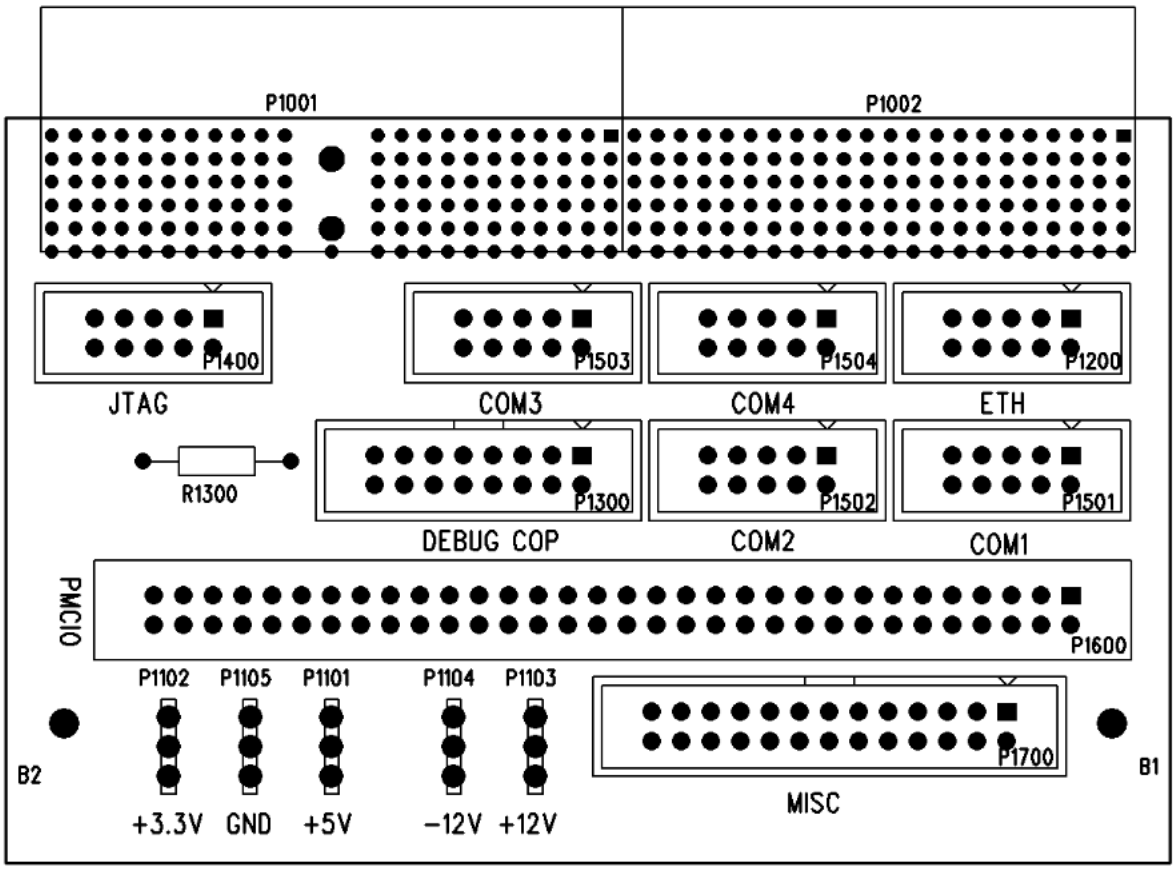
4 Appendix A

4.1 Transition Module RLTM

For easy connection of the I/O signals to standard connectors, a transition module RLTM is available. The RLTM is connected to a CPCI backplane over P2 and distribute the I/O signals to dedicated interface connectors.

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4.1.1 Placement Plan



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4.1.2 Connectors

4.1.2.1 CPCI Connector P1001/P1002 (P1/P2)

No.	A	B	C	D	E	F
P1-1	+5V	-12V	\TRST	+12V	+5V	GND
P1-2	TCK	+5V	TMS	TDO	TDI	GND
P1-3				+5V		GND
P1-4		GND	V_I/O			GND
P1-5				GND		GND
P1-6		GND	+3.3V			GND
P1-7				GND		GND
P1-8		GND	V_I/O			GND
P1-9		GND		GND		GND
P1-10		GND	+3.3V			GND
P1-11				GND		GND
P1-12-14	Key Area					
P1-15	+3.3V			GND		GND
P1-16		GND	V_I/O			GND
P1-17	+3.3V			GND		GND
P1-18		GND	+3.3V			GND
P1-19	+3.3V			GND		GND
P1-20		GND	V_I/O			GND
P1-21	+3.3V					GND
P1-22		GND	+3.3V			GND
P1-23	+3.3V			+5V		GND
P1-24		+5V	V_I/O			GND
P1-25	+5V			+3.3V	+5V	GND
P2-1		GND				GND
P2-2						GND
P2-3		GND				GND
P2-4		COP_TDO	\COP_QACK	BOOTSEL	COP_TDI	GND
P2-5	\COP_RST	\QREQ	WDG_REL	S3_TXD-	S3_TXD+	GND
P2-6	S1_TXD	S1_RXD	S3_RXD-	PMCIO01	S3_RTS-	GND
P2-7	\COP_HRST	COP_TMS	PMCIO02	S3_RTS+	S3_CTS-	GND
P2-8	PMCIO03	PMCIO04	S3_RXD+	PMCIO05	S3_CTS+	GND
P2-9	PMCIO06	COP_TCK	PMCIO07	S4_RXD-	S4_RXD+	GND
P2-10	PMCIO08	PMCIO09	BITOK	PMCIO29	S4_TXD-	GND
P2-11	PMCIO11	\CHKST_OUT	PMCIO30	S4_TXD+	S4_RTS+	GND
P2-12	S2_RXD	PMCIO13	PMCIO14	PMCIO15	S4_RTS-	GND
P2-13	S2_TXD	\COP_SRST	PMCIO17	S4_CTS-	S4_CTS+	GND
P2-14	PMCIO18	PMCIO16	PMCIO19	PMCIO21	PMCIO20	GND
P2-15	PMCIO52	PMCIO50				GND
P2-16	PMCIO38	PMCIO36		GND	PMCIO33	GND
P2-17	PMCIO12	PMCIO10	\RST_BUT			GND
P2-18	PMCIO25	PMCIO26	PMCIO22	PMCIO28	BATT+	GND
P2-19	GND	GND	PMCIO27	ETX-	ERX-	GND
P2-20		GND	PMCIO23	ETC	ERC	GND
P2-21		GND	PMCIO24	ETX+	ERX+	GND
P2-22						GND

In normal configuration P1001(P1) is not mounted.

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4.1.2.2 Power Connectors P110x

These power terminals are only used for supplying the transition module functions. In normal case 5V, 3.3V, +12V, and -12V have no connection to the RL4 board.

P1101	+5V
P1102	+3.3V
P1103	+12V
P1104	-12V
P1105	Ground

4.1.2.3 VIO

In normal configuration P1001 (P1) is not mounted, therefore the VIO of the RLTM is not used.

4.1.2.4 Interface Connectors

4.1.2.4.1 Ethernet Interface P1200

At the 10pin header P1200 the Ethernet 10/100 interface signals are available.

Ethernet Signals	P1200	Remarks
ETX+	1	
ETX-	2	
ETC	3	Center tap of transmit transformer
ETC	4	
ERX+	5	
ERX-	6	
ERC	7	Center tap of receive transformer
ERC	8	
-	9	
-	10	

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4.1.2.4.2 COP Debug Interface P1300

A 16pin header P1300 provides the COP debug interface for the PowerPC processor of the RL4.

COP Interface	P1300	Remarks
COP_TDO	1	
\COP_QACK	2	
COP_TDI	3	
\COP_RST	4	
\QREQ	5	
COPVCC3	6	3.3V supplied via P1102 and 1Kohm resistor
COP_TCK	7	
-	8	
COP_TMS	9	
-	10	
\COP_SRST	11	
-	12	
\COP_HRST	13	
Key	14	
\CHKSTOP	15	
GND	16	

4.1.2.4.3 JTAG Interface P1400

At the 10pin header P1400 the JTAG interface signals are available.

JTAG	P1400
JTAG_TCK	1
GND	2
JTAG_TDO	3
-	4
\JTAG_RST	5
JTAG_TMS	6
-	7
-	8
JTAG_TDI	9
GND	10

P1400 is not mounted at the RLTM.

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4.1.2.4.4 Serial Interfaces P150x

The signals of the four (4) serial interfaces are available at 10pin headers P150x.

4.1.2.4.5 COM1 Serial Interface P1501

COM1	P1501	Remarks
-	1	
-	2	
S1_RXD	3	
-	4	
S1_TXD	5	
-	6	
-	7	
-	8	
GND	9	
VCC	10	supplied via P1101 (+5V)

4.1.2.4.6 COM2 Serial Interface P1502

COM2	P1502	Remarks
-	1	
-	2	
S2_RXD	3	
-	4	
S2_TXD	5	
-	6	
-	7	
-	8	
GND	9	
VCC	10	supplied via P1101 (+5V)

4.1.2.4.7 COM3 Serial Interface P1503

COM3	P1503	Remarks
S3_TXD-	1	
S3_TXD+	2	
S3_RTS-	3	
S3_RTS+	4	
S3_CTS+	5	
S3_CTS-	6	
S3_RXD+	7	
S3_RXD-	8	
GND	9	
VCC	10	supplied via P1101 (+5V)

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4.1.2.4.8 COM4 Serial Interface P1504

COM4	P1504	Remarks
S4_TXD-	1	
S4_TXD+	2	
S4_RTS-	3	
S4_RTS+	4	
S4_CTS+	5	
S4_CTS-	6	
S4_RXD+	7	
S4_RXD-	8	
GND	9	
VCC	10	supplied via P1101 (+5V)

4.1.2.5 PMC I/O Connector P1600

A 64pin header P1600 provides the PMC I/O signals

PMC	P1600		PMC
PMCIO01	1	2	PMCIO02
PMCIO03	3	4	PMCIO04
PMCIO05	5	6	PMCIO06
PMCIO07	7	8	PMCIO08
PMCIO09	9	10	PMCIO10
PMCIO11	11	12	PMCIO12
PMCIO13	13	14	PMCIO14
PMCIO15	15	16	PMCIO16
PMCIO17	17	18	PMCIO18
PMCIO19	19	20	PMCIO20
PMCIO21	21	22	PMCIO22
PMCIO23	23	24	PMCIO24
PMCIO25	25	26	PMCIO26
PMCIO27	27	28	PMCIO28
PMCIO29	29	30	PMCIO30
	31	32	
PMCIO33	33	34	
	35	36	PMCIO36
PMCIO37	37	38	PMCIO38
	39	40	
	41	42	
	43	44	
	45	46	
	47	48	
	49	50	PMCIO50
	51	52	PMCIO52
	53	54	
	55	56	
	57	58	
	59	60	
	61	62	
	63	64	

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4.1.2.6 Miscellaneous Connector P1700

A 26 pin header P1700 provides miscellaneous interface signals.

	P1700		
nc	1	2	nc
BOOTSEL	3	4	GND
GND	5	6	\RST_BUT
+5V*	7	8	nc
+5V*	9	10	\WDG_REL
+5V*	11	12	BITOK
+5V*	13	14	BATT+
GND	15	16	
+5V*	17	18	
GND	19	20	
+5V*	21	22	Reserved
reserved	23	24	
	25	26	GND

* Supplied via P1101 terminal (5V)

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5 Appendix B

The RL4 has a boot load program in the EEPROM. This boot loader will initialize the RL4 and load the appropriate operating system. For newest version please contact factory.

The RL4 is a very versatile board with highly integrated device. Each of these devices have many options and features, which could only partly or not at all be described in this manual. Please refer to the data sheets, which are applied on the SBS WEB-site or contact the manufacture WEB site directly.

Device	WEB site
PowerPC (Motorola)	www.mot.com/SPS/PowerPC
PowerPC (IBM)	www.chips.ibm.com
ChipSet (Motorola)	www.mot.com/SPS/PowerPC
Ethernet (Intel)	www.intel.com
Flash (Intel)	www.intel.com
PCI/PCI Bridge (Texas Instruments)	www.ti.com
UART (Exar)	www.exar.com
RTC (Dallas Semiconductor)	www.dalsemi.com
nvSRAM (Simtek)	www.simtek.com
RL4 support	www.SBS.com

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Error Report Form

When you are returning a product for repair, it is very important to include a written report which details the nature of the problem in order to expedite the repair.
Please always use the Error Report Form attached a the end of this maual or include the following information:

- RMA Number
- Product & Serial Number
- Part Number
- Version
- Contact: Name & Phone Number
- Detailed Description of the Problem/Defect

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Error Report Form

SBS Technologies GmbH & Co.KG	Company Name
Memminger Str. 14	Department
86159 Augsburg	Contact Person
	Mailing Address
Phone Number +49 821 5034-116	Phone Number
Fax Number +49 821 5034-119	Fax Number
	Email Address

Part. N. RL4 Version: V _ . _ Date __ __ __ Serial N. _____

Error Description:
Hardware Environment:
Operating System/Software:
Warranty repair: ☐ YES ☐ NO (Please see section 'Warranty')

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Error Report Form (US + Rest of World)

SBS Technologies, Inc.	Company Name
6301 Chapel Hill Road	Department
Raleigh, NC 27607-5115	Contact Person
	Mailing Address
Phone Number +1 919 851-1101	Phone Number
Fax Number +1 919 851-2844	Fax Number
	Email Address

Part. N. RL4 Version: V _ . _ Date __ __ __ Serial N. _____

Error Description:
Hardware Environment:
Operating System/Software:
Warranty repair: ☐ YES ☐ NO (Please see section 'Warranty')

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