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V5C

Technical Manual



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V5C

Pentium PC/AT Compatible VMEbus Single Board Computer

Technical Manual

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V5C Technical Manual
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This manual applies to the V5C Embedded PC, revision A2 and above, until superceded.

Revision Date	by	Comments
05-09-2001	jev	Initial Release
09-19-2001	jev	Updated logo, some typo's and Power info in specifications.
10-11-2001	jev	Changed Bit 0 & 4 under Reset Control Register on Page 6-3.
11-06-2002	jev	Correction to Keyboard/Mouse connector drawings on Page 3-6

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This manual uses some generally accepted conventions for clarity and accuracy. These include:

- The use of an 'H' suffix before a number indicates hexadecimal (base sixteen) notation.
- The use of a '-' (minus) suffix to a signal name indicates an active low signal. The signal is either true when it is at a logic zero level or the signal initiates actions on a high-to-low transition.
- Text in `Courier` Font indicates a command entry or output from an SBS embedded PC product using its built-in character set.

This manual is designed to provide information regarding the general use and application of the V5C Embedded PC, as well as detail the hardware design. Some software programming information is also provided in Chapters 6 and 7 of this manual.

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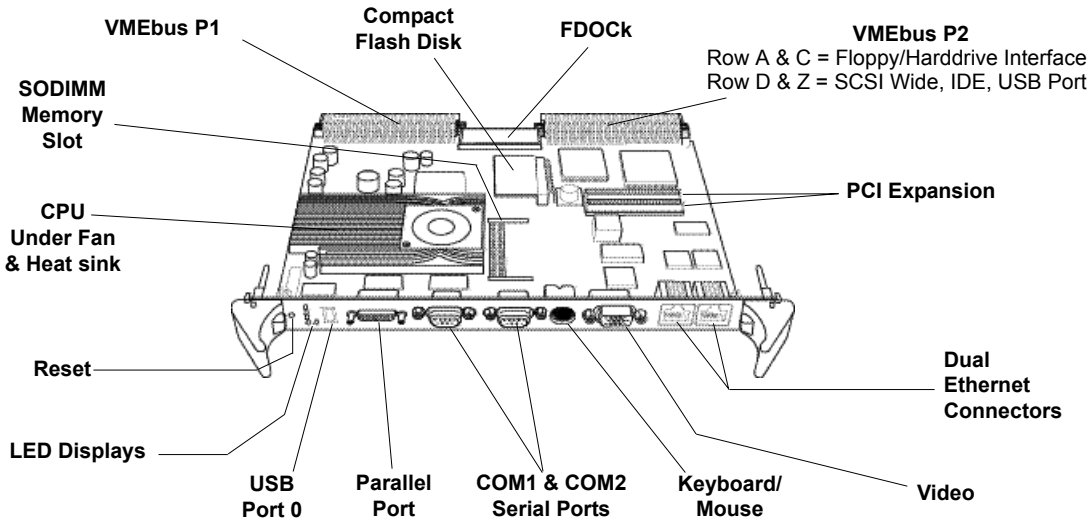
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CHAPTER 1 Introduction



Chapter Scope

This chapter describes the features, capabilities and compatibilities of the V5C.

PC99 Design Guide Compatibility Features

The V5C Embedded PC is compatible with software written compliant with the PC99 Design Guide. All of the functions necessary for operation as a Pentium based computer are included. There are also a number of features provided on board which usually require plug-in cards in a desktop Pentium computer. The following paragraphs describe features which relate to the V5C PC99 functionality.

Intel Pentium III Microprocessors

The V5C is available from the factory with an Intel Pentium III or Celeron processor at a variety of speeds. Celeron processors of 450MHz and up, and Pentium III processors of 450MHz and up (as available) are currently supported. The Celeron has a 66MHz front side bus, and the Pentium III has a 100MHz front side bus. Each processor will run standard software written in compliance with the PC99 Design Guide. They provide the capability of running 8-bit (8086), 16-bit (80286), as well as full 32-bit (80386) software & operating systems, and support MMX technology. This choice of processors allows you to select a V5C with the performance best suited to your application.

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Compatible ROM BIOS
The V5C uses a ROM BIOS produced by AWARD to ensure that the BIOS is compatible with PC99 and existing Pentium systems without infringing on copyrights. The BIOS provides low-level machine dependent software functions, relieving the operating system from dealing with hardware directly. A substantial number of software programs use BIOS calls rather than Operating System calls, so it is important to have a BIOS that works exactly like the original PC99 compatible BIOS.

Compatible I/O
The V5C incorporates the I/O capabilities of a PC99 compatible system by using the ALi 1543C Southbridge chip with its built-in super I/O controller. These capabilities include two RS-232 serial communications ports, a parallel printer port, and a keyboard /mouse port. The COM-2 serial port is enhanced for selectable RS-232, RS-422 or RS-485 operation.

System Memory
The V5C default onboard memory is 256MB SDRAM, but can be customized to 512MB. There is a standard 144-pin SODIMM expansion socket onboard for memory upgrade. An SODIMM with a minimun PC100 rating, and maximum of 512MB can be accomodated. The socket “foot-print” size is expanded from the industry standard to allow 2 in. deep modules.

Compact Flash
The V5C has an on-board Compact Flash Drive slot, compatible with standard units such as Sandisk© ATA Flashdrive. Currently available memory sizes are supported.

Floppy Controller
The ALI 1543C Southbridge chip also includes a fully PC99 compatible floppy disk controller onboard the V5C. It can control one 3.5” 1.44M floppy disk drive. The floppy control signals are provided through the P2 connector for simple connection to an SBS Embedded Computers VME-6200 series disk drive module, or to an external disk drive setup using SBS Embedded Computers’ VME-TB21 transition board, or VME-TB51 for VME64 5-row expansion.

Primary Integrated Drive Electronics (IDE) Controller
The onboard Enhanced Integrated Drive Electronics (EIDE) controller provided by the ALi chip set is an industry standard IDE interface for disk drives or other IDE peripherals. IDE control signals are provided through the P2 connector for easy connection to VME-6200 series disk drive modules, or to an external disk drive setup using a VME-TB21/VMETB-51.

Secondary Integrated Drive Electronics (IDE) Controller
The secondary IDE can operate from a TB51 with 5-row P2, or is shared with on board Compact Flash Interface. If Compact Flash IDE is used, the second IDE drive must be a slave device.

Small Computer Systems Interface (SCSI) Controller
The Symbios 53C875E Small Computer Systems Interface (SCSI) controller

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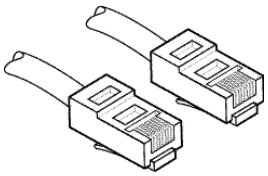
provides an Ultra Fast 40 SCSI compatible interface for hard disk drives or other SCSI peripheral devices. The SCSI control signals are provide through the P2 connector for painless connection to a VME-6200 series disk drive module, or to an external disk drive setup using a VME-TB21. This interface can be either 8-bit (6200, TB21) or 16-bit (TB51 only).

Video Accelerator

The V5C uses the 69030 Dual HiQVideo Accelerator, with 4 Megabytes of embedded SDRAM memory. The 69030 is designed to support high performance graphics and acceleration for all supported display resolutions, display types, and color modes (up to 1600 x 1200, @ 60Hz refresh). A standard 15-pin VGA connector is provided through the front panel for attaching VGA and SVGA capable monitors.

On-Board Ethernet

The V5C incorporates dual high-performance Intel 82559 Ethernet controllers on-board. The 82559 is a fully IEEE 802.3 compatible, low power ethernet controller in a small BGA package. The V5C comes with two Twisted-Pair (10/100BaseT) physical interfaces provided through dual RJ45 connectors mounted on the front panel. (100BaseT is indicated by a yellow LED.)



Dual Ethernet Controllers

PCI Expansion

The V5C provides a primary bus PCI connect to the SBS Embedded Computers TPMCC carrier. Since the V5C does not contain a PCI Bridge, a 21150 PCI Bridge is included on the TPMCC for using PCI Mezzanine Cards (PMC).

VMEbus VME64 Compatibility Features

To meet the VME64 ANSI/VITA 1-1994 standard, the V5C uses the Tundra Universe IIB VMEbus Interface chip. The VMEbus interface of the V5C is high-speed and very flexible, yet is easy for software to utilize.

A complete technical manual for the Tundra Universe IIB chip can be downloaded via the Internet from Tundra Semiconductor Corporation's website at **http://www.tundra.com**.

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Full Universe IIB VMEbus Master/Slave Operation
The V5C was designed to provide both VMEbus Master and VMEbus Slave capability. As such, it can initiate data transfers over the VMEbus and receive data from other VMEbus Masters. A number of facilities have been provided to enhance VMEbus Master and Slave operation.

The VMEbus interface provides 8 master and 8 slave VMEbus access paths. A path configured as a slave allows access to the V5C System DRAM and other local resources from the VMEbus. The interface can be configured to allow all, part, or none of the local address space to be accessible, allowing local data to be configured as inaccessible from the VMEbus.

An access path configured as a master allows the V5C to perform data transfers on the VMEbus. A path can be configured to appear anywhere in available local address space, and map anywhere on the VMEbus, providing for a very flexible interface.

Byte Swapping Capability
The V5C features hardware implemented byte swapping. This allows for faster data transfers than possible using software implemented byte swapping. Supported modes of byte swapping are M32(no swapping), I32(Intel swapping), and I16(D16 byte swap). These modes can be specified for both master and slave transfers.

VMEbus System Controller Capability
The V5C can be software configured as a VMEbus System Controller, independent of VMEbus Master or Slave operation. This is especially important if the V5C is going to be the only CPU card in the VMEbus system. Also, the V5C can automatically detect if it is in the VME slot one and turn on the System Controller function.

Interrupter and Interrupt Handler
The Universe IIB chip provides a flexible scheme to map interrupts to either the PCI bus or the VMEbus. The Universe IIB Interrupter provides an 8-bit STATUS/ID to a VMEbus interrupt handler during the IACK cycle, and optionally generates an internal interrupt to signal that the interrupt vector has been provided. A VMEbus interrupt can trigger the Universe IIB to generate a normal VMEbus IACK cycle. When the IACK cycle is complete, the Universe IIB releases the VMEbus and the interrupt vector is received by the PCI resource servicing the interrupt output.





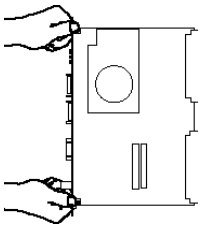
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CHAPTER 2

Unpacking, Inspection, and Initial Operation

Chapter Scope

This chapter covers the suggested inspection, preparation considerations and background information necessary prior to using the V5C. Unpacking, initial inspection, and first-time operation of the V5C are also covered. Following the procedures given in this chapter is recommended, since these will verify proper operation, both after shipping and before the product is integrated into your VMEbus system.





ATTENTION
Static Sensitive Devices
Handle only at Static Safe Work Stations

Proper handling of the V5C is critical to ensure proper operation and long-term reliability. When unpacking the board, and whenever handling it thereafter, be sure to hold the V5C by the front panel or the card ejectors as shown in the drawing on the left. Do not hold the V5C by the circuit card edges, the heat sink, or the VMEbus connectors.

Electrostatic Discharge Notice

The discharge of static electricity, known as **E**lectro**S**tatic **D**ischarge or ESD, is a major cause of electronic component failure. The V5C has been packaged in a static-safe bag which protects the board from ESD while the board is in the bag. Before removing the V5C or any other electronic product from its static-safe bag, be prepared to handle it in a static-safe environment.

You should wear a properly-functioning antistatic strap and ensure you are fully grounded. Any surface upon which you place the unprotected V5C should be static-safe, usually facilitated by the use of antistatic mats. From the time the board is removed from the antistatic bag until it is in its card cage and functioning properly, extreme care should be taken to avoid “zapping” the board with ESD. You should be aware that you could “zap” the board without your knowing it; a small discharge, imperceptible to the eye and touch, can often be enough to damage electronic components. Extra caution should be taken in cold and dry weather when static easily builds up.

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Unpacking and Handling

Although the V5C is carefully packaged against the rigors of shipping, it is still possible that shipping damage can occur. Careful inspection of the shipping carton should reveal some information about how the package was handled by the shipping service. If evidence of damage or rough handling is found, you should notify the shipping service and SBS Embedded Computers as soon as possible.

Only after ensuring that both you and the surrounding area are protected from ESD, carefully remove the V5C from the shipping carton by grasping it by the front panel and the VME connectors. Place the board, in its anti-static bag, flat down on a suitable surface. You may then remove the board from the anti-static bag by tearing the ESD warning labels.

Initial Inspection

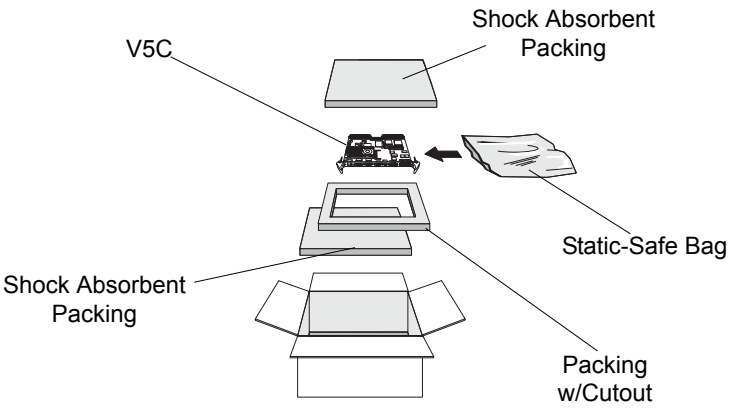
After unpacking the V5C, you should inspect it for visible damage that could have occurred during shipping or unpacking. If damage is observed (usually in the form of bent component leads or loose socketed components), contact SBS Embedded Computers for additional instructions. Depending on the severity of the damage, it may need to be returned to the factory for repair. ***DO NOT apply power to the board if it has visible damage.*** Doing so may cause further, possibly irreparable damage, as well as introduce a fire or shock hazard. Since the V5C incorporates a number of socketed components, including the CPU, memory, Etc., these should be inspected to make sure they are seated fully in their sockets.

Included Items

Table 2-1 lists accessories which are included with each V5C. You may want to make sure that you have the items shown in the event that you need them during installation or configuration.

Qty.	Item	Purpose
1	Cable Adapter	Custom PC Keyboard/Mouse Adapter

Table 2-1 Included Items



Retain all packing materials in case of future need.

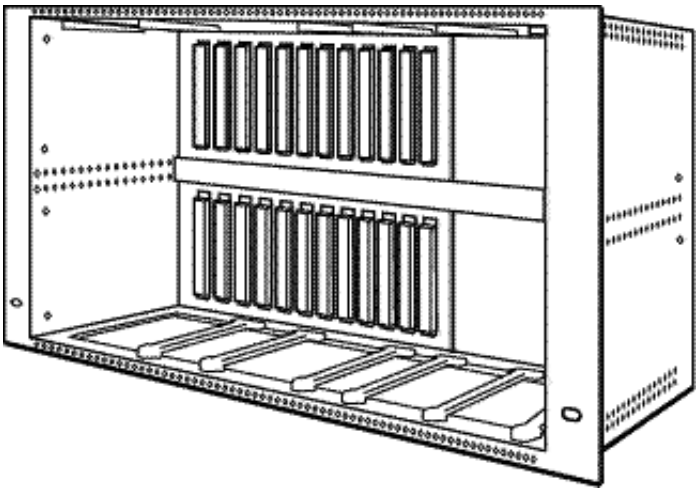
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Minimum System Requirements

As shipped, the V5C has been thoroughly tested and *burned-in*, and is nearly ready for use in your VMEbus system. In order to verify V5C operation for the first time, it is suggested that you only configure a minimal system. It is not necessary to have disk drives or other accessories connected in order to perform the V5C confidence tests. The following items are all that are required:

VMEbus Backplane and Power Supply

You will need a standard VMEbus P1 or combination P1/P2 backplane wired into a regulated power supply capable of providing stable low noise +5 volt, +12 volt, and -12 volt sources. Make sure that the supply is capable of meeting the total power requirements of the V5C. Please refer to chapter 8 for the V5C Specifications. Initially, you may plug the V5C into any available 6U slot of your VMEbus backplane. Later you will need to select the proper slot for your particular application. Make certain the power supply is NOT turned ON when the V5C is plugged into your backplane.



Typical VMEbus backplane Assembly

Never install or remove any VMEbus card while power is applied unless it is certified for hot-insertion (the V5C is not).

Keyboard/Mouse connector

You should have a PC99 compatible keyboard for initial system operation. Depending on your application, this keyboard may be a standard full-travel keyboard, or one which utilizes membrane switches for harsh environments. The miniature DIN keyboard connector is located on the front panel and is directly compatible with existing PC99 compliant keyboards. If your keyboard has the normal IBM PC-type keyboard connector you will need to use the supplied cable adapter for proper mouse operation.

> **NOTE:**
> *The V5C has a single connector defined for both keyboard and mouse. The definition is such that without an SBS adapter, only the keyboard is available. With the SBS adapter, keyboard and mouse port access are provided.*

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Plug your adapter into the keyed PS2 connector on the front panel, then plug the keyboard and mouse into the adapter before power is applied. Plugging and unplugging the keyboard while power is applied is not recommended and can cause a software failure or damage to the keyboard and/or on-board circuitry.

Video Monitor

Any VGA-compatible video monitor can be used initially for display output. The 15-pin front panel connector is fully compatible with the VGA standard connector and pinout. Plug your video monitor into the connector labeled 'VIDEO'.

After making sure that you have installed the V5C properly into your VMEbus backplane, apply power to your video monitor and then the VMEbus supply. When the board is completely reset, the processor should begin executing initial BIOS-resident routines.

Initial Power-On Operation

After a few seconds, the V5C System BIOS banner will be displayed similar to that shown in Figure 2-1.

If you have seen all the messages to this point, you can be confident that the board is running properly and is ready to be installed and setup for your application. You may now shut off power to the VMEbus chassis and begin board setup and configuration as described in Chapter 3.

```
Award Modular BIOS
Copyright (C)  1984-98, Award Software, Inc.

SBS Embedded Computers - V5C ver. 0.9 R.C. - 11/17/2000

INTEL Pentium III - 600 CPU found
Memory Test: 512,000k OK
```

Figure 2-1 System BIOS Banner

If the board did not perform as described above, some damage may have occurred in shipping or the board is not installed or setup properly. Contact SBS technical support as described in Chapter 9 for further instructions.

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CHAPTER 3 Installation and Interfacing

Chapter Scope

This chapter covers installing the V5C in a VMEbus system and interfacing the V5C to external devices and peripherals.

Installing the V5C

The V5C is designed to conform to the VMEbus physical specifications for a 6U×4HP dual eurocard (dual-height, single-width). It can be plugged directly into any standard card cage designed for these types of cards. Installation of the V5C is relatively simple as described below. The V5C with Pentium III requires full P1 and P2 Backplane installation to prevent +5V power starvation.

Installation Requirements

The following paragraphs describe requirements which your VMEbus system must meet in order to install and successfully integrate the V5C. If you are uncertain about any requirements, be sure to contact SBS Embedded Computers Technical Support before installing your V5C.

VMEbus Power Requirements

Power is supplied to the V5C via the VMEbus P1 connector as shown in Table 3-1 below.

Signal	Location on VMEbus P1
+5 Volts	Row a, pin 32
	Row b; pin 32
	Row c; pin 32
Ground	Row a; pins 9, 11, 15,17,19
	Row b; pins 20,23
	Row c; pin 9
+12 Volts	Row c; pin 31
-12 Volts	Row a; pin 31

Table 3-1 VMEbus P1 Power Pins

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If you are using the V5C in a full 32-bit address system, additional power and ground pins are connected according to VMEbus specification for P2 row *b* as shown in Table 3-2.

Signal	Location on VMEbus P2
+5 Volts	Row b; pins 1,13,32
GND	Row b; pins 2,12,22,31

Table 3-2 VMEbus P2 Power Pins

The actual electrical requirements of the V5C are defined in the Specifications section of chapter 8.

WARNING:

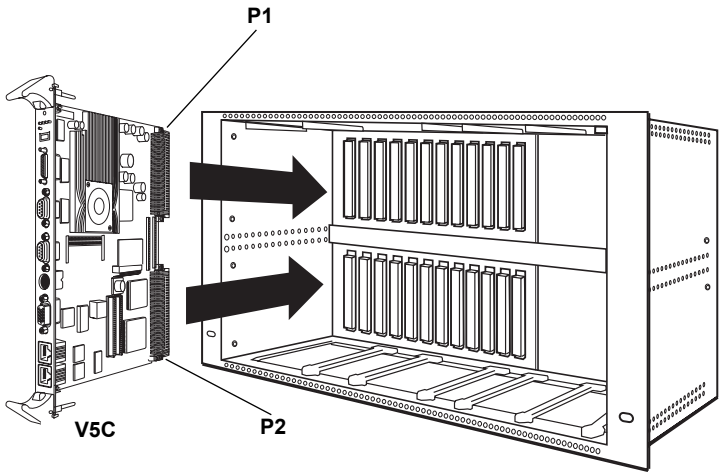
The P2 connector of the V5C has the a and c rows ***defined by SBS*** *as the VMEbus specification permits. However, other boards on the VMEbus may also define these rows. Damage can result to the V5C or other boards if the P2 a,c,d and z row signals are bussed between boards which are not compatible.*

VMEbus Backplane Requirements

Not recommended for P1 only with any Pentium III design. The V5C with Pentium III requires full P1 and P2 Backplane installation to prevent +5V power starvation.

VMEbus P1 Connector

The V5C has been designed to directly interface with any VMEbus P1 backplane conforming to the Rev. C.1 specification. Table 3-3 summarizes the VMEbus P1 signals used.



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Pin	Row z Signal	Row a Signal	Row b Signal	Row c Signal	Row d Signal
1	RSRVD33	D00, Data bit 0	BBSY-	D08, Data bit 8	RSRVD1
2	GND9	D01, Data bit 1	BCLR-	D09, Data bit 9	RSRVD2
3	RSRVD34	D02, Data bit 2	ACFAIL-	D10, Data bit 10	RSRVD3
4	GND10	D03, Data bit 3	BG0IN-	D11, Data bit 11	RSRVD4
5	RSRVD35	D04, Data bit 4	BG0OUT-	D12, Data bit 12	RSRVD5
6	GND11	D05, Data bit 5	BG1IN-	D13, Data bit 13	RSRVD6
7	RSRVD36	D06, Data bit 6	BG1OUT-	D14, Data bit 14	RSRVD7
8	GND12	D07, Data bit 7	BG2IN-	D15, Data bit 15	RSRVD8
9	RSRVD37	GND1	BG2OUT-	GND8	RSRVD9
10	GND13	SYSCLK	BG3IN-	SYSFAIL-	RSRVD10
11	RSRVD38	GND2	BG3OUT-	BERR-	RSRVD11
12	GND14	DS1-	BR0-	SYSRESET-	RSRVD12
13	RSRVD39	DS0-	BR1-	LWORD-	RSRVD13
14	GND15	WRITE-	BR2-	AM5	RSRVD14
15	RSRVD40	GND3	BR3-	A23	RSRVD15
16	GND16	DTACK-	AM0	A22	RSRVD16
17	RSRVD41	GND4	AM1	A21	RSRVD17
18	GND17	AS-	AM2	A20	RSRVD18
19	RSRVD42	GND5	AM3	A19	RSRVD19
20	GND18	IACK-	GND6	A18	RSRVD20
21	RSRVD43	IACKIN-	Not used	A17	RSRVD21
22	GND19	IACKOUT-	Not used	A16	RSRVD22
23	RSRVD44	AM4	GND7	A15	RSRVD23
24	GND20	A07	IRQ7-	A14	RSRVD24
25	RSRVD45	A06	IRQ6-	A13	RSRVD25
26	GND21	A05	IRQ5-	A12	RSRVD26
27	RSRVD46	A04	IRQ4-	A11	RSRVD27
28	GND22	A03	IRQ3-	A10	RSRVD28
29	RSRVD47	A02	IRQ2-	A09	RSRVD29
30	GND23	A01	IRQ1-	A08	RSRVD30
31	RSRVD48	-12V	+5VSTDBY	+12V	RSRVD31
32	GND24	+5V1	+5V2	+5V3	RSRVD32

Table 3-3 V5C P1 Signals

VMEbus P1 Daisy Chain Signals

The VMEbus specification defines two signal paths which are connected in daisy chain fashion, meaning that they are intercepted at each card position before being passed on the the adjacent card. These signals are associated with bus acquisition and interrupt acknowledgement. Before plugging the V5C into the P1 backplane, you should make sure that the backplane slot is configured appropriately for these signals.

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Bus Grant Daisy Chain

The VMEbus has four bus grant daisy chain signal pairs: BG0IN-/BG0OUT-, BG1IN-/BG1OUT-, BG2IN-/BG2OUT-, BG3IN-/BG3OUT-. When configuring a VMEbus P1 backplane, it is necessary to jumper all bus grant daisy chain signals on the backplane so that the bus grant outputs are connected to the bus grant inputs at all unused slots. At the slot in which a V5C is installed none of the bus grant signals should be jumpered. Most VMEbus P1 backplanes provide an easy method of jumpering the bus grant signals at each card slot position.

Interrupt Acknowledge Daisy Chain

The VMEbus has a single interrupt acknowledge daisy chain signal pair; IACKIN-/IACKOUT-. As the V5C has an on-board VMEbus interrupter, it utilizes these signals for determining that a VMEbus acknowledge cycle in progress is intended for it. Therefore, it is necessary to make sure that the IACKIN- is not connected to the IACKOUT- at the slot where the V5C is to be installed. During an interrupt acknowledge cycle, the V5C will intercept the IACKIN- signal and either respond if it has a pending interrupt at the proper level, or it will pass the signal on to the next card via the IACKOUT- signal line. The interrupt controller in non-Slot 1 applications requires the backplane to have a “wrap-around” path for IACK- to Slot 1. Most VMEbus P1 backplanes provide an easy method of setting the interrupt acknowledge daisy chain at each slot.

The Standard P2 Connector

Row *b* of the V5C P2 connector conforms to the VMEbus specification for A32/D32 operation. SBS Embedded Computers has defined the *a* and *c* rows of the P2 connector with the signals for SCSI, IDE hard disk, and ST412 floppy disk interfaces. This is perfectly acceptable and in accordance with VMEbus specifications. SBS Embedded Computers has a TB-21 Translation Board which can adapt the row *a* and *c* signals of the P2 to standard SCSI, IDE hard disk, and ST412 floppy disk connectors. Also, SBS Embedded Computers has several disk drive modules which can directly connect to the V5C P2 via a P2-to-P2 cable. This system avoids cables in the card space of a card cage, and provides flexibility as to the placement of drives and other peripherals. The pinout of the V5C P2 connector is shown inTable 3-4.

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Pin	Row z Signal	Row a Signal	Row b Signal	Row c Signal	Row d Signal
1	SDB8	SDB0	+5V1	HDRESET-	SHDMRO
2	GND1	SDB1	GND17	PHD0	SHD0
3	SDB9	SDB2	Reserved	PHD1	SHD1
4	GND2	SDB3	A24	PHD2	SHD2
5	SDB10	SDB4	A25	PHD3	SHD3
6	GND3	SDB5	A26	PHD4	SHD4
7	SDB11	SDB6	A27	PHD5	SHD5
8	GND4	SDB7	A28	PHD6	SHD6
9	SDB12	SPAR0-	A29	PHD7	SHD7
10	GND5	SATN-	A30	PHD8	SHD8
11	SDB13	SBSY-	A31	PHD9	SHD9
12	GND6	SACK-	GND18	PHD10	SHD10
13	SDB14	SRST-	+5V2	PHD11	SHD11
14	GND7	SMSG-	D16	PHD12	SHD12
15	SDB15	SSEL-	D17	PHD13	SHD13
16	GND8	SC/D-	D18	PHD14	SHD14
17	SPAR1-	SREO-	D19	PHD15	SHD15
18	GND9	SI/D-	D20	LLOUT-	SPDIAG-
19	TB51DET	HDMARO	D21	PHDIOW-	SHDIOW-
20	GND10	FRWC-	D22	PHDIOR-	SHDIOR-
21	SPKR	FINDEX-	D23	PIORDY	SIRDY
22	GND11	FMT0-	GND19	PHDMACK-	SHDMACK-
23	+5V IN1	RLOUT	D24	PIRQ	SIRQ
24	GND12	FDS1-	D25	GND21	SIO18-
25	USB1 5V	RLIN	D26	PHDA0	SHDA0
26	GND13	FDIRC-	D27	PHDA1	SHDA1
27	USB1 D+	FSTEP-	D28	PHDA2	SHDA2
28	GND14	FWD-	D29	PHCS0-	SHCS0-
29	USB1 D-	FWE-	D30	PHCS1-	SHCS1-
30	GND15	FTK0-	D31	LLIN	SDASP-
31	USB1 GND	FWP-	GND20	FHS-	Reserved2
32	P5DET-	FRO-	+5V3	FDSKCHG	Reserved3

Table 3-4 V5C P2 Signals

Cooling Requirements

The V5C integrates a large number of high-performance components in the small space of a single-slot VME card. These components generate a lot of heat. To prevent damage to the board and to ensure reliable operation, the V5C MUST be cooled with forced air. A 100LFM fan is recommended, with ambient remaining below 55°C.

Interfacing the V5C to External Devices

Several connectors are provided on-board the V5C in order to establish an electrical interconnection to external devices. The normal PC keyboard/mouse, serial, parallel and video connections are provided through the front panel where they may be easily accessed while the card is installed in a card cage. In addition, the COM-2 port has software selectable RS-232, RS-422 & RS-485 signals, Ethernet interfaces 1 and 2 are provided through the front panel.

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Keyboard / Mouse Interface

The keyboard/mouse interface consists of six electrical connections provided on a 6-pin circular mini-DIN connector (PS/2-style). Two terminal connections are for communication between the keyboard and the keyboard interface port. Two similar connections are for communication between the mouse and the mouse interface port. All four of these signals are CMOS compatible. The two remaining connections provide power for the mouse and keyboard's operation. The keyboard/mouse connector with pin assignments as viewed from the front of the V5C are shown in Figure 3-1. Signal definitions are given in Table 3-5.

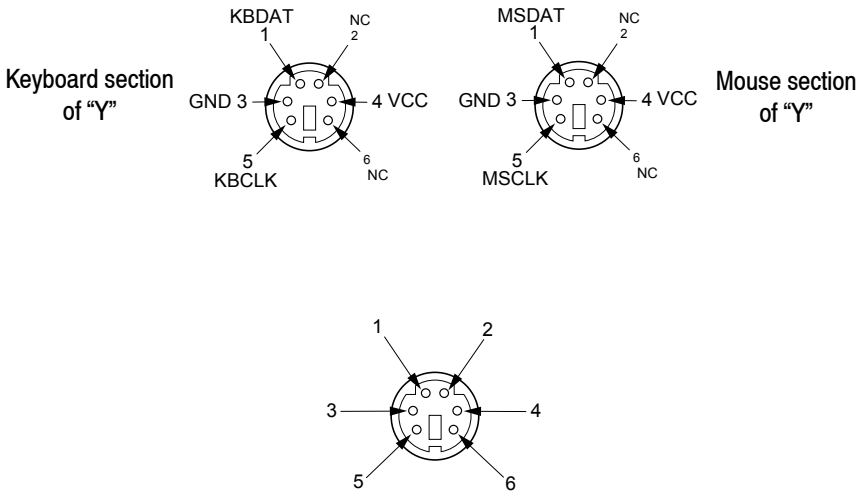


Figure 3-1 Keyboard / Mouse Interface

Pin	Signal	Function
1	KBDAT	Bidirectional serial data to/from keyboard
2	MSDAT	Bidirectional serial data to/from mouse
3	GND	Digital Ground (0 volt) reference to keyboard
4	VCC	+5 volt power to the keyboard
5	KBCLK	Bidirectional data clock to/from keyboard
6	MSCLK	Bidirectional data clock to/from mouse

Table 3-5 Keyboard / Mouse Interface Signals

A keyboard alone will work plugged into the keyboard/mouse connector, but a mouse alone will not function. The mouse operation requires a mini-DIN "Y" adapter, supplied with the V5C. The bottom part of the "Y" connects to the V5C keyboard/mouse port with two sections splitting to form a separate keyboard and mouse connecting point. This connector accepts any manufacturer's keyboard that is designed with a standard PS/2 interface

When plugging a keyboard into the V5C's keyboard connector, it is recommended that the system power be switched OFF. Plugging a keyboard into a powered-up system may cause improper initialization of the keyboard. If there is a static charge on the keyboard, it may cause damage to the V5C's keyboard controller circuitry or to the keyboard circuitry itself.

The supplied Keyboard/Mouse "Y" cable is Belkin Prt# F3G117-01.

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Serial Ports

The V5C is equipped with two serial ports which are compatible with the COM-1 and COM-2 ports on a PC99 compliant computer. Its signals are defined for industry standard interfacing using RS-232 compatible signal levels. COM-1 and COM-2 connectors are located between the parallel port and the keyboard/mouse connector. The connector pins are identified in Figure 3-2.

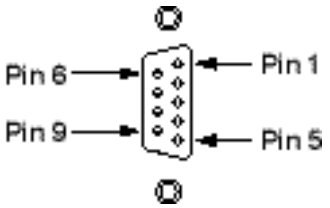


Figure 3-2 Serial Communications (COM) Port

Table 3-6 below defines the signals present on the pins of the COM-1 and COM-2 port connector, their intended function and their direction.

Pin	Signal	Direction	Function
1	DCD	To V5C	Data Carrier Detect, from modem
2	RXD	To V5C	Received Data, from modem
3	TXD	From V5C	Transmitted Data, to modem
4	DTR	From V5C	Data Terminal Ready, to modem
5	SIGND	—	Serial Interface Ground reference
6	DSR	From V5C	Data Set Ready, from modem
7	RTS	From V5C	Request To Send, to modem
8	CTS	To V5C	Clear To Send, from modem
9	RI	To V5C	Ring Indicator, from modem

Table 3-6 COM-1 and COM-2 (RS-232 Mode) Pin Assignments

Extended COM-2 Functionality

The COM-2 serial port of the V5C provides functionality beyond that of the basic PC99 standard. Under software control, COM-2 can be configured for RS-422 or RS-485 operation in place of standard RS-232. RS-422 operation on the V5C is four-wire full duplex. RS-485 operation on the V5C is two-wire half duplex. Table 3-7 shows the COM-2 signals for RS-422 operation. Table 3-8 shows the COM-2 signals for RS-485 operation.

In RS-422 or RS-485 mode it may be necessary to provide termination at the V5C if it is at either end of a multidrop link. For RS-485 this is be done automatically by the V5C. For RS-422, terminating resistors must be installed in the external connector shield. The terminating resistors should result in a low impedance of 100 ohms or less.

Note that the DSR and CTS signals are always true which allows DOS drivers and communications software to work properly. Also, the RTS line, when true, enables the RS-422 transmitter when V5C RS-422/485 operation is enabled.

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Pin	Signal	Direction	Function
1	NC	—	No connection
2	RXD-	To V5C	Receive data, negative
3	TXD-	From V5C	Transmit data, negative
4	TXD+	From V5C	Transmit data, positive
5	SIGND	—	Serial Interface Ground reference
6	RXD+	To V5C	Receive data, positive
7	NC	—	No connection
8	NC	—	No connection
9	NC	—	No connection

Table 3-7 COM-2 RS-422 Mode Pin Assignments

Pin	Signal	Direction	Function
1	NC-	—	No connection
2	TX/RX-	From/To V5C	Transmit/receive data, negative
3	NC	—	No connection
4	NC	—	No connection
5	SIGND-	—	Serial Interface Ground reference
6	TX/RX+	From/To V5C	Transmit/receive data, positive
7	NC	—	No connection
8	NC	—	No connection
9	NC	—	No connection

Table 3-8 COM-2 RS-485 Half-Duplex Mode Pin Assignments

Parallel Port

The parallel port on the V5C is accessible through a 25 pin male micro-miniature D-type connector, which appears just below the keyboard port on the V5C front panel. In its normal operating mode, the port functions exactly as does a standard PC99 compliant parallel printer port. In this mode of operation, it will interface with printers utilizing the industry standard Centronics parallel interface. Figure 3-3 below is the connector pinout and signals are defined in Table 3-9.

Operation of the printer port is accomplished with routines built into the ROM BIOS supplied with the V5C. Therefore, standard MS-DOS printer functions will work with a printer attached as the “PRN” device.

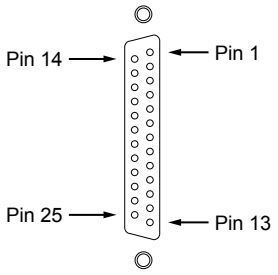


Figure 3-3 Parallel Port

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Under software control, the parallel port supports the optional PS/2 bidirectional parallel port (SPP), the Enhanced Parallel Port (EPP), and the Extended Capabilities Port (ECP) modes. Refer to the 1543C specifications for configuration information.

Pin	Signal	Direction	Function
1	STROBE-	Output	Data strobe
2	PD0	Output	Data bit 0
3	PD1	Output	Data bit 1
4	PD2	Output	Data bit 2
5	PD3	Output	Data bit 3
6	PD4	Output	Data bit 4
7	PD5	Output	Data bit 5
8	PD6	Output	Data bit 6
9	PD7	Output	Data bit 7
10	ACK-	Input	Data acknowledge
11	BUSY	Input	Printer busy
12	PE	Input	Printer enabled
13	SLCT	Input	Printer selected
14	AUTOFD-	Output	Automatic feed
15	ERROR-	Input	Printer error indicator
16	INIT-	Output	Initialize
17	SLCTIN-	Output	Printer select
18–25	GND	—	Signal Ground

Table 3-9 Parallel Port Pin Assignments

Video Interface

The 69030 Dual HiQVideo accelerator provided on-board the V5C Embedded PC is capable of supporting a variety of VGA-compatible video devices, such as VGA and SVGA CRTs. Maximum screen resolution is 1600 x 1200. The standard 15-pin VGA connector is provided through the front panel.

Ethernet Interface

The V5C contains Dual high performance Intel 82559 Ethernet controllers, and comes standard with dual Twisted Pair (10/100BaseT) interfaces and two RJ45 connectors through the front panel. Table 3-10 below shows the pin assignments for the RJ45 connectors.

Pin	Signal
1	Transmit Data Positive
2	Transmit Data negative
3	Receive Data Positive
4	No connection
5	No connection
6	Receive Data Negative
7	No connection
8	No connection

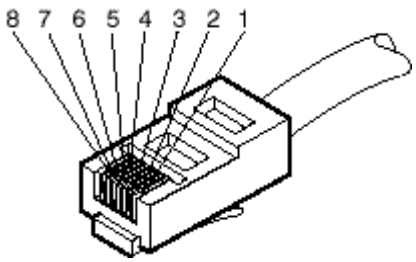


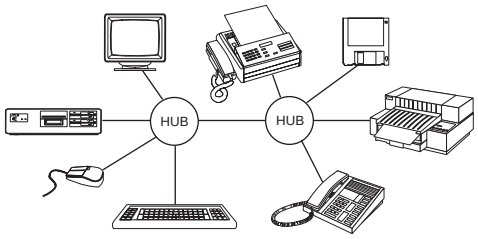
Table 3-10 Ethernet, 10/100BaseT, RJ45 Pin Assignments

LEDs on the Front Panel indicate Ethernet activity:
Green LED = Connect
Green LED Flash = Transmit
Yellow LED = 100MB operation

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USB Ports

Universal Serial Bus (USB) is a relatively new personal computer (PC) interconnect that can support simultaneous attachment of multiple devices. The host serves as master of the bus. Data transfer is serial with two modes of signaling: Full speed mode with a signaling rate of 12 megabits per second (Mbs), and a low speed mode with a signaling rate of 1.5 Mbs. The peripheral devices serve as slaves connected either directly to the host or through hubs which give additional connective capability.



USB System Example

The USB cable consists of four wires. Two wires, D+ and D-, are used for information transfer using differential signaling. The two other wires are used for power: Vbus and Ground. Low-cost unshielded cables are used for the low speed (1.5Mbs) while shielded cables are required for the 12Mbs rate. Essentially the USB protocol is similar to a Token Ring Network. The USB host keeps the bus active by sending a Start Of Frame (SOF) packet every millisecond. The available bus bandwidth is shared between simultaneously connected devices within this 1 millisecond time interval.

Due to the capability of “Hot Swapping”, it is not necessary to power-down to connect or disconnect a USB device. Immediately after a device is attached to the USB host, the host controller is alerted by way of voltage change on the D+ and D- lines. Once the host detects that a device is connected, it determines the exact port it is connected to and enables it. After a reset sequence the host can provide the device with up to 100mA of current through the Vbus/Gnd lines. Of course, self-powered devices do not use the power from the host.
The host uses an interrogation sequence through which it acquires information from the connected device, gives it a unique address, and assigns a configuration value. The system software then either recognizes the device and loads the corresponding device driver, or prompts the user to provide a device driver for the application. After the device driver is loaded, the device performs its intended function until it is detached from the host. Immediately after a device is detached from the USB host port, specific voltage changes on the D+ and D- lines alert the host of the action. The USB system software then acknowledges the removal of the device and frees up any host resources the device was using. For example the host reclaims the bandwidth, and if the device was bus-powered, it reclaims the power and makes it available to other devices.

The V5C has two USB Ports, designated USB0 and USB1. USB0 is a standard USB connector located on the V5C front panel. USB1 is incorporated into the P2 expansion. The V5C supports both the Full Speed (12Mbs) and Low Speed (1.5Mbs) USB serial transfer. The V5C USB Protocol is facilitated by the 1543C Southbridge chip.

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CHAPTER 4 Booting and Operation

Chapter Scope

This chapter describes the Award Software BIOS Setup program. The Setup program allows you to modify basic system configuration settings. The settings are stored in a dedicated battery-backed memory, called CMOS RAM, that retains the information when the power is turned off.

The Award Software BIOS is immediately activated when you first turn on the computer. The BIOS reads system configuration information in CMOS RAM and begins the process of checking out the system and configuring it through the Power-On Self Test (POST). The BIOS then seeks an operating system on one of the data storage devices (hard drive, floppy drive, etc.). The BIOS launches the operating system and hands control of system operations to it. You can enter the Setup program by pressing <DEL> immediately after switching the system on.

In Case of Problems

If you should discover that your computer is no longer able to boot after making and saving system changes with Setup, the BIOS supports an override to the CMOS settings that resets your system to its default configuration. You can invoke this override by immediately pressing <Del> when you restart your computer. You can restart by either using the ON/OFF switch, the RESET button, or by pressing Ctrl-Alt-Del.

It is recommended that you only alter settings that you thoroughly understand.

Mode Switch

Mode switch operation allows for a CMOS Clear operation if the Reset Button is held true for at least 2 seconds. This function does not work if the Reset Button is held at power up.

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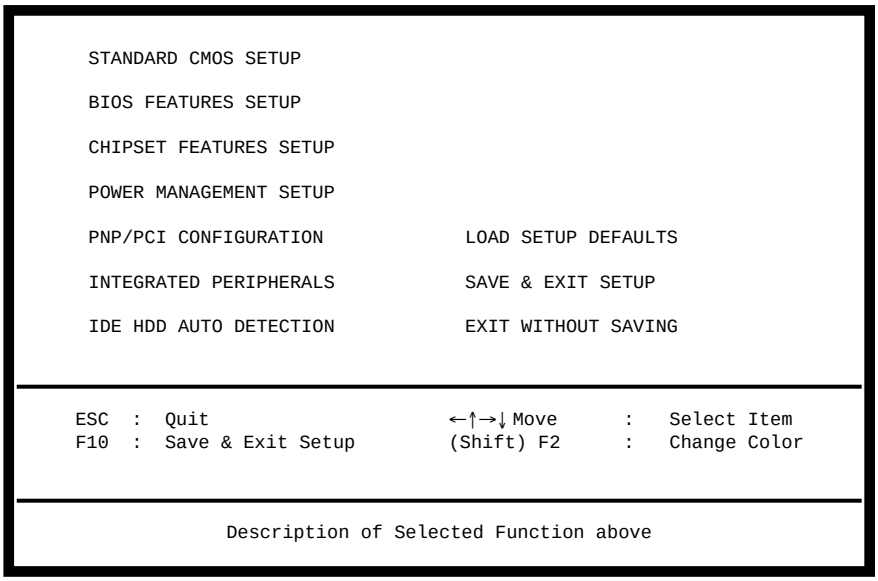
Setup Key Commands

The following keys may be used to operate the Setup program:

Arrow Keys	The arrow keys are used to move around the Setup screen. The up and down arrows move you through the previous and the next options respectively. The right arrow moves the cursor into the right side of the screen. The left arrow moves the cursor into the left side of the screen.
ESC	In the Main Menu, pressing the escape key exits the Setup program without saving changes. In other screens, it will exit current page and return to main menu.
PgUp or +	Increase the numeric value, or make changes.
PgDn or **-**	Decrease the numeric value, or make changes.
F1	General help only for Status page and Option page Setup Menu.
F2	Change color from total 16 colors. F2 to select color forward, Shift-F2 color backward.
F5	Restores the previous CMOS value from CMOS, only for Option Page Setup Menu..
F7	Loads Default BIOS values. (Option Page Setup Menu)
F10	Saves all CMOS changes. (Main Menu only)

Main Setup Menu

```
ROM PCI/ISA BIOS (2A6KLU80)
CMOS SETUP UTILITY
AWARD SOFTWARE, INC.
```



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Standard CMOS	Options in the original PC99 compatible BIOS.
BIOS Features	Award Software enhanced BIOS features.
Chipset Features	AT Clock, DRAM Timings, etc.
Power Management	Sleep Timer, Suspend Timer, Etc.
PNP/PCI Configuration	Local bus configuration options.
Integrated Peripherals	Settings for HDD, controllers, serial ports and other peripheral devices.
IDE HDD Auto Detection	Auto detect IDE Hard Disk Drive.
Load Setup Defaults	Factory settings for the most common options.
Save and Exit Setup	Save settings in non-volatile CMOS RAM and exit Setup.
Exit Without Save	Abandon all changes and exit Setup.

The following screens detail additional options available with the respective selections from the Main Menu screen.

Standard CMOS Setup

```
                ROM PCI/ISA BIOS (2A6KLU80)
                  STANDARD CMOS SETUP
                AWARD SOFTWARE, INC.

Date  (mm:dd:yy)  : Tue, May 8 2001
Time  (hh:mm:ss)  : 10:28:39

Hard Disks         TYPE   SIZE  CYLS  HEAD   PRECOMP LANDZ  SECTOR  MODE

Primary Master    : Auto   0     0     0      0       0      0       Auto
Primary Slave     : Auto   0     0     0      0       0      0       Auto
Secondary Master  : Auto   0     0     0      0       0      0       Auto
Secondary Slave   : Auto   0     0     0      0       0      0       Auto

Drive A           : 1.44M, 3.5 in.
Drive B           : None

Video             : EGA/VGA
Halt On           : All Errors

Base Memory       :      640K
Extended Memory   :   261120K
Other Memory      :      384K

Total Memory      :   262144K

ESC : Quit               ←↑→↓ Move  : Select Item     PU/PD/+/- : Modify
F10 : Save & Exit Setup  (Shift) F2 : Change Color
```


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Date This field is for information only, and can't be altered.

Time Time format is based on the 24-hour military clock. For example, 1 pm is 13:00. Pres right or left arrow to to move to desired fileds. Press PgUp or PgDn to increment the setting, or type in the desired value.

Hard Disks The BIOS supports up to four IDE drives. This section does not show information about other IDE drives, such as a CD ROM drive, or other hard drive types, such as SCSI drives. It is recommended that you select type AUTO for all drives. The BIOS can automatically detect the specifications and optimal mode for almost all IDE hard drives. When you select type AUTO for a hard drive, the BIOS detects its specifications during POST, each time the system boots. If you do not want to select type AUTO here, you may do one of the following:

1.) Match the specifications of your IDE hard drive(s) with the preprogrammed values for types 1 thru 45.
2.) Select USER and enter values directly into each drive parameter field.

Drive A, Drive B Select the correct specifications for the diskette drive(s) installed in your system.

Video Select the type of primary video subsytem in your computer. The BIOS usually detects the correct video type automatically.

Halt ON During the power-on self-test (POST), the computer stops if the BIOS detects a hardware error. You can tell the BIOS to ignore certain errors during POST and continue the boot process. These error selections are:

No Errors POST does not stop for any errors.

All Errors If the BIOS detects any non-fatal errors, POST stops and prompts you to take corrective action.

All But Keyboard POST does not stop for a keyboard error, but stops for all other errors.

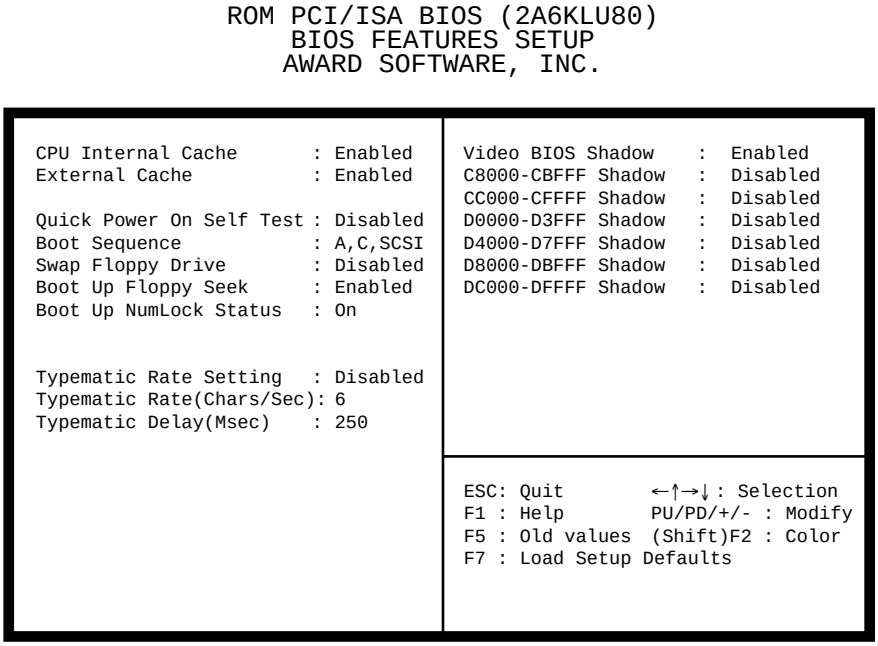
All But Diskette POST does not stop for diskette drive errors, but stops for all other errors.

All But Disk/Key POST does not stop for a keyboard or disk error, but stops for all other errors.

Memory You cannot change any values in the Memory fields. They are there for information only.

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BIOS Features Setup



CPU Internal Cache /External Cache Cache memory is additional memory that is much faster than conventional DRAM (system memory). When the CPU requests data, the system transfers the requested data from the main DRAM into cache memory, for even faster access by the CPU.

Quick Power On Self-Test Select enabled to to reduce the amount of time required to run the power-on self-test (POST). A quick POST skips certain steps. It is recommended that you normally disable Quick POST.

Boot Sequence The original IBM PCs loaded the DOS from drive A (floppy disk), so IBM PC-compatible systems are designed to search for an operating system first on drive A, and then on drive C (hard disk). Most modern computers load the operating system from the hard drive, and may even load it from a CD ROM drive. The options are: A,C,SCSI; C,A,SCSI; C,CDROM,A; CDROM,C,A; D,A,SCSI; E,A,SCSI; F,A,SCSI; SCSI,A,C; SCSI,C,A; C only, LS120,C; 21D100,C

Boot Up Floppy Seek When enabled, the BIOS tests (seeks) floppy drives to determine whether they have 40 or 80 tracks. Only 360k drives have 40 tracks. 720k, 1.2M, and 1.44M drives all have 80 tracks. Because very few modern PCs have 40-track drives, it is recommended that you set this field to DISABLED to save time.

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Boot Up NumLock Status	Toggle between ON and OFF to control the state of the NumLock key when the system boots. When toggled On, the numeric keypad generates numbers instead of controlling cursor operations.
Typematic Rate Setting	When DISABLED, Typematic Rate and Typematic Delay are irrelevant. Keyboard repeats at a rate determined by the keyboard controller in your system. When this is ENABLED, you can select Typmatic Rate and Delay.
Typematic Rate (Chars/Sec)	When the Typematic Rate setting is ENABLED, you can select a typematic rate (the rate at which a character repeats when you hold down a key) of 6, 8, 10, 12, 15, 20, 24,or 30 characters per second.
Typematic Delay (msec)	When the Typematic Rate setting is ENABLED, you can select a typematic delay (the delay before key strokes begin to repeat)of 250, 500, 750, or 1000 milliseconds.

Shadow

Software residing in a Read-Only Memory (ROM) is called Firmware. The Award Software BIOS permits *Shadowing* of firmware such as system BIOS, video BIOS and similar operating instructions that come with some expansion peripherals such as a SCSI adapter. Shadowing copies from ROM into system RAM, where the CPU can read it through the 64-bit DRAM bus. Firmware not shadowed must be read by the system through the 8-bit X-bus. Shadowing improves the performance of the system BIOS and similar ROM firmware for expansion peripherals.

ENABLE shadowing into each section of memory separately.

Video BIOS shadows into memory area C0000-C7FFF. The remaining areas shown on the BIOS features Setup screen may be occupied by other expansion card firmware. If an expansion peripheral in your system contains ROM-based firmware, you need to know the address range the ROM occupies in order to shadow it correcly into RAM.

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PnP/PCI Configuration

```
ROM PCI/ISA BIOS (2A6KLU80)
PNP/PCI CONFIGURATION
AWARD SOFTWARE, INC.
```

```
PNP OS Installed          : No
Resources Controlled By   : Auto
Reset Configuration Data  : Disabled

PCI IRQ Activated By      : Level
Slot 1 Use IRQ No.        : Auto
Slot 2 Use IRQ No.        : Auto
Slot 3 Use IRQ No.        : Auto
Slot 4 Use IRQ No.        : Auto

ESC: Quit       ←↑→↓ :Select
F1 : Help       PU/PD/+/- : Modify
F5 : Old values(Shift)F2 : Color
F7 : Load Setup Defaults
```

Resources Controlled By

The Award plug and play BIOS can automatically configure plug-and-play devices. AUTO selection displays the screen as above. MANUAL introduces additional options as indicated below. These additional options are automatically handled in AUTO selection.

```
PNP OS Installed          :No
Resources Controlled By   :Manual
Reset Configuration Data  :Disabled

IRQ-3 Assigned To         :PCI/ISA PnP
IRQ-4 Assigned To         :PCI/ISA PnP
IRQ-5 Assigned To         :PCI/ISA PnP
IRQ-7 Assigned To         :PCI/ISA PnP
IRQ-9 Assigned To         :PCI/ISA PnP
IRQ-10 Assigned To        :PCI/ISA PnP
IRQ-11 Assigned To        :PCI/ISA PnP
IRQ-12 Assigned To        :PCI/ISA PnP
IRQ-14 Assigned To        :PCI/ISA PnP
IRQ-15 Assigned To        :PCI/ISA PnP
DMA-0 Assigned To         :PCI/ISA PnP
DMA-1 Assigned To         :PCI/ISA PnP
DMA-3 Assigned To         :PCI/ISA PnP
DMA-5 Assigned To         :PCI/ISA PnP
DMA-5 Assigned To         :PCI/ISA PnP
DMA-6 Assigned To         :PCI/ISA PnP
DMA-7 Assigned To         :PCI/ISA PnP

PCI IRQ Activated By      : Level
Slot 1 Use IRQ No.        : Auto
Slot 2 Use IRQ No.        : Auto
Slot 3 Use IRQ No.        : Auto
Slot 4 Use IRQ No.        : Auto

ESC: Quit             ←↑→↓ :Select
F1 : Help         PU/PD/+/- : Modify
F5 : Old values   (Shift)F2 : Color
F7 : Load Setup Defaults
```

Reset Configuration Data

This is normally left DISABLED. Select ENABLED to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system re-configuration has caused such a serious conflict that the operating system cannot boot.

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IRQ x Assigned To When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt:

LEGACY ISA:

Devices compliant with the original PC AT bus specification, requiring a specific interrupt (such as IRQ4 for serial port 1).

PCI/ISA PnP:

Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

DMA x Assigned To When resources are controlled manually, assign each system DMA channel as one of the following types:

LEGACY ISA:

Devices compliant with the original PC AT bus specification, requiring a specific DMA channel.

PCI/ISA PnP:

Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

Integrated Peripherals

```
ROM PCI/ISA BIOS (2A6KLU80)
   INTEGRATED PERIPHERALS
    AWARD SOFTWARE, INC.
```

```
On-Chip Primary IDE      : Enabled
Master PIO               : Auto
Slave PIO                : Auto
Master Ultra DMA         : Auto
Slave Ultra DMA          : Auto
On-Chip Secondary IDE    : Enabled
Master PIO               : Auto
Slave PIO                : Auto
Master Ultra DMA         : Auto
Slave Ultra DMA          : Auto
IDE HDD Block Mode       : Enabled
On-Chip USB Controller   : Disabled
Init Display First       : PCI Slot
```

```
OnBoard FDC Controller  :Enabled
OnBoard UART Port 1     :3F8/IRQ4
OnBoard UART Port 2     :2F8/IRQ3


OnBoard Parallel Port   :378/IRQ7
Parallel Port Mode      :ECPEPP1.9
ECP Mode Use DMA        :3
```

```
ESC: Quit      ←↑→↓ : Selection
F1 : Help        PU/PD/+/- : Modify
F5 : Old values  (Shift)F2 : Color
F7 : Load Setup Defaults
```

On-Chip IDE Controller The integrated peripheral controller contains an IDE interface with support for two IDE channels. Select ENABLED to activate the IDE interface.

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IDE HDD Block Mode	Block mode is also called block transfer, multiple commands, or multiple sector read/write. If your IDE drive supports block mode (most new drives do), select ENABLED for automatic detection of the optimal number of block read/writes per sector the drive can support.
Onboard FDC Controller	Select ENABLED if your system has a floppy disk controller (FDC) installed on the system board and you wish to use it. If you install an add-in FDC or the system has no floppy drive, select DISABLED in this field.
Onboard Serial Ports (1/2, A/B)	Select a logical COM port name and matching address for the first and second serial ports. Select an address and corresponding interrupt for the first and second serial ports. Options are: AUTO, COM1/3F8, COM2/2F8, COM3/3E8, COM4/2E8, and DISABLED.
Onboard Parallel Port	Select a logical LPT port address and corresponding interrupt for the physical parallel port. Options are: DISABLED, 278/IRQ5, 3BC/IRQ7, and 378/IRQ7.
Parallel Port Mode	Select an operating mode for the onboard parallel (printer) port. Select SPP unless you are certain your hardware and software both support one of the other available modes. Options are: SPP, EPP 1.7, ECP EPP 1.7, EPP 1.9, ECP, ECP EPP 1.9.

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CHAPTER 5 Board Resources

Chapter Scope

This chapter describes the software- and hardware-configurable options of the V5C, as well as interrupts, DMA channels, and non-PC99 registers.

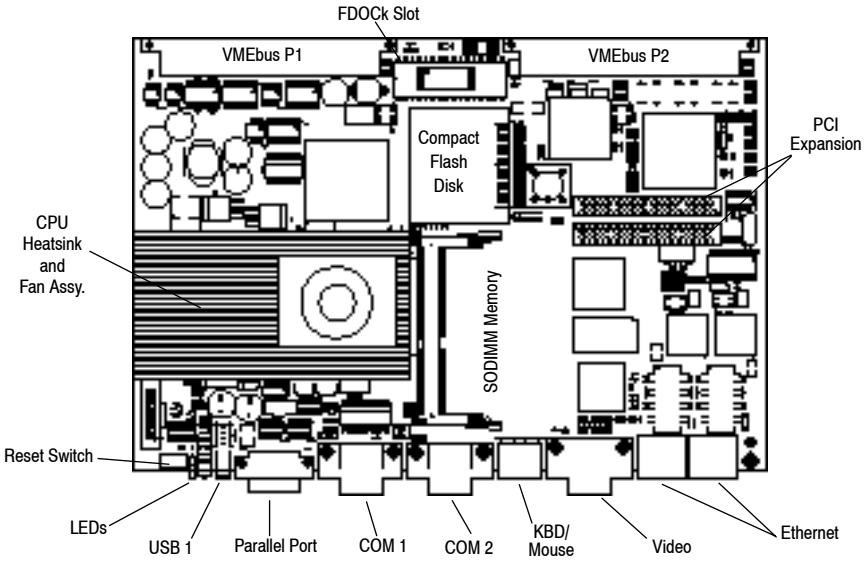
V5C Options

Processor Type & Speed

The V5C is designed to accommodate socket 370 processors (Pentium III or Celeron) at a variety of speeds. It can operate with a Celeron 450/66 and above, or a Pentium III/100 and above, according to market availability.

DRAM Size

The V5C comes standard with 128MB SDRAM. This memory is selectable for 128, 256 and 512MB. A single SODIMM expansion socket allows memory upgrades up to 1 GigaByte, depending on the on-board memory size. (SODIMM max = 512MB.)



V5C Assembly, Top View

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Front Panel LEDs

The V5C front panel contains five LEDs which provide important information regarding the status of the board. These LEDs are, from top to bottom:

SCON This LED is ON when the V5C is configured as the System Controller in a VMEbus system. This is an important indicator as it allows you to more easily verify that you have only one System Controller on the VMEbus.

RUN This LED indicates that the processor is active. This LED may flicker as other devices occupy the local bus, but extended outage could indicate that the board is locked up.

ENET 1&2 These LEDs indicate Ethernet activity:
Green LED On = Connect: Green LED Flash = Transmit
Yellow LED On = 100MB operation.

VMA This LED is illuminated when the V5C is performing a master access to the VMEbus.

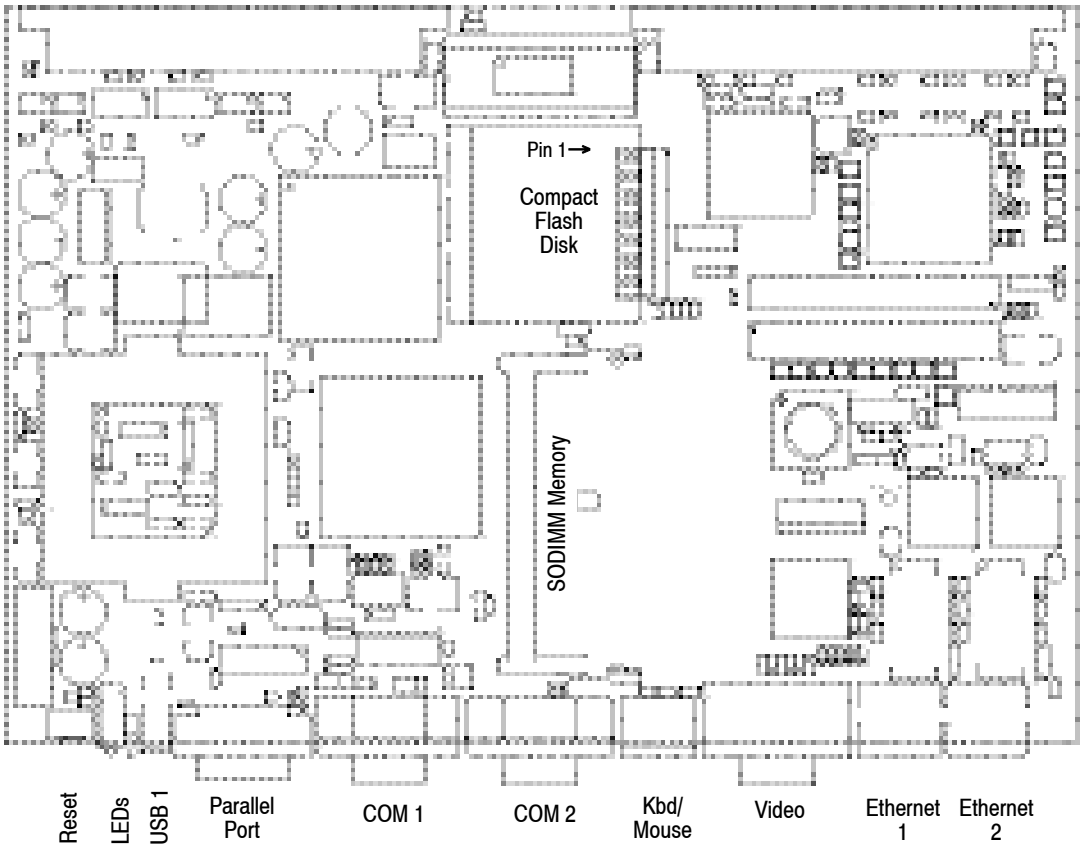
VSA This LED is illuminated when the V5C is being accessed as a slave from the VMEbus.

(Both **VMA** and **VSA** illuminate forV5C originated VME Block Transfers.)

ALARM This LED will be illuminated according to the following:
- Register bit 0x2A2[7] =1 turns LED on w 64 Hz flash rate.
- VME SYSFAIL = On Constant.

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V5C Circuit Board, Top View



V5C Circuit Board, Bottom View

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PC Interrupts

The 17 PC interrupts (including NMI) are allocated as shown in Table 5-1. Note that these are the default allocations, some can be changed. The PCI Interrupt is selectable between IRQ5, IRQ10, IRQ11, and IRQ15. IRQ11 is the default.

Interrupt	Interrupt Number	Description/Use
NMI	N/A	Parity Error 1 (Memory) or PE2 (ISA IOCHK)
IRQ0	8	Timer
IRQ1	9	Keyboard
IRQ2	A	Chain to Interrupts 8–15
IRQ3	B	COM2
IRQ4	C	COM1
IRQ5	D	Available; Selectable as PCI Interrupt**
IRQ6	E	Floppy Disk*
IRQ7	F	LPT1
IRQ8	70	Real Time Clock
IRQ9	71	Re-Directed to IRQ2
IRQ10	72	Default PCI Interrupt D (Ethernet)**
IRQ11	73	Default PCI Interrupt A (SCSI)** or Watchdog if Enabled.
IRQ12	74	Bus Mouse
IRQ13	75	Coprocessor
IRQ14	76	IDE Hard Disk*
IRQ15	77	Available; Selectable as PCI Interrupt**

Table 5-1 PC Interrupt Allocation

* These devices can be disabled to free the occupied interrupt.

** The PCI Interrupt is configurable as PC interrupt IRQ5, IRQ10, IRQ11, or IRQ15. IRQ11 is the default setting for INTA and IRQ10 is the default for INTD. Any of these PC interrupts to which the PCI Interrupt is not assigned can be considered available for other uses.

DMA Channels

The eight PC DMA channels are allocated as shown in Table 5-2. These are the default allocations, some can be changed. With all onboard devices enabled, six DMA channels are available for use by peripheral cards. Disabling the Floppy Disk will free DMA channel 2.

DMA Channel	Description/Use
0	Memory Refresh
1	Unavailable
2	Floppy Disk*
3	Unavailable
4	Unavailable
5	Unavailable
6	Unavailable
7	Unavailable

Table 5-2 DMA Channel Allocation

* These devices can be disabled to free the occupied DMA channel.

V5C Registers

The V5C has several non-AT registers such as Reset Control Register and the Serial EEPROM which allow complete control of the hardware by software. These registers are fully documented in the Programming section.

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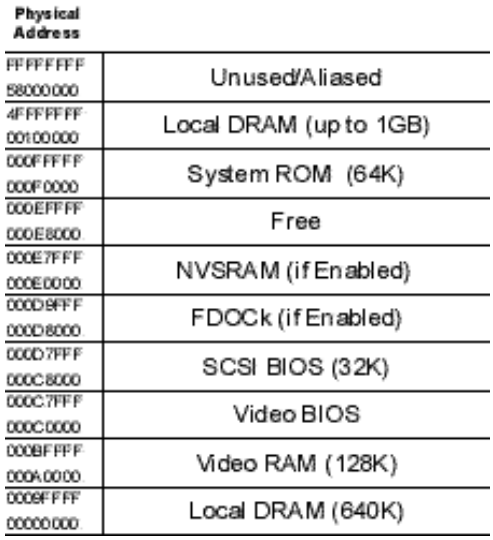


Figure 5-1 V5C Memory Map

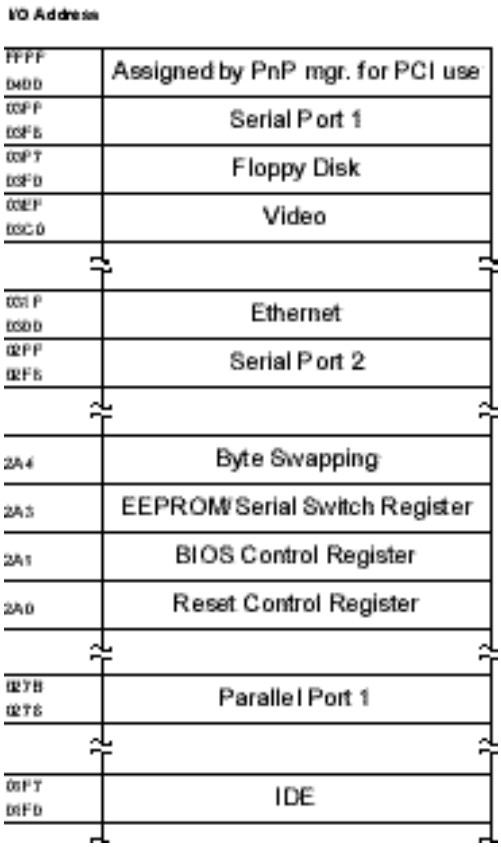


Figure 5-2 V5C Legacy I/O Map

Note that Local DRAM entries are dependent on the amount of DRAM installed. Also, some devices such as Floppy can be disabled, freeing space in the I/O map.

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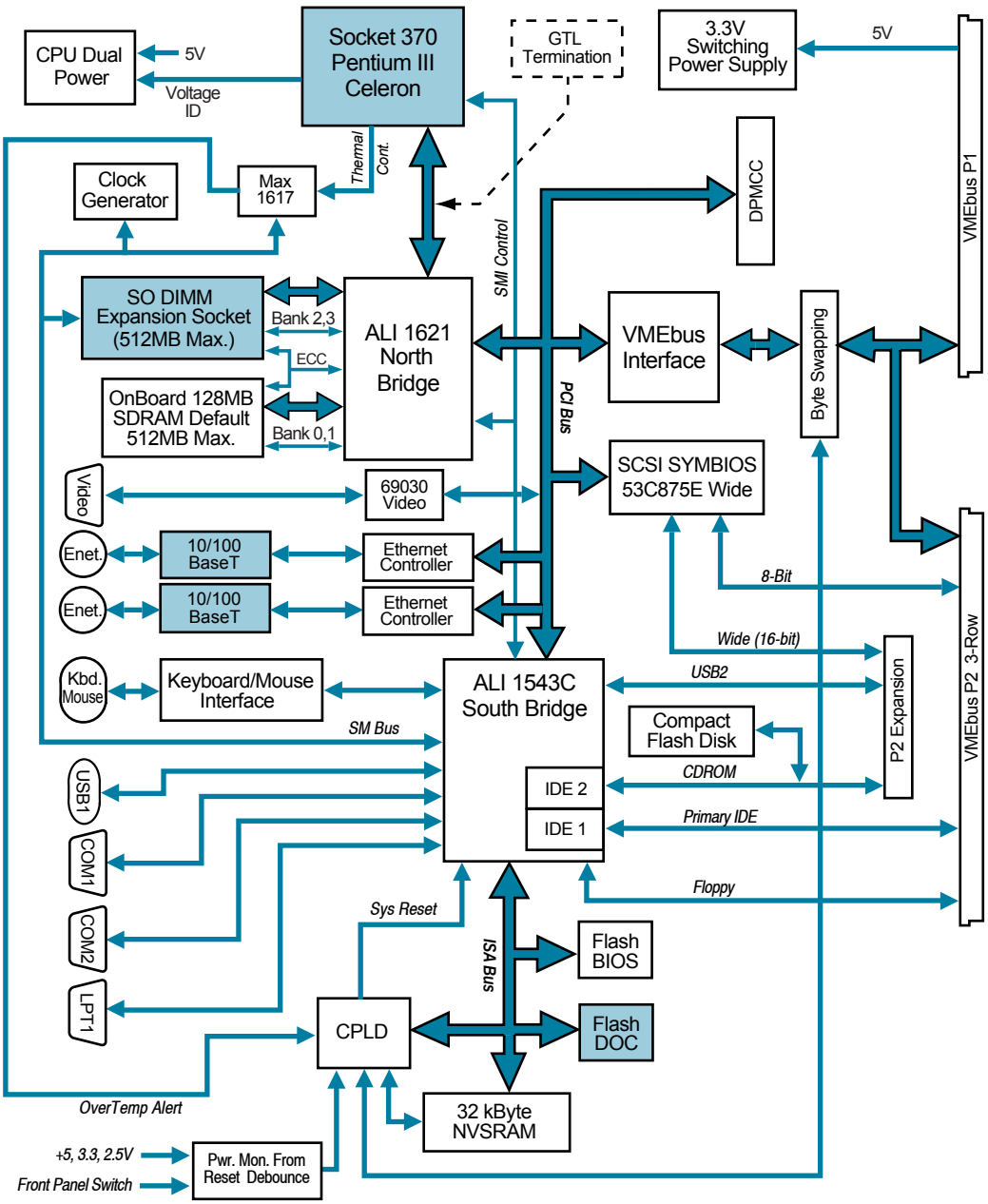


Figure 5-3 V5C Block Diagram

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CHAPTER 6

PC/AT Devices Programming

Chapter Scope

This chapter describes programming the PC/AT devices of the V5C. The basic peripherals such as the serial ports, the parallel port, and the keyboard port are covered generally, as are the more advanced controllers for the video, floppy disk, and hard disk interfaces. Devices not usually found on a standard desktop PC/AT, such as onboard Ethernet are covered in more detail.

Note that it is beyond the scope of this manual to provide the programming details associated with the IBM PC/AT compatible hardware, MS-DOS software, and the ROM BIOS. Rather, it is suggested that one of the many good programming reference books for the PC/AT architecture be consulted. We highly recommend that you obtain a copy of *Advanced MS-DOS* which is published by Microsoft Press. It presents the details of the software environment of MS-DOS and the associated calls to the ROM BIOS. If you are planning to program in 80x86 assembler or a high-level language such as 'C' and need to access system resources directly, you will find this book absolutely essential.

PC/AT Compatible ROM BIOS

The ROM BIOS is a firmware (installed in ROM) resident set of routines which is used to interface the particular system hardware to the MS-DOS operating system, and subsequently to MS-DOS applications. The use of a ROM BIOS in the original IBM PC/AT design has allowed programs to be developed specifically for the operating system environment without concern for the underlying hardware. Programs developed using the AT BIOS can be run on a variety of PC/AT compatible computers without modification. The BIOS provides a very rigid interface between the operating system and applications, and the hardware devices of the system. MS-DOS accesses devices through BIOS calls. These routines must perform their functions and return to the operating system after completion, without disturbing other system functions.

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SBS Embedded Computers has implemented the Award ROM BIOS for complete compatibility with IBM's BIOS, without infringing on IBM's copyright. Since the BIOS is completely compatible in operation with the original, you can rest assured that programs developed correctly will run, unmodified on the V5C.

In order to use the routines contained in the AT ROM BIOS, you will need to know how to make BIOS calls through software interrupts. This is described in detail in *Advanced MS-DOS*.

Serial Communications Interface

The NS16450/16550-compatible UART serial controllers within the ALI 1543C Southbridge chip fully implement both the standard PC/AT COM1 and COM2 serial ports. These devices normally appear at the standard addresses of 3F8H–3FFH for COM1 and 2F8H–2FFH for COM2. These addresses are software configurable. Standard input and output with the COM ports is accomplished with BIOS calls through interrupt 14H. These calls are fully described in Section 3 of Advanced MS-DOS.

The V5C incorporates a COM2 with additional functionality. COM2 can be configured for an RS-232, RS-422, or RS-485 driver type. The COM2 driver type can be configured in the Setup utility, as well as by using bit 7 of the Serial Switch (See Serial Switch below).

WARNING: Be sure that the type of driver selected matches the type of actual connection. The differences in driver voltages and currents between the driver types may cause damage to a connection of a different driver type. Changing the COM2 configuration while the COM2 port has a connection is not recommended.

Parallel Port

The parallel port is also provided by the ALI 1543C and is typically used for interfacing to Centronics-compatible parallel printers. MS-DOS defines the device, PRN, as the normal printer output device of the system. Therefore, the programmer should not require access to the parallel port directly. Rather, printer services available through the AT BIOS at interrupt 17H should be used. AT BIOS services are fully described in Section 3 of Advanced MS-DOS. Also, be aware that the parallel port of the V5C is capable of SPP, ECP and EPP modes.

Keyboard/Mouse Port

The ALI 1543C Southbridge has built-in PS2/AT Keyboard and PS2 Mouse Controllers. Built into the AT BIOS are calls for keyboard services using interrupt 16H. Section 3 of Advanced MS-DOS describes these calls in detail.

Real Time Clock

The Real-Time Clock of the V5C is equivalent to the Motorola 146818A and is contained in the DS12887 IC. The RTC occupies 3FH indexed locations and contains registers for clock timekeeping and control, as well as 16 bytes of scratchpad RAM (reserved for use by AT Setup). As long as battery power is provided, the clock will continue updating the date and time registers as well as preserve the contents of the scratchpad RAM.

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Accessing the RTC is accomplished by first writing the index address to I/O port address 70H. The valid index address range is 0-7FH. The first 40H locations are used by the V5C, while the remaining 40H are available for general use. The register or RAM data can then either be written or read at I/O port address 71H. The specific use of clock registers is covered in the data sheet on the Motorola 146818A.

Notice: The RTC clock is a 100-year device. No hardware provisions exist to denote the rollover in the year 2000. An attempt to circumvent this problem has been implemented in the BIOS. However, advanced operating systems such as Windows NT do not use the BIOS to interface to the RTC. As such, they may display the year 2000 as the year 1900, etc.

Non-Volatile RAM

The V5C uses the Simtek© STK14C88, 32-pin 32k x 8 Non Volatile SRAM. The NVSRAM has the ability to store data indefinately without the need for batteries or other power sources.

Reset Control Register

The Reset Control Register is used to configure the sources and effects of reset conditions. The register is located at I/O address 2A0H.

RST	VRSTU	RSV	FPSR	SYSRST	RST	RSTEN	ENVME
7	6	5	4	3	2	1	0

Figure 6-1 Reset Control Register (I/O 2A0H)

Bit 0: From VME SYSRST buffer to UNI SYSRST input control. Enables reset from the VMEbus.

Bit 1: Enables bit 2A0[7] to cause reset. This bit must be set before 2A0[7] is set and must remain set when 2A0[7] is set.

Bit 2: Indicates reset ocurred from 2A0[7]. Write 1 to clear.

Bit 3: System Reset or Power up indicator.

Bit 4: From UNI SYSRST to VME. Enables reset to the VMEbus.

Bit 5: Reserved

Bit 6: Reset VME via Universe IIB control. VMERST will cause the Universe chip to assert VXSYSRST while bit 4 is set. Bit 4 must be cleared to de-assert VMERST.

Bit 7: Setting this bit causes an equivalent to a front panel reset if 2A0[1] has been set in a prior write.

NOTE: To clear the 0x2A4[7,5,4] bits, read 0x2a4, shift right 1 bit and write to 0x2A0 to clear.

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BIOS Control Register

The BIOS Control Register controls the write enables to both the onboard FLASH BIOS and the BIOS socket. The register is located at I/O address 2A1H.

BSEL	SBWE	OBWE	FHDU	FDOC	SCSW	RSX	STRM
7	6	5	4	3	2	1	0

Figure 6-2 BIOS Control Register (I/O 2A1H)

Bit 0: Eight bit SCSI bus termination. 1 = On, 0 = Off. For system operation with the V5C as the first device in the SCSI chain this bit must be set to On.

Bit 1: This bit controls the selection of the COM2 serial port mode. 0 = RS-232 and 1 = RS-485.

Bit 2: Upper 8-bit SCSI Wide Termination control. 1 = On.

Bit 3: FDOC2k control. 1 = On.

Bit 4: RS-485 Receive Data Control. 0 = Half Duplex, 1 = Full Duplex. This control allows the COM2 RTS (Request To Send) signal to prevent transmitted data from being received during half-duplex operation. This signal must be high for correct full-duplex operation.

Bit 5: This bit enables programming the onboard FLASH BIOS. For normal operation, this bit should be clear so that the onboard BIOS is a read-only device. It should not be set by user programs.
WARNING: Setting this bit makes the BIOS susceptible to data corruption.

Bit 6: This bit enables programming of a FLASH ROM in the BIOS socket. For normal operation, this bit should be clear so that any socketed ROM is a read-only device. It should not be set by user programs. ***WARNING: Setting this bit makes a FLASH device in the socket suceptable to data corruption.***

Bit 7: This bit controls the location of the chip select line for the bios. Setting this bit to 1 enables the chip select for the on board flash device, disabling the socketed chip select line. Clearing this bit enables the socketed flash chip select line while disabling the on board chip select line.

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User Register

User Register implementation. The register is located at I/O address 2A2H.

SYS	RSV	RSV	RSV	RSV	RSV	RSV	CM1X
7	6	5	4	3	2	1	0

Figure 6-3 User Register (I/O 2A2H)

Bit 0: COM1 shutdown. 1 = shutdown.

Bit 1: Reserved.

Bit 2: Reserved

Bit 3: Reserved

Bit 4: Reserved.

Bit 5: Reserved

Bit 6: Reserved

Bit 7: Setting this bit illuminates the SYS LED on the V5C front panel. The purpose is user-defined. Reading this bit returns the opposite of the value written.

Serial EEPROM Register

The Serial EEPROM Register provides a direct interface to the program, data, and clock lines of the serially-programmable EEPROM (see Serial EEPROM below). Programming of this device requires knowledge of device-specific timing requirements, and should be done cautiously. Refer to the National Semiconductor *NM93C66 User's Manual* if you need to access this part directly.

The Serial EPROM Register is an eight-bit register at I/O address 2A3H. The bits are defined as follows:

RSV	OEECS	SDI	RSV	RSV	RSV	SDO	CLK
7	6	5	4	3	2	1	0

Figure 6-4 Serial EEPROM Register (I/O 2A3H)

Bit 0: EEPROM Data Out. To Serial EEPROM (Data In).

Bit 1: Directly connected to the DI pin of the NM93C46. It is used to send **data** to the Serial EEPROM.

Bits 2-4: Reserved.

Bit 5: EEPROM Data In. From Serial EEPROM (Data Out).

Bit 6: Serial EEPROM Chip Select (R/W)
This bit is directly connected to the CS pin of the NM93C46. It selects the NM93C46 chip, making it active and ready for read or write cycles.

Bit 7: Reserved.

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Serial EEPROM

The V5C uses a 64x16 bit serially-accessed Electrically Erasable Programmable Read Only Memory, or EPROM. This part is the National Semiconductor NM93C46, and is used for storing board setup and configuration data for SETV5C and the VME BIOS. Programming the EEPROM is facilitated through the Serial EPROM Register (see Serial EPROM Register above). However, user programs should make use of the EEPROM only under special circumstances. SBS Embedded Computers can provide more information about programming the EEPROM, including the dangers of doing so.

The EEPROM is 64 words in size. The first 43 words are used for VME setup values and board setup information. The remaining 21 words are available for general use.

Note: Like most EEPROM devices, the NM93C46 has a limited lifetime for write cycles. For the NM93C46, the average device life is 10^6 write cycles. Conservative use of the EEPROM will ensure that it lasts the life of the board.

Byte Swapping Control Register

Byte Swapping Control register

The Byte Swapping control register is used to configure the operation of the hardware byte swapping circuitry. The register is located at I/O address 2A4.

RSV	RSV	RSV	RSV	BYM1	BYM0	BYS1	BYS0
7	6	5	4	3	2	1	0

Figure 6-5 Byte Swapping Control Register (I/O 2A4H)

	Master		Slave	
	BYM1	**BYM0**	**BYS1**	**BYS0**
M32	0	1	0	1
I32	0	0	0	0
I16	1	0	1	0

Bit	**Description**
0-1	These bits control the byte swap mode when doing a VME Slave transfer.
2-3	These bits control the byte swap mode when doing a VME Master transfer.
4-7	Reserved.

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PLD Revision Register

PLD Revision Register Implementation (Limit of 256 Revisions).

PLD7	PLD6	PLD5	PLD4	PLD3	PLD2	PLD1	PLD0
7	6	5	4	3	2	1	0

Figure 6-7 PLD Revision Register (I/O 2A6H)

Bit 0: Hex bit 0 (Read Only).

Bit 1: Hex bit 1 (Read Only).

Bit 2: Hex bit 2 (Read Only).

Bit 3: Hex bit 3 (Read Only).

Bit 4: Hex bit 4 (Read Only).

Bit 5: Hex bit 5 (Read Only).

Bit 6: Hex bit 6 (Read Only).

Bit 7: Hex bit 7 (Read Only).

Board Status Register

Board Status Register Implementation. Bits are Read Only. Any ***Write*** to this Register resets the Watchdog Counter.

RSV	HDBS	VSYSFL	RSV	RSV	RSV	RSV	IOCHK
7	6	5	4	3	2	1	0

Figure 6-8 Board Status Register (I/O 2A7H)

Bit 0: (R) IOCHK (1 = Asserted).

Bits 1-4: Reserved.

Bit 5: (R) VME SYSFAIL (1 = Asserted).

Bit 6: (R) Hardware Boot Select.

Bit 7: Reserved.

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Board Status Register 2

Board Status Register Two, and NVRAM Address Control.

TB51	NVSEN	RSV	RSV	RSV	RSV	STFL	BPP5
7	6	5	4	3	2	1	0

Figure 6-9 Board Status Register 2 (I/O 2A8H)

Bit 0: (R) P5 VME Backplane Detect (1 = P5 Present).

Bit 1: (R) NVSRAM Store Flag (1 = Store in Progress).

Bit 2: Reserved

Bit 3: Reserved

Bit 4: Reserved

Bit 5: Reserved

Bit 6: {W/R} NVSRAM Enable.

Bit 7: {R} TB51 Detect. 1 = TB51 Present.

* These register bits are reserved for paging control of the NVSRAM. This function is not implemented in this version of the equations

Intel® Dual HiQVideo™ Accelerator Engine

The 69030 graphics accelerator is designed to support high performance graphics and video acceleration for all supported video resolutions, display types and color modes. Primarily, you should not need to program the video controller directly, because the Video BIOS provides functions for video operation through interrupt 10H. These are fully defined in Section 3 of Advanced MS-DOS. However, if it becomes necessary to program the controller directly, refer to the Intel Corporation 69030 Databook.

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CHAPTER 7 Byte Swapping

Byte Swapping Modes

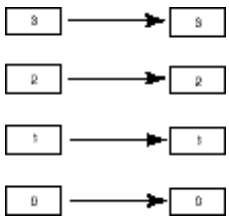
Byte Swapping

The V5C has Byte Swapping implemented in hardware. This allows for proper data transfer between the PCI and VME busses. The hardware implementation is much faster than a software implementation since no extra processor time is devoted to this task. Supported modes are: No swapping (M32), 32 bit swapping (I32), and 16 bit swapping (I16). Note that byte swapping is not applied to status ID's associated with interrupt processing.

Type of VMEbus Access	Byte Swapping Modes		
	M32	I32	I16
Byte	Valid	Invalid	Invalid
Word	Valid	Invalid	Valid
Long Word	Valid	Valid	Invalid

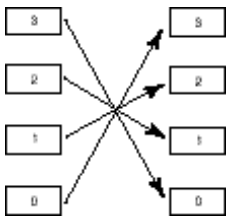
Mode M32

M32 allows data to transfer with no swapping of the bytes. All address and data modes are supported with M32 since there is no swapping of bytes. M32 is the default setting in the BIOS setup.



Mode I32

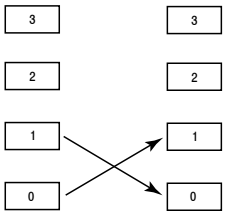
I32 allows conversion of big-endian to little-endian on a 32-bit transfer. Supported address modes are A16, A24, and A32. Supported data mode is D32. As can be seen from the diagram on a four-byte transfer, bytes 0 and 3 are swapped, and bytes 1 and 2 are swapped.



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Mode I16

I16 allows conversion of big-endian to little-endian on a 16-bit transfer. Supported address modes are A16, A24, and A32. Supported data mode is D16. As can be seen from the diagram on two-byte transfer, bytes 0 and 1 are swapped.



The recommended method of controlling the byte swap mode is through the BIOS Setup program. Under the VME system menu both slave and master byte swapping can be set by the user. Another method of controlling byte swapping is through the register located in ISA space.

Byte swapping can be user controlled by a register in ISA space. This register is located at 2A4. Byte swap mode and bit settings are shown in the table below. By changing the bits in this register the user can change the mode of byte swapping. Note that the byte swapping mode will not be changed until the VME bus is inactive. This prevents the byte swap mode from changing while a transfer is in progress.

Byte Swapping Mode By Control Register

RES	RES	RES	STAT	BYM1	BYM0	BYS1	BYS0
7	6	5	4	3	2	1	0

Byte Swapping Control Register
The Byte Swapping control register is used to configure the operation of the hardware byte swapping circuitry. The register is located at I/O address 2A4.

	Master		Slave	
	BYM1	**BYM0**	**BYS1**	**BYS0**
M32	0	1	0	1
I32	0	0	0	0
I16	1	0	1	0

Bit	**Description**
0-1	These bits control the byte swap mode when doing a VME Slave transfer.
2-3	These bits control the byte swap mode when doing a VME Master transfer.
4	If bits 0-3 are modified, the new mode is not in effect until the VMEbus is inactive. Bit 4 of the byte swapping register is read-only and indicates when the mode specified by by bits 0-3 is in effect.

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CHAPTER 8 Specifications

General

Model	V5C
Description	PC99 Design Guide Compatible VMEbus Single Board Computer
Hardware Compatibility	VMEbus Dual Eurocard, VME64 ANSI/VITA 1-1994

VMEbus

Controller	Tundra Universe IIB
Configuration	DTB Master, Option A32/A24/A16, D32/D16/D08(EO), RMW DTB Slave, Option A32/A24/A16, D32/D16/D08(EO), RMW
Interrupter	Programmable, 1-of-7
Interrupt Handler	Programmable, IH(1-7)
Requester	Programmable, BR(3,2,1,0), Option ROR and RWD
Arbiter	RRS, PRI, SGL
Block Mode Transfer	Master/Slave BLT and MBLT D64/D32/D16

CPU

Intel	Pentium III / Celeron

PCI Bus

Controller	ALI Aladdin-Pro II Chip Set, 1621 Northbridge
Clock Rate	33MHz

PC/AT Bus

Controller	ALI Aladdin-Pro II Chip Set, 1543C Southbridge
Clock Rate	8.0 MHz

Serial Interface

Controller	ALI Aladdin-Pro II Chip Set, 1543C Southbridge
Number	2 Com Ports
Compatibility	IBM PC
Interface Type	COM1: RS-232; COM2: RS-232/422/485 *(Due to common physical environment, COM2 RS-422/RS-485 function is constrained to ±30V limitation of RS-232 port.)*
Signals Provided	RxD, TxD, RTS, CTS, DSR, DTR, DCD, RI
Connector	DB9P

Parallel Interface

Controller	ALI Aladdin-Pro II Chip Set, 1543C Southbridge
Number	1 Parallel Port
Compatibility	Centronics Parallel, PS/2 Bidirectional
Interface	Buffered Parallel
Connector	Micro-Miniature DB25S

Mouse / Keyboard Interface

Controller	ALI Aladdin-Pro II Chip Set, 1543C Southbridge
Compatibility	Microsoft Mouse and PS/2 style Keyboard resident in a single 6-Pin mini-connector reverse IBM standard. Keyboard Default, Mouse through Adapter
Connector	6-pin Circular Mini-DIN

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Video Interface

Controller	Intel 69030
Compatibility	VGA/SVGA
Capability	1280×1024×256 colors, 1024x768x64k, 800×600×16.7M, 680x480x16.7M colors
Display Supported	Color CRT/ LED simultaneous mode support
Connector	HD15S
Video Memory	4 Megabytes of Video RAM

Disk Drive Interface

Floppy Disk	ALI 1541C-B1 provides Control Through P2
Hard Disk	Bus Mastering IDE Interface Provided Through P2 Ultrafast SCSI-2 Interface Provided Through P2
Compact Flash Disk	Mounted On-Board

Ethernet Interface

Type	IEEE 802.3 Dual 10/100BaseT (Twisted Pair), Provided Through two Front Panel RJ45 connectors

Electrical

Power	+5VDC @ 6A with 256MB at 850MHz (Typical) +12VDC @ 10mA + PMC requirements -12VDC @ (Dependent on PMC card current usage only)

Physical

Size	160mm × 233mm (Dual Eurocard), 6U×4HP
Construction	Multi-Layer Printed Circuit, FR-4 with Flammability rating of 94V-0 by UL recognized manufacturers

Environmental

Temperature	0 to 55° Celsius Inlet Air, Operating -40 to 85° Celsius, Non-Operating
Cooling	Forced Air, 100LFM Fan Recommended
Humidity	10 to 95% Relative Humidity, Non-Condensing
Shock	6G Max. Operating, 10G Max. Non-Operating

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CHAPTER 9

Support, Service, and Warranty

Chapter Scope

The following sections describe SBS Technologies product support program. It states our product warranty terms and provides details about what action to take if you experience a problem with the product.

Warranty Statement

SBS Technologies CPU products come with a “return-to-factory” warranty that covers defects in materials and workmanship for a period of two years from the date of product shipment to the customer (original purchaser), provided the product is unmodified and has been subject to normal and proper use. This warranty applies to all standard board-level products which do not incorporate disk drives. Products which incorporate floppy or hard disk drives are also warranted for two years with the exception of the drives themselves. The drives will be warranted for a period of ninety days, according to the normal period for electromechanical components. SBS Technologies makes no warranty or representation, express or implied, with respect to software, its performance, quality, or fitness for a particular purpose. This does not include the media on which the software is distributed, which carries a warranty covering defects in materials and workmanship for a period of ninety days.

If You Have a Problem with an SBS Product

Technical support is available by phone, fax or email. Telephone suppport is available during the following Eastern Time hours:

Monday through Friday 8:30 am - 5:30 pm.

You can reach technical support at:

(919) 851-1101 (voice)
(919) 851-2844 (fax)
support@sbs.com (email)

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Product Repairs

To expedite assistance for problems, be able to provide the following:

- Your Name, Phone and Company.
- Product with which you are having trouble.
- Serial Number and Revision.
- Operating system you are running.
- Detailed description of your problem and any error messages that have appeared on the screen.

Depending on the circumstances of the problem, it may be deemed necessary to return the product to SBS Technologies for repair. In order to return the product for repair, the following steps are necessary:

1. Obtain a Return Material Authorization number (RMA#) from SBS Customer Support.

2. Ship the product prepaid to the designated repair point.

3. Provide a written description of the claimed defect with the product.

Obtaining an RMA Number

To obtain a product return authorization number (RMA#), you should call our Customer Service department through our main number.

Shipping the Product

Any product returned to SBS should be in its original shipping carton if possible. Otherwise the product should be carefully packaged in a conductive packing material and placed in a cushioned corrugated carton suitable for shipping. Please mark the shipping label with the RMA number and return it to:

Customer Service Department
Att: RMA# *(put RMA number here)*
SBS Technologies, Inc.
6301 Chapel Hill Road
Raleigh, NC 27607

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Providing a Product Defect Report

When you are returning a product for repair, it is very important to include a written report which details the nature of the problem in order to expedite the repair. Please make sure that the following information is included:

- RMA Number
- Product:
- Serial Number
- Contact:
- Phone
- Description of the Problem/Defect

Warranty Repairs

Any product returned and found to be under warranty will be repaired or replaced at the discretion of SBS Technologies.

Non-Warranty Repairs

If a product is found not to be under warranty, we will notify you of the non-warranty situation and provide you with a fixed cost and a schedule for the repair. Non-warranty repairs generally require that a purchase order be issued to SBS Technologies Inc. for the amount of the repair before repairs are undertaken.

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APPENDIX

VME Address Modifier Codes

The following table shows the standard VME address modifier codes. Codes 10H through 1FH are user-defined. All other codes are reserved.

Address Modifier	Address Size	Transfer Type
3FH	24	Standard Supervisory Block Transfer (BLT)
3EH	24	Standard Supervisory Program Access
3DH	24	Standard Supervisory Data Access
3BH	24	Standard Non-Privileged Block Transfer (BLT)
3AH	24	Standard Non-Privileged Program Access
39H	24	Standard Non-Privileged Data Access
38H	24	Standard Non-Privileged 64-bit Block Transfer (MBLT)
37H	40	A40 BLT
35H	40	A40 Lock Command (LCK)
34H	40	A40 Access
32H	24	A24 Lock Command (LCK)
2FH	N/A	Configuration ROM/Control & Status Register
2DH	16	Short Supervisory Access
2CH	16	A24 Lock Command (LCK)
29H	16	Short Non-Privileged Access
0FH	32	Extended Supervisory Block Transfer (BLT)
0EH	32	Extended Supervisory Program Access
0DH	32	Extended Supervisory Data Access
0CH	32	Extended Supervisory 64-bit Block Transfer (MBLT)
0BH	32	Extended Non-Privileged Block Transfer (BLT)
0AH	32	Extended Non-Privileged Program Access
09H	32	Extended Non-Privileged Data Access
08H	32	Extended Non-Privileged 64-bit Block Transfer (MBLT)
05H	32	A32 Lock Command (LCK)
04H	64	A64 Lock Command (LCK)
03H	64	A64 Block Transfer (BLT)
01H	64	A64 Single Transfer Access
00H	64	A64 64-bit Block Transfer (MBLT)

Table E-1 Address Modifier Codes

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