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CP-340

PMC Carrier for
3U CompactPCI® with
Front-Panel I/O

User Manual

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CP-340
PMC Carrier for
3U CompactPCI with
Front-Panel I/O

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Table of Contents

PRODUCT DESCRIPTION 1

KEY FEATURES 1

PMC SLOTS 2

OVERVIEW 2

PCI SLOTS 2

PCI-TO-PCI BRIDGE 2

COMPACTPCI HOT SWAP 3

HOT SWAP REGISTER 3

CONNECTORS 4

OVERVIEW 4

CONNECTOR SIGNAL ASSIGNMENT 4

CompactPCI Connector Pin Assignment *4*

J1 4

J2 5

PMC Connectors For PCI Interface *6*

P11/J11 6

P12/J12 7

P13/J13 8

SPECIFICATIONS 9

REPAIR 10

SERVICE POLICY 10

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List of Figures

FIGURE 1: PMC SLOT ASSIGNMENTS 2
FIGURE 2: PMC SLOT COMPATIBILITY SUMMARY 2
FIGURE 3: PCI CONFIGURATION REGISTERS 2
FIGURE 4: HOT SWAP REGISTER 3
FIGURE 5: CONNECTOR SUMMARY 4
FIGURE 6: COMPACTPCI J1 CONNECTOR PIN ASSIGNMENT 4
FIGURE 7: COMPACTPCI J2 CONNECTOR PIN ASSIGNMENT 5
FIGURE 8: PMC CONNECTOR P11/J11 PIN ASSIGNMENTS 6
FIGURE 9: PMC CONNECTOR P12/J12 PIN ASSIGNMENTS 7
FIGURE 10: PMC CONNECTOR P13/J13 PIN ASSIGNMENTS 8

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Product Description

The CP-340 mezzanine carrier board holds one PCI Mezzanine Card (PMC) with front - panel I/O support in a single 3U CompactPCI® slot. The CP-340 is ideal for use in high-performance industrial, COTS, and telephony CompactPCI systems that require I/O expansion using the PMC form factor.

Using the industry standard Intel 21154-BC PCI-to-PCI Bridge, the CP-340 supports a 64-bit data path at 66 MHz, for 512 MB/s operation. The PMC site supports bus mastering.

The CP-340 carrier board complies with the PICMG 2.0, version 3.0 CompactPCI specification.

Key Features

3U CompactPCI carrier board holds one PMC

64-bit, 33/66 MHz, up to 512 MB/s operation

Full hot swap capability

Status LEDs for Power (green) and Hot Swap (blue)

Intel 21154-BC PCI-to-PCI Bridge

Supports standard (IEEE1386.1) PMCs

CompactPCI specification, PICMG 2.0, version 2.1 compliant

Front-panel I/O supports PMC site

5V PCI signaling for the PMC site (CP-340-5) or 3.3V PCI signaling (CP-340-3)

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PMC Slots

Overview

A PMC slot is provided, as shown in Figure 1:

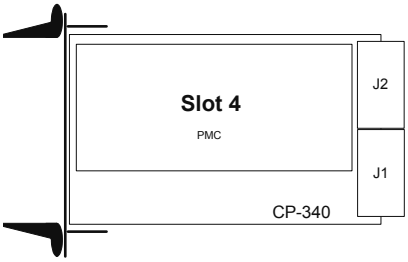


Figure 1: PMC Slot Assignments

PCI Slots

Each slot is a hard-wired PCI slot and has front and back-panel I/O access as shown in Figure 2:

Slot	Card	Front-Panel I/O Location	Bus Master
4	PMC	On card	Yes

Figure 2: PMC Slot Compatibility Summary

PCI-to-PCI Bridge

The PCI bridge chip, an Intel 21154-BC, is a transparent 32/64-bit, 33/66 MHz device. The PMC on the carrier is visible to the system CPU.

The wiring of the bridge to the PMC slots controls the mapping of PCI slot numbers to physical slots. The PCI slot for the PMC is 4.

The bridge implements the interrupt mapping for the PMC slot. This mapping is defined by the PCI specification.

The bridge implements the bus mastership control for the PMC slot. A two-level round-robin arbiter selects one master between slot 4 and the host PCI bus. Figure 3 lists the salient configuration registers:

Location	Value	Description
Vendor ID	0x1011	Intel, the manufacturer of the chip
Device ID	0x0026	21154-BC PCI to PCI Bridge chip
Revision	0x0005	21154-BC chip revision

Figure 3: PCI Configuration Registers

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CompactPCI Hot Swap

The CP-340 hot swap functionality is implemented using the “alternate register” method as defined in section 2.3.2.4 in the PICMG 2.1 R1.0 CompactPCI Hot Swap Specification. The 21154 PPB is not hot swap “silicon friendly”. That is, it does not have the hot swap Control and Status register as part of its configuration registers.

A General Purpose I/O (GPIO) register is located in the 21154’s configuration registers. This register has 4 bits, each of which can be programmed as input or output. Also, each of these 4 bits corresponds to an I/O pin on the 21154 PPB. Bit GPIO<3> is defined as the INS bit, Bit GPIO<2> is defined as the EXT bit, Bit GPIO<1> is defined as the LOO bit, and Bit GPIO<0> is defined as the EIM bit.

Hot Swap Register

The Hot Swap register starts at offset 65H (GPIO Output Data) from the 21154’s PCI configuration space. The LOO and EIM bits are output only, while the INS and EXT bits are inputs as well as outputs. Therefore, the pins must be configured as input during read cycles and, whenever a write must be performed, the pins must then be set to output and then back to input. The reset configuration is input.

Figure 4 shows the Hot Swap register.

MSB															LSB	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Bit
GPIO Input Data								GPIO Output Enable Control								Register
INS	EXT	X	X	X	X	X	X	1 = INS out	1 = EXT out	1 = LOO out	1 = EIM out	1 = INS in	1 = EXT in	X	X	Bits Definition

MSB															LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bit
GPIO Output Data								P_serr_l Event Disable								Register
1= INS set	1= EXT set	1= LOO set	1= EIM set	1= INS clear	1= EXT clear	1= LOO clear	1= EIM clear									Bits Definition

Figure 4: Hot Swap Register

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Connectors

Overview

Connectors are fitted as shown in Figure 5.

Connector	Wired To	Description
J1	PCI Bridge	CompactPCI bus
J2	PCI Bridge	CompactPCI bus
J11, J12, J13	PCI Bridge	PCI bus for slot 4

Figure 5: Connector Summary

Connector Signal Assignment

CompactPCI Connector Pin Assignment

J1

	Row					
Position	A	B	C	D	E	F
25	+5V	REQ64#	ENUM#	+3V	+5V	GND
24	AD[1]	+5V	V[I/O]	AD[0]	ACK64#	GND
23	+3V	AD[4]	AD[3]	+5V	AD[2]	GND
22	AD[7]	GND	+3V	AD[6]	AD[5]	GND
21	+3V	AD[9]	AD[8]	M66EN	CBE[0]#	GND
20	AD[12]	GND	V[I/O]	AD[11]	AD[10]	GND
19	+3V	AD[15]	AD[14]	GND	AD[13]	GND
18	SERR#	GND	+3V	PAR	CBE[1]#	GND
17	+3V	N/C	N/C	GND	PERR#	GND
16	DEVSEL#	GND	V[I/O]	STOP#	LOCK#	GND
15	+3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND
14	Key	Key	Key	Key	Key	GND
13	Key	Key	Key	Key	Key	GND
12	Key	Key	Key	Key	Key	GND
11	AD18	AD[17]	AD[16]	GND	CBE[2]#	GND
10	AD21	GND	+3V	AD[20]	AD[19]	GND
9	CBE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	AD[26]	GND	V[I/O]	AD[25]	AD[24]	GND
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	REQ#	GND	+3V	CLK	AD[31]	GND
5	N/C	N/C	RST#	GND	GNT#	GND
4	N/C	Healthy#	VIO	N/C	N/C	GND
3	INTA#	INTB#	N/C	+5V	N/C	GND
2	N/C	+5V	N/C	TDO	TDI	GND
1	+5V	-12V	N/C	+12V	+5V	GND

Figure 6: CompactPCI J1 Connector Pin Assignment

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J2

	Row					
Position	**A**	**B**	**C**	**D**	**E**	**F**
22	PU-V(I/O)	PU-V(I/O)	PU-V(I/O)	PU-V(I/O)	PU-V(I/O)	GND
21	N/C	N/C	N/C	N/C	N/C	GND
20	N/C	N/C	N/C	GND	N/C	GND
19	N/C	N/C	N/C	N/C	N/C	GND
18	N/C	N/C	N/C	GND	N/C	GND
17	N/C	GND	N/C	N/C	N/C	GND
16	N/C	N/C	N/C	GND	N/C	GND
15	N/C	GND	N/C	N/C	N/C	GND
14	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
13	A0[38]	GND	V(I/O)	AD[37]	AD[36]	GND
12	AD[42l	AD[41]	AD[40]	GND	AD[39]	GND
11	AD[45]	GND	V(I/O)	AD[44]	AD[43]	GND
10	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
9	AD[52]	GND	V(I/O)	AD[51]	AD[50]	GND
8	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	AD[59]	GND	V(I/O)	AD[58]	AD[57]	GND
6	AD[63]	AD[62]	AD[61l	GND	AD[60]	GND
5	C/BE[5]#	64EN#	V(I/O)	C/BE[4]#	PAR64	GND
4	V(I/O)	GND	C/BE[7]#	GND	C/BE[6]#	GND
3	N/C	GND	N/C	N/C	N/C	GND
2	N/C	N/C	N/C	N/C	N/C	GND
1	N/C	GND	N/C	N/C	N/C	GND

Figure 7: CompactPCI J2 Connector Pin Assignment

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PMC Connectors For PCI Interface

The following three figures list the PCI interface pin assignments for the PMC slot.

P11/J11

Pin #	Signal Name		Signal Name	Pin #
1 (PD)	TCK		-12V	2
3	Ground		INTA#	4
5	INTB#		INTC#	6
7(N/C)	BUSMODEI#		+5V	8
9	INTD#		PCI-RSVD	10 (N/C)
11	Ground		PCI-RSVD	12 (N/C)
13	CLK		Ground	14
15	Ground		GNT#	16
17	REQ#		+5V	18
19	V (I/O)		AD[31]	20
21	AD[28]		AD [27]	22
23	AD[25]		Ground	24
25	Ground		C/BE[3]#	26
27	AD[22]		AD[21]	28
29	AD[19]		+5V	30
31	V (I/O)		AD[17]	32
33	FRAME#		Ground	34
35	Ground		IRDY#	36
37	DEVSEL#		+5V	38
39	Ground		LOCK#	40
41 (PU)	SDONE#		SBO#	42 (PU)
43	PAR		Ground	44
45	V (I/O)		AD[15]	46
47	AD[12]		AD[11]	48
49	AD[09]		+5V	50
51	Ground		C/BE[O]#	52
53	AD[06]		AD[05]	54
55	AD[04]		Ground	56
57	V (I/O)		AD[03]	58
59	AD[02]		AD[01]	60
61	AD[00]		+5V	62
63	Ground		REQ64#	64 (PU)

Figure 8: PMC Connector P11/J11 Pin Assignments

N/C = Not Connected, PU = Pull-up, PD=Pull-down

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P12/J12

Pin #	Signal Name		Signal Name	Pin #
1	+12V		TRST#	2 (PD)
3 (PU)	TMS		TDO	4 (N/C)
5 (N/C)	TDI		Ground	6
7	Ground		PCI-RSVD	8 (N/C)
9 (N/C)	PCI-RSVD		PCI-RSVD	10 (N/C)
11 (PU)	BUSMODE2#		+3.3V	12
13	RST#		BUSMODE3#	14(GND)
15	3.3V		BUSMODE4#	16(GND)
17 (N/C)	PCI-RSVD		Ground	18
19	AD[30],		AD[29]	20
21	Ground		AD[26]	22
23	AD[24]		+3.3V	24
25	IDSEL		AD[23]	26
27	+3.3V		AD[20]	28
29	AD[18]		Ground	30
31	AD[16]		C/BE[2]#	32
33	Ground		PMC-RSVD	34 (N/C)
35	TRDY#		+3.3V	36
37	Ground		STOP#	38
39	PERR#		Ground	40
41	+3.3V		SERR#	42
43	C/BE[1]#		Ground	44
45	AD[14]		AD[13]	46
47	Ground		AD[10]	48
49	AD[08]		+3.3V	50
51	AD[07]		PMC-RSVD	52 (N/C)
53	+3.3V		PMC-RSVD	54 (N/C)
55 (N/C)	PMC-RSVD		Ground	56
57 (N/C)	PMC-RSVD		PMC-RSVD	58 (N/C)
59	Ground		PMC-RSVD	60 (N/C)
61 (N/C)	ACK64#		+3.3V	62
63	Ground		PMC-RSVD	64 (N/C)

Figure 9: PMC Connector P12/J12 Pin Assignments

N/C = Not Connected, PU = Pull-up, PD=Pull-down

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P13/J13

Pin #	Signal Name		Signal Name	Pin #
1 (N/C)	PMC-RSVD		Ground	2
3	Ground		C/BE[7]#	4
5	C/BE[6]#		C/BE[5]#	6
7	C/BE[4]#		Ground	8
9	V (I/O)		PAR64	10
11	AD[63]		AD[62]	12
13	AD[61]		Ground	14
15	Ground		AD[60]	16
17	AD[59]		AD[58]	18
19	AD[57]		Ground	20
21	V (I/O)		AD[56]	22
23	AD[55]		AD[54]	24
25	AD[53]		Ground	26
27	Ground		AD[52]	28
29	AD[51]		AD[50]	30
31	AD[49]		Ground	32
33	Ground		AD[48]	34
35	AD[47]		AD[46]	36
37	AD[45]		Ground	38
39	V (I/O)		AD[44]	40
41	AD[43]		AD[42]	42
43	AD[41]		Ground	44
45	Ground		AD[40]	46
47	AD[39]		AD[38]	48
49	AD[37]		Ground	50
51	Ground		AD[36]	52
53	AD[35]		AD[34]	54
55	AD[33]		Ground	56
57	V (I/O)		AD[32]	58
59 (N/C)	PMC-RSVD		PMC-RSVD	60 (N/C)
61 (N/C)	PMC-RSVD		Ground	62
63	Ground		PMC-RSVD	64 (N/C)

Figure 10: PMC Connector P13/J13 Pin Assignments

N/C = Not Connected, PU = Pull-up, PD=Pull-down

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Specifications

Form Factor	3U CompactPCI
PMC Sites	One
Carrier Interface	CompactPCI, PICMG 2.0, version 2.1 compliant
PCI	PCI Specification, Revision 2.2 compliant
PMC Interface	IEEE1386.1 PMC
PCI Bridge	Intel 21154-BC PCI-to-PCI Bridge
PCI Bus Master	PMC slot through a transparent bridge
I/O Access	Front panel
Power Requirements	+3.3 VDC, 90 mA max Additional power consumed by PMCs
Dimensions	100 mm x 160 mm
Weight	0.26 kg (0.56 lb)
Environmental	Operating temperature: 0° to 70° C Humidity: 5% to 95% non-condensing Storage: -40° to +85°C

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