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Digital Voltmeter 7075



Part No. 70750011

Issue 3, January 1978

Schlumberger

THE SOLARTRON ELECTRONIC GROUP LIMITED
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TECHNICAL MANUAL

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Solartron pursue a policy of continuous development and product improvement. The specifications in this document thus may be changed without notice.

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SECTION 1 General Description

The 7075, with its simple to use controls and clear, easy-to-read display enables the most inexperienced user to discover that precise digital measurement is now within his grasp.

Automatic range selection means that there is, basically, only one operator decision to be made - that of the quantity to be measured : dc volts, ac volts or resistance. The instrument instantaneously evaluates the order of magnitude of the applied input and selects the appropriate range.

Ranging Points: (5 x 9's)

Range-up > 140 000 digits reading.

Range-down < 12 000 digits reading.

N.B. Excessive series mode signals may cause range-up to occur earlier.

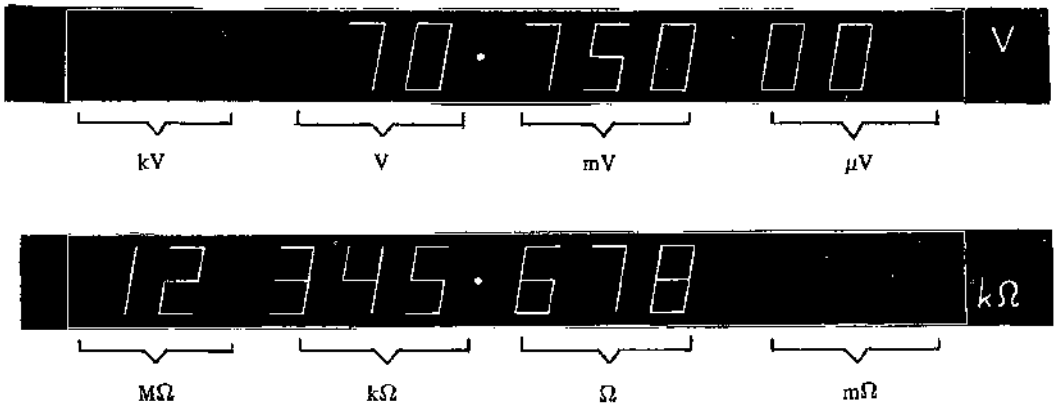
The facilities available are those of:-

DC Voltage	continuous range from 1μV to 1kV
AC (RMS) Voltage	continuous range from 1μV to 750V rms (1.1kV Peak).
Resistance	continuous range from 1mΩ to 14MΩ

True rms measurement: many instruments in the past presented the mean value of an alternating quantity or if rms value was displayed, it was arrived at by some method of 'doctoring' the mean value actually measured. The disadvantage of that system is that validity of the reading is very much dependent on waveform shape, only a pure sinusoidal input giving acceptable results.

The 7075 is a true rms measuring instrument, in which the input is directly converted to its root mean square at the measurement stage. The displayed reading, therefore, is the precisely computed rms value of the alternating quantity being measured.

A twelve decade display is used, bright and sharply defined, no extraneous light being permitted to degrade the displayed reading. The **fixed decimal point** and unique grouping of the displayed digits makes possible an instant appreciation of the order of magnitude of the reading thus obviating the need for multiple and submultiple unit annunciators.



Scale length from 3 x 9's to 7 x 9's can be selected by the user, the above being typical 7 x 9's displays.

The display 'moves' to the right as the applied input reduces in magnitude; leading zeros, except that to the immediate left of the decimal point, are suppressed; and if the quantity is negative the minus sign travels with the display always maintaining its position immediately to the left of the most significant whole digit.

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The new conversion technique used is capable of obtaining linearities two orders better than those possible using dual ramp and related techniques. An important property of this method is that the applied input is being continuously averaged. Together with the very fast autoranging system, this feature makes conventional filters, with their associated problems, unnecessary. A new exclusive **digital filtering** technique is utilised whereby the difficulty that used to be associated with low frequency ac measurement has, with the 7075, become a thing of the past.

Operator confidence is increased by a self check facility. At the touch of a button the instrument can be commanded to carry out a series of tests designed to prove the correct functioning of all its circuits, displaying the result of each check instantaneously.

SAFETY

Your 7075 has been carefully engineered with ease of use as one of the primary considerations. Attention has also been given to making the instrument immune to most inadvertent overloads and to ensuring operator safety. However it should be appreciated that even the most sophisticated of measuring instruments can be dangerous when connected to high voltages, unless elementary safety precautions are observed.

The voltage limit of 1.1kV means that no damage will be caused to the instrument at this level of input. Other than the displayed reading, however, no indication is given to the user that a voltage of such a magnitude is present at the input terminals. Care should therefore be exercised whenever the dvm input leads are being connected to/removed from live circuits, especially where high voltages are known to exist or high transients could occur.

Similarly, when using the instrument on mains operated equipment capable of delivering high voltage outputs, it is strongly recommended that the equipment under test is NOT switched off with the dvm still connected. For example, consider the 7075 connected across the secondary winding of a large mains transformer. The instrument's very high input resistance is such that, in the event of the mains supply being interrupted, the resultant back emf induced in the undamped secondary could be of the order of 100kV. This is obviously hazardous to the user and would certainly harm the voltmeter.

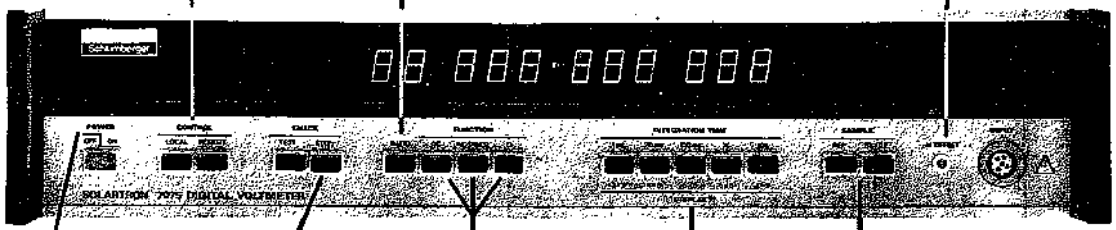
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CONTROL: Permits operation by means of front panel switches, when on LOCAL: or under the control of an external system when REMOTE is selected. REMOTE has no effect in the absence of an Interface Unit. (Note 1).

RATIO: Disconnects internal reference and connects external reference applied to the rear input terminals.

μV OFFSET: Facility for offsetting the effects of externally generated emf's. Applicable on DC and Ω.



DC, AC (RMS), Ω : Used for selection of measurement mode.

REP: Display is repeatedly updated at a rate set by the selected Integration Time.

SINGLE: Display retains last commanded reading. Update occurs each time button is pressed (Note 2).

TEST: Initiates a series of self-check operations.

STEP: Progresses the test routine step-by-step.

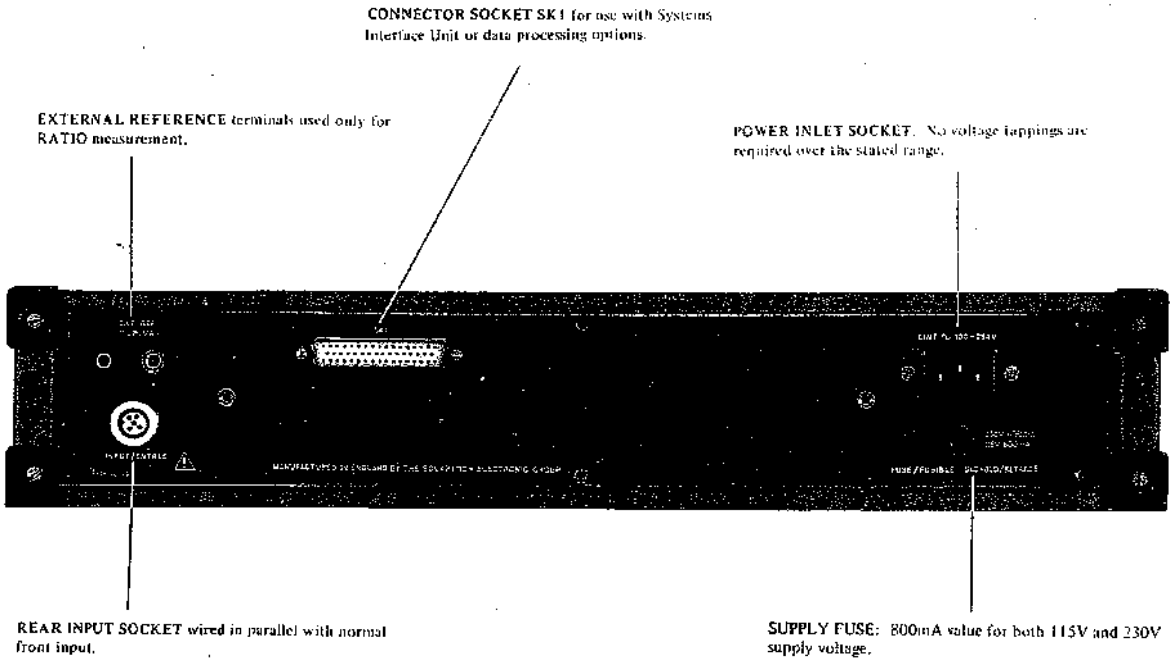
INTEGRATION TIME: Choice of 5 scale lengths by selecting one of 5 integration periods. The longer scale lengths give greater resolution.

POWER: Push-on/push-off. Applies mains power to the instrument. No remote control facility.

NOTES

1. An external command from the Interface Unit, FRONT PANEL LOCKOUT, can be used to inhibit all front panel controls (except POWER).

2. When in SINGLE operation, changes of FUNCTION or INTEGRATION TIME will not be implemented until the SINGLE button is again pressed.



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CONTROLS

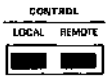
The push button controls are arranged in groups in accordance with the decisions which have to be made for any measurement.

1. POWER



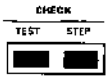
This mains switch operates with a push on - push off action and is clearly marked to indicate whether on or off. The display is always illuminated when the instrument is switched on, thus obviating the need for separate button illumination. The switch cannot be remotely controlled, however remote switch-off can be achieved by interrupting the power supply.

2. CONTROL



With the (optional) interface unit fitted, selection of LOCAL inhibits the effect of all remote command inputs except FRONT PANEL LOCKOUT (a command signal from the interface unit) and control is via the front panel push buttons. When REMOTE is selected all functions except SAMPLE are controlled by remote command inputs (see Section 5). the remaining three groups of push-buttons being disabled. With no interface unit fitted selecting REMOTE has no effect.

3. CHECK



When TEST is selected the Self Test programme is initiated, designed to check the overall function of the instrument. Progression from one test to the next is effected by pressing the STEP button. The 5 tests check the function of:-

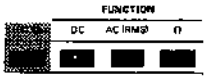
1. The DC Measurement system	Should display 7V DC ± 0.005V
2. The A - D converter internal zero	Should read zero ± 0.0002V
3. The AC converter	Should display 10V AC ± 0.01V
4. The Ohms converter	Should display 10kΩ ± 0.02kΩ
5. The Display	Should display a "full house" of eleven 8's.

4.a. RATIO



This push on - push off switch, when selected, replaces the internal reference with the user's choice of external reference applied to the terminals on the Rear Panel. A suitable reference voltage between 2 and 11 volts should be used. This function is not available with resistance measurement. N.B. It is important to disconnect any external reference supply when not making Ratio measurements.

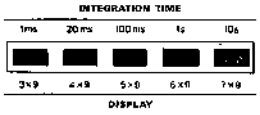
b. FUNCTION



These three push buttons are mechanically linked, mutually exclusive and left-justified electronically. The mechanical linkage ensures that, barring misuse, selection of one switch automatically disengages any other which had previously been selected. Should accident or misuse result in the forcing in of two of these buttons simultaneously, left-justification causes the left hand one of the pair to be the function selected electronically.

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5. INTEGRATION TIME

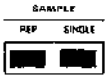


Each push button selects one of five available measurement times and, as can be seen from the legend below the switches, causes the display length to vary between 3 × 9's and 7 × 9's. The switches are of the mutually exclusive mechanically linked type with left justification as described above (4b).

The tables in Section 2 show the results of varying integration time. It should be particularly noted here, however, that when the longer integration times are used, there is a finite delay between successive updatings of the reading. This lengthening of the conversion time is true for both REP and SINGLE operation. During the delay any alteration the operator might make to the front panel controls will not be effective.

For more detailed information on the significance of integration time, the user is referred to Section 4 (Measurement Techniques).

6. SAMPLE



When REP is selected (i.e. normal operation) the instrument makes repeated readings at the rate determined by the selected Integration Time, each reading updating the display. When SINGLE is selected the display presents the next complete reading, and holds it. Updating of the displayed information is achieved by a further pressing of the SINGLE button, which initiates one further measurement. As a safety precaution the autorange circuits will still cause range-up while SINGLE is selected and overload protection remains operative. However care must still be exercised to ensure that the specified limits of input for the displayed mode of operation are never exceeded.

7. μV OFFSET

The instrument's internal zero is extremely stable and no operator adjustment is necessary. The μV OFFSET is provided to 'back-off' any small disturbances to the instrument zero which might be generated externally to the dvm. In those applications where, for example, thermal effects generated in the external circuit could be of significance and degrade the measured result, use of the μV offset will provide a correction of approximately ± 10μV.

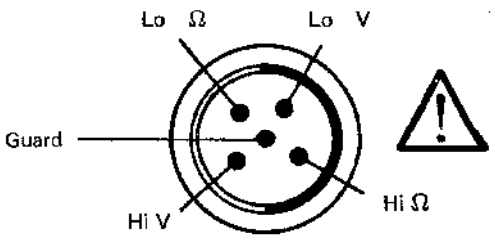
FRONT PANEL LOCKOUT

Not apparent from the front panel legends is a facility known as Front Panel Lockout. Under the control of an external electrical command applied via the optional interface unit the action of all front panel controls, except POWER, can be inhibited. This command signal even disables "LOCAL" and can be used to prevent unauthorised use of the dvm when it is committed within a system or, with suitable remote programming, enables a test sequence to include both automatic and manual control.

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INPUT CONNECTOR

The input connector simply pushes into the front panel socket with a 'snap-in' action. This cannot be released by pulling on the cable, but separation occurs when the skirt of the connector is pulled away from the panel.



Input connector socket, showing pin identification (front panel view).

The skirt of the connector acts as an isothermal chamber thus preventing errors which could otherwise result from temperature differentials across the input terminals.

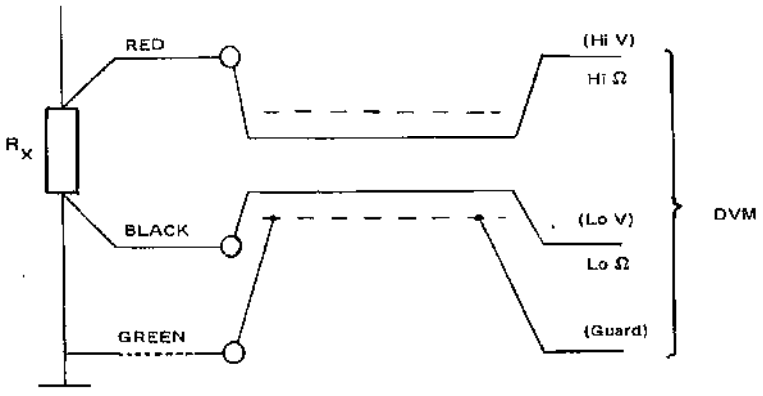
Three types of input lead are available as follows:-

(a) **2 Way Lead (supplied as standard).**

This input lead may be used for all standard measurements. The RED lead is connected to HiV and should be used as Hi, normally at the largest potential with respect to earth. The BLACK lead is connected to LoV and provides the return path. The 2 cores are enclosed in a braided screen which is connected to Guard. At the free-end of the cable, this screen is connected to the black lead thus effectively preserving the guard right up to the signal source. This prevents the measurement being affected in any way by common mode current flowing in the screen and via leakage to earth. The input may be floated above mains' earth by up to 500V, the use of higher common mode voltages is not recommended purely to ensure safety for equipment and the user. The guard is not made available as a separate termination.

(b) **3 Way Lead**

In some rare measurement situations, common mode voltages can have an affect on the readings. Most users will never encounter the problem, but those who do can still eliminate error by using this lead which has 2 cores and a screen which is available to the user. The RED should be used for Hi and the BLACK for Lo as above. The screen is available as Guard and colour-coded GREEN.



Note. In both (a) and (b) HiΩ and LoΩ are internally connected within the lead to HiV and LoV respectively. The same lead can thus be used for both voltage and resistance measurement.

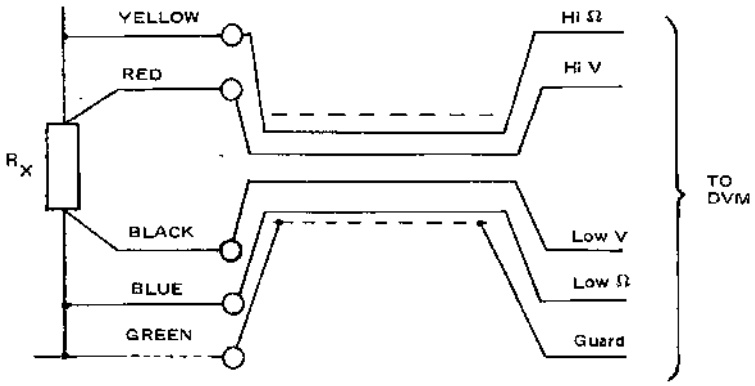
When the 3-way lead is not being used as illustrated the GREEN wire should be connected to Lo (BLACK).

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(c) **5 Way Lead**

This lead has 4 cores and a screen which is available to the user. The RED lead is connected to HiV, the BLACK lead to LoV, the YELLOW to HiΩ, the BLUE to LoΩ and the GREEN to GUARD.

When measuring low values of resistance, the voltage dropped along the leads can sometimes introduce errors. This effect may be eliminated by employing the 4 wire technique in which two wires supply the current to the resistor and two others sense the potential developed across it.



The example shows the correct method of using the lead, the order of connections is important, i.e. the RED and BLACK leads should be as close to the resistor as possible. The GREEN (guard) may be used as previously detailed to reduce common mode interference if this introduces errors.

These and other leads are available to order as Optional Accessories. (see full Accessories List Section 2).

To preserve the integrity of readings obtainable with this instrument it is recommended that only copper connecting clips, as supplied, are used with the input connector.

Rear Input

A rear input socket is fitted as standard, wired in parallel with the normal front input. This is provided as an alternative (e.g. in rack mounting use of the instrument) and connections should never be made to both front and rear input sockets.

N.B. The symbol which appears in places on the instrument of an exclamation mark enclosed within a triangle, ⚠, is an indication to the user that reference should now be made to relevant sections of this book.

A pull-out instruction card, repeating the basic operating parameters, is mounted below the front panel.

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DISPLAY

The display area is covered by a tinted screen laminated with a circularly polarised membrane to inhibit stray light or reflected light which might otherwise reduce the clarity of the reading. The front surface is lightly frosted to eliminate surface reflection from overhead lights or light coloured garments worn by the user. Very slight de-focussing results from this frosting.

The reading is updated at the selected integration rate or on pressing the SINGLE button as described earlier.

From left to right the displayed information is:-

(a) RATIO — Selection of RATIO operation illuminates this legend.

(b) ∿ — This sign is displayed when AC (RMS) is selected.

(c) **Numerical Indication.** Plasma discharge tubes are used to present the result of measurement. The numerals are grouped in threes, for ease of reading.

(d) **Decimal Point.** This is a fixed point, floating display instrument, leading zeroes being suppressed.

(e) **Units.** V and kΩ annunciators are illuminated as a result of selecting the required mode of measurement with the FUNCTION buttons.

(f) REMOTE — An indication that the instrument is under REMOTE control - only applicable when the (optional) interface unit is fitted.

BUSY — Should this legend be illuminated it advises the operator that the reading currently being displayed should be regarded as invalid. The legend is extinguished when the new result is displayed. The BUSY signal has the additional function of inhibiting the front panel push buttons. Thus once a command has initiated a measurement, the instrument will not abort that reading.

INVALID READINGS

In addition to 'BUSY' described above, an indication that a reading is invalid is that of a flashing display. Normally this occurs as a result of an overload on the range in use. Notwithstanding this automatic warning, the user is reminded that **the limits of input specified should never be exceeded.**

The limits are:-

DC **1100V DC**

AC **750V RMS (1100V Peak)**
above 20kHz limit is 200V RMS
400V dc when on AC

N.B. These limits only apply to LOCAL operation - for details of limits applicable when instrument is under REMOTE control see Technical Specification and Section 5.

RACK MOUNTING

The overall dimensions conform to international standards for rack mounting. The instrument can if desired be rack mounted within its case, no additional protection being necessary. Users who so wish can remove the covers which are simply secured by four screws. For rack mounting either the handle-less rack mounting fittings, or the combination handle/ears should be substituted for the normal handles. Rack mounting fixtures of both types are included in the accessory pack supplied with the voltmeter, (See Accessories list in Section 2).

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SECTION 2 Specifications and General Information

This section contains a copy of the technical specification applicable to the voltmeter.

The 7075 has been designed and manufactured to the highest specification possible for an instrument of its type. Where typical figures are quoted, they are realistic estimates of obtainable performance based on known component tolerances and stability. Guaranteed performance, on the other hand, is specified from the results of exhaustive tests, stringently controlled, applied to every instrument produced. "Worst-case" figures are quoted in many instances, hence your 7075 may be found to exhibit a performance better in some particulars than the tables suggest. However no additional claims are made for the instrument above that published in the current data sheet.

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SPECIFICATIONS

Manufacturers calibration temperature 20°C.

Table 1 GUARANTEED PERFORMANCE 1s Integration

Nominal Range	Input Sensitivity	Displayed Full Scale	Limits of Error 24 hrs ± 1°C ±[% rdg. + % f.s.]		6 mnth ± 5°C ±[% rdg. + % f.s.]		1 yr ± 5°C ±[% rdg. + % f.s.]		Input Resistance
10mV	1μV	0.013 999V		0.007		0.007		0.007	> 10GΩ
100mV	1μV	0.139 999V	0.0014	0.0014	0.002	0.0014	0.003	0.0014	> 10GΩ
1V	1μV	1.399 999V	0.0006	0.0004	0.002	0.0008	0.003	0.001	> 10GΩ
10V	10μV	13.999 99 V	0.0003	0.0002	0.0015	0.0005	0.002	0.0008	> 10GΩ
100V	100μV	139.999 9 V	0.0007	0.0005	0.003	0.0008	0.004	0.001	10MΩ
1000V	1mV	1 000.000 V	0.0007	0.0007	0.003	0.0008	0.004	0.001	10MΩ

Table 2 TYPICAL PERFORMANCE 10s Integration

Nominal Range	Input Sensitivity	Displayed Full Scale	Limits of Error 24 hrs ± 1°C ±[% rdg. + % f.s.]		6 mnth ± 5°C ±[% rdg. + % f.s.]		1 yr ± 5°C ±[% rdg. + % f.s.]		Input Resistance
10mV	1μV	0.013 999V		0.007		0.007		0.007	15GΩ
100mV	1μV	0.139 999V		0.0007	0.001	0.0007	0.0015	0.0007	20GΩ
1V	1μV	1.399 999V	0.0004	0.00015	0.001	0.0003	0.0015	0.0005	200GΩ
10V	1μV	13.999 999V	0.00015	0.0001	0.0005	0.00025	0.001	0.0004	1000GΩ
100V	10μV	139.999 99 V	0.0005	0.0002	0.0015	0.0005	0.002	0.0007	10MΩ
1000V	100μV	1 000.000 0 V	0.0005	0.0003	0.0015	0.0005	0.002	0.0008	10MΩ

Reduced scale lengths

Scale Length	Integration Time	Input Sensitivity	Limits of Error [1 year ± 5°C]
5 x 9	100ms	1μV	± 0.004% rdg. ± 1 digit ± 1μV
4 x 9	20ms	1μV	± 1 digit ± 1μV
3 x 9	1ms	10μV	± 1 digit ± 10μV

Temp. coeff.

Range	<± [% rdg. + % f.s.] per °C	
10mV	0.0004	0.0015
100mV	0.0004	0.0002
1V	0.0004	0.0001
10V	0.0002	0.00007
100V	0.0005	0.0001
1000V	0.0005	0.0001

Zero offset <± 0.2μV per °C

Input Current
Typically < 20pA at 20°C

Overload protection:
Autorange: 1.1kV
Commanded ranges:
up to 10V: 350V
100V & 1000V: 1.1kV

Linearity:
error due to non-linearity is less than 1ppm and is included in the above specification.

Temperature corrections:
need be applied only when operating beyond the temperature limits quoted under Limits of Error.

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Manufacturers calibration temperature 20°C.

Performance guaranteed above 10% of f.s. (i.e. Range-change point)

Table 3 24 hrs at 20°C ± 1°C 1s integration

Nominal Range	Input Sensitivity	Displayed Full Scale	Limits of Error 10Hz to 40Hz	40Hz to 10kHz	10kHz to 100kHz
100mV	1µV	0.139 999V			
1V	10µV	1.399 99 V	± 0.3% rdg.	± 0.05% rdg.	± 0.5% rdg.
10V	100µV	13.999 9 V	± 0.05% f.s.	± 0.05% f.s.	± 0.2% f.s.
100V	1mV	139.999 V			
1000V	10mV	750.00§ V	± 0.3% rdg. ± 0.1% f.s.	± 0.05% rdg. ± 0.1% f.s.	± 0.5% rdg. ± 0.4% f.s.

§Above 20kHz: 200V rms max.

Table 4 6 months at 20°C ± 5°C 1s integration

Nominal Range	Limits of Error 10Hz to 40Hz	40Hz to 10kHz	10kHz to 100kHz
100mV	± 0.4% rdg. ± 0.08% f.s.	± 0.1% rdg. ± 0.06% f.s.	± 0.5% rdg. ± 0.2% f.s.
1V			
10V	± 0.4% rdg. ± 0.08% f.s.	± 0.1% rdg. ± 0.06% f.s.	± 0.7% rdg. ± 0.2% f.s.
100V			
1000V	± 0.4% rdg. ± 0.08% f.s.	± 0.1% rdg. ± 0.1% f.s.	± 0.7% rdg. ± 0.4% f.s.

Table 5 1 year at 20°C ± 5°C 1s integration

Nominal Range	Limits of Error 10Hz to 40Hz	40Hz to 10kHz	10kHz to 100kHz
100mV	± 0.5% rdg. ± 0.1 f.s.	± 0.15% rdg. ± 0.1% f.s.	± 0.6% rdg. ± 0.2% f.s.
1V			
10V	± 0.5% rdg. ± 0.1% f.s.	± 0.15% rdg. ± 0.1% f.s.	± 1.0% rdg. ± 0.2% f.s.
100V			
1000V	± 0.5% rdg. ± 0.2% f.s.	± 0.15% rdg. ± 0.2% f.s.	± 1.0% rdg. ± 0.4% f.s.

Other integration times

Time	Sensitivity	Scale Length	Min. Frequency*	Specification
10s	1µV	139 999	as Tables 3 to 5	as Tables 3 to 5
100ms	1µV	139 999	40Hz	as Tables 3 to 5
20ms	10µV	13 999	100Hz	add ± 0.01% f.s.
1ms	100µV	1 399	400Hz	add ± 0.1% f.s.

*< 40Hz best performance is given by 1s or 10s integration.

Temp. coeff.

Range	<± [% rdg. + % f.s.] per °C	
100mV	0.015	0.004
1V	0.015	0.004
10V	0.015	0.004
100V	0.015	0.004
1000V	0.015	0.004

Overload protection:
100mV & 1V ranges: 350V peak
10V, 100V, 1000V ranges: 1.1kV peak
All ranges, above 20kHz: 200V rms

Crest factor: 5 : 1 at f.s.

Input impedance:
at input socket: 1MΩ//< 150pF
of standard input cable: < 300pF

Very low frequency measurement:
Useful readings can be made down to 1Hz with <1dB error by employing the 10s integration time.

Temperature corrections:
need be applied only when operating beyond the temperature limits quoted under Limits of Error.

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Manufacturers calibration temperature 20°C.

Table 6 GUARANTEED PERFORMANCE 1s integration

Nominal Range	Input Sensitivity	Displayed Full Scale	Limits of Error 24 hrs ± 1°C ±[% rdg. + % f.s.]		6 mnth ± 5°C ±[% rdg. + % f.s.]		1 yr ± 5°C ±[% rdg. + % f.s.]		Measuring Current
10Ω	1mΩ	0.013 999kΩ		0.014		0.014	0.01	0.014	1mA
100Ω	1mΩ	0.139 999kΩ	0.001	0.002	0.003	0.002	0.005	0.002	1mA
1kΩ	1mΩ	1.399 999kΩ	0.002	0.0005	0.003	0.001	0.005	0.0015	1mA
10kΩ	10mΩ	13.999 99 kΩ	0.002	0.0003	0.0025	0.0008	0.004	0.001	1mA
100kΩ	100mΩ	139.999 9 kΩ	0.001	0.0005	0.003	0.001	0.006	0.0015	10μA
1MΩ	1Ω	1 399.999 kΩ	0.001	0.0003	0.003	0.001	0.006	0.0015	10μA
10MΩ	10Ω	13 999.99 kΩ	0.002	0.001	0.006	0.0015	0.008	0.0015	1μA

Maximum dissipation in unknown: 14mW Maximum overload: 250V rms Maximum Voltage, Lo current/Lo sense: 10V peak.

10s integration time: specification as above, but having one additional decade displayed on ranges 10kΩ and above.

Reduced scale lengths

Scale Length	Integration Time	Input Sensitivity	Limits of Error 1 year ± 5°C
5 x 9	100ms	1mΩ	± 0.008% rdg. ± 1 digit ± 1mΩ
4 x 9	20ms	1mΩ	± 1 digit ± 2mΩ
3 x 9	1ms	10mΩ	± 1 digit ± 10mΩ

Open circuit condition:
A source resistance of 1000GΩ ensures full protection to external circuits.

Temp. coeff.

Range	<± [% rdg. + % f.s.] per °C	
10Ω	0.0007	0.0015
100Ω	0.0007	0.0002
1kΩ	0.0007	0.0001
10kΩ	0.0005	0.00007
100kΩ	0.0007	0.0001
1MΩ	0.0007	0.0001
10MΩ	0.0012	0.0001

Zero offset <± 0.2mΩ per °C

Temperature corrections:
need be applied only when operating beyond the temperature limits quoted under Limits of Error.

RATIO FACILITY

Reference Voltage:	2 to 11V
Input Resistance:	Ref Hi to Ref Lo: 2 MΩ Ref Hi to Sig Lo: 1.7MΩ Ref Lo to Sig Lo: 1.7MΩ
Reference Overload:	100V peak differential 100V peak either terminal to Sig Lo.
Limits of Error 1 yr at 20°C ± 5°C:	$\pm$ [Normal % rdg. + 0.005% rdg. + (Normal % f.s. + 0.005% rdg.) $\frac{10}{V_{Ref}}$]
Temperature Coefficient:	$\pm$ [Normal % rdg. T.C. + 0.001% rdg. + (Normal % f.s. T.C. + 0.001% rdg.) $\frac{10}{V_{Ref}}$]

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Ratio of peak interference to 1 digit reading error.

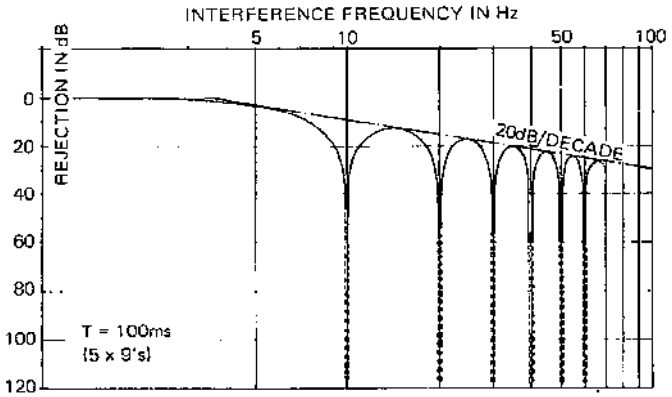
Series mode

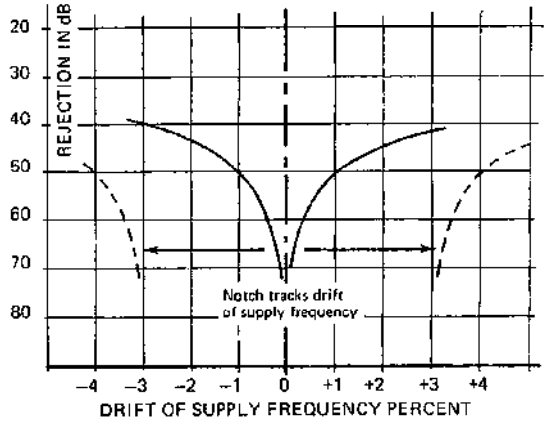
Maximum Series Mode:	Autorange:	1.1kV pk	
	Command Range:	1.5 x V_{Range}	
DC Measurement:	Rejection of 50 (60) Hz ± 3%	>	70dB
Ratio Measurement:	Rejection of 50 (60) Hz ± 3% at Ref.	>	40dB

Effective common mode

Measured with 1kΩ imbalance in Lo lead.

Maximum Common Mode:		500V dc or peak ac.
DC Measurement:	Rejection of dc:	> 150dB
	Rejection of 50 (60) Hz ± 3%:	> 144dB
AC Measurement:	Rejection of dc:	> 150dB
	Rejection of 50 (60) Hz ± 3%:	> 74dB
Ratio Measurement:	Max. Common Mode Ref. Hi or Lo to Sig Lo:	30V
	Rejection of Common Mode Ref Lo to Sig Lo with up to 80Ω lead imbalance:	> 80dB





In the measurement of dc voltage 7075 gives the mean (average) value of the input during the chosen integration time. Except for 1ms, the times are multiples of the period of the mains supply. Hence the curves for interference rejection exhibit deep notches at discrete frequencies, those for 100ms shown above having a notch every 10Hz. By using the 10s integration the notches become spaced at only 0.1Hz intervals. Furthermore the tangent to the peaks, while retaining the slope of 20dB/decade, is spaced 20dB lower on 1s integration and 40dB lower on 10s integration.

The precise integration time is locked to the period of the mains supply by a digital servo. The notches move to right or left as supply frequency changes thus preserving maximum rejection up to a shift of ± 3%. This is beyond the limit of frequency deviation specified for the national grid.

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Environment

Working Temperature Range:	0 to + 50°C.
Storage Temperature Range:	–30 to + 70°C.
Maximum Relative Humidity:	70% at + 40°C.

Other specifications to Solartron spec. 50/01/102.

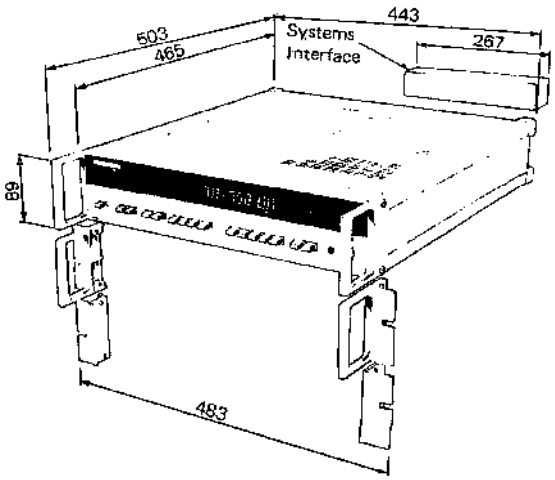
Power supply

Voltage:	100 to 264V (no mains tap).
Frequency:	50(60)Hz ± 3%. Internal switch provides optional 400Hz operation. The instrument is capable of operating up to 2400Hz supply frequency.
Consumption:	Approx. 65VA (35W)
Fuse	800mA Slo Blo

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Dimensions

Width:	443mm	(17.4ins)	Rack mounting depth,
Height:	89mm	(3.5ins)	over interface + cable:
Depth:	465mm	(18.3ins)	533mm (21ins).
Weight:	9.1kg	(20lbs)	



Safety

This instrument conforms to IEC 348 recommendations.

Accessories

Included Accessories		Part No.
Input Cable		A2000168
Crocodile Clip (copper)		355901030
Test Probe	Red	351901020
Test Probe	Black	351901010
Spare fuse	800mA	360106310
Mains cable		480140220
Rack mounting handles	(2 off)	429700101
Rack mounting ears	(2 off)	469601201
Operating Manual		70750010
Technical Manual		70750011

Optional Accessories	Part No.
Systems Interface (Parallel BCD)	70754A
Systems Interface (IEC TC66/IEEE 488)	70755A
High Voltage Probe	70757A
3-Terminal input lead	3193
5-Terminal input lead	3183
Telescopic Rack Slides (pair)	70759A
ESI Kelvin clip leads (pair)	70758E
Low thermal lead kit	70758D
Master Series adaptor lead	70758G
Service kit	70759C
Calibration cover	70759D

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SECTION 3 Operating Instructions

PRELIMINARIES

Check that the correct fuse is fitted, 800mA SLO-BLO

Connect a suitable plug to the mains lead:-

BROWN	LINE
BLUE	NEUTRAL
GREEN/YELLOW	EARTH

N.B. It is important that this Earth connection is made.

Operation at other than 50Hz supply frequency

The link for 60Hz operation and the switch for 400Hz operation are positioned on board 2, on the right hand side of the instrument. Access to these necessitates partial removal of the cover.

The instrument should be disconnected from the mains supply before any attempt is made to remove the cover.

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DC VOLTAGE MEASUREMENT

1. Switch POWER on.
2. Select LOCAL, unless Remote operation with optional interface unit is required. (In that instance refer to Section 5).
3. Ensure TEST and RATIO push buttons are released.
4. Select DC.
5. Select INTEGRATION TIME for the resolution, noise rejection and reading rate that are required.
6. Connect input lead to the unknown voltage source - BLACK lead to signal Low, RED to signal High (in that order).
7. Select REP for repetitive display of measurement or press SINGLE for each single reading required. 'V' will now be illuminated.
8. Read the displayed value. The indicated polarity is that of the red lead with respect to the black. (Polarity is positive unless the minus sign is illuminated).

   The user is referred to Section 4 for further information on measurement technique, and the significance of varying Integration Time.

AC VOLTAGE MEASUREMENT (True RMS)

1. Switch POWER on.
2. Select LOCAL, unless Remote operation with interface unit is required. (In that instance refer to Section 5).
3. Ensure TEST and RATIO push buttons are released.
4. Select AC (RMS).
5. Select INTEGRATION TIME for the resolution, noise rejection and reading rate that are required.

Note. A maximum of 5 × 9's reading can be obtained, selection of 1s or 10s resulting in a quieter display at low frequencies, by a process of Digital Filtering (the user is referred to Section 4 for more detailed information on the significance of Integration Time when measuring AC).

6. Connect input lead to the unknown Voltage source.
7. Select REP for repetitive display of measurement or press SINGLE for each single reading required. The ∿ sign will be illuminated.
8. Read the displayed value.

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CURRENT MEASUREMENT

Although not a facility directly provided by this instrument, current measurement can be easily effected by measuring the potential difference developed across a known precision resistor, either a resistance Standard or a precision wire wound component. For ac measurement a metal film precision resistor is recommended. Alternatively the Solartron Current Adaptor may be used to convert your voltmeter into an ac/dc digital ammeter capable of measuring currents in the range 100pA to 1.2A. Full details and operating instructions are contained in the Adaptor handbook.

RATIO MEASUREMENT DC/DC and AC/DC (True RMS)

Without RATIO selected, all instrument measurements are made with reference to an internal reference supply.

With RATIO selected an external reference supply (between 2V and 11V dc) must be connected to the rear terminals and all instrument measurements are then referenced to this supply. The relationship between input and the display becomes:-

$$V_{out} = \frac{10V_{in}}{2 < V_{ref} < 11}$$

where V_{out} is the displayed reading, V_{in} is the applied voltage and V_{ref} is the chosen value of external reference.

After the external reference supply is connected, RATIO measurement operation is as for normal operation. The ratio is,

$$\frac{\text{displayed reading}}{10}$$

RESISTANCE MEASUREMENT

1. Switch POWER on.
2. Select LOCAL, unless remote operation with interface unit is required. (In that instance refer to Section 5).
3. Ensure TEST and RATIO push buttons are released.
4. Select Ω.
5. Select INTEGRATION TIME for the resolution, noise rejection and reading rate that are required.
6. Connect input lead to the unknown resistance.
7. Select REP for repetitive display of measurement or press SINGLE for each single reading required. The kΩ annunciator will be illuminated.
8. Read the displayed value.

   For details of 4 terminal measurement and other refinements of technique the user is referred to Section 4 of this manual.

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SECTION 4 Measurement Techniques

The following notes are written for those users who wish to know more about the techniques of precision measurement. They also provide the user with a guide as to how he can obtain the optimum performance from the dvm in more unusual applications and avoid some of the pitfalls.

INPUT RESISTANCE

In making a measurement of voltage virtually all instruments take a current from the voltage source. The one exception is the true potentiometer in which, at balance, the current drawn falls to zero. The current drawn by the measuring device causes a voltage drop across the internal resistance of the source such that the voltage measured is less than the true emf of the source. (Fig. 4.1).

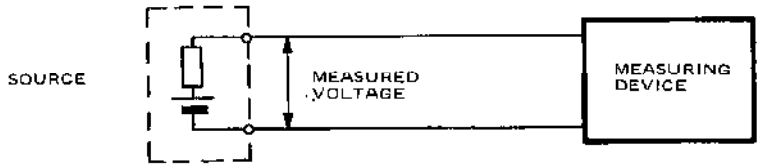


Fig. 4.1 *Current taken by a measuring instrument can cause a voltage drop across source resistance.*

A good moving coil meter will take a current of typically 10μA (100kΩ/V) so that with a source resistance of 1kΩ the voltage drop would be 10mV. This is obviously unacceptable for precision work since an instrument with such a low input resistance would read 1.49V instead of 1.50V.

Fortunately, electronic feedback techniques can give a digital voltmeter such a high input resistance that, for most practical purposes, the effect can be ignored. Thus the 7075 when measuring dc voltages less than 14V, has an input resistance in excess of 10GΩ. This means that the source resistance has to exceed 10kΩ before an error of 1 part per million is produced. If this sounds somewhat vague, it should be understood that defining the input resistance more closely is impossible since a group of voltmeters will have differing gains in their input amplifier. This will of course have no effect on their accuracy, but will make the input resistance different - possibly 20GΩ to 50GΩ, but never as low as 10GΩ.

When measuring voltages greater than 14V it is not possible to apply the unknown input directly to the input amplifier: first it must be attenuated. The attenuator must be very accurate and stable, capable of withstanding high input voltages, hence precision wire wound resistors are used. Since the use of high value resistors would make the attenuator more difficult and expensive to produce, a 10MΩ network is used. Hence, for voltages greater than 14V the input resistance is 10MΩ ± 0.25%, errors arising from source resistance being calculable with reasonable accuracy. For example, a source resistance of 1kΩ will degrade the reading by 0.01%, which is expressed as 1 digit in 10 000.

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INPUT CURRENT

All solid state devices have finite input currents and/or leakage currents. A voltmeter will therefore have a current flowing at the input terminals even with zero input signal. The effects of this current are additional to those of input resistance. (Fig. 4.2).

By careful design this current can be reduced such that its effects are almost negligible and in the 7075 it is less than 20pA at room temperature. The input current will flow into or out of the Hi terminal and must therefore, be regarded as lying between + 20pA and − 20pA.

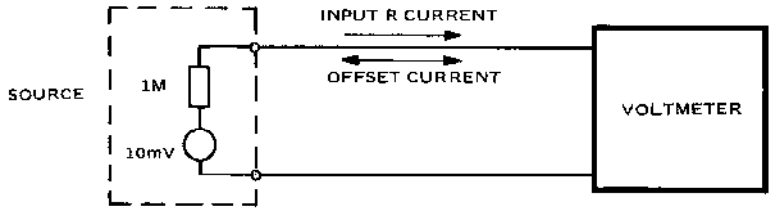


Fig. 4.2 *Current taken by input resistance flows into the voltmeter; offset current may flow either way. Both effects are present together.*

If we take an extreme example of a 10mV source having a resistance of 1MΩ, the input resistance (> 10GΩ) would give a reading that is up to 1μV in error. In addition an input current of 20pA will introduce an error of ± 20μV which will add to or subtract from the input resistance error. The total uncertainty then will be in the range + 19μV to − 21μV.

The condition given in the above example is unlikely to be encountered by the average user because low level signals nearly always have a relatively low source resistance, less than 10kΩ, the effects of which are insignificant.

ASSESSING INPUT RESISTANCE AND CURRENT

1. **Input Current:-**

Connect a 10MΩ resistor across the input terminals. Select 1s or 10s integration time and DC. (In a "noisy" environment it may be necessary to enclose the resistor in a screening box connected to the Lo terminal). The input current in pA is obtained by dividing the reading in μV by 10.

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2. **Input Resistance:-**

Connect the voltmeter to a source of approximately 10V dc. via a 10MΩ resistor and a switch, mounted in a screening box as illustrated in Fig. 4.3.

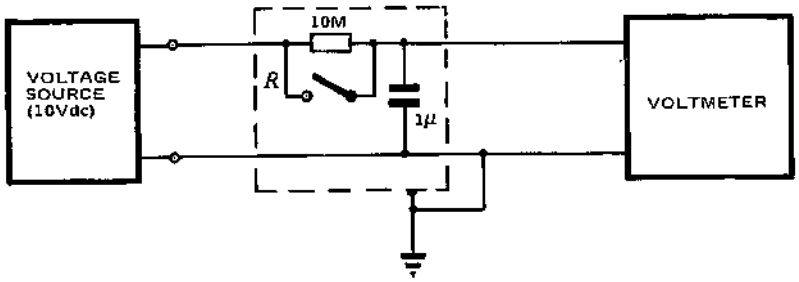


Fig. 4.3 *An assessment of input resistance will include an effect due to offset current.*

Select 1s or 10s integration time and DC.
With switch closed note the reading.
Open the switch and note the fall in reading (ΔV)

The fall is the algebraic sum of the voltage drop across R as a result of the source current and the instrument's input current, I_{in}. Thus:

$$\Delta V = \frac{R}{R_{in}} V_{in} + RI_{in} \qquad \text{(assuming } R_{in} \gg R\text{)}$$

then:
$$\Delta V - RI_{in} = \frac{R}{R_{in}} V_{in}$$

$$R_{in} = \frac{R V_{in}}{\Delta V - RI_{in}}$$

Substituting the experimental known values:

$$R_{in} = \frac{(10 \times 10^6) \times 10}{\Delta V - (10 \times 10^6) I_{in}} \quad \Omega$$

For convenience this can be simplified and R_{in} expressed in GΩ (1GΩ = 10^9Ω), taking ΔV in μV and I_{in} in pA, thus:

$$R_{in} = \frac{10^5}{\Delta V - 10 I_{in}} \quad G\Omega$$

It was previously noted that I_{in} may flow into or out of the dvm Hi terminal, assisting or opposing the source current. The magnitude of I_{in} is evaluated as in 1. above (Fig. 4.2); its direction and hence its effect on R_{in} can be readily established by reversing the source terminals in the circuit of Fig. 4.3 and again noting the reading with the switch open. A higher reading is obtained when I_{in} opposes the source current, in which case ΔV will be smaller and I_{in} in the final expression will have a negative value.

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SPURIOUS VOLTAGES

Although small emf's occur in the voltmeter input circuit, they are compensated for by careful design. Thereafter, when the instrument has warmed-up for about 30 minutes, they are so stable as to be quite insignificant to the user.

The voltmeter will faithfully measure any input that is applied to its terminals; it is the responsibility of the user to ensure that the input contains only the voltage that he wishes to measure. In low level work - with perhaps a few tens of microvolts - this may require some care and thought in the arrangement of the circuit.

As an example, consider measuring the voltage produced by passing a very small current through a wirewound resistor. On the 100mV range the reading is recorded as 126μV. But the resistor is placed - in the sun or near a power transistor - so that one end is a little warmer than the other. Because of the dissimilar materials used in the wire of the resistor and the copper connections, a net thermal emf of possibly 40μV/^{o}C will exist. Thus a differential of 0.5^{o}C across the resistor could mean that the true result should be either 106μV or 146μV. The voltmeter cannot possibly distinguish between the wanted and unwanted parts of the signal that is applied to it. In this example, without altering the conditions of the resistor in any way, a measurement should be made with the small current flowing first in one direction and then in the other. In one case the thermal emf will add and in the other it will subtract. So the mean of the two results will eliminate the error

Metal oxide resistors and reed relays are two other examples in which thermal emf's bring about similar errors, in the reed relay the heat produced by the operating coil being the contributing factor.

When the unwanted emf can be determined and is steady, it can be 'backed-off' by using the μV OFFSET control. This has a range of $\pm$ 10μV. (typically)

In attempting precision measurement of low level signals, effects other than thermal emf's can cause problems. Leakage across an insulator which is degraded by humidity or an industrial atmosphere may produce an unsuspected voltage across a source resistance. Coaxial cables, when flexing under vibration, can generate quite high transient voltages due to the screen scrubbing the pvc insulant; the use of low noise cables will prevent this effect.

SERIES MODE INTERFERENCE

The examples of thermal and other, spurious emf's given above can be regarded as forms of interference because they interfere with the accurate assessment of the unknown signal. They are in series with the signal and voltmeter input and represent a special case of series mode interference because there is nothing that the voltmeter can do about rejecting dc interference while measuring a dc signal.

Series mode ac interference is a different matter. Because of the basic design principle, this voltmeter will ignore all the usual forms of ac and noise that may be intermingled with the dc signal. Hence in all normal measurement work the user will be unaware of ac interference and it will not cause errors.

Nevertheless, it would be possible to introduce such a degree of interference that the voltmeter would be unable to cope, so the keen user may be interested in the mechanism that brings about rejection.

The most common form of ac interference is simple hum - i.e. 50Hz superimposed on the dc signal. This can be visualised either as pick-up on the connecting leads, as shown in Fig. 4.4(a), or as a generator that is a part of the source, as in Fig. 4.4(b). In both the result is the same and is shown graphically in Fig. 4.5.

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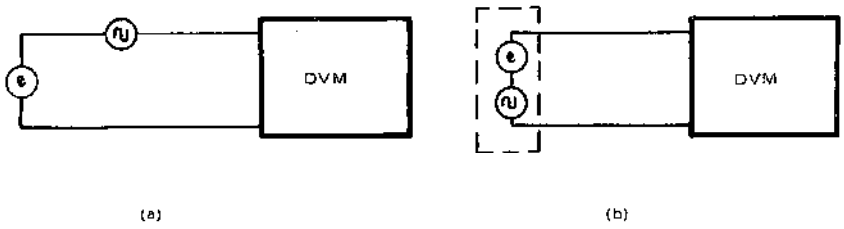


Fig. 4.4 *Interference at 50Hz can arise from pick-up on the leads (a), or may be inherent in the source (b).*

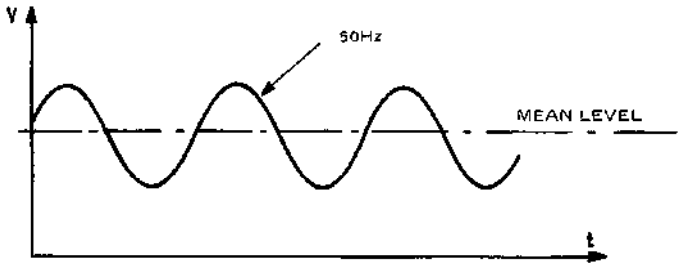


Fig. 4.5 *50Hz superimposed on the dc level that the voltmeter is trying to measure.*

Users of oscilloscopes will be familiar with this sort of picture and will know that the ac component is typically a few milli-volts peak-to-peak. This may be superimposed on a wanted dc signal of a mere 10μV.

The 7075 rejects ac signals by averaging the input voltage over the period of time selected, i.e. the integration time. Since the most common form of interference is attributable to the 50Hz (60Hz) mains, the integration times are chosen to be exact multiples of the mains period (20ms at 50Hz). This is achieved by timing the integration periods using a clock synchronised to the mains supply. Thus over the integration period the average 50Hz (60Hz) interference will be zero, the reading being unaffected.

This total rejection occurs at any frequency with a period equal to an exact fraction of the integration time. Harmonics of the mains frequency will also be totally rejected, while at other frequencies the rejection will be less.

Considering, as an example, the 1s integration time:-

1Hz, 2Hz, 3Hz, 4Hz, 5Hz. . . . . 57Hz, 58Hz. . . . . 83Hz, 84Hz. . . . . 126Hz etc., being whole numbers of Hz their periods are exact fractions of 1s and hence total rejection will occur.

For the 10s integration time there will be 10 times as many totally rejected frequencies, starting at 0.1Hz and spaced 0.1Hz apart. The only practical limitation of frequency rejection is that imposed by clock accuracy and in the 7075 rejection of 50Hz (60Hz) is better than 70dB.

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Series mode rejection is defined as:-

$$SMR = 20 \log_{10} \frac{\text{Peak reading error}}{\text{Peak of interference}} \quad dB.$$

N.B. The 1ms integration time has of course no rejection at 50Hz.

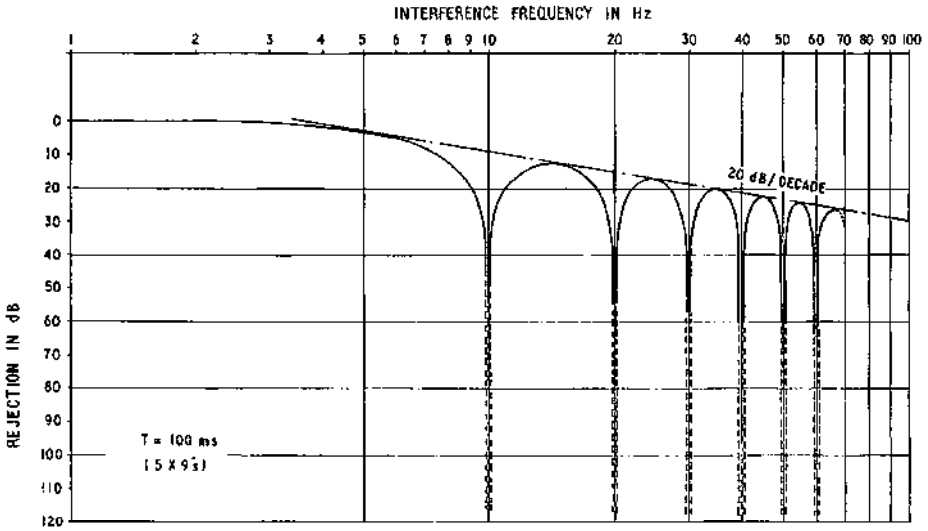


Fig. 4.6 *SERIES MODE REJECTION: These curves show the rejection at the frequencies given whilst measuring dc. The integration time is locked to the mains period so the curves will shift along the frequency axis as the mains supply frequency alters.*

COMMON MODE INTERFERENCE

Interference can also arise from unwanted voltages which are common to both input leads. This is illustrated in Fig. 4.7, where the signal source is earthed locally and the voltmeter input has also been earthed.

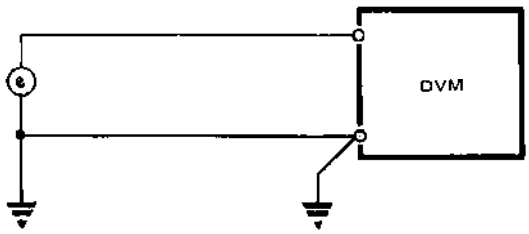


Fig. 4.7 *An 'earth' at both source and voltmeter input may introduce common mode interference. For this reason the voltmeter input is fully isolated.*

There is a distinct possibility that the two 'earths' are not at a common zero potential; in large industrial plants and in some multi-terminal system applications, widely separated earths can have potential differences between them in excess of 10V.

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This situation can be represented as in Fig. 4.8, where the source is shown to be at a finite potential with respect to earth.

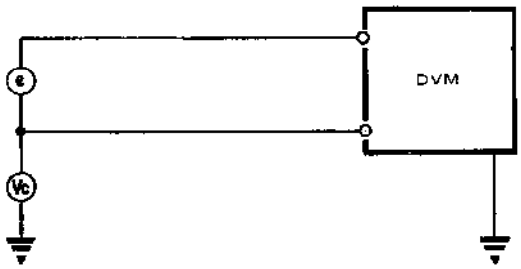


Fig. 4.8 *The source can be at a high potential above earth without causing errors.*

This would happen in practice, for example, where a thermocouple is used to measure the temperature of a furnace element. The signal emf might be millivolts of dc while the element itself is at 240V ac with respect to earth. Obviously earthing the voltmeter input would not be possible, although the case and many of the instrument's circuits are earthed via the mains lead.

The 7075 has been engineered so that the input circuits are extremely well isolated from the case, which itself is connected to mains earth. In all normal measurement the small current which does flow as a result of a large common mode voltage, will not cause any error. However, purely for the safety of equipment and operator, this voltage should not exceed 500V.

The lead supplied with the dvm is shown in Fig. 4.9. Within the instrument the cable screen is connected to the guard "box" (a screening compartment which encloses the input circuits) and at the free end the screen is strapped to signal Lo (Black). Hence the guard is preserved right up to the signal source and measurements cannot be affected by common mode current flowing in the screen and via leakage to earth.

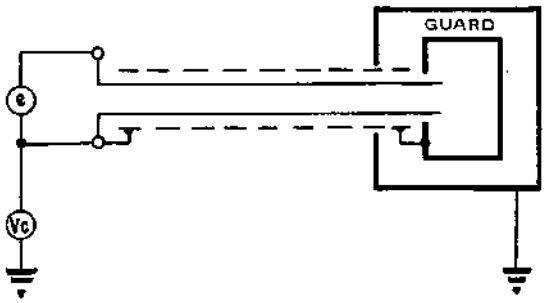


Fig. 4.9 *In the lead provided with the voltmeter Guard is strapped to Lo (BLACK) within the free end of the cable.*

In some measurement situations common mode voltage can have an affect on the reading. Most users will never meet the problem, but those who do can still eliminate errors by using the voltmeter correctly. When there is resistance associated with the source - perhaps inherent in the source, or in the connecting leads - common mode current can flow through this resistance. Examples are: the resistance of strain gauges, long compensating leads from a thermocouple. This is illustrated by Fig. 4.10 where it will be seen that current flowing from V_c to earth through the screen will pass through the resistance. If the guard-earth leakage is assumed to be the specified minimum of $10^{10}\Omega$ and V_c = 100V dc the common mode current will be 10^{-8}A. Taking a lead resistance of 1kΩ, 10^{-8}A will develop a voltage drop of 10μV. Since the voltmeter cannot reject dc interference the worst error will be 10μV.

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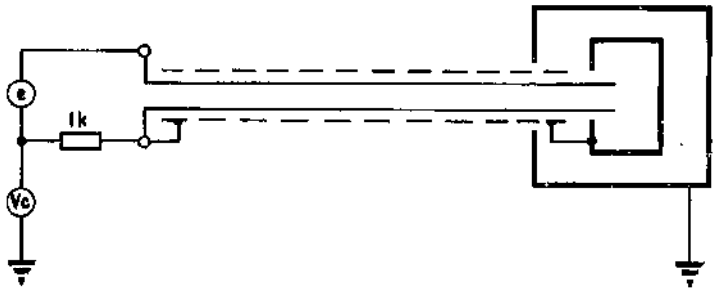


Fig. 4.10 *A rare, but more difficult, situation is where common mode current flows through lead resistance. This is entirely overcome by the arrangement of Fig. 4.11.*

If the source of common mode is ac, the stray capacitance from guard to earth is more important. The figure specified is 500pF which exhibits a reactance of about 6MΩ at 50Hz. With V_c now 100V rms the drop across 1kΩ is approximately 17mV rms or 24mV peak. This appears at the input terminals and the inherent rejection of series mode will be effective in reducing reading error to much less than 24mV. At worst the final reading error will not exceed 1μV.

In these examples a 1kΩ resistance has been assumed in one lead. Obviously the magnitude of the errors is proportional to this resistance and it is accepted practice to specify common mode rejection with 1kΩ unbalance in the leads using the configuration of Fig. 4.10. Even in these exceptionally adverse circumstances the error can be overcome by using a different input arrangement as in Fig. 4.11.

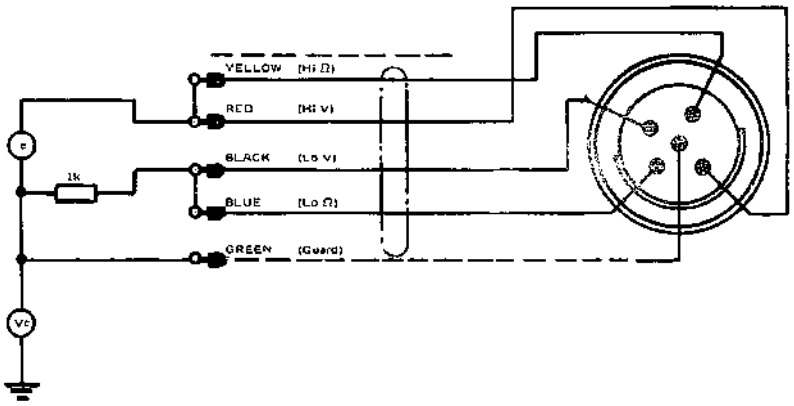


Fig. 4.11 *A special lead (EX 3183) is obtainable from Solartron which enables the Guard to be driven directly by the common mode voltage.*

Here use has been made of a special 5 way lead from which 4 cores and the screen are brought out at separate terminations.

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The four cores are required for 4-terminal resistance measurement as described later. For voltage measurement with guard, however, only 3-terminals are required - signal Hi, signal Lo and screen (guard). When measuring voltage the YELLOW and BLUE cores are internally linked to RED and BLACK by the selection circuits. To prevent inadvertent contact of these plugs with earth, other terminals or each other. the user should plug YELLOW into RED and BLUE into BLACK. GREEN is connected directly to the source of interference thus isolating common mode current from the input leads.

Using this arrangement, even though the interference were the permitted maximum (500V dc or peak ac), it is most unlikely that there would be any discernable error - even on the most sensitive range.

For a more complete treatment of interference in digital voltmeter measurement the reader is referred to the following monographs:-

(1) Digital Voltmeters and Interference.

(2) Principles of Interference Rejection.

both of which are available free on request to Solartron.

NOISE

The foregoing explanation of interference dealt specifically with 50Hz because by far the most common source of interference is the mains supply or fields radiating from mains wiring and mains energised equipment. It has been shown in earlier pages of this Section that, at harmonics of 50Hz, rejection is improved so that 100Hz ripple from power supplies or 400Hz/1600Hz aircraft and ship supplies are unlikely to cause difficulty. When considering noise of no specific frequency (e.g. white noise) the integration process still applies and the resultant noise component over the integration period will tend to zero.

INTEGRATION TIME

When considering immunity to series mode interference, reference was made to the integration time. This time, which is capable of selection by the user, is the period over which the instrument takes an *average* measurement of the input level. The conversion technique continuously integrates (i.e. averages) the input signal, results being obtained which in principle, increase the accuracy of the conversion in direct proportion to the integration time. Averages over periods greater than 10s may be achieved in practice by recording successive 10s measurements and calculating the average over the time required. The result would be a true average of the input signal. For example an input of 10.00001V measured with an integration time of 100ms (full scale 14.0000) will be displayed as 10.0000 with the least significant digit changing to a 1 once every ten readings. This indicates that the true reading (the average over a large number of readings) is in fact 10.00001.

Integration time determines the resolution, maximum sensitivity, noise rejection and, of course, the number of readings presented per second.

The maximum displayed sensitivity is limited to 1μV but achieved in the instrument and present in the Interface output data is a sensitivity to 10nV.

All integration times are available in DC AC and Ω but the display on AC is limited to 5 × 9's (full scale 140000). This is discussed more fully in the following paragraphs.

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AC MEASUREMENT

In its simplest form a dvm is able to measure dc voltage only. It can be adapted to measure ac by including an ac - dc converter before the dc input circuits. This is the case in the 7075, which employs a sophisticated circuit which converts the input into a dc proportional to its true rms value. This is an obvious advantage over previous, mean sensing, instruments, since alternating voltages are conventionally specified by rms value. In order to appreciate the difference between rms and mean, the reader is reminded of the precise relationship between the three ways of specifying the magnitude of a sinusoidal waveform:-

$$\text{Mean} = \frac{2}{\pi} \text{ peak} \qquad \text{i.e.} \quad 0.637\ V_p$$

RMS (i.e. the *root* of the *mean* of the *square* of the input).

$$= \frac{1}{\sqrt{2}} \text{ peak} \qquad \text{i.e.} \quad 0.707\ V_p$$

Two other relationships are important when evaluating alternating quantities. They are *form factor* and *crest factor*, derived as follows:-

$$\text{Form factor} = \frac{\text{rms}}{\text{mean}} = 1.1 \quad \text{for a sine wave.}$$

$$\text{Crest factor} = \frac{\text{Peak}}{\text{rms}} = 1.414 \text{ for a sine wave.}$$

Maximum crest factor for the 7075 is specified as 5:1.

COMPUTING TECHNIQUE FOR DERIVING RMS

A circuit for deriving true rms value of an alternating quantity is, in its simplest form, a circuit which:

a. squares the input V^2

b. obtains a mean $\overline{V^2}$

c. takes the square root $\sqrt{\overline{V^2}}$

That used in the 7075 is one of many configurations based on the simplified illustration in Fig. 4.12. It has the advantage of being, to a large extent, unaffected by waveform shape.

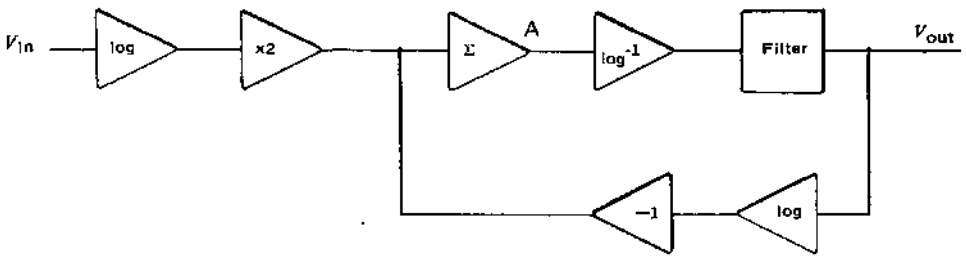


Fig. 4.12 *Typical computing technique for deriving true rms value.*

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Expressed mathematically, the output of the summation amplifier, Point A, is

$$2 \log V_{in} - \log V_{out}$$

while the circuit output, V_{out}, is:

$$V_{out} = \overline{\text{Antilog}\,(2\overline{\log V_{in}} - \overline{\log V_{out}})}$$

$$\therefore \quad V_{out} = \frac{\overline{V_{in}^2}}{\overline{V_{out}}}$$

$$\therefore \quad V_{out}^2 = \overline{V_{in}^2}$$

$$\therefore \quad V_{out} = \sqrt{\overline{V_{in}^2}}$$

It has been said that with a circuit of this type the possibility of errors due to waveform distortion are virtually eliminated. However, when the 7075 is used on pulse waveforms, care may be necessary to ensure that it is operating within the specified limits. An approximate Crest Factor value for a pulsed waveform can be calculated from the formula:

$$\text{C.F.} = \sqrt{\text{Mark/space ratio}}$$

Elsewhere in this Section it was noted that when measuring dc voltages the dvm cannot reject thermal or other dc interference. Similarly there cannot possibly be rejection of series mode ac interference when measuring ac voltages. Common mode rejection is, however, still preserved and the input circuits on ac are still fully isolated from the instrument case and from earth.

For those who are interested in pursuing the subject in greater depth, a monograph 'AC Voltage Measurement', with particular reference to waveform errors, is available free on request to Solartron.

INTEGRATION TIME

In an earlier note reference was made to the limitation of scale length imposed on the ac mode of measurement. All integration times are available on AC but selection of the two longer periods is not accompanied by the increased resolution obtained in dc measurement. Selection of 1s or 10s integration time introduces Digital Filtering, enabling more stable, less noisy readings to be achieved with low frequency ac inputs. It is recommended that, in a noisy environment, users wishing to measure low frequency ac voltages make use of the significant advantages to be gained, by selecting one of the two longer integration times.

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RESISTANCE

The 7075 measures the value of a resistor by passing a defined current through it and measuring the resulting potential difference. The current is small so that the power dissipated in the resistor is negligible.

Resistance Value measured	Current used
$< 14k\Omega$	1mA
$> 14k\Omega < 1.4M\Omega$	$10\mu A$
$> 1.4M\Omega \leqslant 14M\Omega$	$1\mu A$

The $1m\Omega$ sensitivity is satisfactory for most low value measurements. Should there be a requirement for increased sensitivity on low values the voltmeter can be used on a dc voltage range to measure the potential difference across the resistor with the current provided from an external source (Fig. 4.13).

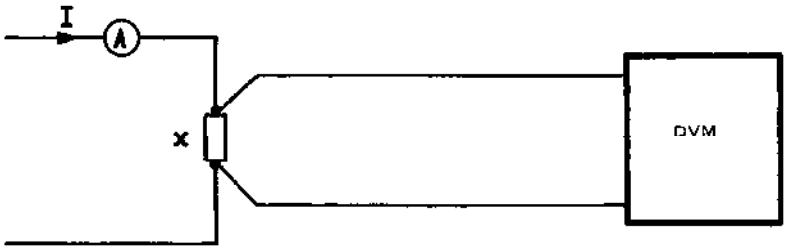


Fig. 4.13 *A very low value resistance may be measured by measuring the voltage developed across it. The voltage leads should be connected close to the ends of the resistor.*

If I is 10mA, a reading of 0.101245V means that X is 10.1245Ω. Obviously other appropriate currents could be used. The first point to observe is that, in this example, the sensitivity is $0.1m\Omega$ per digit. Hence the voltmeter connections must be made right at the ends of the resistor and must not embrace any significant length of the current carrying leads (1cm of 22swg copper wire is approximately $0.4m\Omega$).

A second point is that the accuracy is affected directly by the precision of the current setting. There would be little point in using a moving coil multimeter to set the current and then record a reading of 12.631Ω.

An improved technique is shown in Fig. 4.14.

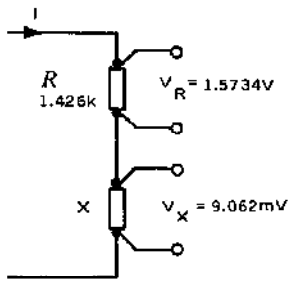


Fig. 4.14 *A ratio measurement avoids having to set a precise value of current.*

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Here a resistor R, whose value is known, is connected in series with the low value unknown X. R can be a much higher value than X. If R is not already known it can be measured on one of the ohms ranges.

The voltmeter is connected across R and the current supply adjusted to give a reading. The precise value of V_R is not important; neither is the value of the current I. In this example I could be simply provided by a 1.5V cell. The reading V_R is recorded. The voltmeter is transferred to X and the reading V_X is noted. The value of X is then given by:-

$$X = R \frac{V_x}{V_R} \text{ ohms}$$

Using the values shown in Fig. 4.14:-

$$= \frac{1.426 \times 10^3 \times 9.062 \times 10^{-3}}{1.5734} = 8.213\Omega$$

If X is being set to different values it may be necessary to measure V_R each time because, unless I comes from a constant current supply, changes of X may significantly alter I.

Should it be necessary to measure resistance at a distance from the voltmeter which is beyond the reach of the standard lead, a special lead may be obtained from Solartron. In this the four cores and screen are terminated separately as shown in Fig. 4.15.

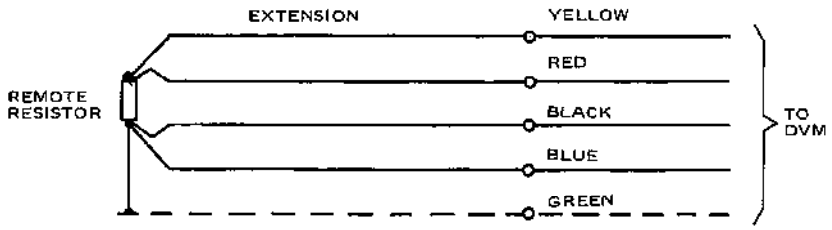


Fig. 4.15 *In measuring a remote resistor, lead compensation can be preserved by using the special input cable (obtainable from Solartron) and extending it by a 4 core screened cable.*

This cable should be extended to reach the point of measurement by means of a similar 4 core screened cable and connected to the remote resistor as shown.

This arrangement will preserve the compensation for lead resistance up to a maximum of 1Ω per wire, on any ohms range. Using an extension of 7/.0076 wires a length of 100m can be safely used. (The Yellow and Red leads may have resistances as high as 1kΩ).

The user is reminded that, should separate extension wires be used for this purpose, the connector run should be identical for each lead - preferably by employing twisted pairs. In this way the effects of interference emf's, induced in the leads as a result of local electromagnetic fields, will be minimised.

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RATIO MEASUREMENT

Ratio is a relationship, of one quantity relative to another. When considering ratio measurement one intends that measurement is to be made relative to a reference source. It is essential, therefore, when making precision ratio measurements with the 7075, that the integrity of the reference matches the stability and accuracy of the dvm. If that cannot be guaranteed, it is suggested that reference and signal inputs are derived from the same voltage source. Thus any variation in the source, providing it is within both input limits, will not affect the readings.

DC/DC RATIO

Example 1. Comparing the performance of one device against another, standard, device.

Two transducers, A and B are in the same environmental enclosure and fed from a common power source. to ensure that variations in the supply and of temperature, vibration etc., affect both devices equally (Fig. 4.16).

The output of A, the standard, is taken to the dvm reference terminals while that of B - the transducer under test - is taken to the dvm signal input.

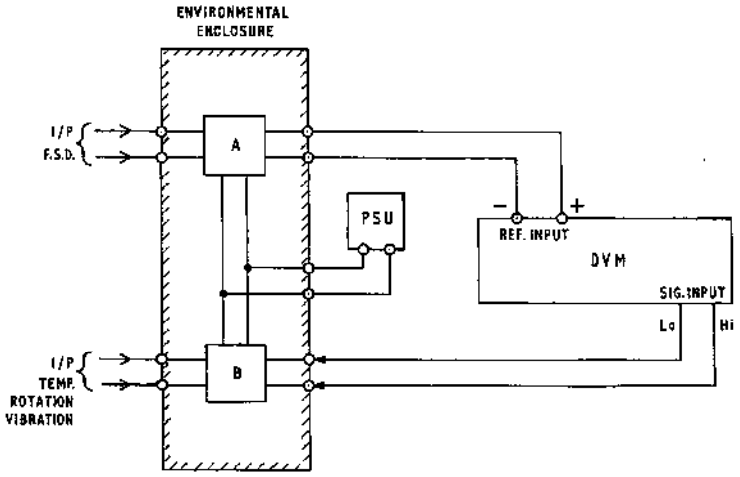


Fig. 4.16.

As was stated in Section 3 of this manual, the relationship between the dvm reading (V_{out}) and its input (V_{in}) when RATIO is selected is:-

$$V_{out} = \frac{10V_{in}}{V_{ref}}$$

Thus the ratio $V_{in} : V_{ref} = \frac{\text{displayed reading}}{10}$

which in the example is the ration of the output of transducer B to that of A. Thus a true comparison can be made.

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Example 2. Determining the actual value of a number of 0.1Ω precision resistors, given a standard resistor of known value 10.0002Ω (± 0.005%) rated at 1A.

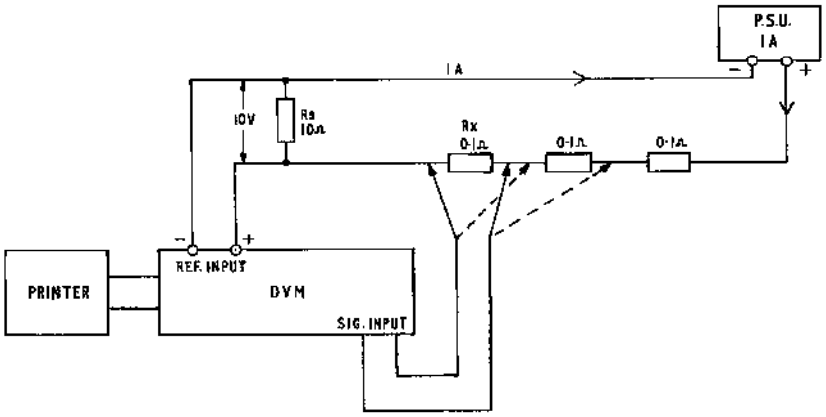


Fig. 4.17.

The constant current psu delivers 10V nominal at 1A. With the dvm operating on the 100mV range:

$$\frac{R_x}{R_s} = \text{Ratio} = \frac{\text{displayed reading}}{10 \times 10^3}$$

$$R_x = \frac{\text{displayed reading}}{10^4} \times R_s$$

If the dvm reading is 100.050mV

$$\text{then } R_x = \frac{100.050}{10^4} \times 10.0002$$

$$= 0.100053\Omega$$

Note that the resolution of the result is 1μΩ and the total uncertainty is the sum of the limits of error of the dvm on the selected range and the tolerance of the standard resistor.

This technique should be compared with that shown in Fig. 4.14 and the two important differences noted:

(i) the actual voltage across R_s does not have to be measured

(ii) provided V_{ref} does not fall below 10V (for minimum uncertainty) the source current need not be stable.

CONCLUSION

Use of the Ratio facility is not intended to, nor does it, give more accurate measurements than those possible using the instrument's internal reference. It does, however, simplify many otherwise time consuming measurement tasks. The reader will no doubt discover many more applications than the examples given.

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SECTION 5 Servicing

INTRODUCTION

Sections 5-8 contain Technical Information and are written primarily to meet the needs of the Service engineer. A detailed treatment of the principles of operation is not included but the descriptive text accompanying each circuit diagram is sufficient to enable the reader to understand the purpose of the circuit and its effect on its input(s). To facilitate fault diagnosis attention is drawn to special features of circuits, together with any precautions necessary when carrying out checks.

PRESENTATION OF INFORMATION

The circuit diagrams (Section 6) are arranged to fold out clear to the right, the functional description appearing on the facing left hand page. Similarly the pcb layout and notation diagrams will fold out clear to the left, where possible arranged to immediately precede the relevant text. Hence immediate cross reference can be made between the circuit and the component layout diagram.

Signal paths are indicated by bold lines, arrows being used where necessary to indicate the direction of functional flow. In general this is from left to right, feedback paths flowing from right to left. To prevent ambiguity however and where space is limited, this convention has not been followed rigidly.

COMPONENT IDENTIFICATION

In addition to the pcb layout diagrams, line drawings and/or clear photographs are reproduced in the manual to facilitate rapid identification of components during diagnostic checks.

The component numbers on each diagram are particular to that pcb only – thus each board will have, for example, an R1. Identification is by reference to the Parts List in Section 7.

On two major circuit boards the component numbering has been coded, a prefix digit being used to differentiate between components of the several functions carried on those boards. Thus R201 indicates R1 in the circuit coded '2'.
(This is explained in greater detail in the circuit descriptions.)

POWER RAILS

These are represented by short, detached bars annotated to show the nominal voltage. Several separate bars, annotated with the same voltage, may appear on a diagram. These of course are electrically connected to a common rail derived from the Power Supply circuits.

Zero volts may be either Supply 0V or one of six separate Signal 0V lines. Signal 'earth' rails are annotated Sig 0V1 to Sig 0V6, these being commoned at a star point. They should not be joined at any time during servicing.

Note that voltages specified on the circuit diagrams are in all cases nominal values, the actual value being dependent upon the load offered to the supply by the specific circuit. Inconsistencies between actual measured values and those quoted should not, therefore, be regarded with suspicion without considering other symptoms of possible unserviceability.

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ELECTRICAL CONNECTIONS

Scotchflex ribbon connectors are generally used for pcb interconnections, though in some instances Berg - type pins/sockets have been used where pcb's are mounted in the same vertical plane. The latter are marked 'B', followed by a number.

It is important to ensure correct mating of all inter-board connections after any servicing operation.

SPLIT PADS

These are used to provide a means of isolating various parts of the circuit for fault diagnosis and, in some instances, to permit alteration of circuit parameters for a particular operating need. They are simply bridged with solder, open circuit being effected by removing the solder. It should be noted that excessive heat applied during this operation could damage the solder track – a small, low wattage iron should be used.

TEST POINTS

A further aid to rapid circuit check-out is the provision of test pins. These are indicated on the circuit diagrams and clearly marked on the pcb's.

TEST KIT 70759C

To provide access to certain circuit areas when servicing the instrument 'live', extension connectors have been assembled into a kit which can be ordered as an Optional Accessory.

CAUTION Ohms Guard

Before commencing any Servicing the instrument should be inspected to determine whether an Ohms Guard modification has been embodied. Serious permanent damage can be caused by an inadvertent short circuit of the Ohms Guard line to earth/signal low.

FLOATING CIRCUITS

As much of the instrument's electronic circuitry is floating with respect to Supply Earth, it is recommended that an isolating transformer is used for all servicing work within this voltmeter.

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PRINCIPLES OF OPERATION

The 7075 dvm employs an A/D converter which converts the input voltage to a time analogue, which in turn is split into discrete, equal-length time units. These are counted and the result displayed as a numerical indication of the measured quantity.

The V to t converter produces a pulse train, the pulse width being variable and proportional to the magnitude of the input signal. The pulses gate the output of a fixed frequency clock into a counter, over a time period which can be chosen by the user. At the end of the time period the total accumulated in the counter is a measure of the input during that time. An averaging (integrating) technique is used whereby the total count is divided by the number of gating-pulses used. The average thus obtained is displayed as a direct reading of the measured quantity.

Statistically, the larger the sample the truer will be the average. This reasoning has been applied in the 7075, in that the integration time (the measurement period) can be varied by the user. At a fast reading rate the measurement period is very short and the average obtained is correct to, say, 2 decimal places. Increasing the measurement period provides a much truer average the resolution is increased to much smaller sub-divisions.

Since the total count is much larger when operating at the longer integration times, the counter requires more capacity. This results in an increase in scale length and it follows that the display sensitivity is improved hand-in-hand with the increased measurement resolution.

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FUNCTIONAL DESCRIPTION

7075 can conveniently be regarded as consisting of four major functional sub-divisions. Reference to the Block Diagram (Diag 5.0) will identify those as:

1. the SIGNAL CONDITIONING section.
2. the A/D CONVERTER.
3. the DIGITAL section.
4. the POWER SUPPLY.

Considering the overall functioning of the instrument, an input is processed by the Signal Conditioning circuits which change all measured functions into a dc voltage, scaled to a level suitable for further processing. Input protection, reference and guard circuits are included in this sub-division.

The correctly scaled dc signal is converted to a train of digital pulses by the A/D Converter, these pulses being used to gate the output of a Clock circuit.

Control of the measurement conversion and timing of the control sequences are two important parts of the Digital section. It also contains the counters which accumulate the gated clock-pulses, the multiplexer and memory circuits and the display drivers. The decoded counter output ultimately provides drive currents to light the appropriate Display elements.

All necessary operating power for the analogue circuits and logic levels for the digital circuits are provided by the Power Supply. Also derived from this section of circuitry is the synchronising waveform for the mains-locked clock.

SIGNAL CONDITIONING

Regardless of what measurement is being made the Voltmeter is only capable of measuring dc volts, hence all other quantities require to be converted into a dc level. Once converted, the input signal is applied to an amplifier, the gain of which is determined by the range on which the instrument is operating. It is the output of this amplifier which is compared with the instrument's reference, both being applied to the A/D Converter.

A/D CONVERTER

The analogue input, changed to a dc voltage level and correctly scaled, is converted to digital form by a circuit which produces a pulse train, the width of the pulses being proportional to the magnitude of the input. This conversion technique is known as Voltage-to-time conversion - the method employed being a variant in which the "time" is in fact the difference between two distinct time periods. It is this time-differential which is used to control the number of clock pulses finally accumulated in an up/down counter in the Digital circuits.

DIGITAL SECTION

The heart of this section is the clock which produces the pulses which will be counted to digitally measure the applied signal. The clock pulses are gated into a counter stage by the V-to-t converter output pulse train. Two counters are used, the main one being concerned with the measurement function proper while a small, 3 × 9's counter gives a fast indication of range overload and initiates an autorange action. A further, timing counter determines the counting (or integrating) period.

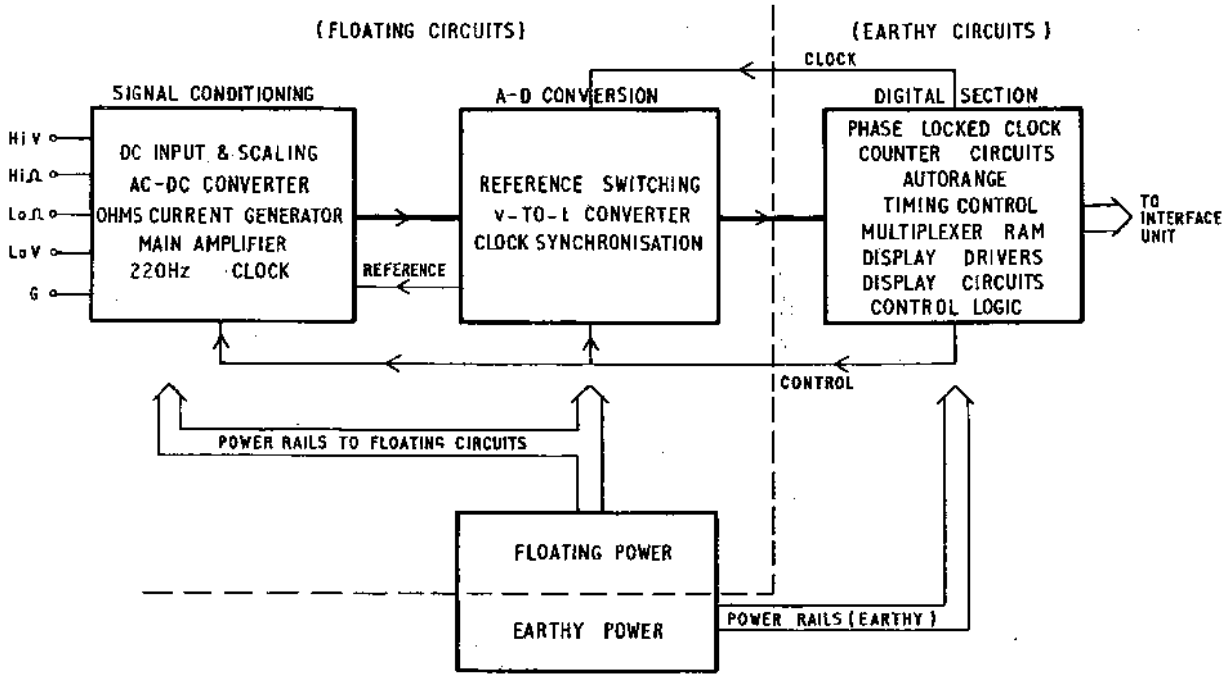
The up/down (7 × 9's) counter output is multiplexed into the random-access memory (RAM) via a zero blanking circuit. Under the control of the sequence timing circuit the RAM is accessed, outputs being applied to the display interface to generate display drive signals.

POWER SUPPLY

The power supply consists of a switching regulator driving a 25kHz invertor to provide the main supply rails. Thus no mains transformer is used and voltage tappings are not required. A small transformer is included to provide the reference frequency for the mains locked clock.

It should be noted that parts of the power supply are floating with respect to supply earth. The use of an isolating transformer is essential when carrying out checks on the floating circuits.

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Diag 5.0

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SECTION 6 Circuit Descriptions

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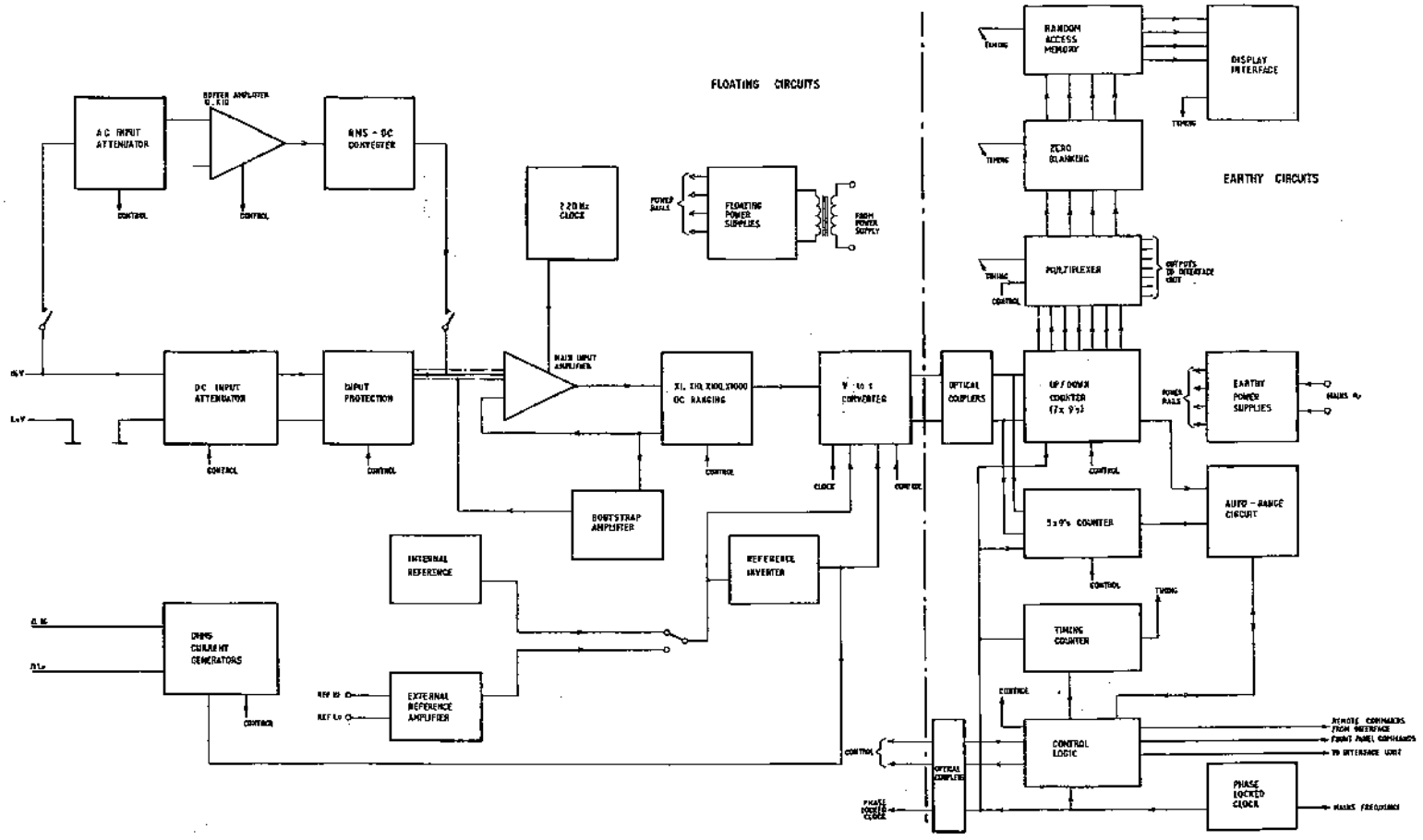
This section provides the Servicing engineer with information concerning the function of the instrument's circuits, the treatment being one of defining the *effect* of each circuit on the input(s) applied to it. In the main the descriptions follow a signal path through the circuit board, diversions from the flow being examined as they become relevant to the signal. When considering the digital circuits, however, the descriptive text is concerned more with sequences and parallel logic activities. In these instances a flow treatment is inappropriate.

INTRODUCTION

The Block Schematic Diagram (Diag 6.1) illustrates the functional layout of the instrument. The diagram can be seen to be an expansion of that in Diag 5.0 and while it's primary function is that of affording an overall appreciation of the instrument, it also provides the reader with a pictorial index to the ensuing circuit descriptions

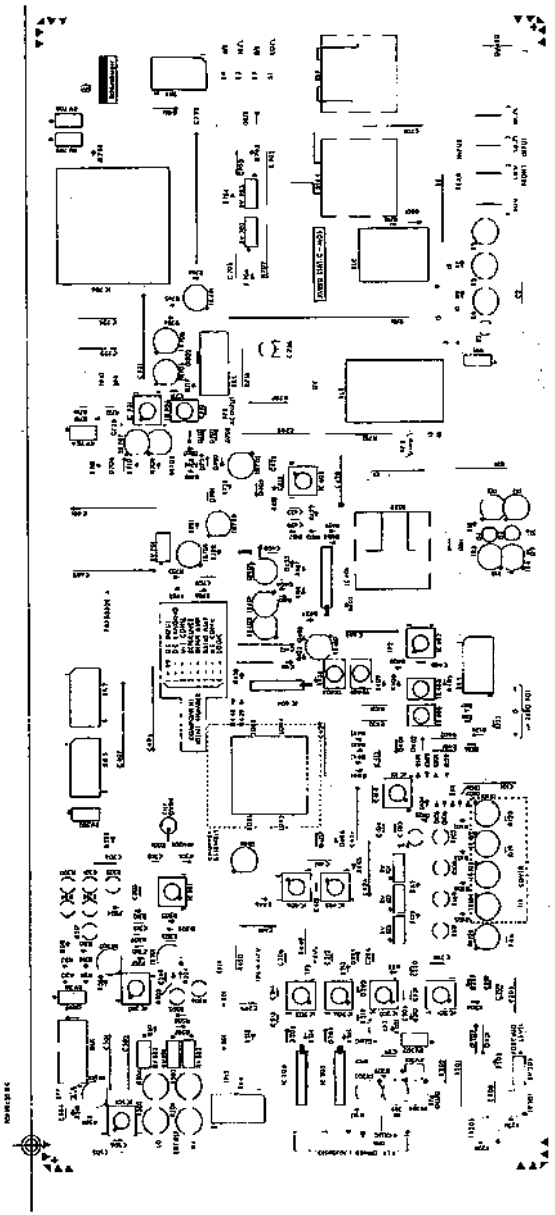
Block Schematic Diag. 6.1 →

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Block Schematic Diag. 6.1

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PCB 5 Notations

DC INPUT (Diag 6.2)

The purpose of these circuits is to provide initial conditioning of the input signal and to protect the Input Amplifier (Diag 6.3) against voltage overloads.

INPUT ATTENUATOR

The instrument can accept inputs up to 14V without attenuation, this circuit providing the necessary attenuation on the top two ranges. For inputs below 14V RLB is energised, relay drive being derived from pcb 6. The signal path is thus via R8 only. Above 14V RLB is de-energised providing 1:100 attenuation of the input signal, adjusted by RV1.
C2, R7 and R9 are spark suppression components.
The output from this stage can be monitored at Test Point 1.

INPUT PROTECTION

Despite the use of an Input Attenuator, large input swings could still occur, sufficient to overdrive the Input Amplifier. The Input Protection circuit provides an extra safeguard, limiting the signal line excursions to approximately 17V on the 10V and 1000V ranges.

On all other ranges the output from this circuit is limited to approximately 1.7V, Zeners D1, D2 being shunted by TR3, TR4.

LED's D3, D4 are used as normal diodes in this circuit. However they can provide a useful clue to an engineer if a persistent overload indication is being investigated.

AC AND Ω

This circuit provides partial conditioning for the output from the AC/DC Converter, via RLE contacts, Input Protection being identical to that described above.

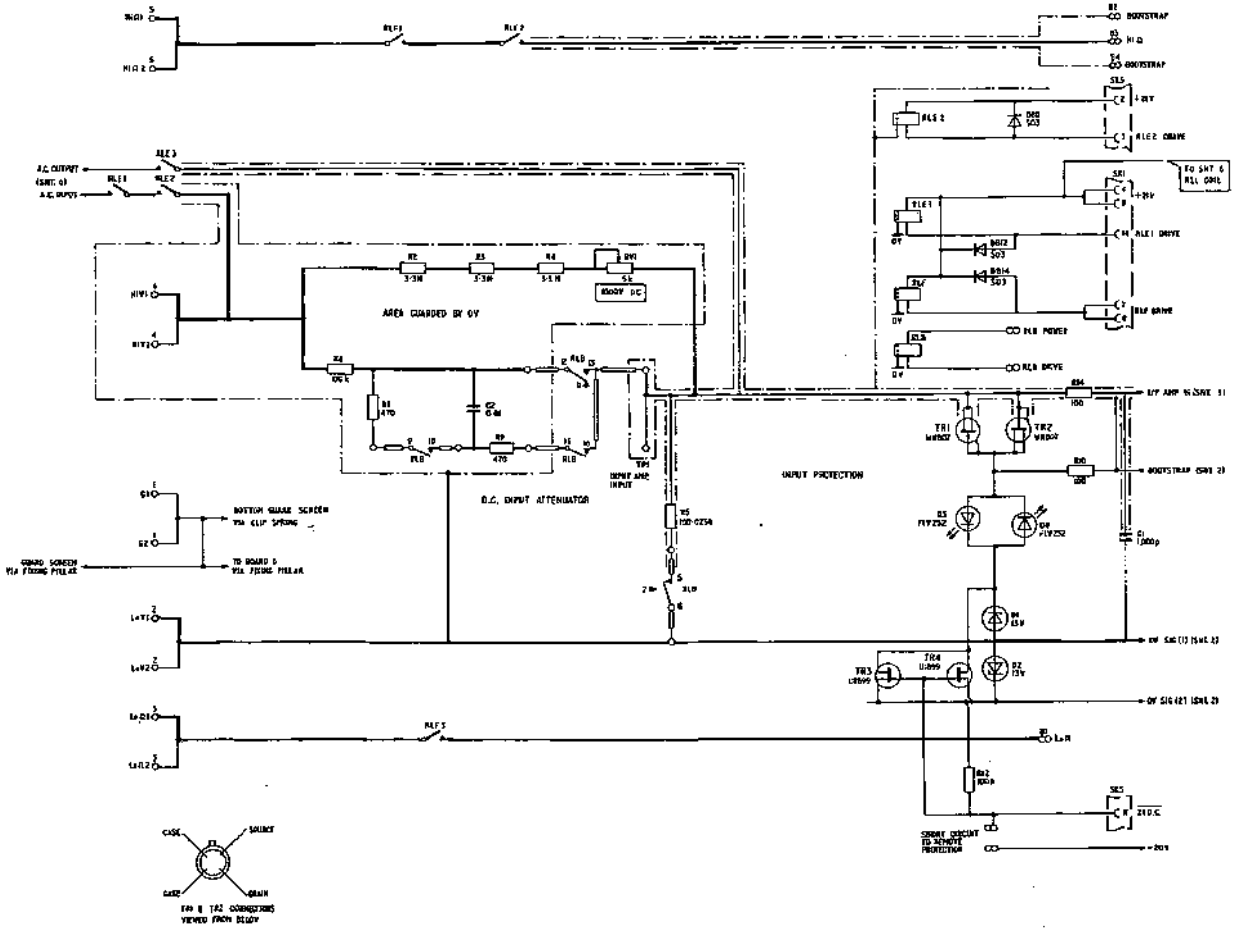
The Ohms Converter inputs are also to be found within this section of circuit, RLF providing the necessary switching.

BOOTSTRAP

Note the guard afforded to much of this circuit by the Bootstrap line. The output of a voltage follower (BOOTSTRAP AMPLIFIER, Diag. 6.4) provides local voltage 'guard', supplementing the effect of the main instrument Guard. Bootstrap potential is always that of the input to the main Input Amplifier.

PCB 5 Notations

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DC Input Diag. 6.2 pcb 5 (sheet 1)

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INPUT AMPLIFIER (Diag 6.3)

All input signals, however derived, are applied to this circuit, the last in the signal conditioning chain. In conjunction with the DC RANGING circuit (Diag 6.4) the signals are scaled to a level suitable for processing by the A/D converter. The circuit is "area" coded 4.

MAIN AMPLIFIER

This is the amplifying element proper, the output from the circuits on Diag 6.2 being applied to a differential amplifier, which in turn feeds the operational amplifiers, IC's 402 and 408.

The gain of this operational amplifier is determined by the range resistors shown on Diag 6.4 .

DRIFT CORRECTION

The function of the remaining circuits illustrated is that of correcting differential amplifier drift caused by temperature variations. The drift errors, being no more than a few μ volts, are amplified in a Chopper Amplifier stage, the chopping being performed opto-electronically at 220Hz. LDR's 1 to 4 are light dependent resistors forming the Modulator. The amplified error is demodulated, the same 220Hz waveform (derived from pcb 6) driving the Demodulator. After passing through the Filter the drift correction potential is applied to one side of the differential amplifier output (IC 401).

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DC RANGING (Diag 6.4)

The gain of the main Input Amplifier (Diag 6.3) is controlled by the scaling resistor network in this circuit, which also provides an additional measure of Input Amplifier protection, relative to Bootstrap. The circuit is "area" coded 1.

DC RANGING

The FET switches TR's 101 to 104 are switched on by ranging signals derived from the DC Decoder on pcb 6. Thus the amplifier gain is determined by one of the matched set of 4 resistors R107 to R110. (Note that R111 completes the matched set).

BOOTSTRAP AMPLIFIER

IC101 is a low output impedance unity gain voltage follower producing an output which faithfully follows the input to the Input Amplifier. Its function in this circuit is to provide a rapid means of switching off FET's TR101 to 104. As mentioned earlier, Bootstrap also affords additional input guarding throughout the Input circuits.

PROTECTION

The Input Protection circuit shown in Diag 6.2 was concerned with protection relative to Signal 0V. The circuit shown here provides protection relative to the Bootstrap line.

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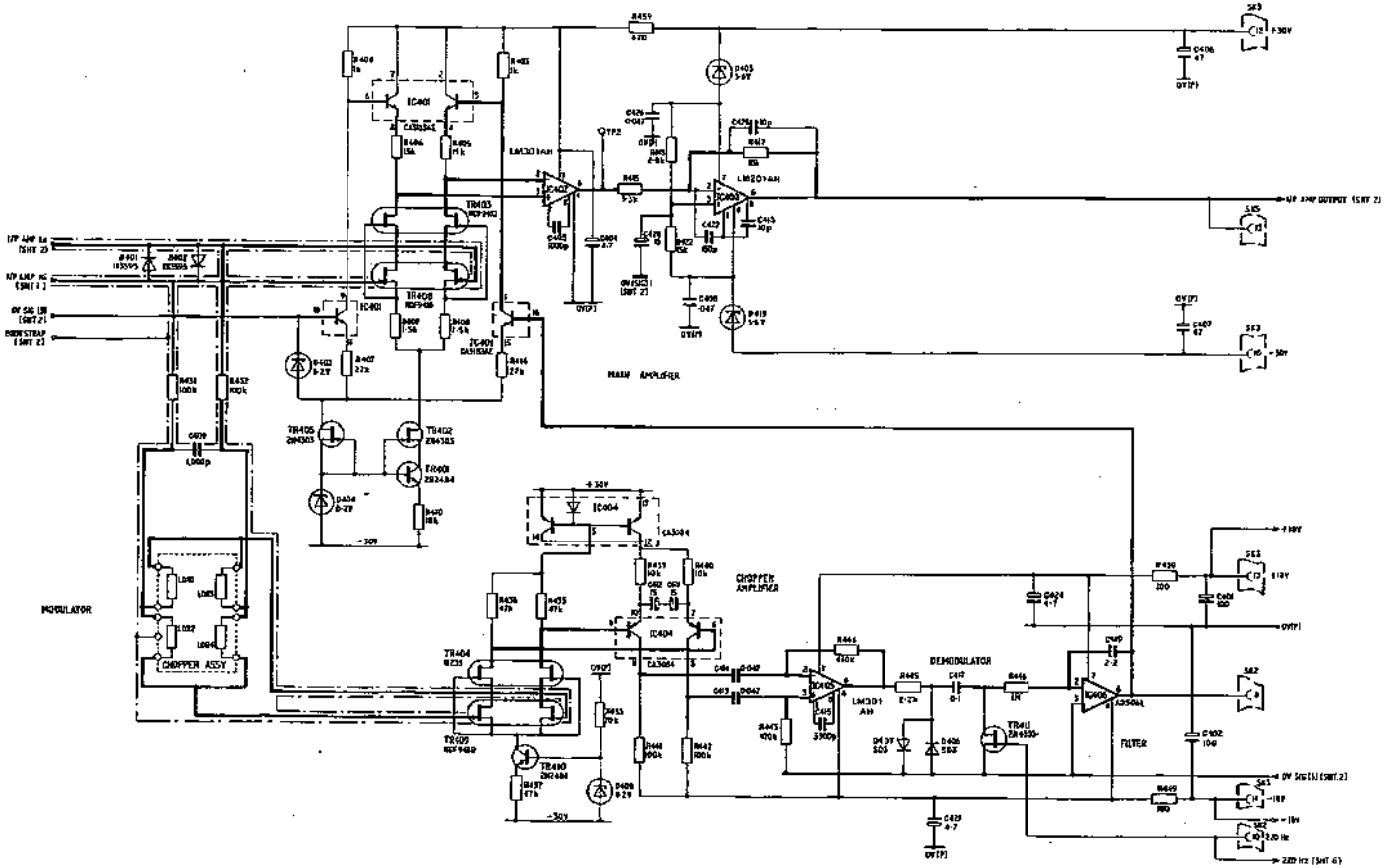








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Input Amplifier Diag. 6.3 pcb 5 (sheet 3)

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V to t CONVERTER (Diag 6.5)

This circuit performs Analogue to Digital conversion, the applied voltage being converted to time periods which are used to gate the output of a Clock circuit. The circuit is clock synchronised to ensure that the pulses in the "pulse train" start and finish exactly on a clock edge. This section of pcb 5 is "area" coded 1.

INTEGRATOR

A continuously running Dynamic Integrator is driven between preset limits by a 1kHz forcing waveform, to produce a symmetrical triangular waveform output.

LEVEL DETECTOR

Compares the excursions of the Integrator output with reference levels, switching Integrator reference potentials which maintain the closed loop action of the Integrator. This system can be regarded as having pulse-width modulated feedback — the pulse width varying in proportion to the input signal applied to the instrument.

REF. SWITCHES

Controlled by the Level Detector via the FET Driver, these switches apply one of two reference potentials, or Sig. 0V to the "virtual earth" of the Integrator. The cut-on/cut-off of the FET switches is determined by the polarity of the input (dc) and its magnitude. The voltage across R202 can be represented by a train of positive and negative pulses, running at 1kHz, the pulse width being variable with voltmeter input.

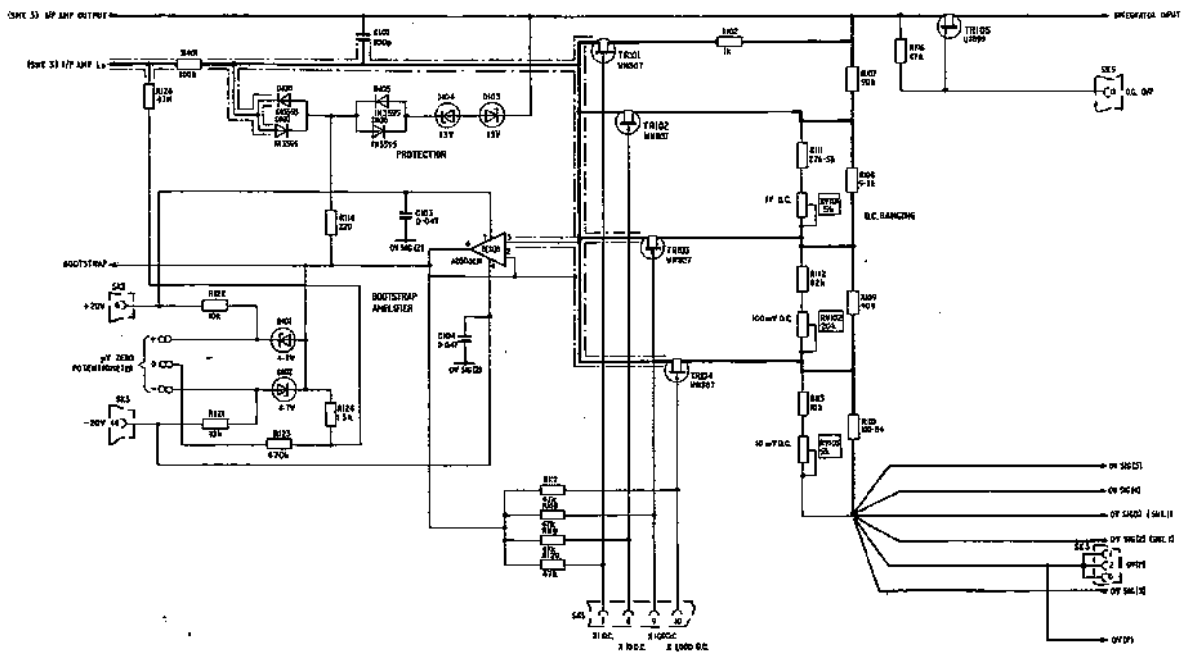
CLOCK SYNC.

Synchronisation of the feedback waveform with the Clock is achieved by this section of the circuit.

FET DRIVER

The circuit carried on pcb 12 is described overleaf.

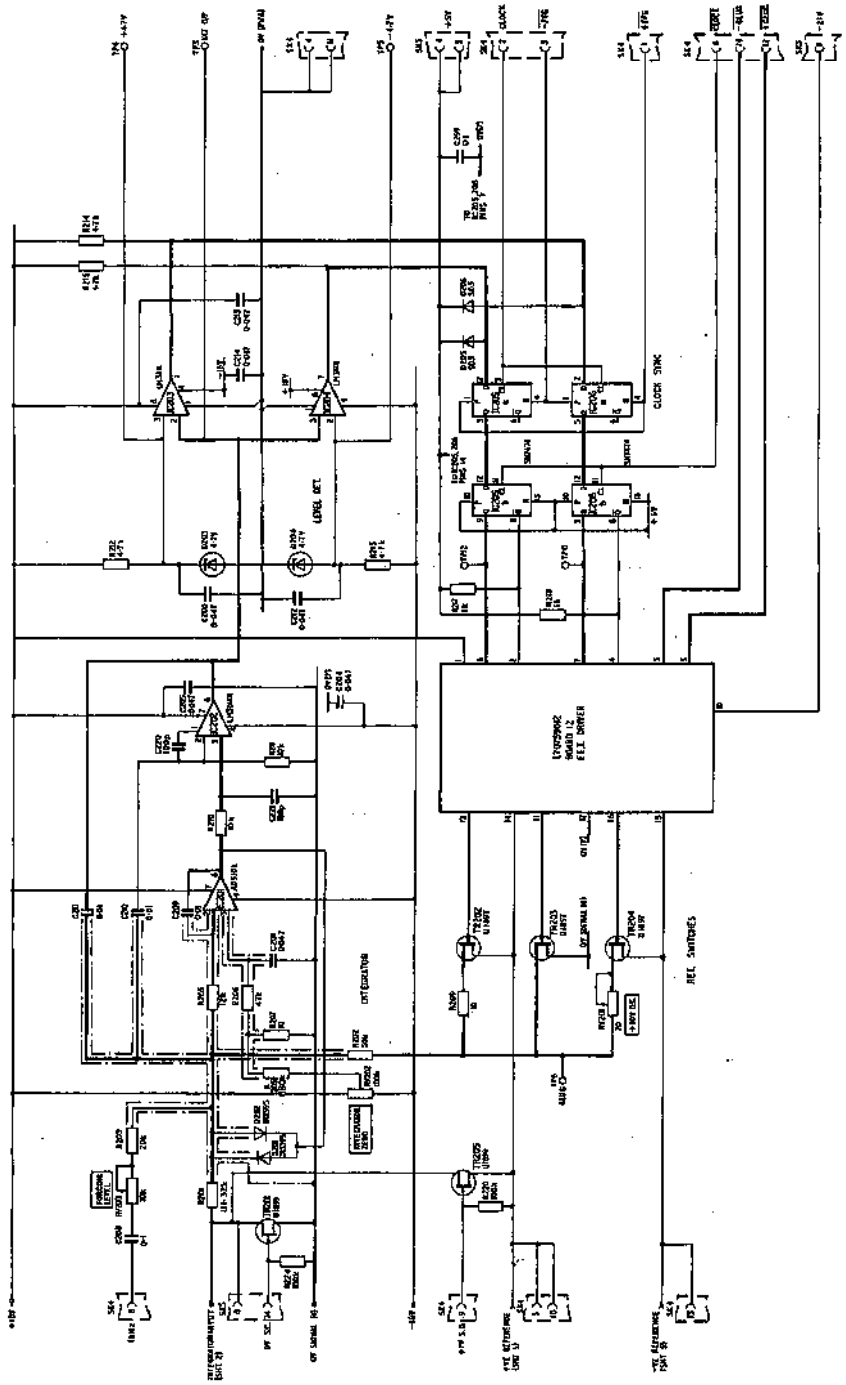
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DC Ranging Diag. 6.4 pcb 5 (sheet 2)

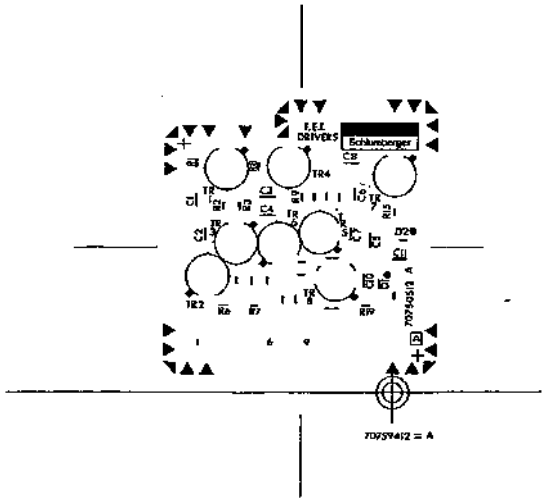
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V to f Convertor Diag 6.5 pcb 5 (sheet 4)

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PCB 12 Notations

FET DRIVERS (Diag 6.6)

The circuit illustrated, though forming part of the reference switching arrangement on Diag 6.5, is carried on a separate plug-in card, pcb 12. Interconnection with board 5 is via Berg-type horizontal sockets, the mating pins being mounted vertically on board 5.

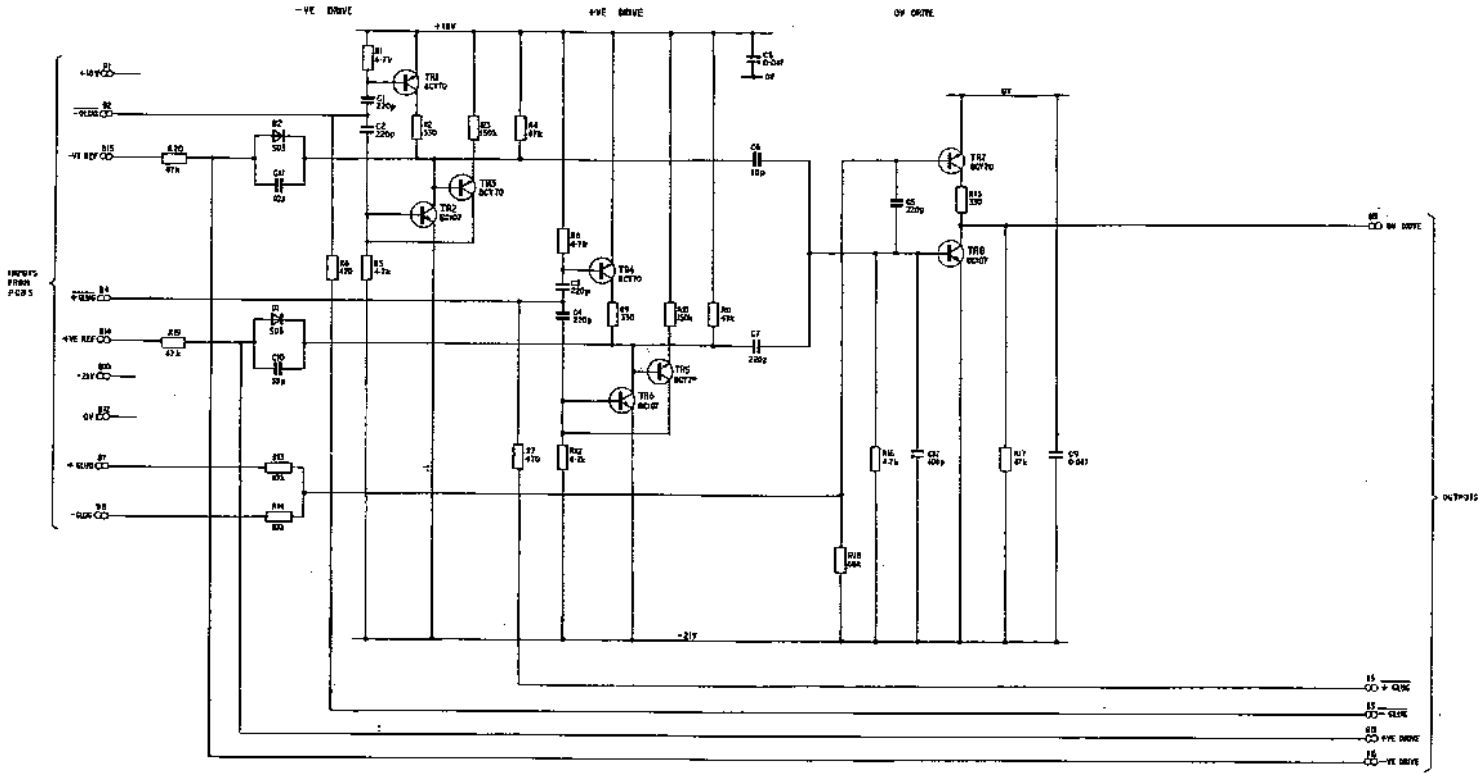
The FET Drivers provide fast switching of the reference potentials and 0V, the circuit configuration ensuring rapid transition from one switch state to the other. TR3, TR5 perform a 'latching' function for the ON state of their associate switches. In the case of the 0V switch both ON and OFF states are latched by the inputs on pins B7, B8. Pins B6, B9 are not used.

GLUG

Within this manual the reader will find many signal annotations which include the word "Glug". The word may be abbreviated to the letter 'G', as in FG (*forced* glug), FFG (*forced forced* glug) etc. The term is used as a convenient alternative to the cumbersome title "Quantum of Charge" (i.e. V × t) and should be treated merely as an identifier label, facilitating circuit tracing.

← PCB 12 Notations

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Fet Drivers Diag. 6.6 pcb 12

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AC CONVERSION (Diag 6.7)

Diag. 6.7 illustrates the circuits concerned with processing an alternating input to produce an equivalent dc level. The dc thus obtained is further conditioned as described in earlier pages under "DC". This circuit is "area" coded 7 on pcb 5.

AC ATTENUATOR

Three alternative signal paths provide attenuation as follows:

On the 1000V range	1 : 1000 via R701, R702, RLL
On the 10V, 100V ranges	1 : 100 via R701, TR701
Other ranges	no attenuation via RLC

The output from this stage is thereby scaled to a maximum of 1V. Relay drive for RLC and RLL is derived from the AC DECODER circuit (FLOATING LOGIC pcb 6), as is the signal $\overline{\text{AC ATTEN}}$. Potentiometers RV702, RV703 provide attenuator adjustment for the 10V and 1000V ranges while C736 is adjusted to balance the attenuator for 100V at input frequencies above 10kHz.

BUFFER

The Buffer Amplifier has a dual role, that of isolating the input from the low input impedance of the Converter and of providing amplification of small input signals from the attenuator. Buffer gain is switched between unity and X10 by TR's 705, 706, R704 controlling the gain at 100mV.

AC SCALING SUMMARY

Nominal Range	Attenuation			Buffer gain	
	1 : 1000	1 : 100	1 : 1	X1	X10
100mV	–	–	√	–	√
1V	–	–	√	√	–
10V	–	√	–	–	√
100V		√	–	√	–
1000V	√	–	–	√	–

CONVERTER

IC706 with its associated components performs the conversion of the rms of the ac to a dc level.

Zero adjustment is provided by RV705, the 1V output potentiometer being RV706.

SELF CHECK

The voltmeter internal reference is chopped at 220Hz and applied as a 100mV ac "reference" to the Buffer, via the switch TR709, TR703. The 1V signal thus obtained is scaled to give a Self Check display of 10V.

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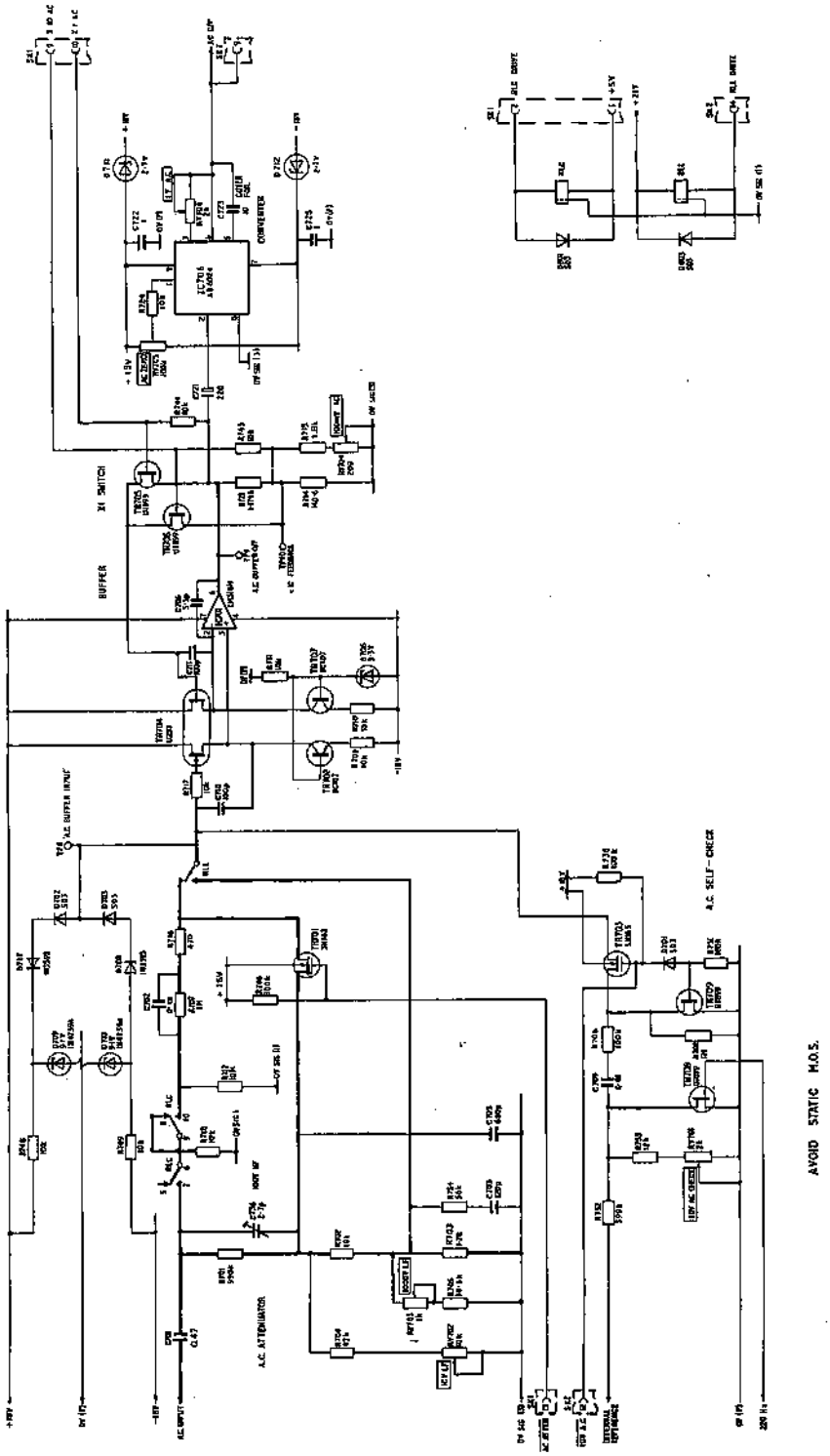






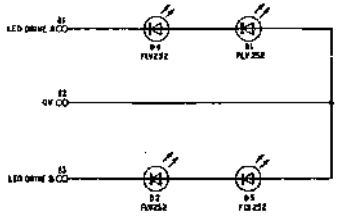




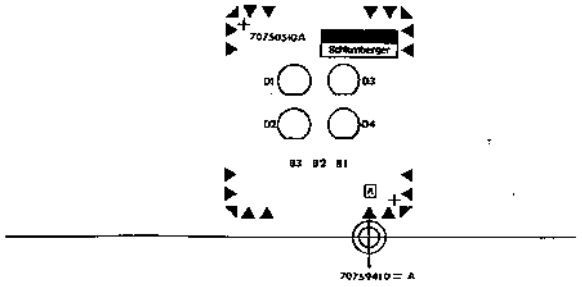



AC Conversion Diag. 6.7 pcb 5 (sheet 6)

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PCB 10 Circuit Diagram



PCB 10 Notations

RESISTANCE (Diag 6.8)

Resistance measurement with the 7075 is accomplished by measuring the voltage developed across the unknown resistor by virtue of a known current passing through it. The major function of the section of Board 6 illustrated is that of generating the necessary current. The circuit is "area" coded 6.

CURRENT GENERATORS

The instrument's negative reference is utilised to determine a current which, in it's turn, produces a reference potential relative to the +30V rail — divided down across R602, R604 (a matched set). This potential defines the Hi Current, the value of which depends on the position of reed switches as follows:

RLH 1 closed	1mA	(10Ω to 10kΩ)
RLG 1 closed	10μA	(100kΩ to 1MΩ)
Both reeds open	1μA	(10MΩ)

The Lo Current generator provides the necessary current sink to give effective 4 - terminal measurement, potentials arising from lead resistances being nullified. The second contacts of reeds RLG, RLH perform a similar function to those outlined for RLG1, H1 above.

Link A across R603 is set as required during factory calibration. IC's 601 to 603, unity gain amplifiers are used in this configuration as voltage followers. High voltage (up to 300V) protection is given by D606, R610 and TR's 605 and 606.

Note that the Hi Current circuits are guarded relative to the potential developed across R604, Bootstrap providing the remaining guard potential.

SELF CHECK

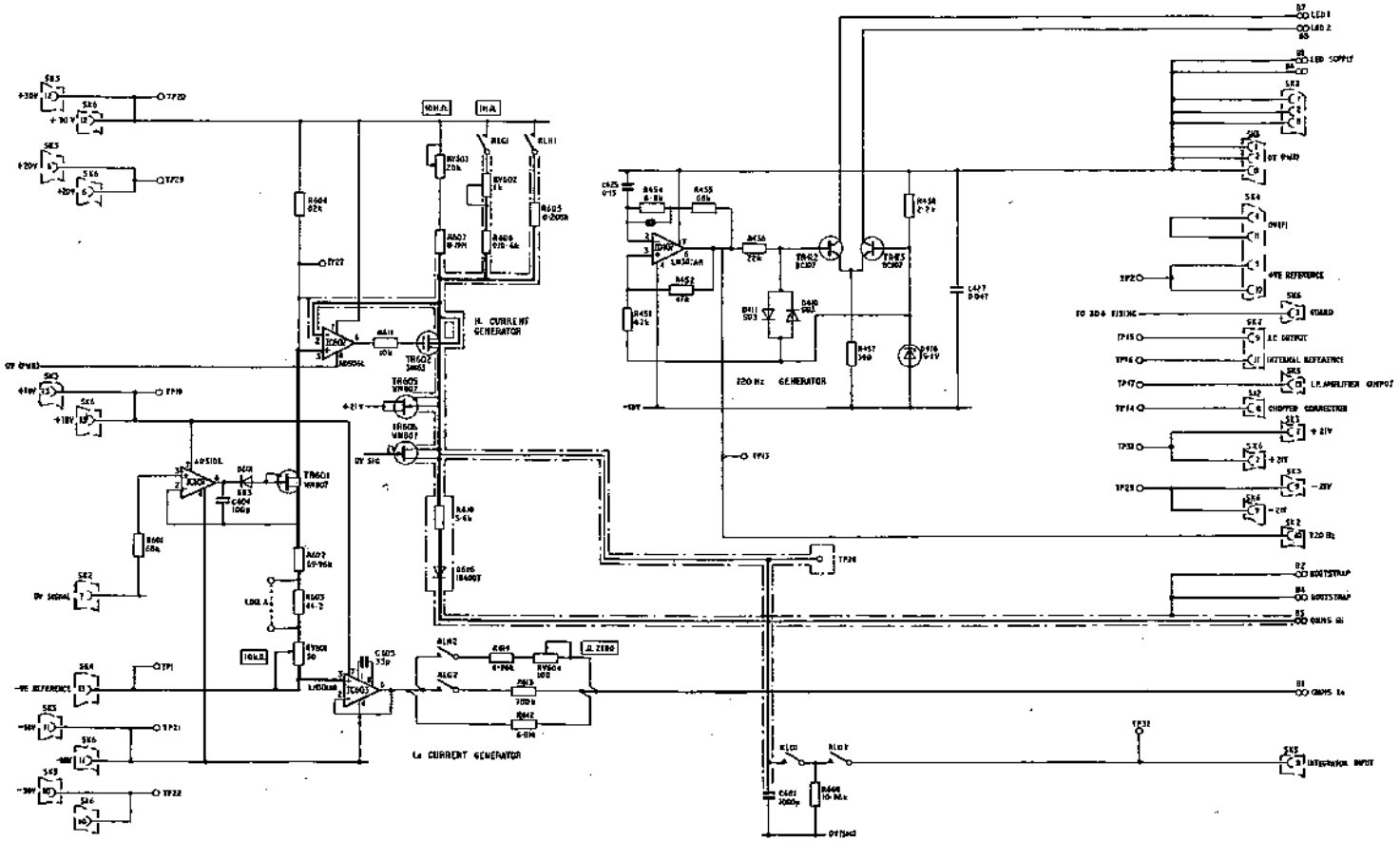
The 1mA current through R608 in parallel with the input resistance of the Integrator produces 10V for the nominal Self Check 10kΩ display. Control is via RLD.

CHOPPER DRIVE

Also illustrated in Diag 6.8 is the 220Hz Generator (area code 4) which produces the chopping waveform used in the Input Amplifier circuit (Diag 6.3). Outputs are taken via Berg pins 5 and 7 to the LED's forming part of the opto-electronic Chopper Modulator (Diag 6.3). A further output feeds the Demodulator in the same circuit area of pcb 5. A link is provided across R454 to permit a small adjustment of the nominal 220Hz, if the oscillator frequency is found to be a harmonic of the supply frequency.

← PCB 10 Notations and Circuit Diagram

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Resistance Diag. 6.8 pcb 6 (sheet 1)

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REFERENCE (Diag 6.9)

The voltmeter's reference potentials are generated in the circuits illustrated, which are "area" coded 3 on Board 5. The other circuit, coded 5, processes the External Reference associated with RATIO operation.

INTERNAL REFERENCE

Zener D301 defines the +ve Reference at +9V above the potential of the inverting input of IC301. The zener current is that through R301 derived from the Inverter. The junction of the matched pair R321 R322 is at --2V, regulated by the action of IC301, TR301. Thus the emitter of TR301 is held at +7V, which is used as the +ve Reference.

The network R311 through R320, with RV301, is used during calibration to take out zener tolerances and thus accurately define the +7V.

REFERENCE INVERTER

The system is stabilised by using an inverted version of the +ve reference as the current source for D301. A closed loop is thus formed, producing --7V at TR302 emitter for use as the —ve Reference.

The circuits described, once set up, are very stable and independent of variations of the 18V rails. However under certain circumstances it would be possible for latching to occur in the wrong direction. D303 prevents this by holding TR301 base above +5V.

RATIO AMP

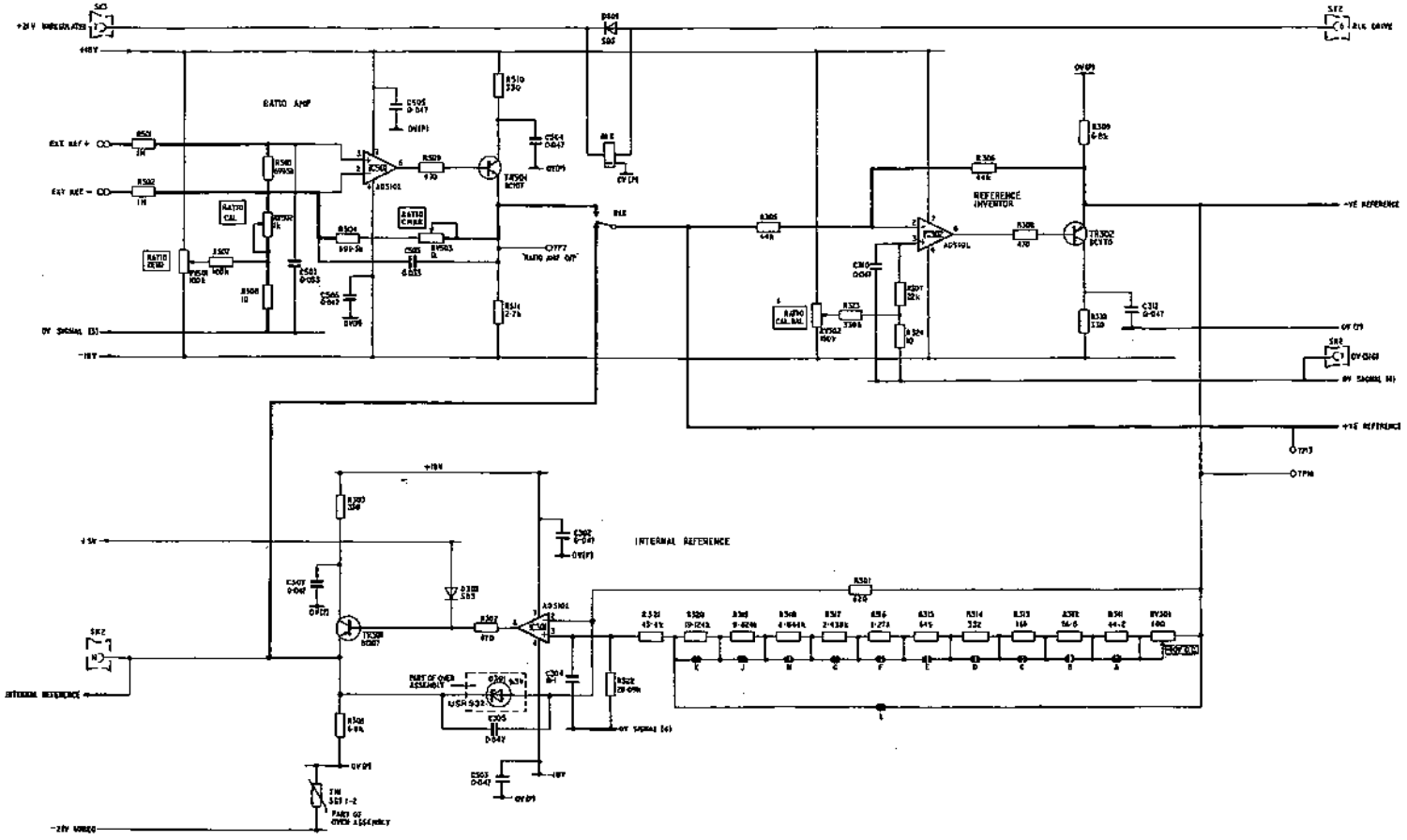
An external reference is fed to the Inverter via IC501, TR501 and the changeover relay RLK. This replaces the Internal Reference with the user's choice of reference potential for RATIO measurement.

RV503 corrects for Common Mode errors between Ratio Hi and Ratio Lo, RV502 setting the output of IC501/TR501. Offsets in the IC are taken out by RV501.

Offsets in the amplifier IC302 are taken out by adjusting RV302, such adjustment forming part of the RATIO calibration procedure.

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Reference Diag. 6.9 pch 5 (sheet 5)

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FLOATING LOGIC (Diag 6.10)

The main function of the area of Board 6 coded 8 is that of decoding Front Panel (and Systems Interface*) Commands associated with measurement Mode (Function) and Range. The circuits are floating with respect to supply 0V, data transfer being accomplished by means of optical couplers. The circuit coded 2 forms parts of the V - to - t Converter (Diag 6.5).

SERIAL DECODER

Data is sent at the beginning of each reading to determine the Function and the measurement Range. The state of the Serial Data lines is fed as an 8 - bit serial word to the Serial Decoder, strobed by an 8 - pulse clocking signal, Serial Strobe (Test Point 12). The resulting data is set on lines A to H of the 8 - bit shift register IC819.

NOISE REJECTOR

This binary counter circuit only produces a strobe output if the 8 - pulse clocking signal is complete. Thus spurious noise peaks are not detected as Clock pulses.

The strobe thus produced clocks the output lines of the Shift Register into a pair of 4 - bit buffer stores, IC's 814 and 815, the decoded Mode and Range data being held for the duration of the current reading.

SK8 is a test socket for use with an ATE device such as Membrain.

MODE DECODER

Apart from RATIO, which is processed directly into a drive for RLK (Diag 6.9), the binary Mode code and that for Self Check are decoded in a 4 to 16 line decoder IC802. For each of the possible input codes one of the 16 output lines is set Lo. All 16 outputs are connected, those corresponding to each measurement mode being commoned in 4 - way wired OR networks. The remaining 4 outputs specify the measurement tests of the Self Check function — shown in tabular form overleaf.

AC DECODER

IC's 803, 804 and 805 (excluding pins 5, 11 and 2, 14) provide the necessary decoding and current drive for the control of the AC signal conditioning circuits (Diag 6.7). The input on pin 12 of IC803 is the AC decode from the Mode Decoder, the other inputs being binary coded Range data from IC815.

OHMS DECODER

Control for the Ohms Converter (Diag 6.8) is derived from this circuit, the input being $\overline{\Omega}$ from the Mode Decoder and Range data in binary code from IC815.

DC DECODER

Together with part of IC805 (pins 5 and 11), this section of the circuit generates the control and drive signals for the DC Signal Conditioning circuits (Diags 6.2, 6.3, 6.4). $\overline{DC}$ and binary coded Range data are the inputs, derived from IC802 and IC815 respectively.

*see Section 9 of this manual.

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SELF TEST (Diag 6.10)

Test	IC802 Pin No.	Decoded/Processed by	Range/Mode Selection	Control Signal Output	Effective on Diagram
7V dc	5	IC813(b), IC805		7V SC	6.5
			D804, IC808	DC O/P	6.4
0V	1	IC811(d), IC808		0V SC	6.5
			D813, IC808	DC O/P	6.4
10V ac	14	IC805		10V AC	6.7
			IC811(b), IC812(e).	RLE/2 DRIVE	6.2
			IC809(b), IC811(c), IC808, IC807.	X10 DC (Note 1).	6.7
10kΩ	9	IC810(c)		RLD DRIVE	6.8
			D805, IC808	DC O/P	6.4
			IC810(c), D815	RLH DRIVE (Note 2)	6.8
Display	--- (Note 3)	---	---	---	---

Notes

1. This control signal selects the correct scaling factor for the test ac.

2. RLH is energised to provide a measurement current of 1mA.

3. Self Check Test No. 5 is not decoded on this board. The Control Signal LAMP TEST, derived from the Self Check logic on pcb 3, is connected directly to pcb 2. The decode is equivalent to Test 1 (code 00).

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INTEGRATOR CONTROL (Diag. 6.10)

The Integrator Control logic, "area" coded 2, provides controlling waveforms for the dynamic integrator described earlier (V - to - t CONVERTER, Diag 6.5). A floating circuit, the inputs to it are made via optical couplers.

INTEGRATOR CONTROL

Clock pulses are processed by IC209, the three sections of which provide ÷ 16, ÷ 10, ÷ 10 to the input 1.6MHz. The resulting square wave at 1kHz is the Forcing Waveform (FW) controlling the ramp up and down of the Integrator (Diag 6.5). D207 limits the positive excursions of FW to +10V.

The 1kHz signal is further processed by IC207(a) and (b) to produce two pulses, each coincident with an edge of FW. The pulses, +FFG AND −FFG, are utilised in the Clock Sync circuit of the V - to - t Converter (Diag 6.5).

PCB 6 Notations ⟶

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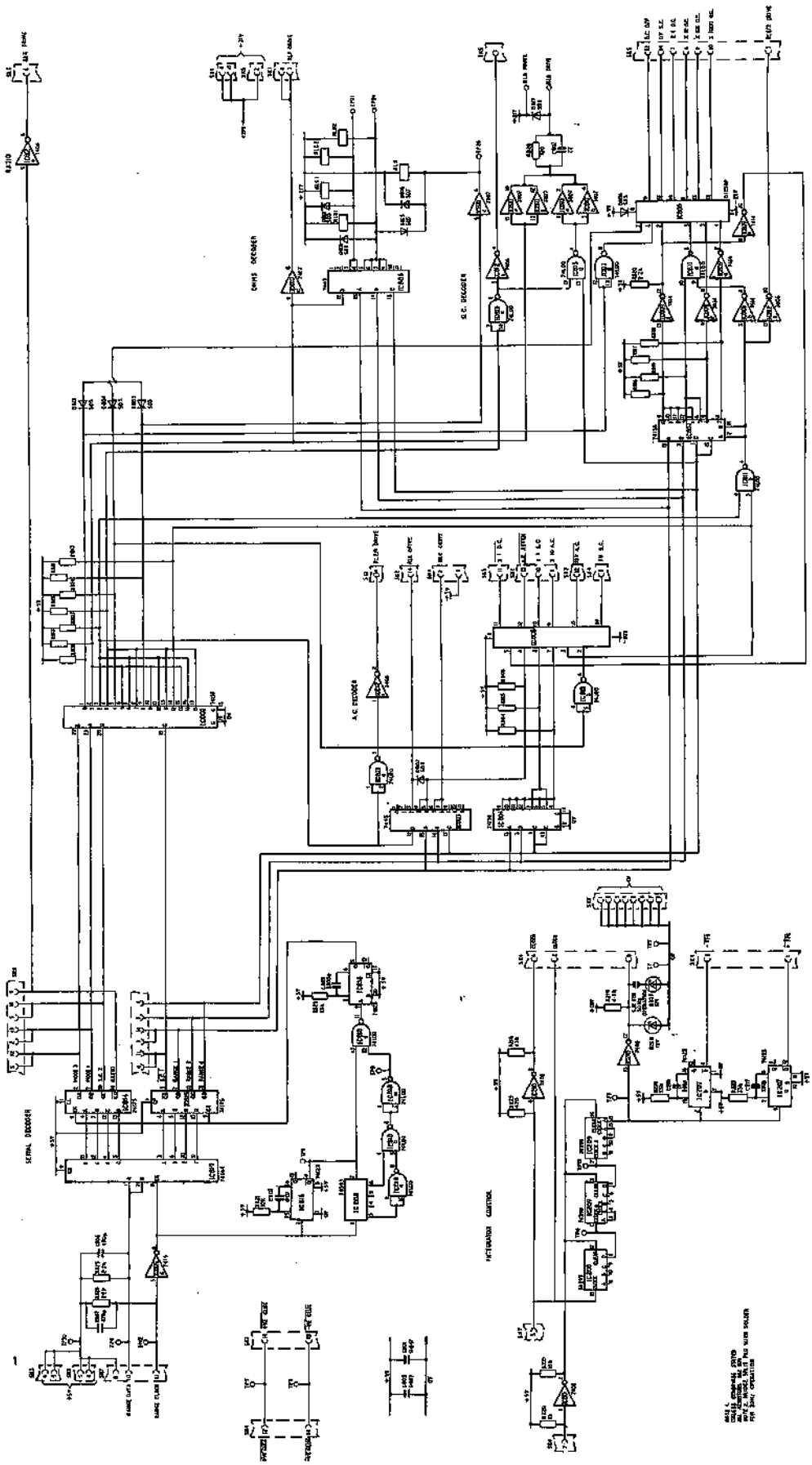






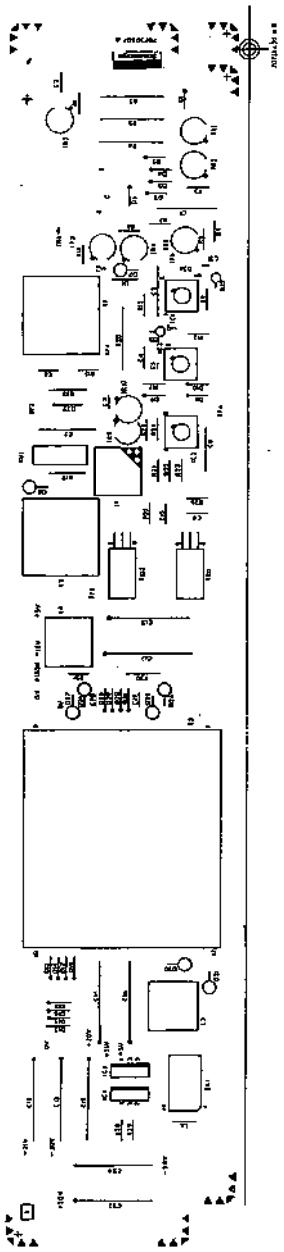


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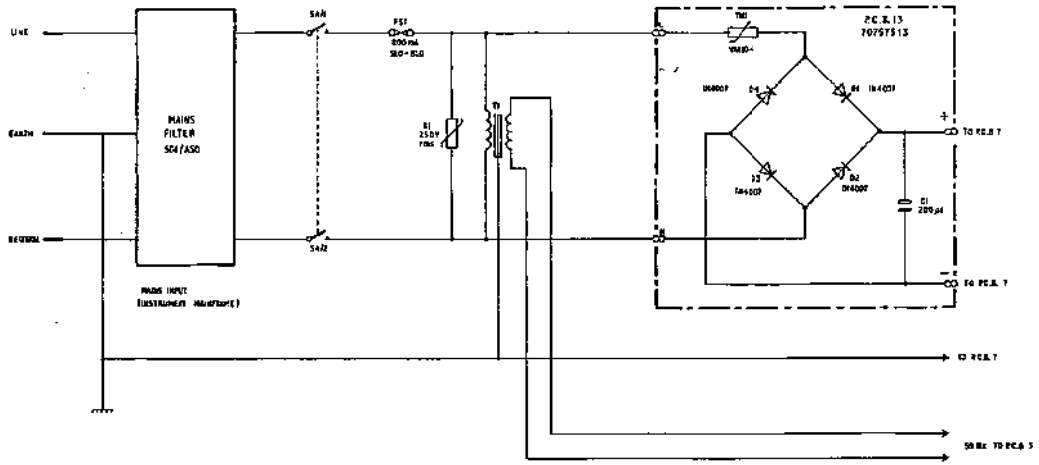


Floating Logic Diag 6.10 pcb 6 (sheet 2)

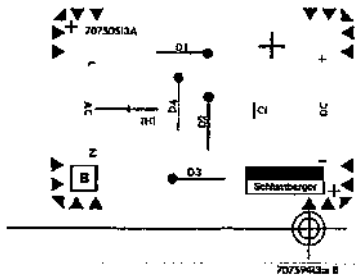
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PCB 7 Notations



Mainframe Diag. 6.11



PCB 13 Notations

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POWER SUPPLY (Diag 6.12)

The instrument's power rails are derived from the circuits on the facing page and that shown overleaf.

Applied directly, without the use of a mains transformer, the supply voltage is roughly rectified by the circuit on pcb 13 (Diag 6.11) before being converted to a regulated dc by a Switched Regulator circuit. The dc thus obtained is again converted to a stable ac by means of an Inverter stage, the output of which feeds the primary of a transformer.

The transformer secondary winding and it's associated conventional rectifier circuits are shown on (Diag 6.13).

START UP

When the instrument is switched ON this circuit produces an initial supply for the remaining circuits. The current through TR3 is controlled by that through TR1, which is itself dependent on TR2. The base level for D4, D5 is determined by TR2 which conducts reducing TR3 conduction when the potential across the zeners exceeds their combined nominal limit. The circuit thus operates in a closed current loop maintaining the junction of D5, R4 at +30V derived from the mains input.

VOLTAGE REGULATOR

After the initial current surge the circuit described above settles very rapidly. The Voltage Regulator then takes control to re-define the +30V rail and switch-off the Start Up circuit. A series transistor, TR6, is switched on/off at 30kHz by the output of oscillator IC1 via TR8, TR5. The mains supply is therefore pulsed by TR6 before being smoothed by choke L1. The mark/space ratio of the switching 30kHz is controlled by the output of comparator IC2, determining the ON/OFF time of TR6 and thus the regulated voltage level. RV1 adjusts the comparator 'sample' to set the output of the regulator to +70V.

The current through R20 now defines the +30V rail and, via D5, D4, it causes the now redundant Start Up circuit to be turned off.

Note that mains ripple is eliminated by the high switching speed of IC's 1 and 2.

INVERTER

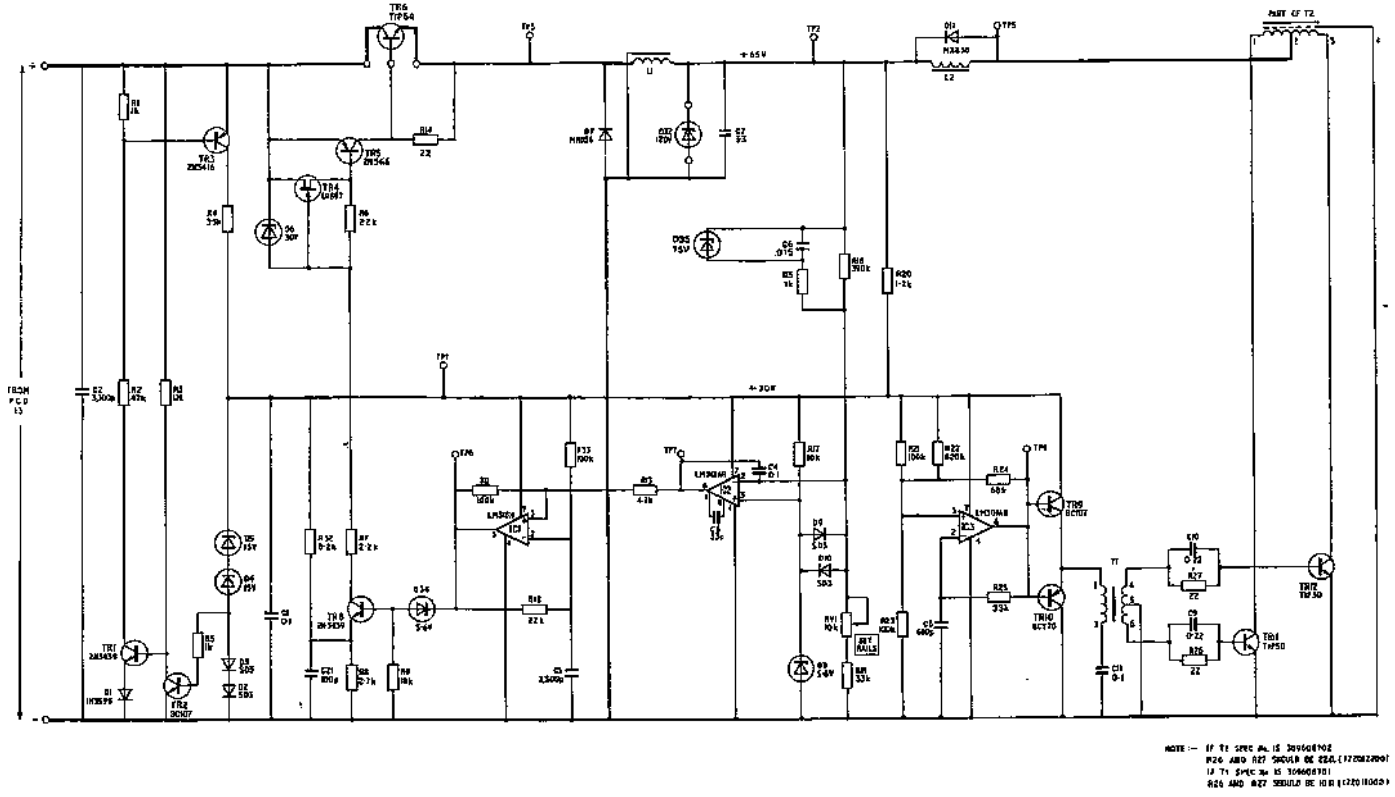
IC3 is connected as an oscillator, switching the common emitter of TR9, TR10 between +30V and the neutral rail, at approximately 20kHz. The square switching waveform, stepped down by transformer T1 causes TR11, TR12 to alternately turn on and off. Thus the primary winding of T2, centre fed by the regulated +70V rail, produces an alternating current which is independent of mains supply voltage and frequency. This "supply" is used in the rectifier circuits which follow.

Diag. 6.11. PCB 7 and PCB 13 Notations

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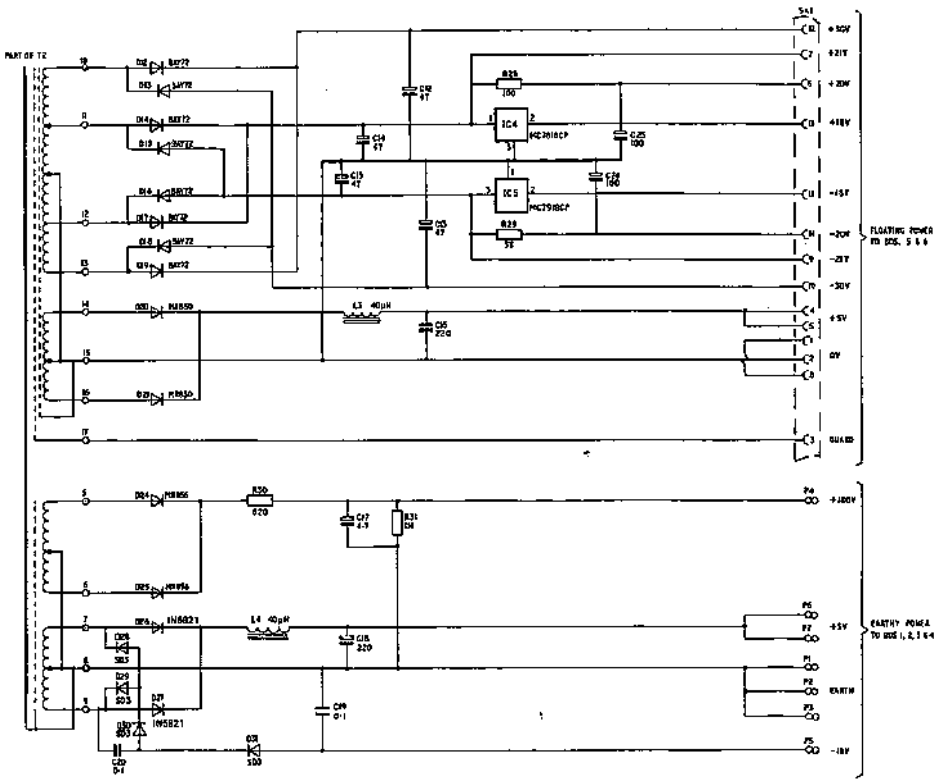


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Power Supply Diag. 6.12 pcb 7 (sheet 1)

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Rectification Diag. 6.13 pcb 7 (sheet 2)

RECTIFICATION (Diag. 6.13)

T2 secondary windings provide the rectifier current required to power the various dc rails used within the voltmeter.

IC4, IC5 are used to regulate the floating positive/negative 18V rails.

D27 to D30 act in a voltage trebler circuit from the earthy +5V winding to give a nominal −18V on P5. This rail supplies the keep-alive electrode of the display tubes.

The anodes of the display elements are fed with +180V, output on P4.

Note that terminal 17 of transformer T2 is at Guard potential and should NOT be connected to 0V, nor to Supply Earth.

WARNING – FLOATING SUPPLIES

For safety always use an isolating transformer.

← Diag. 6.13

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DIGITAL

This part of section 6 covers those circuits which convert the pulses generated in the A/D converter into a digital count, which after further processing is used to drive the display.

The Block Schematic Diagram (Diag 6.14) illustrates the functional layout of the digital section, which for convenience, can be considered as having 3 sub-sections:

1) **Counters and Memory (Diag 6.15, 6.16)**
2) **The Control Logic (Diag 6.17, 6.18)**
3) **The Display, Display Drive and Phase Locked clock (Diag 6.19, 6.20).**

COUNTERS AND MEMORY

This sub-section is illustrated on two sheets, Diag 6.15 and 6.16, and comprises the counter chain with its associated input circuits, the data transfer Multiplexer and the Random Access Memory (RAM) including the necessary Read/Write logic. The Timing Counter, together with the organisational logic associated with the formatting of the geographical display is shown on Diag 6.16.

THE CONTROL LOGIC

This board controls the other logic boards and the floating circuitry. Shown on Diag 6.17 are the Main Control, the Range Control logic and Self Control logic circuits, the "State" Counter and its decoder.

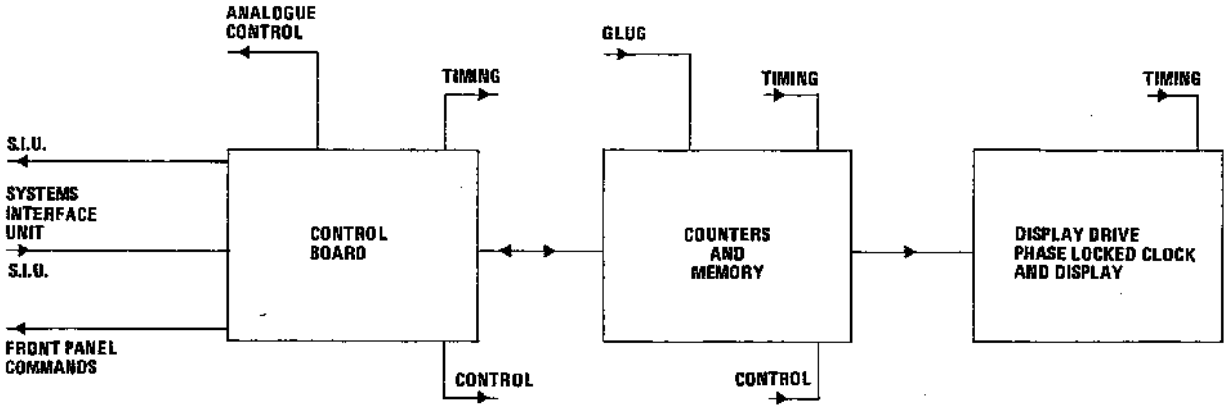
On Diag 6.18 are the Opto-Couplers, Autorange circuits and Display Flashing logic.

THE DISPLAY, DISPLAY DRIVE AND PHASE LOCKED CLOCK

The Display Drive and Phase Locked Clock are illustrated on Diag 6.19. In this sub-section the BCD information is decoded and presented to the display, which has 12 decade windows to enable the visual information to be positioned correctly relative to the fixed decimal point Diag 6.20.

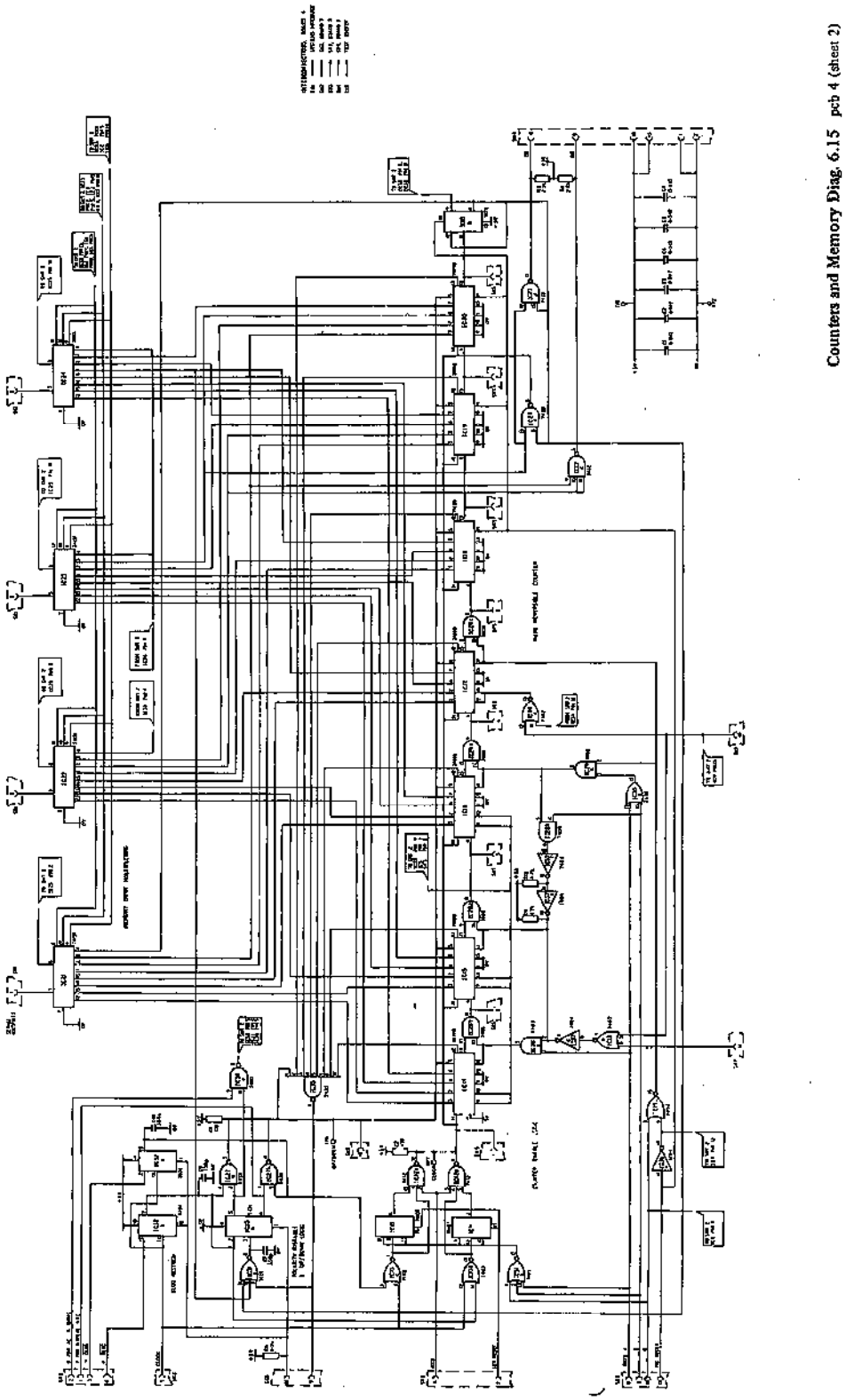
Diag. 6.14 ——▶

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Block Schematic Diag. 6.14

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Counters and Memory Diag. 6.15 pcb 4 (sheet 2)

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COUNTERS AND MEMORY

GLUG RESYNCH (Diag 6.15)

The output from the A/D converter is a pulse train pair. The pulse trains are labelled + GLUG and -- GLUG, and are transferred from the floating circuits via optical couplers. To restore synchronization the signals are gated with Clock in the dual flip-flop IC32. The input to pins 1 and 13 is for test purposes only.

COUNTER ENABLE LOGIC

Provided Main Counter Enable (MCE) SK2 pin 6 is present the resynchronized $\overline{+GLUG}$, $\overline{-GLUG}$ signals are permitted to gate Clock pulses through IC13, IC12 into the counter chain. The indirect path for each half of IC13, via IC11, provides the ÷ 2 function necessary when the instrument is operating at 20ms (4 x 9's) integration time. IC31b inputs all low.

POLARITY BISTABLE & UP/DOWN LOGIC

The direction of count is governed by two factors. Essentially $\overline{+GLUG}$ will drive the counter in one direction, $\overline{-GLUG}$ causing the count to reverse. However, if at any time the counter content is being decremented through zero, gate IC35 will detect underflow and force a reversal via IC31a and IC10a. Thus the effect of the GLUG-lines on pin 5 of each counter element is reversed. The labelled polarity of the inputs at SK2 Pins 3 and 4 is not in itself significant to the direction of count, the counter content at all times being the modulus of the input value irrespective of sign. The need for a minus sign is detected by IC38 Pin 10, and depends on the final state of IC10a. The gate is inhibited in the AC or OHMS mode. The input on SK2 pin 14 blanks decades 6 and 7 (see Fig. 6.1) during STAT period when AC is selected. (Maximum AC mode displayed scale length is 5 x 9's).

MAIN REVERSIBLE COUNTER

IC14 to IC20 plus IC10b form the 7½ decade counter chain, IC20 being the most significant "9" while IC10b can only assume a 1 or 0. The counter operates in BCD, pin 13 of each element providing the "ripple" enable to the next decade. Elements IC17, 16, 15 and 14 are capable of being held at zero by the Rate lines (SK2 Pins 8, 9 and 10) when low, so that unwanted decades are inhibited for the shorter scale lengths. Main Counter Reset ($\overline{MCR}$) generated by the Process Control circuits, provides the zero resetting on pin 11 of the counter elements at the end of each conversion.

SCALE LENGTH

For operation as a 7 x 9's instrument the complete counter is used. The coded inputs on SK2 pins 8, 9 and 10 are decoded to provide progressive inhibition of the least significant decades as the Integration time is changed. (Pin 11 set low on each IC in turn). This is illustrated in the following table:-

RATE	SCALE LENGTH	COUNTER ELEMENTS INHIBITED
10s	7 x 9's	–
1s	6 x 9's	IC14
100ms	5 x 9's	IC14, IC15
20ms	4 x 9's	IC14, IC15, IC16
1ms	3 x 9's	IC14, IC15, IC16, IC17

← Diag. 6.15

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MEMORY INPUT MULTIPLEXING

Parallel to Serial Conversion is performed by IC's 21 to 24 inclusive. The outputs on Pin 6 of each being determined by the state of the select lines feeding pins 9, 10 and 11 of each converter element. The counter content is fed in serial BCD form to the data selector (IC25) on Diag 6.16

DATA SELECTOR (Diag 6.16)

IC25 a 4 x 2 line-to-1 line data selector completes the multiplexing of the Counter data into the Random Access Memory (RAM).

Control of the selector is the clock ÷ 128 output from IC2 which when low selects the counter data and when high selects the organisational data. Memory load addresses are generated by the range counter code from pcb3, fed in on SK3 pins 9, 10, 11 and 12 via IC5 when STAT is high (SK3 pin 5). The output from IC33 pin 8 determines the operation of the "RAM". When low, memory load occurs. When high, Read is selected. The 16 load pulses (during STAT) are derived from the timing counter and phased with the 16 selected input words.

DISPLAY SECONDARY ORGANISATION

The function of these elements (IC's 29, 30, 31, 33, 34, 36 and 38) is to test for certain conditions which determine what type of secondary display is necessary.

The conditions tested are:-

1) Address of word to be loaded - display digit.

2) The presence or absence of a 1 as the most significant measurement digit.

3) The operation on 3 x 9's scale length (10mΩ range) – trailing zero restoration.

4) The need for a minus sign.

5) The need for extra leading zeros in certain cases – low ranges.

6) Autorange mode – affects leading zero blanking and minus sign.

The display calls for the generation of 16 words of data, of which 12 are actually visible display information. The words are presented in two groups of 8, the first group being derived from the counter chain BCD data. The second, being generated from the Display Secondary Organisation, fills in the gaps, as it were generating all the necessary blanks and extra zero's required and in some instances, a minus sign. For convenience in the explanatory text which follows, the display windows are identified by the numbers 0 to 11, reading from left to right.

DISPLAY WINDOWS

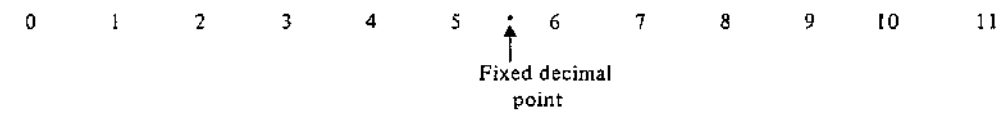


Fig 6.1

MINUS SIGN

The need for a minus sign is detected in the Polarity Bistable on Diag 6.15 . This is applied as a low on pin 5 of IC34 (Diag 6.16) . The second input to IC34 will be low if IC33b inputs are all high, i.e. Autorange is true, the msd of the measurement data is a zero and the word being scanned is not that for display windows 5, 6 or 7. This would normally generate a 'blank required' signal on IC36 pin 4, but the presence of a 'minus sign required' signal on IC34 pin 4 will override the blank. This also determines whether a zero, blank or -ve sign is displayed before the most significant 9.

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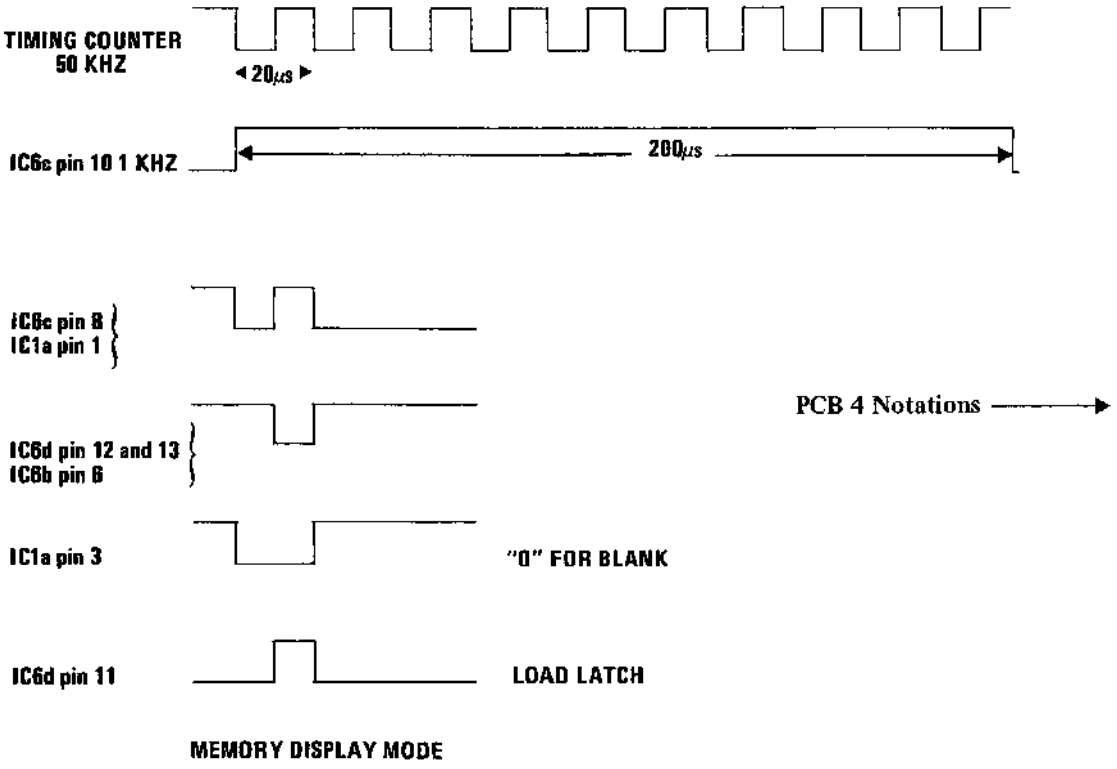
If the m.s.d. of the measurement data is not zero but 1, the minus sign for a negative quantity is normally needed one place further left than the previously described case. The element involved is IC29b whose output will be high. Additionally the memory address being loaded is address 7 i.e. the last to be loaded of secondary organisation. The high on pin 6 of IC29b will set IC25 output pins all low, which will cause the memory to output 1.1.1.1., which is the minus sign code.

There is a further special case requiring a secondary organisation minus sign, necessitated by the convention of preceding a fractional number with a zero before the decimal point. The display organisation normally inserts a minus sign before the m.s.d. of the displayed value, which for the 100mV and 10mV ranges would be position 5 or 6. Since this would result in, for example, (on the 100mV range), a display of "−.414", it is necessary to force a zero into position 5 and re-insert the minus sign in position 4. IC38 pin 3 goes low when position 4 word is being scanned enabling IC30 pin 4 to allow a minus sign if required, to force IC25 pin 6 to a low. Similar logic determines the position of Blanks in the display entered by the inverted codes on IC25 pins 13 and 10.

When the instrument is operating on the 10MΩ range at the 3 x 9's scale length, the input on IC34d pin 11 in conjunction with STAT from pcb 3 forces IC17 to register a zero for display in the decade window immediately preceding the decimal point i.e. position 5.

MEMORY DISPLAY MODE

The data previously loaded into memory are output to the display circuits under the control of the display scanner (IC1). The timing counter 50kHz output is gated via IC6b (pin 6) with a 1kHz pulse train, both pulse trains derived from the timing counter divider stages, the resulting gate pulse on IC6c pin 8 is used to enable the scanner (the address lines being pins 3, 4, 5, 6) accessing the two "words" needed for the digit pair to be displayed. The scan is such that no two digit pairs are ever addressed in sequence (bits 8 and 2 being transposed for this purpose)
IC6d pin 11, the inverse of IC6b pin 6 is used as a load latch for the righthand digits in the display drive circuit. When they are being latched, the selected display element pair is blanked by the low on IC1a pin 3 via SK3 pin 8.



MEMORY DISPLAY MODE

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PCB 4 Notations

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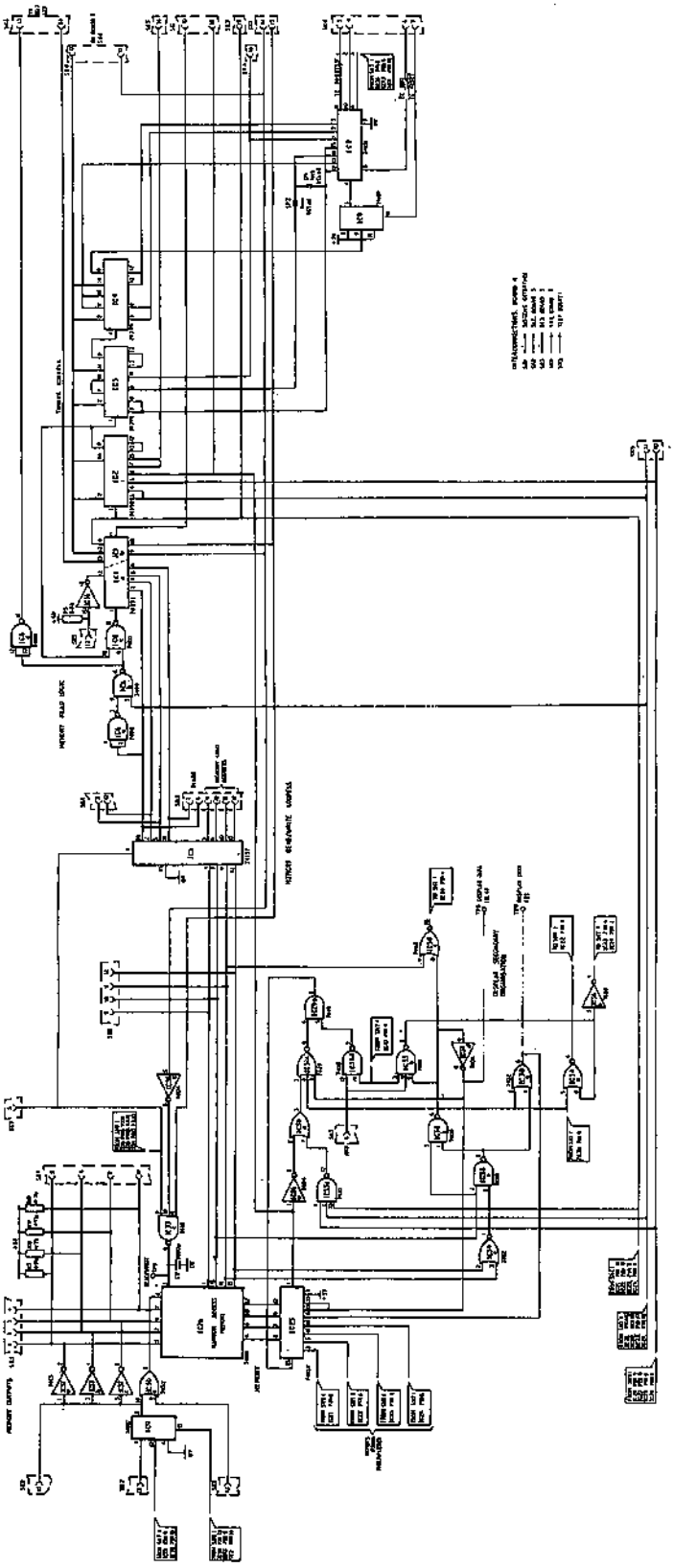






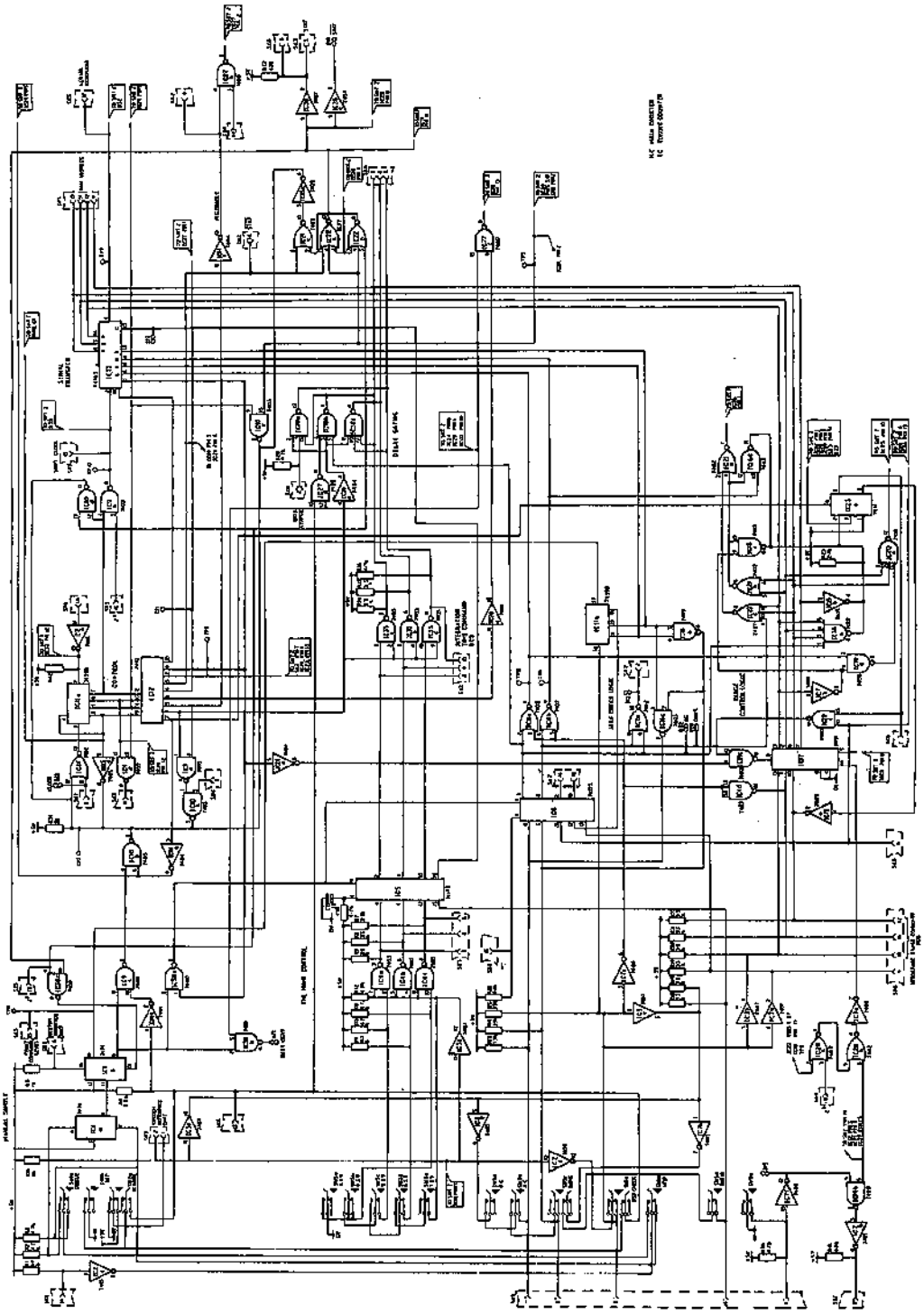


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Counters and Memory Diag. 6.16 pcb 4 (sheet 1)

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Control Board Diag. 6.17 pcb 3 (sheet 1)

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CONTROL LOGIC (Diag. 6.17, 6.18)

IC11a is the "state" counter, decoded into the 10 states by IC12. At anytime one of the10 outputs of IC12 will be low.

The states, advanced by a low at TP7 synchronously with the 1.6MHz clock are tabulated below, and described in sequence, starting at state ⑤ , the state that accepts a digitise command.

7075 CONTROL SEQUENCE

CODE		ACTION	IC12 PIN No.	TERMINATED BY
6	0110	HOLD – waits for Dig Command unless "not-in-Remote", overload or in Rep.	7	(i) CLOCK (in Rep) (ii) Overload (on Autorange) (iii) Dig Command
7	0111	LOAD – Integration & Mode latches. Range counter if not in Autorange serial transfer Shift Register	9	CLOCK
8	1000	SERIAL TRANSFER (Floating & Fan-out)	10	TIMING COUNTER
9	1001	(Not Used)	11	CLOCK
0	0000	DELAY PERIOD before Measurement Start	1	TIMING COUNTER
1	0001	RESET Autorange ccts & ÷ 2 bistable on Bd. 4	2	CLOCK
2	0010	MEASUREMENT PERIOD	3	TIMING COUNTER
3	0011	PULSE BEFORE STAT – Samples down-range system	4	CLOCK
4	0100	STAT – Memory Write Sequence Resets Dig Command & Print Command Autorange counter reset	5	TIMING COUNTER OR CLOCK (if autoranging)
5	0101	PULSE AFTER STAT – resets Main Counter resets "O/L during HOLD" bistable	6	CLOCK

OPERATION

State ⑤

State ⑥ enables IC10b pin 5. IC10b pin 4 will go high, putting a low on TP7 to advance control for a low on either IC9d pin 9 or 10. If in "REP" IC14a pin 1 will be high making IC9c pin 10 low and control will advance to state ⑦ on next clock. If in "SINGLE" sample IC14a pin 1 will be low. The system is therefore waiting for a low on IC1b pin 8 from either a remotely commanded digitise command on IC1b pin 10 or a front panel command via the anti-bounce latch IC1a from the single sample switch.

State ⑥ can also be advanced by an overload signal via IC10c – see autorange system.
State ⑤ resets range error bistable IC23a.

◀——— Diag. 6.17

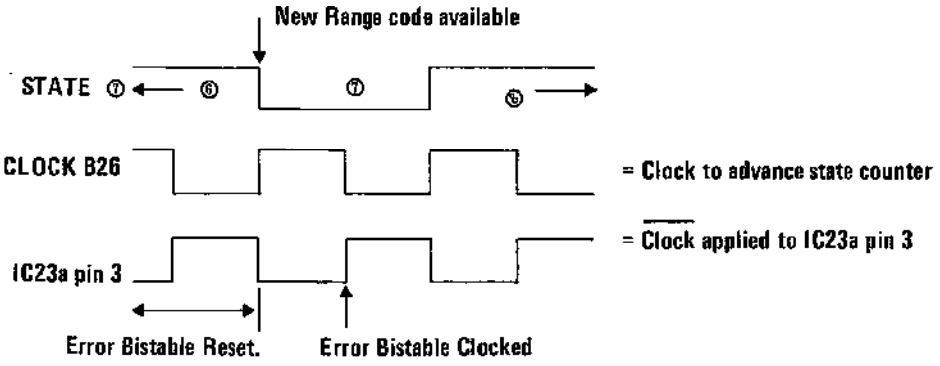
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State ⑦

Integration and Mode latches (IC5 and IC6) are loaded. If in remote these latches are already loaded via IC38a pin 2.

IC17 the range counter is loaded via IC19c pin 9 if IC19d pin 12 or IC19d pin 13 is low. IC19d pin 12 will be low if not in Autorange. IC19d pin 13 will be low if the error bistable detects an incorrect range code, putting a low on IC23a pin 5 when clocked, which corrects and resets the range counter.

When state ⑦ ends the shift register IC13 will be loaded (IC13 pin 1) with the final range and mode information. As it is an odd state (IC11a pin 3 = high) it is terminated by clock via IC15d holding TP7 low. Also it will have reset the Timing Counter via IC7d, e, and the measurement counter via IC9d.

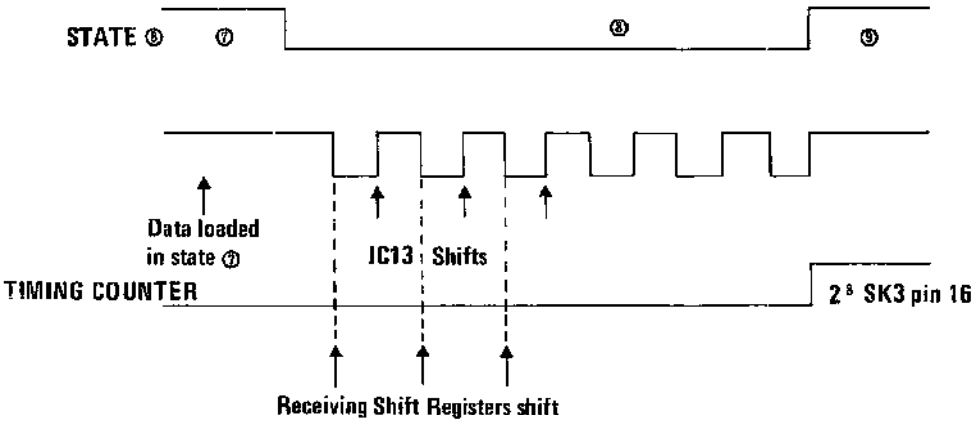


State ⑧

IC13 is now ready to transfer its information to the floating logic on board 6 via the opto-couplers IC30 and IC31 and to the systems interface unit (S.I.U.) if fitted.

IC11 pin 7 is high enabling IC9b to pass strobe pulses on SK3 pin 15 (from the 4TH output) down the timing counter chain (2^4) to the clock input; to the shift registers IC13; via SK5 pin 13 to the receiving shift register in the S.I.U. and via opto-coupler IC31 to the floating logic. IC13 pin 2 is enabled by IC12 pin 10 being at a low, and shifts on the positive edges. The receiving shift registers are arranged to shift on the negative edges to allow for data settling time.

This state is terminated by a high from the 8th output of the timing counter arriving at SK3 pin 16 enabling gate IC10d, (already enabled by IC11a pin 7), putting a low on TP7 to advance IC11a on the next clock edge.



CONTROL BOARD WAVEFORMS

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State ⑨

State ⑨ is not used, clocked to state ⓪ as it is an odd state.

State ⓪

This state lasts for the time needed for analogue settling before a measurement starts. The required delays are normally 20ms unless:-

1) SIU determines no command changes since the last measurement, in which case it puts a low on IC18a pin 1 requesting a 4ms delay only.

2) AC mode and Single measurements or Autorange change – 800ms delay.

Operation 2) has priority over 1).

IC35a, b and c is disabled by state ⑧ (IC12 pin 1 low). Codes set up on SK4 pins 3, 4 and 5 by IC18a, b and c and IC27a address the output of the Timing Counter, which will go high after the required delay. This is applied to SK4 pin 6 which enables gate IC10a already set up by state ⑧ to put a low on TP7 to advance IC11a.

Codes to Timing Counter:-

	SK4/ 3	4	5
20ms	1	1	0
800ms	0	1	1
4ms	1	0	1

State ①

Resets autorange bistables IC24a, IC23b
Resets ÷ 2 bistable for 4 x 9's rate.
Resets Timing Counter via IC7d and e.
Terminated by clock as odd state.

State ②

This is the measurement period. The code for the required integration time is held in IC5 and applied to the timing counter via IC35a, b, c and SK4 pins 3, 4 and 5.

The Codes are:-

	SK4/ 3	4	5
1ms (3 x 9's)	1	1	1
20ms (4 x 9's)	1	1	0
100ms (5 x 9's)	0	1	0
1s (6 x 9's)	1	0	0
10s (7 x 9's)	0	0	0

Similar codes on SK2 pins 8, 9 and 10 select the required measurement counter length. The codes are either encoded from the front panel switches SW3a to SW3e or from the S.I.U. via SK5 pins 3, 4 and 5. In the latter case IC4 a. b. and c. are disabled by SK5 pin 2 via IC3f.

This state will be terminated by either:-

1) The "time-up" signal on SK4 pin 6 from the timing counter. IC10a enabled by state ② via IC9a
or
2) By an autorange decision via IC10c enabled by state ② or ⑥ by IC11a pin 5. (See Autoranging).

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State ③

This is an odd state and so if resets the timing counter ready for state ④ . It also samples the autoranging system for a "slow-down" range decision in case this has not already been made during state ② (see autoranging).

State ④

Memory is loaded with display data measurement and status information during state ④ and the same data is sent to the S.I.U. via SK1 pins 5, 6, 7 and 8. It is normally terminated by the timing counter 8th output on SK3 pin 16 via IC22b, IC21c and IC15c, putting a low on TP7 to advance IC11a on the next clock edge.

It may be by-passed by the autoranging system placing a high on IC22b pin 4 which will inhibit STAT on IC22a pin 12 and advance IC11a immediately on the next clock pulse.

STAT normally lasts for 80μs during which time there are 16 pulses on SK4 pin 10, the 2nd output of the timing counter. These, clock the binary counter through its 16 states, starting and finishing on the same range code. The range counter is reversible and the direction is determined by IC17 pin 5. This is held low (count up) by IC28c pin 10 since IC28c pin 8, is high (STAT).

If state ④ is being by-passed by the autoranging system, IC28c pin 8 is held low by IC22a pin 1 at a high. Instead of 16 pulses there is now only one. IC28b pin 6 is low (IC12 pin 5 low in state ④). IC28a pin 2 is high and blocked, so as state ④ passes there is one pulse on IC28b pin 4 which is delivered to IC17 pin 14. This changes the range code. Clock input to IC17 while high during state ① ensures correct direction of count.

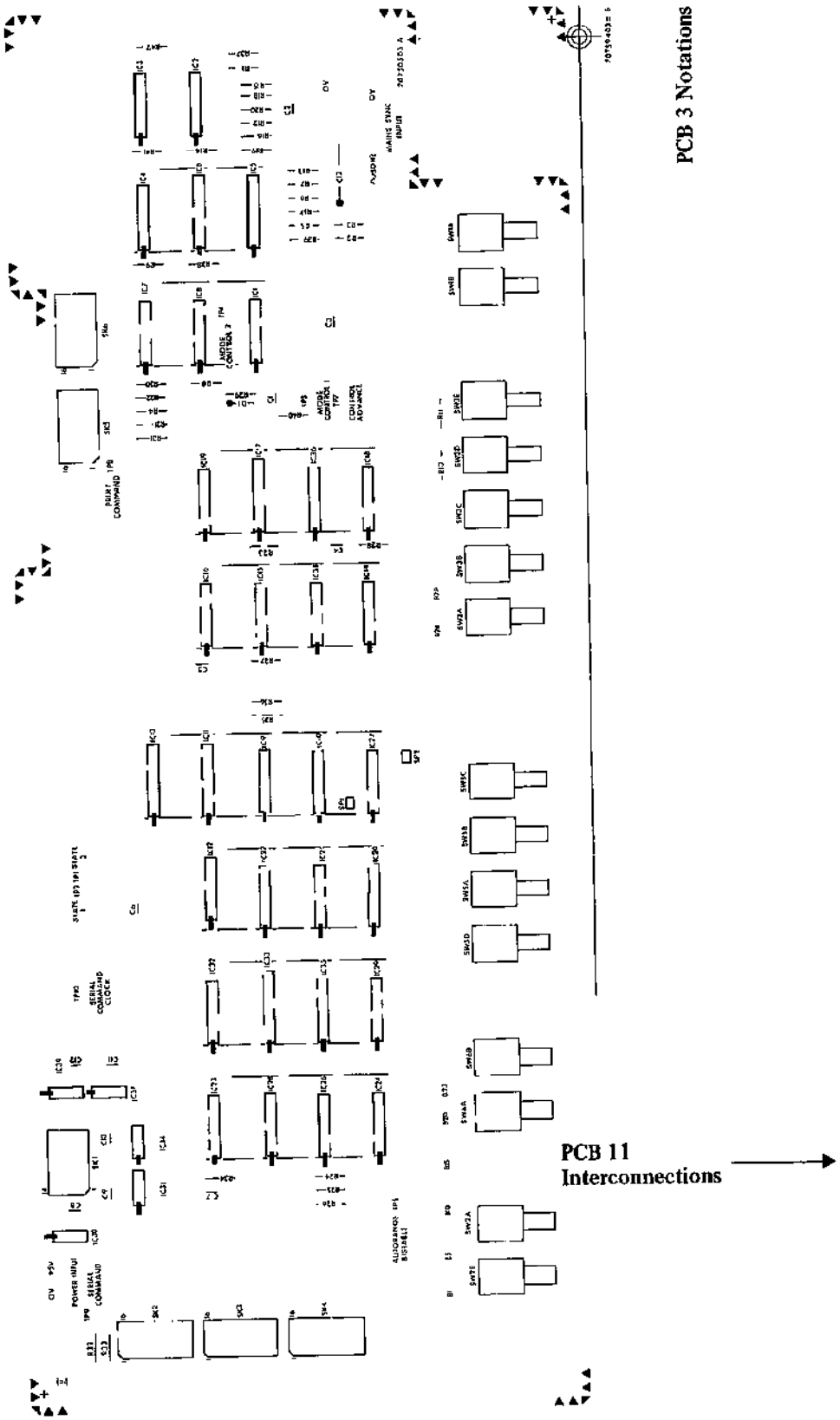
State ⑤

Resets measurement latch via IC9d.
Resets timing counter via IC7d and e.
Resets latch in autoranging system.
Terminated by clock (odd state).

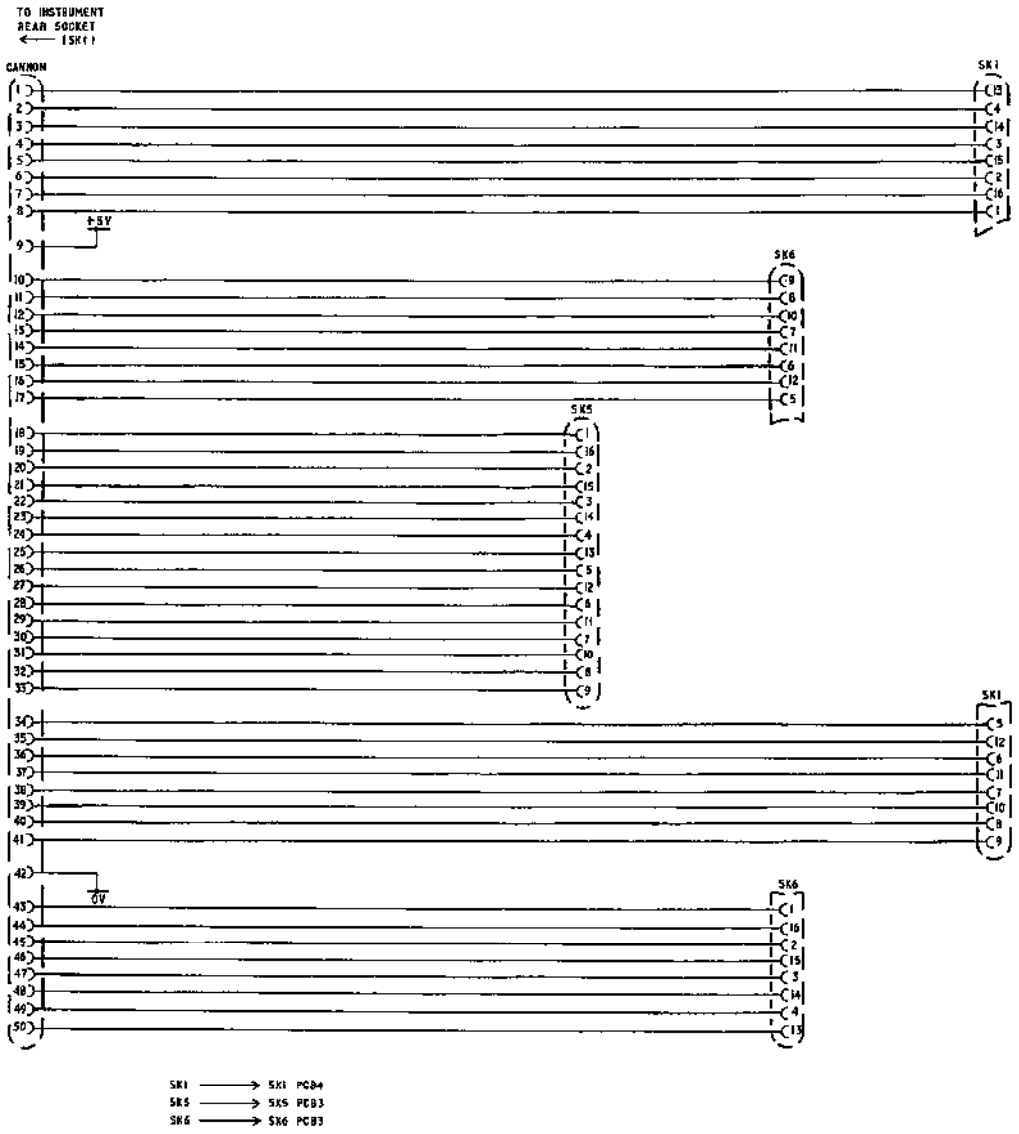
State ⑥

As before.

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DVM TO S.I.U. INTERCONNECTION BOARD

PCB 11 Interconnections

PJL/7075/3

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AUTORANGING SYSTEM

IC32a, 33a and 33b are the autorange counters. Should the presence of either GLUG (IC38 pin 13 or 12 low) occur during state ⑦ and state ⑤ IC11a pin 5 gates IC29c pin 9 enabling the autorange counters. They are reset at all other times.

During a GLUG there will be at least one transition of output (IC33a pin 9) if the GLUG is larger than the size of GLUG corresponding to the down range point.

For a steady DC input voltage to the analogue system there will be at least one GLUG larger than the critical size if the input value is greater than the down range value. This incident will clock IC23b and prevent a down range decision (see later).

Similarly for an input greater than the up range value, there will be at least one transition of output IC33b pin 11 with IC33a pin 9. This will pass through IC35d, IC26 pins 3 and 4 and IC36b pin 12 to clock IC24a, the main autorange bistable. In both cases the information is OR-ed with information from the measurement counter on board 4. Should the measurement count exceed the up range value SK4 pin 8 will go low at least once. Should the measurement count exceed the down range value SK4 pin 9 will go low at least once.

The system will therefore up-range if:-

1) Any GLUG exceeds the size equivalent to that obtained with a steady input equal to the up range value.

2) The top range for the mode has not been reached.

3) Autorange is enabled.

The system will down-range if:-

1) During the measurement or the first 20ms there are no GLUGS greater than those obtained by a steady input at the down-range point.

2) It is not already on the bottom range.

3) It is in the autorange mode.

IC24a and IC23b (the autorange and down range bistables) are reset before a measurement starts on state ① . If during a measurement, the main reversible counter output or a GLUG greater than the down range value occurs, IC15e pin 10 will go low. This will clock IC23b to prevent down ranging on the next clock IC29a pin 2, if IC24a is not already set (IC29c pin 9). If on the bottom range IC23b will be set anyway (IC23b pin 10).

The down-range bistable will be sampled by either the 20ms output from the timing counter IC26b pin 6, or state ③ (IC27a pin 1), by IC20b pin 3 to set the main bistable IC24a if autorange is true (IC20b pin 4) to start an autoranging sequence. IC24a will terminate state ② or state ⑤ if not already finished, inhibit state ① , and increment the range counter by one during the passing of state ① in the direction determined by IC28c pin 10. As STAT is inhibited (IC28c pin 8) the direction will be determined by whether IC23b had been clocked or not (i.e. if not clocked – down range).

An overload signal from the GLUG counter or the main counter will clock IC24a directly (providing IC23b had already been clocked up-range). State ② and ⑤ will be terminated immediately. To do this Autorange must be true (IC36b pin 13) and the top range must not have been reached (IC26a pin 1).

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If an overload occurs while in state ⑥ and the system is not in remote, the main autorange bistable (IC24a) will terminate state ⑥ (subject to the usual conditions. i.e. Autorange must be true and not on the top range) and start a measurement cycle. A normal upranging sequence will follow. IC24b inhibits STAT and Print Command until the autoranging is complete. It is reset on state ⑤ if the main autorange bistable is reset.

IC27c on pcb 4 detects a count of "14" which is the range overload point, the output on SK4 pin 8 causing up-range to be actioned on pcb 3. The other output (IC27c pin 8) locks-out the clock at full scale "freezing" the counter action.

IC12c also on pcb 4 detects the "12" condition producing down-range at SK4 pin 9. Down range automatically occurs every conversion or 20ms after conversion start whichever is the shorter time, unless during that time it is inhibited by the output from IC12c.

FLASHING LOGIC

Under normal conditions IC29e and IC20c latch is reset. IC29e pin 13 detects analogue overload, IC29e, and IC20c latch. IC32b pin 8 produces a 12.5Hz pulse train which resets the latch while low causing the display to "flash" for as long as the overload persists.

To prevent flashing during auto/normal range change, a low is applied via IC20c pin 10.

To ensure that invalid readings are not displayed during memory update, a blanking pulse is applied to B16 which inhibits IC12 and IC11.

SELF CHECK LOGIC

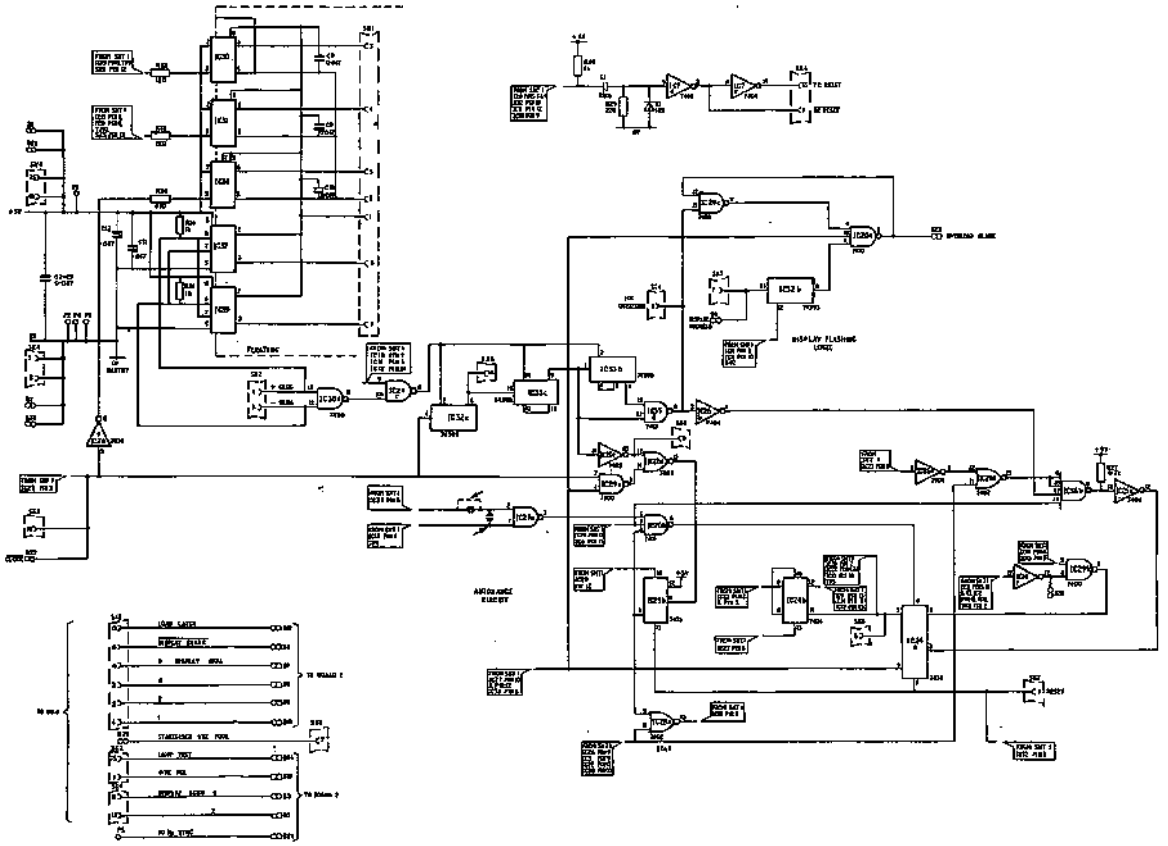
In the instrument self check mode, the OHMS, AC and DC front panel switches are disabled (IC2f, IC2c and IC3e). Autorange is also disabled via IC3a. IC17 is set via IC3b, by range code 0 1 1. S.I.U. and fan-out are informed from IC8a pin 1 and IC8b pin 4 via IC13 pins 5 and 6. Self check codes are also sent via IC13 pin 11 and 12. The appropriate self check codes are then formed for each test.

The information displayed during the self check of the instrument through its 5 sequential steps is given in section 2.

PCB 11

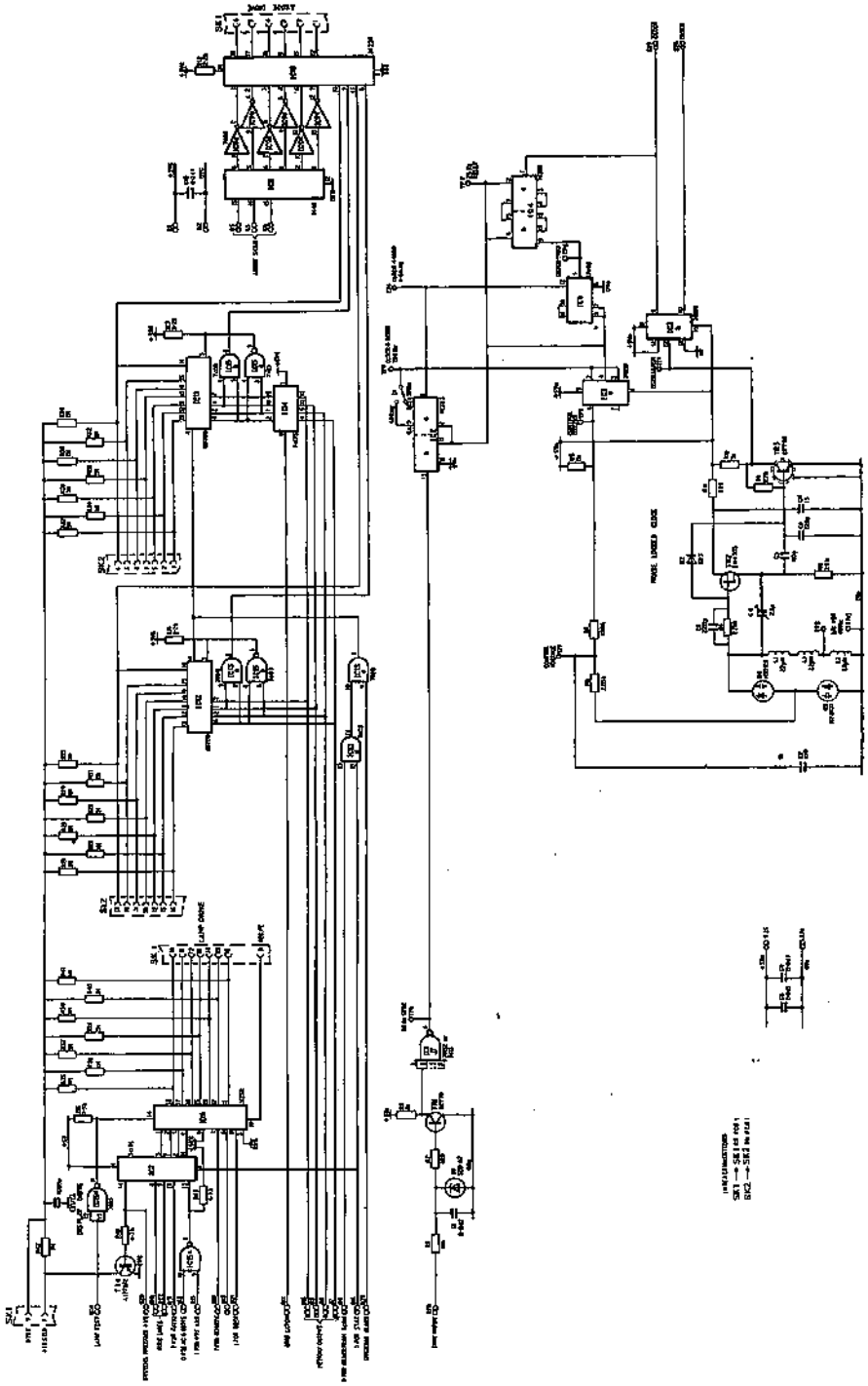
Enables the rear panel socket SK1 for instrument use with ATE in a systems environment.

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Control Board Diag. 6.18 pcb 3 (sheet 2)

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Display Drive and Phase Locked Clock Diag. 6.19 pcb 2

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THE DISPLAY, DISPLAY DRIVE AND PHASE LOCKED CLOCK

PHASE LOCKED CLOCK (Diag 6.19)

A mains derived synchronising signal is shaped by R_1, C_1, D_1, and buffered by TR1 before being applied to IC1. The output from this gate is a repeatable, free from bounce, 50Hz signal but possibly of unequal mark-space ratio. IC2 divides this signal by 2 giving a 25Hz output (TP2) with an equal mark-space ratio.

The voltage controlled clock oscillator is phase locked to the mains frequency. Voltage to frequency adjustment is achieved by C4. For 50Hz operation with a control voltage of 2.2V, frequency should be 3.2 MHz. For 60Hz (TP8 connected to TP10) operation and a control voltage of 2.2V, frequency should be 3.84MHz. Frequency control is by varactor diodes D4 and D5.

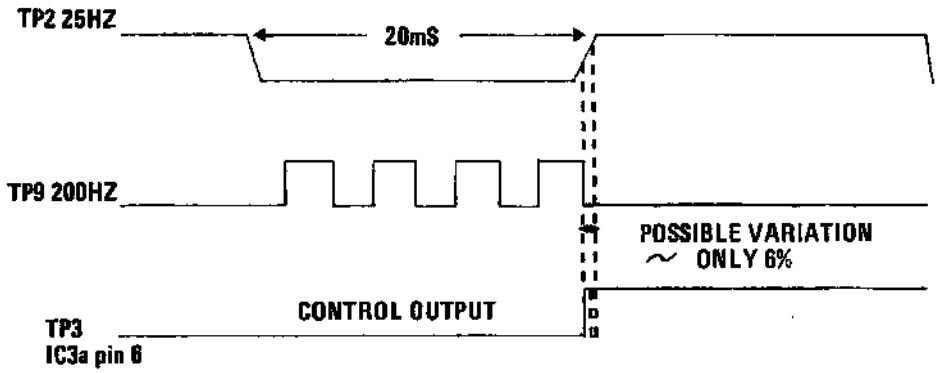
TR3 acts as a buffer, its output (TP1) is applied to the counter chain, the final output of which is 200Hz.

OPERATION

When the level of the synchronising signal (TP2) is high, the counter is held in reset; when it goes low, the chain is enabled. As it returns to the high state, IC3a is clocked and the state of the final 200Hz output is stored until the next cycle. Should the final 200Hz output be high at this instant, the clock is running too slow. Should it be low, the clock is running too fast.

A high on the control voltage tends to reduce the capacitance of D4 and D5 thereby increasing the clock frequency and vice versa. Because the possible error in frequency is 6% maximum, there is no likelihood of sampling the wrong output pulse.

The control voltage is averaged and smoothed by R7, C2 so that a gradual control is achieved. In lock the decision tends to alternate on consecutive samples giving a small slow ramping of the clock frequency. The effect of one decision is arranged to be very small, therefore the extent of the final jitter is also very small.



PHASE LOCKED CLOCK

← Diag. 6.19

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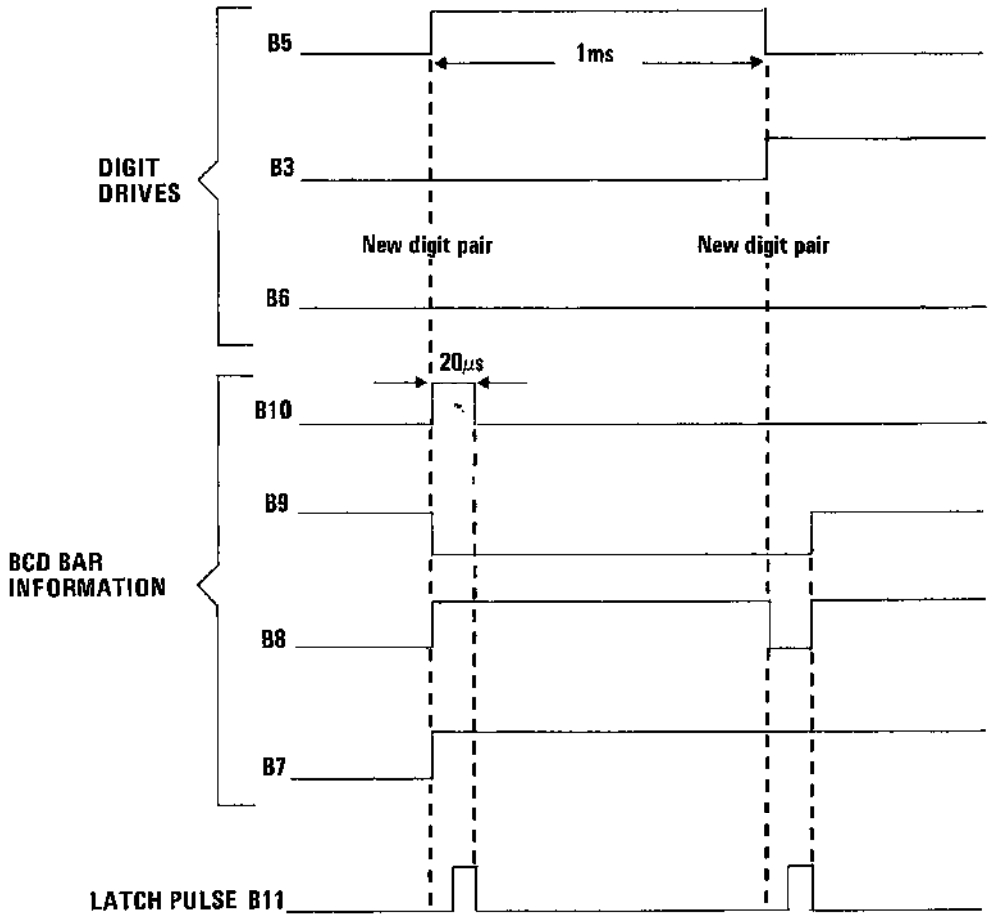
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THE DISPLAY DRIVE

The display is multiplexed, two digits at a time on a 1 in 8 duty cycle. Digit pairs are selected by the BCD information on B5, B3 and B6, decoded by IC8 and level shifted by IC10 to the anode switches on the display board.

For each new digit pair addressed, two sets of 7 bar information are required. These appear, in BCD, on B10, B9, B8 and B7. One set of information is applied for 20μs and stored in IC14, gated by a latch pulse on B11, thence decoded by IC11, IC13b and IC15a (special codes) to drive the left hand digits.

The second set of information is applied for the remainder of the multiplex period, decoded by IC12, IC13a and IC15b driving the right hand digits.



DISPLAY DRIVE WAVEFORMS

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The BCD codes are:-

Character	BCD	
0 TO 9	0 TO 9	
A	1 0 1 0	NOT USED
B	1 0 1 1	
BLANK	1 1 0 0	Generated by IC15a
	1 1 0 1	Generated by IC15b
NEGATIVE SIGN	1 1 1 0	Generated by IC13a
	1 1 1 1	Generated by IC13b

R13 and R14 program the current drive to the segments of the display. R21 to R34 clamp the unlit segments to the 75V rail.

When the information for the left hand digit is being accessed, the selected display element pair is blanked by a low applied to B4 which inhibits IC12 and IC11 for 20μs.

ANNUNCIATOR DRIVES

Information for the annunciators appears on B20, 18, 22, 17, 12, 13, 19, 15 and 21. Some lines are latched in IC7 before being applied to IC16 (level shifter). R15 programs the current drive to all the neon annunciators. A high input on B14 removes this program current and blanks the annunciators on lamp test.

Unlit annunciators are clamped to the 75V rail by R35 to R41 to ensure that leakage currents do not cause faint discharges.

THE DISPLAY (Diag 6.20)

An 11 x 9's display is used to facilitate a 7 x 9's scale length in conjunction with the fixed decimal point.

The display decades are 7 bar co-planar gas discharge type.

ANNUNCIATOR DISPLAY

V5 to V10 provide the following annunciator displays:- VOLTS, kΩ, BUSY, REMOTE, RATIO and AC.

The travelling minus sign is derived from the centre segment of each display element, the positive annunciator is not used.

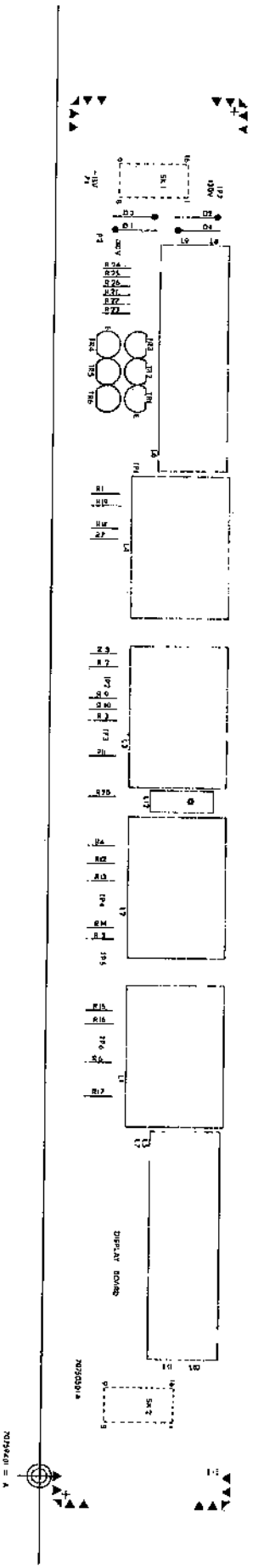
The VOLTS, kΩ, REMOTE, RATIO and AC annunciators are illuminated on selection of the appropriate function or control button.

The BUSY annunicator is illuminated during range change and on overload. When this occurs, the readings should be regarded as invalid. The annunciator is extinguished when the new range is settled upon, when the new result is displayed, and/or when the overload is removed.

The BUSY signal has the additional function of inhibiting the front panel push buttons, thus once a command has initiated a measurement, the instrument will not abort that reading.

PCB 1 Notations ⟶

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PCB 1 Notations

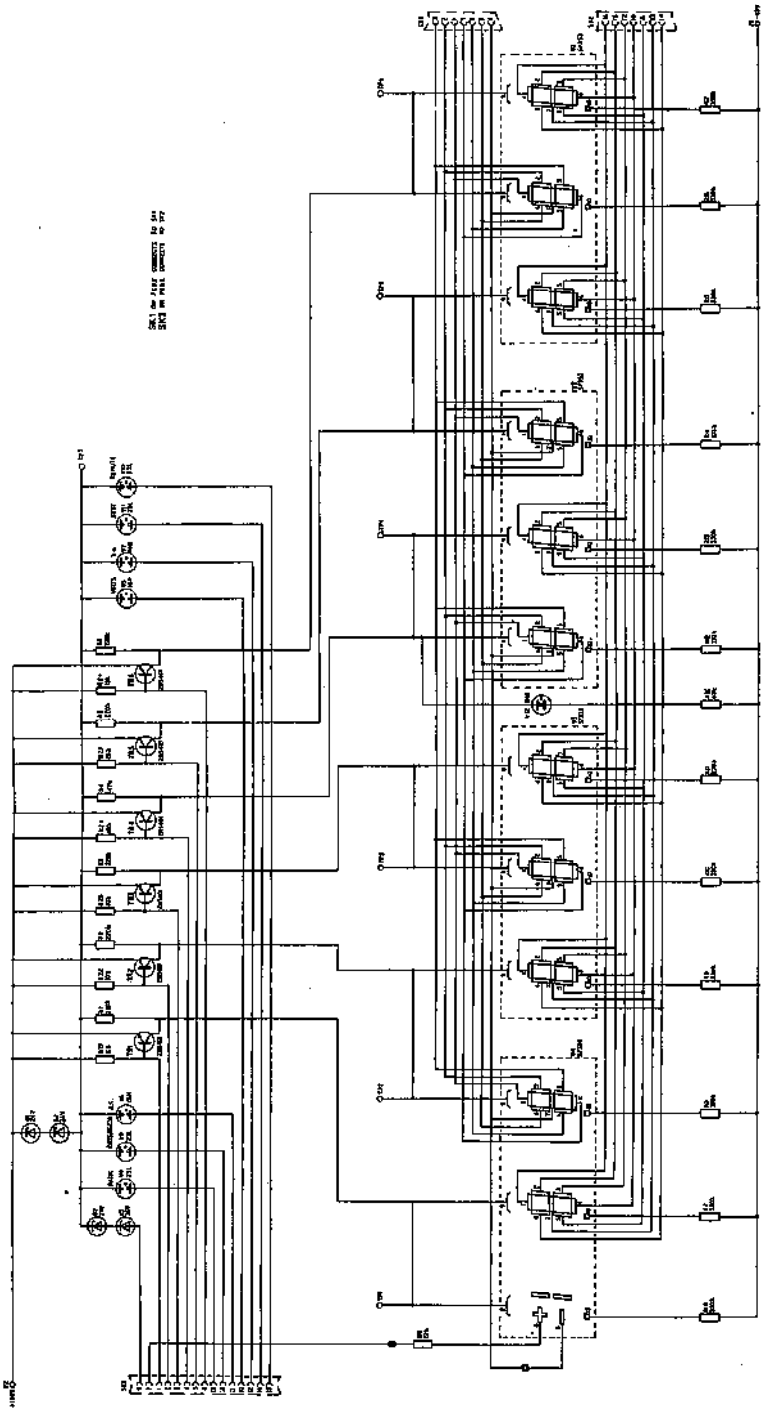
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Display Diag, 6.20 pcb 1



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SECTION 7 Parts List

This section contains detailed parts lists for each of the printed circuit boards fitted in the instrument. When ordering spare parts, it is essential to quote the instrument serial number, located on the rear panel, as well as the full description shown in the appropriate parts list.

COMPONENT PARTS LIST ABBREVIATIONS

CIRCUIT REFERENCES

AE	Aerial
B	Battery
C	Capacitor (μF)
CSR	Thyristor
D	Diode
FS	Fuse
IC	Integrated Circuit
L	Inductor
LP	Lamp (including Neon)
LK	Link
M	Motor
ME	Meter
MSP	Mains Selector Panel
PL	Plug
R	Resistor (Ω)
RE	Recording Instrument
RL	Relay
S	Switch
SK	Socket
T	Transformer
TP	Terminal Post (or Test Point)
TR	Transistor
V	Valve
X	Other Components

Also Used:-

RNL	Non Linear Resistor (Ω)
RV	Variable Resistor (Ω)

COMPONENT TYPES

Fixed Resistors		Variable Resistors		Capacitors	
Carbon Composition	CACP	Carbon Front Panel Multiturn	CAFM	Air	AIR
Carbon Film	CAFM	Carbon Front Panel Single Turn	CAFS	Aluminium Electrolytic	ALME
Cracked Carbon	CKCA	Carbon Preset Multiturn	CAPM	Aluminium Solid	ALMS
Metal Film	MEFM	Carbon Preset Single Turn	CAPS	Polycarbonate	CARB
Metal Oxide	MEOX	Cermet Front Panel Multiturn	CMFM	Ceramic	CERM
Power Wirewound	POWW	Cermet Front Panel Single Turn	CMFS	Polyester Foil	ESTF
Precision Wirewound	PRWW	Cermet Preset Multiturn	CMPM	Polyester Metallised	ESTM
Temperature Sensitive	TEMP	Cermet Preset Single Turn	CMPS	Glass	GLAS
Thick Film	TKFM	Wirewound Front Panel Multiturn	WWFM	Mica	MICA
Thin Film	TNFM	Wirewound Front Panel Single Turn	WWFS	Metallised Lacquer	MLAC
Voltage Sensitive	VOLT	Wirewound Preset Multiturn	WWPM	Paper Foil	PAPF
		Wirewound Preset Single Turn	WWPS	Paper Metallised	PAPM
				PTFE	PTFE
				Polypropylene Film	PYLN
				Polystyrene	STYR
				Tantalum Dry	TAND
				Tantalum Foil	TANF
				Tantalum Wet	TANW

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PCB 1

Cct. Ref.	General Description				Solartron Part No.
R1 to R3	CACP	220k	1/4W	10%	172052200
R4	CACP	47k	1/4W	10%	172044700
R5	CACP	220k	1/4W	10%	172052200
R6	CACP	220k	1/4W	10%	172052200
R7 to R18	CACP	330k	1/4W	10%	172053300
R19	CACP	22k	1/4W	10%	172042200
R20	CACP	68k	1/4W	10%	172046800
R21 to R26	CACP	10k	1/4W	10%	172041000
D1	Zener	24V	0.4W	5%	300523930
D2	Zener	24V	0.4W	5%	300523930
D3	Zener	30V	0.4W	5%	300521430
D4	Zener	24V	0.4W	5%	300523930
TR1 to TR6	2N5401				300555470
V1 to V3	Display SP353				300730280
V4	Display SP354				300730290
V5 to V7	Neon Hivac 16H				300720300
V8 to V11	Neon, Hivac 23L				300720240
V12	Neon Hivac 1MH				300720460
SK1	16 pin DIL				300584860
SK2	16 pin DIL				300584860

Cct. Ref.	General Description	Solartron Part No.
TR1	BCY70	300553590
TR2	2N4303	300553160
TR3	BFY90	300553890
TR4	MPS-A42	300555460
IC1	SN7413N	510000710
IC2	SN74393N	510002150
IC3	SN74109N	510002120
IC4	SN74390N	510002140
IC6	SN7490AN	510000260
IC7	SN74175N	510001310
IC8	SN7442N	510000330
IC9	SN7404N	510000410
IC10	DI258N	510002160
IC11	DD700	510001600
IC12	DD700	510001600
IC13	SN7408N	510000830
IC14	SN74175N	510001310
IC15	SN7403N	510001200
IC16	DI258N	510002160
TP1 to TP10	Disconnect pins	355900550
SK1	16 pin DIL	300584860
SK2	16 pin DIL	300584860
SK3	14 pin DIL	300584680
SK4	14 pin DIL	300584680
SK5 to SK7	16 pin DIL	300584860
SK8	18 pin DIL	300584850
SK9	18 pin DIL	300584850
B1 to B28	Horizontal amp	352501700
L1 to L3	Choke, R.F.	305020630
S1	DPDT	375000510

PCB 2

Cct. Ref.	General Description				Solartron Part No.
R1	CACP	10k	1/2W	10%	172341000
R2	CACP	47Ω	1/4W	10%	172024700
R3	CACP	1k	1/4W	10%	172031000
R4	CACP	220k	1/4W	10%	172052200
R5	CACP	1k	1/4W	10%	172031000
R6	CACP	220k	1/4W	10%	172052200
R7	CACP	680k	1/4W	10%	172056800
R8	CACP	2.7k	1/4W	10%	172032700
R9	CACP	82k	1/4W	10%	172048200
R10	CACP	1k	1/4W	10%	172031000
R11	CACP	220	1/4W	10%	172022200
R12	CACP	2.2k	1/4W	10%	172032200
R13	CACP	2.2k	1/4W	10%	172032200
R14	CACP	2.2k	1/4W	10%	172032200
R15	CACP	1.5k	1/4W	10%	172031500
R16	CACP	4.7k	1/4W	10%	172034700
R21 to R42	CACP	1M	1/4W	10%	172061000
R43	CACP	4.7k	1/4W	10%	172034700
C1	CERM	0.047	25V	+50% −25%	241944700
C2	TAND	100	10V	20%	265481000
C4	GLAS	2—24p	2000		290060020
C5	CERM	150p	500V	20%	241321500
C6	CERM	220p	500V	20%	241322200
C7	CERM	220p	500V	20%	241322200
C8 to C10	CERM	0.047	25V	+50% −25%	241944700
C11	TAND	15.0	20V	20%	265771500
C12	CERM	1000p	500V	20%	241331000
D1	Zener	4.7V	0.4W	5%	300521470
D2	SD3				300522160
D4	MV2107				300525020
D5	MV2107				300525020

PCB 3

Cct. Ref.	General Description				Solartron Part No.
R1 to R3	CACP	4.7k	1/4W	10%	172034700
R4 to R7	CACP	3.3k	1/4W	10%	172033300
R8	CACP	1k	1/4W	10%	172031000
R9 to R12	CACP	4.7k	1/4W	10%	172034700
R13 to R15	CACP	3.3k	1/4W	10%	172033300
R16	CACP	1k	1/4W	10%	172031000
R17 to R22	CACP	3.3k	1/4W	10%	172033300
R23	CACP	2.7k	1/4W	10%	172032700
R24	CACP	3.3k	1/4W	10%	172033300
R25	CACP	3.3k	1/4W	10%	172033300
R26 to R28	CACP	4.7k	1/4W	10%	172034700
R29	CACP	220	1/4W	10%	172022200
R30	CACP	4.7k	1/4W	10%	172034700
R31	CACP	1k	1/4W	10%	172031000
R32	CACP	120	1/4W	10%	172021200
R33	CACP	120	1/4W	10%	172021200
R34	CACP	470	1/4W	10%	172024700
R35	CACP	1k	1/4W	10%	172031000
R36	CACP	1k	1/4W	10%	172031000
R37	CACP	470	1/4W	10%	172024700
R38	CACP	4.7k	1/4W	10%	172034700
R39	CACP	4.7k	1/4W	10%	172034700
R40	CACP	1k	1/4W	10%	172031000

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PCB 3 (Cont)

Cct. Ref.	General Description				Solartron Part No.
R41	CACP	4.7k	1/4W	10%	172034700
R42	CACP	4.7k	1/4W	10%	172034700
C1	CERM	220p	500V	20%	241322200
C2 to C7	CERM	0.047	25V	+50% −25%	241944700
C8 to C12	CERM	0.047	25V	+50% −25%	241944700
C13	TAND	15	20V	10%	265771500
D1	SD3				300522160
IC1	SN7474N				510000490
IC2	SN7405N				510002080
IC3	SN7407N				510000750
IC4	SN7403N				510001200
IC5	SN74175N				510001310
IC6	SN74175N				510001310
IC7	SN7404N				510000410
IC8	SN7402N				510000270
IC9	SN7400N				510000340
IC10	SN7403N				510001200
IC11	SN74390N				510002140
IC12	SN7442N				510000330
IC13	SN74165N				510001480
IC14	SN7404N				510000410
IC15	SN7405N				510002080
IC16	SN7403N				510001200
IC17	SN74191N				510000940
IC18	SN7412N				510002090
IC19	SN7400N				510000340
IC20	SN7410N				510000420
IC21	SN7402N				510000270
IC22	SN7427N				510001590
IC23	SN7474N				510000490
IC24	SN7474N				510000490
IC26	SN7404N				510000410
IC27	SN7400N				510000340
IC28	SN7402N				510000270
IC29	SN7400N				510000340
IC30	5082-4351 Opto Coup.				300540150
IC31	5082-4351 Opto Coup.				300540150
IC32	SN74393N				510002150
IC33	SN74390N				510002140
IC34	5082-4360 Opto Coup.				300540160
IC35	SN7403N				510001200
IC36	SN7422N				510002100
IC37	5082-4360 Opto Coup.				300540160
IC38	SN7400N				510000340
IC39	5082-4360 Opto Coup.				300540160
SW1	Twin DPDT (sample)				379600402
SW2	Twin DPDT (control)				379600101
SW3	Quintuplet DPDT (rate)				379613801
SW5	Quintuplet DPDT (mode)				379613201
SW6	Twin DPDT (self check)				379613101
SK1	14 pin DIL				300584680
SK2	16 pin DIL				300584860
SK3	16 pin DIL				300584860
SK4	16 pin DIL				300584860
SK5	16 pin DIL				300584860
SK6	16 pin DIL				300584860
SK8	14 pin DIL				300584680
B1 to B28	Berg Post				355501050
TP1 to TP10	Disconnect pins				355900550
	Test Hook				359600101
	Bus Bars				480090080

PCB 4

Cct. Ref.	General Description				Solartron Part No.
R1	CACP	47Ω	1/4W	10%	172024700
R2	CACP	47Ω	1/4W	10%	172024700
R3	CACP	2.7k	1/4W	10%	172032700
R4	CACP	2.7k	1/4W	10%	172032700
R5 to R12	CACP	4.7k	1/4W	10%	172034700
C1 to C6	CERM	0.047	25V	+50% −25%	241944700
C7	CERM	680p	500V	20%	241326800
C8	CERM	1000p	500V	20%	241331000
C9	CERM	330p	500V	20%	241323300
C10	CERM	330p	500V	20%	241323300
IC1	SN74393N				510002150
IC2 to IC4	SN74390N				510002140
IC5	SN74157N				510001280
IC6	SN7400N				510000340
IC8	SN74151N				510000850
IC9	SN74107N				510000810
IC10	SN7474N				510000490
IC11	SN74107N				510000810
IC12	SN7412N				510002090
IC13	SN7402N				510000270
IC14 to IC20	SN74190N				510000930
IC21 to IC24	SN74151N				510000850
IC25	SN74157N				510001280
IC26	SN7489N				510001300
IC27	SN7438N				510002110
IC28	SN7408N				510000830
IC29	SN7408N				510000830
IC30	SN7432N				510001510
IC31	SN7427N				510001590
IC32	SN7474N				510000490
IC33	SN7410N				510000420
IC34	SN7402N				510000270
IC35	SN7430N				510000430
IC36	SN7404N				510000410
IC37	SN7405N				510002080
IC38	SN7400N				510000340
TP1 to TP7	Disconnect Pins				355900550
SK1 to SK6	16 pin DIL				300584860

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