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T1/E1 SERIAL DATA SEQUENCER

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HEALTH AND SAFETY AT WORK

Introduction

Schlumberger Technologies have made every effort to ensure that ATE products comply with the relevant statutory safety requirements for electronic measuring apparatus detailed in **EN60950**. However, as with any apparatus that involves a degree of flexibility in order to suit a particular customer's requirements, various factors remain outside Schlumberger Technologies' control, and, broadly speaking, these fall into the categories below.

Hazardous Voltages/High Current Sources

It is of **paramount importance** that only properly trained service personnel are allowed to gain access to the interior of the equipment as this may expose areas at hazardous potentials or carrying high currents.

The test head receiver, unit under test and Signal Access Unit (where fitted) may also have hazardous voltages present while testing is in progress. A hazardous voltage is defined as a potential exceeding 42.4V peak A.C. or 60V D.C.

The voltages present depend on the particular system configuration and application test program. Consequently it must be the responsibility of the customer to:

a) Warn operating personnel of potential hazards,

b) Ensure adequate training of personnel, and

c) Provide, where appropriate, means of guarding operators from hazardous voltages whilst testing is in progress.

Motorized Assemblies

Most cooling fans are shrouded assemblies. Nevertheless, before attempting to remove air filters, etc., service personnel must ensure that equipment is switched off, since it is not always obvious when fan blades are in motion.

Toxic Material

The use of items from an Original Equipment Manufacturer (OEM) cannot preclude the use of toxic materials. For example, some power supply manufacturers use beryllium oxide, a high-toxicity compound, to provide the thermally conductive, electrically insulating washer between a power transistor and its heatsink. Before attempting to repair any such item, the customer should read the appropriate manufacturer's handbook.

Networked Systems

Test systems controlled via a Local Area Network from remotely sited workstations can be activated without warning, leading to equipment or test connections becoming 'live' at any time whilst the test system is connected to the network. Where test systems are networked, precautions should be taken to ensure remote activation of a test system cannot cause injury to people working in the immediate vicinity of the tester.

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PREFACE

DOCUMENT CONTENT

The **T1/E1 Protocol Generator** manual forms part of the user documentation for the Schlumberger Technologies CATE software and test systems.

It describes the T1/E1 Serial Data Sequencer card and control software used in telecoms test systems, and is intended as a guide for the test programmer.

REVISION POLICY

This document is deemed to be correct at the time of publication but Schlumberger Technologies assumes no responsibility for any errors found herein. Schlumberger Technologies reserve the right to amend this document without prior notice, in order to maintain currency with latest system software/hardware developments.

Schlumberger Technologies reserve the right to amend and update hardware and software without prior notice.

RELEASE NOTES SUPPLEMENTARY INFORMATION

There is no Release Notes Supplementary Information in this revision of this document.

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REVISION HISTORY

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01	May 94	Initial issue

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SECTION 1

INTRODUCTION

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SCOPE AND ORGANIZATION OF THIS DOCUMENT

GENERAL	This manual is a guide to the use and programming of the T1/E1 Serial Data Sequencer instrument.
Section 1 - Introduction	This section, describing the scope and organization of the manual and providing an overview of the T1/E1 SDS Card.
Section 2 - General Control Features	A description of the TELECOM WORKBENCH facilities provided for general control of SDS cards and VXI triggering.
Section 3 - Clocks	A description of the clock sources and programming facilities. How to synchronize multiple SDS cards.
Section 4 - T1/E1 SDS Formatting Facilities	The SDS frame format, line code violation, CRC and Tx and Rx alarms options and the TELECOM WORKBENCH facilities for programming them.
Section 5 - Data Resources	The SDS data resources. Active and Control Data Resources, Signaling and Parity resources. Setting up the PRBS and BERT generators. Setting up the Rx Errors and Channel Associated Signaling facilities.
Section 6 - Line I/O and UART Facilities	Setting up the T1/E1 line interface and Jitter facilities. A description of the UART channels, how to enable them and how to set up the serial data format.
Section 7 - Installation and Hardware	An overview of the installation and networking requirements of the SDS card. Example `VXI.config` and `Instrument.config` entries for T1/E1 SDS cards. An outline of the front panel layout and connections.

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INTRODUCTION

The **T1/E1 Protocol Generator** (Serial Data Sequencer or SDS) Card provides protocol and timing signals for line interface units using the T1 1.544 MB/s or E1 2.048 mb/s interfaces defined by ANSI T1.107, CCITT G.703 and CCITT G.704.

Using external or on-board clock and data sources, the SDS maps data and control information into two data streams and provides supplementary clock and control pin (phase pin) signals to the Unit Under Test or Test Interface.

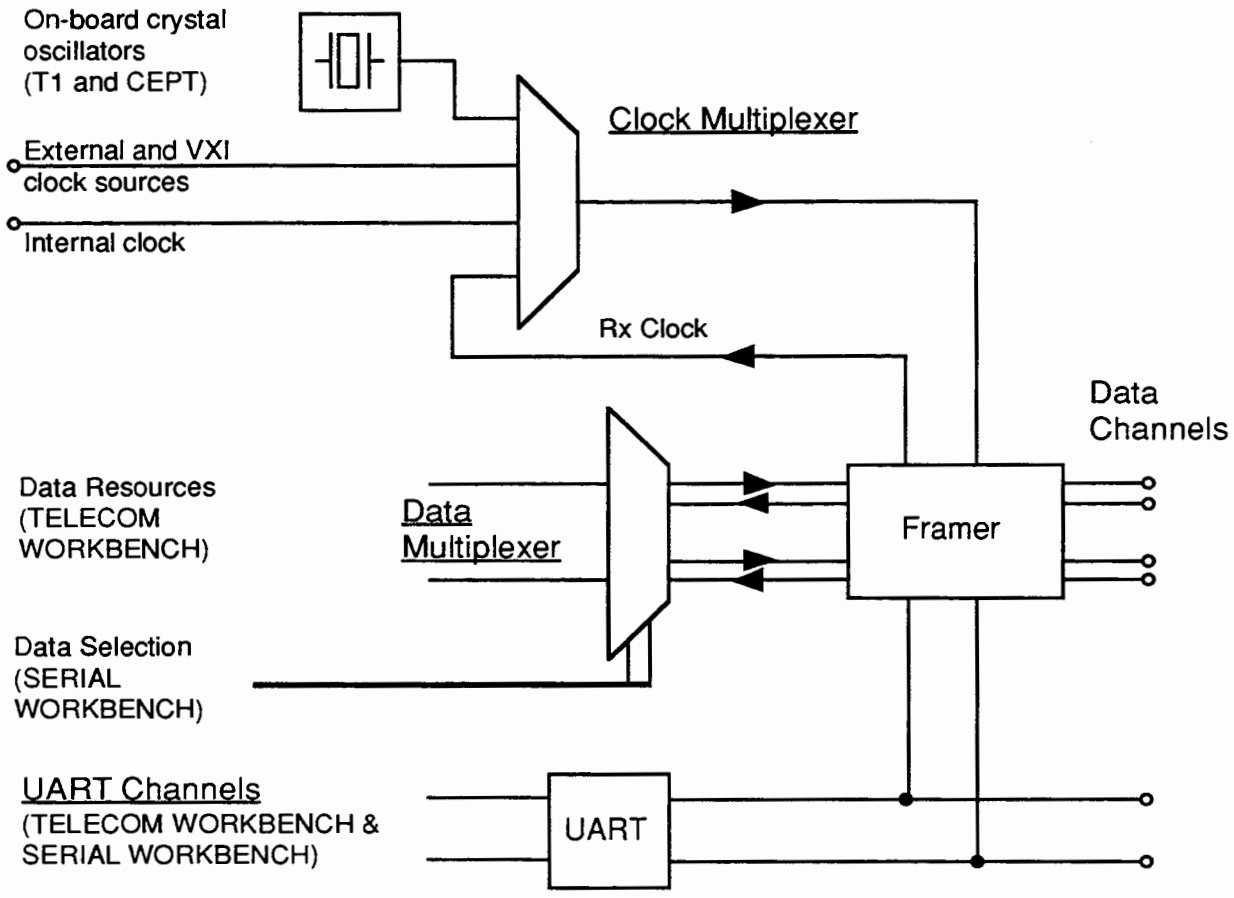


FIG 1 - MAIN ELEMENTS OF THE SDS CARD

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Features

The main features of the SDS card are:

- Two Tx/Rx data highways
- 1.544 or 2.048 MHz clock sources
- Multiple data sources, using programmable or dynamically calculated data
- Multiple clock generation from standard, user defined and external sources
- Wide variety of T1 and E1 frame formats
- Jitter generator
- Four selectable interrupt inputs
- Two semi-custom serial (UART) ports, which may be used for FDL
- Synchronization to VXI bus and/or other SDS cards

Physical

The SDS card is a C size VXI module operating in conjunction with the CPU30 bus controller. The CPU30 provides high level control of the SDS, with low level control of data streams and timing pins carried out by the SDS card on board controllers.

CONTROLLING THE SDS CARD

The SDS is controlled by Schlumberger's graphic SERIAL WORKBENCH and TELECOM WORKBENCH software. The SERIAL WORKBENCH defines the data sources, while the TELECOM WORKBENCH specifies the protocols and test data and provides control and test information.

TELECOM WORKBENCH

The TELECOM WORKBENCH is an application of the INSTRUMENT WORKBENCH, containing facilities to drive and control telecom instruments. SDS control facilities are installed in the TELECOM WORKBENCH when the target system contains an SDS card.

SYSTEM DESCRIPTION

SDS cards must be identified in the compiled test database **System description** file. The System description syntax is:

`SDSnT1E1` where:

`n` is an integer identifying the card in the system. Normally 0 is used for the first card, 1 for the second card, and so on. `n` must correspond to the SDS names in the VXI_config file.

`T1/E1` identifies the SDS card type.

Example

```
#INSTRUMENTS        (#IEEE_PINS may be used instead for compatibility)
etc...
SDS0T1E1
SDS1T1E1      etc...
```


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SECTION 2

GENERAL CONTROL FEATURES

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INTRODUCTION

Most of the SDS TELECOM WORKBENCH facilities control specific aspects of SDS operation, such as clock or PLL setup. The following facilities affect the card as a whole, or are used by several SDS functions.

SDS facilities use standard TELECOM WORKBENCH windows. Two features, the **Device** selector and **Wait for Completion** checkbox, are common to many or all windows.

SDS DRIVERS

SDS functions are controlled using calls from the SDS driver library. It is not necessary to use or be familiar with the SDS driver called. Advanced users can obtain information on the library by selecting Help from any point and entering `C_SDS_call_driver` into the **apropos** field.

SETTINGS

In general, any settings made remain in force until specifically changed by the programmer, or cleared by program termination. For instance, once a data source has been enabled, the tools for that source may be ignored in any further events using the same facility. It is not necessary to enable the source in further events until a change is required.

When inspecting an event, you should be aware that "not selected" means "no change", and does not necessarily mean "not in use".

DEVICE

Up to four SDS cards may be fitted to a system. The Device Selector identifies the card to which the particular setup will be applied (Fig 1).

The default state of the selector is **Undefined**. A valid card number or **All** must be selected even if only one card is fitted.

The list of devices is generated from the compiled System Description file in the current test database.

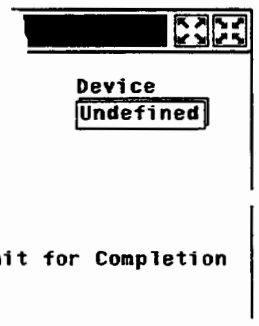


FIG 1 - DEVICE AND WAIT FOR COMPLETION

All

All sends the same command to all SDS cards fitted to the system. This selection should be **used with care** if the system contains more than one type of SDS card - if the command is not valid for all types, system operation will be undefined.

If more than one type of SDS card is fitted, a separate event must be used for each instrument if the command is not relevant to all types.

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WAIT FOR COMPLETION

When a setup or operation is encountered during runtime, appropriate commands are sent to the hardware. The software can then continue to process the test program without waiting for an acknowledgment, pipelining the hardware commands to be executed in turn. This allows fastest test program execution.

Alternatively, program execution can be halted until the operation is completed by checking the **Wait for Completion** box, where present. This is used when a particular event must be finished before the program should continue.

Debug Mode

In **Debug** mode, all commands complete before returning regardless of the state of the Wait for Completion checkboxes.

SDS WAIT

The **SDS Wait** facility synchronizes the operation of the Serial Data Sequencer with the test program, and inserts delays in the SDS command queue.

The card can be programmed to wait for

- a specified time, in milliseconds. This is applied to all data resources.
- completion of Tx and/or Rx sequences on any (or all) of the Active Data Resources.

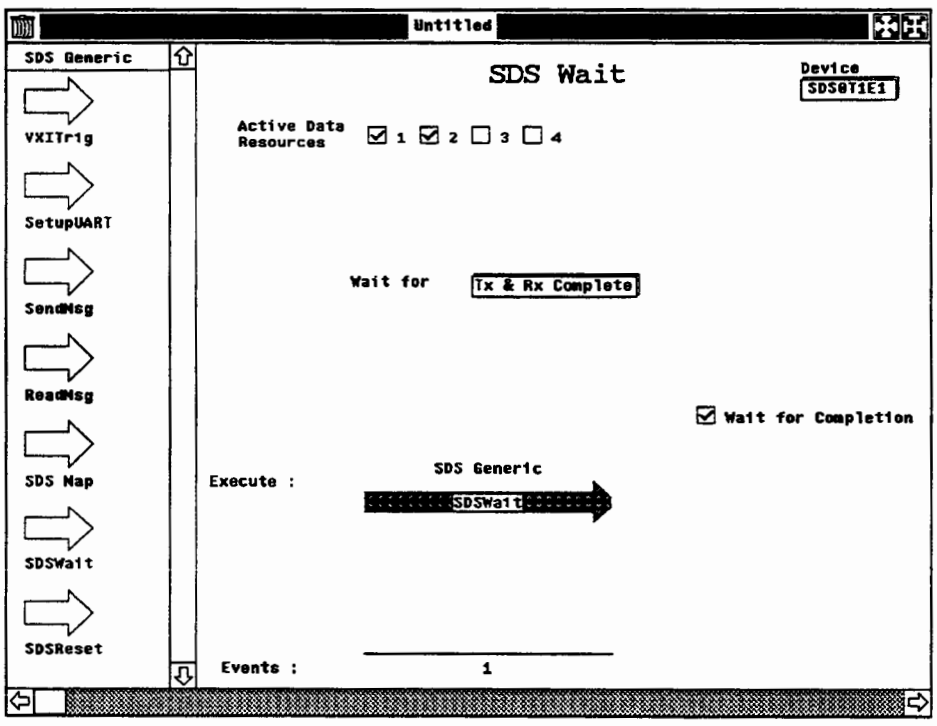


FIG 2 - SDS WAIT FACILITY

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Use

- Choose the SDS **instrument** that will receive the command.
- Select the **resources** to which the wait will apply. **Wait for Time** applies to all resources.
- Select the **wait** event, or time.
- If **Time** is selected, enter a MEDIATOR I expression specifying the **wait interval** in milliseconds.
- Select **Wait for Completion** if required.

SDS MAP

The **SDS Resource Mapping** Facility (**SDS Map**) allows the user to specify a logical mapping between UUT channel numbers and certain SDS physical resources. This is particularly useful for managing test programs where concurrency is used, as the level of concurrency may then be altered (within the capabilities of the hardware resources) without the need to reprogram all instances of the resource control facilities.

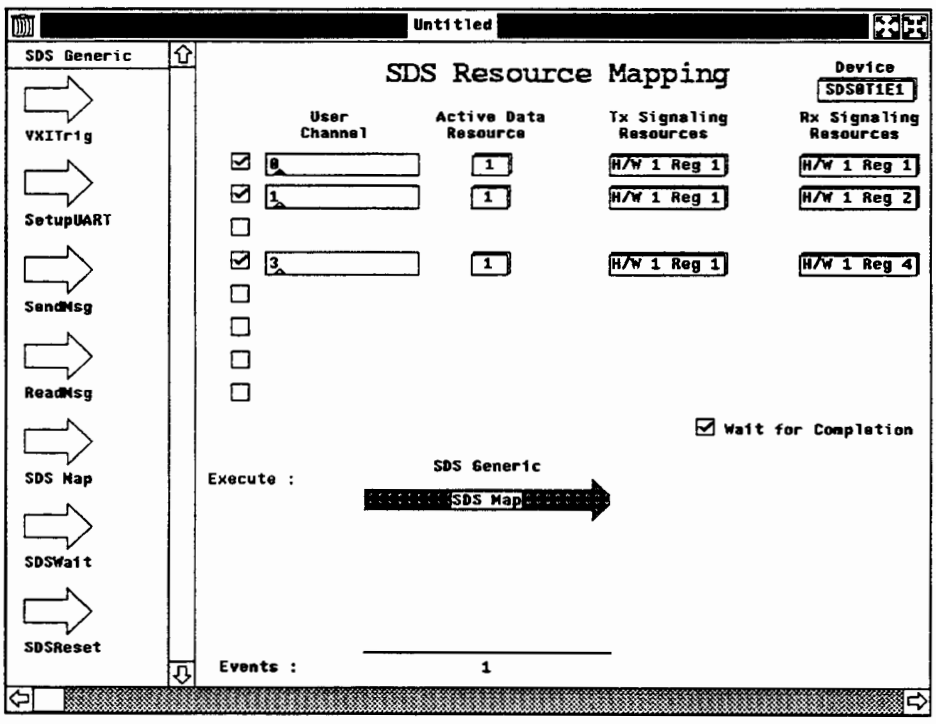


FIG 3 - SDS RESOURCE MAPPING FACILITY

The user may program up to eight mappings per screen. The User Channel may be entered as a MEDIATOR I expression, which gives the possibility of placing this facility inside a repeat loop to give mappings for many more channels.

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Use - General

- Choose the SDS instrument to receive the command, using the **Device** tool. The choices are generated from the contents of the compiled Target System file in the current test database.
- Select **Wait for Completion** if required.

For Each Channel

- Enter a MEDIATOR `I` expression evaluating to the number of the **User Channel** to be programmed.
- Select the **Active Data Resource** which will carry that channel's data.
- Select the T**x** or **Rx Signaling** register which corresponds to that channel. This capability is useful for programming concurrent tests for UUTs which employ channel associated signaling.

SDS RESET

The **SDS Reset** facility resets the Serial Data sequencer to its power on reset state.

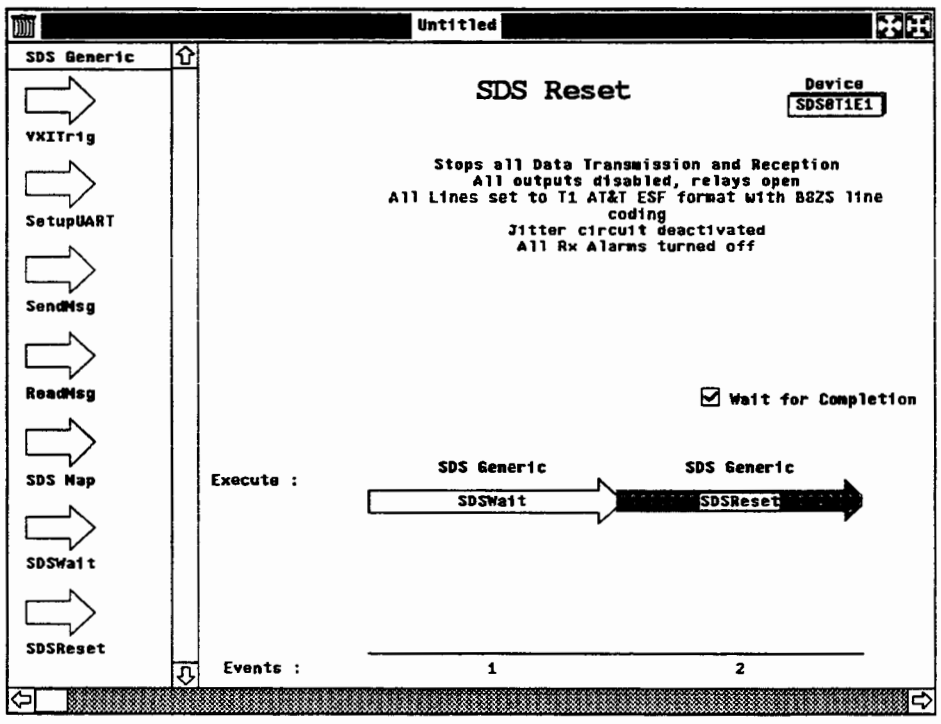


FIG 4 - SDS RESET FACILITY

The only user action required is to select the instrument that will receive the command.

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DEFAULT SETTINGS

The **default settings** restored by a Reset are:

- All data transmission is stopped
- Any executing SERIAL WORKBENCHES are stopped
- Tx Signaling Registers are cleared to zero
- All outputs are disabled (set to high impedance)
- All output connect relays are opened (data and clock)
- All connections to VXI TTL triggers are opened
- All clocks are disabled (set to Quiet)
- Parity is set to Odd

VXI TRIGGERS

The SDS card has access to the eight backplane **VXI trigger** lines. Two multiplexers are available to select any two of the trigger lines on to the SDS card, and a further three multiplexers select a variety of signals from the card on to the backplane trigger bus.

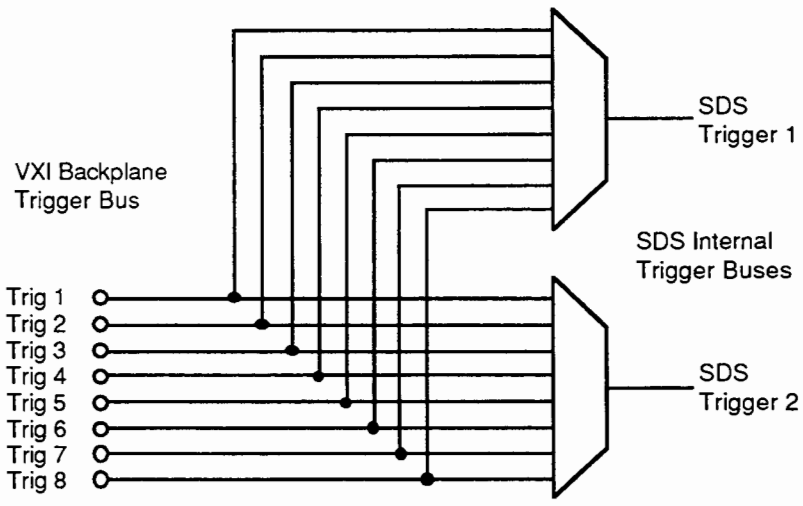


FIG 5 - VXI TRIGGER 1 AND 2

The two incoming trigger buses are called **SDS Trigger 1** and **SDS Trigger 2**. The three outgoing buses are **SDS Trigger 3** to **5**. Each of the trigger buses may be connected to any of the backplane buses, or may be off.

VXI TRIGGER FACILITY

This facility connects the backplane **VXI TTL Trigger** (**VXITrig**) bus to the Serial Data Sequencer's internal trigger and clock circuits. The incoming signals are displayed on the left of the window, and the signals from the SDS card to the backplane are displayed on the right.

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The VXITrig facility selects the backplane trigger line to connect to the SDS card. The source or destination of the on board bus are not defined by this facility, but by other facilities such as **ClockSel**.

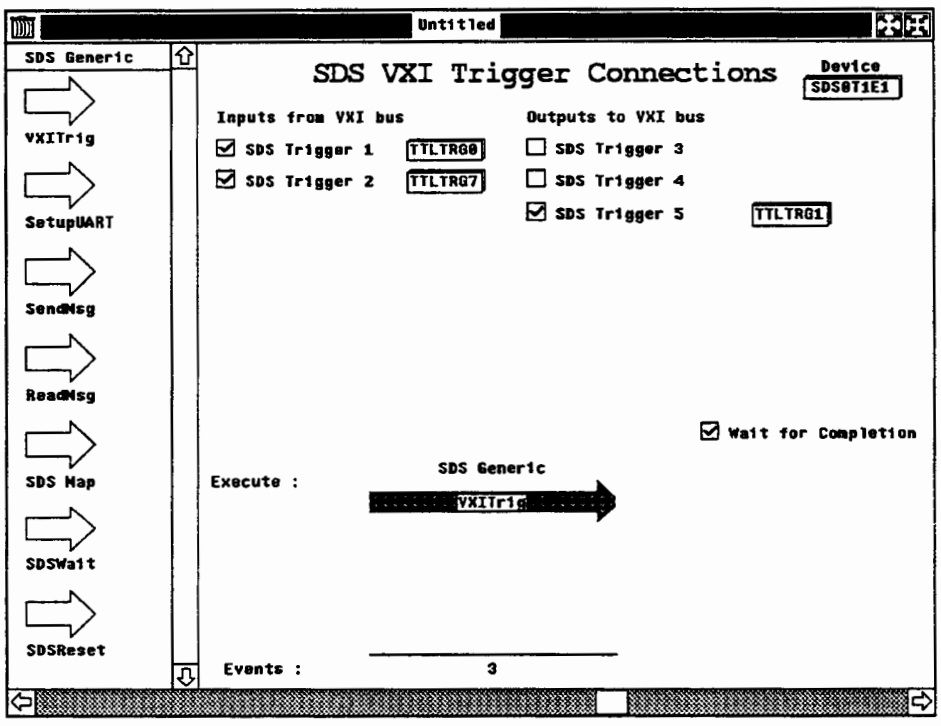


FIG 6 - VXI TRIGGER FACILITY

Each trigger is enabled by checking the box next to its name. Once enabled, a multiple choice button is displayed to select the backplane trigger line to which the bus will be connected.

If a check box is not selected, the settings for that trigger remain unaltered. Any settings made in a previous event remain unaltered.

Use

- Choose the SDS instrument to receive the command, using the **Device** tool.
- Enable **SDS Trigger 1/2**, if required, and select the TTLTRG line which will drive them, or disconnect from the TTLTRG bus by choosing **None**. If the checkbox is not ticked the SDS hardware state is not changed.
- Enable **SDS Trigger 3/4/5**, if required, and select the TTLTRG line that will be driven by them, or disconnect from the TTLTRG bus by choosing **None**. If the checkbox is not ticked the SDS hardware state is not changed.
- Select **Wait for Completion** if required.

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SECTION 3

CLOCKS

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T1/E1 CLOCKS

INTRODUCTION

The SDS card provides several clocks, which may be obtained from a variety of sources. The clocks from the SDS are used to clock data and phase pins, to provide clocks and timing signals on the tester VXI trigger bus for other cards, and to directly clock the Unit Under Test (UUT).

Clock control

Clocks are selected, and on-board clocks set up, using facilities in the TELECOM WORKBENCH. The TELECOM WORKBENCH facilities used are:

Facility Title	Facility Name
SDS VXI Trigger Connections	VXITrig
SDS Clock Select	ClockSel
Setup Phase Locked Loop	SetupPLL
Jitter	Jitter

The Jitter facility is described in the **Line I/O and UART Facilities** section.

CLOCK SOURCES

The SDS card provides an extremely flexible choice of clock sources. Clocks can be obtained from:

- On board crystal oscillators (User defined)
- External connector (Front panel)
- Tester-derived clocks (via VXI trigger lines)
- Internal 16.667 MHz master clock
- Recovered Rx clock
- Phase Locked Loop (PLL)

The following table lists the main clock features:

Clock	Number of Sources	Frequency	Remark
On board Crystal	Up to two	64 MHz max	XTAL1 configured to 4.096 MHz, XTAL2 configured to 3.088 MHz
Front Panel Synchronous	Two	16.384 MHz max	
VXI Trigger	Eight	12 MHz max	Signals are provided by other instruments.
Internal	One	16.667 MHz	Fixed
Phase Locked Loop	One, with three outputs	20 MHz max input frequency	Wide range of output frequencies

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Phase locked loop

Each of the above clocks can be passed through an internal phase locked loop circuit. The PLL provides a highly stable user-specified derivative of the selected clock frequency.

The PLL circuit and control software is described under a separate heading in this section.

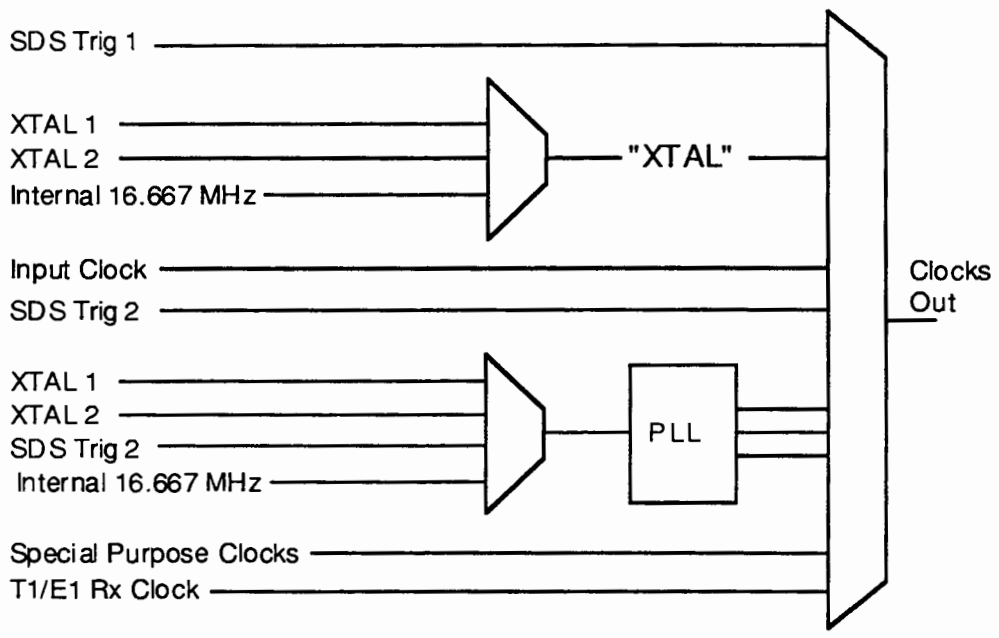


FIG 1 - CLOCK SOURCES

VXI Trigger Inputs

Eight VXI trigger inputs are accessible from the VXI backplane. Any of the trigger inputs may be selected as a clock input, either directly or via the PLL circuit.

The trigger inputs are selected by two hardware multiplexers on to two internal trigger bus signals, **SDS Trig 1** and **SDS Trig 2**. Any of the eight triggers (or none) may be selected on to either bus, using the **SDS VXI Trigger Connections** facility. The SDS Trig bus signals are further selected by the clock multiplexing circuits as required.

Signals

The signals present on the VXI trigger lines are not controlled by the SDS card, but are supplied by other instruments, and must be set up by the facilities controlling those instruments.

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Crystal Clocks

Two crystal clocks are fitted on the card. The crystal frequencies are defined when the SDS card is ordered, although alternative crystals may be fitted or added later by arrangement with Schlumberger. The maximum frequency of any oscillator is 64 MHz.

Unless otherwise specified, the following are supplied as factory settings:

Crystal	Frequency
XTAL 1	2.048 MHz
XTAL 2	1.544 MHz

XTAL Bus

The crystal sources **and** the internal 16.667 MHz clock are multiplexed on to an internal bus called **XTAL**, which is further selected by the main clock multiplexer. The PLL circuit differs slightly, taking the individual XTAL clocks as inputs instead of the multiplexed XTAL bus.

The internal 16.667 MHz clock is also multiplexed on to the XTAL bus. Only one of the crystal clocks is switched to the XTAL bus at any time, therefore changing the selected crystal affect all other clocks using the crystal bus as input.

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GENERAL

The clocks available on T1/E1 SDS cards include several **Output** clocks which may also be used to clock/trigger other instruments or the Unit Under Test (UUT). A front panel **input** is also provided to clock the SDS card from an external source. The output clocks are:

- Tx Data Clock
- Output Clocks 1 and 2
- SDS Trigger 3 to 5
- SDS Multiboard Sync

TX DATA CLOCK

Tx Data Clock is the signal which provides the transmit data clock to the SDS frame formatters. It should be set to 1.544MHz for T1 formats and 2.048MHz for CEPT formats. **Jitter** can be applied to Tx Data Clock except when Input Clock or Rx Data Clock is selected as the source for this clock.

The frequency applied to Tx Data Clock is divided by two if the source selected is SDS Trigger 1 or PLL Output/N (described later in this section).

OUTPUT CLOCKS 1 AND 2

Output Clock 1 and 2 are front panel clock outputs which may be used to supply synchronizing signals to other instruments or to the Unit Under Test.

TRIGGER BUS CLOCKS

SDS Trigger 3 to 5 are trigger signals connected to the VXI backplane. A clock from the SDS card may be connected to one or more of these lines by checking the appropriate box in the SDS Clock Select facility. All three may also be routed onto the VXI backplane using the **VXITrig** facility.

SDS Trigger 3 is programmed to **SWB Sync** for the SDS device which will be the timing master. This provides the Sequencer synchronization signal to the slave SDS cards.

SDS MULTIBOARD SYNC

SDS Multiboard Sync is used to identify the trigger source when cards are synchronized. Synchronization is described under a separate heading.

INPUT CLOCK

Input Clock is a front panel clock/trigger input. Note that the Input Clock radio button must be selected if Input Clock is selected as the source for any of the other clocks. Selecting the button closes the isolation relay to connect the front panel connector to the clock circuits.

SOURCES

The sources available for each clock are described below. Note that programmable sources such as the Phase Locked loop or SERIAL WORKBENCH lines must be separately set up.

The outputs may be enabled by checking the checkbox alongside the clock name. A multiple choice button is displayed alongside each **selected** clock, listing the sources which may be selected for that clock. Note that not all sources may be selected for each clock, as shown in the following table.

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PLL PLL sources are setup using the **SetupPLL** facility, described in this section.

Tx Data Clock Tx Data Clock may be specified as a source for other clock signals.

Rx Data Clock Rx Data Clock 1 & 2 are the recovered receive line data clocks for line interfaces 1 and 2, generated by the frame formatters.

Triggers The trigger selectors enable the on board input SDS trigger lines, and allow their source to be defined. Sources may be None, one of the VXI trigger lines or Sync.

Sync is used when two or more cards are to be synchronized. Synchronization is described under a separate heading.

SWB Triggers SWB Trigger 1-4 are trigger signals, whose position relative to the superframe boundaries may be programmed via SERIAL WORKBENCH.

SWB Single Shot SWB Single Shot is a SERIAL WORKBENCH positioned trigger signal which occurs only once. It may be used to trigger the start of measurements or other actions on other instruments.

SWB Sync SWB Sync is the inter-SDS synchronization signal generated by the Master SDS. SDS cards configured as slaves should have this signal connected to their Multiboard Sync input.

Source: / Clock:	Xtal	PLL Output ÷ N	PLL Output	Tx Data Clock	Rx Data Clock	Front Panel	Trigger	SERIAL WORK-BENCH
Tx Data Clock	Mux (XTAL 1 or 2)	Yes	No	n/a	Yes	Input Clock	1	
Output Clock 1	Mux	Yes	No	Yes	No		1	Trigger 1
Output Clock 2	Mux	Yes	No	Yes	No		1 & 2	
SDS Trig 3		Yes	Yes	Input Clock	No		No	Sync
SDS Trig 4		Yes	Yes	Input Clock	No		No	
SDS Trig 5	No	No	No		No			Triggers 1-4, Single shot
Multi-board sync	No	No	No		No	Input Clock	1 & 2	

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CLOCK SELECT FACILITY

The **SDS T1E1 Clock Select** facility (**ClockSel**) is used to route various clock and trigger sources to the data sequencing and trigger circuits of the Serial Data Sequencer

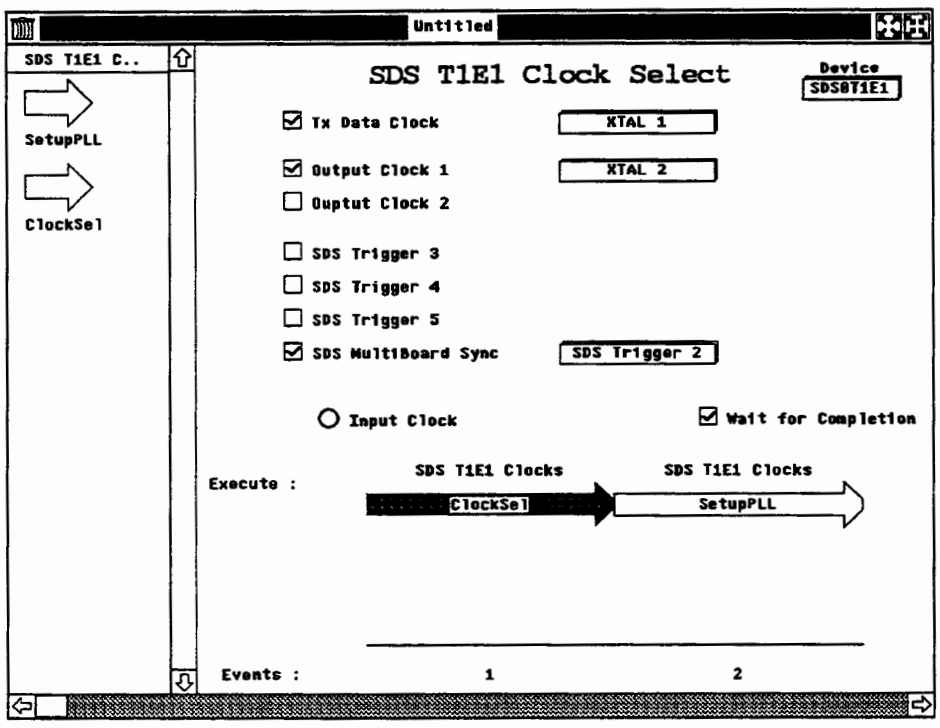


FIG 4 - SDS CLOCK SELECT FACILITY

Use

- Choose the SDS instrument to **receive** the command, using the **Device** tool.
- Choose a **source** for the **Tx Data Clock**. If not checked, the source selection is not changed from any previous selection.
- Choose **sources** for **Output Clock 1&2**, if used.
- Choose **sources** for **SDS Trigger 3-5,** if used.
- Choose a **source** for **SDS MultiBoard Sync**, used by slave SDS cards to receive Sequencer synchronization from the master SDS.
- Enable the **Input Clock** by selecting its radio button if it is used as a source for any of the other clocks.
- Check the **Wait for Completion** box if required.

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INTRODUCTION

The **Phase Locked Loop** (PLL) circuit may be regarded as a programmable crystal source, which can be used to provide a specific frequency even if a crystal or other source of the correct frequency is not available.

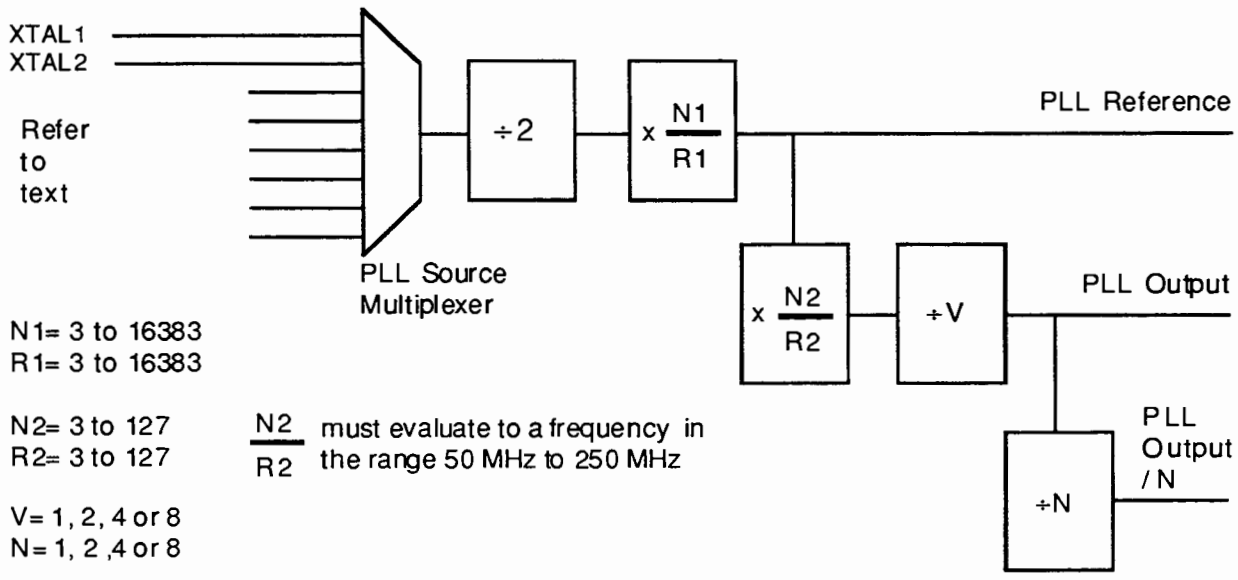


FIG 5 - PHASE LOCKED LOOP

The PLL circuit has three outputs, **PLL Reference**, **PLL Output** and **PLL Output/N**, all derived from the selected source. The maximum source frequency is **20 MHz**. The division ratios are programmed from the **SetupPLL** facility.

SETUP PHASE LOCKED LOOP FACILITY

The **Setup Phase Locked Loop** facility (**SetupPLL**) programs the PLL clock generation circuit, producing a wide range of frequencies which can then be used to drive various parts of the Serial Data Sequencer hardware.

Sources

The **Clock Sources** button is used to select the clock source for the PLL circuit. The options available are:

- XTAL 1 and 2
- Rx Data Clock 1 and 2
- SDS Trigger 2
- Input Clock
- Tx Data Clock

The PLL Clock source has direct access to each of the user crystals, so it can be programmed independently of the selections made in the SDS Clock Select facility.

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Output Frequencies

The facility calculates and displays the **frequency** at each output, using the values in the TWB.defaults file entries SDS_XTAL_1. and 2 for the frequencies of the crystals.

In the case of the other inputs the incoming frequency is not known. The **Source Frequency** field may optionally be used to identify the frequency used, by entering a numeric value (real), in kHz. The value provided will be used to calculate the output frequencies.

The output frequencies can also be set using MEDIATOR expressions. In this case the output frequencies are not calculated, as the MEDIATOR expressions cannot be evaluated until program run time.

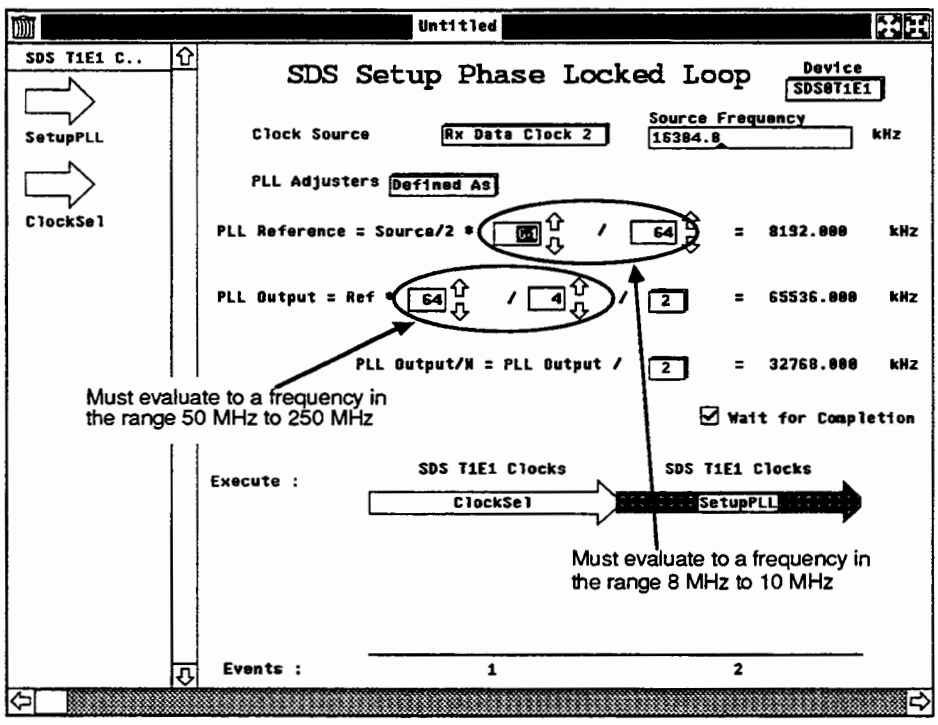


FIG 6 - SETUP PLL FACILITY

PLL OUTPUTS

PLL Output is derived by passing the Clock Source through two fractional rate multipliers. The first provides a very fine adjustment using 14-bit multipliers to produce **PLL Reference** which is a clock signal in the range 8.0 to 10.0 MHz. PLL Reference is available as a source for some SDS circuits. The second rate adjuster provides coarser rate multiplication of the PLL Reference clock.

PLL Output/N is simply the PLL Output clock divided by the selected value of N, which can be 1,2,4 or 8.

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PLL Adjusters

The relationship between the above SDS block diagram and the SetupPLL facility window is shown in Fig 7 below.

The rate adjusters can be programmed directly using incrementer tools or by MEDIATOR `I` expressions, selected using the PLL Adjusters button.

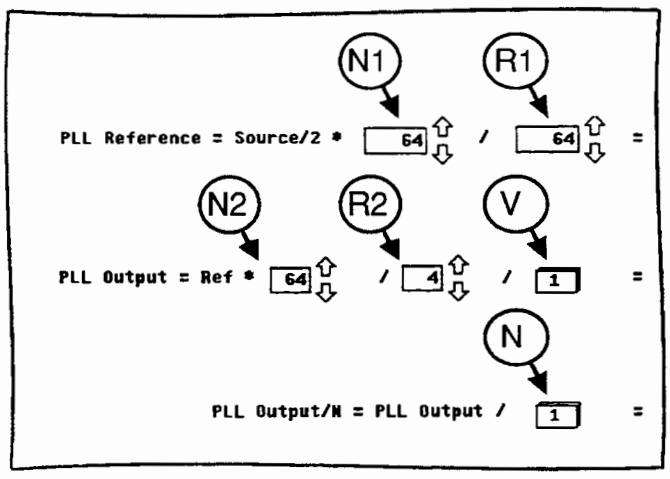


FIG 7 - RATE ADJUSTMENT TOOLS

DELAY

The SetupPLL facility always inserts a 1 second delay in the SDS command queue to allow the PLL to settle.

Use

- Choose the SDS instrument to **receive** the command, using the **Device** tool.
- Choose a clock **input** for the Phase Locked Loop circuit, with the **Clock Source** selector.
- If using a **VXI trigger** line as a clock source, make sure that the VXI trigger multiplexer has been set up to select the correct trigger line using the **VXITrig** facility.
- Enter the clock **source frequency** in kHz into the **Source Frequency** box, if using an external or trigger source for the clock (optional).
- Use the **PLL Adjusters** tool to select **Defined As**, for direct numerical input of adjustment factors, or **Expression** to use MEDIATOR expressions.
- Enter the figures or MEDIATOR expressions for the **PLL Reference**, **PLL Output** and **PLL Output/N** adjusters.
- Check the **Wait for Completion** box if required.

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INTRODUCTION

Two or more SDS cards may be synchronized to each other. One card is designated a master, and the others slaves. Any card may be designated as the master, some or all of the remaining cards as slaves. The designations may later be changed if required.

The following description is for a PCM SDS card. Synchronization for a T1/E1 card is similar.

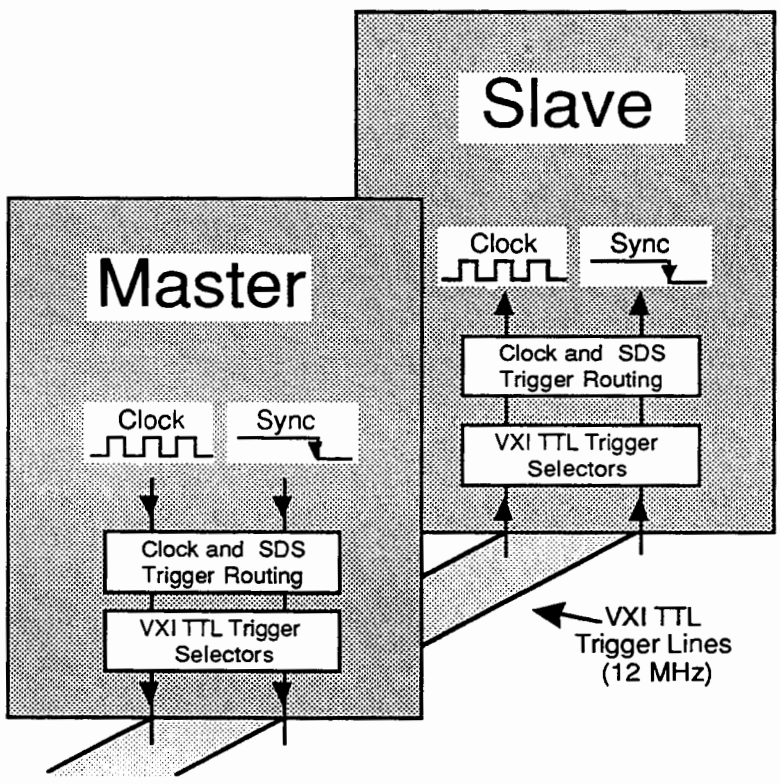


FIG 8 - TYPICAL SDS SYNCHRONIZATION SETUP

The master provides the sync signal and clock to the slaves, typically but not necessarily via the backplane VXI TTL Trigger lines.

Synchronizing Cards

To synchronize cards:

- Identify which card will be the master, and which slaves
- Decide how the clock and sync signal will be routed

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On the **master**:

- Set up and route the clock
- Select and route one of the SDS triggers for Sync

On each **slave**:

- Select and route the clock from the master
- Check the SDS Multiboard Sync box
- Identify the SDS trigger which will carry the sync signal
- Route the SDS trigger to match the master

In the **test plan**:

- Create a SERIAL WORKBENCH reference for the master SDS card
- Create a SERIAL WORKBENCH reference for each slave SDS card

Note that the SERIAL WORKBENCH reference for the master must execute first.

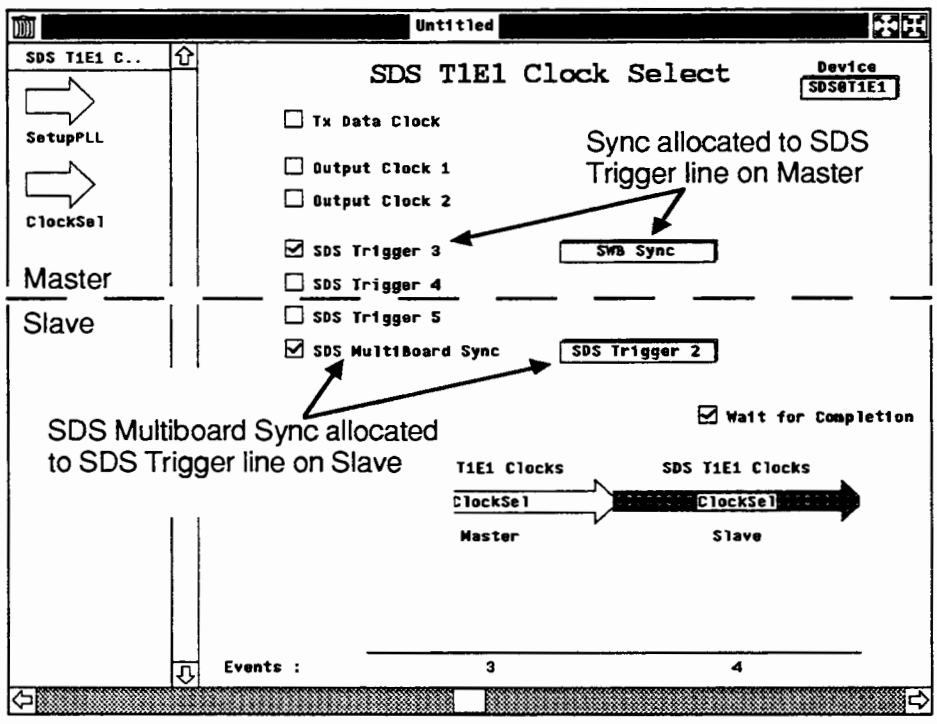


FIG 9 - INITIAL SYNC ROUTING

Clock

The clock frequency is chosen to suit the test requirements, and is selected as the **PCM Deskew Clock** on the master and all slave PCM cards.

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The clock may be routed by various means, for instance:

- Directly via the backplane **VXI TTL trigger** lines. This path is straightforward, but is subject to the VXI frequency limit of 12 MHz.
- Via **front panel/test head** connectors. This is a viable option for clocks up to 16.384 MHz, at the expense of additional fixture wiring.
- Via the **PLL Circuit**. The master clock may be divided via the PLL to a frequency suitable for the VXI bus, routed to the PLL circuit on each slave and multiplied back to the correct frequency. The clock is then routed from the PLL to the PCM Deskew clock input on each slave.

Alternatively a lower frequency clock may be routed to a VXI TTL trigger line from the master. The VXI trigger line may then be selected to the PLL input on all cards, including the master. This ensures that the clock signal has the same routing on all synchronized cards and avoids propagation differences.

SYNC

The **Sync** signal is created in the SERIAL WORKBENCH, by editing the Sync waveform to provide a negative going sync edge at the required point. Any Sync settings in slave SERIAL WORKBENCH setups are ignored.

Master

One of the SDS trigger lines 3 to 5 is allocated to Sync on the **master** SDS card, using the **ClockSel** facility. SDS Multiboard Sync is **not** checked on the master. If the sync signal is being sent along the VXI backplane, the **VXITrig** facility is typically used next to route the SDS trigger to one of the VXI TTL Trigger lines.

Slave

On **each slave**, SDS Multiboard Sync is checked and routed to one of the SDS trigger lines 1 or 2, using **ClockSel**. This is followed by the **VXITrig** facility to route the SDS trigger to the same VXI TTL Trigger line used for sync on the master.

TEST PLAN

There are several ways in which the synchronization setups may be organized in a test plan. Each card may be set up using a separate TELECOM WORKBENCH, or a single TELECOM WORKBENCH may be used to contain all the setups.

If more than one card is addressed in a single TELECOM WORKBENCH, the **Remark** tool may be used to identify each card in the TELECOM WORKBENCH window to improve program readability.

Order

The following **order** must be observed:

- TELECOM WORKBENCH setups to identify master and slaves, and to route clock and sync signals.
- A SERIAL WORKBENCH setup for the master, defining the Sync edge
- SERIAL WORKBENCH setups for slaves.

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SECTION 4

T1/E1 SDS FORMATTING FACILITIES

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INTRODUCTION

The facilities described below are used to set up the general format and operating conditions of the SDS instrument.

FRAME SETUP FACILITY

The **FrameSetup** facility (**FrameSetup**) sets the working mode of the SDS frame formatting hardware. The two line interfaces may be programmed individually but must use a common sequencer clock rate i.e. both set to either T1 or CEPT.

The user must ensure that the SERIAL WORKBENCH file correctly matches the selected frame format or data alignment errors will result.

The frame format, line code and signaling scheme may be selected for each interface. The choices available depend on whether T1 or CEPT is selected.

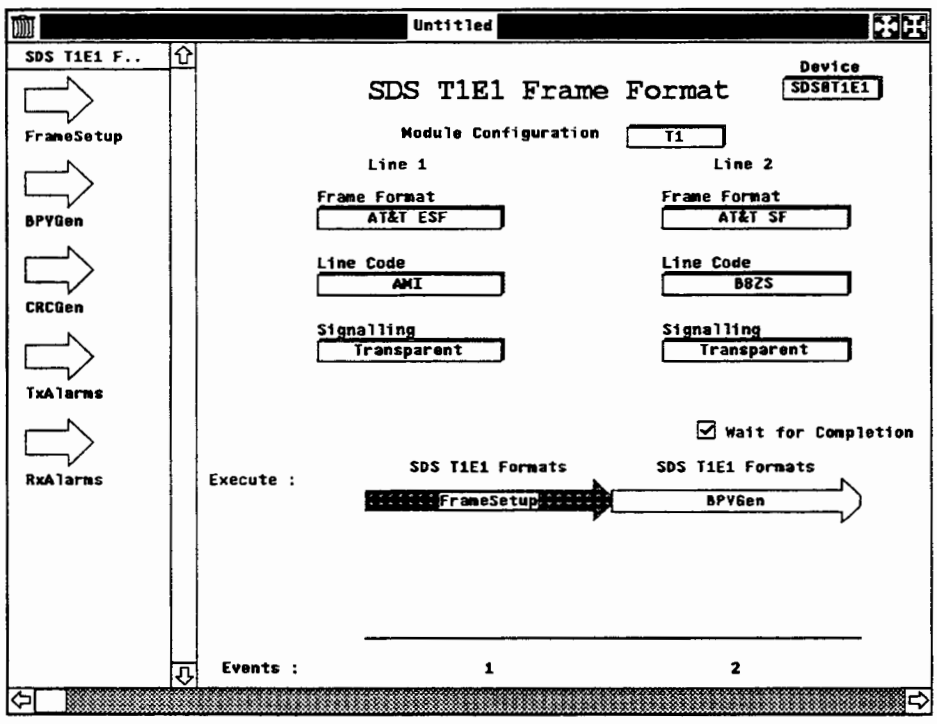


FIG 1 - FRAME SETUP FACILITY (T1)

The Module Configuration, Frame Format and Signaling tools are set to Unchanged when a Frame Setup event is created. The event will inherit and use any settings already in force, unless specifically altered.

The first Frame Setup event in the test program must be explicitly programmed to the required settings.

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T1 Formats

T1 Frame Formats and **Line Codes** supported are :

T1 Frame Formats	T1 Line Codes
AT&T and ANSI Extended Superframe	Alternate Mark Inversion (AMI)
AT&T and ANSI D4 Superframe	Zero Code Suppression (ZCS)
SLC-96	Binary 8-zero substitution (B8ZS)
Digital Data Service and Digital Data Service with Facility Data Link	

T1 **Signaling formats** supported are :

Format	Remark
Transparent	All signaling bits are defined by the SERIAL WORKBENCH programming
Robbed Bit signaling	The least significant bit of every timeslot in each sixth frame is used to transmit /receive signaling data. The data is defined by the **Tx CAS** and **Rx CAS** facilities

Message Oriented Signaling

To achieve **Message Oriented Signaling** in which timeslot 24 is reserved for signaling data, use the **Transparent** option. The messages are generated by a Control Data Resource mapped at timeslot 24. The Control Data resource should be configured to PCM CCS in the SetupActive facility.

CEPT Formats

CEPT Frame Formats and **Line Codes** supported are :

CEPT Frame Formats	CEPT Line Codes
CEPT with and without CRC4	Alternate Mark Inversion (AMI) High Density Bipolar with 3 zeros substitution (HDB3)

CEPT Signaling formats supported are :

Format	Remark
Transparent	All signaling bits are defined by the SWB programming
Per Channel Signaling Phase 0 (PCS0)	A channel associated signaling mechanism. Timeslot 16 contains four bits per channel of signaling data. The timeslot 16 multiframe is aligned with the FAS word of timeslot 0.
Per Channel Signaling Phase 1 (PCS1)	As PCS0 except that the time- slot 16 multiframe is aligned with the timeslot 0 not word.
International Remote Switching module(IRSM)	A variant of PCS0 which also provides a per channel control bit (E bit) in timeslot 0.

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Common Channel Signaling

To achieve **Common Channel Signaling** in which timeslot 16 is reserved for signaling data, use the **Transparent** option. The messages are generated by a Control Data Resource mapped at timeslot 16. The Control Data resource should be configured to PCM CCS in the SetupActive facility.

The channel associated **signaling data** for the PCS0, PCS1 and IRSM modes is programmed with the Tx CAS and Rx CAS facilities. For these modes, the user may also select "Channel Signaling Suppression" in which case the signaling bits are all programmed to 1 if they would otherwise be all 0.

Use

- Choose the SDS **instrument** to receive the command, using the **Device** tool.
- Select the required **mode** - T1 or CEPT.
- Choose the required **frame format.**
- Choose the required **signaling** method.
- Select whether **channel signaling suppression** should be applied, if appropriate.
- Check the **Wait for Completion** box if required.

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BPVGEN FACILITY

The **BPVGen** facility (**BPVGen**) controls the generation of **line code violations** for testing the error handling capabilities of a Unit Under Test. The user specifies the number of violations to be generated and the interval at which they are generated, in milliseconds.

The number of errors actually generated will lie between the number entered as a minimum, and twice that number.

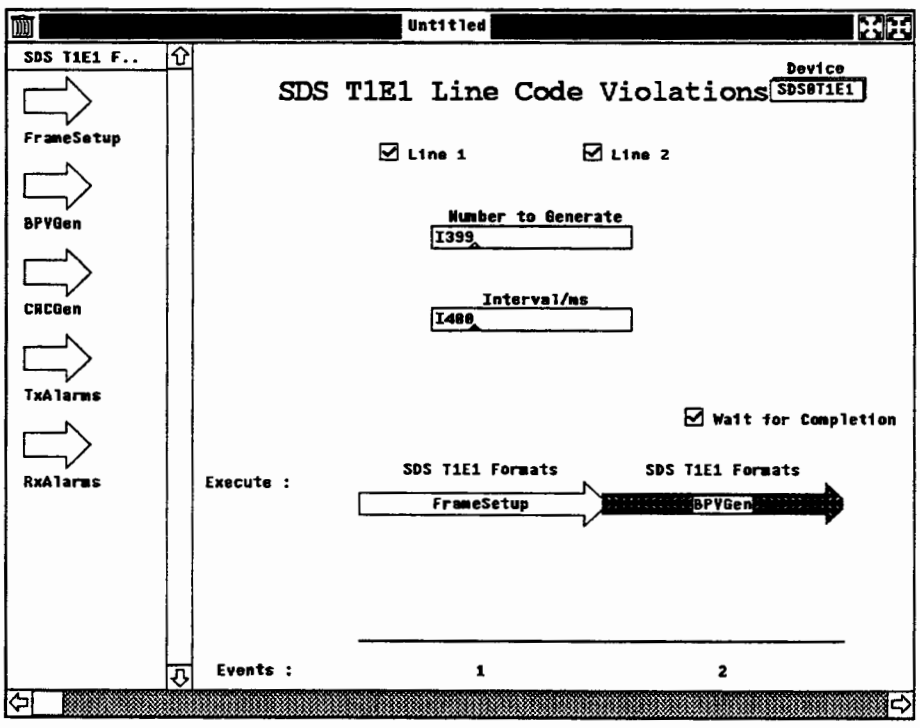


FIG 2 - BPVGEN FACILITY

Use

- Choose the SDS **instrument** to receive the command, using the **Device** tool.
- Select the **line** interface on which the violations will be generated.
- Enter a MEDIATOR I expression for the **number** of violations to generate.
- Enter a MEDIATOR I expression for the **interval** at which violations will be generated, in milliseconds.
- Check the **Wait for Completion** box if required.

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CRCGEN FACILITY

The **CRCGen** facility (**CRCGen**) controls the generation of corrupted CRC codes for testing the error handling of a Unit Under Test.

Normal or **Corrupted** CRC generation may be selected for each line interface. The hardware state after RESET is Normal. Once set to Corrupted, inverted CRC words are generated until another CRCGen event sets the mode back to Normal.

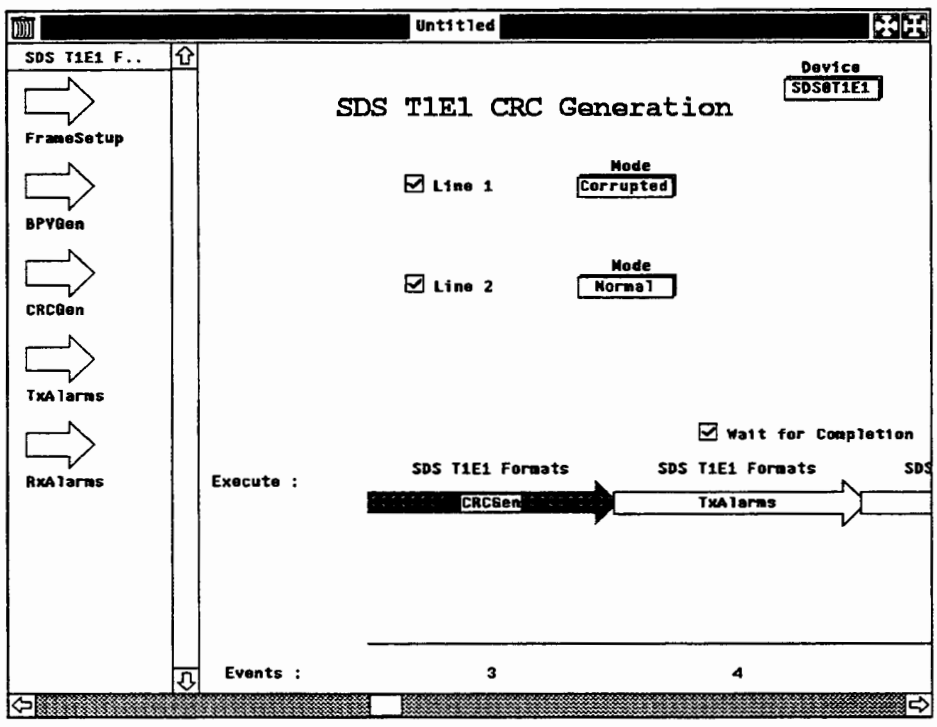


FIG 3 - CRCGEN FACILITY

If the SDS instrument is set to a mode for which CRC is not applicable (SF, SLC-96, DDS and CEPT without CRC4) the facility is ignored.

Use

- Choose the SDS **instrument** to receive the command, using the **Device** tool.
- Select the **line** or lines for which the state will be changed.
- For each selected line, select **Normal** or **Corrupted** CRC generation.
- Check the **Wait for Completion** box if required.

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TXALARMS FACILITY

The **TxAlarms** facility (**TxAlarms**) controls the SDS alarm generation capability for testing the error handling of a Unit Under Test. The alarm condition continues until another TxAlarms event sets the state to No Alarm.

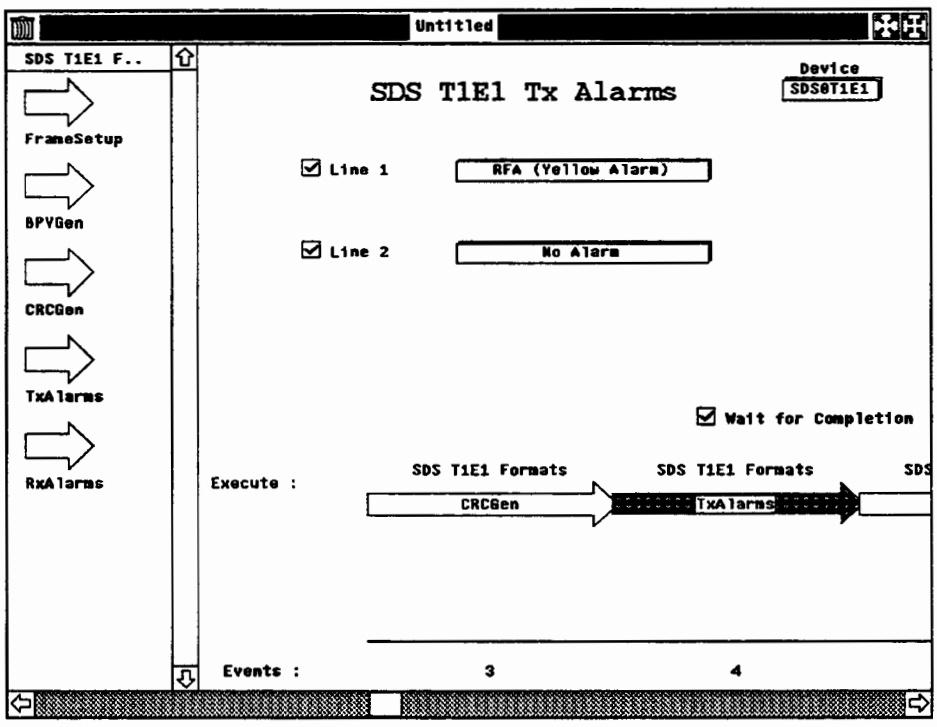


FIG 4 - TXALARMS FACILITY

The following alarm conditions may be selected for each line:

Alarm	Action
No Alarm	Turn all alarms off
RFA (Yellow Alarm)	Remote Frame Alarm
RMA	Remote Multiframe Alarm (CEPT only)
Unframed AIS (Blue Alarm)	Alarm Indication Signal (unframed)
Framed AIS (Blue Alarm)	Alarm Indication Signal (with framing information)

Use

- Choose the SDS card to receive the command, using the **Device** tool.
- Select the **line** or lines for which the alarm state will be changed.
- Choose the alarm condition for each selected line interface.
- Check the **Wait for Completion** box if required.

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RXALARMS FACILITY

The **RxAlarms facility** (**RxAlarms**) controls the monitoring of received alarm conditions from the Unit Under Test. Monitoring is also provided for several SDS internal alarm conditions.

Some alarm conditions (Remote Multiframe Alarm, Loss of TS0/16 multiframe) are only applicable to CEPT operation. A FrameSetup event must be used to program the hardware for CEPT mode before using these options.

Note that not all tools are visible with the window at its default size. It may be necessary to resize the window vertically to see all the tools.

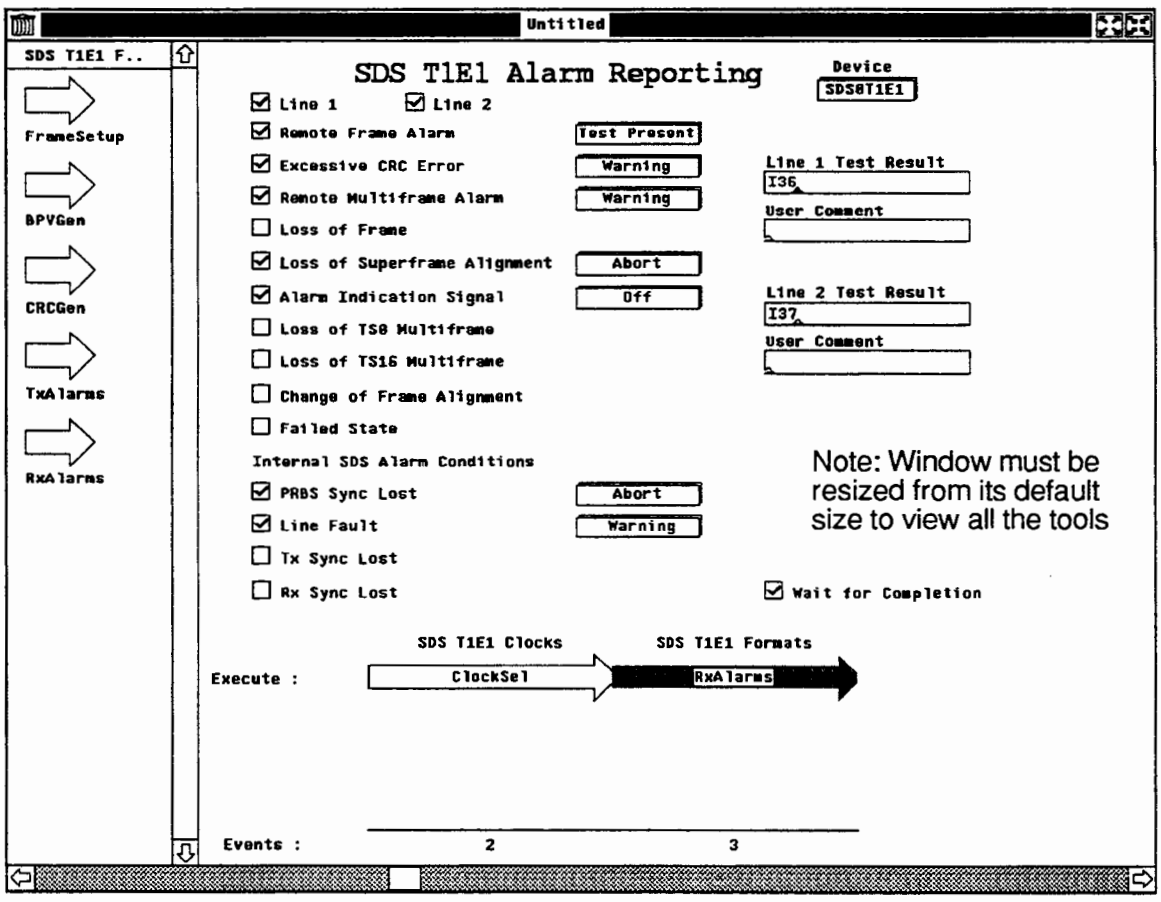


FIG 5 - RXALARMS FACILITY

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Result

The result of the test is placed in a MEDIATOR `I` variable. The result is in the form of a bit mask where a bit is set for each type of alarm present. The facility generates an expected data vector and mask vector from the alarm types checked.

Default values for the `I` variables are specified by the TWB.defaults entries T1E1_ALARMS_1 and T1E1_ALARMS_2.

Alarm and other conditions are represented as set bits in a bitfield:

bit 0	(0x00000001):	Remote Frame Alarm TS0 (Yellow alarm)
bit 2	(0x00000004):	Excessive CRC Error Indication
bit 3	(0x00000008):	Remote Multiframe Alarm TS16
bit 5	(0x00000020):	Out Of Frame (red alarm)
bit 6	(0x00000040):	Loss of Superframe Alignment
bit 7	(0x00000080):	Alarm Indication Signal (blue alarm)
bit 9	(0x00000200):	Loss of TS0 Multiframe Alignment
bit 10	(0x00000400):	Loss of TS16 Multiframe Alignment
bit 11	(0x00000800):	Failed State
bit 14	(0x00004000):	Change in Frame Alignment
bit 18	(0x00040000):	PRBS lock lost in last second [SDS_Start_PRBS]

Unused bits are masked.

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UUT Alarms

For each alarm type, monitoring may be set to:

Alarm	Action
Off	Do not monitor this alarm
Warning	Send a warning message to the DEBUG WORKBENCH if this alarm is detected
Abort	terminate the test program if this alarm is detected
Test Present	Test for the presence of this alarm.
Test Absent	Test for the absence of this alarm.

Alarm	Remark
Remote Frame Alarm	Monitor for receipt of RFA alarms from the UUT
Excessive CRC	Monitor for the receipt a large number of CRC errors occurs (CRC compatible modes only).
Remote Multiframe Alarm	Monitor for the receipt of a Timeslot 16 multiframe alarm from the UUT.
Loss of Frame	Monitor for the receipt of a Loss of Frame or Out of Frame condition at the SDS line input.
Loss of Superframe Alignment	Generate an alarm if the SDS cannot detect superframe boundaries in the received signal from the UUT.
Alarm Indication Signal	Generate an alarm if the SDS detects an AIS signal from the UUT.
Loss of TS0 Multiframe	Generate an alarm if the SDS cannot detect a Timeslot 0 multiframe in the received signal from the UUT (CEPT CRC modes only).
Loss of TS16 Multiframe	Generate an alarm if the SDS cannot detect a Timeslot 16 Multiframe in the received signal from the UUT (CEPT only).
Change of Frame Alignment	Generate an alarm if the SDS reframes.
Failed State	The SDS receiver has detected ten consecutive severely errored seconds.

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Internal SDS Alarm Conditions

Several internal alarm may be monitored, allowing the user to be alerted in the case of any problems occurring with the SDS hardware. These alarms can be set to **Off**, **Warning** or **Abort**.

Alarm	Remark
PRBS Sync Lost	The currently active PRBS detector circuit has lost synchronization with the PRBS generator stream during the previous second. It is recommended that this alarm be activated before starting a Bit Error Rate Test
Line Fault.	The transmit line driver has detected a line fault condition, which may be the transmission of continuous zeros from the frame formatter, or a short circuit on the line output.
Tx Sync Lost	The transmit section of the SDS frame formatter is unable to synchronize with the superframe marker of the bandwidth allocation sequencer. This is probably due to an incompatibility between the SERIAL WORKBENCH file and T1/CEPT mode setup of the hardware.
Rx Sync Lost	The receive section of the SDS frame formatter is unable to synchronize with the superframe marker of the bandwidth allocation sequencer. This may be due to an inconsistency between the SERIAL WORKBENCH file and the T1/CEPT hardware mode selected, or may result from the SDS framer formatter losing synchronization with the received line data.

Use

- Choose the SDS **instrument** to receive the command, using the **Device** tool.
- Select the **line** or lines to be monitored.
- Choose the alarm **condition** to be monitored for each selected line interface, and the **action** if detected.
- Specify a MEDIATOR `I` variable to receive the **result** (not applicable to internal alarms).
- Enter a user **comment** if required (not applicable to internal alarms).
- Check the **Wait for Completion** box if required.

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SECTION 5

DATA RESOURCES

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DATA CHANNELS

The SDS card has two internal Tx/Rx highway pairs. Each Tx data stream is made up of data from a number of sources, routed on to the data channel at the correct time by SDS hardware.

Data Sources

The source of each part of the data stream, or destination for Rx channels, is defined by the SERIAL WORKBENCH as part of the overall protocol definition. The SERIAL WORKBENCH defines which data sources are used, when each data source is connected to the data channel and how many bits of data are used. In addition, the SERIAL WORKBENCH defines the frame and superframe structure of the data channel.

The SDS card contains some of the data sources, for instance the signal registers. Some data is provided by other sources, such as the Array Processor, or defined in the SERIAL WORKBENCH. The SDS card obtains data from sources external to itself and collates data from all used sources into the final data stream.

Bit Rate

The data bit rate is determined by SDS facilities in the TELECOM WORKBENCH, which set up clock sources and where appropriate frequencies, as described under the heading **Clocks**.

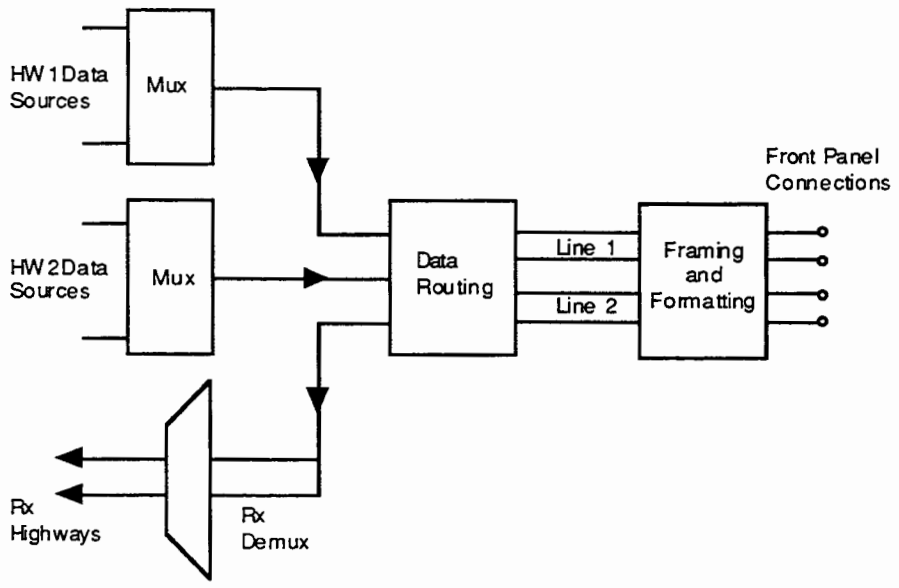


FIG 1 - DATA CHANNELS

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Active Data Sources

Four Active Data sources may be connected to either Tx or Rx Highway. The Active Data sources take data from, or place data in, Array Processor buffers as defined by Array Processor and SDS control facilities in the TELECOM WORKBENCH.

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	Applicable To:		
Data Resource	**Channel:**	**Single/Multiple Channels:**	**Tx or Rx**
No data	Both	Multiple	Both
High	Both	Multiple	Tx Only
Low	Both	Multiple	Tx Only
Pseudo random data	Both	Multiple	Both
Parity ch1	1	Single	Tx Only
Parity ch2	2	Single	Tx Only
Active Data			
Active data 1	Both	Single	Both (see text)
Active data 2	Both	Single	Both (see text)
Active data 3	Both	Single	Both (see text)
Active data 4	Both	Single	Both (see text)
Background data			
Background data	Both	Multiple	Tx Only
Control Data			
Control data 1	Both	Single	Both
Control data 2	Both	Single	Both
Signaling data HW1:			
Signaling data Tx 1 to 4	1	Single	Tx Only
Signaling data Rx 1 to 4	1	Single	Rx Only
Signaling data bit A to H	1	Single	Tx Only
Signaling data HW2:			
Signaling data Tx 1 to 4	2	Single	Tx Only
Signaling data Rx 1 to 4	2	Single	Rx Only
Signaling data bit A to H	2	Single	Tx Only

There are certain requirements when the same Active Data sources are used in both a Tx and Rx channel. The requirements are described under the Active and Control Data Resources heading.

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INTRODUCTION

The Active Data and Control Data resources are used for variable data controlled by the test program, typically data which may change frequently during the program such as PCM data. The data is obtained from MSP buffers, which are accessible to other instrument software. For instance, active data can be derived from an array processor calculation, placed into an active data resource and framed into an output data stream.

Allocation

The data resources may be used in any sequence in a Tx channel. If used in a Tx channel, the same data resources must also be used in the corresponding Rx channel in the same sequence as in the Tx channel.

The requirements are:

- The same Active Data resources must be used
- They must be in the same order
- They must have the same number of bits.

The Active Data sources in the Rx channel need not align with the Tx data, and data received in these timeslots does not need to be used. Other data resources may be used in between the Active data timeslots.

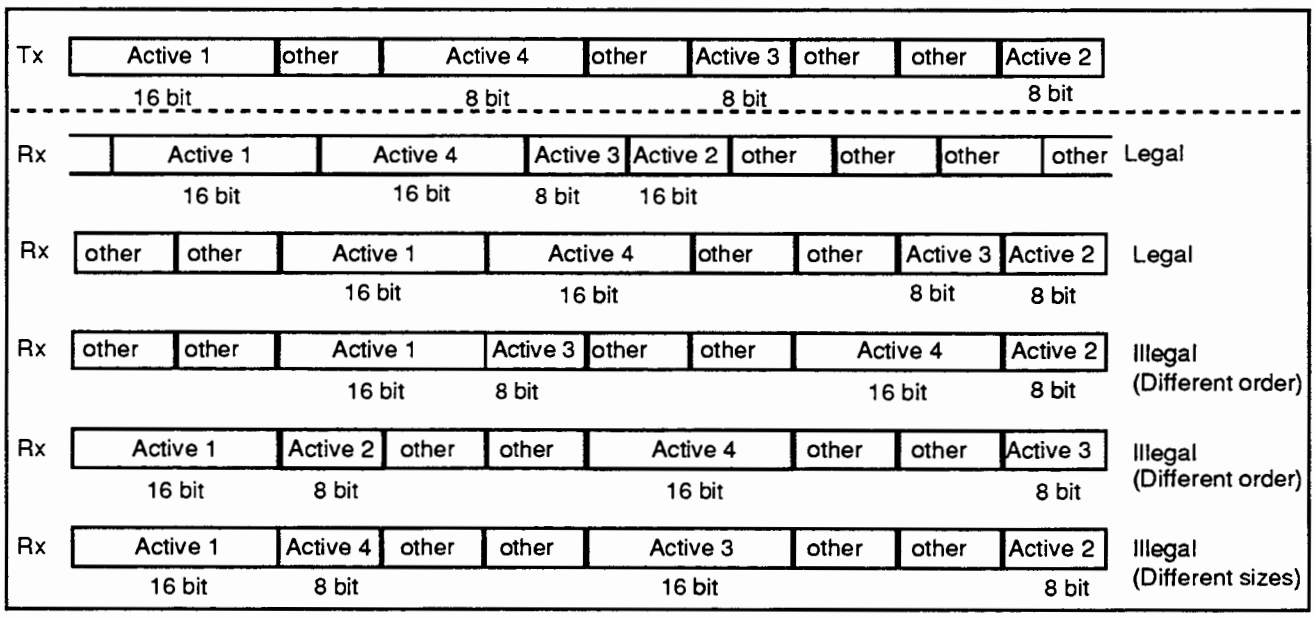


FIG 3 - ACTIVE DATA SOURCES - LEGAL AND ILLEGAL USE

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Rx Bit Skew

Rx bit skew delays the Rx edge timing with respect to the Tx channel. This SERIAL WORKBENCH option is not appropriate for T1/E1 SDS cards, and should **not** be used.

Setting Up

The data resources are initially set up using the **SDS Setup Data Resources** facility, described below. This facility identifies the data protocol used by each resource. Further facilities corresponding to the selected protocol are then used to allocate data buffers to each resource.

SDS SETUP DATA RESOURCES FACILITY

The **SDS Setup Data Resources** facility (**SetupActive**) programs the Active and Control Data resource setups of the Serial Data Sequencer, and identifies the protocols for which they are configured.

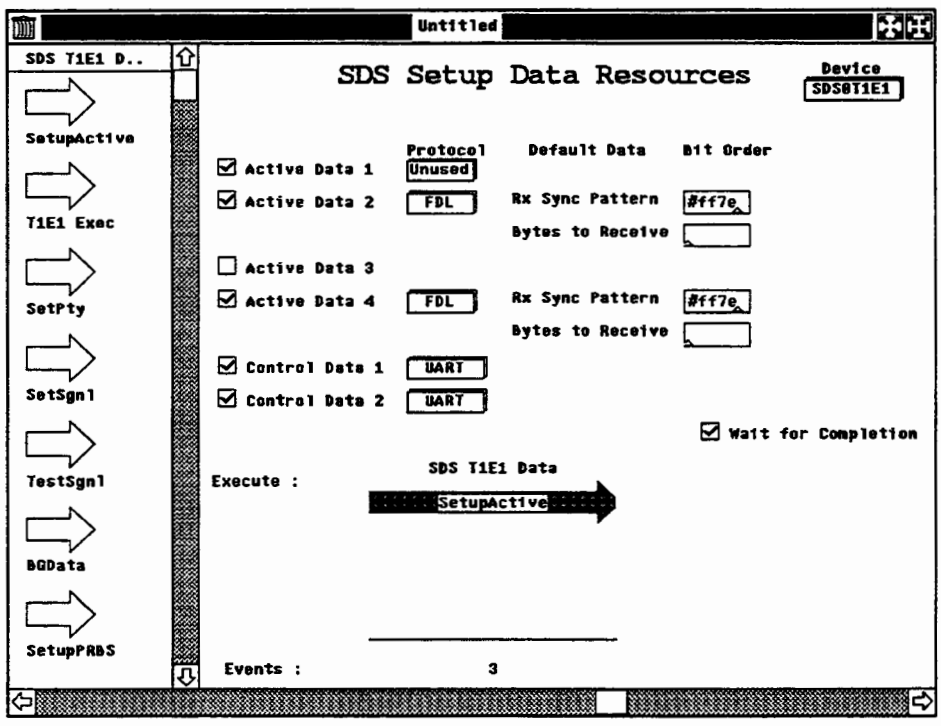


FIG 4 - SDS SETUP DATA RESOURCES FACILITY

SetupActive should occur in the test plan before the Serial Reference icon containing the associated SERIAL WORKBENCH file.

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Active Data

Active Data resources can be configured for

- **PCM**
- **FDL** Active Data 2 and 4, channels 1 and 2 only
- **Unused** the resource is deconfigured

If **FDL** is selected Active Data 2 provides the Facility Data Link data for Line 1 and Active Data 4 the data for Line 2. In this case the resource should not be mapped in Serial Workbench as the data outputs are routed directly into the T1/E1 frame formatting hardware. The data from these resources is then used to supply the Facility Data Link bits at the frame position appropriate to the frame format chosen.

Control Data

Control Data may be configured as

- **Unused** the resource is deconfigured
- **PCM CCS** a transparent 8-bit protocol intended for supplying Common Channel Signaling data
- **UART** used for asynchronous byte-oriented protocols such as RS232

Rx Sync Pattern

In FDL mode data reception begins when a pattern is received matching that entered into the **Rx Sync Pattern** field. Enter a MEDIATOR I expression representing the required sync pattern.

The sync pattern is not included in the receive buffer.

Bytes to receive

Enter a MEDIATOR I expression for the number of bytes to be received, in multiples of 128 bytes. Attempting to receive more than this amount of data (using the ReadMsg facility) will result in reception timing out.

Facilities

Resources set to PCM are programmed to send and receive data using the **PCM Exec** facility. They should have a timeslot mapping defined by SERIAL WORKBENCH.

Data Send and Receive for other formats is accomplished using the **SendMsg** and **ReadMsg** facilities in the **SDS Generic** instrument. Note that resources set to PCM CCS require a timeslot mapping in SERIAL WORKBENCH.

Window

Each resource is selected by checking the box against its name. A multiple choice button is displayed against each selected resource to select the protocol.

Default Data

Default data must be specified if any Active Data resource is set to PCM. Each Active Data resource may have different default data.

The specified data is transmitted as "Idle" code by Active Data resources when their transmit buffer lists are empty. The field specifies 16 bits of data, so the two bytes must be identical if 8-bit timeslots are used.

Default data is entered in the box as a MEDIATOR `I` expression, which may be the name of a MEDIATOR `I` variable or a constant. The expression is evaluated at runtime, unless a constant is used.

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Bit Ordering

The data in a PCM **Active Data** resource may be transmitted LSB first or MSB first. The Bit Ordering button is used to select the order.

Control Data is transmitted LSB first.

Use

- Choose the SDS **instrument** to receive the command, using the **Device** tool. The hardware state of unselected resources is not changed.
- Select the **resources** to program, and their **protocols**.
- Enter a MEDIATOR `I` expression for the **default** data for Active data resources.
- Choose the **order** in which the bits within an Active Data resource slot will be transmitted.
- Check the **Wait for Completion** box if required.

SDS EXECUTE ACTIVE DATA FACILITY

The **SDS Execute Active Data** Facility (**T1E1 Exec**) loads a Transmit and /or Receive list of array processor buffers into the Serial Data Sequencer and starts the sequence running. The driver functions called by the facility transfer data to and from the Array Processor as necessary.

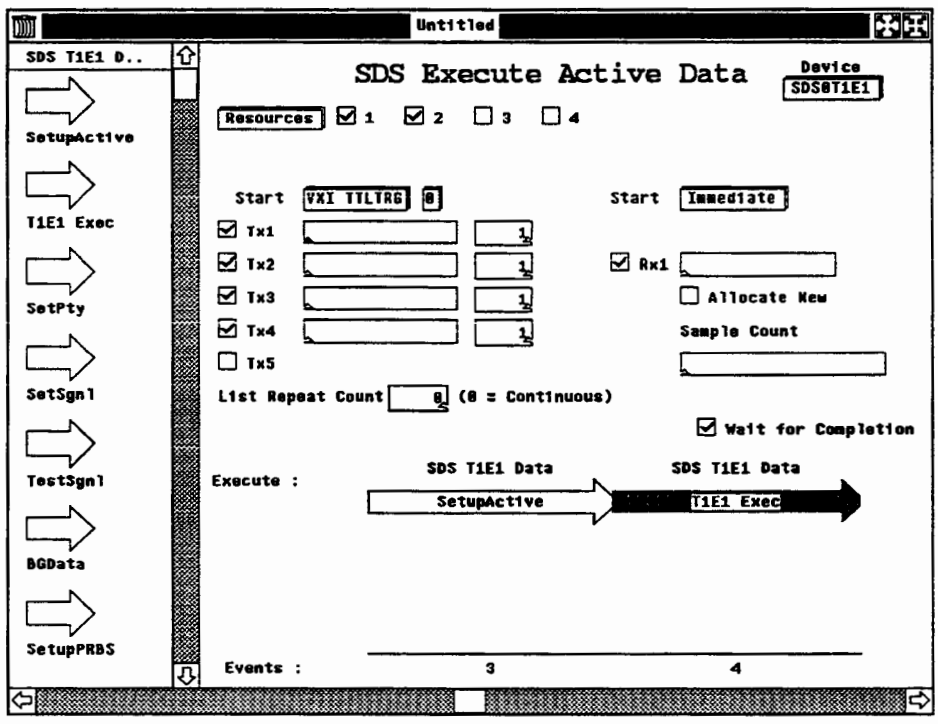


FIG 5 - SDS EXECUTE ACTIVE DATA FACILITY

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Up to five transmit buffers (Tx1 to Tx5) and one receive buffer (Rx1) may be selected for mapping into a Tx or Rx data stream. Within the Tx list, each buffer may be inserted more than once, and the complete sequence may be looped.

Each buffer may be mapped in sequentially up to 65535 times, and the entire list may also be looped up to 65535 times, or continuously. Each buffer may contain up to 16384 bytes. A named buffer may be used in more than one location.

Rx operation is similar, although only one buffer may be used.

Potentially very long data streams can be obtained from this facility. The amount of data used in any frame or superframe is controlled and limited by the SERIAL WORKBENCH.

Active Data Resources

The bit stream created by SDS Execute Active Data may be routed to any of the programmed data resources by selecting the Resources multiple choice button, and checking the box alongside the required resource(s). The resources shown correspond to the PCM Active Data resources set up with the Setup Data Resources facility. Data is loaded and executed only for the channels which are checked.

Resource Mode

The facility may be used to set up active data sources as follows. During any one event:

- One active resource may be selected if Rx is enabled, since only one Rx data buffer is available. Rx is automatically deselected if more than one active resource is enabled.
- More than one active data source may be selected if only Tx data buffers are programmed.

Active data resources may be individually programmed with different buffers on subsequent events.

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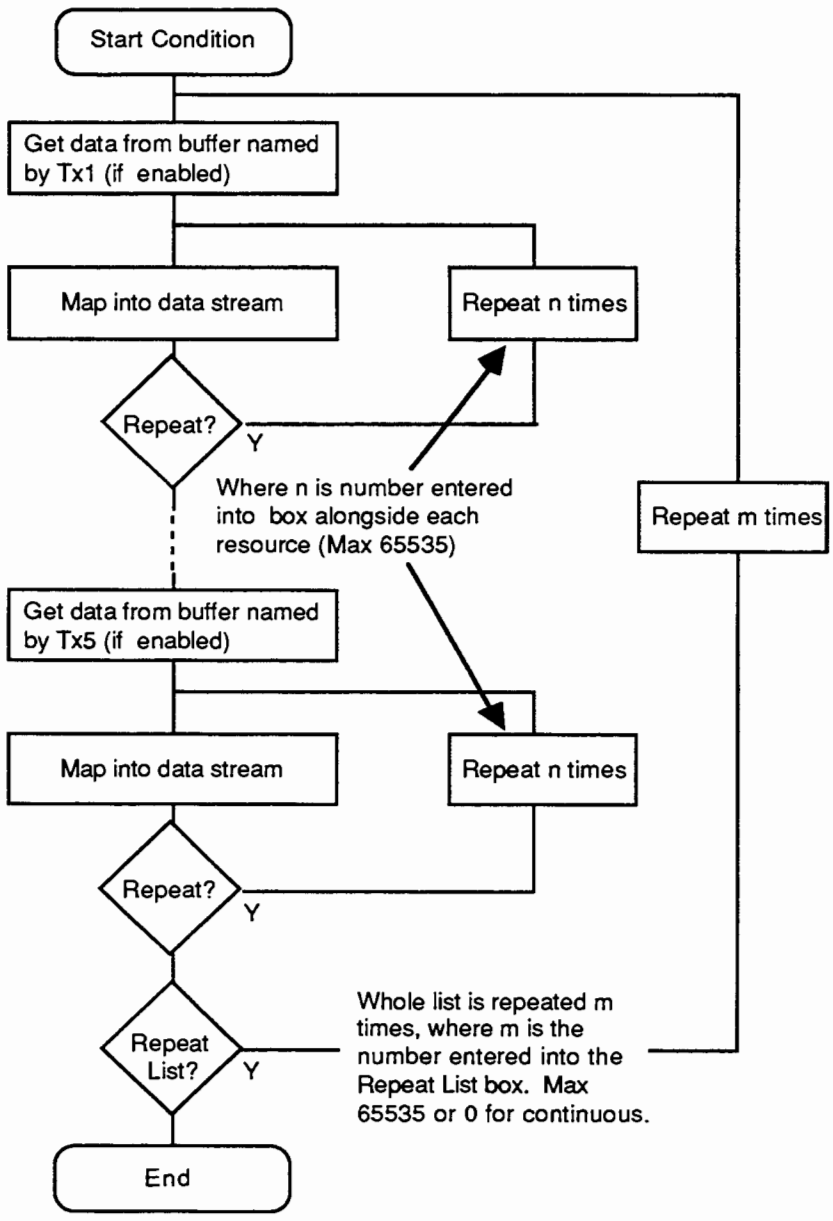


FIG 6 - DATA STREAM CREATION

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Concurrent mode

Concurrent mode is selected by clicking on the Resource button to change it to **Concurrent**. Concurrent testing is described in more detail in the TELECOM WORKBENCH documentation.

Concurrent mode allows more than timeslot to be simultaneously tested. Active data from each resource is mapped into a different timeslot in the t1/E1 frame.

In concurrent mode the checkboxes for resource mapping are not displayed. The resources to be programmed are determined by the current value of CONCURRENCY and BASE_CHANNEL, assuming the following default mapping :

User Channel 0 = Active Data 1	User Channel 4 = Active Data 1
User Channel 1 = Active Data 2	User Channel 5 = Active Data 2
User Channel 2 = Active Data 3	etc.
User Channel 3 = Active Data 4	

Mapping can be changed using the **SDS Map** facility.

The CONCURRENCY and BASE_CHANNEL variables are described in the TELECOM WORKBENCH documentation.

Buffers

Tx and Rx buffers must initially be allocated using the Array Processor MSPAllocate facility before they can be used by other facilities.

Tx Buffers

The selections Tx 1-5 represent the **TX data buffers**, in the order in which they are mapped into a bit stream. Each buffer is enabled by checking the box next to its title.

A text entry box is displayed next to each selected buffer. The name of a previously allocated **Array Processor buffer** must be typed into this box. Any valid buffer name may be assigned to any of the Tx buffers.

The TELECOM WORKBENCH checks that a syntactically correct name has been assigned when the event is closed. The program checks at runtime that the Array Processor buffer exists and has been correctly set up.

A further numeric entry box is displayed, after the text entry box. A repeat count in the range 1 to 65535 may be entered. Zero is not valid. To obtain zero insertions, deselect the buffer by clicking again on the check box.

For PCM protocol , buffers in the Transmit list must contain **time domain data** in MSP_INT format. The maximum buffer length is 16384 samples.

Rx Buffer

A single **Rx buffer** may be specified for reading data from the Serial Data Sequencer. The buffer is loaded with time domain data in MSP_INT format from the Rx data stream.

Default Data

If no transmit or receive list is specified, the current operation on the specified resources is aborted and **Default Data** is transmitted.

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Start

The **start** condition may be selected using the Start choice button. Tx and Rx start are selected separately. The choices available are:

Tx:	Immediate	
	VXI TTLTRG	(VXI TTL trigger 0-7)
Rx:	Immediate	
	VXI TTLTRG	(VXI TTL trigger 0-7)
	Pattern	
	Sync to Tx	

Immediate indicates the transmission and Rx capture start as soon as the event is encountered at runtime.

When **VXI TTLTRG** is selected, a further choice button is displayed to allow backplane VXI trigger line to be selected. Tx and Rx start may use different triggers.

Selecting **Pattern** (Rx only) causes a further text entry box to be displayed. Type in a MEDIATOR I expression evaluating to a sixteen bit pattern. Rx capture will start immediately after the pattern has been detected in the Rx data stream.

Note The first eight bits of the search pattern are not included in the capture. However, the second eight bits **are** included in the captured data.

Sync to Tx displays a radio button next to each selected Tx buffer. Click on the radio button to select the start buffer. Rx capture starts as soon as execution of the indicated TX buffer begins.

Repeat Count

A repeat count for the whole list may also be specified in the **List Repeat Count** box. A value of 0 to 65635 may be entered, where zero represents repeat Tx continuously.

Requirements

The following conditions must be set up in the test program prior to the SDS Execute Active Data Facility being used:

- The appropriate Active Data resources must have been programmed for PCM (described above).
- The Tx Buffers must have been allocated and initialized and the Rx Buffer must have been allocated (Array processor).
- In concurrent mode, the values of CONCURRENCY and BASE_CHANNEL must have been initialized.

Use

General:

- Choose the SDS **instrument** to receive the command, using the **Device** tool.
- Select **Resource** or **Concurrent**, as required.
- Enable the **Active Data** Resource(s) to be used by checking the corresponding box(es) - only one if Rx will be enabled.

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- Check the **Wait for Completion** box if required.

Transmit:

- Select the required **Tx Start** event. Select the trigger line if starting from a VXI trigger.
- Enable the **Tx Buffers** that you wish to use. Enter the data buffer name and repeat count for each selected buffer.
- Enter a **repeat count** for the whole **Transmit list**. A count of 0 means repeat continuously.

Receive:

- Enable the **Rx buffer**, if required. Enter the name of the data buffer to receive captured Rx data from the UUT.
- Select the **Rx Start** event.
  - Select the trigger line if starting from a **VXI trigger**.
  - Select the start Tx buffer, if **Sync to Tx** is selected.
  - Enter a MEDIATOR I expression for the start pattern, if **Pattern** is selected.

BACKGROUND DATA SELECTION FACILITY

The **BackGround Data Selection facility** (**BGData**) provides control over which resource is switched onto the data highways at run time. The values of each of the background data resources are programmed using SERIAL WORKBENCH.

If the checkbox for a highway is not checked the hardware is unchanged.

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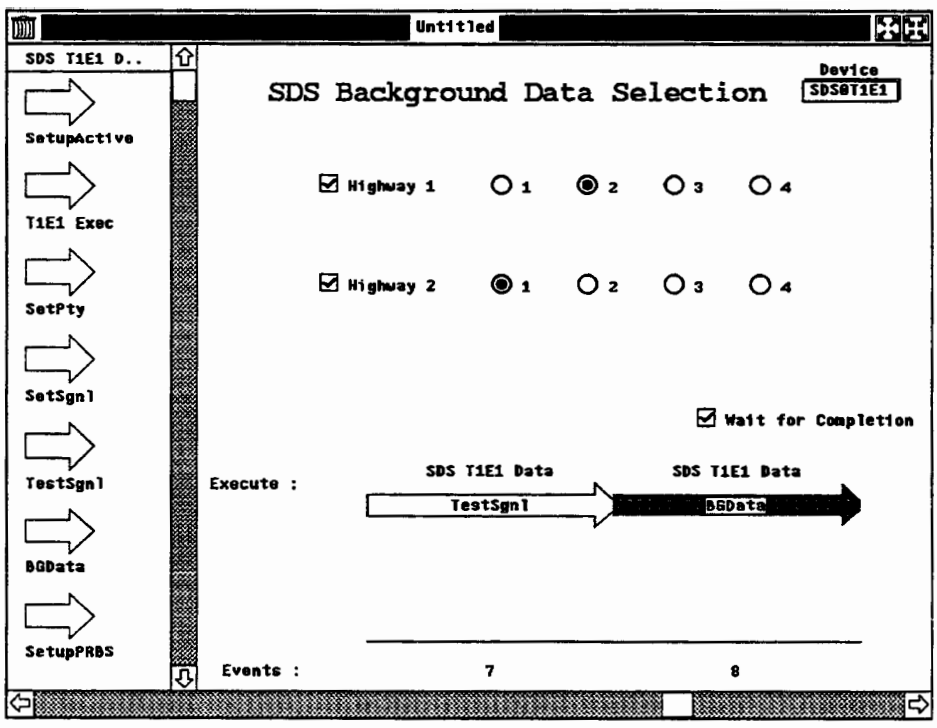


FIG 8 - BACK GROUND DATA SELECTION FACILITY

The Background data resource for each connected Data Highway is selectable by radio buttons, labeled 1 to 4.

Use

- Choose the SDS instrument to receive the command, using the **Device** tool.
- Select the **highways** for which the background data source is to be changed.
- Select the background data resource to be used, for each selected highway.
- Check the **Wait for Completion** box if required.

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RXERRORS FACILITY

The **RxErrors facility (RxErrors)** allows the T1/E1SDS error count registers to be read and tested. Each T1/E1line interface has two sets of error count registers, those associated with the frame formatting hardware devices and those associated with the PRBS detectors.

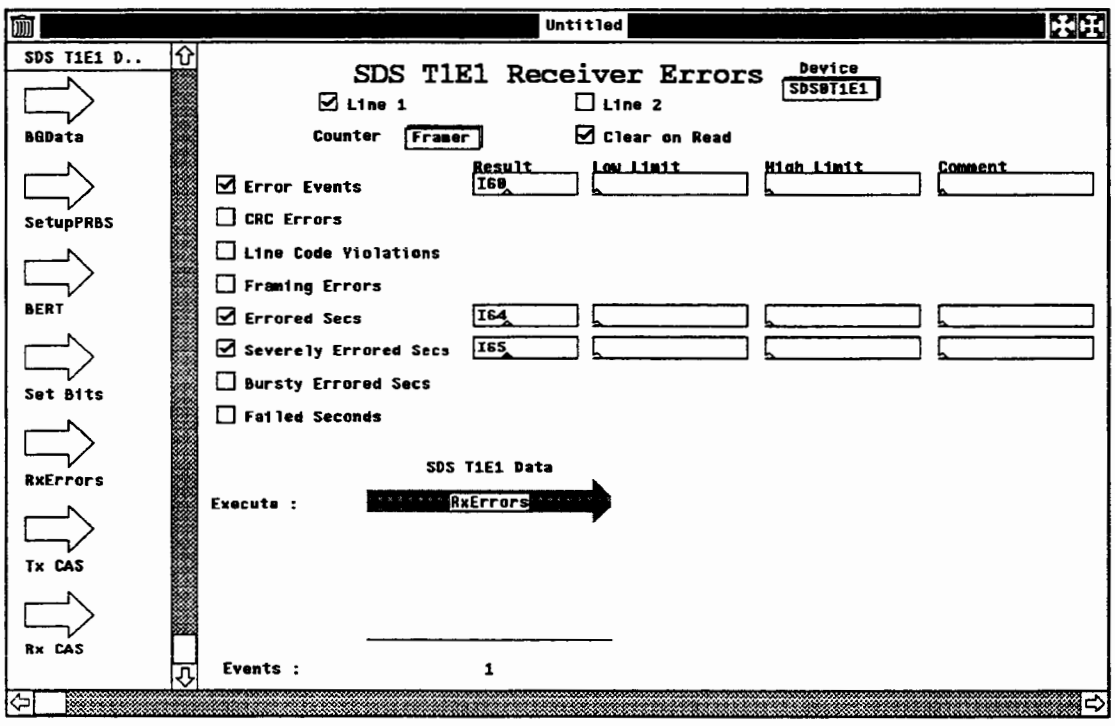


FIG 9 - **RXERRORS FACILITY**

Some **error types** may only be measured by the Framer counters, as shown in the following table.

For each error type, specify an `I` **variable** to receive the result, an `I` **expression** for the error count test limit and a **Comment** string to be displayed in the results log. Default values for the **result** `I` variables are defined by the following TWB.defaults entries:

Type	TWB.defaults entry	Measured By:
Error Events	SDS_ERROR_EVENTS	Both
CRC Errors	SDS_CRC_ERRORS	Framer only
Line Code Violations	SDS_BPV_ERRORS	Framer only
Framing Errors	SDS_FRAMING_ERRORS	Framer only

(Continued overleaf)

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Type	TWB.defaults_entry	Measured By:
Errored Seconds	SDS_ES_COUNT	Both
Severely Errored Seconds	SDS_SES_COUNT	Both
Bursty Errored Seconds	SDS_BES_COUNT	Framer only
Failed Seconds	SDS_FS_COUNT	Framer only

Line 1 & Line 2

Select which of line 1 or 2 will be read. Since both lines cannot be read at the same time, only one line may be read in a specific event.

Counter

The **Counter** button selects whether the error counters in the framer hardware are read (**Framers**) or whether the PRBS error counters are used (**Rx Data**).

Clear on Read

The error counters used can be set to zero following the read operation by selecting **Clear on Read**. All selected counters are cleared.

Errors

Each of the eight errors type may be tested during the same event, depending on the Counter selected. When an error counter is selected, four new fields are displayed for the result, high and low limits and comment.

Field	Expected Entry
Result	MEDIATOR `I` variable
Low Limit	MEDIATOR `I` expression
High Limit	MEDIATOR `I` expression
Comment	Text

It may be necessary to resize the window to display the **Comment** fields.

Use

- Choose the SDS instrument to receive the command, using the **Device** tool.
- Select the required **line** for which the error data will be read.
- Select whether the counter value will be **cleared** after the read operation.
- Select the error counts to be read.
- For each selected error type, enter a MEDIATOR `I` variable for the result and MEDIATOR `I` expressions for the limits.
- For each selected error type, enter a **comment** string to be displayed in the results log, if required.

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INTRODUCTION

A Bit Error Rate test may be carried out using the Pseudo Random Binary Sequence (PRBS) generators and detectors available on the SDS card. Any SDS card identified in the System Description file can be used, and types may be mixed in the same event. SDS cards configured for T1/E1 operation have a single Pseudo Random Binary Sequence (PRBS) generator and two detectors available.

The displayed options vary according to the type of SDS selected. Options for other SDS types are described in the documentation relating to that card type.

Synchronization

PRBS detectors require a sequence of 64 error-free bits to synchronize to the generator output. Error counting does not begin until synchronization has been achieved. A runtime error occurs if synchronization is not achieved within a specified time.

Error Count

A maximum of 65335 errors may be counted in a single test.

SDS BIT ERROR RATE TEST FACILITY

The **SDS Bit Error Rate Test Facility** (**BERT**) selects and sets up the Pseudo Random Binary Sequence (PRBS) generators and detectors.

Up to six generators may be selected in a particular event. An error message is displayed when the window is closed if any invalid selection was made, for instance programming the same generator to two different patterns.

Note that not all tools are visible with the window at its default size. It may be necessary to resize the window to display all the tools.

PRBS GENERATOR

The list of generators is taken from the compiled System Description file in the test database. Any available generator may be selected. Selecting the same generator more than once will result in an error message on leaving the event.

Pattern

The following patterns are available when a T1/E1 SDS card is selected:

- 15 bit (2^{15})
- 20 bit (2^{20})
- fixed 0
- fixed 1
- alternate 0/1
- 11 bit (2^{11})

The pattern selector sets the pattern on the generator and the associated detector or detectors. It is not necessary to use the detector associated with a specific generator to receive data from that generator, although the detector used must be set to the same pattern.

Not all polynomials are available for all SDS types. The selected pattern must be available on the corresponding detector.

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Zero Suppression Zero suppression as ITU-T O.151/152 may be selected for the 2^{11} and 2^{20} polynomials. A separate check box labeled **ZS** is displayed when these polynomials are selected. Check the box to enable zero suppression on the selected generator.

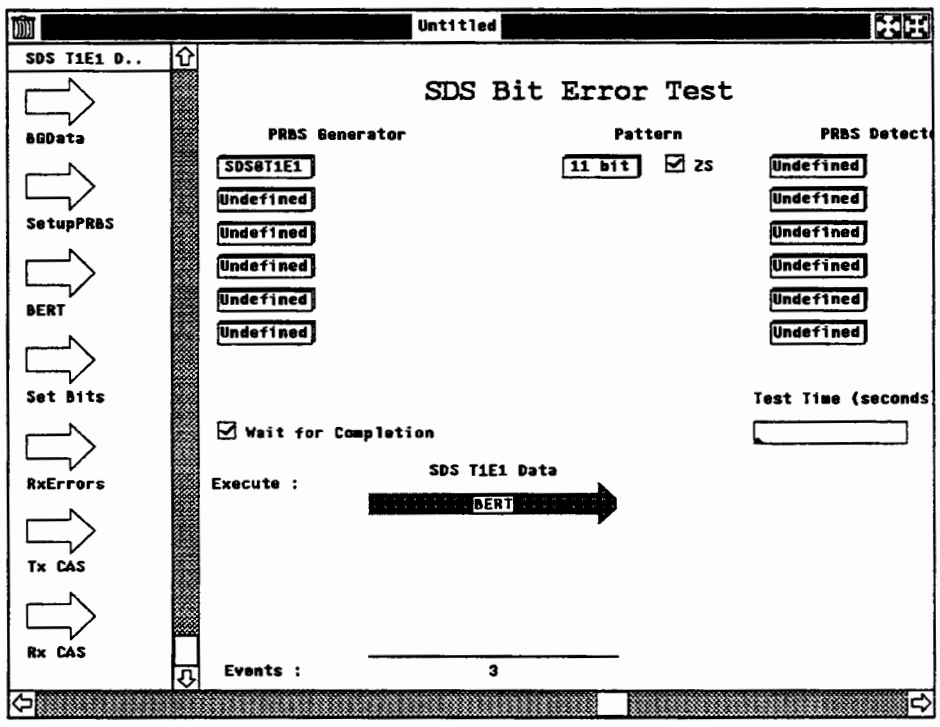


FIG 10 - SDS BIT ERROR RATE TEST FACILITY - GENERATORS

DETECTOR The list of detectors is similarly taken from the compiled System Description file. Any available detector may be selected. The **PRBS Detector** tool selects the SDS card containing the detector circuit to be used.

Line The **Line** selector determines which detector is used on the selected card and may be set to **Both Lines**, **Line 1** or **Line 2**.

Limit Enter a MEDIATOR I expression for the maximum permitted bit error count, for each detector used.

Place Result in Enter the name of a MEDIATOR I variable to receive the bit error count at the end of the test. The default value for this variable is specified by the TWB.defaults entries SDS_BERT_RESULT/2/3/4/5/6. Where the detector is set to **All lines** the specified I variable is the base for line 1.

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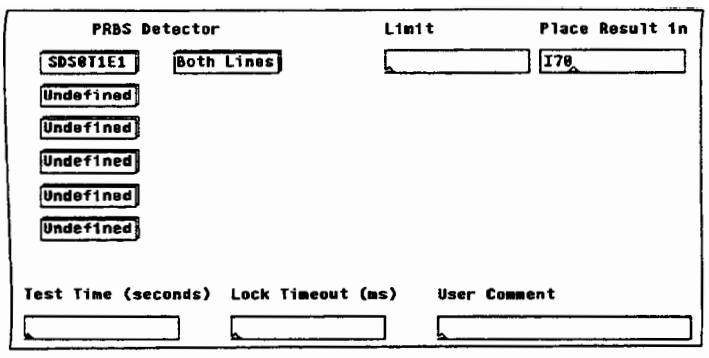


FIG 11 - SDS BIT ERROR RATE TEST FACILITY - DETECTORS

GENERAL CONTROLS The following fields set the test time and limits, and the time allowed for synchronization in a particular test.

Test Time Enter a MEDIATOR I expression evaluating to a number in the range 0 to 32767 representing the required test time in **seconds**. The test time period begins when the detector successfully synchronizes to the generator.

Lock Timeout **Lock Timeout** defines the time that a detector will wait to synchronize to the pattern from a generator, in **milliseconds**. Enter a MEDIATOR I expression evaluating in the range 0 to 32767. A run time error will occur if synchronization is not achieved within this time.

User Comment An optional user comment may be entered as an ASCII string. The comment will be displayed in the results log.

Wait for completion **Wait for Completion** is displayed when only generators are selected, and is suppressed when any detectors are selected.

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Use

- Choose the SDS instrument(s) to act as the PRBS **generator**(s) for the test, using the **PRBS Generator** tool.
- Choose the SDS instrument(s) to act as the PRBS **detector**(s) for the test, where required, using the **PRBS Detector** tool.
- Select the Lines and/or Circuits to be used. for each selected instrument.
- Select the data **pattern**(s) to be used. Enable zero suppression if required, where it is available for the selected pattern.
- Enter MEDIATOR `I` expressions for the test time, lock timeout and limit.
- Specify a MEDIATOR `I` variable for each detector used, to receive the bit error count **result** (or use the default variable).
- Enter a User **Comment** if required, for each detector used.
- Check the **Wait for Completion** box if required (generators only).

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INTRODUCTION

The Serial Data Sequencer has four byte wide and eight bit wide Transmit signaling registers and four Receive signaling registers per highway, which may be programmed independently of the execution of the Active Data Resources.

TX SIGNALING REGISTERS

The Tx signaling registers are programmed using the **Set Tx Signaling Resource** facility (**SetSgnl**). The registers to be programmed may be selected Individually or Concurrently using the **Signaling Resources** button.

If **Concurrent** programming is selected, the registers corresponding to User Channels from:

BASE_CHANNEL to BASE_CHANNEL+CONCURRENCY-1

are programmed. The mapping from User Channels to physical register numbers should have been set up, using the **SDS Map** facility, and the values of BASE_CHANNEL and CONCURRENCY should have been initialized.

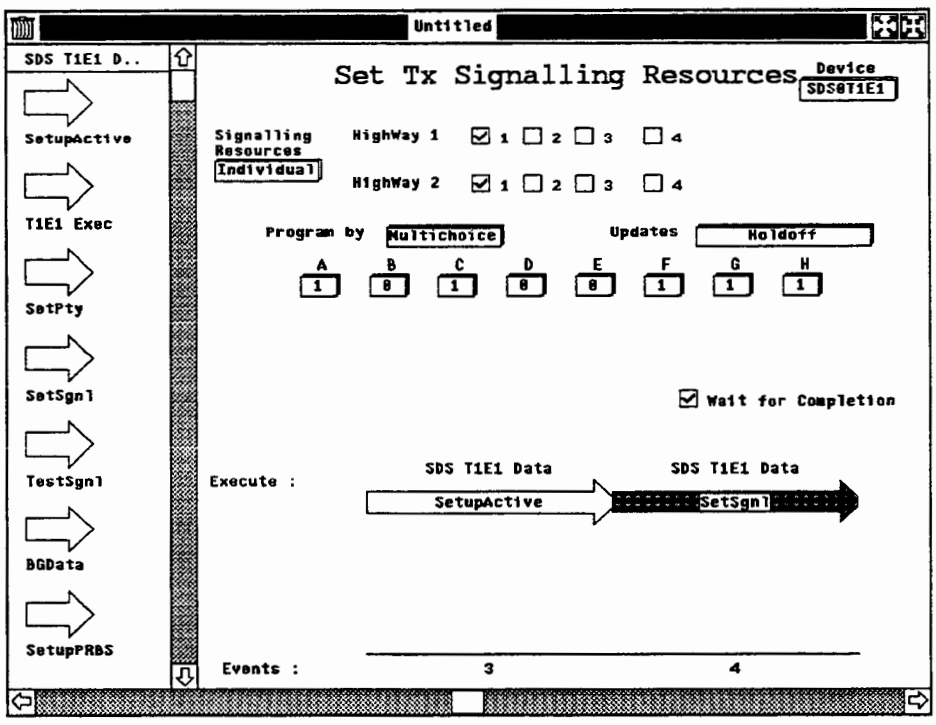


FIG 12 - SET TX SIGNALING RESOURCE FACILITY WINDOW

Different data can be programmed into different registers on subsequent events.

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Bit Order Bit A is transmitted first, and Bit H last. If the resource envelope in the SERIAL WORKBENCH is less than 8 bits, the rightmost bits are ignored.

Program By The Tx data can be explicitly set using multichoice buttons to define each data bit, or programmed using a MEDIATOR expression. Selection is made using the **Program by** button.

Updates The **Updates** button selects the point in the SERIAL WORKBENCH at which the register data is updated. The options are:

- Holdoff
- End of Timeslot
- End of Frame
- End of Superframe
- SWB SubMultiframe

If **Holdoff** is selected, the registers are not updated until the update mode is reprogrammed to one of the other choices.

Use

- Choose the SDS instrument to receive the command, using the **Device** tool.
- Select the required **Signaling Resources** 1 to 4 on highway one and/or two by checking the corresponding box.
- Choose the value (1 or 0) for each bit A to H.
- Check the **Wait for Completion** box if required.

SET BITS FACILITY The **Set Bits facility** (**Set Bits**) programs the two Single Bit signaling registers. The registers are 8 bits wide, and each bit may be mapped **individually** by SERIAL WORKBENCH.

Register Updates The **register update** point may be selected to be Immediate, at the end of the SERIAL WORKBENCH timeslot, frame or superframe, or on the occurrence of the SERIAL WORKBENCH SubMultiframe marker.

Line 1 & Line 2 The Line checkboxes are used to select which line or lines are to be programmed. If a line is not selected its hardware state is not changed.

Program By The bit values for each line may be programmed by multichoice tools or by MEDIATOR `I` expression, selected using the **Program By** button.

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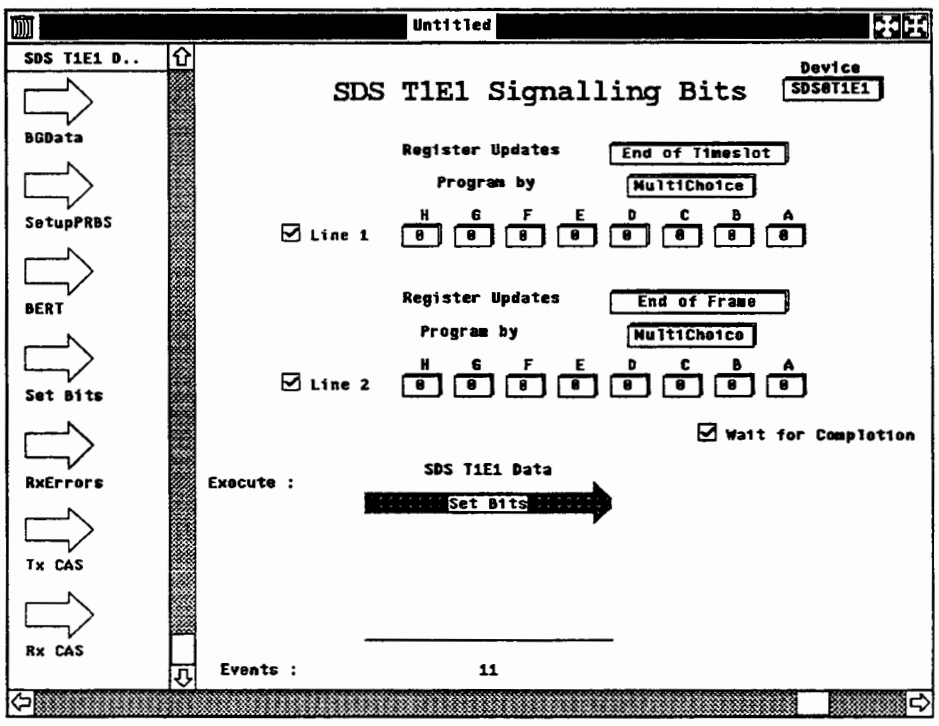


FIG 13 - SET BITS FACILITY

Use - General

- Choose the SDS instrument to receive the command, using the **Device** tool.
- Select the point in the SERIAL WORKBENCH superframe at which the register contents will be updated.
- Check the **Wait for Completion** box if required.

For Each Line

- Select the **checkbox** for the line, if its status is to be changed.
- Select the programming method, Multichoice or MEDIATOR expression.
- For Multichoice, choose the value (1 or 0) for each bit A to H of the register.
- For Expression, enter the name of a MEDIATOR `I` variable containing the signaling data.

RX SIGNALING RESOURCES

The Serial Data Sequencer has four Receive signaling registers per highway which may be read independently of the execution of the Active Data Resources. The **Test Rx Signaling Resources** Facility (**TestSgnl**) reads the registers and tests the value against a user defined bit pattern.

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Resources

Resources may be programmed individually by physical register number, in which case only the selected channels are tested, or Concurrently in which case the registers tested depend on the SDS resource mapping and concurrency control variables

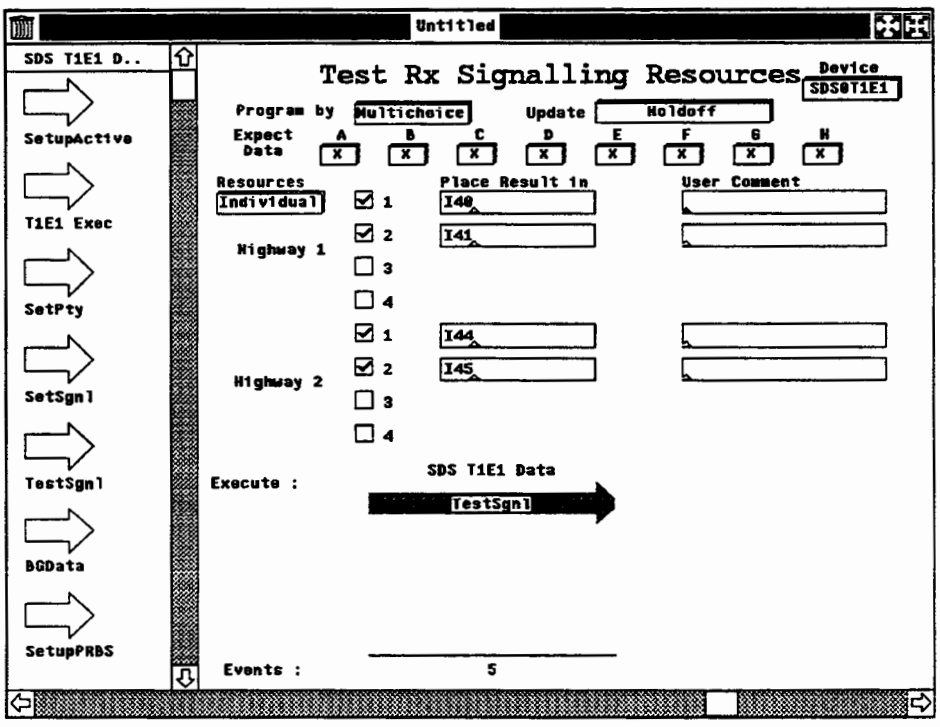


FIG 14 - TEST RX SIGNALING RESOURCES FACILITY WINDOW

If **Concurrent** resource programming is selected, the registers corresponding to User Channels from BASE_CHANNEL to BASE_CHANNEL+CONCURRENCY-1 are programmed.

The same test is applied to all selected registers.

Program by

The expected data is selected with the **Program by** tool, which has two options, Multichoice and Expression.

Multichoice Eight choice tools labeled A to H are used to program the data for each bit to 0, 1 or X (Don't Care). Choose the expect data for each signaling bit.

Expression Enter two MEDIATOR `I` expressions representing the expected data and the Don't Care mask. The expressions must evaluate to numbers in the range 0 to 255. When using expressions, only those bits of the mask expression which are set (i.e. "1") are tested.

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Updates

The **Updates** button selects the point in the SERIAL WORKBENCH at which the register data is updated. The options are:

- Holdoff
- End of Timeslot
- End of Frame
- End of Superframe
- SWB SubMultiframe

If **Holdoff** is selected, the registers are not updated until the update mode is reprogrammed to one of the other choices.

This facility may be used to simply read the registers without carrying out a test. Each bit of the expected data must be set to don't care (X) in Multichoice mode, or the expression boxes left blank in Expression mode.

Defaults

The **defaults** are defined as:

RX_SIG_RES_1 to 8, where:

RX_SIG_RES_1 to 4 apply to Highway 1 registers 1 to 4.

RX_SIG_RES_5 to 8 apply to Highway 2 registers 1 to 4.

The names of the default variables are automatically loaded in to the boxes when the facility is first opened, if any have been defined. You can replace the default names with other variable names by typing the new names into the boxes.

Note that default names are only loaded when the facility is first opened. The names are not updated if the defaults file is subsequently altered.

It is not necessary to use a different variable for each register if **Expected data** has been defined. At least one variable name must be given, but the same variable may be used for all registers if subsequent examination is not required.

Place Result in

A MEDIATOR `I` variable **must** be specified for each selected register. The variable is used to store the result and used internally by the facility. Each variable will contain an image of an Rx signaling register in its least significant byte.

Enter the name of a MEDIATOR `I` variable to store the result or use a default variable identified in the TWB.defaults file.

The value appearing in the variables is the received data with all Don't care bits set to zero (after ANDing with the Care/Don't Care mask). If the resource envelope in the SERIAL WORKBENCH is less than 8 bits, the right most bits of expect data are ignored.

Channel Mapping

The mapping from User Channels to physical register numbers is programmed by the **SDS Map** facility. If a mapping other than the default is required, it must have been programmed in a previous SDS Map facility.

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Update

The **Update** tool selects the point in the SERIAL WORKBENCH at which the register data is updated. "HoldOff" implies that the registers are not updated until the update mode is reprogrammed to one of the other choices. If the expect data is set to all "X" in Multichoice mode, or the Expect Data and Mask Data fields are left blank in Expression mode, the update point may be programmed independently of performing any tests.

Comment

An optional user comment may be entered into the **User Comment** box. The comment will be displayed in the test results when the test program is run. Any alphanumeric or punctuation character except quotation marks may be used.

Use

- Choose the SDS instrument to receive the command, using the **Device** tool.
- Select the resources to be tested, for each highway. Only the checked channels are tested.
- Select the update point with the **Update** tool.
- Enter the name of a MEDIATOR `I` variable to store the result, in the **Place Result in** box, or retain any default name.
- Enter a test results log comment in the **User Comment** box, if required.

Multichoice Mode

- Choose the value (1 or 0) for each bit A to H of the **Expect data** for each signaling bit. X = Don't Care.

Expression Mode

- Enter the name of a MEDIATOR `I` variable containing the expected data.
- Enter the name of a MEDIATOR `I` variable containing a bit mask to define which bits of the selected registers will be tested.

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TX CHANNEL ASSOCIATED SIGNALING FACILITY

The **Tx CAS facility** (**Tx CAS**) programs the per channel transmit signaling registers used for Channel Associated Signaling. This applies to 2, 4, or 9/16-state robbed bit signaling for T1 frame formats, or PCS0, PCS1 and IRSM signaling modes for CEPT frame formats.

Frame Setup

The Frame and Signaling formats for the selected device should have been previously programmed using the **FrameSetup** facility. The number of registers shown depends on the device mode set in the FrameSetup facility.

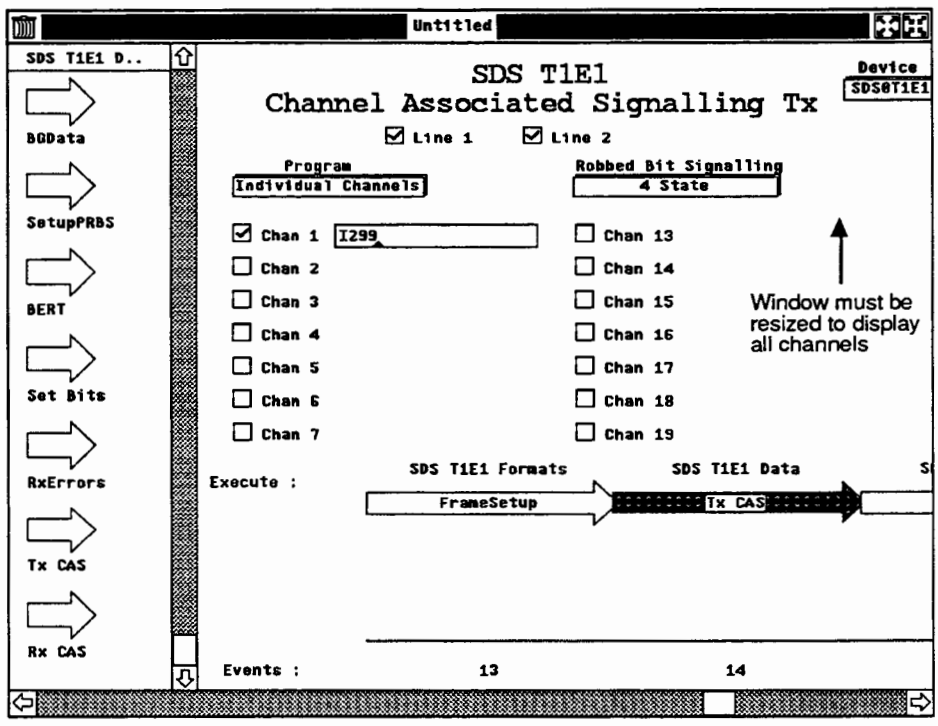


FIG 15 - TX CAS FACILITY

Registers

The signaling **registers** for the selected interface(s) can be programmed individually or all set to the same value using this facility.

Programming

Either line interface may be **programmed** during a specific event. Registers for both interfaces may be programmed at the same time only if line interfaces have been programmed to compatible frame formats and signaling schemes.

An error message is displayed if both interfaces are programmed under inappropriate conditions. One of the lines must then be deselected and programming constrained to one interface.

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Channels

Any combination of the available channels may be selected for programming by checking the corresponding box. A further field is displayed for a MEDIATOR I expression defining the data to be programmed into that channel register.

The number of channels displayed depends on the frame format settings made in the Frame Setup facility. The window must be **resized** from the default size to display all channels:

SF formats	channels 1 to 12
ESF formats	channels 1 to 24
CEPT formats	channels 0 to 31

Robbed Bit Signaling

The **Robbed Bit Signaling** options available depend on the settings made in the Frame Setup facility. Different events must be used to program different signaling modes.

The Robbed Bit Signaling **Transparent** option allows a mixture of Robbed Bit Signaling and Transparent signaling to be set up if Robbed Bit Signaling was previously selected in the Frame Setup facility.

Channels set to Transparent ignore the given I expressions.

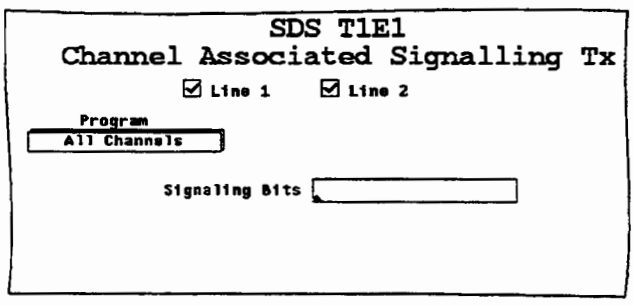


FIG 16 - TX CAS FACILITY "ALL CHANNELS" SELECTED

Use

- Choose the SDS instrument to receive the command, using the **Device** tool.
- Select the required **line** or lines to be programmed.
- Select whether the registers will be programmed individually or all set to the same value.
- If using Robbed Bit Signaling, select whether 2, 4, or 9/16 state signaling will be used.
- For each selected channel enter an I expressions for the register data.
- Select the channel(s) to be programmed.
- Check the **Wait for Completion** box if required.

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RX CHANNEL ASSOCIATED SIGNALING FACILITY

The **Rx CAS facility (Rx CAS)** tests the per channel receive signaling registers used for Channel Associated Signaling. This applies to 2, 4, or 9/16-state robbed bit signaling for T1 frame formats, or PCS0, PCS1 and IRSM signaling modes for CEPT frame formats.

Frame Setup

The Frame and Signaling formats for the selected device should have been previously programmed using the **FrameSetup** facility. The number of registers shown in the facility depends on the device mode inherited from the FrameSetup facility.

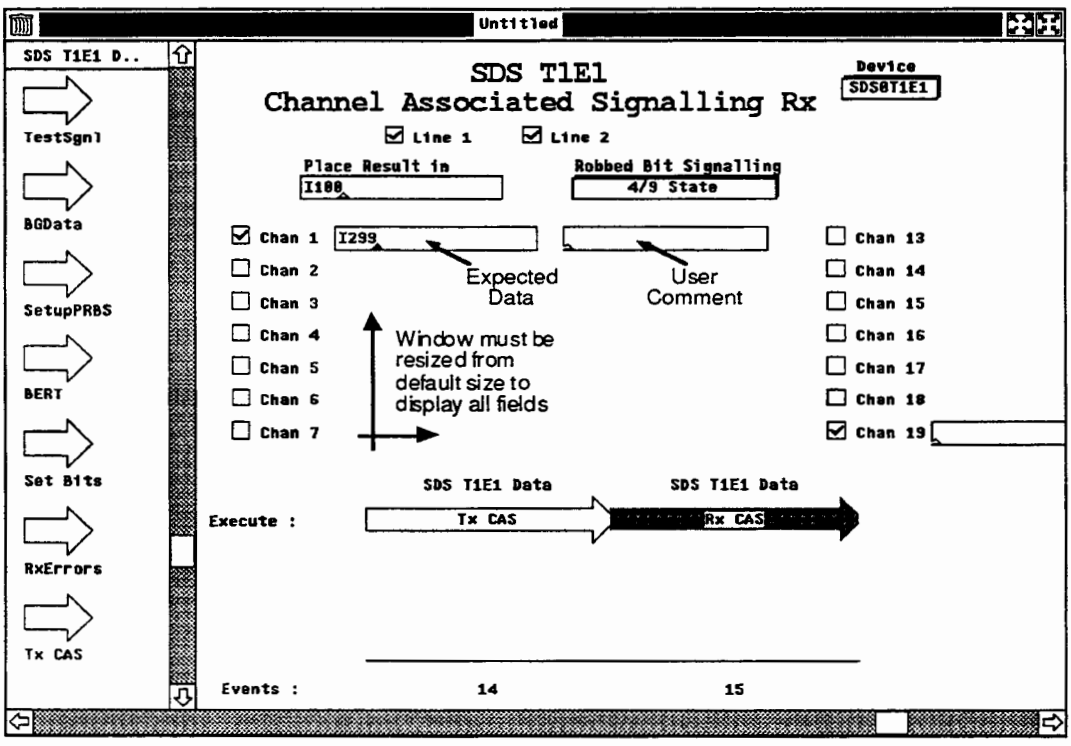


FIG 17 - RX CHANNEL ASSOCIATED SIGNALING FACILITY

Line 1 and Line 2

The **Line** check boxes are used to identify which set of registers will be tested in the current event, since both line interface register sets cannot be read at the same time.

Place Result in

The returned values for each channel are placed in a MEDIATOR `I` variable. Enter the name of the variable to be used in the **Place Result in** field.

The same I variable is used for all channels. On completion the variable contains the data for the highest numbered monitored channel.

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Channels

Any combination of available channels may be tested by checking the corresponding box. A further two fields are displayed for each selected channel.

Enter a MEDIATOR I expression defining the expected data in the first field. The signaling register for this channel is read and tested against the associated MEDIATOR `I` expression.

Comment

Enter a user **comment** in the second field. The comment is displayed in the results log.

Note that it may be necessary to resize the window from its default size to display all available channels.

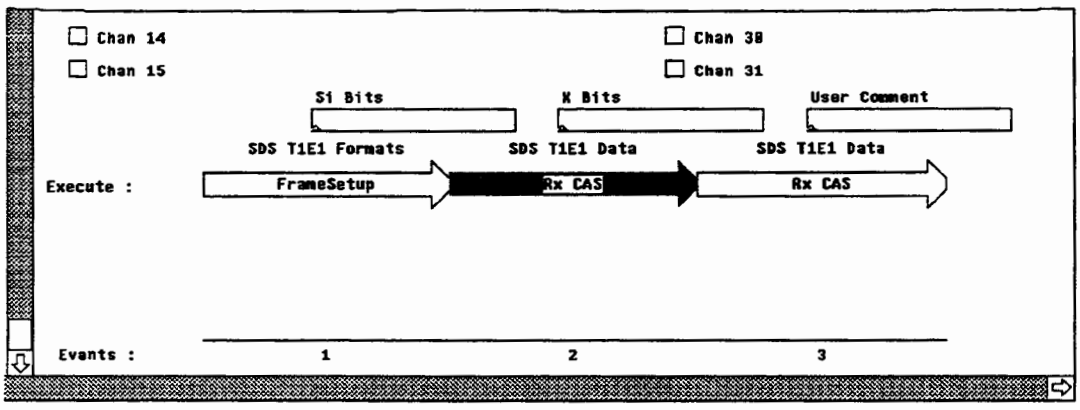


FIG 18 - RX CAS FACILITY - CEPT TOOLS

Si Bits and X Bits

Enter MEDIATOR `I` expressions evaluating to the required Si Bits and X Bits values.

Use

- Choose the SDS instrument to receive the command, using the **Device** tool.
- Select the required **line** or lines to be programmed.
- Select whether 2, 4, or 9/16 state signaling will be used.
- Enter the name of the first MEDIATOR `I` variable containing the expected register data.
- Select the channel(s) to be tested. For each selected channel, enter a MEDIATOR `I` expression defining the expected result.
- Enter MEDIATOR `I` expressions for the Si Bits and X Bits.
- For each selected channel, enter a comment string to be displayed in the results log, if required.

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INTRODUCTION

The **Set TX Parity** facility (**SetPty**) specifies the parity to be applied for each highway when the parity resource is encountered in the SERIAL WORKBENCH. Parity is calculated for internal highways 1 and/or 2 over the Parity Window region selected graphically in the SERIAL WORKBENCH.

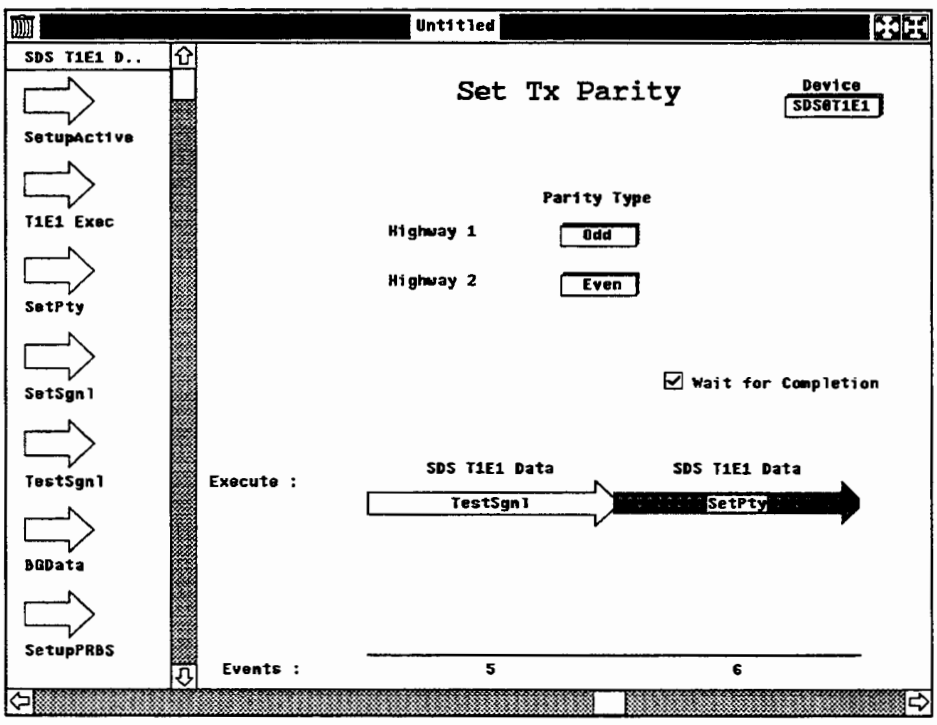


FIG 19 - SET TX PARITY FACILITY WINDOW

Odd or **Even** parity may be selected. **No parity** is obtained by not selecting the parity resource in the SERIAL WORKBENCH.

Use

- Choose the SDS **instrument** to receive the command.
- Select the Parity Type for each highway:
  - Odd Odd Ones parity is generated
  - Even Even Ones parity is generated.
- Check the **Wait for Completion** box if required.

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SECTION 6

LINE I/O AND UART FACILITIES

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LINE I/F FACILITY

The **Line I/F** facility (**Line I/F**) programs the physical interface setting of the T1E1 SDS. The line impedance, various pulse shaping parameters and connection of transmit and receive ports and loopback relays may be set up for each channel.

As usual, any characteristic not programmed in a specific event remains unchanged from previous settings.

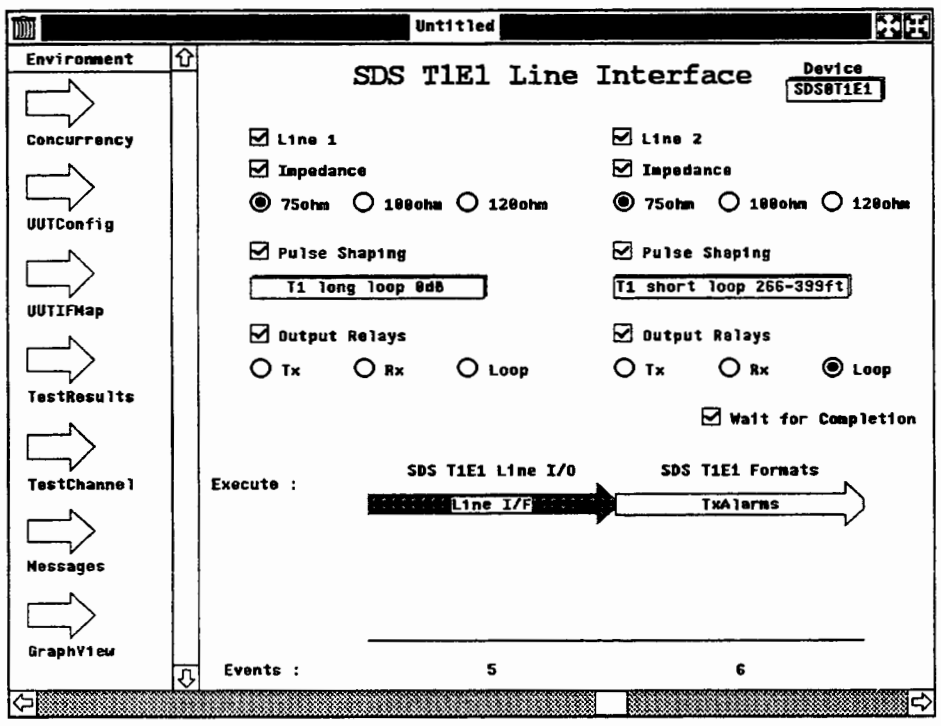


FIG 1 - LINE I/F FACILITY

Impedance

Checking the **Impedance** checkbox determines whether the impedance will be programmed on the current event. The following impedances are available:

- 75ohm single ended coaxial connection.
- 100ohm balanced connection.
- 120ohm balanced connection.

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Pulse Shaping

Select **Pulse Shaping** if required to program the pulse shaping hardware. A choice button is displayed, with the following options:

T1 long loop 0dB
T1 long loop -7.5dB
T1 long loop -15dB
T1 short loop 133-266ft
T1 short loop 266-399ft
T1 short loop 399-533ft
T1 short loop 533-655ft
CEPT

Outputs

The Tx and Rx channels are isolated from the front panel by relays. Select the **Outputs** box to program the relays, then the appropriate radio button to set the relay state. If the radio button is not selected, the relay is open. The options are:

Tx. Close/Open the transmit relay
Rx. Close/Open the receive relay.
Loop Close/Open the loopback relay.

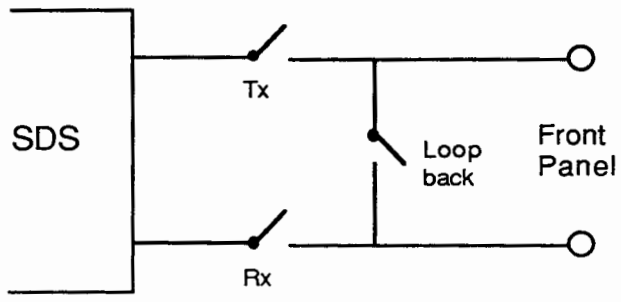


FIG 2 - OUTPUT RELAYS

Use

- Choose the SDS **instrument** to receive the command, using the **Device** tool.
- Select one or both **line** interface(s) to be programmed.
- Select **Impedance** and choose the impedance to be set, or leave unchanged to use existing settings.
- Enable **Pulse Shaping** if required, and select the pulse shaping options to be programmed.
- Enable **Outputs** to change the state of the output relays, and select the radio buttons to close or open the required relays.
- Check the **Wait for Completion** box if required.

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JITTER FACILITY

Clock jitter can be applied from the internal programmable jitter generation circuit, or from an external generator. The **Jitter** facility (**Jitter**) selects the source and programs the internal generator.

The external source may be connected to the SDS front panel, and is relay isolated when not selected. The maximum frequency that may be used with an external generator is 2.048 MHz.

A T1E1 Frame Setup facility must be present earlier in the test plan, to determine the choice between T1 and CEPT clocking.

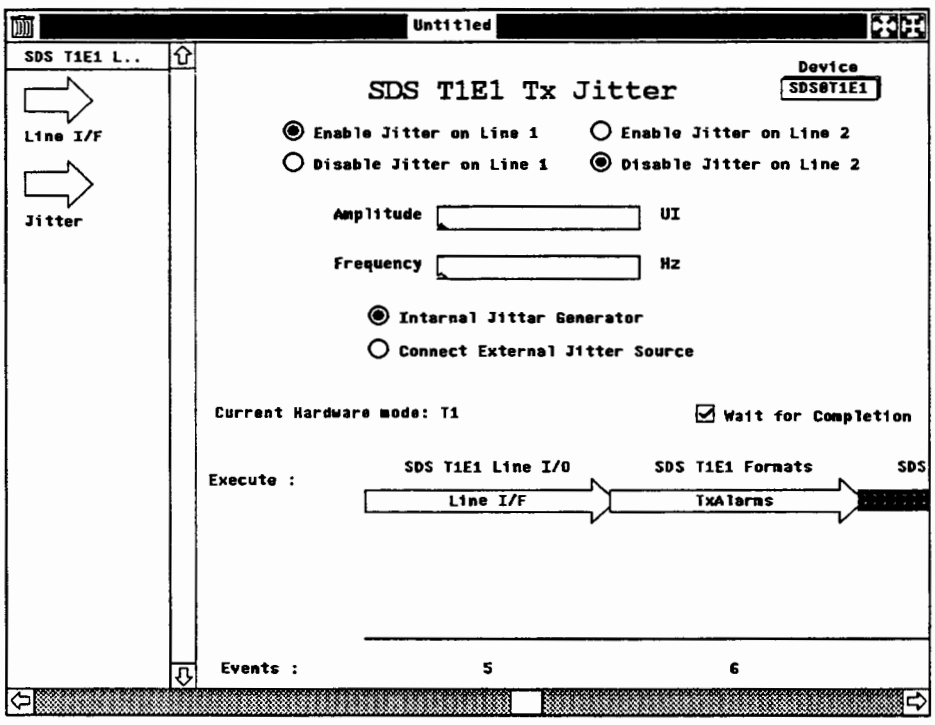


FIG 3 - JITTER FACILITY

Enabling and Disabling Jitter

Jitter may be enabled or disabled for each line by selecting the appropriate radio button. The settings for a line are unchanged if neither button is selected.

Two entry fields are provided in which the Frequency and Amplitude of the sinusoidal jitter must be entered.

- Amplitude. Enter an S constant for the amplitude in Unit Intervals.
- Frequency. Enter an S constant for the frequency in Hz.

Select the appropriate radio button to connect the internal generator or the external jitter source.

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Note that Save times may be become long if low frequency values are used, due to the generation of data for the jitter circuit.

Use

- Choose the SDS **instrument** to receive the command, using the **Device** tool.
- Select the appropriate radio buttons to enable or disable jitter for each line, as required.
- Select the internal jitter generator or the external source.
- If using the internal generator, enter S (real) constants for the amplitude and frequency of jitter to be applied.
- Check the **Wait for Completion** box if required.

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INTRODUCTION

The SDS card has two serial UART channels similar in operation to the Active Data sources but available on dedicated external ports.

UART CHANNEL

UART 1, using the Control Data 1 resource, may be configured as a basic two wire UART channel. UART 2 may be set up as a seven wire UART channel with hardware handshaking.

SETUP UART INTERFACE FACILITY

The **Setup UART Interface** facility (**SetupUART**) defines the clock source, data word length, stop bits and parity. Parity is calculated separately from the data channels parity generator. The Setup Active facility should be used to set up Control Data 1/2 as UARTs before using this facility.

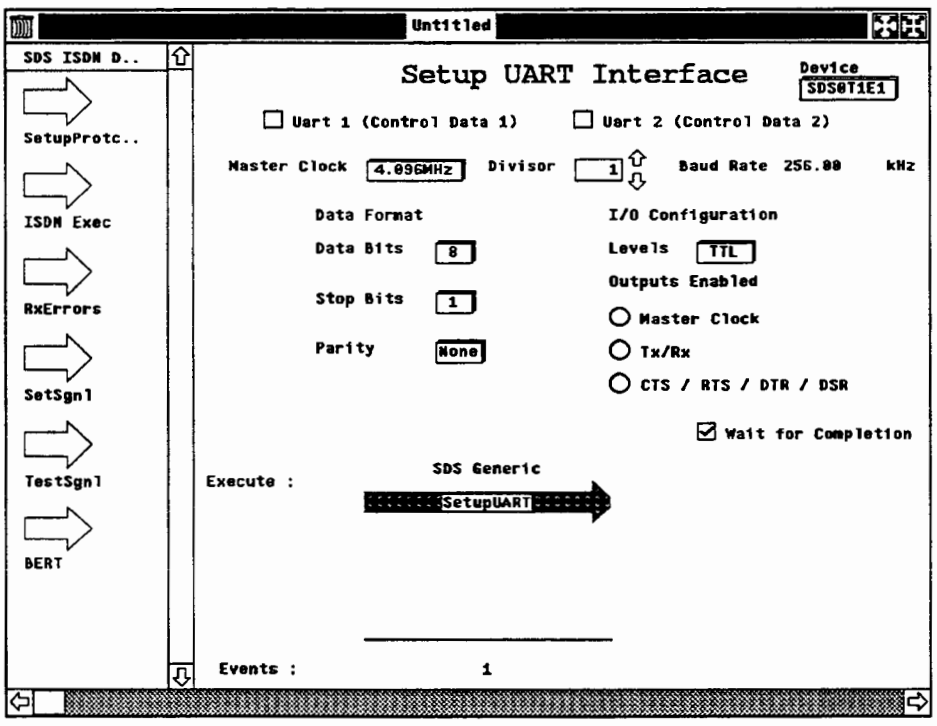


FIG 4 - SETUP UART INTERFACE FACILITY WINDOW

UART 1 and UART2

The settings programmed in the current event may be applied to one or both UART channels by checking the corresponding UART 1 and UART 2 checkboxes. Settings inappropriate for channel 1, the two wire channel, are ignored.

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Baud rate

A 4.096MHz or 3.6864 MHz UART master clock may be selected. The **baud rate** clock is set as the division ratio from the UART master clock by entering the required divisor in the **Divisor** box, or using the incrementer tool provided.

The selected clock is internally divided by 16 in the UART device to generate the final baud rate.

Data Word Settings

The following settings may be selected:

Start Bit	Single (fixed)
Data bits	7 or 8
Stop bits	1 or 2
Parity	Odd, even or none

I/O Configuration

The output level may be selected between TTL levels (default) or RS232 (+/- 12V) levels using the **Levels** button. The levels are applied to both Tx and Rx channels.

The Master Clock, Tx/Rx and hardware handshake CTS/RTS/DTR/DSR signals can be selectively enabled using the **Outputs Enabled** buttons. The signals can be set up without having been enabled, and may be separately enabled at a later point in the test program.

Use

- Choose the SDS **instrument** to receive the command, using the **Device** tool.
- Select the **division ratio** from the UART master clock to achieve the desired baud rate.
- Select the **data bits**, **parity** and **stop** bits
- Select the output level.
- Enable the required **outputs**, if any.
- Check the **Wait for Completion** box if required.

SDS SEND MESSAGE FACILITY

The **SDS Send Message Facility** (**SendMsg**) sends control messages via SDS Control Data resources configured as UARTs or PCM CCS (Common Channel Signaling)and FDL (Facility Data Link).

The facility transmits an Array Processor buffer using selected data resources and allows a user to optionally specify the number of **bytes** to send, **timeout** and flushing of any existing receive data prior to transmission.

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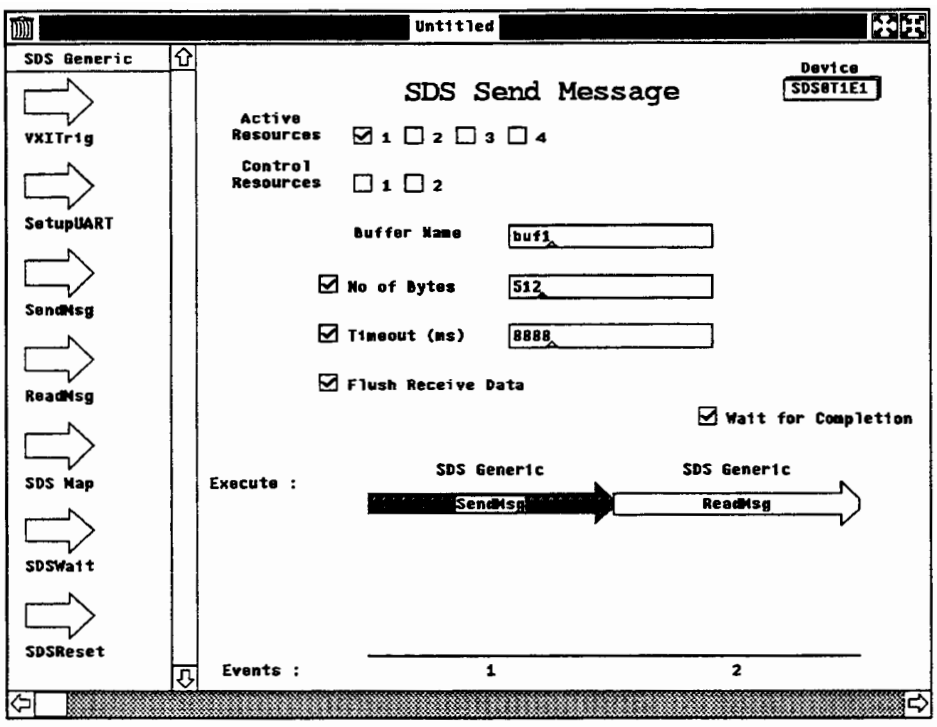


FIG 5 - SDS SEND MESSAGE FACILITY

The specified resources must have been programmed first either using the **SetupActive** facility or **SetupUART** facility. Run time errors will occur if this facility is used to control an Active Data resource which is programmed for the PCM protocol.

Buffer Name Enter the name of the Array Processor **buffer** to transmit. The name must refer to a previously allocated buffer.

No of Bytes Enter a `I` expression for the **number of bytes** to send. If left blank, the number defaults to the amount of valid data in the specified buffer.

Timeout Enter a MEDIATOR `I` expression specifying the **timeout** period in milliseconds. A runtime error is generated if transmission is not completed before the timeout expires.

Flush Receive Data Select **Flush Receive Data** if the SDS internal receive buffer should be cleared of data before the start of transmission.

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Use

- Choose the SDS **instrument** to receive the command, using the **Device** tool.
- Enter the **name** of the Array Processor **buffer** to transmit.
- Enter a MEDIATOR I expression for the **timeout** period (in milliseconds).
- Check the **Flush Receive Data** box if required.
- Check the **Wait for Completion** box if required.

SDS READ MESSAGE FACILITY

The **SDS Read Message** facility (**ReadMsg**) reads a message received by a Serial Data Sequencer data resource into an Array Processor buffer and allows a user to optionally specify the number of **bytes** to receive, **timeout** and flushing of any existing receive data prior to transmission..

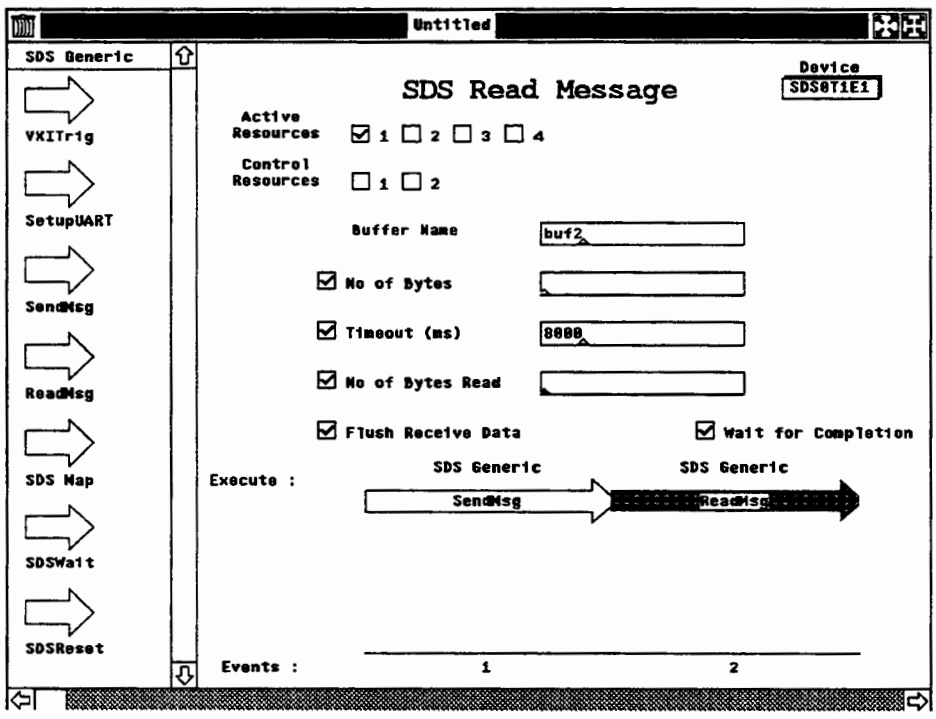


FIG 6 - SDS READ MESSAGE FACILITY

The specified resources must have been programmed first either using the **SetupActive** facility or **SetupUART** facility. Run time **errors** will occur if this facility is used to control an Active Data resource which is programmed for the PCM protocol.

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Buffer Name

Enter the name of the Array Processor **buffer** to receive the data. The name must refer to a previously allocated buffer.

Timeout

Enter a MEDIATOR `I` expression specifying the **timeout** period in milliseconds.

No. of Bytes Read

Enter a MEDIATOR `I` variable to contain the **number of words** expected, or leave blank. If the field is left blank the Array Processor buffer is filled to its allocated size.

If an `I` variable is specified the actual number of bytes read is returned at the end of the timeout period or as soon as the specified number of bytes has been received. If no `I` variable is specified a run time error is generated if the specified number of bytes was not received before the end of the timeout period

Flush Receive Data

Reading the specified number of bytes from the SDS internal receive buffer into the Array Processor buffer may leave some unwanted data in the receive buffer. Select **Flush Receive Data** to clear this unread data.

Use

- Choose the SDS **instrument** to receive the command, using the **Device** tool.
- Enter the **name** of the Array Processor **buffer** to receive the data.
- Enter a MEDIATOR `I` expression for the **timeout** period (in milliseconds).
- Enter a MEDIATOR `I` variable for the **number of words expected.**
- Check the **Flush Receive Data** box if required.
- Check the **Wait for Completion** box if required.

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SECTION 7

INSTALLATION AND HARDWARE

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INSTALLATION

Installation of SDS cards must be carried out by a Schlumberger engineer. Contact your local Schlumberger representative for details.

Software Installation

Software installation is described in the **Software Administration Manual** or in the **System Manual** supplied with each test system. Refer to the **Software Release Notes** supplied with the software for changes and up to date information. Systems are shipped with software installed.

The following information is supplied for reference only, and will not normally be altered by a user. Complete installation information is **not** supplied in this document.

SDS Cards

SDS cards fitted to a system must be identified in some files mentioned in installation procedures. SDS references are described below. Sample configuration files are normally supplied with each system, in the config area, with examples of the current format.

VXI_Config file

Multiple SDS cards may be fitted to a system. Each requires a separate entry in the VXI_config file. The format is:

```
SDSn [logical and physical address details] Poll END [firmware loader]
```

`n` identifies the card in the system, and corresponds to the System description file entry for each card. `Poll` and `END` are not used, but must be present as shown.

`[firmware loader]` - path to firmware loader to be used. If more than one SDS is fitted the firmware loader is identified on the **last** SDS entry only. .

An example is shown below.

```
#  Schlumberger Serial Data Sequencer. If more than one SDS is fitted, only
#  the last line should contain an entry for the firmware loader.
SDS0 1  1:4 Poll END
SDS1 2  1:5 Poll END SDS_main $HOME/s765_drivers/LOADER/SDS_VXI.o
```

SDS card entries must be placed after the Array Processor (MSP) entry.

IEEE Config file

SDS cards do not require entries in the `IEEE_config` file.

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Instrument.config file

The `instrument.config` file requires entries for SDS cards if one or more is fitted. Example entries are shown below.

```
# TIWB (including its constituent instruments)

TIWB                    tiwb     TIWB   tiwb_intro.help

#SDS Generic is required for all SDS cards:

"SDS Generic"           dummy    SDS    sds.help                c.SDS_SWB

#SDS PCM entries required if any PCM SDS cards are fitted:

"SDS PCM Clock"         dummy    SDS    sds_pcm_clock.help      c.SDS_SWB
"SDS PCM I/O"           dummy    SDS    sds_pcm_io.help         c.SDS_SWB
"SDS PCM Data"          dummy    SDS    sds_pcm_data.help       c.SDS_SWB

#SDS T1E1 entries required if any T1E1 SDS cards are fitted:

"SDS T1E1 Clock"        dummy    SDS    sds_t1e1_clock.help     c.SDS_SWB
"SDS T1E1 Line I/O"     dummy    SDS    sds_t1e1_lineio.help    c.SDS_SWB
"SDS T1E1 Data"         dummy    SDS    sds_t1e1_data.help      c.SDS_SWB
"SDS T1E1 formats"      dummy    SDS    sds_t1e1_format.help    c.SDS_SWB

# Extra lines for special customer-specific facilities
(further entries may be required here depending on the configuration)
```

765_config file

The `765_config` file contains entries for all instruments fitted to a particular system, and is created individually for each system. The following entry is required for each SDS card:

`SDS SERIAL NUMBER = xxxxxxxxx`

NETWORKING

SDS cards use Internet protocols to communicate with the CPU30 controller over the system backplane network. Each card must therefore be allocated an **IP number** by the local system or ATE manager, and must have the next consecutive local IP numbers following the CPU30 (see below).

The number allocated must be from a different network or subnet to that used by the Ethernet network.

CPU30

The CPU30 also requires a local IP number to communicate over the backplane network. Thus the CPU30 actually has two IP numbers, an Ethernet IP number and a local backplane IP number.

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INTRODUCTION

The information provided in this section is for reference purposes. Normal test access to the SDS functions and facilities is via the test head connections, and user access to the front panel is not required.

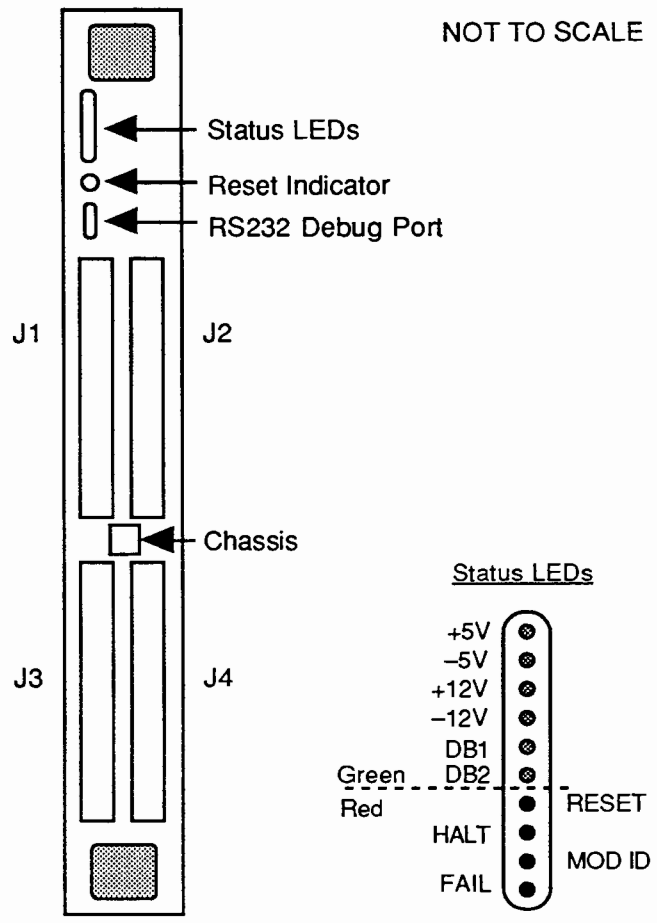


FIG 1 - SDS FRONT PANEL LAYOUT

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IDC CONNECTOR PINOUTS

As described above, normal test connections are via the test head. Refer to the test head map supplied with the system. The following pinout information is supplied for reference only.

Note pins not listed below may have connections to the SDS card. Such connections are reserved for Schlumberger use.

J2 CONNECTIONS

J2 is used for Tx and Rx data channel and clock connections.

Pin	Function	Comment	Name	Type
J2 - 2	Output Clock 1	+ve	RLY_OPCLK1	5V TTL
J2 - 4	Output Clock 1	-ve	(RLY_OPCLK1)	5V TTL
J2 - 8	Output Clock 2		RLY_OPCLK2	5V TTL
J2 - 6	Input Clock		RLY_IPCLK	5V TTL
J2 - 20	Tx Output Ch 1	+ve	TX1_P	T1/E1
J2 - 22	Tx Output Ch 1	-ve	TX1_N	T1/E1
J2 - 24	Tx Output Ch 2	+ve	TX2_P	T1/E1
J2 - 26	Tx Output Ch 2	-ve	TX2_N	T1/E1
J2 - 28	Rx Input Ch1	+ve	RX1_P	T1/E1
J2 - 30	Rx Input Ch1	-ve	RX1_N	T1/E1
J2 - 32	Rx Input Ch2	+ve	RX2_P	T1/E1
J2 - 34	Rx Input Ch2	-ve	RX2_N	T1/E1

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J3 CONNECTIONS

J3 is used for UART channels. UART channel 2 may be switched between 5V TTL and +/- 12V RS232 levels - each set of levels is connected to a different set of pins.

Pin	Function	Comment	Name	Type
J3 - 2	UART 1 Tx	UART 1		5V only
J3 - 4	UART 1 RX	UART 1		5V only
J3 - 6	Master Clock Out			5V TTL
J3 - 8	Jitter Clock			5V TTL
J3 - 18	UART 5V Logic CLK	UART 2	5VCLK	5V TTL
J3 - 20	UART 5V Logic Tx	UART 2	5VTX	5V TTL
J3 - 22	UART 5V Logic Rx	UART 2	5VRX	5V TTL
J3 - 24	UART 12V RS232 Tx	UART 2	12VTX	RS-232
J3 - 26	UART 12V RS232 Rx	UART 2	12VRX	RS-232
J3 - 27	UART 12V RS232 DTR	UART 2	12VDTR	RS-232
J3 - 28	UART 5V Logic DTR	UART 2	5VDTR	5V TTL
J3 - 29	UART 12V RS232 DSR	UART 2	12VDSR	RS-232
J3 - 30	UART 5V Logic DSR	UART 2	5VDSR	5V TTL
J3 - 31	UART 12V RS232 CD	UART 2	12VCD	RS-232
J3 - 32	UART 5V Logic CTS	UART 2	5VCTS	5V TTL
J3 - 33	UART 12V RS232 CTS	UART 2	12VCTS	RS-232
J3 - 34	UART 12V RS232 RTS	UART 2	12VRTS	RS-232

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J4 CONNECTIONS

J4 is used for event/interrupt pins. These pins are not currently supported for T1/E1 SDS cards.

Pin	Function	Comment	Name	Type
J4 - 22	Interrupt/Sense		Event 1	5V TTL
J4 - 24	Interrupt/Sense		Event 2	5V TTL
J4 - 26	Reserved			
J4 - 28	Reserved			
J4 - 30	Interrupt/Sense		Event 3	5V TTL
J4 - 32	Interrupt/Sense		Event 4	5V TTL
J4 - 34	n/c			

LOOPBACK CONNECTIONS

Loopback connections shown are internal connections, controlled from the TELECOM WORKBENCH facilities described earlier.

GROUND PINS

Odd numbered pins are used for **grounds**, with the exceptions listed above. Different grounds are used, for instance signal and digital grounds. Ground pin allocations are shown on the system test head map.

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