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TECHNICAL OVERVIEW

TO-105-01
JULY, 1986

SY/MAX® CLASS 8020 TYPE SCP-521, 522, 523, 544 MODEL 500 PROCESSOR

The SY/MAX Model 500 is a physically small yet very powerful processor designed for medium applications. It is enclosed in a sheet metal case and contains processor logic and memory for storing the user's control program. The Model 500 is designed to plug into the processor and adjacent register slot of any SY/MAX register rack assembly. The processor has five diagnostic LEDs and a block of diagnostic registers for ease of troubleshooting. To maintain system security the processor has a three position (RUN, HALT & DISABLE OUTPUTS) key operated mode selector switch.

The Model 500 processor has the ability to address up to 2008 registers for the performance of its control functions. Each register can be assigned as a data value, counter, timer, 16 digital I/O, etc. Up to 460 of these registers may reside within the processor with the remainder residing within the SY/MAX Local Interface Modules (LI) and within other intelligent I/O modules such as Analog and BCD I/O, High Speed Counter Input, Stepper Motor and Speech Output Module.

The LI allows for serial communication between the I/O modules and CPU at distances up to 15,000 ft. (4572m). The local interface module registers can be used for external digital and intelligent I/O in addition to internal relays and data storage registers. Each local interface module has the capacity for 2048 digital I/O. Although the Model 500 processor can support seven local interface modules (14,000 I/O), a realistic I/O capacity is 2048, dependent on selected memory size, and application requirements. The ability to communicate to multiple LI modules results in reduced system throughput time.

The SY/MAX Model 500 Processor has all the functions of the Model 300 Deluxe Processor (ASCII Output, peer-to-peer or network communications, asychronous shift registers, two communication ports with programmable BAUD rates) with additional advanced capabilities such as 1) expanded math functions (addition, subtraction, multiplication, division, square root, random number, absolute value, etc., with integer results to ±32,767), 2) scan control (GOTO function, Subroutine and Timed Interrupt), 3) Matrix operations (block data functions), 4) Immediate Communications Update, 5) logical functions (AND, OR, Exclusive OR), 6) program and communication software security features including program view inhibit, etc. Refer to the Instruction Set table.



The Model 500 processor is available in 2K, 4K and 8K RAM versions or a 8K RAM/UV PROM mix. The RAM/PROM mix allows for a maximum of 5461 words to be programmed in UV PROM. The remaining unused memory can be programmed as RAM memory to a total memory size of 8K. This allows critical circuits such as safety interlocks and emergency shutdown sequences to be programmed in the UV PROM memory where they cannot be changed, while the RAM memory can be used for other functions which can be altered.

Multi-level security features can be used to prevent the alteration of data and control programs, prevent I/O forcing, restrict network access of information, and provide password security.

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SPECIFICATIONS

Model 500 Processor

Rated Processor Current Draw On SY/MAX Power Supply
- Type SCP-521 ..... 4000ma
- Type SCP-522 ..... 4000ma
- Type SCP-523 ..... 4000ma
- Type SCP-544 ..... 4000ma

Environmental:
- Ambient Temp (Operational) ..... 0° to 60°C
- Ambient Humidity ..... 0 to 95% R.H. (Non-condensing)
- Storage Temperature .... -40° thru +80°C

Dimensions (WxHxD):
- (Without Key) ..... 3.0 x 13.2 x 6.6 inches (7.62 x 32.5 x 16.76 cm)

Weight (Approx.) ..... 4.0 lbs./1.81 kg.

Scan Speed .... Approximately 2.6 ms/k (relay logic only)

Noise Testing ..... Designed to meet NEMA ICS2-230 (Showering Arc) and ANSI C37.90a (Surge Withstand Capability)

Capabilities:
- Logic ..... Microprocessor-based
- Memory Size 2k, 4k, 8k
- Memory Type ..... RAM or RAM/PROM
- Memory Utilization ..... 1 word per contact, coil
- Memory Overhead ..... 47 words
- Diagnostic Lights ..... RUN, HALT, MEMORY, FORCE, I/O
- Total Addressable Registers ..... Flexible to 2008, 16 Bit data registers (460 registers of which are processor resident).
- External I/O ..... Over 2000 (any mix in groups of 4 or 8 I/O points per module)
- Internal Relay Equivalents ..... Over 2,000
- Data Storage Registers .. Flexible to 2008, 16 Bit data registers (may contain a 5 digit signed decimal value from -32,768 to +32,767)

INSTRUCTION SET

INSTRUCTION	DISPLAY	DESCRIPTION	REMARKS
Contacts	—| |—	Represents on/off status of inputs, outputs, internal relays, and register bits.	Input devices can be monitored in HALT.
Coil	—( )—	Represents an output connected to the processor.	Upon a transition to RUN, all coils are de-energized on the first scan. During the second scan, all coils are updated depending on the solution of the logic in that rung.
Internal Relays	R- —( )—	Represents control relay functions	Operation is much the same as an output but does not directly control output devices.
Latch/Unlatch Relays	—(L)— —(U)—	Duplicates the action of a mechanically held latching relay. This is accomplished through the use of two internal relay coils with the same address. Once a latch coil is energized, it remains on until the unlatch coil is energized, even if power is removed.	Latch and unlatch rungs must be programmed sequentially.
Transitional Coil	—(T)—	An internal or external coil which will only energize on a transition of the logic from open to closed. The output will remain on for a single processor scan. The logic must turn the coil off and transition to on again to re-energize the output coil.	Requires two consecutive I/O addresses, one to record the transition and one to remember the last state. A transitional coil must be assigned an ODD address number. The processor will then use the next I/O address for recording the last state of this same coil.
Master Control Relay	MCR —( )—	MCR ON allows logic to function. MCR OFF disables outputs. MCR controls all succeeding rungs until a new MCR coil is programmed or the end of program is reached.	

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MODEL 500 INSTRUCTION SET (continued)

INSTRUCTION	DISPLAY	DESCRIPTION	REMARKS
Timer	TMR	Timer register can store a four digit decimal value with a range from 0 to 9999. Selectable time bases are .01 sec., .1 sec., .1 min.	Programming techniques allow for programming of ON or OFF delay and interval timers. Replaces timing relays and motor driven timers.
Counter	CTR	Counter register can store a four digit decimal value with a range from 0 to 9999. UP, DOWN, and UP/DOWN counters are standard.	Possible to cascade counters to obtain a count greater than four digits.
Synchronous Shift Register	SHFT	Used to shift individual bits of a storage register in either a forward or reverse direction. Possible to shift 1, 8, or 16 bit channels at a time.	Used in applications requiring sequencing and replaces drum switches.
Asynchronous Shift Register (First In, First Out)	FIFO	Data is loaded into the first zone and exits out the last zone using IN and OUT commands respectively. Possible to shift 8 or 16 bit channels at a time.	Used to record the order of events as they occur, such as in conveyor and alarm annunciation applications.
Data Comparison	IF ($=$, $\neq$, $\geq$, $<$)	Compare functions between storage registers or between an integer or floating point storage register and a constant. When an IF comparison is true, the IF box acts like a short.	It is possible to program 3 comparisons on the line. Integer mode is capable of comparing a 5 digit number from -32,768 to 32,767. Register compares can support negative values. Math functions can be used in IF statements.
Data Transfer	LET	Transfer data from one storage register to another. Also performs integer or floating point or combined mode math.	Ranges are same as Data Compare (above). Occurs once per scan.
Transitional LET, IF	T LET T IF	Transition sensitive: restricts the operation of the LET or IF instruction to one operation for each open to closed transition of the input condition.	
Indirect Register Read	RDSTAT RDDATA FNDBIT	Indirect register read of status field. Indirect register read of data field. Locate and clear the first bit (lowest bit number) set in the indirect register being read.	
Binary to BCD	BCD	Conversion of binary data in a storage register to the binary coded decimal (BCD) equivalent of that data, within a LET or IF instruction.	Allows the processor to drive a BCD-type LED display.
BCD to Binary	BIN	Conversion of binary coded data (BCD) in a storage register to the binary equivalent of that data. Used in a LET or IF instruction.	Used in applications to convert the on/off status from a thumbwheel switch to a binary number which the processor can operate on.
Standard Math Operations Addition Subtraction Multiplication Division Square Root Absolute Value Negate	LET, IF + — x ÷ SQRT ABS NEGATE	Math operations are performed left to right. Programmed in IF or LET instructions. Value range for integer math operations: -32,768 to +32,767 Change sign of current result.	Intermediate results to ±2,147,483,647 are valid.
Accumulator Manipulations	ACCALT ADDALT SUBALT DUPALT DUPACC SWAP 16 SWAP 32	Exchange current accumulator with the alternate accumulator. Add current intermediate result to the alternate accumulator. Subtract current intermediate result from the alternate accumulator. Copy alternate accumulator into current accumulator. Copy current accumulator (intermediate result) into alternate accumulator. Exchange low and high bytes of the current intermediate result. Exchange low and high words of the current intermediate result.	These manipulations allow the user to preserve 32-bit precision when performing calculations which extend beyond a single rung.
Identify Number Type	NUMTYP	Identifies mathematical classification of current intermediate result.	

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MODEL 500 INSTRUCTION SET (continued)

INSTRUCTION	DISPLAY	DESCRIPTION	REMARKS
Forcing	CRT INITIATED	Forcing overrides the actual input status or output as controlled by the ladder diagram.	
Serial communications to other processors or peripherals	T READ T WRTE T ALRM T PRNT	Transfer storage register and I/O status between devices which may be located up to 10,000 ft. apart. All are transition sensitive.	Requires no additional interface hardware.
Read	T READ	Transfers storage register and I/O data from remote device to local processor for peer-to-peer or LAN communication.	
Write	T WRTE	Transfers storage register and I/O data from a local processor to a remote device for peer-to-peer or LAN communication.	
Alarm	T ALRM	Transfers a numerical value from a local processor to a register in a remote device. Peer-to-peer or LAN. The number can range from -32,768 to 32,767.	
Print	T PRNT	Transfers ASCII coded messages from the processor to any device that communicates in ASCII.	Simplified means of producing alarm messages, production reports, etc. ASCII data format is selectable.
AND	$\wedge$	A logical function used within an IF or LET command which has the property such that if X and Y are two logic variables, then the function "X AND Y" is defined by the following table: **X Y X AND Y** 0 0 0 0 1 0 1 0 0 1 1 1	
OR	$\vee$	A logical function used within an IF or LET command which has the property such that if P and R are logic quantities, then the logical result of "P OR R" assumes values as defined in the following table: **P R P OR R** 0 0 0 0 1 1 1 0 1 1 1 1	
Exclusive OR	$\oplus$	A logical function used within an IF or LET command having the property such that if S and T are logic quantities, then the logical result of "S XOR T" is defined by the following table: **S T S XOR T** 0 0 0 0 1 1 1 0 1 1 1 0	
Random Number Generator	RANDOM	Generates random number.	
GOTO	GOTO	Instruction to cause the processor to skip over a section of the program to a designated position in the program. Position is determined by a MARK rung placed in memory.	Shortens processor scan time and immediately jumps to a designated position.

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MODEL 500 INSTRUCTION SET (continued)

INSTRUCTION	DISPLAY	DESCRIPTION	REMARKS
Subroutines	GOSUB MARK ST SUB RTN	Group of ladder diagram rungs that can be executed from the user's ladder diagram only by enabling a GO SUB instruction which is programmed in the main program. Subroutines consist of a start of a subroutine (MARK), one or more ladder rungs, and a return (RTN). All subroutines must be programmed after the ST SUB instruction which denotes the beginning of the subroutine area. Nesting (subroutines within subroutines) are allowed up to 8 levels deep.	Applications include variable sequence machines, recipe programs, repeated programs.
Timed Interrupt, Communications Inhibit, Scan Time Limit	Reg. 8165	A special safeguard rung using register 8165 allows the following features: 1. Communications Inhibit 2. Program Viewing Inhibit 3. Safeguard Registers 4. Timed Interrupt-Scan Control 5. Scan Time Limit	Protect Programs used in conjunction with 8176 ⊢( )⊢ - 16 Scan Control
Matrix	M LET M IF M	A matrix is a group of storage registers handled as a unit. Formulates multi-register data transfers and math functions. Also allows multi-register compare statements.	Application includes machine diagnostics, menu selection, etc.
Immediate Communications Update	Reg. 8176 —( )— -11, 12, 13 and 14	Processes incoming data values from COMM port channels which were received during processor scanning.	

ORDERING INFORMATION

CLASS	TYPE	DESCRIPTION
8020	SCP-521	Model 500 Processor with 2K RAM Memory
8020	SCP-522	Model 500 Processor with 4K RAM Mmeory
8020	SCP-523	Model 500 Processor with 8K RAM Memory
8020	SCP-544	Model 500 Processor with 2.5K RAM/5.5K UV PROM

For additional information refer to Instruction Bulletin 30598-105-XX.

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