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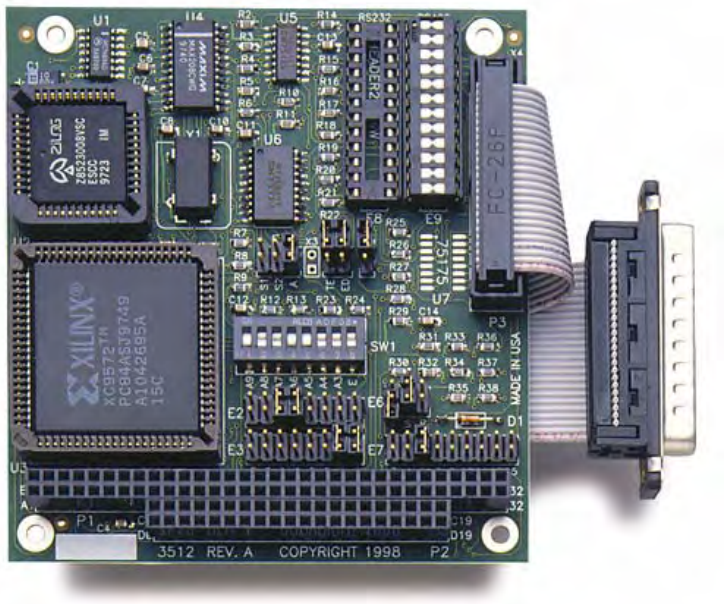
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SEALEVEL®
SYSTEMS INCORPORATED

ACB-104 ™
USER MANUAL



Part # 3512

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Introduction

Overview

The Sealevel Systems **ACB-104** provides the PC with one high-speed RS-232/530/422/485 synchronous/asynchronous port. The **ACB-104** can be used in a variety of sophisticated communications applications such as SDLC, HDLC, X.25, Bi-Sync, Mono-Sync, and high-speed asynchronous.

What's Included

The **ACB-104** is shipped with the following items. If any of these items are missing or damaged, contact the supplier.

- (1) **ACB-104** Adapter
- (1) DB-25 Cable Assembly
- (1) Nylon Hardware Kit
- Sealevel Software

Factory Default Settings

The **ACB-104** factory default settings are as follows:

Base Address	DMA Selection	IRQ	Electrical Specification
238	TX: 1 / RX: 3	5	RS-530/422

To install the **ACB-104** using factory default settings, refer to the section on Installation.

For your reference, record installed **ACB-104** settings below:

Base Address	DMA Selection	IRQ	Electrical Specification

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Card Setup

The **ACB-104** contains several jumper straps for each port, which must be set for proper operation.

Port Enable Disable

The **ACB-104** can be enabled or disabled with switch position 8 on the DIP-switch. The port is enabled with the switch 'On' or 'Closed' and disabled when 'Off' or 'Open'.

Address Selection

The **ACB-104** occupies 8 consecutive I/O locations. A DIP-switch (SW1) is used to set the base address for these locations. The **ACB-104** can reside in any I/O location between 100 and 3F8 Hex. Be careful when selecting the base address as some selections conflict with existing PC ports. The following table shows several examples that usually do not cause a conflict.

Address	Binary	Switch Settings						
	A9----------A0	1	2	3	4	5	6	7
238-23F	1000111XXX	Off	On	On	On	Off	Off	Off
280-287	1010000XXX	Off	On	Off	On	On	On	On
2A0-2A7	1010100XXX	Off	On	Off	On	Off	On	On
2E8-2EF	1011101XXX	Off	On	Off	Off	Off	On	Off
300-307	1100000XXX	Off	Off	On	On	On	On	On
328-32F	1100101XXX	Off	Off	On	On	Off	On	Off
3E8-3EF	1111101XXX	Off	Off	Off	Off	Off	On	Off

Figure 1 - Address Selection Table

The following illustration shows the correlation between the DIP-switch setting and the address bits used to determine the base address. In the example below, the address 300 Hex through 307 Hex is selected. 300 Hex = 11 0000 0XXX in binary representation.

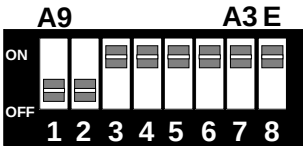


Figure 2 - DIP-switch Illustration

Note: Setting the switch 'On' or 'Closed' corresponds to a '0' in the address, while leaving it 'Off' or 'Open' corresponds to a '1'.

The relative I/O address of the **ACB-104** registers are as follows:

- Base+0 Channel A Data Port
- Base+1 Channel A Control Port
- Base+2 Channel B Data Port
- Base+3 Channel B Control Port
- Base+4 Board Control / Status Port
- Base+5 Reset TCIRQ

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Transmit Clock Header E5

Header E5 sets the input/output clock modes for the transmit clock (TXC). If the transmit clock is to be an input, place the jumper to cover both pins. This board does not support transmit clock as an output.

RS-485 Mode Enable Header E4

E4 position '**TE**' determines whether the RS-485 transmit driver is enabled by the **E**nhanced **S**erial **C**ommunications **C**ontroller (ESCC) signal **R**equest **T**o **S**end (RTS) or always enabled. With the jumper installed, RTS enables the driver. Removing the jumper enables the driver regardless of RTS. This jumper should only be installed if you are running the board in a multi-drop polled environment such as RS-485, and you have software that knows how to 'talk' on the RS-485 bus. ***For normal point-to-point RS-530 and RS-422, remove this jumper.***

E4 position '**ED**' is used to control the RS-485 enable/disable functions for the receiver circuit and determine the state of the RS-422/485 driver. The RS-485 'Echo' is the result of connecting the receiver inputs to the transmitter outputs. Every time a character is transmitted; it is also received. This can be beneficial if the software can handle echoing (i.e. using received characters to throttle the transmitter) or it can confuse the system if the software does not. To select the 'No Echo' mode select silk-screen position 'ED'.

Electrical Interface Selection Headers E8 &E9

The **ACB-104** has the ability to be used in either RS-232 or RS-530/422/485. This is selectable via two 24 pin DIP-shunts at E8 & E9. Please use the following illustration to aid in the configuration of your electrical interface.

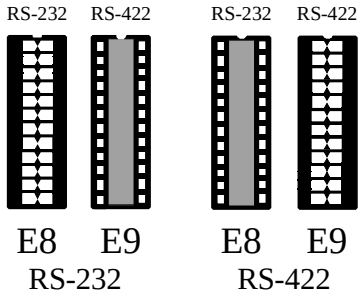


Figure 3 Headers E8 & E9, Electrical Interface Selection

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DMA Channel Selection Headers E2 & E3

Headers E2 & E3 select **D**irect **M**emory **A**ccess (DMA) mode of operation. Each channel of the **E**nhanced **S**erial **C**ommunications **C**ontroller (ESCC) will function in half duplex or full duplex DMA modes. Full duplex means that DMA can be used for simultaneous transmit and receive. Half-duplex DMA means that you can either transmit, or receive with DMA, but not simultaneously. The 85230 has two signals that correspond to DMA request signals, WAIT/REQ and DTR/REQ. E2 corresponds to the SCC signal WAIT/REQ and E3 corresponds to DTR/REQ. WAIT/REQ and DTR/REQ can be programmed to serve as DMA request lines (DRQ) by setting the appropriate bits in Write Register 1 and Write Register 14 in the 85230. WAIT/REQ (E2) can be programmed for ***Transmit*** or ***Receive*** DMA transfers and DTR/REQ (E3) can be programmed for ***Transmit Only***. For additional information on the programming of the 85230 please refer to the Zilog ESCC Users Manual. Please note that each DMA channel is selected by two jumpers. Only one DMA channel may be selected for each header block.

Note: If DMA is not used, remove all of the jumpers on E2 & E2 and remove jumper at E1

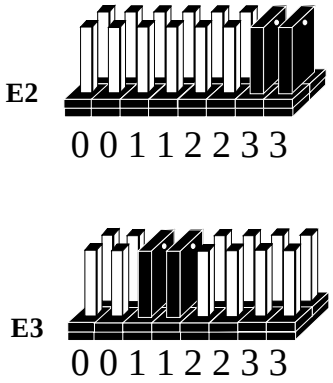


Figure 4 - DMA Selection Headers E2 & E3

Note: DMA Channel 2 can only be used if the floppy disk DMA drivers are turned off. Please refer to the toolkit disk for software examples.

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DMA Jumper Option Tables

The following tables show the jumper setting examples for each mode of DMA:

No DMA

Option	E2	E3
Ch.A No DMA	None	None

Single Channel DMA (Half Duplex Only)

Option	E2	E3
DMA Channel 0	00	None
DMA Channel 1	11	None
DMA Channel 2	22	None
DMA Channel 3	33	None

Full Duplex

Option	E2	E3
DMA Ch.1 Receive Data DMA Ch.3 Transmit Data	11	33
DMA Ch.0 Receive Data DMA Ch.2 Transmit Data	00	22

Note: DMA Channel 2 can only be used if the floppy disk DMA drivers are turned off. Please refer to the Toolkit disk for software examples.

DMA Enable Header E1

Header E1 selects whether the DMA tri-state drivers are enabled permanently, (position A) disabled permanently (jumpers removed), or which DMA enable control port bit is used to enable the DMA hardware request and acknowledge signals. Removing the jumper disables the drivers and no DMA can be performed.

Note: The power on reset signal resets or disables the DMA software enable signal.

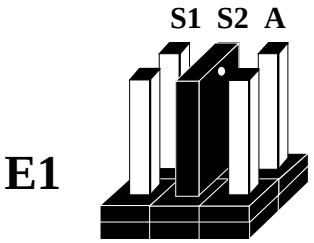


Figure 5 - DMA Enable Header E1

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S1	Base+4 Position D7 enables DMA
S2	RTSB enables DMA
A	Selects Always Enable

Note: Please refer to Section 4 for software bit definitions and examples of DMA driver control.

IRQ Selection Header E7

Header E7selects the interrupt request (IRQ) line for the card. If no interrupt is desired, remove the jumper.

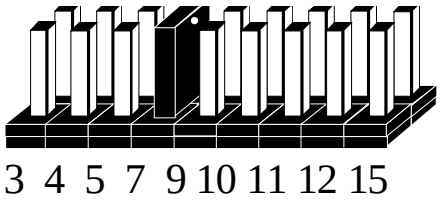


Figure 6 - IRQ Header E7

IRQ Mode Header E6

Header E6 '**N**' indicates the (**N**)ormal, single interrupt mode. Position '**M**' indicates the inclusion of a 1K ohm pull-down resistor required on one port when sharing interrupts with another card. For shared interrupt mode, set one board to '**M**' and all other adapters sharing an IRQ should have neither '**N**' or '**M**' in place. This mode allows more than one board to access a single IRQ.

Position '**T**' on E6 enables the ***DMA Terminal Count Interrupt.*** Setting this jumper allows the selected DMA channel to generate an interrupt once the ***DMA Terminal Count*** has been reached. See Section 4 for the status bit (TC STAT) position and refer to the toolkit disk for software examples.

Note: When using multiple cards on one IRQ in shared mode, be sure that only one port has the 'M' jumper set, providing the necessary pull-down resistor.

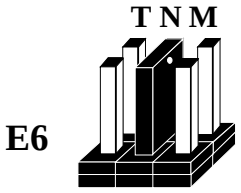


Figure 7 - IRQ Mode Header

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Installation

The **ACB-104** can be installed in any of the PC expansion slots The **ACB-104** contains several jumper straps for each port, which must be set for proper operation.

1. Turn off PC power. Disconnect the power cord.
2. Remove the PC case cover.
3. Locate two available slots and remove the blank metal slot covers.
4. Replace the cover.
5. Connect the power cord.

Installation is complete.

Cabling Options

The **ACB-104** has a number of cabling options available. These options include:

- **CA-104** - This cable provides a 6′ extension for use with RS-530/422
- **CA-107** - This cable provides a simple interface to the RS-449, DB-37 type connector. RS-530 was designed as a replacement for RS-449.

Software Installation

Windows Users

Choose **Install Software** at the beginning of the CD and select **Synchronous/Asynchronous Software** and install the **SeaMAC** software**.**

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Technical Description

The **ACB-104** utilizes the Zilog 85230 **E**nhanced **S**erial **C**ommunications **C**ontroller (ESCC). This chip features programmable baud rate, data format and interrupt control, as well as DMA control. Refer to the ESCC Users Manual for details on programming the 85230 ESCC chip.

Features

- One channel of sync/async communications using 85230 chip
- DMA supports data rate greater than 1 million bits per second (bps)
- Selectable Port Address, IRQ level (3, 4, 5, 7, 9, 10, 11, 12, 15)
- Selectable DMA channels (0, 1, 2, 3)
- EIA-232 interface with full modem control signals TD, RD, RTS, CTS, DSR, DCD, DTR, TXC, RXC, TSET signals
- EIA-530 interface with modem control signals TD, RD, RTS, CTS, DTR, TXC, RXC, TSET signals
- Jumper options for Transmit clock as input or output
- Software programmable baud rate

Internal Baud Rate Generator

The baud rate of the ESCC is programmed under software control. The standard oscillator supplied with the board is 7.3728 MHz. However, other oscillator values can be substituted to achieve different baud rates.

Programming the ACB-104

Control/Status Port

The **ACB-104** occupies eight **i**nput/**o**utput (I/O) addresses. The ESCC chip uses the first four, while the fifth address (Base+4) is the address of the on-board **Control/Status Port**. This port is used to set the **D**ata **T**erminal **R**eady (DTR) and to enable or disable DMA under program control, and to monitor the **D**ata **S**et **R**eady (DSR) input signals from the modem.

Bit	Output Port Bits	Input Port Bits
0	DTR A 1=On, 0=Off	DSR A 1=Off, 0=On
1	Unused bit	Unused bit
2	Unused bit	Unused bit
3	Unused bit	ESCC INT 1=Off, 0=On
4	Unused bit	Unused bit
5	Unused bit	TC STAT 1=Off, 0=On
6	Unused bit	Unused bit
7	CH. A DMA Enable ESCC CH.A 1=On, 0=Off	Ch.A DMA 1=Off, 0=On

Software Examples

Function	Program Bits
Turn On CH.A DTR	Out (Base+4), XXXX XXX1
Turn Off CH.A DTR	Out (Base+4), XXXX XXX0
Enable DMA Drivers	Out (Base+4), 1XXX XXXX
Disable DMA Drivers	Out (Base+4), 0XXX XXXX
Test CH.A DSR	In (Base+4), Mask=0000 0001

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DMA Terminal Count

The **ACB-104** can be setup to operate using a polling method, interrupts, or system DMA. The most efficient method is a combination of DMA and interrupts. The **ACB-104** has been optimized to generate an interrupt at the end of a DMA transfer. This will allow DMA initialization and buffer management to take place at interrupt time and provide a virtually seamless communication channel. If the '**T**' option on header E5 is selected, an onboard latch will be set when Terminal Count for the selected DMA channel(s) is reached. This latch will cause an interrupt to be generated and program execution will be transferred to the application Interrupt Service Routine (ISR). The DMA Terminal Count Interrupt condition should be reset from the ISR by writing to BASE+5. The value that is written to this I/O location is irrelevant. If your application or driver is interrupting on multiple conditions, reading the Status Register located at Base+4 will determine the source of the interrupt (ESCC or DMA Terminal Count generated). Bit D3 in the Status Port corresponds to a ESCC generated interrupt and bit D5 corresponds to an interrupt generated by the end of a DMA transfer. Bit D3 can only be reset by polling the ESCC to determine the interrupt source and required action necessary to reset the interrupt. Please refer to the Software Toolkit and the 85230 Technical Manual for details and examples on interrupt driven and DMA programming examples.

Connector P3 Pin Assignments

RS-232 Signals (At the DB-25)

Signal	Name	Pin #	Mode
GND	Ground	7	
RD	Receive Data	3	Input RS-232
CTS	Clear To Send	5	Input RS-232
DSR	Data Set Ready	6	Input RS-232
TXC	Transmit Clock	15	Input RS-232
RXC	Receive Clock	17	Input RS-232
DCD	Data Carrier. Detect	8	Output RS-232
TD	Transmit Data	2	Output RS-232
RTS	Request to Send	4	Output RS-232
TSET	Transmit Signal Element Timing	24	Output RS-232
DTR	Data Terminal Ready	20	Output RS-232

Note: These assignments meet the EIA/TIA/ANSI-232E DTE Specification

Technical Note: Please terminate any control signals that are not going to be used. The most common way to do this is connect RTS to CTS and RI. Also, connect DCD to DTR and DSR. Terminating these pins, if not used, will help insure you get the best performance from your adapter.

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RS-530/422/485 Pin Assignments (At the DB-25)

Signal		Name	Pin #	Mode
GND		Ground	7	
RDB	RX+	Receive Data Positive	16	Input
RDA	RX-	Receive Data Negative	3	Input
CTSB	CTS+	Clear To Send Positive	13	Input
CTSA	CTS-	Clear To Send Negative	5	Input
TXCB	TXC+	Transmit Clock Positive	12	Input
TXCA	TXC-	Transmit Clock Negative	15	Input
RXCB	RXC+	Receive Clock Positive	9	Input
RXCA	RXC-	Receive Clock Negative	17	Input
TDB	TX+	Transmit Data Positive	14	Output
TDA	TX-	Transmit Data Negative	2	Output
RTSB	RTS+	Request To Send Positive	19	Output
RTSA	RTS-	Request To Send Negative	4	Output
DTRB	DTR+	Data Terminal. Ready Positive	23	Output
DTRA	DTR-	Data Terminal Ready Negative	20	Output
TSETB	TSET+	Terminal Timing Positive	11	Output
TSETA	TSET-	Terminal Timing Negative	24	Output

Note: These assignments meet the EIA/TIA/ANSI-530A DTE Specification.

RS-530/422/485 Line Termination

Typically, each end of the RS-530/422/485 bus must have line-terminating resistors. A 120-ohm resistor is across each RS-530/422/485 input in addition to a 1K ohm pull-up/pull-down combination that biases the receiver inputs.

The RS-530 specification calls for a 100-ohm 1/2-watt resistor between the signal ground and the chassis ground. On the IBM PC, these two grounds are already connected together, therefore this resistor is omitted.

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Specifications

Environmental Specifications

Specification	Operating	Storage
Temperature Range	0º to 50º C (32º to 122º F)	-20º to 70º C (-4º to 158º F)
Humidity Range	10 to 90% R.H. Non-Condensing	10 to 90% R.H. Non-Condensing

Power Consumption

Supply line	+5
Rating	350ma

Mean Time Between Failures (MTBF)

Greater than 150,000 hours. (Calculated)

Physical Dimensions

Board length	3.75 inches	(9.54 cm)
Board Height including Goldfingers	3.5 inches	(8.89 cm)
Board Height excluding Goldfingers	3.2 inches	(8.12 cm)

Please see Appendix G for board layout and dimensions.

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Appendix A - Troubleshooting

An ACB Developers Toolkit Diskette is supplied with the Sealevel Systems adapter and will be used in the troubleshooting procedures. By using this diskette and following these simple steps, most common problems can be eliminated without the need to call Technical Support.

1. Identify all I/O adapters currently installed in your system. This includes your on-board serial ports, controller cards, sound cards etc. The I/O addresses used by these adapters, as well as the IRQ (if any) should be identified.

2. Configure your Sealevel Systems adapter so that there is no conflict with currently installed adapters. No two adapters can occupy the same I/O address.

3. Make sure the Sealevel Systems adapter is using a unique IRQ. While the Sealevel Systems adapter does allow the sharing of IRQs, many other adapters (i.e. SCSI adapters & on-board serial ports) do not. The IRQ is typically selected via an on-board header block. Refer to the section on Card Setup for help in choosing an I/O address and IRQ.

4. Make sure the Sealevel Systems adapter is securely installed in a motherboard slot.

5. Use the supplied diskette and User Manual to verify that the Sealevel Systems adapter is configured correctly. The supplied diskette contains a diagnostic program 'SSDACB' that will verify if an adapter is configured properly. Refer to the 'UTIL.txt' file found in the \UTIL sub-directory on the supplied diskette for detailed instructions on using 'SSDACB'.

6. The following are known I/O conflicts:

    - 3F8-3FF is typically reserved for COM1:
    - 2F8-2FF is typically reserved for COM2:
    - 3E8-3EF is typically reserved for COM3:
    - 2E8-2EF is typically reserved for COM4:

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Appendix B - How To Get Assistance

Please refer to Troubleshooting Guide prior to calling Technical Support.

1. Begin by reading through the Trouble Shooting Guide in Appendix A. If assistance is still needed please see below.
2. When calling for technical assistance, please have your user manual and current adapter settings. If possible, please have the adapter installed in a computer ready to run diagnostics.
3. Sealevel Systems provides an FAQ section on its web site. Please refer to this to answer many common questions. This section can be found at http://www.sealevel.com/faq.htm .
4. Sealevel Systems maintains a Home page on the Internet. Our home page address is www.sealevel.com. The latest software updates, and newest manuals are available via our FTP site that can be accessed from our home page.
5. Technical support is available Monday to Friday from 8:00 a.m. to 5:00 p.m. eastern time. Technical support can be reached at (864) 843-4343.

RETURN AUTHORIZATION MUST BE OBTAINED FROM SEALEVEL SYSTEMS BEFORE RETURNED MERCHANDISE WILL BE ACCEPTED. AUTHORIZATION CAN BE OBTAINED BY CALLING SEALEVEL SYSTEMS AND REQUESTING A RETURN MERCHANDISE AUTHORIZATION (RMA) NUMBER.

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Appendix C - Electrical Interface

RS-232

Quite possibly the most widely used communication standard is RS-232. This implementation has been defined and revised several times and is often referred to as RS-232 or EIA/TIA-232. It is defined by the EIA as the *Interface between Data Terminal Equipment and Data Circuit- Terminating Equipment Employing Serial Binary Data Interchange*. The mechanical implementation of RS-232 is on a 25 pin D sub connector. The IBM PC computer defined the RS-232 port on a 9 pin D sub connector and subsequently the EIA/TIA approved this implementation as the EIA/TIA-574 standard. This standard is defined as the *9-Position Non-Synchronous Interface between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange*. Both implementations are in wide spread use and will be referred to as RS-232 in this document. RS-232 is capable of operating at data rates up to 20 Kbps at distances less than 50 ft. The absolute maximum data rate may vary due to line conditions and cable lengths. The voltage levels defined by RS-232 range from -12 to +12 volts. RS-232 is a single ended or unbalanced interface, meaning that a single electrical signal is compared to a common signal (ground) to determine binary logic states. A voltage of +12 volts (usually +3 to +10 volts) represents a binary 0 (space) and -12 volts (-3 to -10 volts) denotes a binary 1 (mark). The RS-232 and the EIA/TIA-574 specification defines two type of interface circuits, **D**ata **T**erminal **E**quipment (DTE) and **D**ata **C**ircuit-Terminating **E**quipment (DCE). The Sealevel Systems adapter is a RS-232 Synchronous DTE interface.

RS-422

The RS-422 specification defines the electrical characteristics of balanced voltage digital interface circuits. RS-422 is a differential interface that defines voltage levels and driver/receiver electrical specifications. On a differential interface, logic levels are defined by the difference in voltage between a pair of outputs or inputs. In contrast, a single ended interface, for example RS-232, defines the logic levels as the difference in voltage between a single signal and a common ground connection. Differential interfaces are typically more immune to noise or voltage spikes that may occur on the communication lines. Differential interfaces also have greater drive capabilities that allow for longer cable lengths. RS-422 is rated up to 10 Megabits per second and can have cabling 4000 feet long. RS-422 also defines driver and receiver electrical characteristics that will allow 1 driver and up to 32 receivers on the line at once. RS-422 signal levels range from 0 to +5 volts. RS-422 does not define a physical connector.

RS-530

RS-530 (a.k.a. EIA-530) compatibility means that RS-422 signal levels are met, and the pin-out for the DB-25 connector is specified. The **E**lectronic **I**ndustry **A**ssociation (EIA) created the RS-530 specification to detail the pin-out, and define a full set of modem control signals that can be used for regulating flow control and line status. The RS-530 specification defines two types of interface circuits, **D**ata **T**erminal **E**quipment (DTE) and **D**ata **C**ircuit-Terminating **E**quipment (DCE). The Sealevel Systems adapter is a DTE interface.

RS-449

RS-449 (a.k.a. EIA-449) compatibility means that RS-422 signal levels are met, and the pin-out for the DB-37 connector is specified. The EIA created the RS-449 specification to detail the pin-out, and define a full set of modem control signals that can be used for regulating flow control and line status.

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RS-485

RS-485 is backwardly compatible with RS-422; however, it is optimized for partyline or multi-drop applications. The output of the RS-422/485 driver is capable of being **Active** (enabled) or **Tri-State** (disabled). This capability allows multiple ports to be connected in a multi-drop bus and selectively polled. RS-485 allows cable lengths up to 4000 feet and data rates up to 10 Megabits per second. The signal levels for RS-485 are the same as those defined by RS-422. RS-485 has electrical characteristics that allow for 32 drivers and 32 receivers to be connected to one line. This interface is ideal for multi-drop or network environments. RS-485 tri-state driver (not dual-state) will allow the electrical presence of the driver to be removed from the line. The driver is in a tri-state or high impedance condition when this occurs. Only one driver may be active at a time and the other driver(s) must be tri-stated. The output modem control signal **R**equest **t**o **S**end (RTS) controls the state of the driver. Some communication software packages refer to RS-485 as RTS enable or RTS block mode transfer. RS-485 can be cabled in two ways, two wire and four wire mode. Two wire mode does not allow for full duplex communication, and requires that data be transferred in only one direction at a time. For half-duplex operation, the two transmit pins should be connected to the two receive pins (Tx+ to Rx+ and Tx- to Rx-). Four wire mode allows full duplex data transfers. RS-485 does not define a connector pin-out or a set of modem control signals. RS-485 does not define a physical connector.

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Appendix D - Direct Memory Access

In many instances, it is necessary to transmit and receive data at greater rates than would be possible with simple port I/O. In order to provide a means for higher rate data transfers, a special function called **D**irect **M**emory **A**ccess (DMA) was built into the original IBM PC. The DMA function allows the **ACB-104** (or any other DMA compatible interface) to read or write data to or from memory without using the Microprocessor. This function was originally controlled by the Intel 8237 DMA controller chip, but may now be a combined function of the peripheral support chip sets (i.e. Chips & Technology or Symphony chip sets).

During a DMA cycle, the DMA controller chip is driving the system bus in place of the Microprocessor, providing address and control information. When an interface uses DMA, it activates a DMA request signal (DRQ) to the DMA controller, which in turn sends a DMA hold request to the Microprocessor. When the Microprocessor receives the hold request it will respond with an acknowledge to the DMA controller chip. The DMA controller chip then becomes the owner of the system bus providing the necessary control signals to complete a Memory to I/O or I/O to Memory transfer. When the data transfer is started, an acknowledge signal (DACK) is sent by the DMA controller chip to the **ACB-104**. Once the data has been transferred to or from the **ACB-104** the DMA controller returns control to the Microprocessor.

To use DMA with the **ACB-104** requires a thorough understanding of the PC DMA functions. The ACB Developers Toolkit demonstrates the setup and use of DMA with several source code and high-level language demo programs. Please refer to the ESCC User's Manual for more information.

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Appendix E - Asynchronous and Synchronous Communications

Serial data communications implies that individual bits of a character are transmitted consecutively to a receiver that assembles the bits back into a character. Data rate, error checking, handshaking, and character framing (start/stop bits or sync characters) are pre-defined and must correspond at both the transmitting and receiving ends. The techniques used for serial communications can be divided two groups, *asynchronous* and *synchronous*.

When contrasting asynchronous and synchronous serial communications, the fundamental differences deal with how each method defines the beginning and end of a character or group of characters. The method of determining the duration of each bit in the data stream is also an important difference between asynchronous and synchronous communications. The remainder of this section is devoted to detailing the differences between character framing and bit duration implemented in asynchronous and synchronous communications.

Asynchronous Communications

Asynchronous communications is the standard means of serial data communication for PC compatibles and PS/2 computers. The original PC was equipped with a communication or COM: port that was designed around an 8250 **U**niversal **A**synchronous **R**eceiver **T**ransmitter (UART). This device allows asynchronous serial data to be transferred through a simple and straightforward programming interface. Character boundaries for asynchronous communications are defined by a starting bit followed by a pre-defined number of data bits (5, 6, 7, or 8). The end of the character is defined by the transmission of a pre-defined number of stop bits (usual 1, 1.5 or 2). An extra bit used for error detection is often appended before the stop bits.

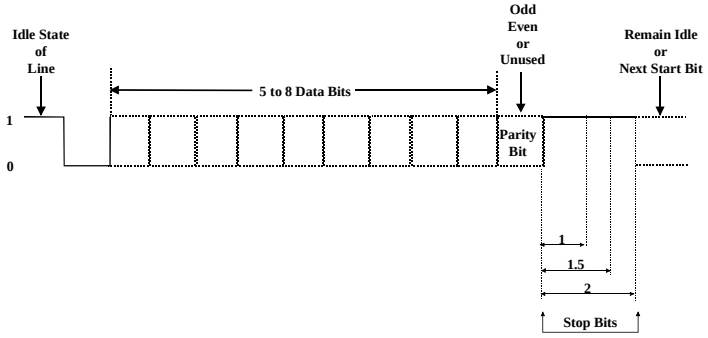


Figure 8 - Asynchronous Communications Bit Diagram

This special bit is called the parity bit. Parity is a simple method of determining if a data bit has been lost or corrupted during transmission. There are several methods for implementing a parity check to guard against data corruption. Common methods are called (E)ven Parity or (O)dd Parity. Sometimes parity is not used to detect errors on the data stream. This is referred to as (N)o parity. Because each bit in asynchronous communications is sent consecutively, it is easy to generalize asynchronous communications by stating that each character is wrapped (framed) by pre-defined bits to mark the beginning and end of the serial transmission of the character. The data rate and communication parameters for asynchronous communications have to be the same at both the transmitting and receiving ends. The communication parameters are baud rate, parity, number of data bits per character, and stop bits (i.e. 9600,N,8,1).

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Synchronous Communications

Synchronous Communications is used for applications that require higher data rates and greater error checking procedures. Character synchronization and bit duration are handled differently than asynchronous communications. Bit duration in synchronous communications is not necessarily pre-defined at both the transmitting and receiving ends. Typically, in addition to the data signal, a clock signal is provided. This clock signal will mark the beginning of a bit cell on a pre-defined transmission. The source of the clock is predetermined and sometimes multiple clock signals are available. For example, if two nodes want to establish synchronous communications, point A could supply a clock to point B that would define all bit boundaries that A transmitted to B. Point B could also supply a clock to point A that would correspond to the data that A received from B. This example demonstrates how communications could take place between two nodes at completely different data rates. Character synchronization with synchronous communications is also very different than the asynchronous method of using start and stop bits to define the beginning and end of a character. When using synchronous communications a pre-defined character or sequence of characters is used to let the receiving end know when to start character assembly.

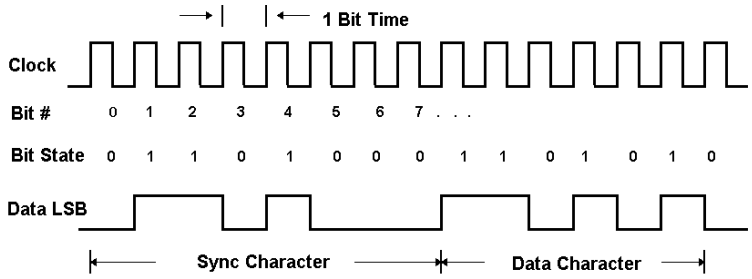


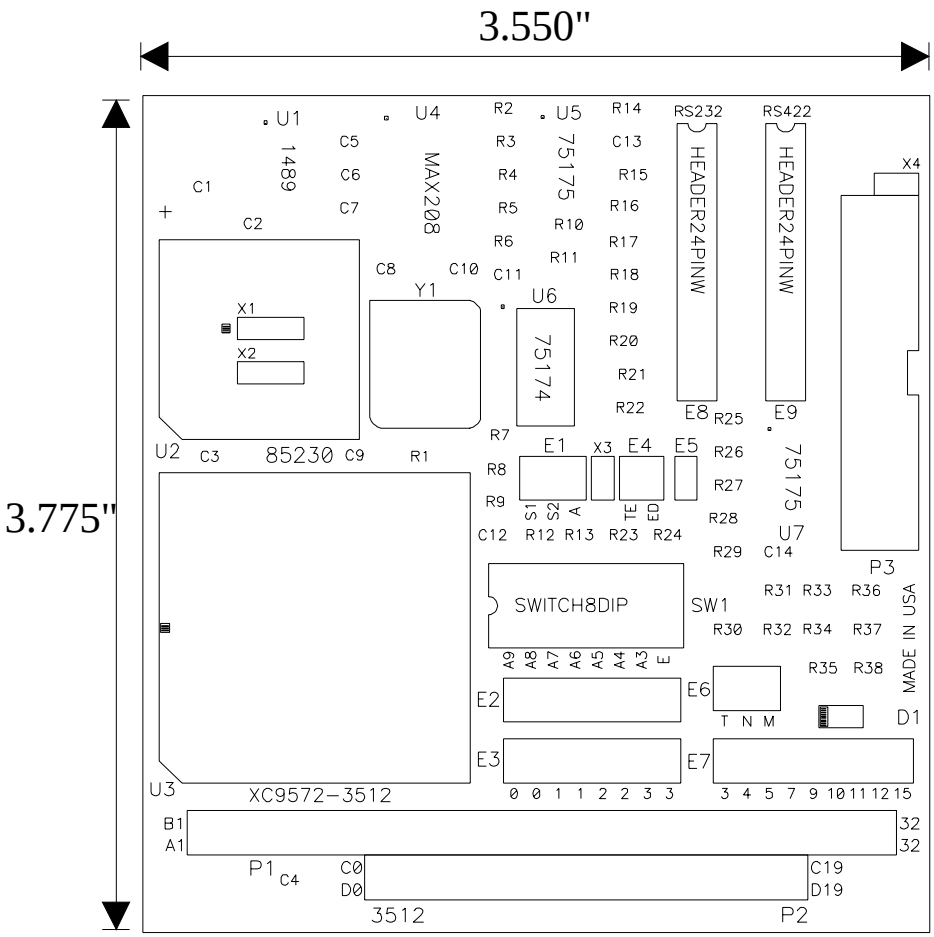
Figure 9 - Synchronous Communications Bit Diagram

This pre-defined character is called a sync character or sync flag. Once the sync flag is received, the communications device will start character assembly. Sync characters are typically transmitted while the communications line is idle or immediately before a block of information is transmitted. To illustrate with an example, let's assume that we are communicating using eight bits per character. Point A is receiving a clock from point B and sampling the receive data pin on every upward clock transition. Once point A receives the pre-defined bit pattern (sync flag), the next eight bits are assembled into a valid character. The following eight bits are also assembled into a character. This will repeat until another pre-defined sequence of bits is received (either another sync flag or a bit combination that signals the end of the text, e.g., EOT). The actual sync flag and protocol varies depending on the sync format (SDLC, BISYNC, etc.).

For a detailed explanation of serial communications, please refer to the book *Technical Aspects of Data Communications* by John E. McNamara, published by Digital Press (DEC) 1982.

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Appendix F - Silk-Screen



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RETURN AUTHORIZATION MUST BE OBTAINED FROM SEALEVEL SYSTEMS BEFORE RETURNED MERCHANDISE WILL BE ACCEPTED. AUTHORIZATION CAN BE OBTAINED BY CALLING SEALEVEL SYSTEMS AND REQUESTING A RETURN MERCHANDISE AUTHORIZATION (RMA) NUMBER.

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