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INSTRUCTION MANUAL

Sensoray Model 621/721

Digital I/O Board

SENSORAY

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Limited Warranty

Sensoray Company, Incorporated (Sensoray) warrants the Model 621/721 hardware to be free from defects in material and workmanship and perform to applicable published Sensoray specifications for two years from the date of shipment to purchaser. Sensoray will, at its option, repair or replace equipment that proves to be defective during the warranty period. This warranty includes parts and labor.

The warranty provided herein does not cover equipment subjected to abuse, misuse, accident, alteration, neglect, or unauthorized repair or installation. Sensoray shall have the right of final determination as to the existence and cause of defect.

As for items repaired or replaced under warranty, the warranty shall continue in effect for the remainder of the original warranty period, or for ninety days following date of shipment by Sensoray of the repaired or replaced part, whichever period is longer.

A Return Material Authorization (RMA) number must be obtained from the factory and clearly marked on the outside of the package before any equipment will be accepted for warranty work. Sensoray will pay the shipping costs of returning to the owner parts that are covered by warranty.

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Special Handling Instructions

The Model 621/721 circuit board contains CMOS circuitry that is sensitive to Electrostatic Discharge (ESD).

Special care should be taken in handling, transporting, and installing the model 621/721 to prevent ESD damage to the board. In particular:

? Do not remove the circuit board from its protective anti-static bag until you are ready to configure the board for installation.

? Handle the circuit board only at grounded, ESD protected stations.

? Remove power from the PCI system before installing or removing the circuit board.

1. Introduction

The Sensoray model 621/721 is a 72 channel digital I/O card. The features include:

? 72 digital I/O channels.

? 64 channels have edge detection and interrupt capability.

? 8 channels have input latch and output enable capability.

? 64 I/O channels are grouped in eight blocks of eight channels. 8 I/O channels are grouped in two blocks of four channels. Each block may be programmed as inputs or outputs.

Model 621 is a PCI card, while model 721 is a Compact PCI card. Aside from differences in their target platforms and board layouts, these two products are identical.

The 621/721 is powered from the 5V supply of the system bus. No auxiliary power supplies are required. Low power circuitry is used to minimize system power consumption and enhance reliability.

A high-density connector on the card's front panel is provided for connecting the I/O channels to external circuitry. A solid state relay board (such as Sensoray model 720RB) may be used to facilitate field wiring.

Block Diagram

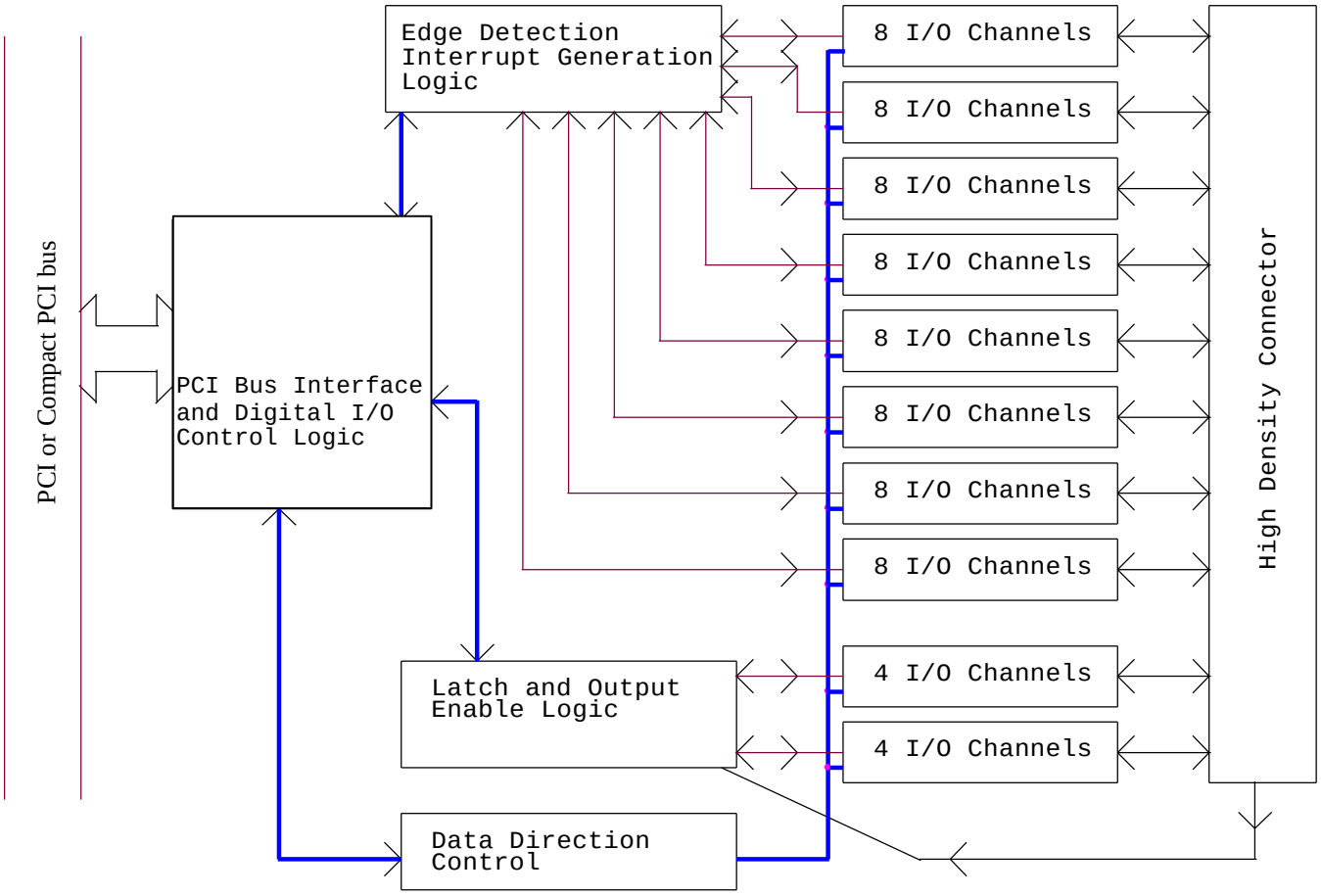


Figure 1

2. Installation

The installation of the Model 621/721 into a PCI or Compact PCI system is straight forward as no special adjustment (jumpers) are required. Follow the directions given in the 621/721 programming guide.

3. Reset

After a system reset or at power up the 621/721 is in its default state:

? Global interrupt enable (GIE) is disabled
? Channel interrupt enables are disabled
? Event capture enables are indeterminate
? Edge polarity selections are indeterminate
? All I/O channels are all set to input mode
? Output registers are indeterminate
? Channel 64 through 71 are set to simple I/O mode (no latching/output enable)
? Light emitting diode 'D1' will be on (controlled by LOE bit, which is set to zero).

4. Device and Vendor Identification

This is the information that identifies a 621/721 board in the PCI system.

Device ID:	9050	Sub Device ID:	6000
Vendor ID:	10B5	Sub Vendor ID:	0001

5. Digital I/O Interface

5.1 Overview

The 621/721 board provides 72 digital I/O (DIO) channels. 64 of the channels have edge detection capability, and eight channels have Input Latch and 3-state Output Enable capability.

DIO channels 0 to 63 are divided into eight groups of eight channels. Each group may be configured either as inputs or outputs by programming the associated data direction register (DDR). These 64 channels have the ability to detect and capture edge transition events. Each channel may be independently to capture either positive or negative edges. A captured event may optionally generate an interrupt.

DIO channels 64 to 71 are divided into two groups of four channels. Each group can be configured either as inputs or outputs by programming its associated data direction register (DDR). In addition to the standard DIO mode, a Latch/Output Enable (LOE) mode is available for channels 64 to 71. Setting the latch enable register (LOE) enables this mode, which applies to all eight channels. The LOE mode enables the DIO input signals (on channels 64 to 71) to be latched by asserting the LATCH signal; the latched data may be read at any time. In addition, the outputs in this mode are tri-stated unless the user asserts the OUTEN input line.

5.2 Registers

I/O bank 0 I/O port **Offset: 00 hex – Read/Write**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I/O CHANNELS 0-31																															

I/O bank 1 I/O port **Offset: 04 hex – Read/Write**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I/O CHANNELS 32-63																															

I/O bank 2 I/O port **Offset: 08 hex – Read/Write**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**I/O CHANNELS 64-71**							

Bank 0 edge capture flags **Offset: 0C hex – Read only**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPTURE FLAGS CHANNELS 0-31																															

Bank 1 edge capture flags **Offset: 10 hex – Read only**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPTURE FLAGS CHANNELS 32-63																															

Bank 0 interrupt flags **Offset: 14 hex – Read only**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTERRUPT FLAGS CHANNELS 0-31																															

Bank 1 interrupt flags **Offset: 18 hex – Read only**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTERRUPT FLAGS CHANNELS 32-63																															

Bank 0 edge select register **Offset: 1C hex – Read/Write**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EDGE SELECT REGISTERS CHANNELS 0-31																															

Bank 1 edge select register **Offset: 20 hex – Read/Write**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EDGE SELECT REGISTERS CHANNELS 32-63																															

Bank 0 arm capture register **Offset: 24 hex – Read/Write**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ARM CONTROL REGISTERS CHANNELS 0-31																															

Bank 1 arm capture register **Offset: 28 hex – Read/Write**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ARM CONTROL REGISTERS CHANNELS 32-63																															

Bank 0 interrupt enable register **Offset: 2C hex – Read/Write**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTERRUPT ENABLE REGISTERS CHANNELS 0-31																															

Bank 1 interrupt enable register **Offset: 30 hex – Read/Write**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTERRUPT ENABLE REGISTERS CHANNELS 32-63																															

Data direction/Misc./Status register **Offset: 34 hex – Read/Write**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GIRQ*	X	X	X	IRQ3*	IRQ2*	IRQ1*	IRQ0*	CAP3*	CAP2*	CAP1*	CAP0*	X	X	**LOE**	GIE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ARM	**X**	**X**	**X**	**X**	**X**	**DDR9 68-71**	**DDR8 64-67**	**DDR7 56-63**	**DDR6 48-55**	**DDR5 40-47**	**DDR4 32-39**	**DDR3 24-31**	**DDR2 16-23**	**DDR1 8-15**	**DDR0 0-7**

Bits marked with an * are read only.

5.2.1 I/O Ports

Reading an I/O port returns either the input logic level (input mode) or the state of the output register (output mode).

The DDR registers are used to set a particular I/O group to function as either inputs or outputs. The DDR bits affect the I/O channels as shown in the table below.

DDR9	DDR8	DDR7	DDR6	DDR5	DDR4	DDR3	DDR2	DDR1	DDR0
CHANNELS 68-71	CHANNELS 64-67	CHANNELS 56-63	CHANNELS 48-55	CHANNELS 40-47	CHANNELS 32-39	CHANNELS 24-31	CHANNELS 16-23	CHANNELS 8-15	CHANNELS 0-7

If a DDR bit is set to zero the associated channels will be inputs. When a DDR bit is set to one the associated channels will be outputs.

A channel's output register will be immediately output when a channel is first configured as an output. To avoid unwanted output levels when configuring DIOs as outputs, preset the output registers (write to the associated channels) with desired values before configuring as outputs.

Note: The values read and written to the I/O ports are true (i.e. not inverted).

5.2.2 Latch/Output Enable Mode

Latching and Output Enable is available on channels 64-71.

When the LOE bit (bit 17) of the "Data direction/Misc./Status" register is set to one, LOE mode is in effect. In this mode, data present on input channels 64-71 is latched into a holding register when the LATCH input signal is asserted low. The host may read latched data at any time. Additionally, output channels are tri-stated while the OUTEN input signal is asserted high.

Note: Channels 64-71 behave as standard DIOs when LOE is not set to one.

The light emitting diode 'D1' is linked to the LOE bit of the "Data direction/Misc./Status" register. The LED is on when LOE is set to zero, and off when LOE is set to one.

5.2.3 Edge Type Select Register (channels 0-63)

Input channels may be configured to detect either rising or falling edge transitions. Set the bits in the "edge select" to "0" to detect rising edges for the associated relay channels, or to "1" to detect falling edges.

5.2.4 Arming & Disarming Capture (channels 0-63)

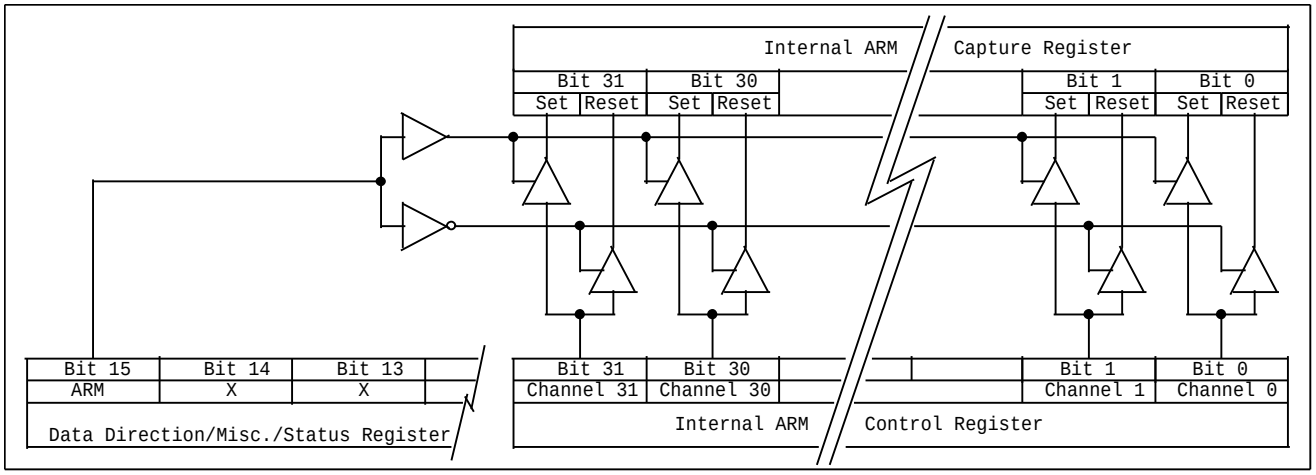


Figure 2

A relay channel must be "armed" before it will capture a detected edge.

An internal ARM Capture register is used to arm or disarm edge capturing. A “1” in the corresponding channel position will allow edge capturing while a “0” will disable edge capturing on that channel.

The host system does not have direct access to this register. It is written to using the ARM Control register and the “ARM” bit of the “Data direction/Misc./Status” register.

If ARM bit = “1”: All channels whose corresponding bit in the ARM Control register is a “1” are armed. Those channels with a “0” in the ARM Control register remain unchanged.

If ARM bit = “0”: All channels whose corresponding bit in the ARM Control register is a “1” are disarmed. Those channels with a “0” in the ARM Control register remain unchanged.

See Figure 2 for a diagram of the process.

Reading the “ARM Control” register accesses the internal ARM Capture register directly and will give the current status of the register. A “0” means that channel is disabled while a “1” shows it is armed.

If a channel is armed for edge capture and the same channel is set for output, a change in output level could result in a captured event. Unless you want a “loop-back” event, a channel set for output should have capturing disabled.

5.2.6 Edge Capture Flag Register (channels 0-63)

Each channel is associated with a one-bit capture register. The capture register is responsible for logging the occurrence of a detected edge. When a selected edge occurs while capture is enabled, the associated capture flag is set. All of the capture flags can be read through the edge capture flag port.

Note: before the capture register can log a detected edge, the channels capture register must be armed. After capturing an edge, the capture register remains set until explicitly reset (cleared) by the host.

5.2.7 Clearing Captured Edges

Sometime after a captured edge is detected, it is necessary to reset the associated capture register. This is accomplished by disarming the associated “arm capture” register.

6. Interrupts

6.1 Overview

I/O channels 0-63 may be individually programmed to request interrupt service upon capture of a selected edge. A channel must have its interrupt enabled before it will generate an interrupt in response to a captured edge. When an interrupt occurs the interrupt service routine needs to check all of the interrupt flags as there may be more that one pending DIO interrupt.

6.2 DIO Interrupt Enable/Disable

DIO channels may be individually programmed to request interrupt service upon capture of a detected edge. Modify a channel's interrupt enable by writing a one to the corresponding interrupt enable register. Set the associated bit in the Interrupt Enable register to zero or one to disable or enable, respectively, the channel's interrupt.

6.4 Global Interrupt Enable/Disable

Clearing this bit in the DDR/Misc. register will disable all interrupts simultaneously. Setting the bit will allow enabled interrupts to generate a system interrupt. When GIE is disabled, interrupts are prevented from reaching the PCI bus host, regardless of other Model 621/721 interrupt enable states (i.e. I/O channel interrupt enables). If interrupts are to be recognized, GIE must be enabled.

6.5 Interrupt Request Flags

A one in the Interrupt Flag register indicates that an interrupt has occurred on the associated channel.

6.3 Clearing an Interrupt Request Flag

A channel's interrupt request flag is cleared by clearing its associated capture register. This is accomplished by clearing the associated Arm Capture register. See the section Clearing Captured Edges.

Appendix A: Specifications

General

Interface	Parameter	Description
Bus	Type	PCI/ Compact PCI, 32-bit, 33MHz
	Address requirements	I/O registers: 56-bytes memory address block, PCI configuration registers require an additional amount.
I/O	Input characteristics	TTL/CMOS compatible.

Limits

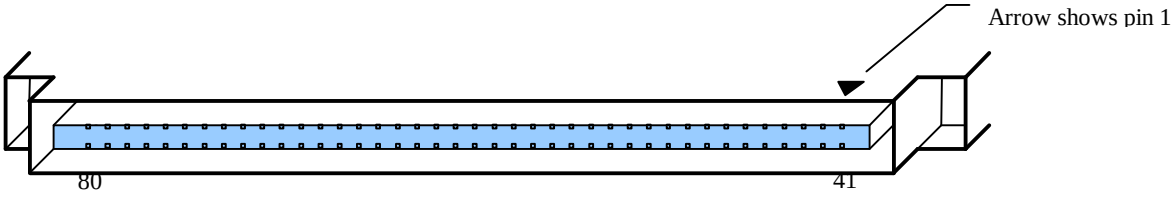
	Parameter	Typical	Min	Max	Units
I/O	Output sink current			20	mA
	Output source current			20	mA
	Input current			?10	uA
	Total output current (all outputs)			500	mA
	LATCH strobe pulse width	125			ns
	OUTEN strobe pulse width	125			ns
	Captured pulse width		100		ns
	Transfer rate			8	MHz
Power	Operating range		+4.75	+5.25	V
	Quiescent current	200			mA
Temperature	Operating range		0	70	C

Appendix B: Accessories

Custom cables and breakout boards available for this product. Contact sales@sensoray.com or visit www.sensoray.com for details.

The mating connector for models 621 and 721 is Robinson Nugent (www.robinsonnugent.com/) part number P50E-080S-TG. The PCB-mounted connector is Robinson Nugent part number P50E-080P-1-SR1-TG. This connector is used with 2 separate pieces of standard .100" ribbon cable, each containing 40 conductors.

Appendix C: Connector Pinout



PIN	FUNCTION		PIN	FUNCTION
1	GND		41	I/O 37
2	I/O 0		42	I/O 38
3	I/O 1		43	I/O 39
4	I/O 2		44	I/O 40
5	I/O 3		45	I/O 41
6	I/O 4		46	I/O 42
7	I/O 5		47	I/O 43
8	I/O 6		48	I/O 44
9	I/O 7		49	I/O 45
10	I/O 8		50	I/O 46
11	I/O 9		51	I/O 47
12	I/O 10		52	GND
13	I/O 11		53	I/O 48
14	I/O 12		54	I/O 49
15	I/O 13		55	I/O 50
16	I/O 14		56	I/O 51
17	I/O 15		57	I/O 52
18	GND		58	I/O 53
19	I/O 16		59	I/O 54
20	I/O 17		60	I/O 55
21	I/O 18		61	I/O 56
22	I/O 19		62	I/O 57
23	I/O 20		63	I/O 58
24	I/O 21		64	I/O 59
25	I/O 22		65	I/O 60
26	I/O 23		66	I/O 61
27	I/O 24		67	I/O 62
28	I/O 25		68	I/O 63
29	I/O 26		69	GND
30	I/O 27		70	LATCH
31	I/O 28		71	I/O 64
32	I/O 29		72	I/O 65
33	I/O 30		73	I/O 66
34	I/O 31		74	I/O 67
35	GND		75	I/O 68
36	I/O 32		76	I/O 69
37	I/O 33		77	I/O 70
38	I/O 34		78	I/O 71
39	I/O 35		79	OUTEN
40	I/O 36		80	GND

Figure 4

Appendix D: Technical Support

For technical support contact Sensoray Company Inc.

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Fax: (503) 684-8164

Email: support@sensoray.com

Web: www.sensoray.com

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