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SI-MOD66xx



The SI-MOD66xx Expansion I/O Module.

Description | Diagrams | Software Support | Technical Specifications | Ordering Information

DESCRIPTION

The SI-MOD66xx is a family of high resolution, multi function data acquisition and control modules that plug into any SI-CxDSP carrier processor card for the PCI bus.

- Up to 64SE/32DE Analog Inputs, 100khz/250khz sampling, 16 bit resolution, 1-100 gains.
- Up to 16 Analog Outputs, 180khz update rates, 16 bit resolution.
- On board 32KByte EEPROM contains offset/gain errors, loaded to FPGA for real time digital calibration on all analog I/O.
- 2 ports of 16 bit digital I/O (32 lines total).
- 2 configurable ports of 2 bit digital I/O (4 lines total):
  - 2 Quadrature Encoder inputs, CW/CCW 32 bit position counter, x1/x2/x4 modes, 37.5Mhz sampling.
  - 2 Pulse inputs for accurately measuring frequency.
  - 2 PWM outputs, up to 18.75Mhz/53ns resolution.

- Extremely flexible timing with 2 onboard DDSes, 4 Event Counters, and routing matrix allowing a myriad of clocking schemes.
- Small 3.7″x3.7″ form factor.
- Software development tools from Sheldon Instruments includes QuVIEW, QuBASE and the SI-DDKs; as well compatibility with separately purchased TI and third party tools.
- Windows and Linux 32/64 bit drivers and sample application support.

Analog Inputs

Each card features either 8DE/16SE, 16DE/32SE or 32DE/64SE analog input channels. Every group of 8DE/16SE channels is comprised of its own multiplexer, programmable gain instrumentation amplifier and ADC circuitry. Up to four (4) distinct channels, one from each group, can be simultaneously sampled. The ADC resolution is 16 bits, each with sampling rates ranging from 0hz to 100khz/250khz, or an additive rate of 400khz/1Mhz respectively. The maximum input voltage level is between ±10Vp (or ±9.5Vp for the "HG" or high gain option), with gains controlled by a precision differential instrumentation amplifier ranging from 1, 2, 5, 10, along with an optional 20, 50, and 100 for the "HG" option. The ADCs are based on a Successive Approximation architecture, which makes them ideal for control applications. Each input's termination can be individually programmed for differential or single ended operation, thereby not limiting you to an all-or-nothing configuration.

Analog Outputs

Additionally, up to sixteen (16) analog outputs can each update at rates up to 180khz, with 16 bits of resolution. These bipolar outputs have a maximum ±10Vp range, along with a 1-pole smoothing filter.

Digitally Controlled Calibration

An on board 32KByte EEPROM contains the offset and gain errors which are loaded into the FPGA and used to implement real time digital calibration on all analog I/O.

Timing

The sample clock can be derived internally or externally. If derived internally from the onboard timing circuitry, either several traditional divide by N counters or a pair of onboard Direct Digital Synthesizers (DDSes) may be used. The DDSes provide programmable sampling rates with precision up to ±1hz resolution. An externally sourced sample clock can also be used to accommodate a variety of sampling schemes. All ADC sample clocks are routed to an external connector in the case that multiple cards need to be synchronized to a common clock.

Digital I/O

Thirty six (36) general purpose, highly flexible digital I/O lines are also available, with thirty two (32) lines configured as a pair bidirectional, buffered 16 bit ports, and the other four (4) which can also double as a pair of Quadrature Encoder inputs, or as a set of four (4) individual Pulse I/Os lines. These lines are in addition to any of the digital I/O lines native to the DSP carrier card, such as its own serial ports and timers.

APPLICATIONS

- Unmanned Aerial Vehicle Control Systems

- Industrial Control and Automation
- Additive Manufacturing
- Military and Aerospace
- Test and Measurement

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