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SHELDON INSTRUMENTS

SI-MOD66xx User's Guide

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1.0 Introduction

The SI-MOD66xx is a family of high resolution, multifunction data acquisition and control cards that plug into the SI-CxDSP processor card for the PCI bus. A full line of software development tools are available from Sheldon Instruments and TI, which include graphical virtual instrumentation, compilers, assemblers, linkers, as well as a real-time source debugger.

This manual describes the SI-MOD66xx-PCI board, its features and design details. Use this manual in conjunction with the SI-CxDSP-PCI processor card manual.

1.1 Key Features

- Daughter module to the SI-CxDSP card, forming a DSP based multifunction I/O card.
- 1 to 4 groups of 16 channels, complete with multiplexer, instrumentation amplifier coupled with a programmable gain amplifier, and ADC, for a total of 8DE/16SE, 16DE/32SE, or 32DE/64SE channels of analog inputs, 16 bits resolution.
- Up to 100khz/250khz sampling per MUX-PGA-ADC group.
- Routable clock sources include a pair of internal DDSes (±1hz resolution), up to 4 independent Event Counters, a pair of Quadrature Encoders, as well as a pair of pulse inputs and PWM outputs.
- Up to 16 analog outputs, 12, 14, or 16 bits resolution.
- On board 32KByte EEPROM contains offset/gain errors, loaded to FPGA for real time digital calibration on all analog I/O.
- 32 Digital I/O lines.
- 2 Quadrature Encoder inputs, CW/CCW 32 bit position counter, x1/x2/x4 modes, 37.5Mhz sampling.
- 2 Pulse inputs for accurately measuring frequency.
- 2 PWM outputs, up to 18.75Mhz/53ns resolution.
- Extremely flexible timing with 2 onboard DDSes, 4 Event Counters, and routing matrix allowing a myriad of clocking schemes.
- Small convenient 3.7"x3.7" form factor.
- Software development tools from Sheldon Instruments includes QuVIEW, QuBASE and the SI-DDKs; as well compatibility with separately purchased TI and third party tools.
- Windows and Linux 32/64 bit drivers and sample application support.
- Analog signals easily accessible through 100 pin half pitch DSub (AMP-SCSI style) connector, digital signals accessible through a separate standard 40 pin IDC connector.

1.2 Analog Inputs

Each card features either 8DE/16SE, 16DE/32SE or 32DE/64SE analog input channels. Every group of 8 differential or 16 single ended channels is comprised of its own multiplexer set (DG409), a two stage programmable gain amplifier (Analog Devices AD8250) and ADC circuitry (Burr-Brown ADS8320 or Linear Technology LTC1864). Up to four (4) distinct channels, one from each group, can be simultaneously sampled.

The maximum input voltage level is between ±10Vp, followed by a two stage amplifier that

combine to yield gains ranging from 1 to 1,000. The first stage is implemented with a precision differential instrumentation amplifier with gains ranging from 1, 2, 5 and 10 (Analog Devices AD8250), while the optional second stage is implemented with a the same precision amplifier with gains of 1, 2, 5, and 10 (AD8250) or with an amplifier with gains of 1, 10, 100, and 1000 (Analog Devices AD8253).

The ADC resolution is 16 bits, each with sampling rates ranging from 0hz to 100khz/250khz, for an additive rate of 400khz/1Mhz respectively, with ±1hz resolution. The ADCs are based on a Successive Approximation architecture, which makes them ideal for control applications (100khz ADC: Burr-Brown ADS8320 or ADS8325; 250khz ADC: Linear Technology LTC1864). Each channel can be individually configured for single or differential ended operation.

The ADC values are buffered in the SRAM, with the respective channel numbers serving as the SRAM address offsets to be accessed by the DSP. Every time an entire channel list is digitized, an interrupt (X_INT0) is generated signaling the DSP that data is ready. In this manner, the DSP simply reads the channels of interest, as it would read any other data on its bus, in a synchronized fashion. The ADC results are stored as a 16 bit, 2's complement signed integer.

1.3 Analog Outputs

Up to sixteen (16) analog outputs can each update at rates up to 180khz, with resolution from 12, 14, and 16 bits (Linear Technology LTC2620, LTC2610, and LTC2600 respectively). These bipolar outputs have a maximum ±10Vp range, along with a 2-pole linear phase smoothing filter. They are mapped directly on the DSP's primary bus. The DAC data is written as a 16 bit, 2's complement signed integer.

1.4 Autocalibration with EEPROM

An on board 32KByte EEPROM contains the factory set offset and gain errors which are loaded into the FPGA and used to implement real time digital calibration on all analog I/O.

The EEPROM values are programmatically transferred to an FPGA buffer which is used to adjust all ADC/DAC values in real time without processor intervention. The EEPROM values may be periodically updated. An I2C interface serves as a link between the EEPROM and the FPGA.

1.5 Sample Clock Timers

Sample clock timing can be derived from a routing matrix allowing the choice between several onboard circuits or from several external sources.

The onboard sample clock timers include the choice between:
1) A pair of Direct Digital Synthesizer (DDS) with a 27 bit resolution Phase Accumulator, with a 37.5Mhz reference clock yielding ±1hz resolution.
2) Up to four cascadable, 16 bit Event Counters that operate as traditional 'divide by N' counters, each with their own routing matrix for deriving an independent clocking source. The counter

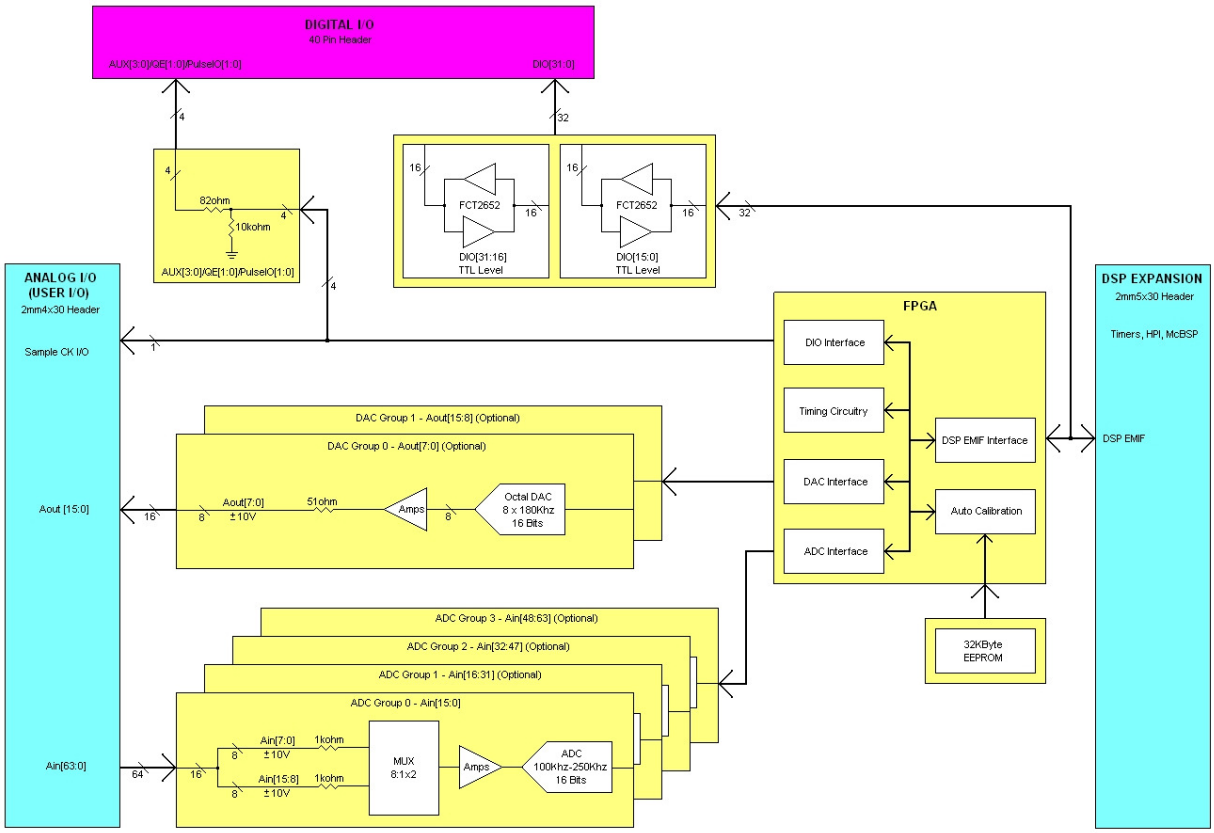
simply increments by integer values on every reference clock transition until a desired, 16 bit preset 'Count' value is reached, at which time a pulse will occur marking the desired sample period.

The external clocking sources include:
1) A dedicated digital I/O pin that may be configured to either operate as a source for other devices external to the SI card, or as an input to a user supplied TTL/CMOS level signal, ideal to accommodate a variety of sampling schemes. The external sample clock is taken from the external 100 pin connector.
2) A pair of very flexible Quadrature Encoders, with edge detection running at the 37.5Mhz clock, available on the 40 pin IDC connector.
3) A pair of Pulse inputs that may also be used as frequency measurement devices.

1.6 Digital I/O

Thirty six (36) general purpose, highly flexible digital I/O lines are also available, with thirty two (32) lines configured as a pair of bidirectional, buffered 16 bit ports that 3.3V and 5V tolerant; and the other four (4) which can also double as a pair of Quadrature Encoder inputs, or as a set of four (4) individual PWM I/Os lines that are only 3.3V tolerant.

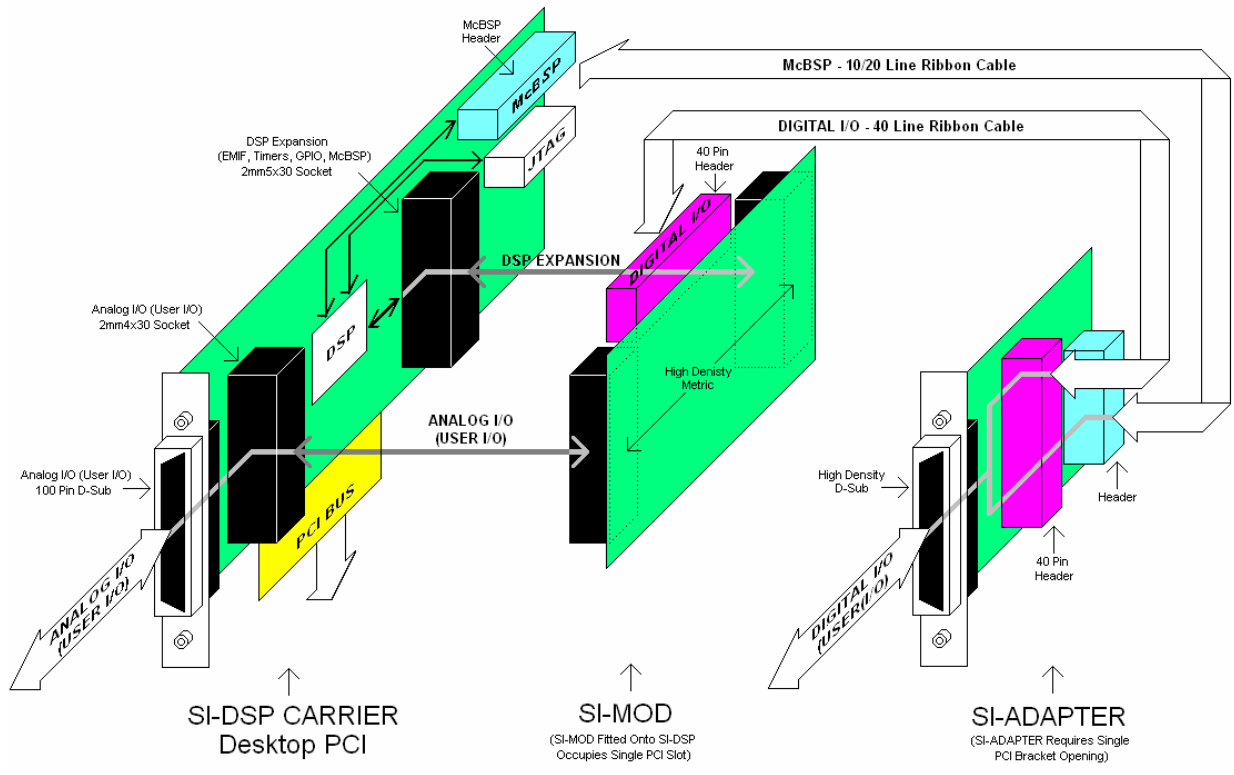
These lines are in addition to any of the digital I/O lines native to the DSP carrier card, such as its own serial ports and timers. Please refer to TI's TMS320Cx reference manual for further details.



SI-MOD6x Block Diagram

1.7 Software Support

All functions for the SI-MOD66xx are fully programmable with QuVIEW and QuBASE, which are a set of DSP-resident libraries for real time performance that greatly accelerate data acquisition, signal processing, and control applications. QuVIEW is a real time accelerator for LabVIEW, and QuBASE a real time accelerator for Visual Basic. A full range of examples and tutors are provided to demonstrate their ease of use and breadth of functionality and capabilities. Complete driver support for Windows and Linux 32/64 bit environments.



2.0 Register Mapping

All of the SI-MOD66xx components are mapped into the base of the DSP's expansion bus. These components are initialized to a dormant state upon reset, and must be configured to a desired mode of operation before any tasks are to be performed. Please refer to the DSP's manual for each card's expansion base address location. Below is a complete summary of registers:

Registers	DSP Address-DWord Boundary (HEX)	DSP Address-Byte Boundary (HEX)	Depth x Width (Bits)	Direction	Initial Value
ADC[63:0]	Base+0x000 thru Base+0x03F	Base+0x000 thru Base+0x3FC	64 x 16	R	0x0
DAC[15:0]	Base+0x100 thru Base+0x10F	Base+0x400 thru Base+0x7FC	16 x 16	W	0x0
Control/Status Registers	Base+0x200 thru Base+0x250	Base+0x800 thru Base+0x940	80 x 32	R/W	0x0
Scan Table/Input Parameters	Base+0x300 thru Base+0x30F	Base+0xC00 thru Base+0xC3C	16 x 32	R/W	0x0

Note: *The expansion base address for the SI-DSP cards are as follows:*
a) SI-C3xDSP: 0xFE0000, DWord boundary.
b) SI-C671xDSP: 0x80380000, byte boundary.

3.0 Control/Status Registers

Several Control/Status Registers manage separate sections of overall board functionality as outlined in the following sections.

Register	DSP Address-Dword Boundary (HEX)	DSP Address-Byte Boundary (HEX)	Width (Bits)	Direction	Initial Value
FPGA VERSION	Base+0x200	Base+0x800	32	R	0x0
TIMING_CSR	Base+0x201	Base+0x804	32	R/W	0x0
EC[0:3]_CSR	Base+0x202 thru Base+0x205	Base+0x808 thru Base+0x814	32	R/W	0x0
EC[0:3]_CNT_LIMIT	Base+0x206 thru Base+0x209	Base+0x818 thru Base+0x824	16	R/W	0x0
EC[0:3]_CNT_VALUE	Base+0x20A thru Base+0x20D	Base+0x828 thru Base+0x834	16	R	0x0
INT_DDS[0:1]_PADATA	Base+0x210 thru Base+0x211	Base+0x840 thru Base+0x844	27	R/W	0x0
I2C_CSR	Base+0x213	Base+0x84C	32	R/W	0x0
I2C_DATA_REG	Base+0x214	Base+0x850	32	R/W	0x0
DAC_CSR	Base+0x220	Base+0x880	32	R/W	0x0
DIO_CSR	Base+0x224	Base+0x890	32	R/W	0x0
DIO_PORT (32 Bits)	Base+0x225	Base+0x894	32	R/W	N/A
GPIO_CSR	Base+0x228	Base+0x8A0	32	R/W	0x0
GPIO_COUNTER32	Base+0x229	Base+0x8A4	32	R/W	0x0
AUX_DIO_CSR	Base+0x22C	Base+0x8B0	32	R/W	0x0
AUX_DIO_PORT (4 Bits)	Base+0x22D	Base+0x8B4	32	R/W	0x0
PULSEIO_CSR	Base+0x230	Base+0x8C0	32	R/W	0x0
PULSEIN0_CSR[0:3]	Base+0x231 thru Base+0x234	Base+0x8C4 thru Base+0x8D0	32	R/W	0x0
PWMOUT0_[LOCOUNT: HICOUNT]	Base+0x235 thru Base+0x236	Base+0x8D4 thru Base+0x8D8	32	R	0x0
PULSEIN1_CSR[0:3]	Base+0x237 thru Base+0x23A	Base+0x8DC thru Base+0x8E8	32	R/W	0x0
PWMOUT1_[LOCOUNT:HICOUNT]	Base+0x23B thru Base+0x23C	Base+0x8EC thru Base+0x8F0	32	R	0x0
QE_CSR	Base+0x250	Base+0x940	32	R/W	0x0

3.1 FPGA_VERSION

Register Name		Description	DSP Address-DWord Boundary (HEX)	DSP Address-Byte Boundary (HEX)
FPGA_VERSION		Returns the hardware revision of the onboard FPGA, along with the ADC circuitry in place.	Base+0x200	Base+0x800
Bit Position	**Name**	**Description**	**Direction**	**Initial Value**
31:30	ADC Circuit	00 (0x0) = N/A 01 (0x1) = LTC1864 (250khz) 10 (0x2) = ADS8320/5 (100khz) 11 (0x3) = N/A	R	Determined by hardware.
29:0	FPGA Revision	TBD	R	TBD

3.2 TIMING_CSR

Register Name		Description	DSP Address-DWord Boundary (HEX)	DSP Address-Byte Boundary (HEX)
TIMING_CSR		Timing Control/Status register. Manages timing circuitry as well as interrupt resources to the DSP.	Base+0x201	Base+0x804
Bit Position	**Name**	**Description**	**Direction**	**Initial Value**
31	XINT1_EN	Enables XINT1 to the DSP, which is triggered by one of the resources selected from XINT1_SRC. 0 = XINT1 Enabled (default). 1 = XINT1 Disabled.	R/W	0
30:29	N/A	N/A	N/A	0
28:25	XINT1_SRC	XINT1n trigger source selector. 0000 (0x0) = Internal DDS0 (default). 0001 (0x1) = Internal DDS1. 0010 (0x2) = External DDS. From optional AD9850 circuit. 0011 (0x3) = External clock. Derived from pin 100 on Analog I/O connector. ***NOTE:*** *Please check status of this register's 'bit 1' defined below, which must be set as an input.* 0100 (0x4) = EC0. 0101 (0x5) = EC1. 0110 (0x6) = EC2. 0111 (0x7) = EC3. ***NOTE:*** *An XINT1 event is triggered after the selected Event Counter reaches its own threshold.* 1000 (0x8) = GPIO0. 1001 (0x9) = GPIO1.	R/W	0

		1010 (0xA) = GPIO2. 1011 (0xB) = GPIO3. ***NOTE:*** *Irrespective of the operation selected for GPIO[3:0] (Auxiliary I/O, Pulse I/O or Quadrature Encoder), XINT1n only looks for LO-HI transitions.* 1100 thru 1111 (0xC thru 0xF) = N/A.		
24:16	N/A	N/A	N/A	0
15	XINT0_EN	Enables XINT0 to the DSP, which is triggered by one of the resources selected from XINT0_SRC or ADC_SAMPLE_SRC. 0 = XINT0 Enabled (default). 1 = XINT0 Disabled.	R/W	0
14:13	SAMPLE_MODE	Selects the manner in which the transition of a selected ADC sample clock source triggers an ADC reading. 00 thru 01 (0x0 thru 0x1) = Multiplexed (default). The sample source transition triggers an individual ADC sample reading. 10 (0x2) = Pseudo simultaneous, default maximum of 250khz/100khz. The sample source transition triggers a single reading of all channels listed in the scan table at the ADC's default maximum rate. Useful for sampling schemes requiring minimal time base skew between adjacent ADC readings. 11 (0x3) = Pseudo simultaneous, divide maximum by ½ or 125khz/50khz. The sample source transition triggers a single reading of all channels listed in the scan table at half of the ADC's default maximum rate. Useful for sampling schemes requiring minimal time base skew between adjacent ADC readings.	R/W	0
12:9	XINT0_SRC or ADC_SAMPLE_SRC	ADC sample source selector which also triggers XINT0 to DSP. 0000 (0x0) = Internal DDS0 (default). 0001 (0x1) = Internal DDS1. 0010 (0x2) = External DDS. From optional AD9850 circuit. 0011 (0x3) = External clock. Derived from pin 100 on Analog I/O connector. ***NOTE:*** *Please check status of this register's 'bit 1' defined below, which must be set as an input.* 0100 (0x4) = EC0. 0101 (0x5) = EC1. 0110 (0x6) = EC2. 0111 (0x7) = EC3. ***NOTE:*** *An XINT0 event or ADC sample is triggered after the selected Event Counter reaches its own threshold.* 1000 (0x8) = GPIO0. 1001 (0x9) = GPIO1. 1010 (0xA) = GPIO2. 1011 (0xB) = GPIO3. ***NOTE:*** *Irrespective of the operation selected for GPIO[3:0] (Auxiliary I/O, Pulse I/O or Quadrature Encoder), XINT0 or the ADC only look for LO-HI*	R/W	0

		transitions. 1100 thru 1111 (0xC thru 0xF) = N/A.		
8:6	DDS1_CLK_SRC	Internal DDS1 sample clock source selector. 000 (0x0) = S/W or free run (default). 001 (0x1) = EC0 triggered. 010 (0x2) = EC1 triggered. 011 (0x3) = EC2 triggered. 100 (0x4) = EC3 triggered. ***NOTE:*** *DDS1 is synchronously enabled after the selected Event Counter reaches its own threshold.* 101 thru 111 (0x5 thru 0x7) = N/A.	R/W	0
5:3	DDS0_CLK_SRC	Internal DDS0 sample clock source selector. 000 (0x0) = S/W or free run (default). 001 (0x1) = EC0 triggered. 010 (0x2) = EC1 triggered. 011 (0x3) = EC2 triggered. 100 (0x4) = EC3 triggered. ***NOTE:*** *DDS0 is synchronously enabled after the selected Event Counter reaches its own threshold.* 101 thru 111 (0x5 thru 0x7) = N/A.	R/W	0
2	N/A (was SAMPLE_MODE)	N/A	N/A	0
1	EXTCLK_EN	Selects direction of an external clock source line on pin 100 of Analog I/O connector. 0 = Input (default). 1 = Output.	R/W	0
0	N/A (was EXT_DDS_RST)	N/A	N/A	0

3.3 EC0_CSR

Register Name		Description	DSP Address-DWord Boundary (HEX)	DSP Address-Byte Boundary (HEX)
EC0_CSR		Event Counter 0 Control/Status register.	Base+0x202	Base+0x808
Bit Position	**Name**	**Description**	**Direction**	**Initial Value**
31	S/W_PULSE	When accessed, a software trigger is created; useful in creating a software controlled trigger for the Event Counter. In order for a S/W trigger to occur, a LO-HI or HI-LO transition sequence must occur for the edge to be recognized. 0 = LO level on S/W trigger. 1 = HI level on S/W trigger.	R/W	0
30:13	N/A	N/A	N/A	0
12:8	EC0_CLK_SRC	Event Counter 0 tick clock source selector. 00000 (0x0) = Internal DDS0 (default). 00001 (0x1) = Internal DDS1. 00010 (0x2) = External DDS. From optional AD9850 circuit. 00011 (0x3) = External clock. Derived from pin 100 on Analog I/O connector. ***NOTE:*** *Please check status of the Timing_CSR's 'bit 1' defined above, which must be set as an input.* 00100 (0x4) = PULSE_I/O0. 00101 (0x5) = PULSE_I/O1. 00110 (0x6) = PULSE_I/O2. 00111 (0x7) = PULSE_I/O3. ***NOTE:*** *Irrespective of the operation selected for PULSE_I/O[3:0] (Pulse Input or PWM output), the Event Counter 0 only looks for edge transitions defined with this register's 'bit 3' below.* 01000 (0x8) = ECa. First available Event Counter. 01001 (0x9) = ECb. Second available Event Counter. 01010 (0xA) = ECc. Last available Event Counter. ***NOTE:*** *Note that Event Counters are cascadable.* 01011 (0xB) = DSP reference clock of 37.5Mhz. 01100 (0xC) = S/W Pulse. ***NOTE:*** *Derived from the transition of this register's 'bit 31' defined above.* 01101 thru 01111 (0xD thru 0xF) = N/A. 10000 (0x10) = QE0. 10001 (0x11) = QE1.	R/W	0

		10010 thru 11111 (0x12 thru 1F) = N/A.		
7	EC0_OUT	The output of the Event Counter 0 may be used as a synchronous source to trigger other devices. 0 = EC0 counting, threshold not reached. 1 = EC0 threshold reached. Asserted only for a single period of EC0's selected clock source.	R	0
6:4	N/A	N/A	N/A	0
3	EC0_POLARITY	Selects the polarity of the incoming clock source. 0 = Positive edge tick source (default). 1 = Negative edge tick source.	R/W	0
2	EC0_WRAP_MODE	Selects the mode of operation after the Event Counter has reached its threshold. 0 = Free running. Automatically wraps in order to restart the count after reaching its threshold/limit (default). 1 = Counts until threshold is reached. The threshold/limit value is latched and retained until either the EC0_CNT_LIMIT register is updated with a new value or if the Event Counter 0 is forcibly cleared by asserting the EC0_RESET bit of this register.	R/W	0
1	EC0_ENABLE	Enables or disables the selected clock that feeds the Event Counter 0. 0 = Enable clock source (default). Free runs, Event Counter 0 is actively counting. 1 = Disable clock source. Event Counter 0 is detained, but NOT cleared/reset	R/W	0
0	EC0_RESET	Asynchronously and forcibly clears the Event Counter 0 when asserted irrespective of its current state. 0 = Runs normally (default). 1 = Reset/Clear. Clears Event Counter 0 irrespective of state/enable line, does NOT clear the EC0_CNT_LIMIT register defined below.	R/W	0

3.4 EC[3:1]_CSR

These registers define the operation of the three remaining Event Counters, which operate identically to Event Counter 0 Control/Status register defined above.

3.5 EC0_CNT_LIMIT

Register Name		Description	DSP Address-DWord Boundary (HEX)	DSP Address-Byte Boundary (HEX)
EC0_CNT_LIMIT		Limit or threshold value for Event Counter 0.	Base+0x206	Base+0x818
Bit Position	**Name**	**Description**	**Direction**	**Initial Value**
31:16	N/A	N/A	N/A	0
15:0		Event Counter 0 limit or threshold value of 'n'. With n=0, the Event Counter 0 is disabled. With n≥1, the Event Counter 0 will have a valid threshold/limit value to reach. ***NOTE:*** *The 'n' value is treated as a comparative value for the Event Counter 0 to reach where the initial value of '0' is a valid starting point and is considered the 'first' tick. Therefore, a total of 'n+1' ticks must occur for the Event Counters to reach the threshold/limit. The EC0_OUT line will assert after the first 'tick', and then assert every time the threshold/limit is reached as defined in the EC0_CSR register.*	R/W	0

Triggerable Event Counter Notes:

1) The direction of the Event Counters is defined by the counter's clock source:
Direction: UP/DN for Quadrature Encoder inputs.
Direction: always 'UP' for PWM inputs.

2) Example for testing: If the 'threshold/limit' is set to a value of '1', only a single transition on the Event Counter's clock source can occur in order to assert its ECn_OUT output, thus creating the equivalent of an 'event marker'.

3.6 EC[3:1]_CNT_LIMIT

These registers define the threshold limits of the three remaining Event Counters, which operate identically to Event Counter 0 Limit defined above.

3.7 EC0_CNT_VALUE

Register Name		Description	DSP Address-Dword Boundary (HEX)	DSP Address-Byte Boundary (HEX)
EC0_CNT_VALUE		Current value read from Event Counter 0.	Base+0x20A	Base+0x828
Bit Position	**Name**	**Description**	**Direction**	**Initial Value**
31:16	N/A	N/A	N/A	0
15:0		Returns the current value of the internal count of EC0.	R	0

3.8 EC[3:1]_CNT_VALUE

These registers return the current count values of the three remaining Event Counters, which operate identically to Event Counter 0 Value defined above.

3.9 INT_DDS0_PADATA

Register Name		Description	DSP Address-Dword Boundary (HEX)	DSP Address-Byte Boundary (HEX)
INT_DDS0_PADATA		Phase Accumulator register for internal DDS0.	Base+0x210	Base+0x840
Bit Position	**Name**	**Description**	**Direction**	**Initial Value**
31:27	N/A	N/A	N/A	0
26:0		Phase accumulator value for the internal DDS0. When updated, the DDS0 begins generating a 50% duty cycle output.	R/W	0

3.10 INT_DDS1_PADATA

The second internal DDS1 operates identically to DDS0.

3.11 I2C_CSR

Register Name		Description	DSP Address-DWord Boundary (HEX)	DSP Address-Byte Boundary (HEX)
I2C_CSR		I2C EEPROM Control/Status register. *NOTE: Transfer of I2C EEPROM values to FPGA CalTable can only occur after the Scan Table has been updated since the values contained within the Scan Table determine the addresses of the I2C EEPROM.*	Base+0x213	Base+0x84C
Bit Position	**Name**	**Description**	**Direction**	**Initial Value**
31:16	I2C_ADDR[15:0]_SINGLE	I2C_ADDR[15:0] = Specifies I2C EEPROM address of a single value to be accessed. *NOTE: Only applicable with single value transfers between the host and I2C EEPROM, since a host application is used to update the I2C EEPROM.*	R/W	0
15:3	N/A	N/A	N/A	0
2	I2C_R/Wn_SINGLE	Selects the direction of the I2C EEPROM data access. *NOTE: Only applicable with single value transfers between the host and I2C EEPROM, since a host application is used to update the I2C EEPROM.* 0 = Write single value from host to I2C EEPROM. 1 = Read single value from I2C EEPROM to host.	R/W	0
1	I2C_TO_CALTBL_XFER_EN	Used to control the transfer of the entire table of gain and offset errors from the I2C EEPROM to the CalTable SRAM buffer inside of the FPGA. *NOTE:* *1) Not applicable for accesses between the host and the I2C EEPROM.* 2) *Transfer of the entire table I2C EEPROM values to FPGA CalTable can only occur after the Scan Table has been updated since the values contained within the Scan Table determine the addresses of the I2C EEPROM.* 0 = When read as a status bit, indicates a completed transfer of the entire I2C EEPROM to host, or none in progress. 1 = When written as a control bit, enables and initiates the transfer of the entire I2C EEPROM to the FPGA's CalTable SRAM buffer; when read as a status bit, indicates transfer is in progress. Bit is automatically cleared when complete.	R/W	0

0	I2C_ENABLE_SINGLE	Controls the flow of single accesses by host to the I2C EEPROM. *<u>NOTE:</u> Only applicable with single value transfers between the host and I2C EEPROM, since a host application is used to update the I2C EEPROM.* 0 = When read as a status bit, indicates a completed single access between I2C and host, or none in progress. 1 = When written as a control bit, enables and initiates a single access between the I2C EEPROM and the host; when read as a status bit, indicates the transfer is in progress. Bit is automatically cleared when complete.	R/W	0

3.12 I2C_DATA_REG

Register Name		Description	DSP Address-DWord Boundary (HEX)	DSP Address-Byte Boundary (HEX)
I2C_DATA_REG		Contains the data accessed between the host and the I2C EEPROM. *NOTE: Used for host->I2C transfers, I2C->host transfers are only available for convenience and verification.*	Base+0x214	Base+0x850
Bit Position	**Name**	**Description**	**Direction**	**Initial Value**
31:0	I2C_DATA[31:0]	I2C_DATA[31:0], only the lower 16 bits are used.	R/W	0

3.13 DAC_CSR

Not yet implemented.

3.14 DIO_CSR

Register Name		Description	DSP Address-DWord Boundary (HEX)	DSP Address-Byte Boundary (HEX)
DIO_CSR		Buffered Digital I/O port Control/Status register.	Base+0x224	Base+0x890
Bit Position	**Name**	**Description**	**Direction**	**Initial Value**
31:2	N/A	N/A	N/A	0
1	DIODIR_HW	Selects the direction of the high order 16 bit word on the buffered digital I/O port available on the dedicated digital I/O connector. 0 = HWord[31:16] is an input (default). 1 = HWord[31:16] is an output.	R/W	0
0	DIODIR_LW	Selects the direction of the low order 16 bit word on the buffered digital I/O port available on the dedicated digital I/O connector. 0 = LWord[15:0] is an input (default). 1 = LWord[15:0] is an output.	R/W	0

3.15 DIO_PORT

Register Name		Description	DSP Address-DWord Boundary (HEX)	DSP Address-Byte Boundary (HEX)
DIO_PORT		Buffered Digital I/O port registers.	Base+0x225	Base+0x894
Bit Position	**Name**	**Description**	**Direction**	**Initial Value**
31:0		Register access to all DIO bits available on dedicated digital I/O connector.	R/W	0

3.16 GPIO_CSR

Register Name		Description	DSP Address-DWord Boundary (HEX)	DSP Address-Byte Boundary (HEX)
GPIO_CSR		General Purpose I/O Control/Status register.	Base+0x228	Base+0x8A0
Bit Position	**Name**	**Description**	**Direction**	**Initial Value**
31:6	N/A	N/A	N/A	0
5:4	FREE_COUNTER_SRC	Selector for the clock source driving an internal free running, general purpose 32 bit counter used by both the Pulse I/O and Quadrature Encoder devices. 00 (0x0) = DSP reference clock of 37.5Mhz (default). 01 thru 11 (0x1 thru 0xF) = N/A.	R/W	0
3:2	GPIO[3:2]_SEL	Selects the mode of operation for the second GPIO pair available on pins 39 & 40 of the dedicated 40 pin digital I/O connector. 00 (0x0) = AUX_DIO[3:2] (default). 01 (0x1) = PULSEIO[2:3]. 10 (0x2) = QE1. 11 (0x3) = N/A.	R/W	0
1:0	GPIO[1:0]_SEL	Selects the mode of operation for the first GPIO pair available on pins 37 & 38 of the dedicated 40 pin digital I/O connector. 00 (0x0) = AUX_DIO[1:0] (default). 01 (0x1) = PULSEIO[1:0]. 10 (0x2) = QE0. 11 (0x3) = N/A.	R/W	0

3.17 GPIO_COUNTER32

Register Name		Description	DSP Address-DWord Boundary (HEX)	DSP Address-Byte Boundary (HEX)
GPIO_COUNTER		Current count value inside of the 32 bit general purpose counter.	Base+0x229	Base+0x8A4
Bit Position	**Name**	**Description**	**Direction**	**Initial Value**
31:0		Returns the current value of the internal free running 32 bit counter used by both the Pulse I/O and Quadrature Encoder devices.	R	0

3.18 AUX_DIO_CSR

Register Name		Description	DSP Address-DWord Boundary (HEX)	DSP Address-Byte Boundary (HEX)
AUX_DIO_CSR		Auxiliary Digital I/O port Control/Status register.	Base+0x22C	Base+0x8B0
Bit Position	**Name**	**Description**	**Direction**	**Initial Value**
31:1	N/A	N/A	N/A	0
0	AUX_DIO_DIR	Selects the direction of the Auxiliary Digital I/O port. ***NOTE:*** *Only applicable when the GPIO bits are configured to operate as an Auxiliary I/O port available on pins 37 through 40 of the dedicated 40 pin digital I/O connector.* 0 = Input (default). 1 = Output.	R/W	0

3.19 AUX_DIO_PORT

Register Name		Description	DSP Address-DWord Boundary (HEX)	DSP Address-Byte Boundary (HEX)
AUX_DIO_PORT		Auxiliary Digital I/O port register.	Base+0x22D	Base+0x8B4
Bit Position	**Name**	**Description**	**Direction**	**Initial Value**
31:4	N/A	N/A	N/A	0
3:0		Register access to all AUX_DIO bits available on dedicated 40 pin digital I/O connector.	R/W	0

3.20 PULSEIO_CSR

Register Name		Description	DSP Address-DWord Boundary (HEX)	DSP Address-Byte Boundary (HEX)
PULSEIO_CSR		Pulse I/O Control/Status register.	Base+0x230	Base+0x8C0
Bit Position	**Name**	**Description**	**Direction**	**Initial Value**
31:4	N/A	N/A	N/A	0
3	PWMOUT1_RESET	Asynchronously and forcibly clears the PWM Output 1 registers that are used to determine both the period and frequency of the generated output pulse train. ***NOTE:*** *Only applicable when the second set of GPIO bits [3:2] are configured to operate as a PULSEIO port available on pins 39 & 40 of the dedicated 40 pin digital I/O connector.* 0 = Runs normal free run (default). 1 = Reset/Clear. Clears the PWMOUT1 counter/value.	R/W	0
2	PULSEIN1_RESET	Asynchronously and forcibly clears the PULSE Input 1 registers that are read to determine both the period and frequency of the incoming pulse train. ***NOTE:*** *Only applicable when the second set of GPIO bits [3:2] are configured to operate as a PULSEIO port available on pins 39 & 40 of the dedicated 40 pin digital I/O connector.* 0 = Runs normal free run (default). 1 = Reset/clear. Clears the PULSEIN1 registers.	R/W	0
1	PWMOUT0_RESET	Asynchronously and forcibly clears the PWM Output 0 registers that are used to determine both the period and frequency of the generated output pulse train. ***NOTE:*** *Only applicable when the first set of GPIO bits [1:0] are configured to operate as a PULSEIO port available on pins 37 & 38 of the dedicated 40 pin digital I/O connector.* 0 = Runs normal free run (default). 1 = Reset/Clear. Clears the PWMOUT0 counter/value.	R/W	0
0	PULSEIN0_RESET	Asynchronously and forcibly clears the PULSE Input 0 registers that are read to determine both the period and frequency of the incoming pulse train. ***NOTE:*** *Only applicable when the first set of GPIO bits [1:0] are configured to operate as a PULSEIO port available on pins 37 & 38 of the dedicated 40 pin digital I/O connector.* 0 = Runs normal free run (default). 1 = Reset/clear. Clears the PULSEIN0 registers.	R/W	0

3.21 PULSEIN0_CSR[3:0]

Register Name		Description	DSP Address-DWord Boundary (HEX)	DSP Address-Byte Boundary (HEX)
PULSEIN0_CSR3		Last of four registers that are simultaneously latched and which contain three edge values along with a position indicator. When written, operates as a 'virtual' register. The action of writing causes all four PULSEIN0_CSRs to be registered. When read, 'bit 0' serves as an indicator to describe the order of the incoming pulses. ***NOTE:*** *A minimum of three edge values is required to compute both the period and frequency of an incoming pulse train. Therefore, this register must be first written before any reads occur in order to ensure that all four PULSEIN0_CSRs are coherent. Only applicable when the first set of GPIO bits [1:0] are configured to operate as a PULSEIO port. The PULSEIN0 signal is measured on pin 38 of the dedicated 40 pin digital I/O connector.*	Base+0x234	Base+0x8D0
Bit Position	**Name**	**Description**	**Direction**	**Initial Value**
31:1	N/A	N/A	N/A	0
0		When read, serves as an indicator to describe the order of the incoming edges. 0 = Rising/Falling/Rising. 1 = Falling/Rising/Falling.	R/W	0

Register Name		Description	DSP Address-DWord Boundary (HEX)	DSP Address-Byte Boundary (HEX)
PULSEIN0_CSR2		Third of four registers that are simultaneously latched and which contain three edge values along with a position indicator. This register returns the current value of the internal free running 32 bit counter indicating the time when the last of three edges occurred. ***NOTE:*** *A minimum of three edge values is required to compute both the period and frequency of an incoming pulse train. Only applicable when the first set of GPIO bits [1:0] are configured to operate as a PULSEIO port. The PULSEIN0 signal is measured on pin 38 of the dedicated 40 pin digital I/O connector.*	Base+0x233	Base+0x8CC
Bit Position	**Name**	**Description**	**Direction**	**Initial Value**
31:0		Current value of the internal free running 32 bit counter indicating the time when the last of three edges	R	0

		occurred.		

Register Name		Description	DSP Address-DWord Boundary (HEX)	DSP Address-Byte Boundary (HEX)
PULSEIN0_CSR1		Second of four registers that are simultaneously latched and which contain three edge values along with a position indicator. This register returns the current value of the internal free running 32 bit counter indicating the time when the second of three edges occurred. ***NOTE:*** *A minimum of three edge values is required to compute both the period and frequency of an incoming pulse train. Only applicable when the first set of GPIO bits [1:0] are configured to operate as a PULSEIO port. The PULSEIN0 signal is measured on pin 38 of the dedicated 40 pin digital I/O connector.*	Base+0x232	Base+0x8C8
Bit Position	**Name**	**Description**	**Direction**	**Initial Value**
31:0		Current value of the internal free running 32 bit counter indicating the time when the second of three edges occurred.	R	0

Register Name		Description	DSP Address-DWord Boundary (HEX)	DSP Address-Byte Boundary (HEX)
PULSEIN0_CSR0		First of four registers that are simultaneously latched and which contain three edge values along with a position indicator. This register returns the current value of the internal free running 32 bit counter indicating the time when the first of three edges occurred. ***NOTE:*** *A minimum of three edge values is required to compute both the period and frequency of an incoming pulse train. Only applicable when the first set of GPIO bits [1:0] are configured to operate as a PULSEIO port. The PULSEIN0 signal is measured on pin 38 of the dedicated 40 pin digital I/O connector.*	Base+0x231	Base+0x8C4
Bit Position	**Name**	**Description**	**Direction**	**Initial Value**
31:0		Current value of the internal free running 32 bit counter indicating the time when the first of three edges occurred.	R	0

3.22 PULSEIN1_CSR[3:0]

These registers for the second Pulse Input 1 frequency measurement device operate identically as those for the first Pulse Input 0 device.

3.23 PWMOUT0_[LOCOUNT:HICOUNT]

Register Name		Description	DSP Address-DWord Boundary (HEX)	DSP Address-Byte Boundary (HEX)
PWMOUT0_LOCOUNT		First of two registers that contain the number of periods at which the output pulse is to remain at a logical LO level. The period is based on the internal free running 32 bit counter driven by a 37.5Mhz reference clock. ***NOTE:*** *Only applicable when the first set of GPIO bits [1:0] are configured to operate as a PULSEIO port. The PWMOUT0 signal is present on pin 37 of the dedicated 40 pin digital I/O connector.*	Base+0x235	Base+0x8D4
Bit Position	**Name**	**Description**	**Direction**	**Initial Value**
31:0		Number of periods for a LO level assertion on the PWM Output 0 line.	R/W	0

Register Name		Description	DSP Address-DWord Boundary (HEX)	DSP Address-Byte Boundary (HEX)
PWMOUT0_HICOUNT		Second of two registers that contain the number of periods at which the output pulse is to remain at a logical HI level. The period is based on the internal free running 32 bit counter driven by a 37.5Mhz reference clock. ***NOTE:*** *Only applicable when the first set of GPIO bits [1:0] are configured to operate as a PULSEIO port. The PWMOUT0 signal is present on pin 37 of the dedicated 40 pin digital I/O connector.*	Base+0x236	Base+0x8D8
Bit Position	**Name**	**Description**	**Direction**	**Initial Value**
31:0		Number of periods for a HI level assertion on the PWM Output 0 line.	R/W	0

3.24 PWMOUT1_[LOCOUNT:HICOUNT]

These registers for the second PWM Output 1 generation device operate identically as those for the first PWM Output 0 device.

3.25 QE_CSR

Register Name		Description	DSP Address-DWord Boundary (HEX)	DSP Address-Byte Boundary (HEX)
QE_CSR		Quadrature Encoder Control/Status register. The sample clock is based on the internal free running 32 bit counter driven by a 37.5Mhz reference clock. ***NOTE:*** *Only applicable when the first set of GPIO bits [1:0] are configured to operate as a Quadrature Encoder port. The QE0_A leading clock signal is read from pin 37 while the QE0_B trailing clock signal is read from pin 38 of the dedicated 40 pin digital I/O connector.*	Base+0x250	Base+0x940
Bit Position	**Name**	**Description**	**Direction**	**Initial Value**
31:25	N/A	N/A	N/A	0
24:23	QE1_INDEX_MODE	Selects the mode of operation for the QE1 index line. The QE Index line is used as a reference to indicate that a complete rotation of the code wheel has taken place. 0x (0x0 or 0x1) = No Index (default). 10 (0x2) = Rising or Positive Edge. 11 (0x3) = Falling or Negative Edge.	R/W	0
22:20	QE1_CNT_MODE	Selects the mode in which the QE1 will operate. 000 (0x0) = x1 pulses (default). 001 (0x1) = x2 pulses. 010 (0x2) = x4 pulses. ***NOTE:*** *The 'QE1_A' line operates as the phase leader while the 'QE_B' line operates as the phase lag.* 011 (0x3) = N/A 100 (0x4) = UpClock/DownClock at x1 pulses. ***NOTE:*** *The 'QE1_A' line operates as the 'up' or CW clock input, while the 'QE1_B' line operates as the 'down' or CCW clock input to one of the selected Event Counters.* 101 (0x5) = Direction/Clock at x1 pulses. ***NOTE:*** *The 'QE1_A' line operates as a level sensitive direction indicator to one of the selected Event Counters, while the 'QE1_B' line operates as the clock input. Therefore, after a clock pulse is sensed from the 'QE1_B' line, the Event Counter will count in the 'up' or CW direction when the 'QE1_A' line is read as a '1', and count 'down' or CCW when the 'QE1_A' line is read as a '0'.* 110 (0x6) = N/A. 111 (0x7) = N/A.	R/W	0

19:16	QE1_WAIT_PERIOD[3:0]	Selects the number of clock periods that the sampled value must remain stable in order to be considered valid. The sample clock period is based on the internal free running 32 bit counter driven by a 37.5Mhz reference clock. In essence, the wait period may be viewed as a form of digital average or filter, with a range of '0' to '15' periods.	R/W	
15:9	N/A	N/A	N/A	0
7:8	QE0_INDEX_MODE	Selects the mode of operation for the QE0 index line. The QE Index line is used as a reference to indicate that a complete rotation of the code wheel has taken place. 0x (0x0 or 0x1) = No Index (default). 10 (0x2) = Rising or Positive Edge. 11 (0x3) = Falling or Negative Edge.	R/W	0
6:4	QE0_CNT_MODE	Selects the mode in which the QE0 will operate. 000 (0x0) = x1 pulses (default). 001 (0x1) = x2 pulses. 010 (0x2) = x4 pulses. ***NOTE:*** *The 'QE0_A' line operates as the phase leader while the 'QE0_B' line operates as the phase lag.* 011 (0x3) = N/A 100 (0x4) = UpClock/DownClock at x1 pulses. ***NOTE:*** *The 'QE0_A' line operates as the 'up' or CW clock input, while the 'QE0_B' line operates as the 'down' or CCW clock input to one of the selected Event Counters.* 101 (0x5) = Direction/Clock at x1 pulses. ***NOTE:*** *The 'QE0_A' line operates as a level sensitive direction indicator to one of the selected Event Counters, while the 'QE0_B' line operates as the clock input. Therefore, after a clock pulse is sensed from the 'QE0_B' line, the Event Counter will count in the 'up' or CW direction when the 'QE0_A' line is read as a '1', and count 'down' or CCW when the 'QE0_A' line is read as a '0'.* 110 (0x6) = N/A. 111 (0x7) = N/A.	R/W	0
3:0	QE0_WAIT_PERIOD[0:3]	Selects the number of clock periods that the sampled value must remain stable in order to be considered valid. The sample clock period is based on the internal free running 32 bit counter driven by a 37.5Mhz reference clock. In essence, the wait period may be viewed as a form of digital average or filter, with a range of '0' to '15' periods.	R/W	0

4.0 Clock Sources

A myriad of clock sources may be used for timing management. Three different device types are described:
1) traditional 'divide by n' ***event counters***,
2) direct digital synthesizers or ***DDS***, of which there are internal and optional external circuits available, and
3) an ***external clock source*** routed through the SAMPLE_CLK_IO signal on pin 100 of the analog I/O connector.

Additionally, a pair of data sampling schemes may be invoked which allow you to separately define either the 'channel rate' or the additive or 'scan rate':

1) ***Multiplexing***. For time slice or multiplexed sampling, the ADC sample clock rate is the additive sample rate of all inputs, alternatively known as the 'scan rate'. The scan rate is defined as the product of the 'channel rate' times the 'number of channels'.

For example, if the Additive Sample Clock rate is set to 80khz, and there are a total of 8 channels per MUX-PGA-ADC section defined in the scan list, the each individual channel will be sampling at 10khz.

2) ***Pseudo simultaneous***. For simulated simultaneous sampling, the sample clock is set to the desired rate common to all channels or 'channel rate'. However, the ADC inputs are sampled at a separate bursted rate, fixed at their maximum of either 100khz or 250khz. The 'channel rate' triggers a single burst at the 'scan rate', thus yielding minimal phase skew between adjacent channels in the scan table list. The lower the 'channel rate' , the lower the phase skew.

Note: *The maximum additive sample clock value is 100khz for the SI-MOD66xx-100 boards using Burr Brown's ADS8320/ADS8325 ADC, or 250khz for the SI-MOD66xx-250 boards using Linear Technology's LTC1864. The scan list is limited to a maximum of 16 channels per MUX-PGA-ADC section. Please refer to the Scan List/Input Parameters section for further details.*

4.1 Event Counters

The four onboard event counters are implemented as classical 'divide by N' 16 bit counters. The counter simply increments by integer values on every reference clock transition until a desired, 16 bit preset 'Count' value is reached, at which time a pulse will occur marking the desired period. The actual value that is generated by the counter is based on the following formula:

Desired ECn output frequency = RefClk/(Count + 1)

The actual value to be downloaded to the counter register is:

ECn_CNT_LIMIT = {(RefClk) / (Desired EC output frequency)} - 1

4.2 Internal DDS[0:1]

Another set of clock generation circuits are the internal Direct Digital Synthesizers or DDS0 and DDS1, which are capable of programmable sampling rates with precision up to ±1hz resolution. The DDS reference clock may be selected from various sources using a flexible routing matrix, including the carrier DSP's reference clock listed below:

1. SI-C33DSP based cards. For C33 based DSP cards, the 16 bit counter's reference clock uses half of the C33's Hx clock (one quarter of the DSP's internal clock frequency), which is fixed at 37.5Mhz.
2. SI-C671xDSP based cards. For C671x based DSP cards, reference clock uses half of the C671x's EMIF clock, which is fixed at 37.5Mhz.

The actual value that is generated by the DDS is determined by the following formula:

DDS Output Rate = (RefClk * PA) / (Ratio * 2exp27).

The actual value to be downloaded to the DDS phase accumulator (PA) register is:

PA = (Additive Sample Clock * Ratio * 2exp27) / (RefClk)

where

DDS Output Rate: Desired sample frequency generated by the DDS's output.
RefClk: Reference clock, sourced from the routing matrix but usually a high speed 37.5Mhz clock derived from the carrier DSP's clock.
PA: 27 bit phase accumulator value loaded to the DDS.
2exp27: A constant reflecting the maximum possible phase accumulator value, whose resolution is 27 bits.
Ratio: A constant equal to '1', only added into the formula for consistency with the optional external DDS circuit based on the AD9850 described below.

Register	DSP Address-Dword Boundary (HEX)	DSP Address-Byte Boundary (HEX)	Width (Bits)	Direction	Initial Value
INT_DDS0_PADATA	Base+0x210	Base+0x840	27	R/W	0x0
INT_DDS1_PADATA	Base+0x211	Base+0x844	27	R/W	0x0

1) The DDS[0:1] devices have a 27 bit phase accumulator occupying the right most (least significant) bits of the entire register. Consequently, it may be accessed and its output generation updated in a single cycle write.

4.3 External Sample Clock Source

The sample clock signal may also be supplied by an external TTL/CMOS level source, routed through the SAMPLE_CLK_IO line that resides on pin 100 of the 100 pin DSub connector.

The SAMPLE_CLK_IO line is bi-directional, making it ideal to accommodate a variety of sampling schemes. When the sample clock is selected to be sourced, it is automatically configured as an output. Alternatively, when selected to be sourced externally, it is automatically configured as an input.

5.0 Digital I/O Registers

Thirty six (36) general purpose TTL/CMOS signal level digital I/O lines are available, divided into two groups: 1) thirty two (32) lines accessible as a pair of bi-directional 16 bit wide ports, and 2) four (4) which can also double as a pair of Quadrature Encoder inputs, or as a set of Pulse I/O lines.

These lines are in addition to any of the digital I/O lines native to the DSP carrier card, such as its own serial ports and timers. Please refer to TI's reference manuals for further details.

5.1 Digital I/O 32 Bit Wide Port

The thirty two (32) bi-directional, CMOS/TTL signal level lines are labeled as DIOx on the 40 pin IDC connector, and are mapped directly on the DSP's expansion bus. This port may be divided into a pair of separate 16 bit ports.

5.2 Auxiliary Digital I/O Pins

The four (4) bi-directional, CMOS/TTL signal level lines are labeled as GPIOx on the 40 pin IDC connector, and are mapped directly on the DSP's expansion bus.

These lines function as general purpose digital IO lines, or can be configured as a pair of Quadrature Encoder inputs, or as a set of four (4) individual PWM I/Os lines.

6.0 ADC Registers

The each MUX-PGA-ADC group performs sampling in a time division multiplexed fashion, with the period between each of its samples determined by the additive sample clock. There can be up to four (4) separate MUX-PGA-ADC groups on a single board, giving way to simultaneous sampling on each ADC's input.

The ADC results are stored in memory as a 2's complement 16 bit signed integer, with an interrupt (X_INT0) signaling the DSP that an entire frame or scan of channels has been completed. ADC values are automatically adjusted for gain and offset errors if the entire table of errors inside of the I2C EEPROM have been transferred to the FPGA's CalTable.

Each input has a unique memory location that is mapped directly onto the DSP's primary bus, with the channel number serving as this memory's address offset. In other words, the channel number designation for each MUX-PGA-ADC group always starts with a fixed number, irrespective of the quantity of channels selected for multiplexing or the selected termination style. For example, 'Channel 16' will always refer to the first channel of the second MUX-PGA-ADC group, irrespective of the quantity of channels multiplexed per ADC or its input termination (single or differential ended).

Register	DSP Address-DWord Boundary (HEX)	DSP Address-Byte Boundary (HEX)	Depth x Width (Bits)	Direction	Initial Condition
ADC0 (Inputs 0 thru 15)	Base+0x0 thru Base+0xF	Base+0x0 thru Base+0x3C	16 x 16	R	0
ADC1 (Inputs 16 thru 31)	Base+0x010 thru Base+0x01F	Base+0x040 thru Base+0x07C	16 x 16	R	0
ADC2 (Inputs 32 thru 47)	Base+0x020 thru Base+0x02F	Base+0x080 thru Base+0x0BC	16 x 16	R	0
ADC3 (Inputs 48 thru 63)	Base+0x030 thru Base+0x03F	Base+0x0C0 thru Base+0x0FC	16 x 16	R	0

6.1 ADC Data Format

Register Name		Description	DSP Address-DWord Boundary (HEX)	DSP Address-Byte Boundary (HEX)
ADC[63:0]		ADC Readings.	Base+0x0 thru Base+0x3F	Base+0x0 thru Base+0xFC
Bit Position	**Name**	**Description**	**Direction**	**Initial Value**
31:16	N/A	N/A	N/A	0
15:0	ADC_DATA	2's compliment	R	0

7.0 DAC Registers

The DACs are updated by direct DSP writes to its expansion bus. Therefore, the only manner in which the DACs may be updated at even intervals is by the DSP servicing interrupts (X_INTn) caused by the completion of a scan of inputs. Please consult the Linear Technology LTC2600 data sheet for further details. DAC values are automatically adjusted for gain and offset errors if the entire table of errors inside of the I2C EEPROM have been transferred to the FPGA's CalTable.

Note: *The maximum update rate is 180khz.*

Register Name		**Description**	**DSP Address-DWord Boundary (HEX)**	**DSP Address-Byte Boundary (HEX)**
DAC[15:0]		DAC registers.	Base+0x100 thru Base+0x10F	Base+0x400 thru Base+0x43C
Bit Position	**Name**	**Description**	**Direction**	**Initial Value**
31:16	N/A	N/A	N/A	0
15:0	DAC_DATA	2's compliment	W	-10 Volts before FPGA loaded, 0 Volts after FPGA loaded.

8.0 Scan Table/Input Parameter Registers

The Scan Table/Input Parameter list is stored in SRAM that is mapped directly on the DSP's primary bus. A group of channels to be converted is to be defined by setting up a list of channels, along with each channel's signal characteristics before the initiation of a conversion cycle. The list is typically started with the lowest channel number of interest per MUX-PGA-ADC section, all the way to the very last channel of interest. This last channel also has a marker or a SYNC bit that is used to indicate the end of the list, after which the scan table is restarted. Once the entire scan or frame of channels is completed, an X_INT0 is generated to the DSP. At this time, the DSP can simply read from memory the ADC data from one or more of the channels.

Register Name		**Description**	**DSP Address-DWord Boundary (HEX)**	**DSP Address-Byte Boundary (HEX)**
Scan Table/Input Parameters		Scan table that contains the ADC channel information in the sequence they are to be sampled.	Base+0x300 thru Base+0x30F	Base+0xC00 thru Base+0xC3C
Bit Position	**Name**	**Description**	**Direction**	**Initial Value**
31:0	SCAN_DATA	Registers that contain channel number and gain settings.	R/W	0

Remember from the DDS section that

Additive Sample Clock = (Number of Channels in the Scan List) x (Sample Rate per Channel).

Note:

1) *The maximum additive sample clock value is 100khz for the SI-MOD66xx-100 boards using Burr Brown's ADS8320 ADC, or 250khz for the SI-MOD66xx-250 boards using Linear Technology's LTC1864. The scan list is limited to a maximum of 16 channels per MUX-PGA-ADC section. Please refer to the Scan List/Input Parameters section for further details.*
2) *The San Table must be updated before a transfer of the entire table of gain and offset errors from the I2C EEPROM to the FPGA's CalTable is to take place, since the Scan Table contents are used as the I2C EEPROM address bits during the transfer.*

The scan list has only 16 locations, with each location defining the channel number of interest, along with its corresponding input termination and gain. The actual ordering of the channel numbers is irrelevant, and each channel's input termination can be individually configured for single ended or differential ended operation. In this manner, channels are not thrown away only to keep even channel boundaries on the input muxes. Please consult the Siliconix/Harris DG407 data sheet for further details on the naming convention used for the analog inputs on the 100 pin D-sub connector.

8.1 Scan Table Data Format

Register Name		Description	DSP Address-DWord Boundary (HEX)	DSP Address-Byte Boundary (HEX)
Scan Table/Input Parameters		Scan table that contains the ADC channel information in the sequence they are to be sampled.	Base+0x300 thru Base+0x30F	Base+0xC00 thru Base+0xC3C
Bit Position	**Name**	**Description**	**Direction**	**Initial Value**
31:30	PGA_HIGAIN3[1:0]	Gain bits for MUX-PGA-ADC Group 3's optional High Gain Amplifier. 00 (0x0) = x1 (default). 01 (0x1) = x10. 10 (0x2) = x100. 11 (0x3) = N/A.	R/W	0
29:28	PGA_HIGAIN2[1:0]	Gain bits for MUX-PGA-ADC Group 2's optional High Gain Amplifier. 00 (0x0) = x1 (default). 01 (0x1) = x10. 10 (0x2) = x100. 11 (0x3) = N/A.	R/W	0
27:26	PGA_HIGAIN1[1:0]	Gain bits for MUX-PGA-ADC Group 1's optional High Gain Amplifier. 00 (0x0) = x1 (default). 01 (0x1) = x10. 10 (0x2) = x100. 11 (0x3) = N/A.	R/W	0
25:24	PGA_HIGAIN0[1:0]	Gain bits for MUX-PGA-ADC Group 0's optional High Gain Amplifier. 00 (0x0) = x1 (default). 01 (0x1) = x10. 10 (0x2) = x100. 11 (0x3) = N/A.	R/W	0
23:22	PGA_LOGAIN3[1:0]	Gain bits for MUX-PGA-ADC Group 3's Low Gain Differential Amplifier. 00 (0x0) = x1 (default). 01 (0x1) = x2. 10 (0x2) = x5. 11 (0x3) = x10.	R/W	0
21:20	PGA_LOGAIN2[1:0]	Gain bits for MUX-PGA-ADC Group 2's Low Gain Differential Amplifier. 00 (0x0) = x1 (default). 01 (0x1) = x2. 10 (0x2) = x5. 11 (0x3) = x10.	R/W	0
19:18	PGA_LOGAIN1[1:0]	Gain bits for MUX-PGA-ADC Group 1's Low	R/W	0

		Gain Differential Amplifier. 00 (0x0) = x1 (default). 01 (0x1) = x2. 10 (0x2) = x5. 11 (0x3) = x10.		
17:16	PGA_LOGAIN0[1:0]	Gain bits for MUX-PGA-ADC Group 0's Low Gain Differential Amplifier. 00 (0x0) = x1 (default). 01 (0x1) = x2. 10 (0x2) = x5. 11 (0x3) = x10.	R/W	0
15:14	SECOND_MUX3[1:0]	Mux B, or Secondary Multiplexer channel selection bits for MUX-PGA-ADC Group 3's DG409. The DG409 is a dual 4:1 analog mux, and serves to route analog inputs for either single ended or differential operation. 00 (0x0) = InA Single Ended (default). 01 (0x1) = InA-InB Differential Ended. 10 (0x2) = InB Single Ended (default). 11 (0x3) = Ground/Common Mode.	R/W	0
13:12	SECOND_MUX2[1:0]	Mux B, or Secondary Multiplexer channel selection bits for MUX-PGA-ADC Group 2's DG409. The DG409 is a dual 4:1 analog mux, and serves to route analog inputs for either single ended or differential operation. 00 (0x0) = InA Single Ended (default). 01 (0x1) = InA-InB Differential Ended. 10 (0x2) = InB Single Ended (default). 11 (0x3) = Ground/Common Mode.	R/W	0
11:10	SECOND_MUX1[1:0]	Mux B, or Secondary Multiplexer channel selection bits for MUX-PGA-ADC Group 1's DG409. The DG409 is a dual 4:1 analog mux, and serves to route analog inputs for either single ended or differential operation. 00 (0x0) = InA Single Ended (default). 01 (0x1) = InA-InB Differential Ended. 10 (0x2) = InB Single Ended (default). 11 (0x3) = Ground/Common Mode.	R/W	0
9:8	SECOND_MUX0[1:0]	Mux B, or Secondary Multiplexer channel selection bits for MUX-PGA-ADC Group 0's DG409. The DG409 is a dual 4:1 analog mux, and serves to route analog inputs for either single ended or differential operation. 00 (0x0) = InA Single Ended (default). 01 (0x1) = InA-InB Differential Ended. 10 (0x2) = InB Single Ended (default). 11 (0x3) = Ground/Common Mode.	R/W	0
7:4	N/A	N/A	N/A	0

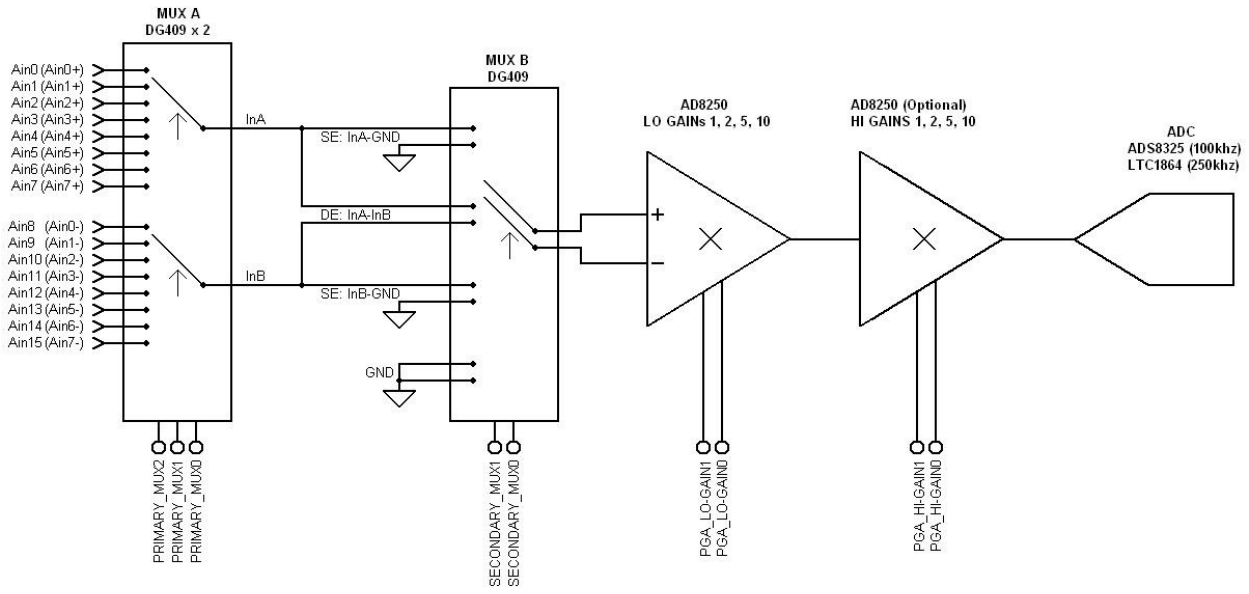
3	SYNC	Synchronization bit that serves to mark the end of the scan list or frame of channels. 0 = Not end of scan list. Continues to the next location in the scan table. 1 = End of scan list. Forces synchronization by starting at the first location in the scan table. ***NOTE:*** *When a scan table has been completed as marked by the assertion of the SYNC bit, an X_INT0 is generated to the DSP indicating that all ADC values pertaining to the last scan/frame are valid.*	R/W	0
2:0	PRIMARY_MUX[2:0]	Mux A or Primary Multiplexer channel selection bits for all of the MUX-PGA-ADC Group's DG407s. The DG407 is a dual 8:1 analog mux, and serves to simultaneously route analog input pairs denoted as 'InA' and InB'. 000 (0x0) = Enable inputs IN0 (IN0A) and IN8 (IN0B). 001 (0x1) = Enable inputs IN1 (IN1A) and IN9 (IN1B). 010 (0x2) = Enable inputs IN2 (IN2A) and IN10 (IN2B). 011 (0x3) = Enable inputs IN3 (IN3A) and IN11 (IN3B). 100 (0x4) = Enable inputs IN4 (IN4A) and IN12 (IN4B). 101 (0x5) = Enable inputs IN5 (IN5A) and IN13 (IN5B). 110 (0x6) = Enable inputs IN6 (IN6A) and IN14 (IN6B). 111 (0x7) = Enable inputs IN7 (IN7A) and IN15 (IN7B).	R/W	0

8.2 Two Stage Gain Amplifiers

Bits 31:16 determine the overall gain by multiplying the gain value of the first stage by the gain value of the optional second stage. The first stage amplifier is a differential low gain device, while the second stage is an optional single ended high gain device.

PGA_LOGAIN[3..0]1	PGA_LOGAIN[3..0]0	PGA207 Differential Amplifier Gains for all MUX-PGA-ADC groups
0	0	1
0	1	2
1	0	5
1	1	10

PGA_HIGAIN[3..0]1	PGA_HIGAIN[3..0]0	PGA103 Amplifier Gains for all MUX-PGA-ADC groups
0	0	1
0	1	10
1	0	100
1	1	N/A



ADC Group Block Diagram

9.0 SI-MOD66xx Configuration Example

All addresses refer to an offset that is added to a DSP's base address, which differ depending on the address boundary scheme used by a particular DSP:

a) SI-C3xDSP base address mapping: 0xFE0000, boundary factor = 1.

b) SI-C67xDSP base address mapping: 0x80380000, boundary factor = 4.

For example, the FPGA_VERSION is mapped as follows:

a) An SI-MOD66xx fitted onto an SI-C3xDSP carrier, the FPGA_VERSION register's address is mapped at 0xFE0,000+0x200 = 0xFE0,200.

b) An SI-MOD66xx fitted onto an SI-C67xDSP carrier, the FPGA_VERSION register's address is mapped at 0x8038,0000+0x800 = 0x8038,0800.

There are several different sequences that are possible to configure the SI-MOD66xx module. However, in order to ensure proper and predictable operation please follow the general steps as outlined in the simple examples below:

9.1 ADC Section

For simplicity, configure the ADC Scan Table such that all channels are identically configured:

a) Number of Channels per Mux = 16, same for all four ADC groups for a total of 64 channels. Required to enable the SYNC bit (SCAN_TABLE bit 3).

b) Input Type on first 8 channels (A group) = A Single Ended, Input Type on second 8 channels (B group) = B Single Ended

c) 1st Gain = 1.

d) 2nd Gain = 1.

Resultant array for the ADC Scan Table to be written at 0xC00 to 0xC3F (C3x: 0x300 to 0x30F):

0
1
2
3
4
5
6
7
AA
AA01
AA02
AA03
AA04
AA05
AA06
AA0F (AA07+8:SYNC Bit=AA0F)

Note: *The San Table must be updated before a transfer of the entire table of gain and offset errors from the I2C EEPROM to the FPGA's CalTable is to take place, since the Scan Table contents are used as the I2C EEPROM address bits during the transfer.*

9.2 Timing Section

Configure timing sources which include onboard Direct Digital Synthesizers (DDS) and Event Counters (EC), as well as external sources.
Sample Rate Values to be used:

a) Sample Rate/Chan (DDS0) = 5000hz, with resultant DDS0 rate 5KHzx16channels = 80khz.

b) Sample Rate/Chan (DDS1) = 1000hz, with resultant DDS0 rate 1KHzx16channels = 16khz.

c) Sample Rate/Chan (Ext_DDS) = 5000hz, with resultant Ext_DDS rate 5KHz x 16channels = 80khz.

Sample Rate Management:

a) External Clock Enable = Input (External Source).
b) Sample Mode = Muxed.
c) DDS0 Trigger Mode = S/W (Free Run).
d) DDS1 Trigger Mode = S/W (Free Run).
e) Sample Clock Source = Internal DDS0.

EC[3:0] Parameters, for simplicity all ECs will be identically configured:

a) EC[3:0] Reset = Free Run.
b) EC[3:0] Enable = Enable.
c) EC[3:0] Wrap Mode = Wrap/Free Run.
d) EC[3:0] Polarity = +Positive.
e) EC[3:0] Tick Clock Source = DSP Ref Clk.
f) EC[3:0] Threshold = 1.

Resultant values to be written:

a) Write Control/Phase info to first internal DDS0, INT_DDS0_PADATA at 0x840 (C3x: 0x210):
0x000045E8.

b) Write Control/Phase info to second internal DDS1, INT_DDS1_PADATA at 0x844 (C3x: 0x211):
0x00000DBF.

c) Optional for SI-MOD68 only - Configure External DDS (Analog Devices' ADS9850):

c1) Clear external DDS by toggling the lsb of the TIMING_CSR:

c1.1) Write a '0x1' to TIMING_CSR at 0x804 (C3x: 0x201) to clear DDS.

c1.2) Write a '0x0' to TIMING_CSR at 0x804 (C3x: 0x201) to remove DDS clear.

c.2) Write Control and Phase info to external DDS, via EXT_DDS_PADATA, in two steps:

c2.1) Write a single '0x0' (Zero) to DDS control byte, EXT_DDS_PADATA at 0x860 (C3x: 0x218):
0x00

c2.2) Write four bytes of phase data, EXT_DDS_PADATA at 0x860 (C3x: 0x218):
0x00
0x11
0x79
0xED

c.3) Start external DDS by toggling EXT_DDS_LOAD:

c3.1) Write any value to 0x864 (C3x: 0x219).

d) Write desired thresholds or count limits for all four ECs, with each value written individually or as a four deep array:

d.1) Write limit for first EC0, EC0_CNT_LIMIT at 0x818 (C3x: 0x206).

d.2) Write limit for second EC1, EC1_CNT_LIMIT at 0x81C (C3x: 0x207).

d.3) Write limit for third EC2, EC2_CNT_LIMIT at 0x820 (C3x: 0x208).

d.4) Write limit for fourth EC3, EC3_CNT_LIMIT at 0x824 (C3x: 0x209).
0x00000001
0x00000001
0x00000001
0x00000001

e) Configure overall board Timing and four ECs:

e.1) Clear each of the four ECs, with each value written individually or as a four deep array:

e1.1) Clear first EC0, write a '0x1' to EC0_CSR at 0x808 (C3x: 0x202).

e1.2) Clear second EC1, write a '0x1' to EC1_CSR at 0x80C (C3x: 0x203).

e1.3) Clear third EC2, write a '0x1' to EC2_CSR at 0x810 (C3x: 0x204).

e1.4) Clear fourth EC3, write a '0x1' to EC3_CSR at 0x814 (C3x: 0x205).

e.2) Write configuration and control value for overall board Timing, TIMING_CSR at 0x804 (C3x: 0x201):
0x00000000

e.3) Write configuration and control values for all four ECs, with each value written individually or as a four deep array:

e3.1) Write config/control for first EC0, EC0_CSR at 0x818 (C3x: 0x206).

e3.2) Write config/control for second EC1, EC1_CSR at 0x80C (C3x: 0x203).

e3.3) Write config/control for third EC2, EC2_CSR at 0x810 (C3x: 0x204).

e3.4) Write config/control for fourth EC3, EC3_CSR at 0x814 (C3x: 0x205).
0x00000B00
0x00000B00
0x00000B00
0x00000B00

9.3 DAC Section

Configures the operation of the analog outputs.

NOTE: this is a reserved address, not yet implemented. Any access is ignored. 0x00000000.

9.4 Digital I/O (DIO) Port Section

Configures the operation of the pair of dedicated 16 bit ports with the following configuration: Digital I/O Port Direction = LW[15:0]: Input, HW[31:16]: Input.

Resultant values to be written:

a) Write desired control value for the pair of DIO ports, DIO_CSR at 0x890 (C3x: 0x224):
0x00000000

9.5 General Purpose Digital I/O (GPIO) Section

This section configures the four GPIO lines as one of three functions: a) Auxiliary I/O, b) Pulse I/O, and c) Quadrature Encoders. Each configuration should be treated separate devices.

9.5.1 Example with Auxiliary I/O

GPI/O Configuration to be used:

a) GPI/O[1:0] Function = Aux DIO[1:0].
b) GPI/O[3:2] Function = Aux DIO[3:2].
c) Free Counter Source = Internal Counter.
d) Aux DI/O Port Direction = Input.

Resultant values to be written:

a) Auxiliary Digital I/O Configuration:

a1) Write desired configuration value to determine the direction of the four pin Auxiliary DIO port, AUX_DIO_CSR at 0x8A0 (C3x: 0x228):
0x00000000

b) Pulse I/O Configuration:

b.1) Clear all four pulse I/Os, write a '0xF' to PULSEIO_CSR at 0x8C0 (C3x: 0x230).

b.2) Write values to determine desired frequency of the pair of output pulse lines:

b.2.1) Write value for first output pulse high period on PWMOUT0, PWMOUT0_HICOUNT at 0x8D4 (C3x: 0x235).

b.2.2) Write value for first output pulse low period on PWMOUT0, PWMOUT0_LOCOUNT at 0x8D8 (C3x: 0x236).

b.2.3) Write value for first output pulse high period on PWMOUT1, PWMOUT1_HICOUNT at 0x8EC (C3x: 0x23B).

b.2.4) Write value for first output pulse low period on PWMOUT1, PWMOUT1_LOCOUNT at 0x8F0 (C3x: 0x23C).
0x00000000
0x00000000
0x00000000
0x00000000

b.3) Start all four pulse I/Os by removing reset, write a '0x0' to PULSEIO_CSR at 0x8C0 (C3x: 0x230).

c) Quadrature Encoders Configuration:

c.1) Write desired configuration value to determine operating mode of the Quadrature Encoders, QE_CSR at 0x940 (C3x: 0x250):

NOTE: QEs work in conjunction with the ECs whose outputs reflect the QE positions. Please refer to demo applications for more insight.
0x00000000

d) Configure GPIO as either Aux I/O by writing appropriate value to the GPIO_CSR at 0x8B0 (C3x: 0x22C):
0x00000000

9.5.2 Example with Pulse I/O

GPI/O Configuration to be used:
a) GPI/O[1:0] Function = Pulse IO[0].
b) GPI/O[3:2] Function = Pulse IO[1].
c) Free Counter Source = Internal Counter.

Pulse I/O Parameters to be used:
a) Pulse_IN0 Reset = Free Run.
b) Pulse_OUT0 Reset = Free Run.
c) Pulse_OUT0 High Tick Count[31:0] = 100 ticks.
d) Pulse_OUT0 Low Tick Count[31:0] = 1000 ticks.

e) Pulse_IN1 Reset = Free Run.
f) Pulse_OUT1 Reset = Free Run.
g) Pulse_OUT1 High Tick Count[31:0] = 500 ticks.
h) Pulse_OUT1 Low Tick Count[31:0] = 5000 ticks.

Resultant values to be written:
a) Auxiliary Digital I/O Configuration:
a.1) Write desired configuration value to determine the direction of the four pin Auxiliary DIO port, AUX_DIO_CSR at 0x8A0 (C3x: 0x228):
0x00000000

b) Pulse I/O Configuration:
b.1) Clear all four pulse I/Os, write a '0xF' to PULSEIO_CSR at 0x8C0 (C3x: 0x230).
b.2) Write values to determine desired frequency of the pair of output pulse lines:
b.2.1) Write value for first output pulse high period on PWMOUT0, PWMOUT0_HICOUNT at 0x8D4 (C3x: 0x235).
b.2.2) Write value for first output pulse low period on PWMOUT0, PWMOUT0_LOCOUNT at 0x8D8 (C3x: 0x236).
b.2.3) Write value for first output pulse high period on PWMOUT1, PWMOUT1_HICOUNT at 0x8EC (C3x: 0x23B).
b.2.4) Write value for first output pulse low period on PWMOUT1, PWMOUT1_LOCOUNT at 0x8F0 (C3x: 0x23C).
0x00000064
0x000003E8
0x000001F4
0x00001388

b.3) Start all four pulse I/Os by removing reset, write a '0x0' to PULSEIO_CSR at

0x8C0 (C3x: 0x230).

c) Quadrature Encoders Configuration:

c.1) Write desired configuration value to determine operating mode of the Quadrature Encoders, QE_CSR at 0x940 (C3x: 0x250):

Note: QEs work in conjunction with the ECs whose outputs reflect the QE positions. Please refer to demo applications for more insight.

0x00000000

d) Configure GPIO as Pulse I/O by writing appropriate value to the GPIO_CSR at 0x8B0 (C3x: 0x22C):

0x00000005

9.5.3 Example with Quadrature Encoders

GPI/O Configuration to be used:

a) GPI/O[1:0] Function = Quad. Encoder 0.
b) GPI/O[3:2] Function = Quad. Encoder 1.
c) Free Counter Source = Internal Counter.

QE Parameters:

a) QE0 Divide Ratio[3:0] = 0 ticks.
b) QE0 Count Mode = A/B = x1 Clk/Cycle.
c) QE0 Index Mode = No Index.

d) QE1 Divide Ratio[3:0] = 0 ticks.
e) QE1 Count Mode = A/B = x1 Clk/Cycle.
f) QE1 Index Mode = No Index.

Resultant values to be written:

a).- Auxiliary Digital I/O Configuration:

a.1) Write desired configuration value to determine the direction of the four pin Auxiliary DIO port, AUX_DIO_CSR at 0x8A0 (C3x: 0x228):

0x00000000

b) Pulse I/O Configuration:

b.1) Clear all four pulse I/Os, write a '0xF' to PULSEIO_CSR at 0x8C0 (C3x: 0x230).

b.2) Write values to determine desired frequency of the pair of output pulse lines:

b.2.1) Write value for first output pulse high period on PWMOUT0, PWMOUT0_HICOUNT at 0x8D4 (C3x: 0x235).

b.2.2) Write value for first output pulse low period on PWMOUT0, PWMOUT0_LOCOUNT at 0x8D8 (C3x: 0x236).

b.2.3) Write value for first output pulse high period on PWMOUT1, PWMOUT1_HICOUNT at 0x8EC (C3x: 0x23B).

b.2.4) Write value for first output pulse low period on PWMOUT1,

PWMOUT1_LOCOUNT at 0x8F0 (C3x: 0x23C).
0x00000000
0x00000000
0x00000000
0x00000000

b.3) Start all four pulse I/Os by removing reset, write a '0x0' to PULSEIO_CSR at 0x8C0 (C3x: 0x230).

c) Quadrature Encoders Configuration:

c.1) Write desired configuration value to determine operating mode of the Quadrature Encoders, QE_CSR at 0x940 (C3x: 0x250):

Note: QEs work in conjunction with the ECs whose outputs reflect the QE positions. Please refer to demo applications for more insight.
0x00000000

d) Configure GPIO as QEs by writing appropriate value to the GPIO_CSR at 0x8B0 (C3x: 0x22C):
0x0000000A

9.6 Calibration Table Section

This is an optional step on the SI-MOD66 only, since the values transferred from the I2C EEPROM to the FPGA's internal Cal Table do not impact any logic other than to perform the autocalibration function as data is updated between the ADC/DAC circuitry.

In any event, the steps required to transfer gain and offset error values from the nonvolatile I2C EEPROM to internal FPGA Cal Table are as follows.

a) Check to see if the calibration E2PROM device is accessible by polling bit 1 of the I2C_ADDR_CSR at 0x84C (C3x: 0x213); a clear or '0x0' value indicates that the E2PROM is accessible and to proceed to next step of performing the actual transfer.

b) Initiate transfer of E2PROM contents to FPGA's internal calibration table by writing a '0x2' to the I2C_ADDR_CSR at 0x84C (C3x: 0x213).

c) Check to see if the transfer to the FPGA's calibration table has been completed by polling bit 1 of the I2C_ADDR_CSR at 0x84C (C3x: 0x213); a clear value indicates that the transfer is complete.

Note: *The San Table must be updated before a transfer of the entire table of gain and offset errors from the I2C EEPROM to the FPGA's CalTable is to take place, since the Scan Table contents are used as the I2C EEPROM address bits during the transfer.*

The SI-MOD66xx has been completely configured and is ready to go!

10.0 Analog IO Connections

10.1 Analog IO Connection for SI-MOD66xx With 64 Analog Inputs and 16 Analog Outputs: 100 Pin D-sub Connector

For PCI and cPCI form factor SI-DSP carriers cards, an AMP 100 pin Series III, half pitch, 0.050" DSub connector, manufacturer part 787170-9, is used to interface the external analog I/O signals. For SI-MOD66xx modules fitted with a maximum of 64 analog inputs and a maximum of 16 analog outputs, below is the connection diagram:

DB1.1	IN0 / IN0+	DB1.51	IN8 / IN0-
DB1.2	IN1 / IN1+	DB1.52	IN9 / IN1-
DB1.3	IN2 / IN2+	DB1.53	IN10 / IN2-
DB1.4	IN3 / IN3+	DB1.54	IN11 / IN3-
DB1.5	IN4 / IN4+	DB1.55	IN12 / IN4-
DB1.6	IN5 / IN5+	DB1.56	IN13 / IN5-
DB1.7	IN6 / IN6+	DB1.57	IN14 / IN6-
DB1.8	IN7 / IN7+	DB1.58	IN15 / IN7-
DB1.9	**AGND**	DB1.59	**AGND**
DB1.10	IN16 / IN16+	DB1.60	IN24 / IN16-
DB1.11	IN17 / IN17+	DB1.61	IN25 / IN17-
DB1.12	IN18 / IN18+	DB1.62	IN26 / IN18-
DB1.13	IN19 / IN19+	DB1.63	IN27 / IN19-
DB1.14	IN20 / IN20+	DB1.64	IN28 / IN20-
DB1.15	IN21 / IN21+	DB1.65	IN29 / IN21-
DB1.16	IN22 / IN22+	DB1.66	IN30 / IN22-
DB1.17	IN23 / IN23+	DB1.67	IN31 / IN23-
DB1.18	**AGND**	DB1.68	**AGND**
DB1.19	IN32 / IN32+	DB1.69	IN40 / IN32-
DB1.20	IN33 / IN33+	DB1.70	IN41 / IN33-
DB1.21	IN34 / IN34+	DB1.71	IN42 / IN34-
DB1.22	IN35 / IN35+	DB1.72	IN43 / IN35-
DB1.23	IN36 / IN36+	DB1.73	IN44 / IN36-
DB1.24	IN37 / IN37+	DB1.74	IN45 / IN37-
DB1.25	IN38 / IN38+	DB1.75	IN46 / IN38-
DB1.26	IN39 / IN39+	DB1.76	IN47 / IN39-
DB1.27	**AGND**	DB1.77	**AGND**
DB1.28	IN48 / IN48+	DB1.78	IN56 / IN48-
DB1.29	IN49 / IN49+	DB1.79	IN57 / IN49-
DB1.30	IN50 / IN50+	DB1.80	IN58 / IN50-
DB1.31	IN51 / IN51+	DB1.81	IN59 / IN51-
DB1.32	IN52 / IN52+	DB1.82	IN60 / IN52-
DB1.33	IN53 / IN53+	DB1.83	IN61 / IN53-
DB1.34	IN54 / IN54+	DB1.84	IN62 / IN54-
DB1.35	IN55 / IN55+	DB1.85	IN63 / IN55-
DB1.36	**AGND**	DB1.86	**AGND**
DB1.37	DACOUT_0	DB1.87	DACOUT_8
DB1.38	DACOUT_1	DB1.88	DACOUT_9
DB1.39	DACOUT_2	DB1.89	DACOUT_10
DB1.40	DACOUT_3	DB1.90	DACOUT_11
DB1.41	**AGND**	DB1.91	**AGND**
DB1.42	DACOUT_4	DB1.92	DACOUT_12
DB1.43	DACOUT_5	DB1.93	DACOUT_13
DB1.44	DACOUT_6	DB1.94	DACOUT_14
DB1.45	DACOUT_7	DB1.95	DACOUT_15
DB1.46	**AGND**	DB1.96	**AGND**
DB1.47	**DGND**	DB1.97	**DGND**
DB1.48	-	DB1.98	-
DB1.49	-	DB1.99	-
DB1.50	-	DB1.100	SAMPLE_CLK_IO

Note: *The SAMPL_CLK_IO is a 3.3V signal, and NOT 5V tolerant.*

10.2 Analog IO Connection for SI-MOD66xx With 32 Analog Inputs and 32 Analog Outputs: 100 Pin D-sub Connector

For PCI and cPCI form factor SI-DSP carriers cards, an AMP 100 pin Series III, half pitch, 0.050" DSub connector, manufacturer part 787170-9, is used to interface the external analog I/O signals. For SI-MOD66xx modules fitted with a maximum of 32 analog inputs and outputs, below is the connection diagram:

DB1.1	IN0 / IN0+	DB1.51	IN8 / IN0-
DB1.2	IN1 / IN1+	DB1.52	IN9 / IN1-
DB1.3	IN2 / IN2+	DB1.53	IN10 / IN2-
DB1.4	IN3 / IN3+	DB1.54	IN11 / IN3-
DB1.5	IN4 / IN4+	DB1.55	IN12 / IN4-
DB1.6	IN5 / IN5+	DB1.56	IN13 / IN5-
DB1.7	IN6 / IN6+	DB1.57	IN14 / IN6-
DB1.8	IN7 / IN7+	DB1.58	IN15 / IN7-
DB1.9	**AGND**	DB1.59	**AGND**
DB1.10	IN16 / IN16+	DB1.60	IN24 / IN16-
DB1.11	IN17 / IN17+	DB1.61	IN25 / IN17-
DB1.12	IN18 / IN18+	DB1.62	IN26 / IN18-
DB1.13	IN19 / IN19+	DB1.63	IN27 / IN19-
DB1.14	IN20 / IN20+	DB1.64	IN28 / IN20-
DB1.15	IN21 / IN21+	DB1.65	IN29 / IN21-
DB1.16	IN22 / IN22+	DB1.66	IN30 / IN22-
DB1.17	IN23 / IN23+	DB1.67	IN31 / IN23-
DB1.18	**AGND**	DB1.68	**AGND**
DB1.19	-	DB1.69	-
DB1.20	-	DB1.70	-
DB1.21	-	DB1.71	-
DB1.22	-	DB1.72	-
DB1.23	-	DB1.73	-
DB1.24	-	DB1.74	-
DB1.25	-	DB1.75	-
DB1.26	-	DB1.76	-
DB1.27	**AGND**	DB1.77	**AGND**
DB1.28	DACOUT_0	DB1.78	DACOUT_8
DB1.29	DACOUT_1	DB1.79	DACOUT_9
DB1.30	DACOUT_2	DB1.80	DACOUT_10
DB1.31	DACOUT_3	DB1.81	DACOUT_11
DB1.32	**AGND**	DB1.82	**AGND**
DB1.33	DACOUT_4	DB1.83	DACOUT_12
DB1.34	DACOUT_5	DB1.84	DACOUT_13
DB1.35	DACOUT_6	DB1.85	DACOUT_14
DB1.36	DACOUT_7	DB1.86	DACOUT_15
DB1.37	**AGND**	DB1.87	**AGND**
DB1.38	DACOUT_16	DB1.88	DACOUT_24
DB1.39	DACOUT_17	DB1.89	DACOUT_25
DB1.40	DACOUT_18	DB1.90	DACOUT_26
DB1.41	DACOUT_19	DB1.91	DACOUT_27
DB1.42	**AGND**	DB1.92	**AGND**
DB1.43	DACOUT_20	DB1.93	DACOUT_28
DB1.44	DACOUT_21	DB1.94	DACOUT_29
DB1.45	DACOUT_22	DB1.95	DACOUT_30
DB1.46	DACOUT_23	DB1.96	DACOUT_31
DB1.47	**AGND**	DB1.97	**AGND**
DB1.48	-	DB1.98	-
DB1.49	-	DB1.99	**DGND**
DB1.50	-	DB1.100	SAMPLE_CLK_IO

Note: *The SAMPL_CLK_IO is a 3.3V signal, and NOT 5V tolerant.*

10.3 Analog IO Connection: 68 Pin D-sub Connector

For PMC form factor SI-DSP carriers cards, an AMP 68 pin Series III, half pitch, 0.050" DSub connector, manufacturer part 787170-7 (SCSI style), is used to interface the external analog I/O signals. Below is the connection diagram:

DB.34	IN0 / IN0+	DB.68	IN8 / IN0-
DB.33	IN1 / IN1+	DB.67	IN9 / IN1-
DB.32	IN2 / IN2+	DB.66	IN10 / IN2-
DB.31	IN3 / IN3+	DB.65	IN11 / IN3-
DB.30	IN4 / IN4+	DB.64	IN12 / IN4-
DB.29	IN5 / IN5+	DB.63	IN13 / IN5-
DB.28	IN6 / IN6+	DB.62	IN14 / IN6-
DB.27	IN7 / IN7+	DB.61	IN15 / IN7-
DB.26	**AGND**	DB.60	**AGND**
DB.25	IN16 / IN16+	DB.59	IN24 / IN16-
DB.24	IN17 / IN17+	DB.58	IN25 / IN17-
DB.23	IN18 / IN18+	DB.57	IN26 / IN18-
DB.22	IN19 / IN19+	DB.56	IN27 / IN19-
DB.21	IN20 / IN20+	DB.55	IN28 / IN20-
DB.20	IN21 / IN21+	DB.54	IN29 / IN21-
DB.19	IN22 / IN22+	DB.53	IN30 / IN22-
DB.18	IN23 / IN23+	DB.52	IN31 / IN23-
DB.17	**AGND**	DB.51	**AGND**
DB.16	IN32 / IN32+	DB.50	IN40 / IN32-
DB.15	**AGND**	DB.49	**AGND**
DB.14	IN48 / IN48+	DB.48	IN56 / IN48-
DB.13	**AGND**	DB.47	**AGND**
DB.12	DACOUT_0	DB.46	DACOUT_8
DB.11	DACOUT_1	DB.45	DACOUT_9
DB.10	DACOUT_2	DB.44	DACOUT_10
DB.9	DACOUT_3	DB.43	DACOUT_11
DB.8	**AGND**	DB.42	**AGND**
DB.7	DACOUT_4	DB.41	DACOUT_12
DB.6	DACOUT_5	DB.40	DACOUT_13
DB.5	DACOUT_6	DB.39	DACOUT_14
DB.4	DACOUT_7	DB.38	DACOUT_15
DB.3	**AGND**	DB.37	**AGND**
DB.2	**DGND**	DB.36	**DGND**
DB.1	-	DB.35	SAMPLE_CLK_IO

Note: *The SAMPL_CLK_IO is a 3.3V signal, and NOT 5V tolerant.*

10.4 Analog IO Connection for SI-MOD66xx With 64 Analog Inputs and 16 Analog Outputs: 50 Pin IDC Connector Pair

For PC104Plus systems, an additional module fitted with a pair of generic 50 pin IDC, 0.1" pitch plug header connectors are used to interface the external analog I/O signals. For SI-MOD66xx modules fitted with a maximum of 64 analog inputs and a maximum of 16 analog outputs, below is the connection diagram:

First 50 pin Connector

IDC1.1	IN0 / IN0+	IDC1.2	IN1 / IN1+
IDC1.3	IN2 / IN2+	IDC1.4	IN3 / IN3+
IDC1.5	IN4 / IN4+	IDC1.6	IN5 / IN5+
IDC1.7	IN6 / IN6+	IDC1.8	IN7 / IN7+
IDC1.9	**AGND**	IDC1.10	IN16 / IN16+
IDC1.11	IN17 / IN17+	IDC1.12	IN18 / IN18+
IDC1.13	IN19 / IN19+	IDC1.14	IN20 / IN20+
IDC1.15	IN21 / IN21+	IDC1.16	IN22 / IN22+
IDC1.17	IN23 / IN23+	IDC1.18	**AGND**
IDC1.19	IN32 / IN32+	IDC1.20	IN33 / IN33+
IDC1.21	IN34 / IN34+	IDC1.22	IN35 / IN35+
IDC1.23	IN36 / IN36+	IDC1.24	IN37 / IN37+
IDC1.25	IN38 / IN38+	IDC1.26	IN39 / IN39+
IDC1.27	**AGND**	IDC1.28	IN48 / IN48+
IDC1.29	IN49 / IN49+	IDC1.30	IN50 / IN50+
IDC1.31	IN51 / IN51+	IDC1.32	IN52 / IN52+
IDC1.33	IN53 / IN53+	IDC1.34	IN54 / IN54+
IDC1.35	IN55 / IN55+	IDC1.36	**AGND**
IDC1.37	DACOUT_0	IDC1.38	DACOUT_1
IDC1.39	DACOUT_2	IDC1.40	DACOUT_3
IDC1.41	**AGND**	IDC1.42	DACOUT_4
IDC1.43	DACOUT_5	IDC1.44	DACOUT_6
IDC1.45	DACOUT_7	IDC1.46	**AGND**
IDC1.47	**DGND**	IDC1.48	-
IDC1.49	-	IDC1.50	-

Second 50 pin Connector

IDC2.51	IN8 / IN0-	IDC2.52	IN9 / IN1-
IDC2.53	IN10 / IN2-	IDC2.54	IN11 / IN3-
IDC2.55	IN12 / IN4-	IDC2.56	IN13 / IN5-
IDC2.57	IN14 / IN6-	IDC2.58	IN15 / IN7-
IDC2.59	**AGND**	IDC2.60	IN24 / IN16-
IDC2.61	IN25 / IN17-	IDC2.62	IN26 / IN18-
IDC2.63	IN27 / IN19-	IDC2.64	IN28 / IN20-
IDC2.65	IN29 / IN21-	IDC2.66	IN30 / IN22-
IDC2.67	IN31 / IN23-	IDC2.68	**AGND**
IDC2.69	IN40 / IN32-	IDC2.70	IN41 / IN33-
IDC2.71	IN42 / IN34-	IDC2.72	IN43 / IN35-
IDC2.73	IN44 / IN36-	IDC2.74	IN45 / IN37-
IDC2.75	IN46 / IN38-	IDC2.76	IN47 / IN39-
IDC2.77	**AGND**	IDC2.78	IN56 / IN48-
IDC2.79	IN57 / IN49-	IDC2.80	IN58 / IN50-
IDC2.81	IN59 / IN51-	IDC2.82	IN60 / IN52-
IDC2.83	IN61 / IN53-	IDC2.84	IN62 / IN54-
IDC2.85	IN63 / IN55-	IDC2.86	**AGND**
IDC2.87	DACOUT_8	IDC2.88	DACOUT_9
IDC2.89	DACOUT_10	IDC2.90	DACOUT_11
IDC2.91	**AGND**	IDC2.92	DACOUT_12
IDC2.93	DACOUT_13	IDC2.94	DACOUT_14
IDC2.95	DACOUT_15	IDC2.96	**AGND**
IDC2.97	**DGND**	IDC2.98	-
IDC2.99	-	IDC2.100	- SAMPLE_CKIO

Note: *The SAMPL_CLK_IO is a 3.3V signal, and NOT 5V tolerant.*

10.5 Analog IO Connection for SI-MOD66xx With 32 Analog Inputs and 32 Analog Outputs: 50 Pin IDC Connector Pair

For PC104Plus systems, an additional module fitted with a pair of generic 50 pin IDC, 0.1" pitch plug header connectors are used to interface the external analog I/O signals. For SI-MOD66xx modules fitted with a maximum of 32 analog inputs and outputs, below is the connection diagram:

First 50 pin Connector

IDC1.1	IN0 / IN0+	IDC1.2	IN1 / IN1+
IDC1.3	IN2 / IN2+	IDC1.4	IN3 / IN3+
IDC1.5	IN4 / IN4+	IDC1.6	IN5 / IN5+
IDC1.7	IN6 / IN6+	IDC1.8	IN7 / IN7+
IDC1.9	**AGND**	IDC1.10	IN16 / IN16+
IDC1.11	IN17 / IN17+	IDC1.12	IN18 / IN18+
IDC1.13	IN19 / IN19+	IDC1.14	IN20 / IN20+
IDC1.15	IN21 / IN21+	IDC1.16	IN22 / IN22+
IDC1.17	IN23 / IN23+	IDC1.18	**AGND**
IDC1.19	-	IDC1.20	-
IDC1.21	-	IDC1.22	-
IDC1.23	-	IDC1.24	-
IDC1.25	-	IDC1.26	-
IDC1.27	**AGND**	IDC1.28	DACOUT_0
IDC1.29	DACOUT_1	IDC1.30	DACOUT_2
IDC1.31	DACOUT_3	IDC1.32	**AGND**
IDC1.33	DACOUT_4	IDC1.34	DACOUT_5
IDC1.35	DACOUT_6	IDC1.36	DACOUT_7
IDC1.37	**AGND**	IDC1.38	DACOUT_16
IDC1.39	DACOUT_17	IDC1.40	DACOUT_18
IDC1.41	DACOUT_19	IDC1.42	**AGND**
IDC1.43	DACOUT_20	IDC1.44	DACOUT_21
IDC1.45	DACOUT_22	IDC1.46	DACOUT_23
IDC1.47	**AGND**	IDC1.48	-
IDC1.49	-	IDC1.50	-

Second 50 pin Connector

IDC2.51	IN8 / IN0-	IDC2.52	IN9 / IN1-
IDC2.53	IN10 / IN2-	IDC2.54	IN11 / IN3-
IDC2.55	IN12 / IN4-	IDC2.56	IN13 / IN5-
IDC2.57	IN14 / IN6-	IDC2.58	IN15 / IN7-
IDC2.59	**AGND**	IDC2.60	IN24 / IN16-
IDC2.61	IN25 / IN17-	IDC2.62	IN26 / IN18-
IDC2.63	IN27 / IN19-	IDC2.64	IN28 / IN20-
IDC2.65	IN29 / IN21-	IDC2.66	IN30 / IN22-
IDC2.67	IN31 / IN23-	IDC2.68	**AGND**
IDC2.69	-	IDC2.70	-
IDC2.71	-	IDC2.72	-
IDC2.73	-	IDC2.74	-
IDC2.75	-	IDC2.76	-
IDC2.77	**AGND**	IDC2.78	DACOUT_8
IDC2.79	DACOUT_9	IDC2.80	DACOUT_10
IDC2.81	DACOUT_11	IDC2.82	**AGND**
IDC2.83	DACOUT_12	IDC2.84	DACOUT_13
IDC2.85	DACOUT_14	IDC2.86	DACOUT_15
IDC2.87	**AGND**	IDC2.88	DACOUT_24
IDC2.89	DACOUT_25	IDC2.90	DACOUT_26
IDC2.91	DACOUT_27	IDC2.92	**AGND**
IDC2.93	DACOUT_28	IDC2.94	DACOUT_29
IDC2.95	DACOUT_30	IDC2.96	DACOUT_31
IDC2.97	**AGND**	IDC2.98	-
IDC2.99	**DGND**	IDC2.100	- SAMPLE_CKIO

Note: *The SAMPL_CLK_IO is a 3.3V signal, and NOT 5V tolerant.*

11.0 Digital IO Connections

11.1 Digital IO Connection: 40 pin IDC Connector

A generic 40 pin IDC, 0.1" pitch connector is used to interface the external digital I/O signals. Below is the connection diagram:

IDC.1 **DGND**	IDC.2 DIO0
IDC.3 DIO1	IDC.4 DIO2
IDC.5 DIO3	IDC.6 DIO4
IDC.7 DIO5	IDC.8 DIO6
IDC.9 DIO7	IDC.10 DIO8
IDC.11 DIO9	IDC.12 DIO10
IDC.13 DIO11	IDC.14 DIO12
IDC.15 DIO13	IDC.16 DIO14
IDC.17 DIO15	IDC.18 **DGND**
IDC.19 DIO17	IDC.20 DIO16
IDC.21 DIO19	IDC.22 DIO18
IDC.23 DIO21	IDC.24 DIO20
IDC.25 DIO23	IDC.26 DIO22
IDC.27 DIO25	IDC.28 DIO24
IDC.29 DIO27	IDC.30 DIO26
IDC.31 DIO29	IDC.32 DIO28
IDC.33 DIO31	IDC.34 DIO30
IDC.35 DIO_STRB_REQ (QE0_Index)	IDC.36 DIO_STRB_ACK (QE1_Index)
IDC.37 GPIO1 (AUXDIO1/PWMOUT0/QE0_a)	IDC.38 GPIO0 (AUXDIO0/PWMIN0/QE0_b)
IDC.39 GPIO3 (AUXDIO3/PWMOUT1/QE1_a)	IDC.40 GPIO2 (AUXDIO2/PWMIN1/QE1_b)

Notes:

a) *The 32 DIO lines are 3.3V signals that are 5V tolerant.*

b) *The 6 Auxiliary lines DIO_STRB_xx and GPIOs are 3.3V signals, and NOT 5V tolerant.*

11.2 Digital IO Connection: 68 pin D-Sub Connector

If the 40 pin IDC connector on the SI-MOD66xx is not accessible, an optional adapter, namely the SI-40IDCx68D, is available where the digital I/O lines are externally accessible with a 68 pin D-Sub connector.

Below is the connection diagram:

DB.1	**DGND**	DB.35	DIO0
DB.2	DIO1	DB.36	DIO2
DB.3	DIO3	DB.37	DIO4
DB.4	DIO5	DB.38	DIO6
DB.5	DIO7	DB.39	DIO8
DB.6	DIO9	DB.40	DIO10
DB.7	DIO11	DB.41	DIO12
DB.8	DIO13	DB.42	DIO14
DB.9	DIO15	DB.43	**DGND**
DB.10	DIO17	DB.44	DIO16
DB.11	DIO19	DB.45	DIO18
DB.12	DIO21	DB.46	DIO20
DB.13	DIO23	DB.47	DIO22
DB.14	DIO25	DB.48	DIO24
DB.15	DIO27	DB.49	DIO26
DB.16	DIO29	DB.50	DIO28
DB.17	DIO31	DB.51	DIO30
DB.18	DIO_STRB_REQ (QE0_Index)	DB.52	DIO_STRB_ACK (QE1_Index)
DB.19	GPIO1 (AUXDIO1/PWMOUT0/QE0_a)	DB.53	GPIO0 (AUXDIO0/PWMIN0/QE0_b)
DB.20	GPIO3 (AUXDIO3/PWMOUT1/QE1_a)	DB.54	GPIO2 (AUXDIO2/PWMIN1/QE1_b)
DB.21	**+5V** (Optional from PC Supply)	DB.55	**+5Vdc** (Optional from PC Supply)
DB.22	**DGND**	DB.56	**DGND**
DB.23	**DGND**	DB.57	**DGND**
DB.24	**+12Vdc** (Optional from PC Supply)	DB.58	**+12Vdc** (Optional from PC Supply)
DB.25	DSPSPa2-CLKX0 (Optional)	DB.59	DSPSPa5-CLKR0 (Optional)
DB.26	DSPSPa1-DX0 (Optional)	DB.60	DSPSPa4-DR0 (Optional)
DB.27	DSPSPa0-FSX0 (Optional)	DB.61	DSPSPa3-FSR0 (Optional)
DB.28	DSPSPa6-ECKS0 (Optional)	DB.62	**DGND**
DB.29	DSPSPb2-CLKX1 (Optional)	DB.63	DSPSPb5-CLKR1 (Optional)
DB.30	DSPSPb1-DX1 (Optional)	DB.64	DSPSPb4-DR1 (Optional)
DB.31	DSPSPb0-FSX1 (Optional)	DB.65	DSPSPb3-FSR1 (Optional)
DB.32	DSPSPb6-ECKS1 (Optional)	DB.66	**DGND**
DB.33	DSPTIMERa1-TOUT0 (Optional)	DB.67	DSPTIMERa0-TIN0 (Optional)
DB.34	DSPTIMERb1-TOUT1 (Optional)	DB.68	DSPTIMERb0-TIN1 (Optional)

Note: *Only the 32 DIO lines are 3.3V signals that are 5V tolerant. All others are NOT 5V tolerant.*

12.0 Technical Specifications

12.1 DSP Interface

All board functions tied directly to DSP's expansion bus.

12.2 Analog Inputs

- 16S/8D, 32S/16D, or 64S/32D analog inputs, 16:1 MUX part # DG407, 8:2 MUX part # DG409:
  a) SI-MOD6816-100, 16S/8D, 0hz to 100khz additive sampling for all channels.
  b) SI-MOD6832-100, 32S/16D, 0hz to 200khz additive sampling for all channels.
  c) SI-MOD6800-100, 64S/32D, 0hz to 400khz additive sampling for all channels.
  d) SI-MOD6816-250, 16S/8D, 0hz to 250khz additive sampling for all channels.
  e) SI-MOD6832-250, 32S/16D, 0hz to 500khz additive sampling for all channels.
  f) SI-MOD6800-250, 64S/32D, 0hz to 1Mhz additive sampling for all channels.
- ±10Vp maximum input voltage level.
- High input impedance of 1Mohm.
- Two stage amplifiers with gains of 1 to 1,000; first stage with precision differential instrumentation amplifier with gains of 1, 2, 5, 10, part #AD8250 (Analog Devices); second stage with another AD8250 or optional AD8253.
- Each MUX-PGA-ADC group has 0hz to 100khz/250khz muxed time division sampling on 16 channels, for a maximum additive rate of 400khz/1Mhz on all channels, respectively.
- Up to 4 distinct inputs are simultaneously sampled, one from each MUX-PGA-ADC group.
- Successive Approximation ADCs with 16 bits of resolution:
  a) 100khz part #ADS8320 (Burr Brown)
  b) 250khz part #LTC1864 (Linear Technology)
- DC coupling.

12.3 Analog Outputs

- Up to sixteen (16) DACs for analog output channels, Linear Technology part # LTC2620 (12 bit resolution), LTC2610 (14 bit resolution), LTC2600 (16 bit resolution).
- Each output has 0hz to 180khz update rates.
- 12, 14, or 16 bits of resolution.
- ±10Vp bipolar voltage range.
- Fixed 39khz, 2-pole linear phase smoothing filter.

12.4 Digital I/O

- Thirty six (36) lines of general purpose digital lines:
  a) Four (4) lines configurable as an auxiliary digital IO port, or as a pair of Quadrature Encoder inputs, or as a set of PWM I/Os lines (two as inputs and the other two as outputs); 3.3V signaling only.
  b) Group of thirty two (32) lines programmable as inputs or outputs, in groups of 16 bits; 3.3V signaling that are also 5V tolerant.

12.5 General features

- Internal and external hardware triggers and sample clocks, software triggers.
- Fully programmable with QuVIEW, an accelerator library for LabVIEW.
- Fully programmable with QuBASE, an accelerator library for Visual Basic.
- Full suite of development tools from Sheldon Instruments and several third parties.
- Drivers support for Windows & Linux 32/64 bit environments.

12.6 Physical Dimensions & Electrical Requirements

- SI-MOD66xx: Fits all SI-DSP cards, measuring 3.7"(L) x 3.7"(H).
- 0.18lbs or 85 grams.
- Supply Voltages: 1.8V and 3.3V for logic circuitry, 5V for 32 bit port buffers, and +/-12V for analog circuitry.
- 6.75 Watts typical with minimum configuration: +12Vdc@0.25A, -12Vdc@0.2A, 5Vdc@0.1A, 3.3Vdc@0.1A, 1.8Vdc@0.25A.
- 14 Watts typical with minimum configuration: +12Vdc@0.55A, -12Vdc@0.5A, 5Vdc@0.1A, 3.3Vdc@0.1A, 1.8Vdc@0.25A.

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