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SHF Communication Technologies AG

Data Sheet

SHF EA 40 GIG

Error Analyser

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Data Sheet Version 1.2

SHF EA 40 GIG

Error Analyser

PRELIMINARY

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1 Introduction

The SHF EA 40 GIG Error Analyser is a tool for the detection of errors in gigabit transmission systems. Used in conjunction with the SHF BPG 40 A Bit Pattern Generator, a system for bit error rate tests can be formed. Ease of use is ensured by simple hardware functions allowing phase adjustments or input threshold variations of the analyser. It is therefore ideal for research and development of high speed logic MMICs and digital communications systems. Further applications include the testing of high rate PCM and SDH systems as well as digital optical components and sub-nanosecond pulse engineering.

Bit rates of 40 GBit/s can be analysed, with the rate defined by the speed of the clock: the bit rate tested is twice that of the clock. An input for an external clock generator is provided, and an internal low noise crystal oscillator clock is available as an option. The clock is buffered and divided into two channels, one of which contains a frequency divider. A 4:1 40 GBit/s fast demultiplexer circuit reduces the input data rate to four signals, each with a rate of 10GBit/s. The phase shift between the clock and data signals can be adjusted using a computer controlled delay line, offering a delay of up to 160ps, with a resolution of 1 ps.

Four further 1:4 demultiplexers then reduce the data rate down to 2.5 GBit/s and compare the data bit by bit to internally generated PRB sequences. Built in PRBS lengths are 2^{31}–1, 2^{23}–1, 2^{15}–1 or 2^{7}–1. Errors are displayed for each channel as well as the total number of errors. Measurement intervals can be varied within the range 10^{5}…10^{14} Bit/s.

Word synchronisation is achieved automatically, as indicated by four LEDs which light up when synchronisation has been achieved. Shifting of sub-sequences is also tested, and an error is displayed due to incorrect multiplexer signal interleaving, even if a single sub-sequence contains no errors.

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2 Summary of Features

- Handling of CCITT conforming PRBS patterns 2^7–1, 2^{15}–1, 2^{23}–1, 2^{31}–1
- Self-synchronising; broadband operation
- Automatic, GPIB or manual thumbwheel threshold adjustment
- Special "External MUX Error" detection
- Clock outputs at subharmonic rates
- Word frame outputs from each internal 10 GBit/s channel (A, B, C and D)
- External clock input 20GHz for SHF BPG 40 A or BPG 40 GIG compatibility
- Internal computer controlled 20 GHz timing delay line
- Display of total errors inside each internal 10 GBit/s subchannel
- Separate display of Error Quote (Errors/time) / Bit Error Ratio (Errors/Bit)
- Internal 6 digit true frequency counter displaying the bit rate
- Display of MUX Error YES or NO
- Measurement sequence start by TTL signal or push button
- Wide range of selectable gate times
- External GPIB control
- Low noise, low jitter timing circuits
- Burst Mode (fast synchronising) capability

Available Option

- Option 01: Internal clock 20 / 10 / 5 / 2.5 / 1.25 / 0.6 GBit/s

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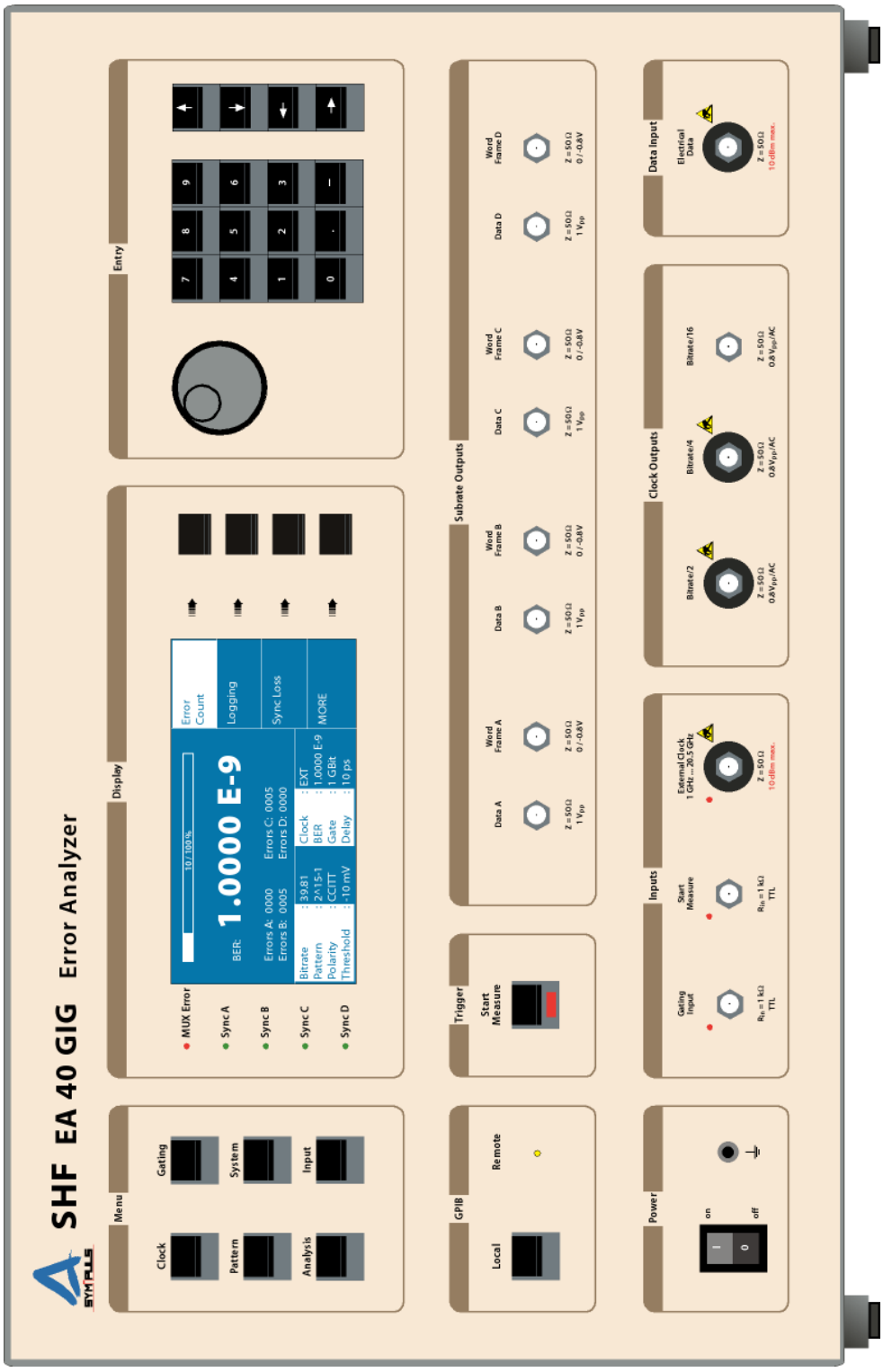
3 Specifications

Synchronization [1]	5 GBit/s…43GBit/s
Phase adjustment of clock and data signal [2]	± 80 ps
Tolerance between data and clock signal (time difference between optimal values of clock and data signals) [3]	± 5ps (± 3.75ps guaranteed)
Clock Input: 50Ω SMA connector, capacitively coupled [1]	 | r | < 0.3 U_i=0.4…1.5 V_{pp}
Bit Pattern: PRBS Noise sequences	2^{31}–1 2^{23}–1 2^{15}–1 2^{7}–1
Trigger Output: Clock with 1/32 bitclock frequency, AC coupled, 50Ω BNC Wordframe clock, 50Ω BNC	 0.7 V_{pp}, | r | < 0.3 0.7 V_{pp}
Data Input: NRZ, logic pos./neg. selectable [2]	 U_i = 0 V / –1 V (typical), | r | < 0.3
Error counter: Display measuring interval (data bits) Error rate	 10^{5}…10^{14} 10^{-5}…10^{-14}
Power supply	90 V…135 V 180V…270 V 47…63 Hz
Weight	20kg
Size (W×H×D)	449×276×444 mm
Operating temperature Storage temperature	+10 to 35°C – 20 to +70°C

[1] Depends on the low frequency limit and sensitivity of the internal 20 GHz 2 : 1 frequency divider at the clock input
[2] 20 GHz precision delay line with DC motor drive.
[3] Depends on the internal 40 GBit/s SHF demultiplexer.

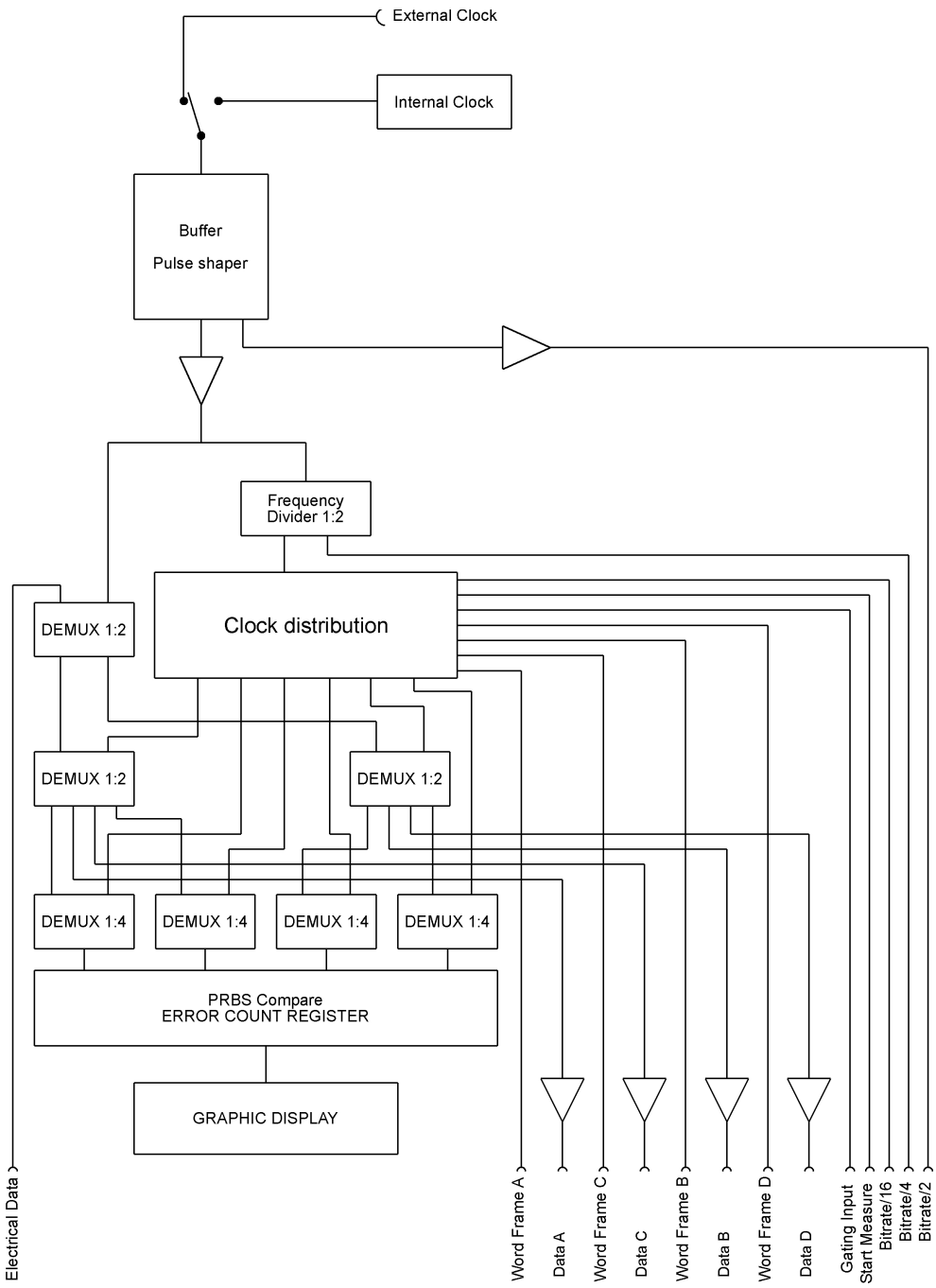
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4 Front Panel



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5 Block Diagram



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