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SHF Communication Technologies AG

Operating Manual

SHF EA 40 GIG

Error Analyzer

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Operating Manual Version 1.02

SHF EA 40 GIG

Error Analyzer

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1 Introduction

The SHF EA 40 GIG Error Analyzer is a tool for the detection of errors in gigabit transmission systems. Used in conjunction with the SHF BPG 40 A Bit Pattern Generator, a system for bit error rate tests can be formed. Ease of use is ensured by simple hardware functions allowing phase adjustments or input threshold variations of the analyzer. It is therefore ideal for research and development of high speed logic MMICs and digital communications systems. Further applications include the testing of high rate PCM and SDH systems as well as digital optical components and sub-nanosecond pulse engineering.

Bit rates up to 44 GBit/s can be analyzed. The bit rate tested is twice that of the clock frequency. An input for an external clock generator is provided, and an internal fixed frequency low noise crystal oscillator clock is available as an option. In Figure 1.1 on the following page, the basic elements of the SHF EA 40 GIG are presented in a block circuit diagram. The clock is buffered and divided into two channels, one of which contains a frequency divider. A 4:1 40 GBit/s fast demultiplexer circuit reduces the input data rate to four signals, each with a rate of 10 GBit/s. The phase shift between the clock and data signals can be adjusted using a computer controlled delay line, offering a delay of up to 160ps, with a resolution of 1ps.

Four further 1:4 demultiplexers then reduce the data rate down to 2.5 GBit/s and compare the data bit by bit to internally generated PRB sequences. Built in PRBS lengths are 2^{31}–1, 2^{23}–1, 2^{15}–1 or 2^{7}–1. Errors are displayed for each channel as well as the total number of errors. Measurement intervals can be varied within the range 10^{6}…10^{16}Bit/s.

Word synchronization is achieved automatically, as indicated by four LEDs which light up when synchronization has been achieved. Shifting of sub-sequences is also tested, and an error is displayed due to incorrect multiplexer signal interleaving, even if a single sub-sequence contains no errors.

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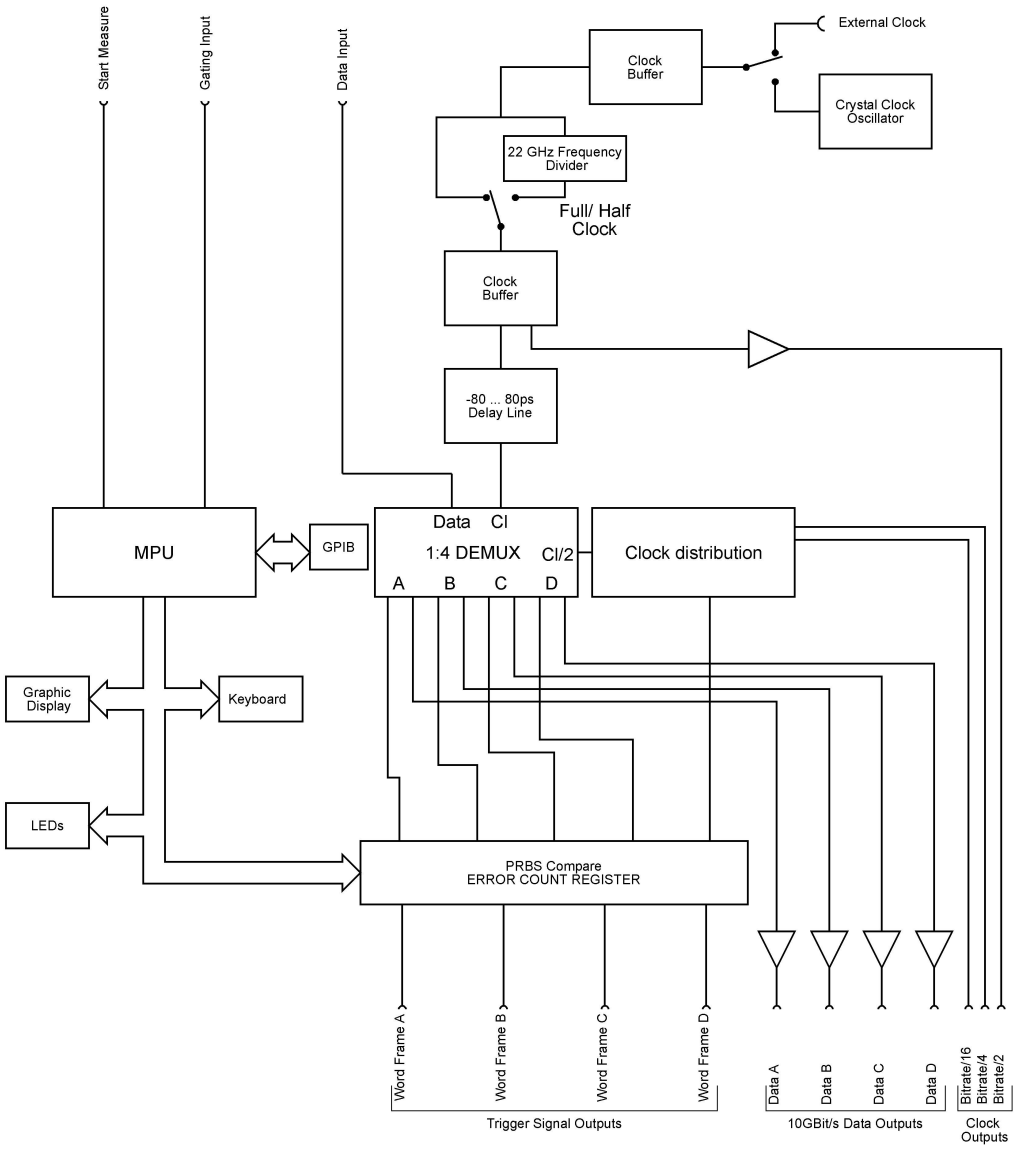


Figure 1.1 Block diagram

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2 Summary of Features

- Handling of CCITT conforming PRBS patterns 2^7–1, 2^{15}–1, 2^{23}–1, 2^{31}–1
- Self-synchronizing; broadband operation
- Threshold adjustment by GPIB or manual thumbwheel
- MUX error indication
- Clock outputs at subharmonic rates
- Word frame outputs from each internal 10 GBit/s channel (A, B, C and D)
- External clock input 22 GHz for BPG 40 A, BPG 44 or BPG 44 E compatibility
- Internal computer controlled 22 GHz timing delay line
- Display of total errors and errors inside each of the four internal 10 GBit/s subchannels
- Full clock input selectable up to 22 GHz
- Internal 6 digit true frequency counter displaying the bit rate
- Measurement sequence start by TTL signal or push button
- Wide range of selectable gate times
- External GPIB control
- Low noise, low jitter timing circuits
- Burst Mode (fast synchronizing) capability

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3 Specifications

Operating range	<5 GBit/s…>44 GBit/s
Phase adjustment between clock and data signal [1]	± 80 ps
Clock phase margin [2] measured with 2^{31}–1 PRBS at 44 GBit/s for an input signal with 100 mV eye height	200°
Clock Input: ruggedized 2.9 mm male connector, capacitively coupled	S_{11}<–10 dB 0.6 V_{pp} 0 dBm
Bit Pattern: PRBS Noise sequences	2^{31}–1 2^{23}–1 2^{15}–1 2^{7}–1
Sensitivity at 44 GBit/s, 2^{31}–1 pattern	<100 mV_{pp}
Trigger Outputs: Bitrate/2, Bitrate/4, Bitrate/16, AC coupled Wordframe, AC coupled	 0.8 ± 0.2 V_{pp}, S_{11}<–10 dB 0.8 ± 0.2 V_{pp}
Data Input: NRZ, logic pos./neg. selectable	max. 1 V_{pp}, S_{11}<–10 dB
Error counter: Display measuring interval (data bits) Bit Error rate	 10^{6}…10^{16} 10^{-6}…10^{-16}
Power supply	90 V…135 V 180V…270 V 47…63 Hz
Weight	20kg
Size (W×H×D)	449×276×444 mm
Operating temperature Storage temperature	+10 to 35°C – 20 to +70°C

[1] 20 GHz precision delay line with DC motor drive.

[2] PMspecified = ((PMmeasured + Peak-Peak-Source-Jitter)/22.73) × 360

Peak-Peak Jitter as displayed on Agilent 86100A Opt. 100 DSO

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Clock output connectors:

Bitrate /2:	50 Ω ruggedized 2.9 mm precision male connector
Bitrate /4:	50 Ω ruggedized 2.9 mm precision male connector
Bitrate /16:	50 Ω SMA female connector

Internal clock generator (Option 01)

60° C ovenized precision crystal oscillator

Available outputs:

1.244 GHz

2.488 GHz

4.976 GHz

9.952 GHz

19.904 GHz

(other frequencies, e.g. 21.5 GHz, available on request)

oscillator stability: $< \pm 1$ ppm/° C;

warm up time: approx. 15 minutes;

ageing: $< 3 \times 10^{-9}$/d

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4 Warnings and Safety Precautions

Disconnect the power cable before opening the instrument. Opening the unit without explicit written permission of the manufacturer will void the guarantee.

Make sure that only fuses with the required rated current and of specified type (normal blow, time delay) are used for replacement.

Never use repaired fuses!

Before switching on the instrument, all protective ground terminals should be connected to a common ground terminal.

The operation of this instrument in a static free environment is highly recommended. Operation of this instrument inside RF fields of more than 10 V/m field strength must be avoided. A trouble free operation can not be guaranteed in such an environment!

Avoid any cellular phone operation within close proximity of the instrument while long term error measurements are in progress.

Because of the very sensitive high speed analogue and digital GaAs technology a number of EMC tests had to be omitted, namely ESD and high electromagnetic fields.

For more detailed information see the IEC 1000-5 sections, which address in detail the mitigation and installation practices with consideration of the relevant ports and associated EM phenomena. The future IEC 1000-5 will address the enclosure port (shielding) and conductive ports (filters, decoupling devices and surge protection).

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5 Operating Instructions

5.1 General Remarks

The instrument has been carefully tested and checked for its specification conformance prior to shipment. To guarantee a long lasting trouble free operation the user should follow all operating hints and warnings listed in this manual.

Failure to comply with these precautions or specific warnings elsewhere in this manual violates the safety standards of design, manufacture and intended use of the instrument.

SHF Communication Technologies AG assumes no liability for the customer's failure to comply with these requirements.

WARNING !

In accordance with international safety standards this instrument has a three-wire power cable. When connected to an appropriate AC power outlet, this cable ensures the grounding of the instrument's metal case.

Do not use power outlets or cable extensions which have only two contacts.

Disconnecting the ground wire will cause health hazards and is strictly forbidden.

The instrument is functional after pressing the power switch.

After a warming up time of 20 minutes it will comply to the listed specifications.

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5.2 Front Panel

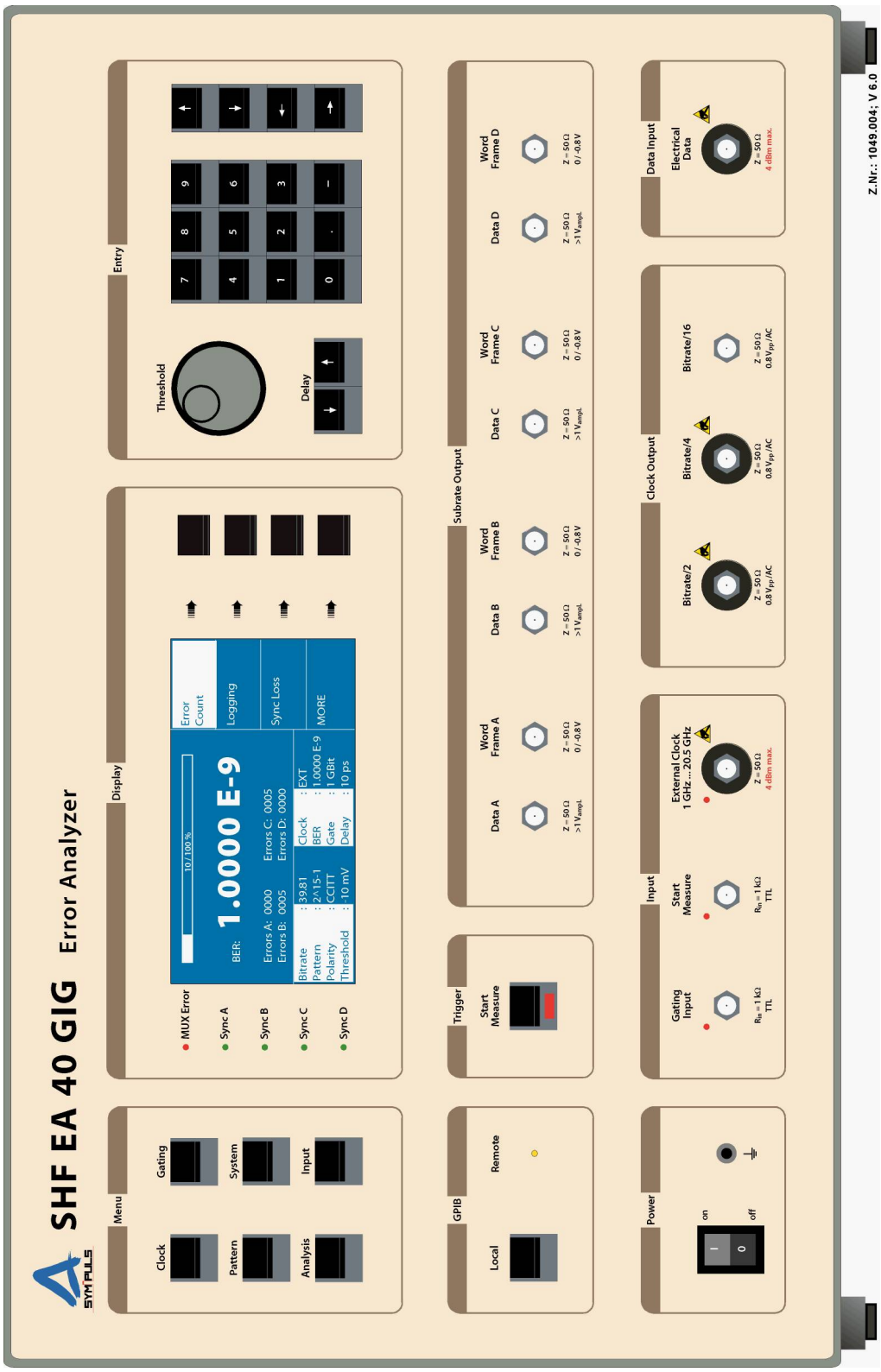


Fig. 5.2 Front Panel

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5.3 Front Panel Operation

For all following descriptions, see the front panel in Fig.5.2. The Front panel is divided into ten rectangular blocks. The blocks **Menu, Display, Entry, GPIB** and **Power** are relevant to this sub chapter.

5.3.1 Power Block

The **Power** block contains the power switch and the ground terminal. This power switch controls the internal DC supply. The main power line switch is located on the rear panel.

To switch on the instrument, actuate the main power switch on the rear panel first and then the power switch on the front panel. To switch off, start with the front panel switch.

5.3.2 GPIB Block

The mode of operation can be switched between local and remote by pressing the button in the **GPIB** block. When the unit is in remote mode, the indicator in the block lights up. The instrument automatically enters remote mode if it receives signals from the GBIP connector at the rear of the unit.

For details of programming the GPIB interface, see the programming manual.

5.3.3 Menu, Display and Entry Blocks

These three blocks work together to control the analyzer. The **Menu** block contains six buttons which switch between the main menus. The **Entry** block allows the user to change the settings shown in the submenus. The **Display** block contains a screen which allows the current menu mode and setting to be read.

The display is divided into three sections, as shown in Figure 6.1.1. The selection field shows the currently selected menu/submenu and the current value of the selected item. The softkey field shows the currently available submenus, which can be selected using the buttons next to each box. The status field shows the current status of the instrument.

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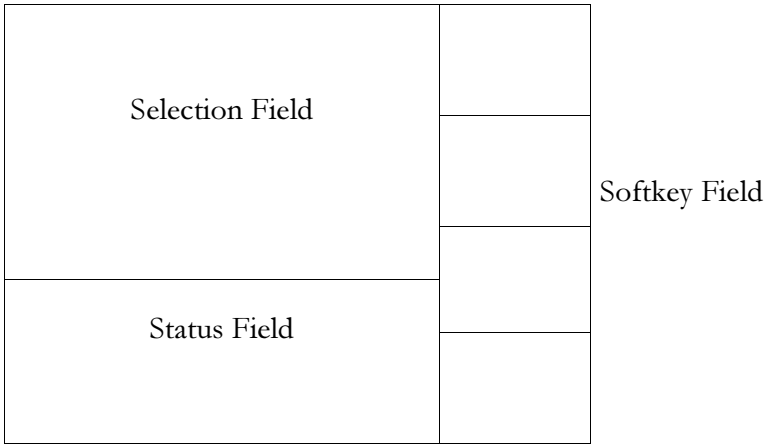


Figure 5.3 The Display Block

5.3.4 Local Operation

The following example of how to operate the EA 40 GIG is based on the menu **Gating**.

Ensure that the instrument is in local operation mode, and that the light in the GPIB block is off.

Select the gating menu by pressing the **Gating** button in the **Menu** block. The selection field in the display will now show **Gating Mode**, with the options **Single** and **Repeat**. In the softkey field, three submenus are shown: **Gating Mode** (already selected), **Gating Period** and **Gate By Bits**.

Press the softkey next to the **Gating Period** submenu. The selection field now shows that the **Gating Period** submenu has been selected, and offers the two options **Bits** and **Time**. These settings determine whether the gating period is set according to a number of bits, or by a fixed period of time.

Press the softkey button **Time**. The gating period time will now be selected in the selection field. The time can be adjusted by using the arrow keys in the Enter block.

All other menus work in the way described above. The structure of the menus described in section 5.4.

There is a rotary dial in the **Entry** block which can be used to set the threshold level of the input. This dial is active regardless of the menu item selected.

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5.3.5 Eye Contour Measurements

The SHF EA 40 GIG can perform an eye contour measurement. First choose a BER limit (10^{-6} to 10^{-12}) in the **Eye contour / BER limit** submenu. This BER limit serves as a criterion to which a measured point is regarded as being inside or outside the eye. Note that the chosen BER limit determines the length of the gating period: the smaller the BER limit, the longer the gate period. A BER limit of 10^{-8} corresponds to a gate period of 100 MBit. In the **Eye contour / Grid** submenu, a simple grid can be enabled or disabled for the eye diagram screen. To select the eye diagram screen, press the soft key **Capture** once. The result of the last eye contour measurement is displayed. Pressing the soft key **Capture** again will start a new eye contour measurement. Note that this will take several minutes or even longer depending on the BER limit and the current bitrate. To cancel a running eye contour measurement press **Capture** again. The measurement stops when the running search at the current delay line position has finished. Note that measurements on very small signals are prone to errors.

The results can be read through the GPIB interface as a data array.

5.3.6 Full Clock Ratio

For bit rates up to 22 GBit/s, the error analyzer can be set to the full clock ratio mode. This can be done with the soft key **Ratio** in the **Clock** menu.

5.4 Gating Modes

Single: Gating period is started by pressing the **Start Measure** key and terminates at the end of the gating period set by the user. Accumulating results are displayed throughout the gating period (>1 s). At the end of gating, results are stored and displayed until a new gating period is started.

Repeat: Gating period starts automatically. After one timed gating period, a new identical period starts. During long gating periods (>1 s) accumulating results are

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displayed throughout the gating period. During short gating periods (<1 s) only final results of the preceding period are displayed.

5.4.1 Burst Gating Mode

The burst gating mode menu can be accessed through the gating menu by pressing the **Burst Gating** soft key which enables or disables the burst gating mode. The burst gating mode is indicated by the illuminated LED next to the gating input. At the same time, the status field of the graphic display changes from the entry *Gate* (which shows the current gate time) to *Burst*, which shows the selected burst length. The burst length is the measurement interval (after successful synchronization) following a negative going starting pulse on the gating input. It can be set from 10 µs to 10.24 ms in 10 µs steps with the soft key **Burst Length**. The number of burst cycles analyzed in the burst gating mode can be set using the soft key **Burst Cycles** between 1 and 262140. Finally a timeout value must be set to prevent the error analyzers from hanging after it receives a start pulse but fails to synchronize. The timeout determines the time between receiving a start pulse of a cycle and synchronization of the analyzer. If the error analyzer could not successfully synchronize, it is counted as "failed". The timeout value can be set under the soft key **Burst Timeout** from 105 ms to 26.88 s in 105 ms steps.

If the instrument is in the burst gating mode, only final results are displayed; no temporary results. The total number of errors and the number of errors in the four sub channels A to D are displayed in the status field of the graphic display. The number of valid burst cycles, the effective gate time and the bit error rate are displayed in the selection field if the error count screen in the analysis menu is selected. If the instrument is just taking a measurement, the LED in the **Start Measure** key is illuminated. Please note that for a large number of burst cycles it may look as if the instrument hangs because no temporary results are returned.

The instrument tries to perform measurements for the given numbers of burst cycles. If a synchronization fails for an individual measurement it is reported to the user. That means the number of successfully measured burst cycles is displayed as valid burst cycles.

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The effective gate time in the gating burst mode is:

$$effective\,gate\,time = burst\,length \cdot valid\,burst\,cycles$$

The bit error rate in the burst gating mode is calculated as follows:

$$bit\,error\,rate = \frac{number\,of\,\,total\,errors}{number\,of\,\,analyzed\,bits} = \frac{number\,of\,\,total\,errors}{effective\,gate\,time \cdot bitrate} = \frac{number\,of\,\,total\,errors}{burst\,length \cdot valid\,burst\,cycles \cdot bit\,rate}$$

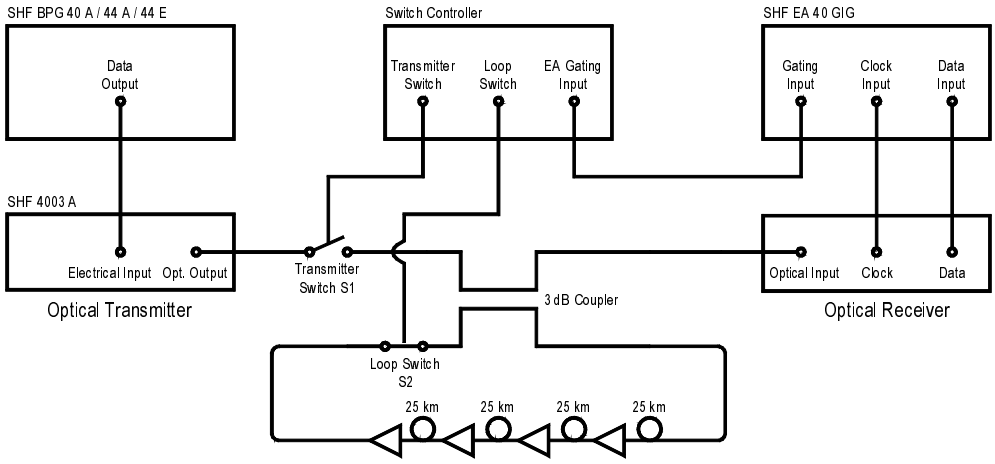


Fig. 5.4. Loop transmission block diagram

The burst gating mode is required in loop experiments. A typical recirculating loop is shown in Fig. 5.4. Let us assume that the length of the loop is 100 km and the speed of light in the fiber is approximately 5 µs/km. The loop is loaded with data, this requires about 500 µs, then the data is recirculated for a specified time, which equates to the distance propagated. Now a measurement is taken, the loop is emptied and the whole process is restarted. Usually, acousto-optic modulators are used for optical switching which have a high extinction ratio, low insertion loss and high switching speed.

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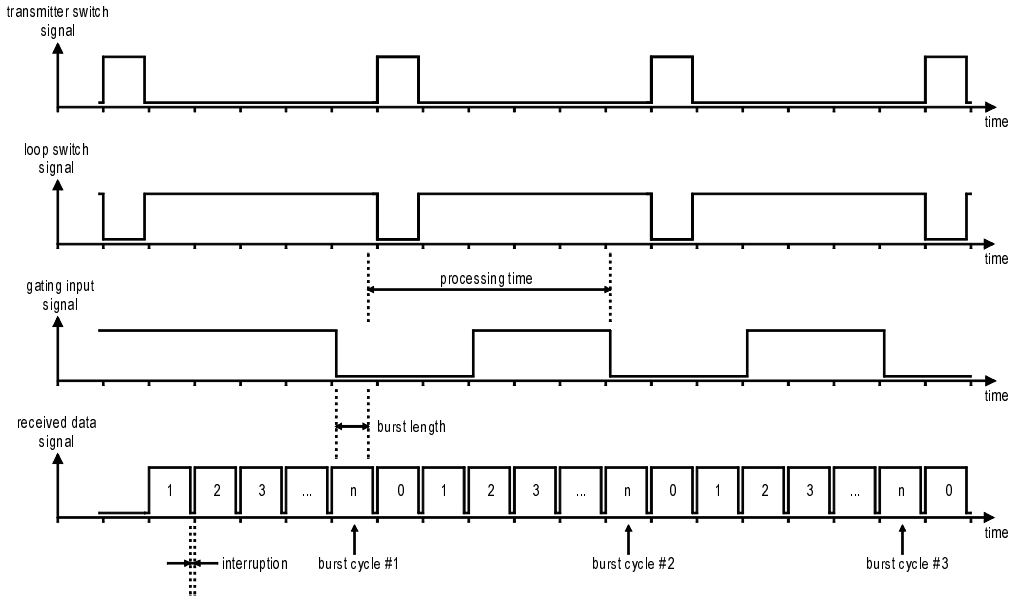


Fig. 5.5 – Received data and switch controller timing

As seen in Fig. 5.4, there is a transmitter switch (shown open) and a loop switch (shown closed). The timing diagram can be found in Fig. 5.5. It is simplified by showing the loop switch as the complement of the transmitter switch. Initially, the transmitter switch is closed and the loop switch is open. For our hypothetical 100 km loop, it would take about 500 µs to fill the loop with data. Once the loop is filled, the transmitter switch is opened and the loop switch is closed. Now the data starts circulating. The length of time that the two switches remain in this state determines the maximum distance the data travels. Let's assume the data should be analyzed after 10,000 km: this time is then approximately 50 ms. After this time, the two switches reverse states and the loading restarts.

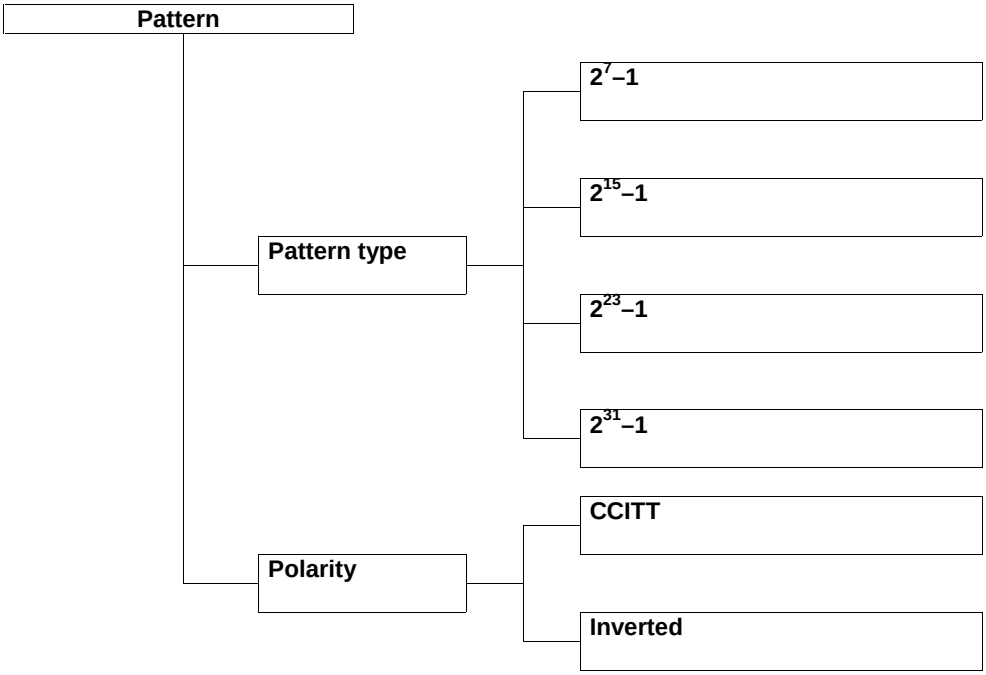
To analyze the data after a certain distance, a gating signal at the input of the error analyzer is required to start the measurement. The measurement starts with the negative-going pulse. The above example shows, that after approximately 50 ms, the signal at the gating input must change from high to low to start the measurement of length *BURST LENGTH*. This process continues until the preselected number of *BURST CYCLES* has been measured.

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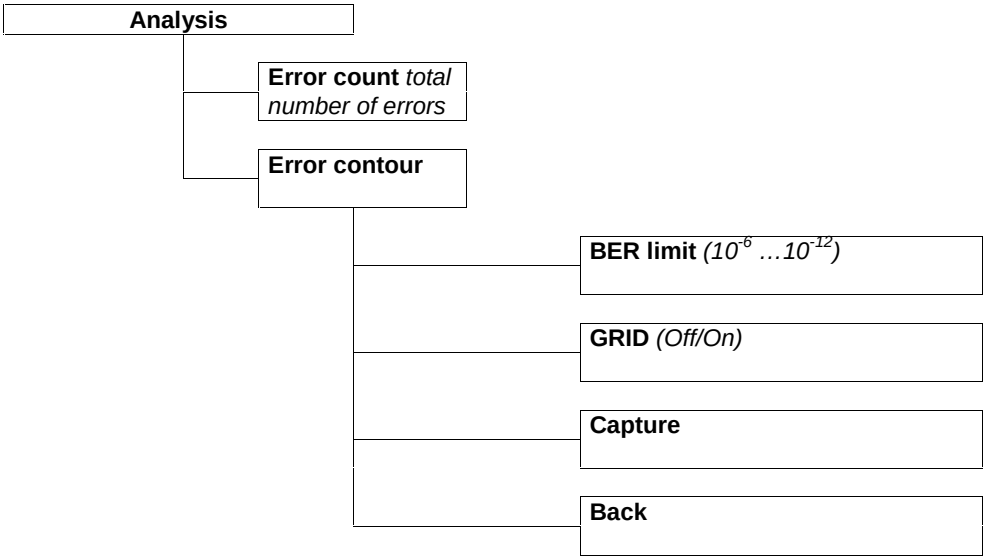
5.5 Menu Structure

The structure of the menus is shown in the following diagrams. Words which appear in bold are those which appear on the screen. Those which appear in italics are explanations (when necessary) of the menu item.

5.5.1 Pattern Menu

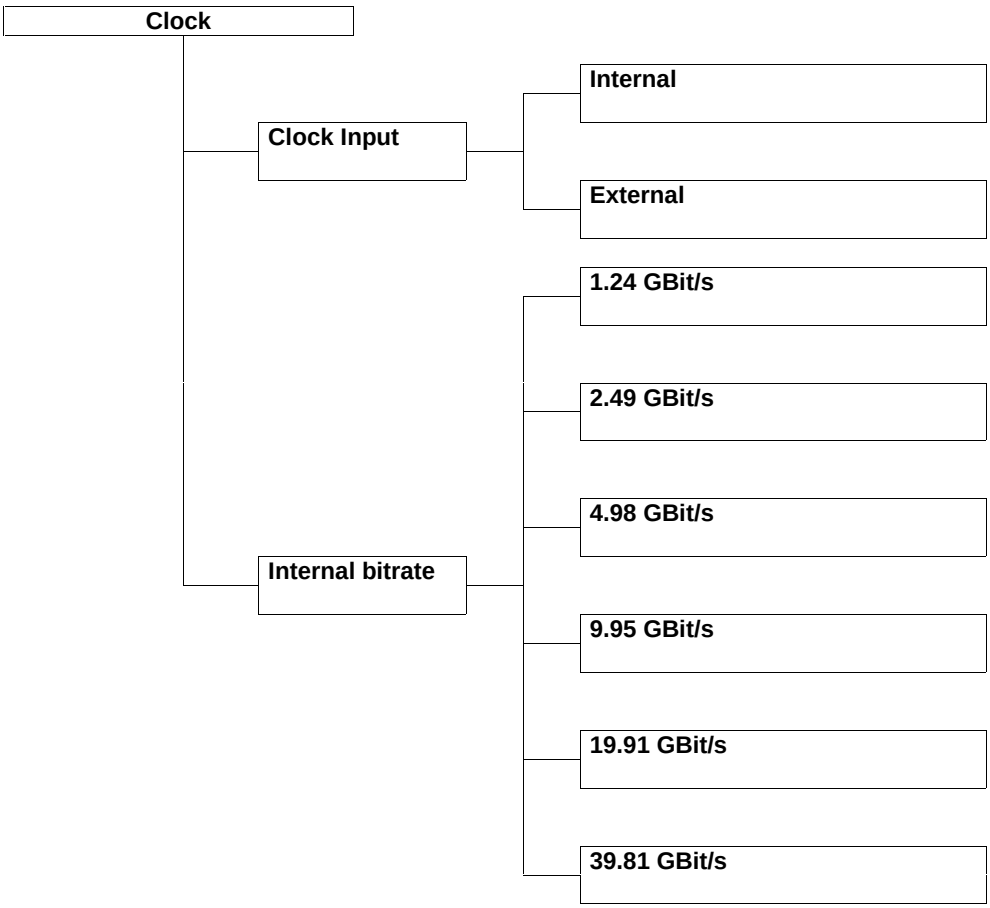


5.5.2 Analysis menu

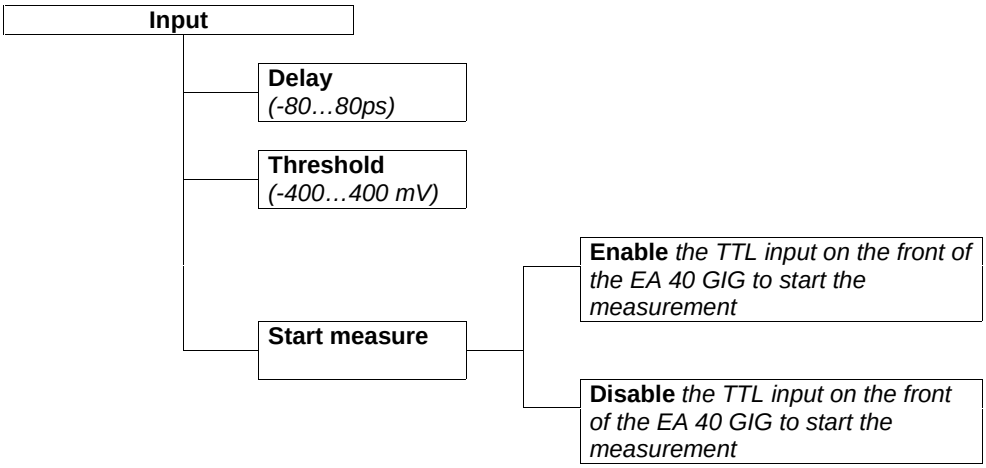


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5.5.3 Clock Menu

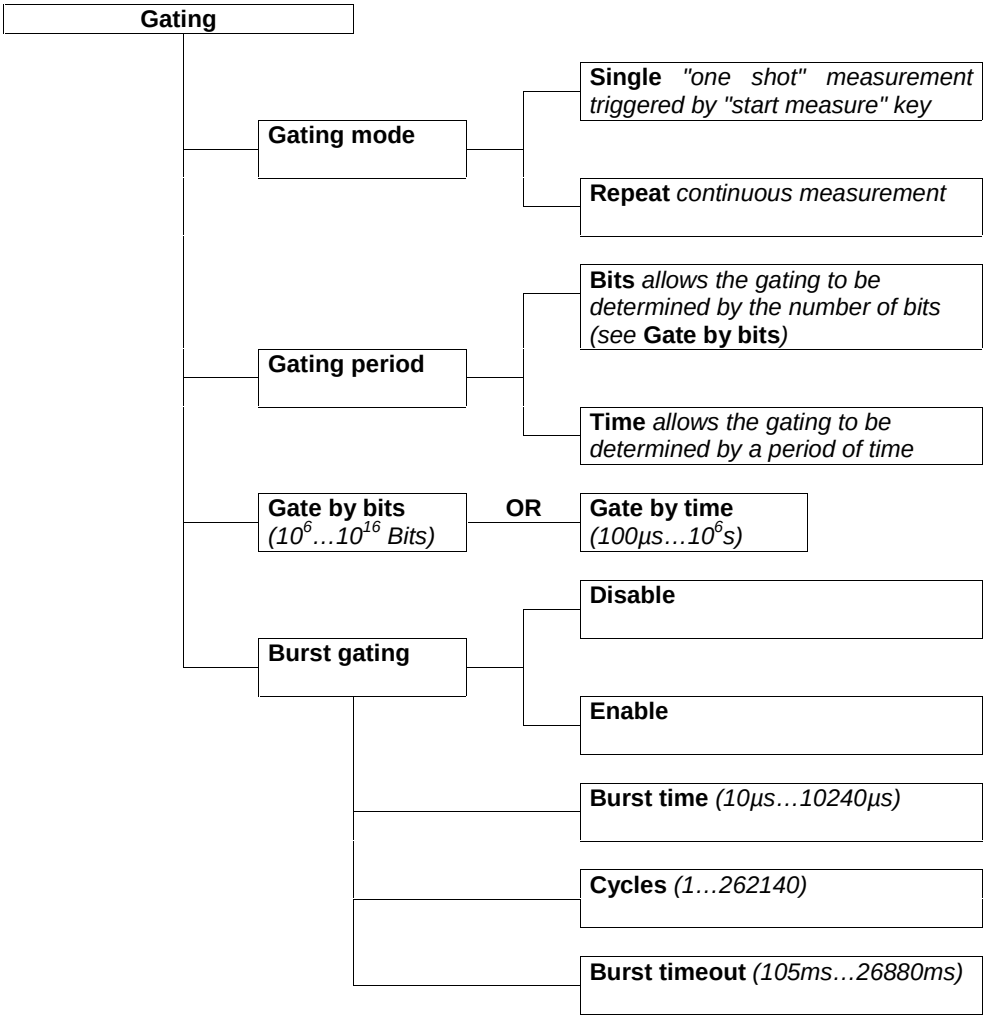


5.5.4 Input menu



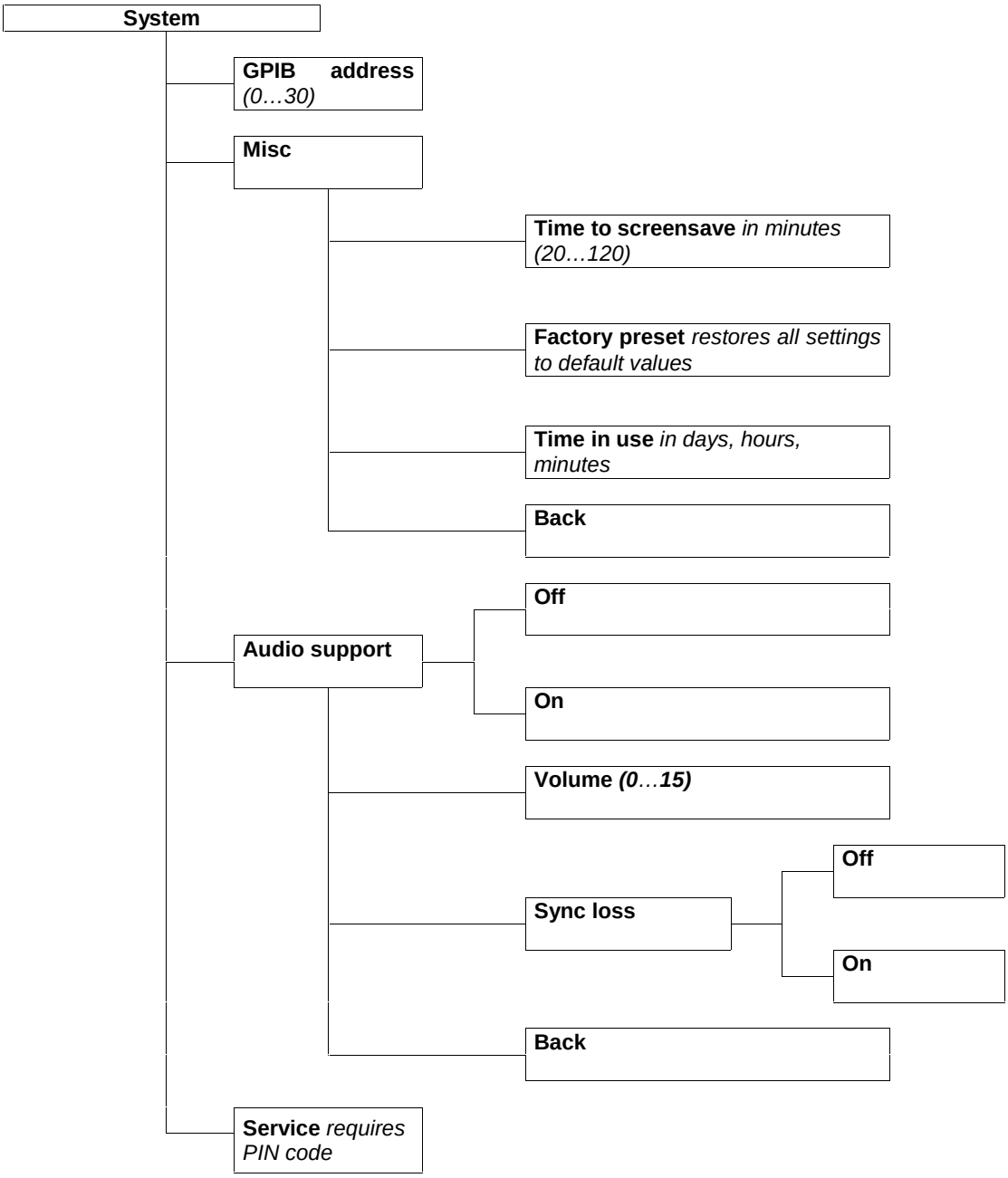
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5.5.5 Gating Menu



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5.5.6 System Menu



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5.6 Front Panel Connections

5.6.1 Input Block

Gating Input (SMA female connector)

This feature is set by going to the **Burst Gating** screen in the **Gating** menu and activating it from there.

Start Measure

The SMA female connector is the external input terminal which allows measurements to be started with a TTL pulse. The input is switched on and off in the Input Menu.

External Clock

The 50 Ω ruggedized 2.9 mm male connector is the external clock input terminal.
To synchronize the generator an external clock signal with 50 % duty cycle (sinusoidal, square) of approximately 0.6 V_{pp} amplitude has to be connected to the clock input connector.
Without sufficient clock input amplitude the instrument will not work properly.

5.6.2 Clock Output Block

This block contains the clock output terminals.
Clock outputs:

Bitrate/2:	50 Ω ruggedized 2.9 mm precision male connector
Bitrate /4:	50 Ω ruggedized 2.9 mm precision male connector
Bitrate /16:	50 Ω SMA female connector

The output level of the clock outputs is 0.8 ± 0.2 V_{pp}
The clock output connectors should **ALWAYS** be connected to a 50 Ω load.

5.6.3 Trigger Block

This can be used to start or restart a measurement when in single mode.

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5.6.4 Data Input

The data input is a 50 Ohm ruggedized 2.9 mm male connector. Note that the maximum input level must not exceed 1 V_{pp}.

5.6.5 Subrate Outputs

These are 50 Ohm SMA connectors. The wordframe outputs produce an output which is correlated to the wordframe of the bit pattern.

5.7 Internal Clock Generator

The internal clock generator uses a high precision ovenized crystal oscillator at 103,679 MHz as a fundamental source. A few minutes warm up time is necessary to bring it up to its final temperature of 60° C. A buffer and a tripling stage lead to a frequency of 311 MHz. A narrow band filter and an output driver amplifier are connected ahead of each SMA outlet. To feed all higher outputs up to 19.909 GHz each lower frequency is fed to an active doubling circuit and afterwards via a narrow band filter to the output driver amplifier. In this way the following frequencies are generated with high stability and very low phase noise:

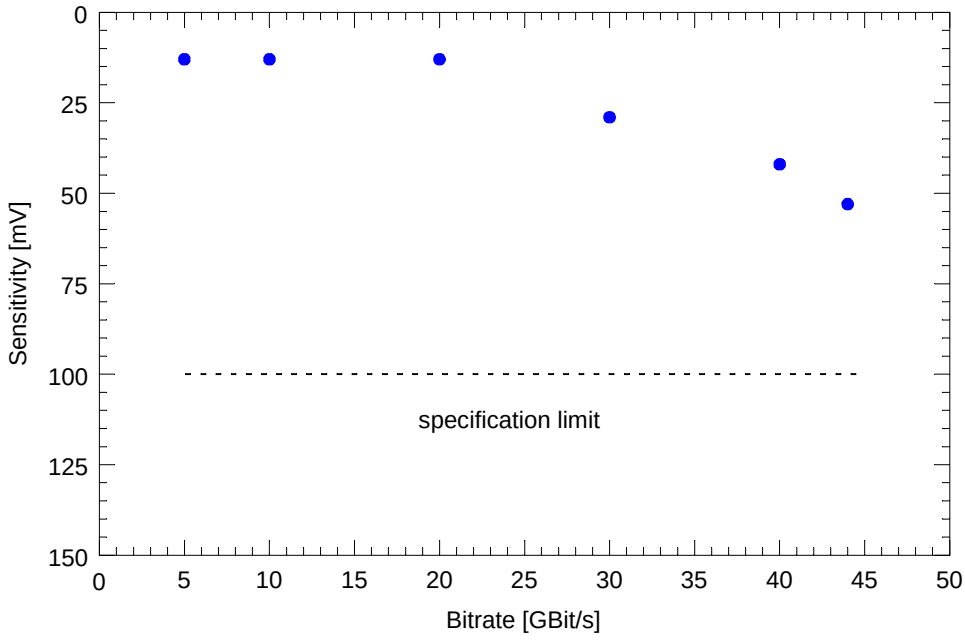
- 622 MHz
- 1.244 GHz
- 2.488 GHz
- 4.977 GHz
- 9.954 GHz
- 19.909 GHz

The required signal is selected via a rotary coaxial relay and fed to the clock input of the pattern generator.

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6 Performance: Test and Measured Results

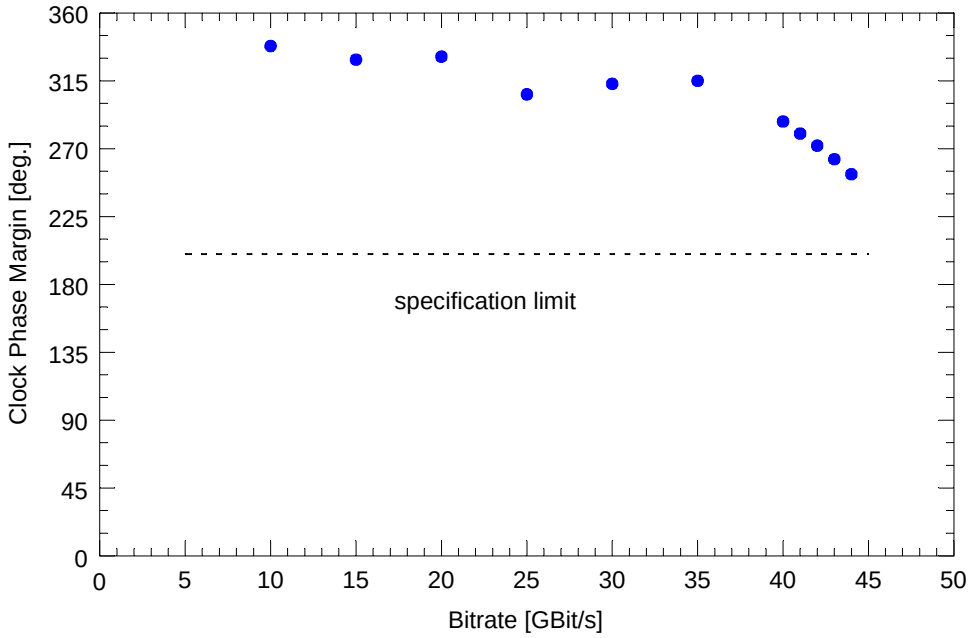
6.1 Sensitivity Measurement



- BER Limit 10^{-9}, PRBS 2^{31}-1
- Input signal attenuated with fixed attenuators until sensitivity limit was reached
- shown value corresponds to the measured eye height on an Agilent 86100 A Opt. 100 DSO

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6.2 Clock Phase Margin Measurement

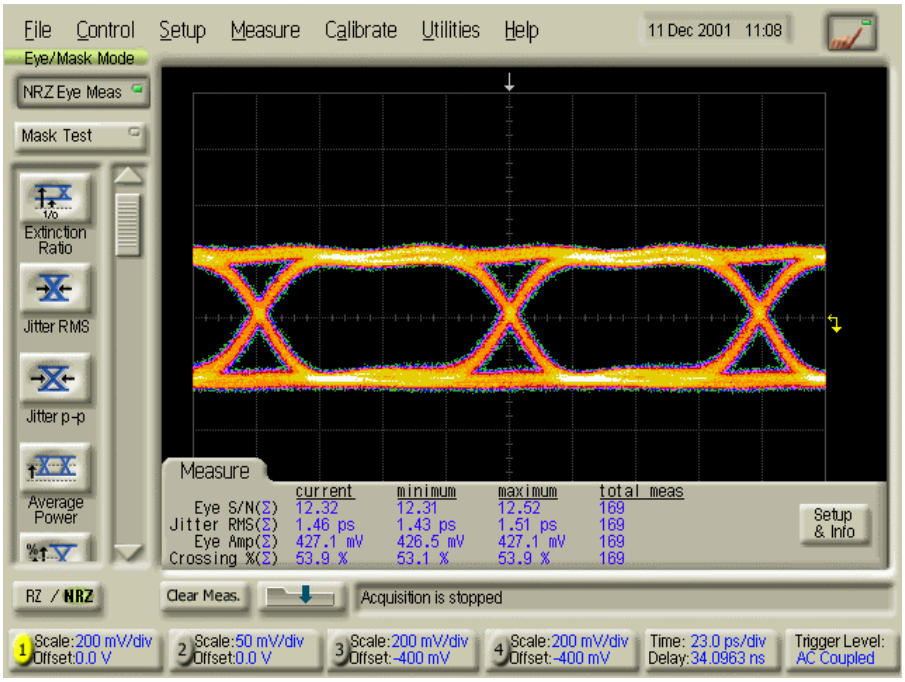


- BER Limit 10^{-9}, PRBS 2^{31}-1, Eye Height 100 mV, Peak-Peak-Source-Jitter 5 ps
- Peak-Peak-Source-Jitter as displayed on an Agilent 86100 A Opt. 100 DSO
- calculated using the formula:

$$\text{Clock Phase Margin [deg]} = \frac{\text{Phase Margin (measured) [ps]} + \text{Peak - Peak - Source - Jitter [ps]}}{\text{Eye Length [ps]}} \cdot 360°$$

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6.3 Subrate Output Signal



- PRBS 2^{31}-1
- Input bitrate = 44 GBit/s

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7 Mechanical Design

The 19" housing carries inside three solid 6 mm aluminum mounting plates. They strengthen the whole structure considerably and at the same time act as heat sinks for all the power dissipating components within the cabinet.

The three levels of mounting plates carry the microprocessor circuit board, the switch mode power supplies, all sub-modules, the demultiplexers and the output driver amplifiers.

The rear side of the cabinet carries the AC power socket, the service connector and the GPIB input connector. The main line fuse is located inside the AC power socket.

The front panel carries all microwave connectors and all operational controls as well as the graphic display.

The microwave connectors are wall feed through types which could be replaced in the factory if accidentally damaged.

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8 Maintenance and repair

The SHF EA 40 GIG error analyzer does not contain any user serviceable parts. The only required outside maintenance is the regular cleaning of all microwave connectors, which should be done according to the frequency of their use.

Should the SHF EA 40 GIG fail to comply to the performance tests listed in chapter 6, the factory should be contacted. A field repair is not possible in most cases since all of the SMD components on the microwave boards and within the modules are selected special types. Servicing the instrument can only be done at the factory. Before returning the instrument a precise error analysis should be made and detailed information about the failure in the laboratory set-up should be completed and be sent to the manufacturer.

In this way a repair down time can be minimized.

Opening the cabinet must only be performed by qualified personnel. Remember to remove the power cable before attempting to open the case. The case can then be opened by loosening the screws on the side of the cover. Now the two halves of the cabinet can be removed and put aside after disconnecting the grounding cables. **Opening the cabinet without explicit written permission from the manufacturer will void the guarantee!**

Do not forget to attach the grounding cables again before closing the unit.

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9 Declaration of conformity

According to ISO / IEC guide 22 and ISO 9001

Manufacturer: SHF Communication Technologies AG
Amalienstr. 14
D-12247 Berlin, Germany

declares

Product name: Error Analyzer

Model number: SHF EA 40 GIG including all options

This product complies with the essential product requirements of the European EMC Directive 89/336/EEC and the low voltage Directive 72/23/EEC.

It also conforms to the following EN-Standards:

Safety: EN60950(1992) + A1(1993)+ A2(1993)
A3(1995)+ A4(1997)

EMC: EN 55022 (08.1994)+ A1(05.1995) Group1 Class A*
EN61000-4-3(09.1996) 10Vm (Radiation immunity)
EN61000-4-6(07.1996) 10V (Injection)
EN61000-4-4(03.1995) 2kV (fast transients)

The product also conforms to the CE standards

* The product was tested in a typical laboratory configuration (Type test).
Because of the very sensitive high speed analogue and digital GaAs technology a number of EMC tests had to be omitted, namely ESD and high electromagnetic fields.



Berlin, December 14, 2001 Dietmar Aue

QS Manager

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10 Warranty

SHF Communication Technologies AG assures that this product is produced according to ISO 9001 quality standards and has left the factory in a perfectly functioning condition complying to all specification listed inside chapter three of this manual.

The instrument is warranted against defects in material and workmanship for a period of one year from the date of shipment. During this period SHF Communication Technologies AG will, at its choice, either repair or replace a product that proves to be defective.
For warranty service or repair the instrument must be returned to the factory or a service facility designated by SHF design. The buyer shall prepay the shipping charges to SHF Communication Technologies AG and SHF Communication Technologies AG shall pay shipping charges to return the instrument to the buyer. However, the buyer shall pay all shipping charges, duties and taxes for products returned to SHF Communication Technologies AG from another country.
Further services and especially any first order or secondary damage claims of the buyer are explicitly excluded from the sales contract.

This warranty shall not apply to damages resulting from improper or inadequate maintenance or handling by the buyer, unauthorized modification or misuse and operation outside the environmental specifications for the product or improper site preparations.

The warranty expires immediately after unauthorized opening of the housing either by the buyer or any other person

Berlin, December 14, 2001

SHF Communication Technologies AG
the bandwidth company

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History

Erstellt am:	13.12.01	von: J. Wilkes
Korrektur am:	14.12.01	von: J. Wilkes
Freigegeben am:	14.12.01	von: M. Martin

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