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9. PRINCIPLE OF OPERATION

(Refer to block diagram)

(1) is a switch for selecting the (3), (4) or (5) module. Remote-controlled selection can be performed by (2).
The level of the selected luminance signal is set by (6) and the signal is applied to (7). Sync and setup signals coming from (9) and (8), respectively are attached to this luminance signal.
The signal of (7) is amplified by (10) to become the luminance signal output. (11) serves to keep the signal pedestal down to a uniform value. (12) receives the modulation signal from the unit and the pedestal position is kept to a uniform value by (13). The subcarrier signal from (15) is modulated by (14) and the R-Y signal is produced. (16), (17) and (18) work in the same way and the B-Y signal is produced. (19) creates the modulation signal for color burst and the color burst signal is produced at (20). This signal alone can be fed out at (21). These three signals are added and mixed at (22), and they are amplified by (23) to become the chroma output signal. This is combined with the (10) signal to form the VBS OUT signal. (24) is a crystal oscillator whose frequency is selected by the (25) switch. At the INT position, the output divided by the fixed resistor is applied to the VCO (24), where a 4 fsc is oscillated. After having passed through the buffer (26), the 4 fsc becomes as a CLOCK signal at the H.ROM (42). On the other hand, the signal latched by (28) becomes as a CLOCK signal at the V.ROM (43). Data of each sync signal for 1H period are recorded in (42), while data of each sync signal for the vertical component of 2 fields are recorded at (43). These outputs are mixed by (47), and pass through the buffer (48), then are sent to

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the corresponding circuit. (29) serves to vary the phase of the subcarrier signal and (31) generates a subcarrier phase modulated signal for the modulation 12.5T signal.

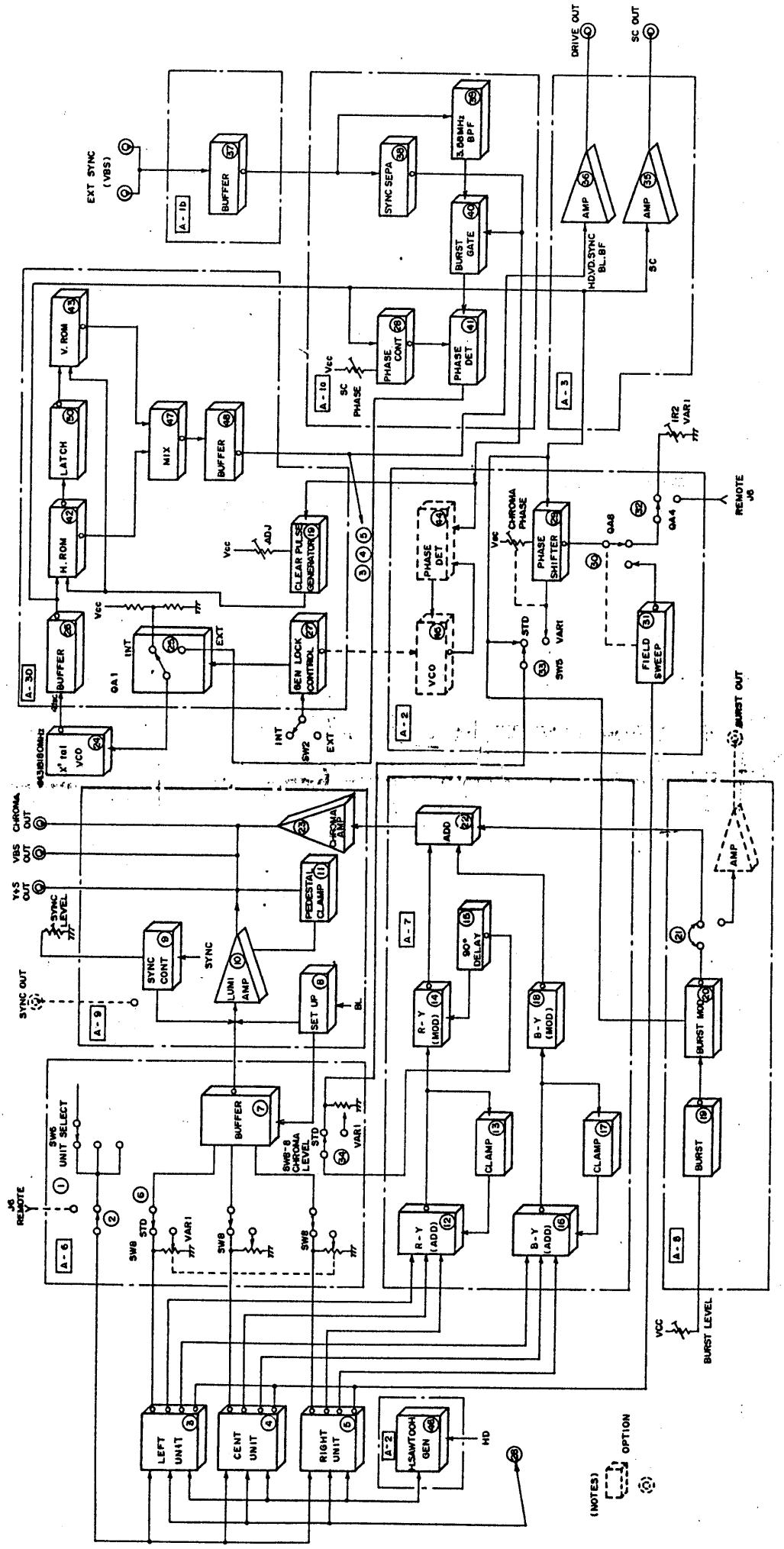
When the U702 module is selected by (1), (30) is connected to (31) and (29). (32) serves to select the phase adjustment mode. (33) selects the phase of the subcarrier signal applied to the chroma modulator. (34) sets its level. (35) is the subcarrier signal output circuit.

(36) is the drive signal output circuit. When the (25) switch is set to the EXT position, the sync signal is separated by (38) from the VBS signal fed in from (37).

The chroma signal is separated by (39) and, using the (38) sync signal, the color burst signal is taken out by (40).

The phase of this signal and of the subcarrier signal is detected by (41) and the output is applied to (24) from (25) to lock the subcarrier onto the external color burst signal input. An external signal supplied from (38) becomes as a CLEAR PULSE at (49) for the ROM's (42) and (43). By detecting whether external sync or internal sync is supplied, (27) controls (25). (45) and (44) make up for the optional circuit so that locked status can be established with an external B/W signal. (46) generates a precise sawtooth wave signal which is synchronized with the horizontal sync signal. This signal is made the reference in the unit and the timing pulse of the output signal waveform is produced.

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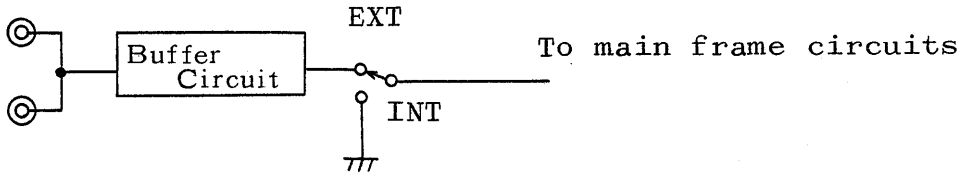
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10. DESCRIPTION OF CIRCUITRY

10-1 Buffer circuitry [A-1b]

Q1 is a buffer which connects the main frame circuit with the external sync input connector and it sends the input signal to the [A-1a] board. In the internal sync mode, Q2 turns on and Q1 is cut off.

External sync input signal
or composite color video
input signal



10-2 Sync separator and color lock [A-1a]

This circuit board separates the color burst signal and sync signal from the external composite color video signal (VBS) and it performs color lock with the phase detector.

Q3, Q4 and Q5 configure an amplifier for sync separation with the signal supplied from the [A-1b] board. The sync end is clamped to about +4V by the feedback circuit composed of Q6, D6 and QA1A and sync separation is performed by the QA2A/B comparator. Q7, QA1B and Q8 form the AGC circuit and the internal resistance of Q7 is controlled so that the signal amplitude applied to the above comparator is made constant at all times. This action serves to keep down the fluctuations in the sync separation signal phase

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with respect to the variations in the external sync signal. C24 and L1 are tuned to 3.58MHz, and the color burst and chroma signals are separated at Q16 and Q17. Since the Q16 emitter has a low impedance, the 3.58MHz component to the sync separator circuit is excluded. Q18 and Q19 form the color burst signal AGC circuit, the burst gate pulse is produced by Q21 and Q22 while the color burst signal is gated at Q19 and then taken out. The signal peak is detected at Q23, D9 and QA3B, the signal is then applied to the Q18 gate and AGC is performed by controlling the internal resistance. This action serves to keep down the phase shift in the subcarrier of the color lock circuit, which is produced by the fluctuations in the external burst signal.

QA5 is a phase detector IC for color lock and it detects the phase of the subcarrier signal from Q13 and the phase of the color burst signal from Q23. This is amplified by Q26, the signal is passed through L2, L3, C41 through C44 low-pass filter and taken out at the Q27 buffer.

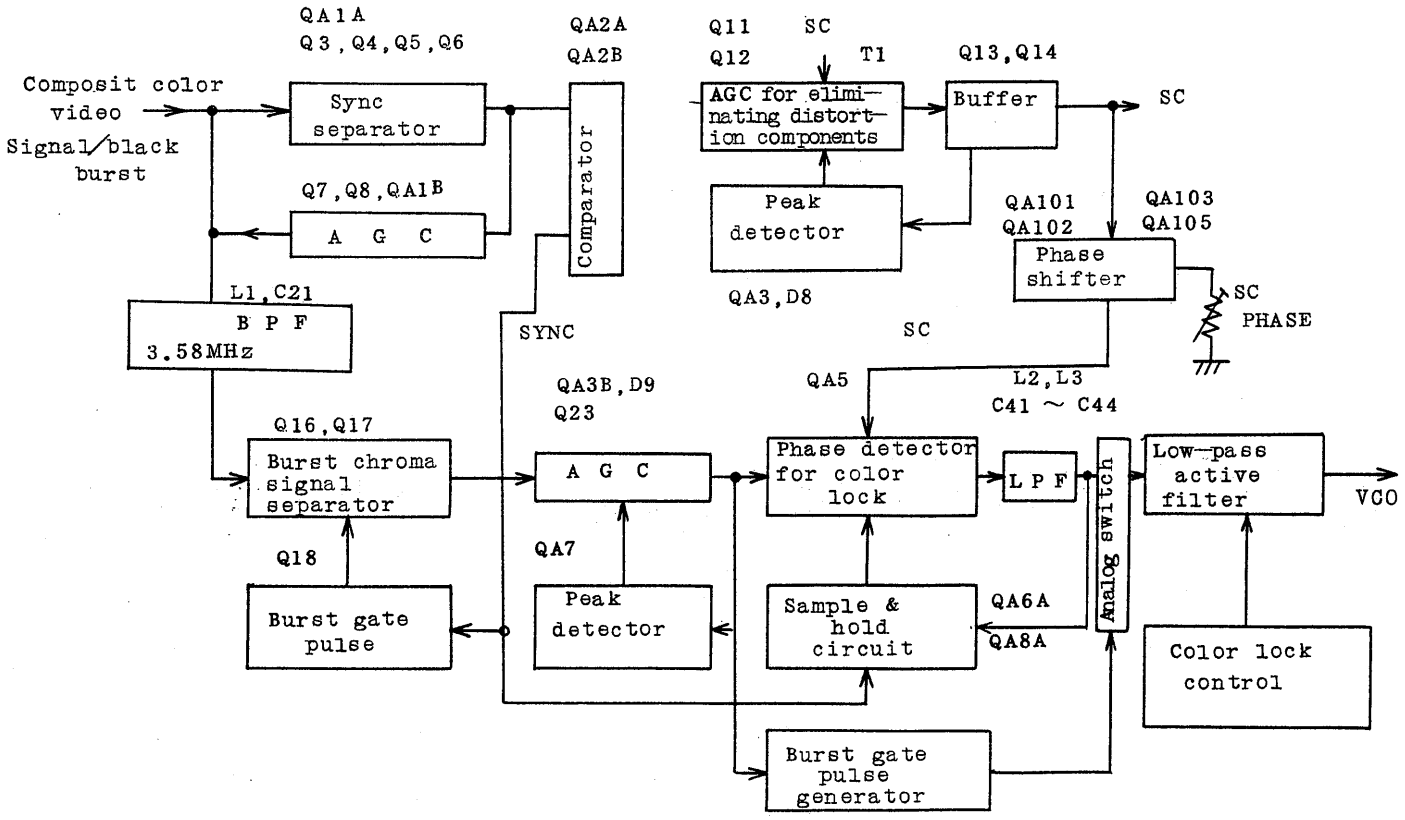
QA9 is an analog switch, the sync signal position of the Q27 output signal is sampled with the QA2B signal and held by QA6A. This voltage is fed back to QA5 and the center voltage of the color burst position and phase detector is clamped to 0V (DC). Furthermore, the signal is sampled with the pulses from QA7 and held by C47 and QA8A. QA8B is a low-pass active filter and color lock is performed by applying its output signal to the A-3D VCO. QA6B and Q28 are a switch circuit for facilitating lock pull-in and for selecting the time constant of the filter. Q28 turns off when color lock is performed.

The distortion components contained in the subcarrier signal

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supplied from A-3D are removed by Q11, Q12 and T1, and the signal is sent to the A-3D board by the Q13 and Q14 buffer. The peak of the signal is detected by D6 and QA3, the signal is applied to the Q12 base and the output level is kept constant by controlling the collector current.

QA101 through QA105 compose the phase shifter, and the phase difference of the subcarrier generated internally and the phase of the color burst signal supplied externally is adjusted by the SC PHASE variable resistor control on the front panel.



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10-3 Subcarrier phase shifter, H sawtooth wave generator circuits A-2

The phase of the subcarrier signal is varied on this board and the H sawtooth waves are generated which determine the timing of the unit H period. Also, clock pulses for the black-and-white external sync use are provided.

QA1 turns the subcarrier signal supplied from A-2 into square waves, their frequency is halved (1/2) by the QA2 flip-flop IC and the signal is applied to the QA5 monostable multivibrator IC. Q1, Q2, Q3 and QA6 configure a constantcurrent type of sawtooth wave generator circuit.

QA7 is a comparator which compares the QA6B op amp signal with this signal and the difference is applied to the QA9 monostable multivibrator. The 1R2 DC signal or Q4 field sawtooth wave signal is selected by the QA8 analog switch and applied to QA6B. This operation causes the phase to change in line with the QA6B signal. The timing of the QA9 monostable multivibrator is selected to a period in which the 3.58MHz signal can easily be reproduced.

Q5 and Q6 form a limiter circuit, its output is routed through the L1 through L6 and C18 through C22 3.58MHz band-pass filter and a variable phase subcarrier signal is produced. This is selected by the QA10 analog switch and sent to A-3D and A-6 from Q7 and Q8. QA3 and QA4 control their selection.

Q12, Q13 and QA11 compose a constant current type of sawtooth generator circuit which determines the timing in the H period of the unit signal. This is triggered by the HD pulse and sent to the unit from the QA14 and Q16 buffer.

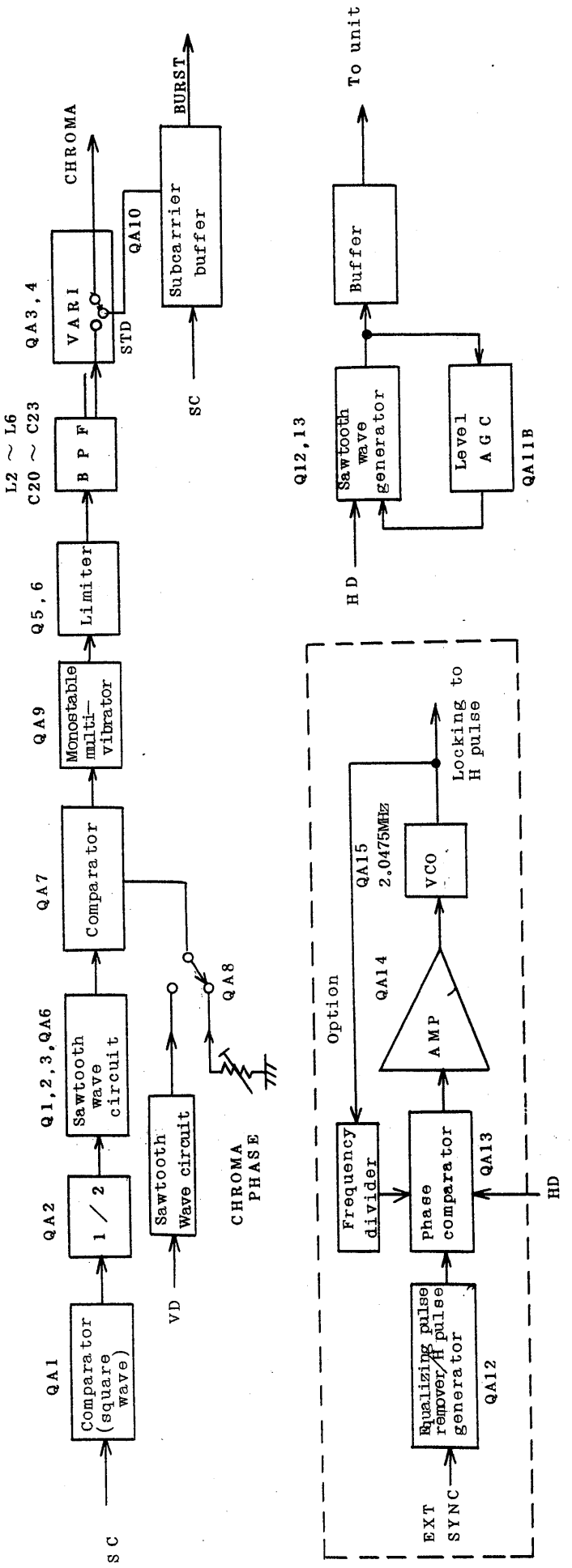
The QA12 monostable multivibrator removes the equalizing pulses of

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the external sync signal from A-1a and generates the H pulses. Together with the clock pulse whose frequency has been divided by QA16, QA17C, QA17D and QA18, this is applied to the QA13 phase comparator, the output is amplified by the QA14 op amp and the QA15 VCO is controlled. This operation serves to lock the VCO to the H pulse at a frequency of 2.0475MHz. This pulse is sent to the A-3 board by QA17B.

Q17, Q18, QA17A and QA18B are designed to activate the above circuit in the black-and-white mode only.

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10-4 Internal sync signal and gen-lock circuits [A-3D]

This circuit board generates the drive signals and other signals required for this signal generator and it performs gen-lock. The 14MHz signal from the VCO is turned into square waves by Q1, Q2 and QA11A, and the cock pulses for the counter (QA14, QA15 and QA16) are produced. Outputs from this counter is used as an address input for the H.ROM QA22. Pulse width for 1H period of each signal is recorded in QA22, while pulse width for 4 fields of each sync signal is recorded in QA28. These outputs are latched by QA29, and at QA22, BL and BF are synthesized with H.BL and H.BF from the H.ROM QA22. Similarly, horizontal and vertical components of SYNC is synthesized at QA35. These synthesized signals are latched by QA23, then will be output from the driver QA7.

QA41 and QA42 make up for the buffer amplifier for the drive output. Frame pulses are produced at QA4D, QA8A and QA7B. Serration pulse is latched at QA24A.

Subcarrier (SC) divides the 14MHz square wave from QA11A and QA11D into 1/4 at the counter QA34B, and sends the divided frequencies to the PC board A1a, where their waveforms are shaped. Then, they are output after having passed through the amplifier (Q3, Q4 and Q5).

QA24B, QA12A, QA12B, QA12C and QA11C make up for the circuit to generate clear pulses for each 1H period of the counter used for the H.ROM. QA8B, QA17A, QA2 and QA25C make up for the circuit to generate clear pulses during EXT LOCK status.

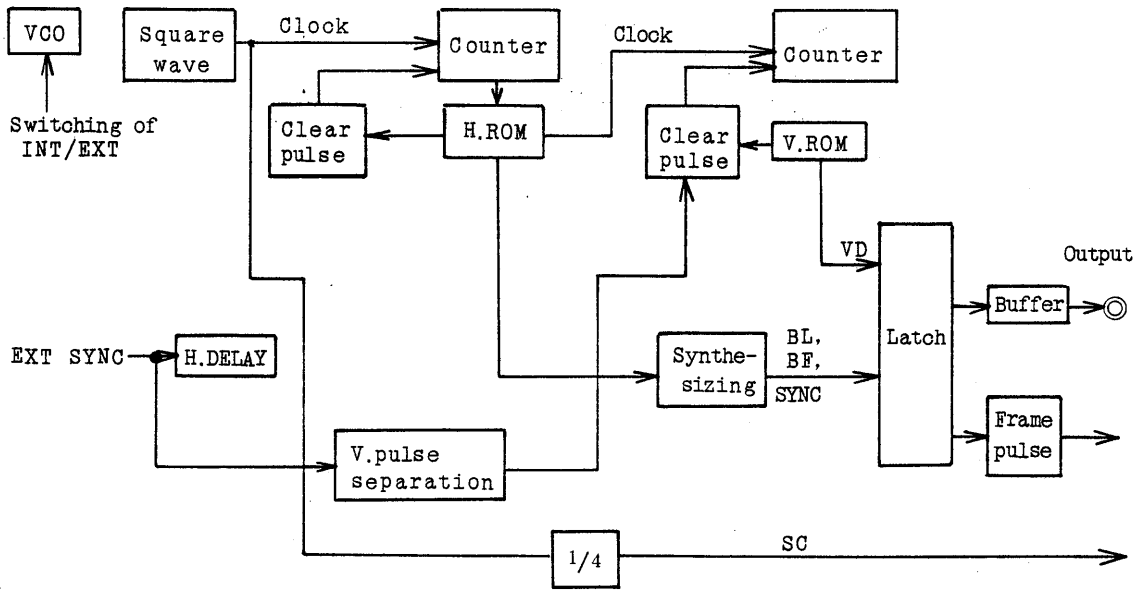
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The switch QA1 switches the control voltage of the VCO to either internal lock or external lock status. QA5A, B and C detect the existence of SYNC and BURST in the external signal, and also detect the signal from the INT/EXT SYNC switch on the front panel, deciding the switch position of QA1.

QA4A is used for lighting up the LED of the LOCK indicator. QA4B and QA4C light up the LED's for the REMOTE indication.

QA11D, QA18, QA20 and QA17 make up for the circuit that varies the phase of output signals of Model TG-7 upto more than ±300 nS. A clear pulse for the H period is produced at QA18A and QA18B, carrying out delay of the H.ROM. A clear pulse for the V period is produced at QA20A, QA20B and QA17B, carrying out delay of the V.ROM.

The switch QA6 selects either monochrome or color. It operates in response to the COLOR and B/W switch on the front panel.



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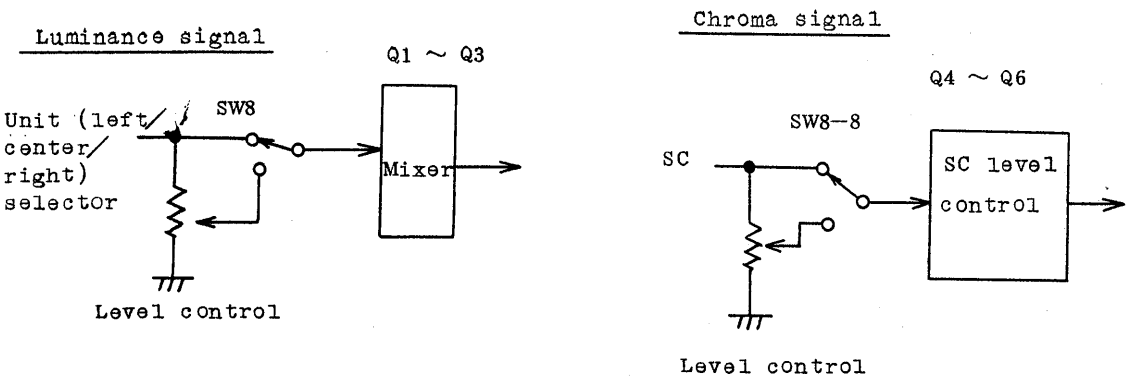
10-5 Unit signal level control circuit [A-6]

This circuit board controls the level of the chroma signal and the level of the luminance signal from the unit. The signals from the unit pass through SW8 and are applied to the Q1 through Q3 mixer. The level of the signals can be contrinuously varied by the three variable resistors: R3, R9 and R15.

At the STD position, the standard values are determined by the R1, R2, R7, R8, R13 and R14 fixed resistors and sent to [A-9]. Q4 through Q6 configure a subcarrier signal level control circuit which works in the same way as above.

The output signal is sent to [A-7] as the subcarrier signal of the modulator. Q7 is the color black-and-white selector circuit and the subcarrier signal to [A-7] is turned on and off by SW7. SW6 is the unit signal selector switch. J21 through J23 are connectors that hook up the main frame with the unit. J6 is a connector for remote control.

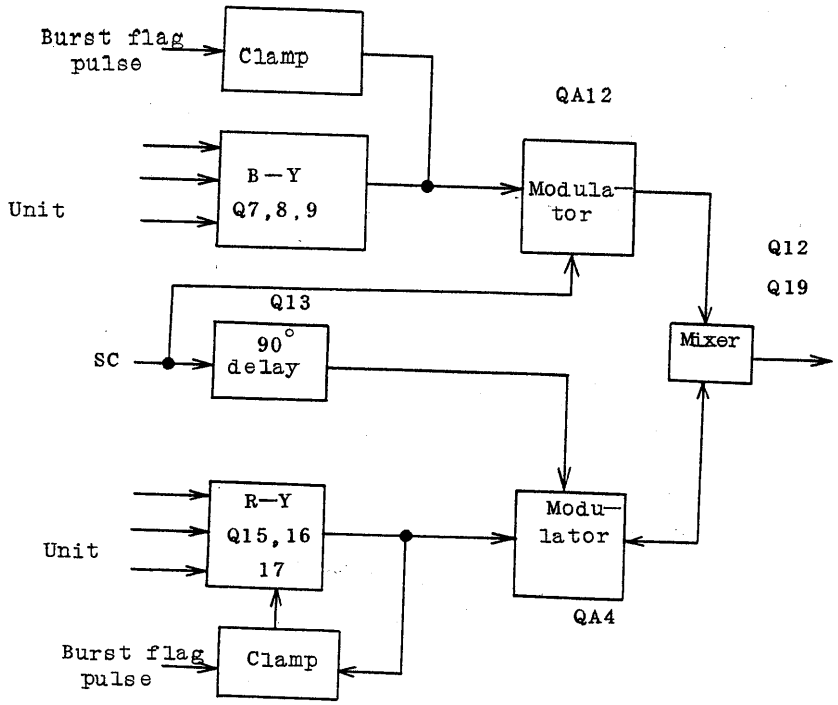
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10-6 Chroma signal modulator circuit A-7

The subcarrier signal is modulated by the B-Y and R-Y signals supplied from the unit and the chroma signal is formed. Q7, Q8, Q9 and QA1A/B form the B-Y signal buffer circuit, the signals from the unit are mixed, the color burst period is clamped to 0V (DC) and the signal is sent to the QA7 modulation signal input. The output is taken out from Q12 and sent to A-9 . Q13 delays the subcarrier signal by 90^{o} and it is supplied as the QA4 modulator's carrier signal. Q15, Q16, Q17 and QA3A/B make up the R-Y signal buffer which works in the same way as above. Its output is obtained from Q19 and sent to A-9 .

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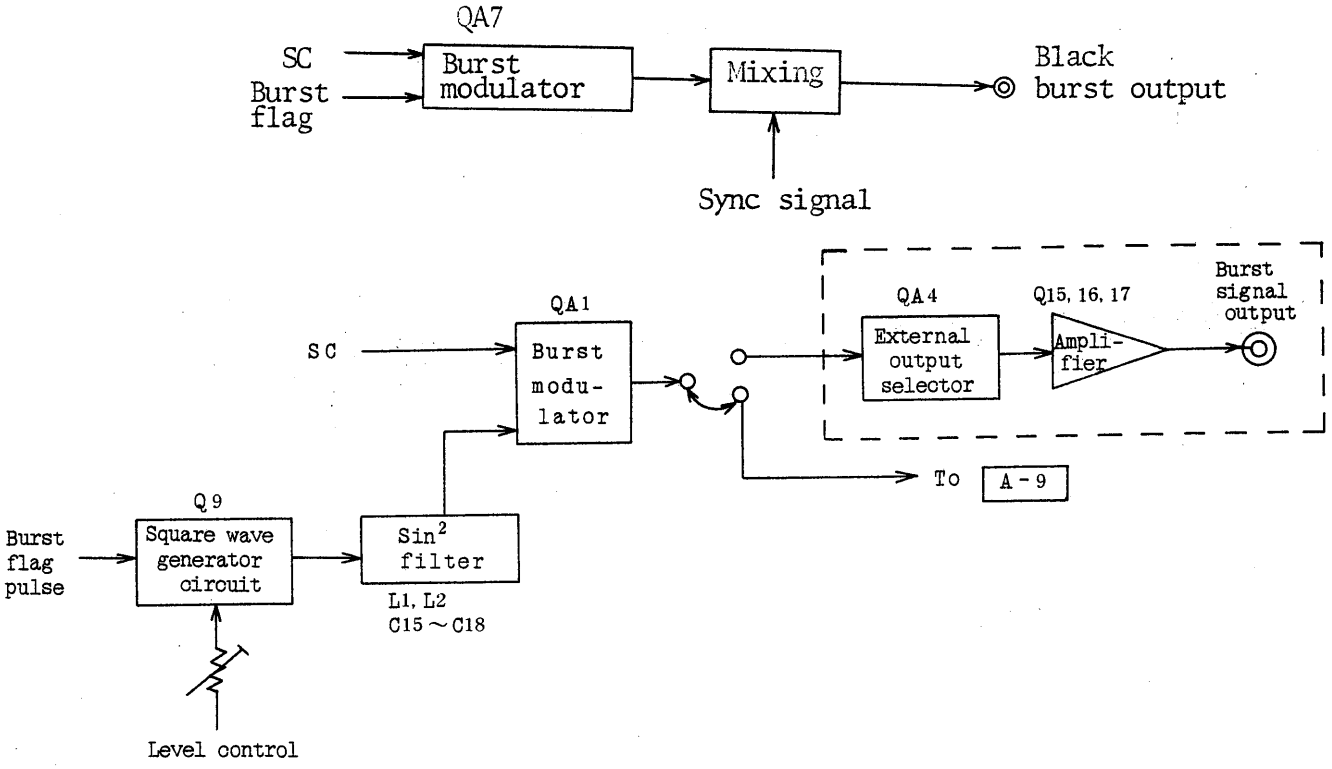


10-7 Color burst signal modulator circuit A-8

This circuit board produces the color burst signal. QA3, Q9 and Q11 form the modulation signal square wave generator circuit and the level of the square waves is controlled by 1R43 and R44. L1, L2, and C15 through C18 compose a $\sin^2$ filter which determines the rise time. QA1 is a burst signal modulator whose output is sent to A-9 via Q7 through QA4. QA4, Q15 through Q17 make up an external output circuit (option) and the color burst signal alone is provided at the output connector. Selection is performed by QA4.

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Both subcarrier signal and burst flag pulse supplied from the PC board A-3 are input to the modulator QA7, where from the PC board A-9 SYNC signal waveform is added. In this way black burst signal will be output.



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10-8 Output amplification circuit [A-9]

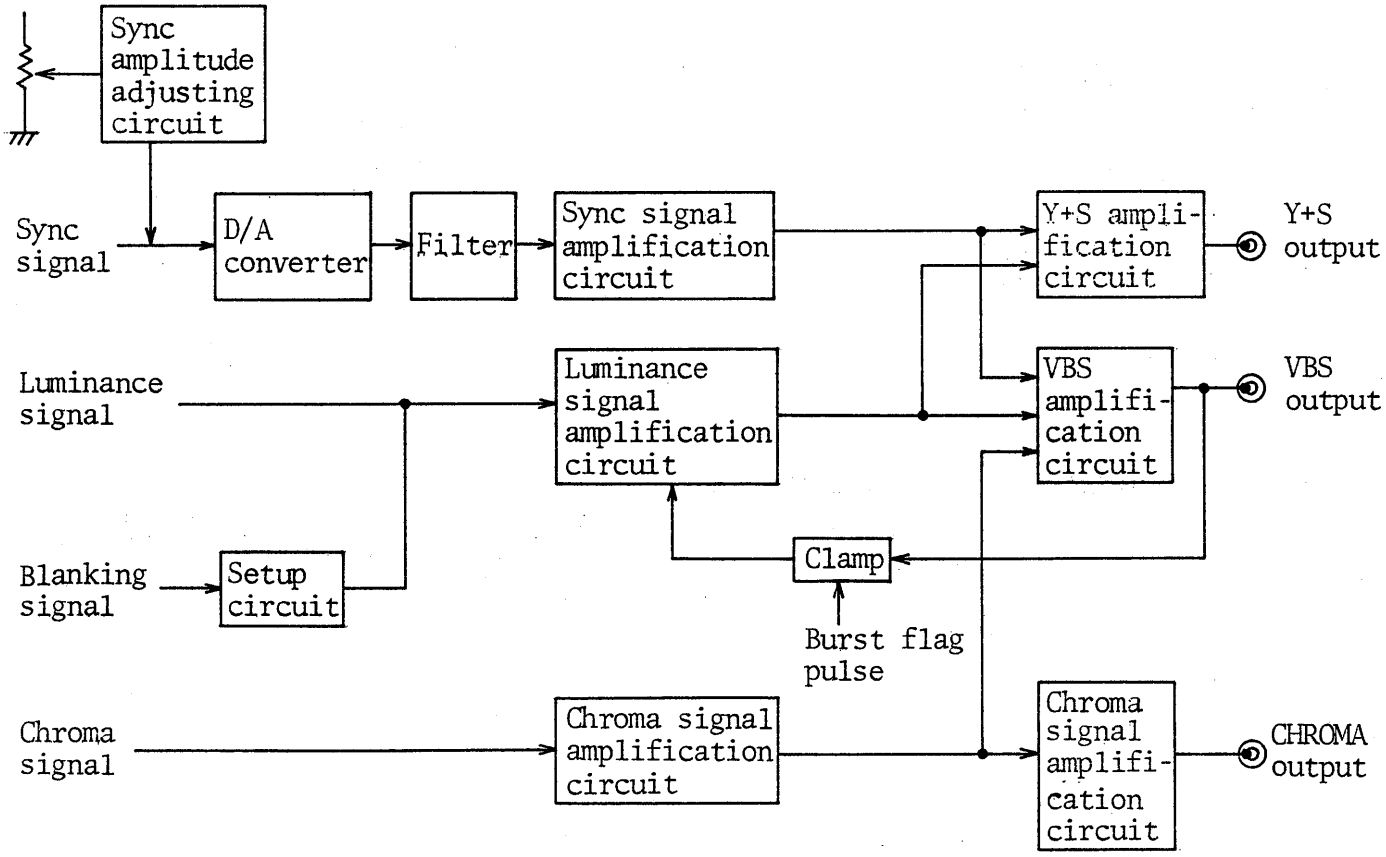
Sync pulse which is input to QA1 is D/A-converted by Q26, and it is shaped by the filters (C1, C2 and L1), then it is input to QA2. QA3 is the amplitude adjusting circuit, where amplitude of the sync signal is variable by IR9 or R6.

Q2 and Q3 form a sync signal amplifier. One of outputs from this amplifier passes through the buffer (Q4), where it is mixed with a luminance signal, producing the resultant Y+S output. The other output passes through the buffer (Q5), where it is mixed with luminance and chroma signals. The resultant mixed signal becomes a VBS output after having passed through the amplifiers, Q8 and Q9. The luminance signal input to the connector, A7, passes through the amplifiers, Q24 and Q23, from which a part of it goes to the buffer, Q15, where it becomes a Y+S output, while the remained part of the input luminance signal goes to the buffer, Q17, where it becomes a VBS output.

QA4 is the circuit to produce a setup signal by using a BL pulse. Output from QA4 passes through Q25, where it is mixed with a luminance signal.

Chroma signals are input to the connector, A11. Having passed through the subcarrier band-pass filters (L2 and L3) and the 2 fsc trap filters (C20, C21 and C22), one of the chroma signals is mixed with luminance and sync signals, becoming a VBS output. Another chroma signal passes through the buffer, Q20, and it becomes a chroma output after having passed through the amplifier consisting of Q12, 13 and 16.

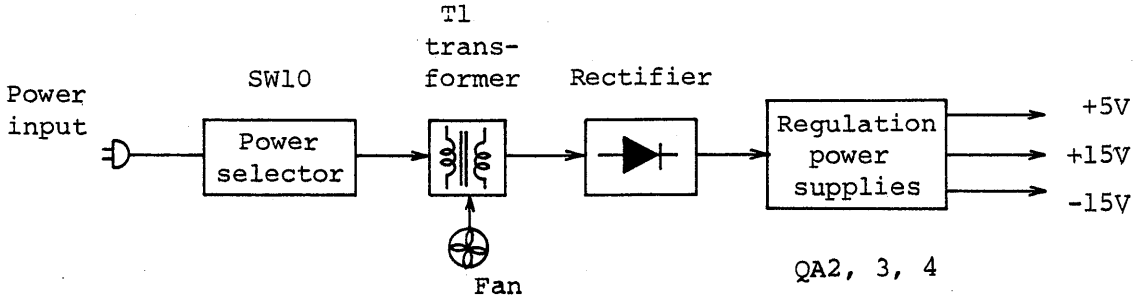
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10-9 Regulated power supply circuit A-10

This circuit board produces the DC power required by the signal generator. SW10 is used to select the T1 power transformer primary to the required input voltage. At the secondary are D1, 1D3, D5, 1D4 and 1D5 rectifiers which provide full-wave rectification.

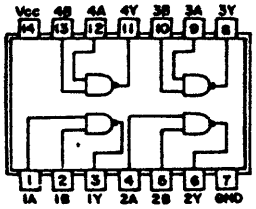
QA1, Q6, 1Q1 and QA2 compose the +15V power supply circuit, 1Q3, Q4 and QA3 the +5V power supply circuit and 1Q5, Q2 and QA4 the -15V power supply circuit. Regulation is provided by ICs.



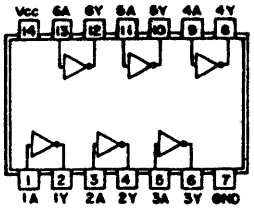
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11. LISTING OF ICs USED

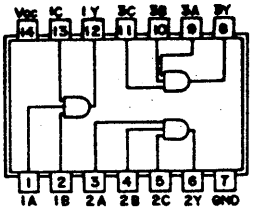
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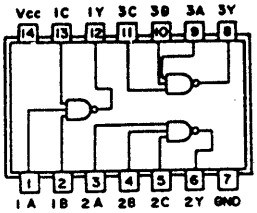
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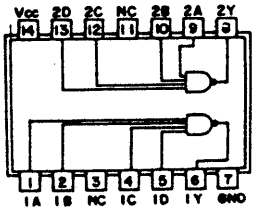
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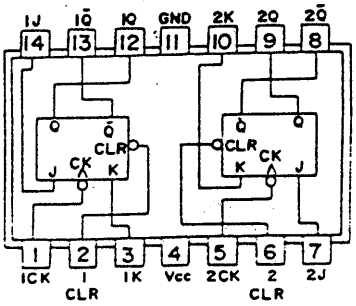
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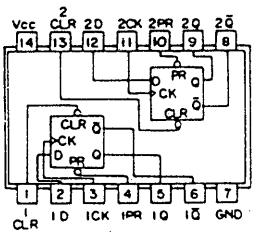
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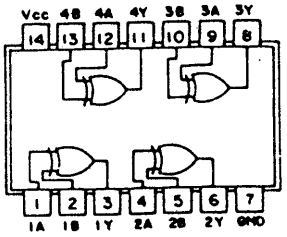
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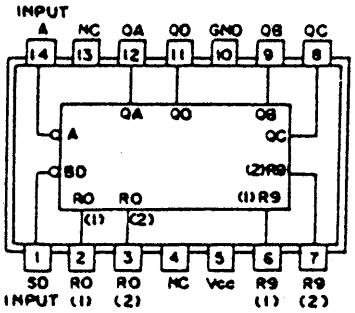


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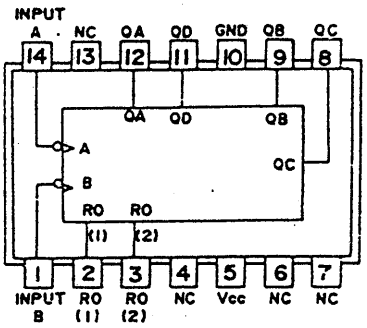


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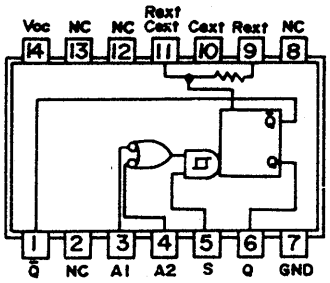
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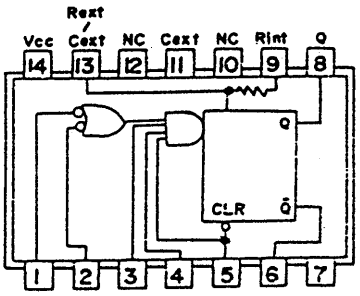
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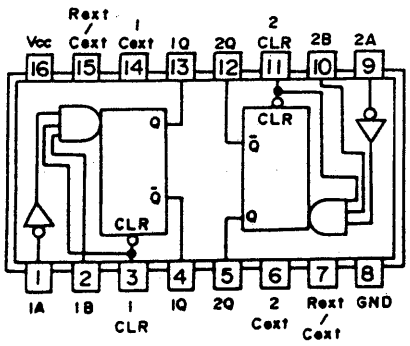
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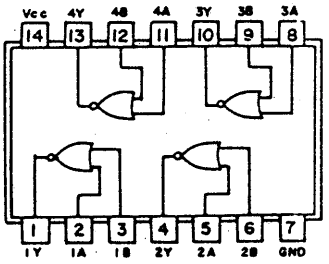
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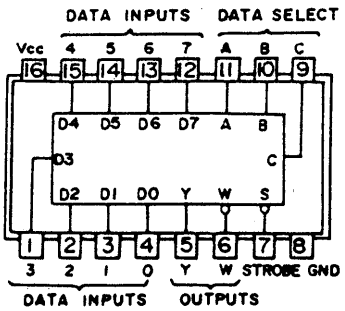
74123, 74LS123



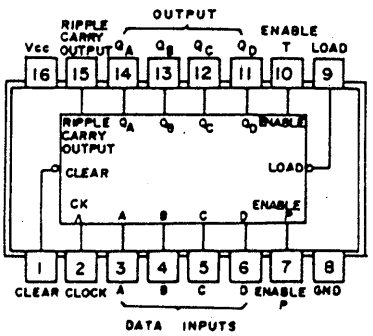
74128



74151A, 741LS151, 74S151

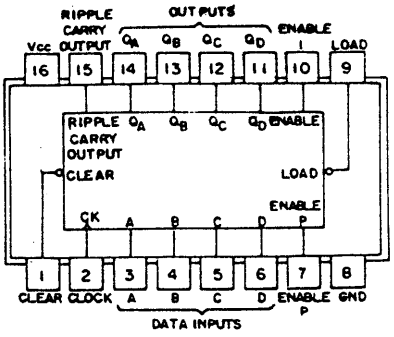


74161, 74LS161, 74LS161A

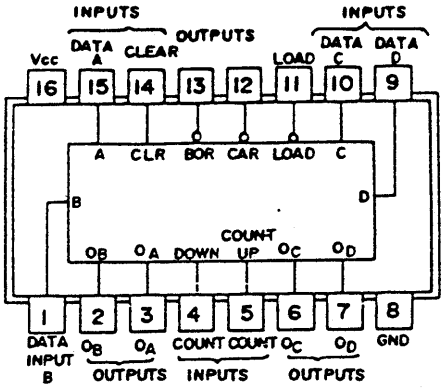


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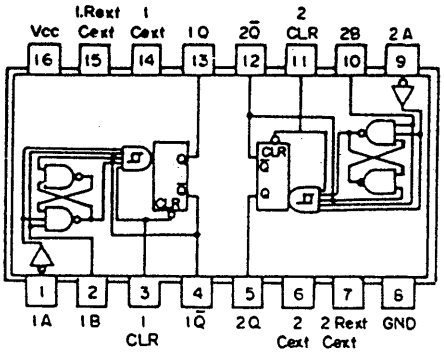
74163, 74LS163, 74LS163A



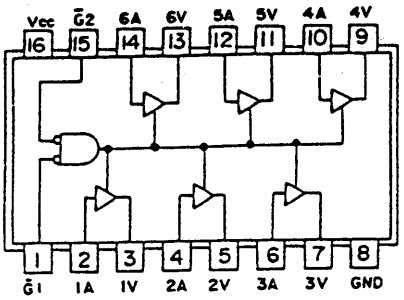
74193, 74LS193



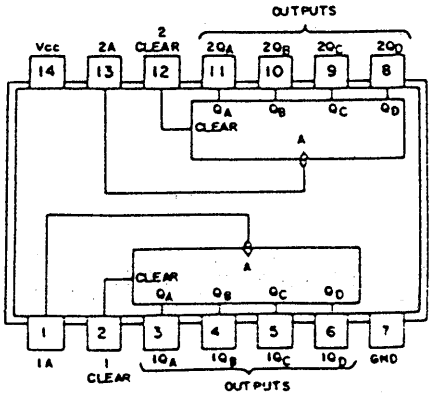
74221, 74LS221



74365A, 74LS365

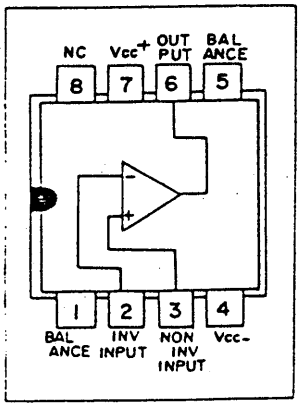


74393, 74LS393



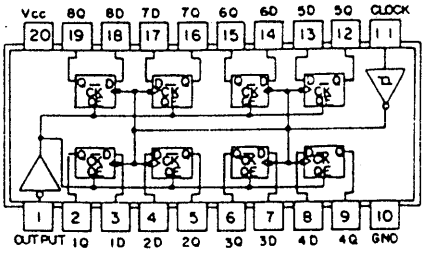
TL081C

JG OR P
DUAL - IN-LINE PACKAGE
(TOP VIEW)



NC - No internal connection

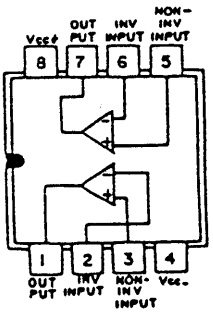
74LS374, 74S374



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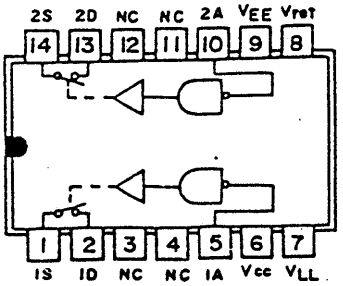
TL082

JG or P
DUAL-IN-LINE PACKAGE(TOP VIEW)



TL182C

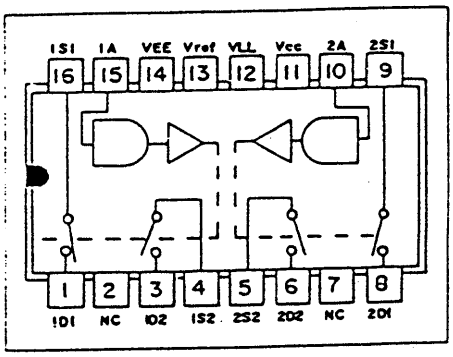
DUAL-IN-LINE PACKAGE(TOP VIEW)



NC-No internal connection
Switch positions shown are A inputs low.

TL191C

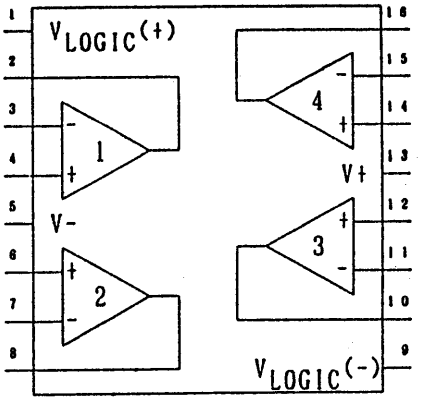
J or N
DUAL-IN-LINE PACKAGE(TOP VIEW)



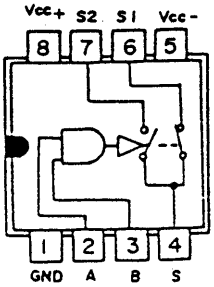
NC-No internal connection
Swich positions shown are for A inputs high.

HA-4905
QUAD COMPARATOR

Top View

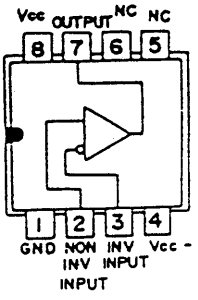


TL601

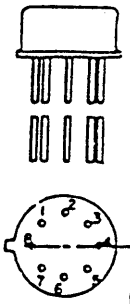


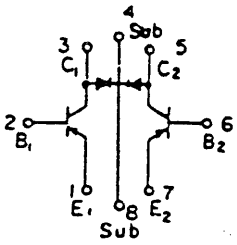
TL710

JG or P
DUAL-IN-LINE
PACKAGE (TOP VIEW)



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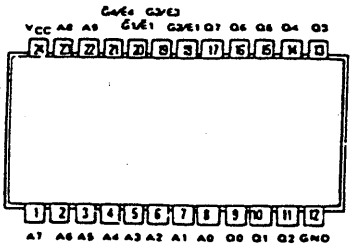




1. Emitter 1
2. Base 1
3. Collector 1
4. Sub (Case)
5. Collector 2
6. Base 2
7. Emitter 2
8. Sub (Case)

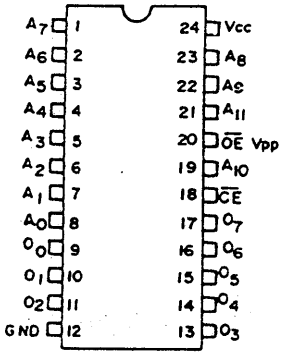
28S86 STANDARD

8K-BIT PROGRAMMABLE READ-ONLY MEMORIES
1K 8-BIT WORDS



M5L2732K

32K (4Kx8) UV ERASABLE PROM



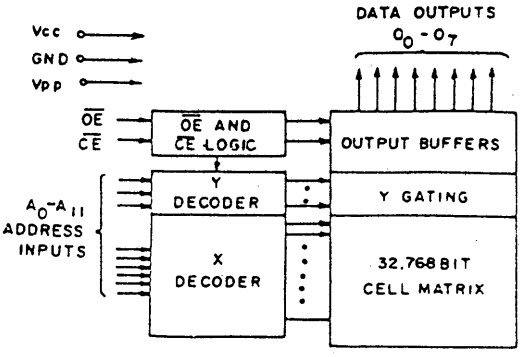
MODE SELECTION

MODE \ PINS	CE (18)	OEN pp (20)	Vcc (24)	OUTPUTS (9,11,13,17)
Read	V_{IL}	V_{IL}	+5	DOUT
Stanaby	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	Vpp	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	DOUT
Program Inhibit	V_{IH}	Vpp	$\overline{+5}$	High Z

PIN NAMES

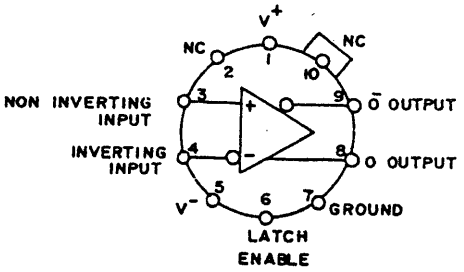
A_0-A_{11}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS

BLOCK DIAGRAM

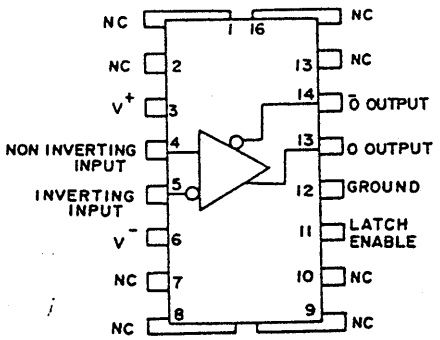


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Metal Can

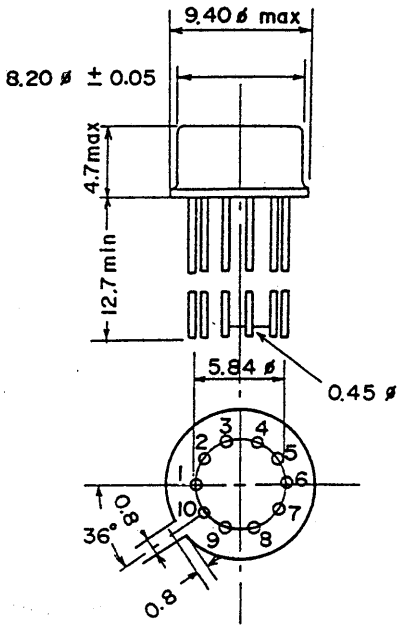


Duol-in-Line

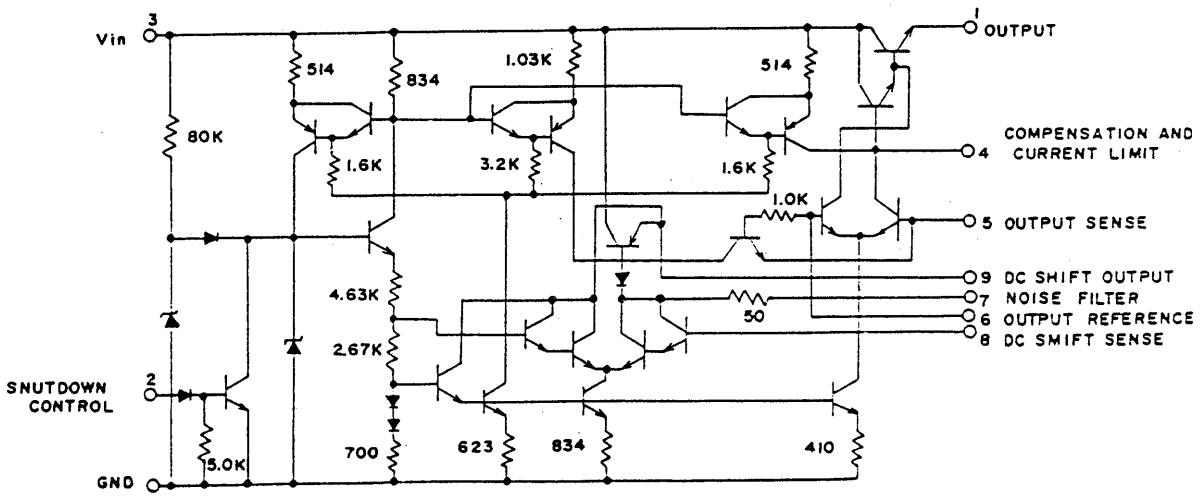


Note 1: On metal package, pin 5 is connected to case.
On Dip, pin 6 is connected to case.

MC 1469G
VOLTAGE REGULATOR



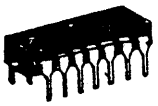
COMPLETE CIRCUIT SCHEMATIC



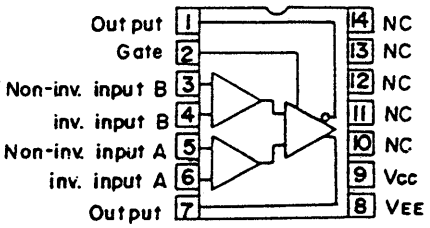
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MC 1445

MC 1596

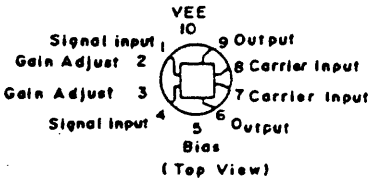


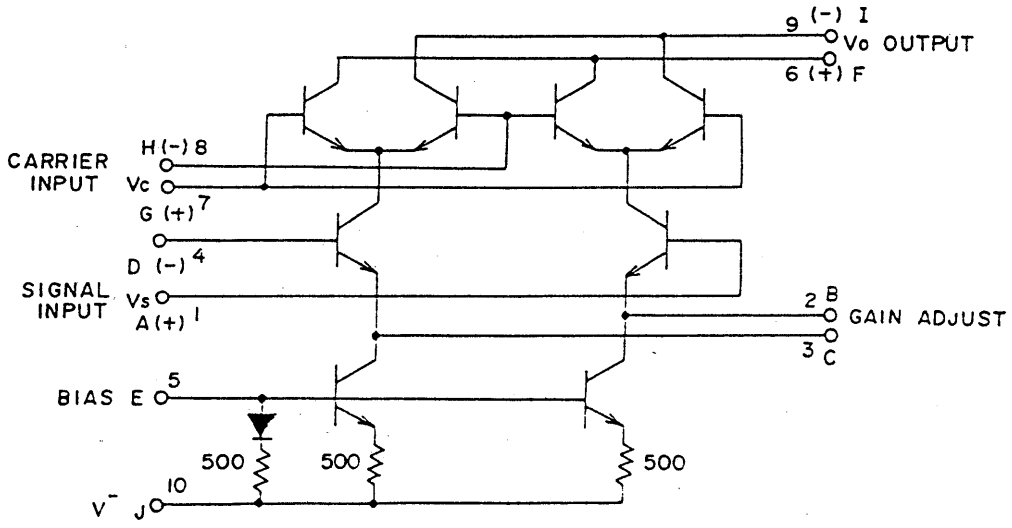
LSUFFIX
CERAMIC PACKAGE
CASE 632
TO - 116



BALANCED
MODULATOR-DEMODULATOR

G SUFFIX
METAL PACKAGE
CASE 603

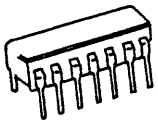




MC 1596

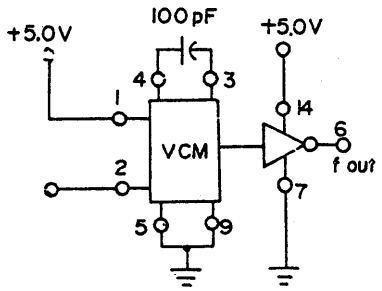
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MC 4024



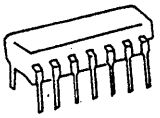
P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC4024 only)

FIGURE 3 - VOLTAGE-CONTROLLED MULTIVIBRATOR



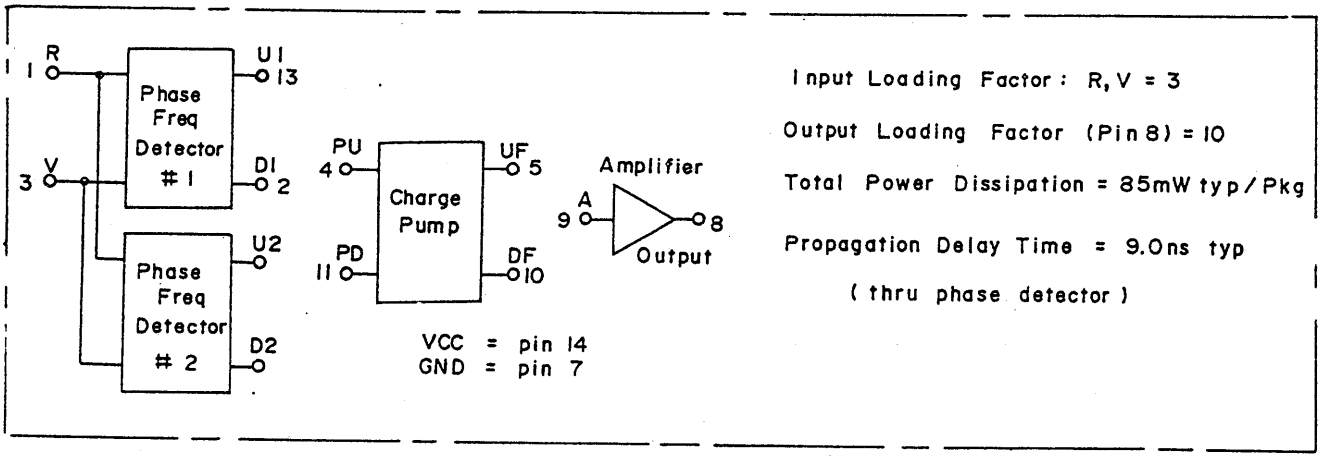
Vin = 2.5V to 5.5V
f out = 1.0MHz min, 5.0MHz max

MC 4044



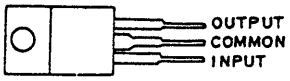
P SUFFIX
PLASTIC PACKAGE
CASE 646
MC4044 only

MC 4 0 4 4

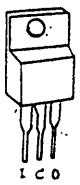


μA78M15C

KC PACKAGE
(TOP VIEW)

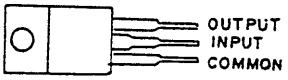


TO-220AB

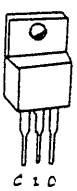


μA79M08C

KC PACKAGE
(TOP VIEW)



TO-220AB



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Conditions for waveform photographs

Set up the unit as shown in the figure below, plug in the U703/1 unit and set the signal to color burst.

(1) Make the external input signal the color burst signal.

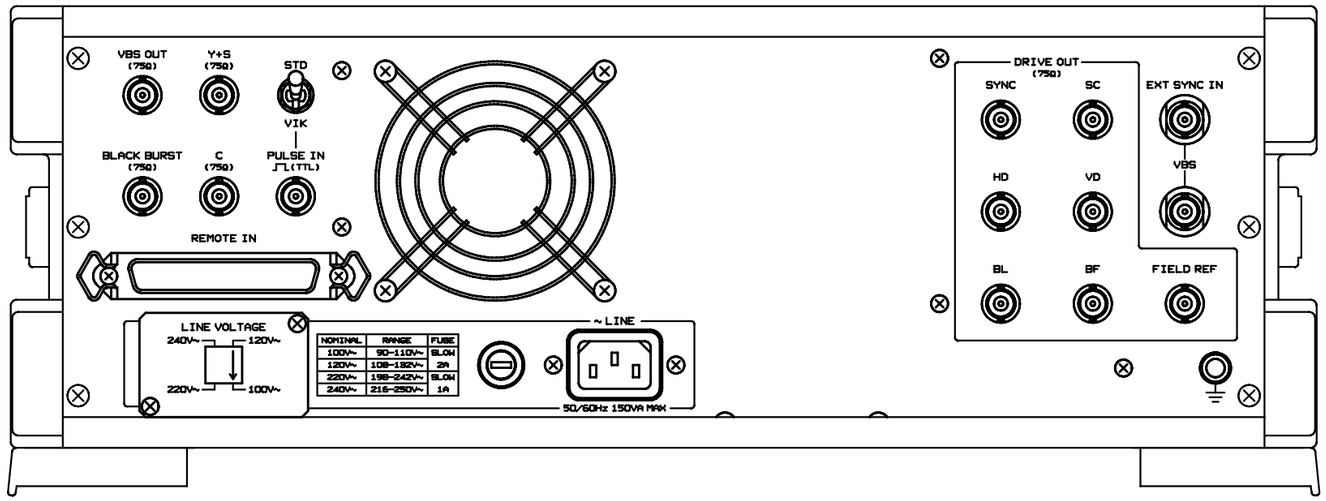
(2) Set the output signal to STD.

Other conditions are shown in the waveform photographs.

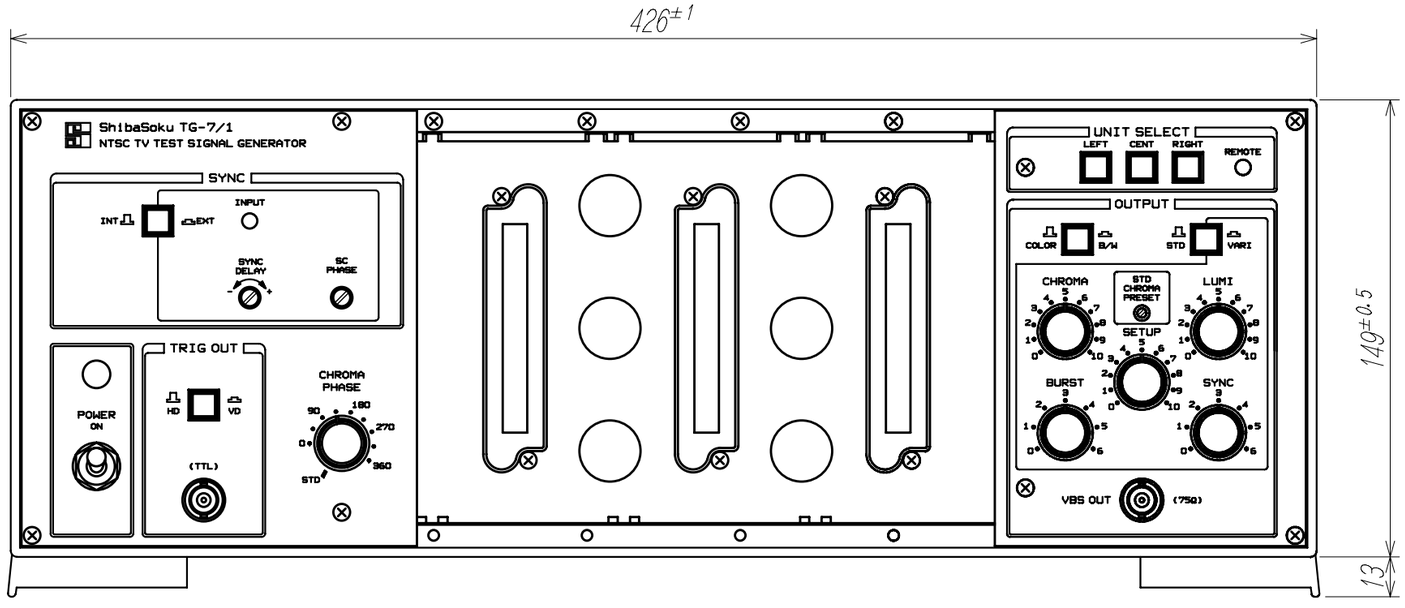
Note: The waveform photographs are in dual-trace form. The top waveform is the output signal waveform (BNC, 75 ohms) of the unit while the bottom waveform is that indicated by the probe.

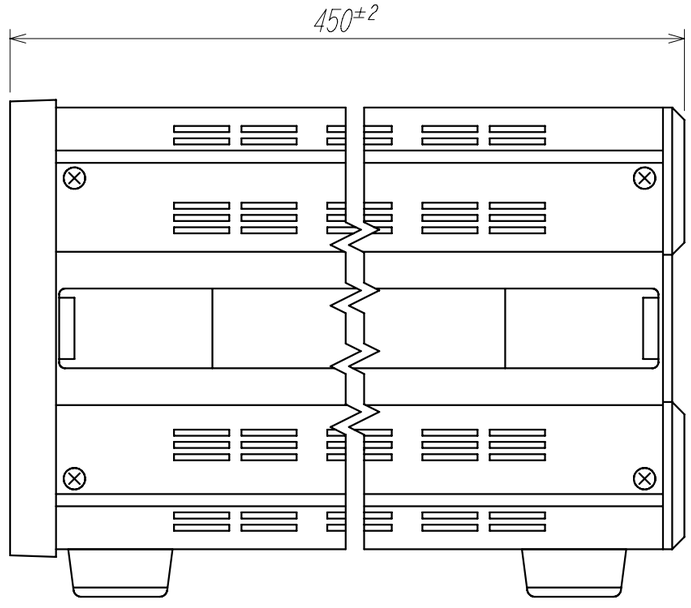
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REAR VIEW





TG-7/1
NTSC TV TEST SIGNAL GENERATOR

APPEARANCE

P3-M257128-2

PDM SYSTEM APPROVED ShibaSoku Co.,Ltd.

TG-7-1AP.DRW

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