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SIEMENS

SIMATIC S5

Digital Position Decoder IP 241 with FB 156/1 57 158

Equipment Manual

Release: 02

Order No.: 6ES5998–0KD21

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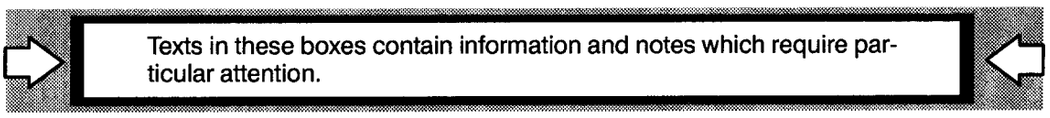
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For clarity's sake, this equipment manual does not cover every conceivable situation in complete detail.

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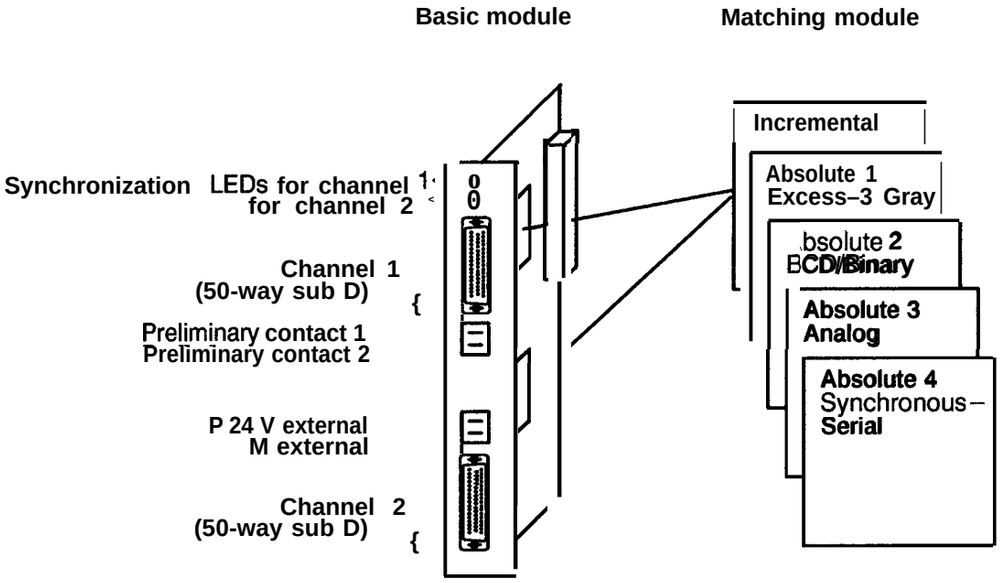
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1.1 Design of the IP 241



Synchronization LEDs – go off after synchronization of the respective channel

Channel 1 – for connection of an encoder (actual value)

Preliminary contacts (C.1/C.2) – for synchronization (reference point method) with incremental encoders per channel (e.g., BERO)

24 V external – voltage supply for encoder and matching modules

Channel 2 – for connection of an encoder (actual value)

For each channel used, an encoder matching module of your choice can be applied.

The connections preliminary contact 1/2 and P/M are intended for FASTON connectors (2,4 mm x 0.8 mm).

These inputs are designed as screw connections starting with MLFB 6ES5 241 –IAA12.

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1.2 Characteristics of the IP 241

– The IP 241 acquires position–based signals.

– The IP 241 provides two independent channels for one each position decoder with a maximum of 16 tracks. Single channel operation, however, with 32 tracks can also be selected.

– Incremental or absolute encoders can be connected via encoder matching modules (the supply voltage for these encoders can also be provided by the IP 241).

– Actual values can be read at any time with an S5 command.

– A cam–operated master controller is electronically imitated in the IP 241. This means that the actual values are continuously compared with the initial and the end track setpoints and the corresponding track identifier bits are set.

– The IP 241 transfers these track identifier bits to the programmable controller (e.g., via a standard function block).

– The track identifier bits are furnished in a way that allows them to be directly scanned and linked in the control program (e.g., by an end switch).

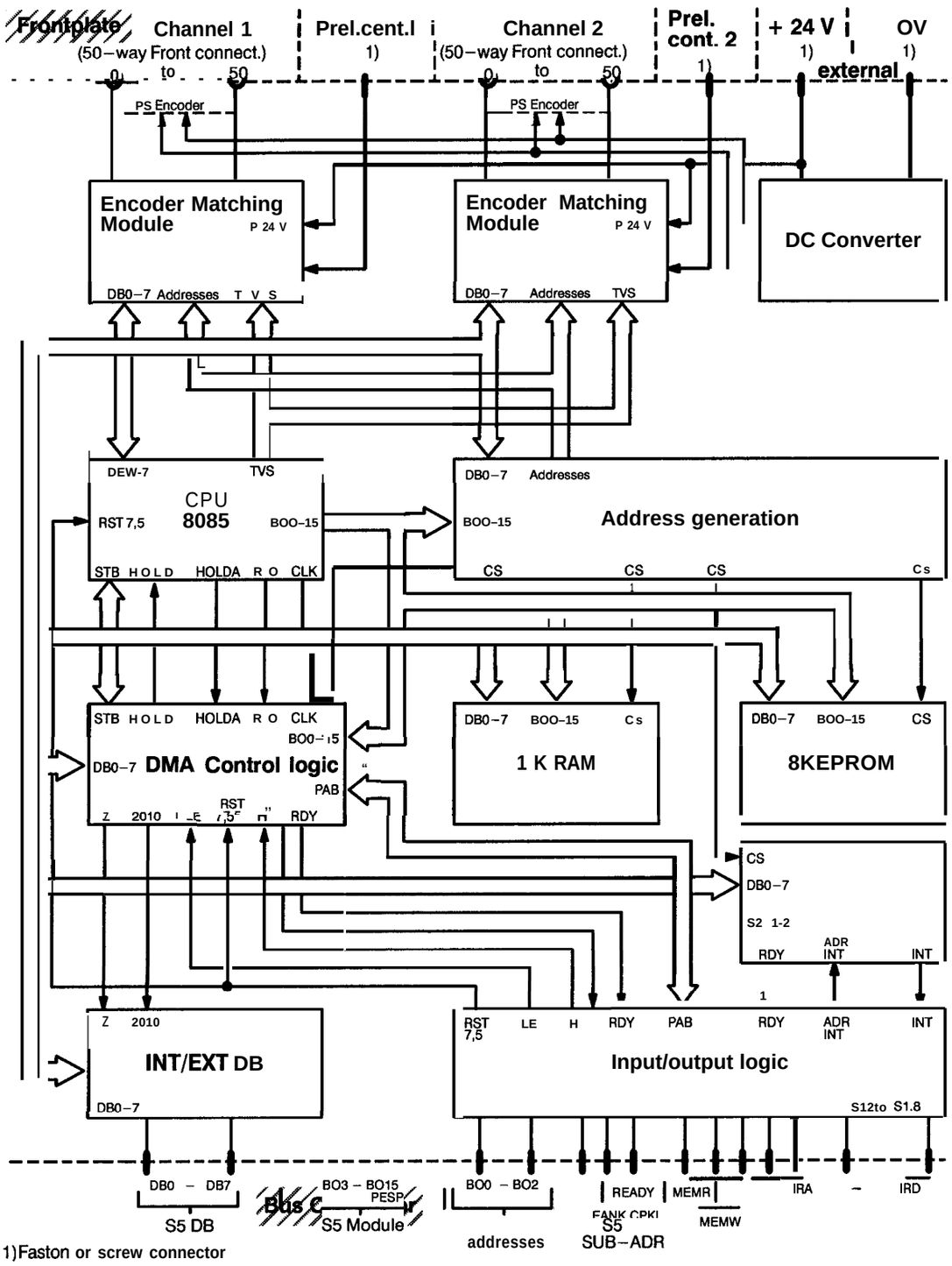
– Hardware or software synchronization is available for incremental encoders.

– Each channel can be used for linear axis operation or for rotary axis operation.

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1.3 Block Diagram: Basic Module IP 241

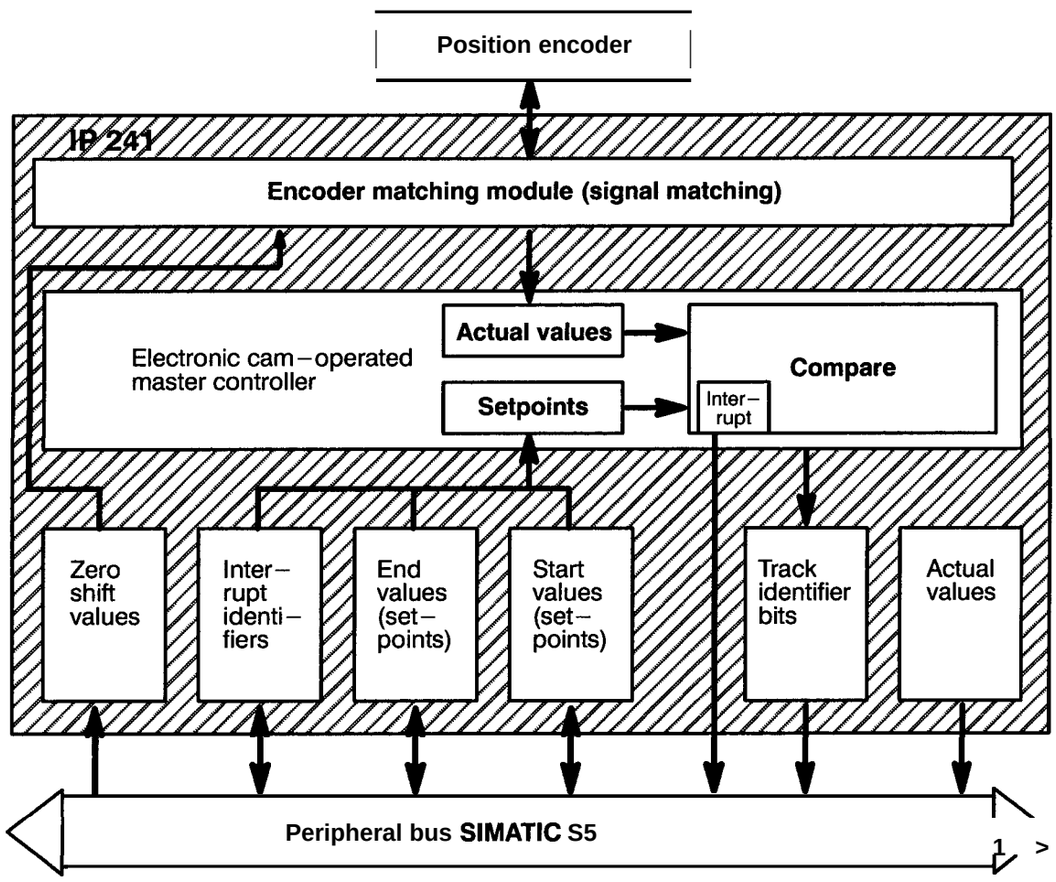


1) Faston or screw connector

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1.4 Structure of a Channel

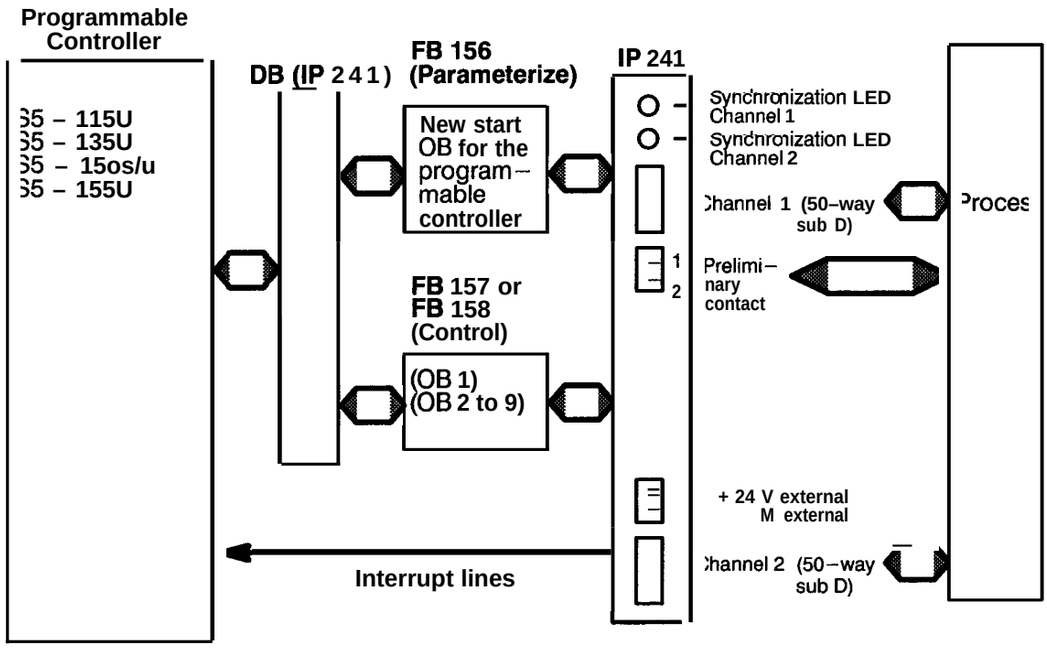


- The position encoder signals are converted to TTL level by the encoder matching module and are transferred as actual values to the basic module.
- The setpoints (i.e., the initial and end values of the cams for each required track) are stored in a data block (IP 241) of the user program.
- The standard function block FB 156 transfers these values to the IP 241.
- Interrupt identifiers for the initial and end values of each track can be specified.
- Interrupt identifiers for zero shift values can be selected separately for channel 1 and channel 2.
- The IP 241 compares the actual values with the setpoints and sets the corresponding track identifier bits.
- The track identifier bits and the interrupts can be read in for processing in the programmable controller (e.g., via the standard function block FB 157).

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1.5 Communication between IP 241 Digital Position Decoder and Programmable Controller



The IP 241 communicates with the programmable controller via two standard function blocks. Furthermore, controller–specific interrupts can be transferred to the programmable controller via interrupt lines or group interrupts (byte O).

The function block accesses a data block. With this data block and with the standard function blocks the user can

– Parametrize
– Control and
– Monitor the IP 241.

The DB (IP 241) contains all parameters (e.g., cam setpoints, interrupts).

The data block number can be selected by the user; the data sequence in the DB (IP 241) must then be strictly adhered to!

The standard FB 156 (parameterize) is called in the new start OBS of the programmable controller. It supplies the IP 241 with the data specified in the DB (IP 241).

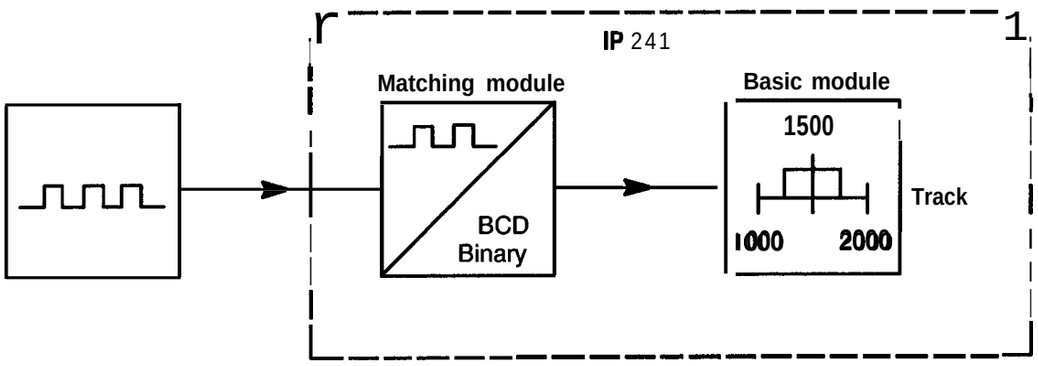
FB 157 (control) is called in the cyclic program and/or in the interrupt–controlled program. The commands given there serve for controlling or scanning the IP 241.

FB 158 (control–indirect parameterization) is also called during the cyclic and/or interrupt–controlled program. In contrast to FB 157, the parameters are transferred indirectly via the working data block.

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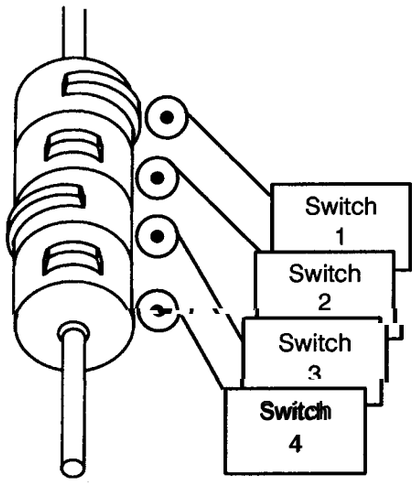
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1.6 General Operating Principle of the IP 241



Electromechanical cam control system

IP 241 = electronic cam–operated controller

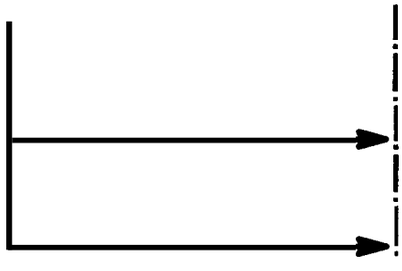


With the IP 241, each switch corresponds to a track.

A maximum of 16 tracks per channel is possible.

If "single channel" operation is selected, maximum of 32 tracks is possible (operation with parallel connection)

Each cam corresponds to an electronic cam on the IP 241; its position is defined by specifying the respective initial value A and the end value E.



Linear axis operating mode (see section 1 .7)

Rotary axis operating mode (see section 1.8)

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For each desired reaction, a cam can be setup on a track.

The size and position of this cam can be specified by writing the respective initial setpoint A and the end setpoint E of the cam into a data block (IP 241).

By means of the standard function block FB 156, this data block is then transferred to the IP 241 and the module is parameterized.

During parameterization, the IP 241 firmware internally arranges the specified initial and end setpoints into an ascending sequence of values.

This is done to obtain brief processing times when these values are processed (i.e., when the actual values from the encoder are compared with the setpoints).

Then the actual value only needs to be compared internally with the next highest and next lowest setpoints and not with all specified values.

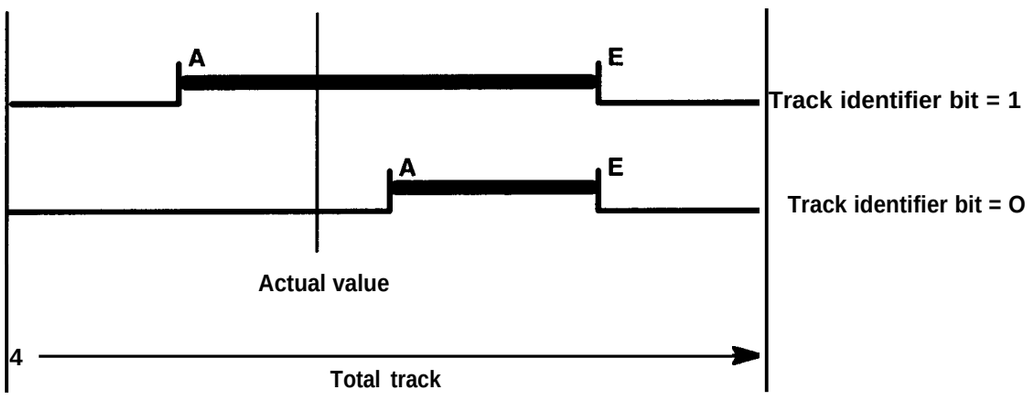
The sorting of these values requires specific running times which are listed in the section "Time Requirements" of the technical specifications (section 8.3). The time requirements must be considered during configuring.

Track Identifier Bits

The result of the comparison with the setpoints (cams) is presented as track identifier bit.

Within the cam, the track identifier bit is "O", outside the cam it is"1".

Example:



The effects of the track identifier bits can be influenced. See next page

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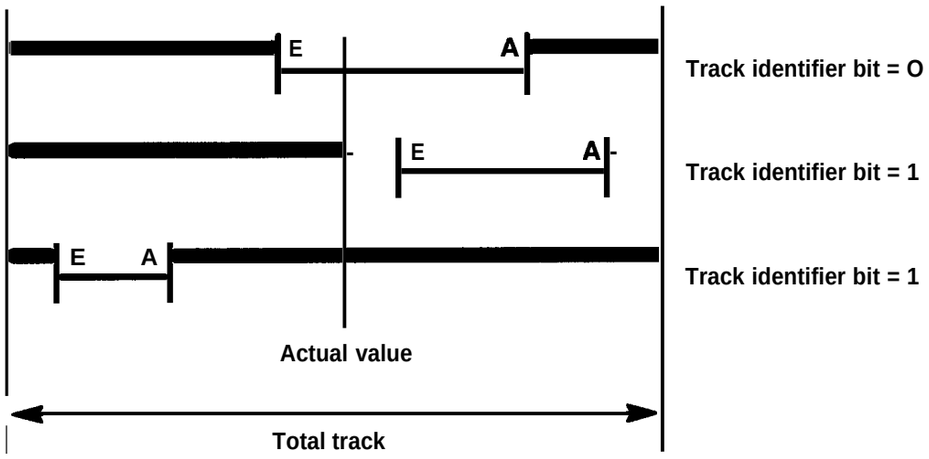
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If the selected end value is higher than the initial value, the track identifier bit is set within the cam (= 1).

If, however, the selected initial value is higher than the end value, the track identifier bit within the cam is reset (= O).

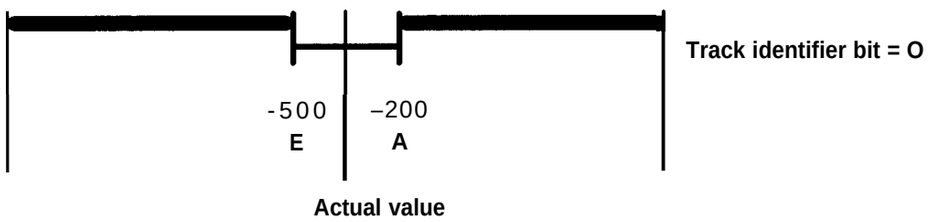
Outside the cam the applicable track identifier bit is set (= 1).

Example:



When encoders allow a negative traversing range, the sign must be considered!

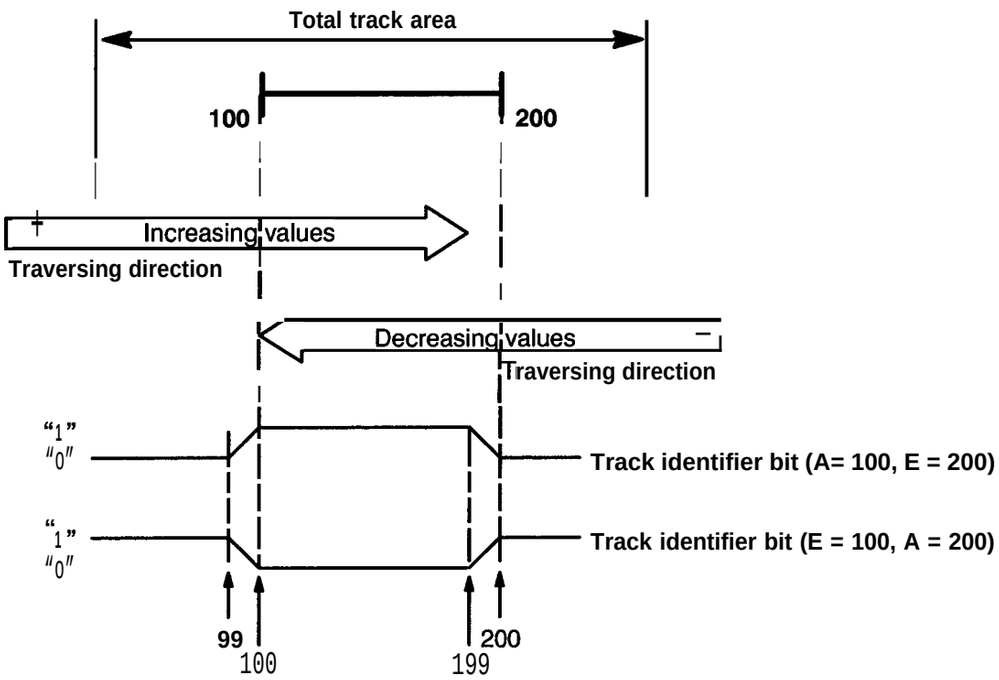
Example: –200 initial value and –500 end value
The track identifier bit is inverted (i.e., within the cam = O)!



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Note 1 (for positive values):



Aside from the traversing direction the following applies:

When the first cam value in traversing direction is reached, the track identifier bit is set (or reset respectively).

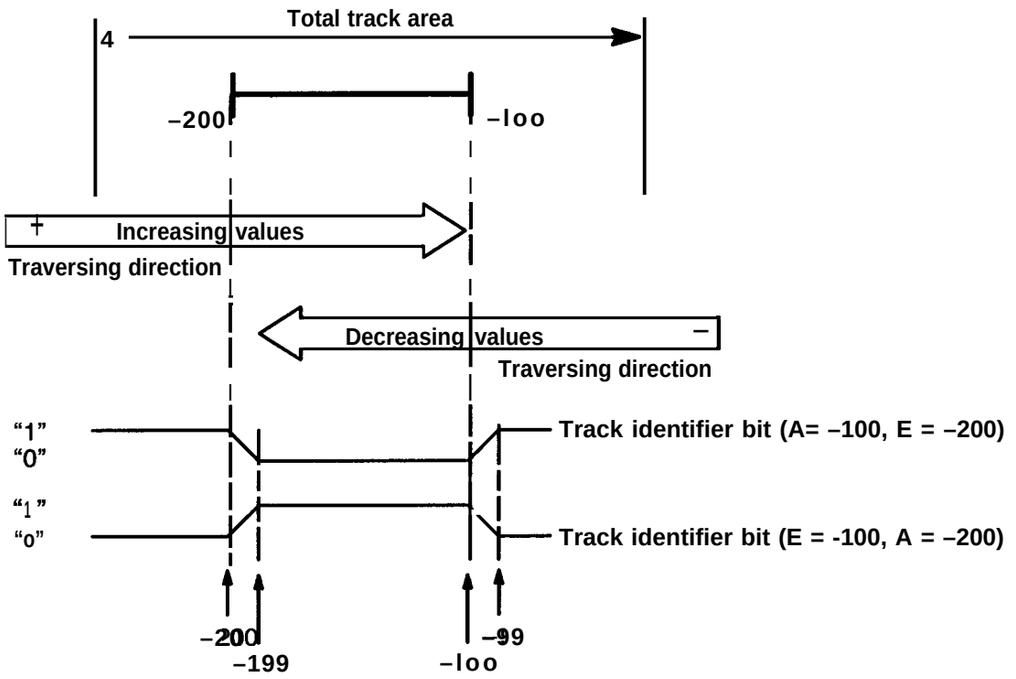
When the cam end is reached in the same direction, the track identifier bit by then is already reset (or set respectively).

If the cam outputs an active−high (or active−low) signal for the exact number of positions, the end value (or the initial value respectively) must be increased by one.

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Note 2 (for negative values):



Aside from the traversing direction the following applies:

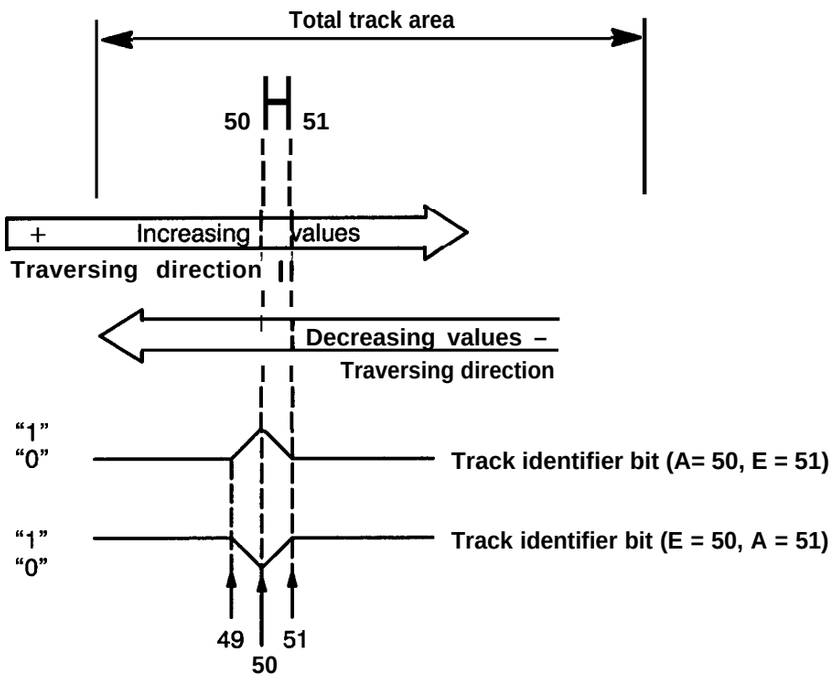
When the position “setpoint + 1“ is reached, the track identifier bit is reset (or set respectively).

If the cam shall output an active–high (or –low) signal for the exact number of positions, the above offset must be considered and the difference between the initial and the end setpoint must be increased by one.

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Note 3 (for positive values):



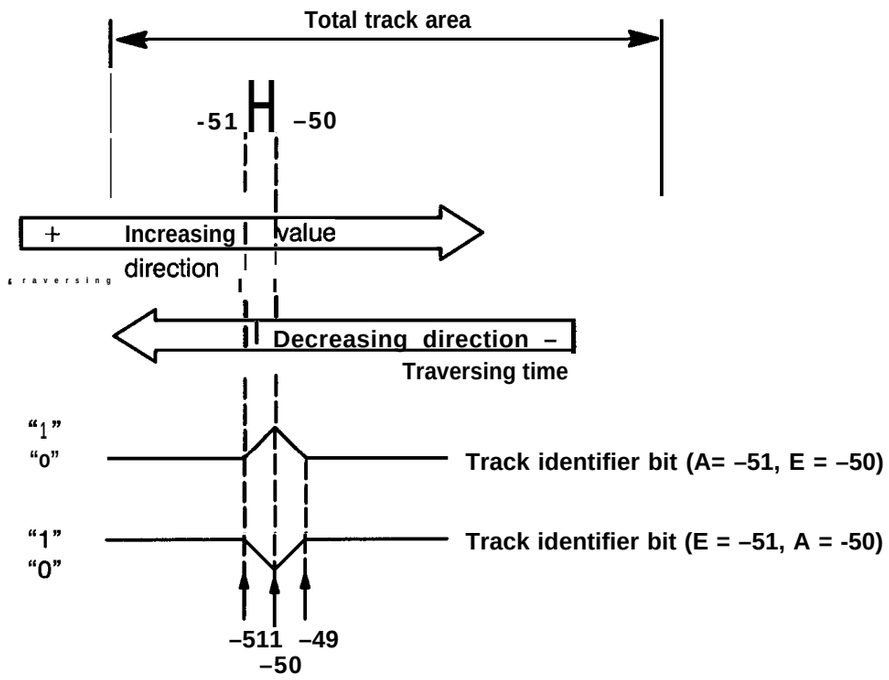
Aside from the traversing direction, in this case the track identifier bit is available as an edge.

This means that an evaluation in the S5 can only be effected by enabling an interrupt for this track.

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Note 4 (for negative values):



Aside from the traversing direction, in this case the track identifier bit is available as an edge.

This means that an evaluation in the S5 can only be effected by enabling an interrupt for this track.

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Note 5:

It is possible to define a cam, the initial value of which is very close to the end values.

It is generally best to adjust the width of the cam to the traversing speed. It must still be possible to read the respective track identifier during normal evaluation in the S5 cycle.

For quick reaction, use interrupts for these cams!

It must be observed, however, that the reaction at the interrupt can first be processed at the next breakpoint in the S5 program.

Depending on the operation mode of the individual programmable controllers, this occurs after the command "AF" or at block limits. For details, see the equipment manual of the programmable controller used.

Note 6:

To influence the effect of the track identifier bit for a cam with an initial value equivalent to the end value (A = E), these values must be transferred to the IP 241 module sequentially.

Example 1:

First input the initial value, then the end value
→ The track identifier bit is constantly 1, and then changes to O briefly when the setpoint is reached.

Example 2:

First input the end value, then the initial value
→ The track identifier bit is constantly O, and then changes to 1 briefly when the setpoint is reached.

This function cannot be effected with the standard function blocks.

After parameter assignment with FB 156 or modification of setpoints with FB 157 (AE), the status is always in accordance with example 1!

Usually when traversing with the system, such a cam is only recognized at extreme creep speeds.

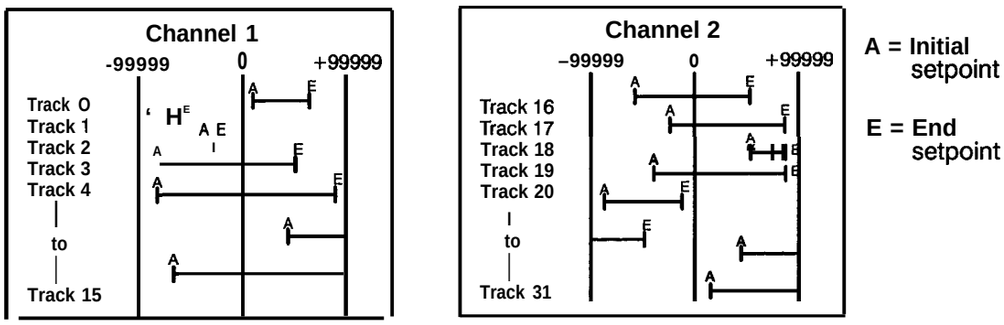
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1.7 Linear Axis Operating Mode

1.7.1 Function

The linear axis operating mode is the basic setting for the IP 241 at the initial start-up, after a power failure, and after software reset.



Encoder	Maximum track area (represented area)
Incremental encoder	- 99999 to +99999
Absolute 1–encoder with Excess–3 Gray code	o to +99999
Absolute 2–encoder with BCD code	0 to +99999
Absolute 2–encoder with binary code	0 to +99999 or O to FFFFF (see section 5.1)
Absolute 3–encoder analog	— 1023 to +1023
Absolute 4–encoder synchronous–serial	0 to +99999 or O to FFFFF (see section 7.3.1)

The operating mode “linear axis” is always used when one or two axes are available per module where, within the maximum track area, positions are decoded or simple positioning operations are performed (drives with fixed rotation speed).

On the next pages two typical examples are shown.

When the area limits are exceeded with incremental and absolute encoders, then in the event of linear axes the track identifier bits for all tracks and any parameterized interrupts are set briefly, and the next actual value displayed is zero!

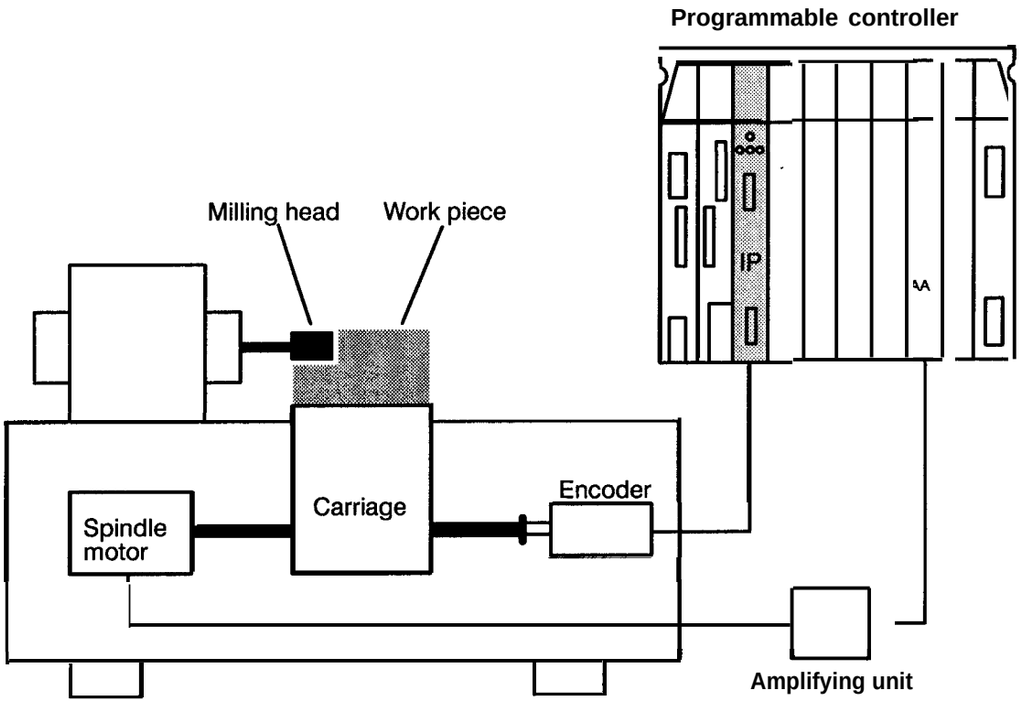
This effect can be avoided as follows:

- Prevent the system from exceeding the limits or
- Use the rotary axis mode (see section 1.8)

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Example 1



Example 1: Automatic Milling Operation with IP 241

Via the encoder, flange attached to the shaft, the IP 241 receives the "actual position" of the carriage and thus accordingly the work piece position.

The end positions of the milling head (respective work piece dimensions) are specified as setpoints.

Via a cam, positioned immediately in front of the work piece edge, a coolant pump can be activated.

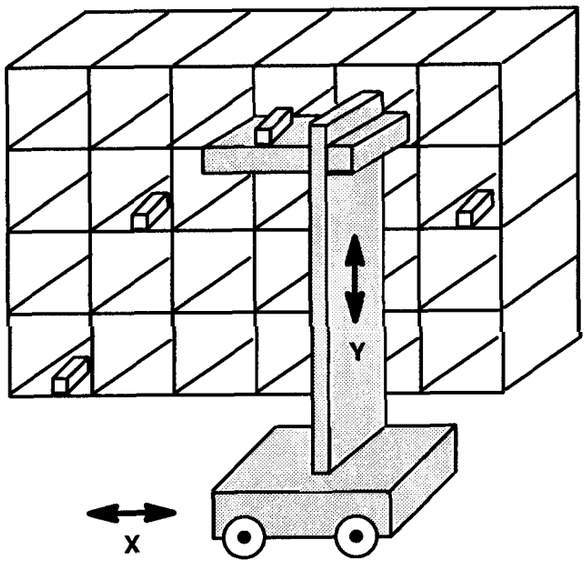
When the end position is reached, a quick and precise cutoff of the spindle motor can be effected via an interrupt to the programmable controller.

For simplification, example 1 is limited to one axis.

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Example 2:



Example 2: Simple Positioning in a High Shelf Storage System

In this case the actual positions are transferred to the IP 241 via absolute value encoders as otherwise long distances would have to be covered by "reference point traversing" in the event of a voltage cut off.

In example 2, the two IP 241 channels are used for acquisition of the individual coordinates (positions).

When the work piece reaches its designated coordinates (i.e., the cams), the respective motor is stopped by the programmable controller.

1.7.2 Conditions

The linear axis function can be transferred to the module in one of the three following ways:

1.) After each power on, this function is automatically selected; the same is applicable after each voltage cut off (no buffering on the 1P).

2.) After parameter assignment by means of the standard function block FB 156, the software reset in this block presets each channel to linear axis. Consider allocation of the data block (IP 241)!

3.) A software reset during operation without the standard function block also causes a linear axis presetting for both channels.
This means that in the relative byte 4 of the module, the settings must be: read bit = "1", actual bit = "1", and end bit = "1" (see section 9.6).

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1.8 Rotary Axis Operating Mode

1.8.1 Function

The rotary axis function can be selected separately for each channel, starting with version:

A14 (firmware release R08) for basic module 6ES5 241 –IAA11 or
AO1 (firmware release R09) for basic module 6ES5 241 – 1AA12

When you are operating in the "connection to parallel" mode and the rotary axis function is required, you must select the function for **both** channels!

- **Specify the desired function in the data block (IP 241) forparameterization via standard function block FB 156 in accordance with the programming instructions.**

- **In case of direct parameterization (without the standard function block) the following applies: Load the constant assigned to the function (see table below) in KM or KH format into the start–up 06s (OB20 to OB22). Transfer the constant to the set module address +4 as shown in section 9.6. SP bit scan.**

Function	KH	KM
Rotary axis channel 1 only	F4	11110100
Rotary axis channel 2 only	F5	11110101
Rotary axis channels 1 and 2	E7	11100111

In practical application the rotary axis function is always used, where exceeding the area end value starts a new traversing path at the same time.

This applies to rotary axes, rotary plates, or continuous conveyors.

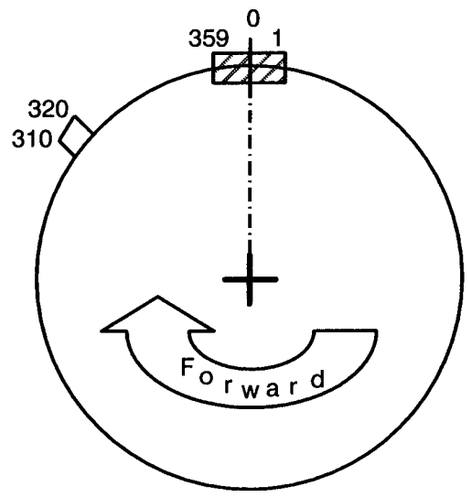
With the rotary axis function, exceeding an area end value by one increment toward O is regarded as a forward movement of one increment by the position encoder. Therefore, no brief and incorrect misleading of the track identifier bit takes place as with the linear axis.

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Use only cyclic movement in one direction in rotary axis mode!

The example shows the most frequently used rotary axis with the end value 359 and a cam from 310 to 320:



The hatched area may not have an initial value and/or an end value (see also section 1.8.2).

This area depends on the processing time per channel.

When the maximum traversing speed is maintained, this area is +/– one position.

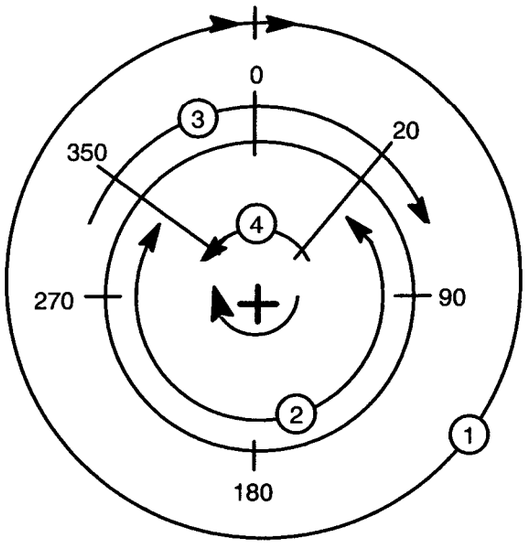
Guide values:
- **With single channel operation the maximum is 1000 pulses per second. ***
- **With two-channel operation the maximum is 500 pulses per second. ***

*** With incremental encoders and two-time evaluation these values are halved.**
With four–time evaluation, the values are divided by four.

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Note



① Cyclic operation in one direction is possible without restriction (this also applies to continuous cyclic operation “backward”).

② In the area preceding the first or the last cam a reversal of direction is possible without restriction.

③ Exceeding the last cam value in a positive direction requires that you maintain the traversing direction until the first cam value behind the zero point is reached.

④ Exceeding the first cam value in a negative direction also requires that you maintain the same traversing-direction until reaching the last cam value after the zero point.

In the event of reversal of direction in the area between the last and the first cam value (in this case 350 and 20), the track identifier bits of all of your assigned tracks are set or reset respectively. Enabled interrupts are also triggered by this.

As a remedy, a track with a cam from 20 (E) via O to 350 (A) can be assigned. With this track identifier bit, the traversing direction in the SIMATIC S5 must then be linked and “held”.

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1.8.2 Conditions

Incremental encoder:

1. The zero mark of the encoder and the preliminary contact define the end value of the rotary axis. The encoder must be selected in accordance with the rotary axis requirements, or the zero mark and the preliminary contact must be transferred to the IP 241 accordingly.

   Example: Desired area O to 359 (360 positions)
   The zero mark with the preliminary contact appears exactly with pulse 360 (i.e., 359 is followed by the actual value O).

2. The preliminary contact, required for synchronizing of incremental encoders, and the zero mark must be active at the zero position at each revolution. This means that in case of continuous conveyors, the application of the respective preliminary contact is also required when the encoder crosses zero. This is one reason why absolute encoders are used for continuous conveyors. Another reason is that often no reference point traversing can be realized with a continuous conveyor.

Absolute encoders:

The encoder end value defines the end value of the rotary axis.

This means that the encoder must be selected in accordance with the rotary axis requirements or that a programmable encoder must be used.

Example: Desired area Oto511
An encoder with512 position resolution is selected.

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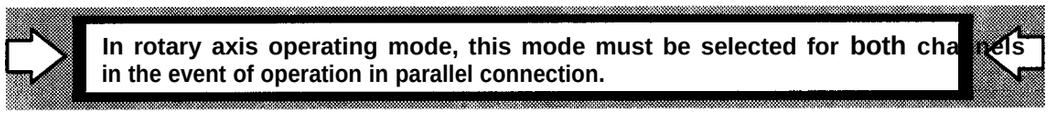
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1.9 Parallel Connection Operation

1.9.1 Function

The "operation in parallel connection" function makes it possible to use a maximum of 32 tracks (with only one encoder matching module) without additional wiring in pseudo single–channel mode.

This means that the result from the comparison of the actual values with the setpoints can be evaluated by reading the track identifier bits for channel 1 (tracks Oto 15) and channel 2 (tracks 16 to 31).



– For parameterization with the standard function block FB 156, the desired function is specified in the data block (IP 241) in accordance with the programming instructions (see section 9).

– In case of parameterization (without the standard function block) the following applies:

The function–associated constant F6 in the format KH (or 1111 0110 in the format KM) is loaded into the start-up OBS (OB 20 to OB22), and F6 is then transferred to the set module address +4 in accordance with section 9.5.

1.9.2 Conditions

1. Insert the encoder matching module of your choice for channel 1.
2. Connect the encoder to channel 1 only.
3. Required release status of the module:
   ≥ A14 (firmware status R08) for 6ES5 241 –IAA11 or
   ≥ AO1 (firmware status R09) for 6ES5 241–1AA12
4. After a power failure this function must be newly parameterized.
   (There is no buffering on the IP.)

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1.10 Verify-Read 1)

This special function is used to eliminate brief disturbances (e.g., on the encoder line).

The basic module reads the actual value of the matching encoder submodule. Immediately after this read access, the actual value is read again, and compared with the value first read in. If equal, calculation is continued with this value. If not equal, reading is continued until the values are equal, or until the maximum number of test read procedures (15) is reached. The last value is then processed as the valid value.

Entry in Byte (Module Address + n)		
n = 0	n = 1	n = 4
Channel no: 1 or 2	Number of test read accesses: O to 15	F2

The function is selected with transfer of F2, and deselected with transfer of F2 and "number of test read accesses = O".

Verify-read should only be used for higher encoder frequencies. This function is not suitable for the BCD/dual matching encoder module.

1.11 Calculation of the Average Value (Analog Submodule) 1)

This special function calculates the average value of up to 15 consecutive actual values and should only be used with the analog submodule.

Entry in Byte (Module Address + n)		
n = 0	n = 1	n = 4
Channel no: 1 or 2	Number: O to 15	F3

The function is selected with transfer of F3, and deselected with transfer of F3 and "number = O".

1) This function is implemented as of firmware release R09. The standard function blocks support the special function starting with the release states given in the technical specifications (→ sections 9.2.6,9.3,6 and 9.4.6) for the library number.

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1.12 Inhibit Interrupt 1)

1.12.1 General

This special function allows you to use software to inhibit all interrupts of the module.

Entry in Byte (Module Address +n)		
n = 0	n = 1	n = 4
		E3

The function is selected by transfer of **E3,** and deselected with another transfer of **E3.**

The status of bits 5 and 6 in response message byte 7 (module address +7) indicates whether this function is active.

Function active: bit 5 = 1
bit 6 = 1

1.12.2 For Supplying the Module with Setpoints 1)

The module does not trigger illegal interrupts during reparameterization and during changing cam setpoints.

Entry in Byte (Module Address +n)		
n = O	n = 1	n = 4
		E4

The function is selected by transfer of **E4,** and deselected by another transfer of **E4.**

The status of bit 6 in response message byte 7 (module address +7) indicates whether this special function is active.

Function active: bit 6 = 1

Do not transfer identifiers E3 and E4 consecutively unless the respectively activated interrupt inhibit function has been cancelled between them.

1) This function is implemented as of firmware release R09. The standard function blocks support the special function starting with the release states given in the technical specifications (→ sections 9.2.6,9.3.6 and 9.4,6) for the library number.

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1.12.3 Depending on Direction 1)

This function allows you to inhibit the interrupts for channel 1 and/or channel 2, depending on the direction.

Channel	Inhibit Direction	Entry in Byte (Module Address +n)		
		n = 0	n = 1	n = 4
1	Backward	xl		F8
1	Forward	x2		F8
1	Backward and forward	x3		F8
2	Backward	lx		F8
2	Forward	2x		F8
2	Backward and forware	3x		F8

1.13 Read Zero Shift Value 1)

This special function can be used to read the values of the zero shift.

Channel	Entry in Byte (Module Address+n)		
	n = 0	n = 1	n = 4
1			E8
2			E9

The function is executed once with transfer of E8/E9.

The zero shift values are indicated in the bytes of module address +4, +5 and +6.

1) This function is implemented as of firmware release R09. The standard function blocks support the special function starting with the release states given in the technical specifications (→ sections 9.2.6,9.3.6 and 9.4.6) for the library number.

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2 Operating Instructions

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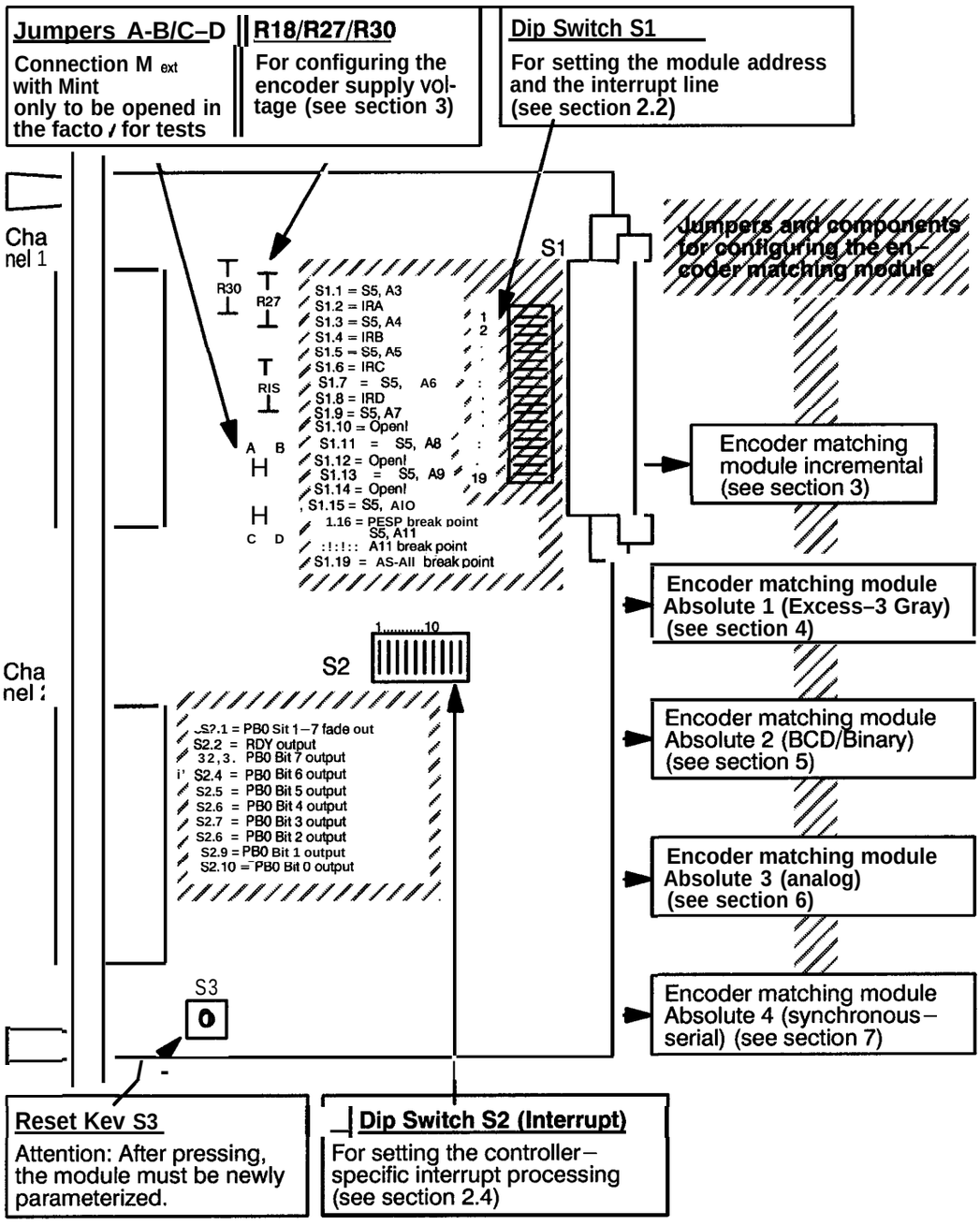
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2.1 Overview of IP 241 Settings



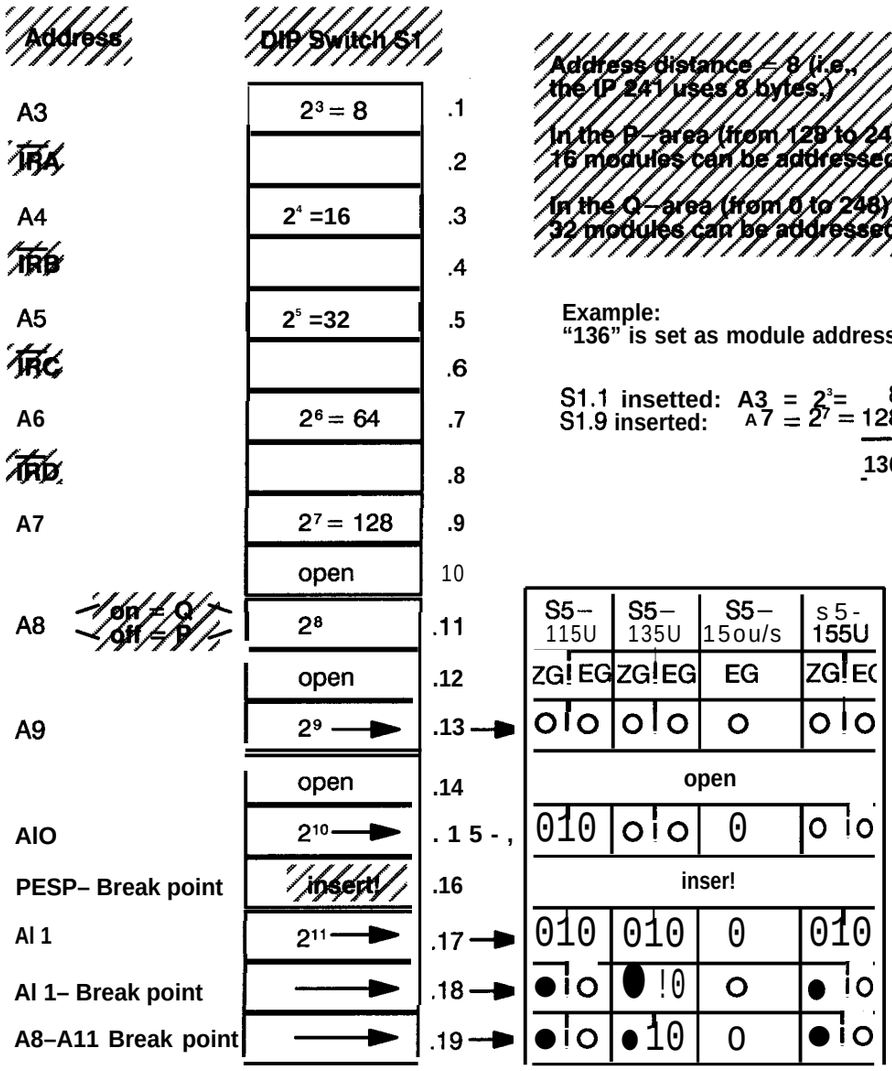
All DIP switches that are not required for the respective use must remain open!

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2.2 Settings for the Module Address and the Interrupt Lines

(See the layout for the basic module, section 2.1.)



Address distance = 8 (i.e., the IP 241 uses 8 bytes.)

In the P–area (from 128 to 248) 16 modules can be addressed.

In the Q–area (from 0 to 248) 32 modules can be addressed.

Example:
"136" is set as module address.

S1.1 insetted: A3 = 2^3 = 8
S1.9 inserted: A7 = 2^7 = 128
136

Sections 2.3 to 2.8 show the settings for the interrupt lines.

When the IP 241 is used without interrupts, the switches S1.2, S1.4, S1.6, S1.8, and S2 must be open!

S5 = Programmable Controller
ZG = Central unit
EG = Expansion unit
O = open
. = inserted

The Q–area cannot be addressed in the central unit.

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2.3 Possible Interrupts (Alarms)

Interrupts can be allocated to the following values by an entry into a data block (IP 241):

- **For each initial track value (of a cam)**

  An interrupt is triggered only when the initial value is reached or exceeded from any traversing direction.

  → This is used when the cam triggers a quick reaction at the start, but not at the end.

  Example: A coolant pump is switched on rapidly. It is not necessary to interrupt the cyclic program to turn this pump off.

- **For each track end value (of a cam)**

  An interrupt is triggered only when the end value is reached or exceeded from any traversing direction.

  → This is used when the cam triggers a quick reaction at the end, but not at the start.

  Example: The forward movement of a milling head is not necessarily started by an interruption of a cyclic program; however, a quick stop is required at the end position.

- **For each track (of each cam) initial and end value**

  An interrupt is triggered when the initial and end value is reached or exceeded.

  -t This is used when, independently from the traversing direction, a quick reaction is required at both ends of the cam.

  Example: A valve is closed very quickly from both traversing directions.

- **With the NV value an additional interrupt can be allocated to the zero shift in the data block (IP 241).**

  – The first synchronization causes an interrupt.
  – Each subsequent synchronization with the same NV value causes no interrupt in rotary axis mode and in linear axis mode.

  Example: A material conveyor is activated very rapidly when a new reference point is transferred by specifying the zero shift.



For enabled interrupts the module "automatically" generates an interrupt under the following circumstances:

– during the reparameterization of set values
– during synchronization of software or hardware
- during deleting with B bit (see section 9.6)

If this is not desired, you can use the new functions in section 1.12.

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As the individual programmable controllers have different interrupt processing routines, the IP 241 provides controller–specific interrupt signals (see section 2.4).

1.) as a hardware interrupt via the interrupt lines IRA, IRB, IRC, IRD
2.) as an interrupt via the peripheral byte 0 (PYO)
3.) in master/slave operation (i.e., a combination of hardware interrupt and peripheral byte 0).

Notes:

- **If the peripheral byte O is used as an interrupt source, the address O may not be used in the P–area of any other 1/0 module (double addressing).**
- **After start-up, the interrupts in OB20 to OB22 must be deleted. This is accomplished by reading identifier bits.**

In all interrupt and time-controlled OBs, when error OBs are used, or in the event of an automatic or manual restart, the scratchpad flags must always be saved prior to interrupt processing (see examples for interrupt processing on the next page) and restored after interrupt processing.

In each of the cases mentioned, a different area of the applied data block must be used to prevent mutual interference.

This procedure also applies to the use of system date!

With the S5–155U programmable controller the cyclic program (user program is interrupted at command limits in case of an interrupt (exception: standard function blocks for which the interrupts can be inhibited for a certain period of time (see technical specifications of the function blocks). Therefore, the scratchpad flags must be saved.

For the S5–135U programmable controllers, allow interrupts only at block limits since the alarm inhibit ("IA") and alarm enable ("RA") functions react only to interrupts and not to timed interrupts.

Scratchpad flags are the flags from 200 to 255. These flags are freely available to the user in the programmable controller.

As these flags are partially used by the standard function blocks, all of these flags must be saved when a standard function block is interrupted and must be restored again. This can be accomplished by transferring the flags to a data block.

The technical specifications for the standard function blocks outline which scratchpad flags (or system data) are used.

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Example for the Recommended Interrupt Evaluation in the Cyclic Program and in the interrupt–OBs:

Program in 062:

Save scratchpad flags!

```
          : JU FB 157
Name      : Per:WST
SPDB      : KY
BEF       : KSKB
ABIT      : KY0,0
W
KB
ST        : FY 191*
PAFE:
SPFE:

          :  O  F  190.0**
          :  O  F  191.0
          :  IC FB xx

          :  O  F  190.1 **
          :  O  F  191.1
          :  IC FB yy

          : L KBO ***
          : T FY 190
          :  T FY 191
```

Reload scratchpad flags

```
          : BE
```

Program in 061:

```
          : JU FB 157
Name      : Per:WST
SPDB      : KY
BEF       : KS)()(
ABIT      : KY
W
KB
ST        : FY 190'
PAFE:
SPFE:

          :  O  F  190.0
          :  IC FB xx

          :  O  F  190.1
          :  IC FB yy
```

* For operation with several modules which output interrupts, different flag bytes must be used here,

** scanned in the interrupt OB accordingly

*** and reset.

At parameter ST Bit O, the interrupt of channel 1 is output.
At parameter ST Bit 1, the interrupt of channel 2 is output.

FBxx = Special interrupt program for channel 1 of the IP 241
FByy = Special interrupt program for channel 2 of the IP 241

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2.4 General Interrupt Routing in the Programmable Controllers

- Setting for the IP 241 without interrupt processing

  DIP Switch S2: All switches OPEN
  DIP Switch S1: IRA to IRD OPEN

- Settings for one IP 241 with interrupt processing via hardware line

  Depending on the interrupt line used, the corresponding switch on the module must be closed.

  The switches for the unused lines must be opened.

	Switch S1.2	Switch S1.4	Switch S1 .6	Switch S1 .8
IRA line	x	–	–	–
IRB line	–	x	–	–
IRC line	–	–	x	–
IRD line	–	–	–	x

x = closed – = open

- Settings for one IP 241 with interrupt processing via peripheral byte O (PY0) and no additional interrupt module.

  The DIP switches for interrupt lines S1 .2/S1 .4/S1 .6/S1.8 must be opened.

  The interrupt is output as a group interrupt via the peripheral byte O; in this case switch S2.1 must be opened.

  Switch S2.2 must be closed. (After recognition of the address O and of the control signal MEMR, the acknowledgement signal RDY goes to the CPU of the programmable controller.)

  The switches S2.3 to S2.1 O must be closed.

  Thus an evaluation is only possible in OB2 of the programmable controller.

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- **Settings for two to eight IP 241s with interrupt processing**

The distinction as to which IP has triggered the interrupt can be made by using the so–called group interrupt (i.e., by output via the peripheral byte O (PY0)).

By means of the peripheral byte O, a programmable controller can distinguish up to eight position decoder modules (IP 241).

For this purpose all modules must be installed in the same central or expansion unit!

The group signals are called by parameters 0.0 to 0.7. The group for each module is switched to the data bus via the contacts of DIP switch S2.

Master/Slave-Principle:

On the first module, the master(the group signal) is routed to bit O of the PY0; on the second module, the slave is routed to bit 1 of the PY0 and so on.

Master: On the first module contact S2.1 must be opened and contact S2.2 closed.
-t the group signal is only activated on bit O of the PY0.
Additionally on the DIP switch S2 those contacts which were assigned to the slave modules as bits of the PY0 are opened. All PY0 jumpers which are not required by a slave must be closed.

Slave: On the other IP 241 modules with group signal, these contacts S2.1 and S2.2 remain closed.
On the DIP switch S2 of the slave modules, in addition to S2.1 and S2.2 only that contact which will be assigned a corresponding bit of the module's peripheral byte O is closed. The other seven S2 contacts on the slave modules must be opened.

Example: x = closed – = open

PY0	DIP switch S2..	Master	Slave 1	Slave 6
Bit O	.10 Group interrupt	x	–	–
Bit 1	.9 –"-	–	x	–
Bit 2	.8 –"–	X	–	–
Bit 3	.7 –"–	x	–	–
Bit 4	.6 –"–	X	–	–
Bit 5	.5 –"–	X	–	–
Bit 6	.4 –"-	–	–	x
Bit 7	.3 –"–	x	–	–
	.2 Enable group int. PY0	x	x	x
	.1 Change over: Only OB2 (o en) or OB2 to8B 9 (closed)	–	x	x

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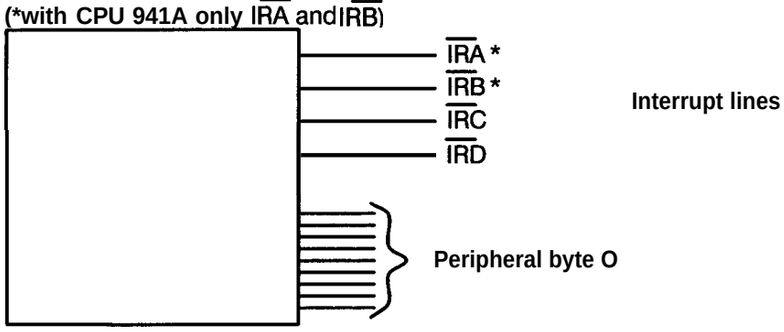
2.5 General Interrupt Processing with thePLCS5–115U

With the programmable controller S5–115U, the interrupt lines in general are available for interrupt processing.

Via the peripheral byte O it then can be established which module(s) has (have) triggered the interrupt on the line.

The IP 241 issues an interrupt by activating the interrupt line (e.g., by outputting a low signal). This is performed in the central unit directly and via interface IM 307/31 7 with light wave conductor coupling for expansion device ER 701–3 or EG 186U.

Interrupt organization for S5-115U
(*with CPU 941A only $\overline{IRA}$ and $\overline{IRB}$)



Interrupt for one 1P 241 module

if only one module (IP 241) is used per interrupt line (IRA to IRD), the peripheral byte O must be disabled (DIP switch S2.1 to S2.1O open) and the interrupt lines must be defined by the corresponding DIP switch S1 setting.

In the CPU, a hardware interrupt on the interrupt line causes a jump to a firmly assigned interrupt OB.

- IRA to OB2 ...highest priority
- IRB to OB3
- IRC to OB4
- IRD to OB5 ...lowest priority

One interrupt IR line is assigned to an IP 241 module.
The DIP switches for the interrupt IR lines not used by this module must be opened! (Section 2.5.2)

WWhen the peripheral byt O is used, the address O may not be used in the P–area of any other I/O module!

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Interrupt for several IP 241 modules on one interrupt line

If several IPs access one interrupt (IRA to IRD), the individual IPs must be identified. For this purpose (up to eight units) a specific bit must be allocated in the peripheral byte O for each 1P; (e.g., peripheral bit 0.0 for IP1, peripheral bit 0.1 for IP2 and soon (see section 2.5.2).

In order to prevent the CPU from stopping because of acknowledgement delay (QVZ), the following program section must be entered into a function block and called by OB21 and OB22:

```
L RS 16
L KH FEFF
A W
T RS 16
```

The peripheral byte 0 is evaluated in the interrupt organization block with the commands:

```
L PY0
T FY...
A F...
```

If, for example, the peripheral bit 0.0 = 1, the IP to which this bit was allocated has triggered this interrupt.

2.5.1 Interrupt Processing with Standard Function Block FB 157 (PER: WST)

When an interrupt occurs, the pertaining interrupt OB is called. The call for function block FB 157 with the parameter assignment BEF = KB is written into this organization block.

After the call by the interrupt OB, parameter ST shows from which channel the interrupt originated (i.e., you can have your specific interrupt program processed then).

If during processing of function block FB 157 in the cyclic program an interrupt occurs, the roup interrupt at the bus is cancelled by FB 157 (or by reading byte 7).

Consequently, no interrupt identity bit can be evaluated in the alarm OB.

In the function block, however, the control bits are updated, so that depending on the interrupt identifier bits saved in the flag, your specific interrupt program can be called. This means the information about the channel from which the interrupt originated is stored in the control byte (ST).

Therefore after each call of FB 157 in the cyclic program both IP 241 interrupt bits must be scanned!

After having been evaluated, the control bits in the interrupt–OB must be reset, as otherwise the interrupt programs (FBxx and FByy) might be processed in the cyclic program once again.

This is taken into account in the example in section 2.3.

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2.5.2 Table for Interrupt Routing (S5–115U)

a) Setting for IP 241 without interrupt

DIP switch S1 (IRAto IRD) All open	DIP switch S2 All switches open

b) One IP 241 per interrupt

CPU 141A/B	CPU 942A/B	CPU 943A/B	CPU 944A/B	Signal	DIP switch S1		DIP switch S2 (Peripheral byte O disable)
OB2	OB2	062	OB2	$\overline{IRA}$	S1.2	Use only one interrupt line per IP 241.	All switches open
OB3	063	OB3	OB3	$\overline{IRB}$	S1.4		S2.1to S2.10 open
OB4 ①	OB4	OB4	OB4	$\overline{IRC}$	S1.6		
OB5 ①	OB5	OB5	OB5	$\overline{IRD}$	S1.8		

c) Several IP 241s per interrupt (Allocation of hardware interrupts in peripheral byte O)

CPU 941A 941B	CPU 942A 942B	CPU 943A 943B	CPU 944A 944B	Signal	DIP switch S1		DIP switch S2 (allocation of the peripheral bits) (see Master/Slave principle, section 2.4)		
							Peripheral BYTE 0	Master	Slave
OB2	OB2	OB2	OB2	$\overline{IRA}$	S1.2	Use only one interrupt line per IP 241.	Bit 0 S2.10	S2.1 open	S2.1 inserted
OB3	OB3	OB3	OB3	$\overline{IRB}$	S1.4		Bit 1 S2.9	S2.2 inserted	S2.2 inserted
OB4 ①	OB4	OB4	OB4	$\overline{IRC}$	S1.6		Bit 2 S2.8		
OB5 ①	OB5	OB5	OB5	$\overline{IRD}$	S1.8		Bit 3 S2.7		
–	–	–	–		S1.10		Bit 4 S2.6		
–	–	–	–		S1.12		Bit 5 S2.5		
–	–	–	–		S1.14		Bit 6 S2.4		
							Bit 7 S2.3		

① Only for CPU 941B

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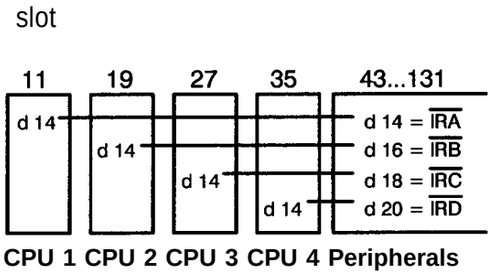
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2.6 General Interrupt Processing with S5-135U

A separate hardware interrupt line is allocated to each CPU slot (IRA to IRD).

The IP triggers an interrupt by activating the interrupt line (i.e., by outputting a low–signal)

In the corresponding CPU a jump to interrupt 062 is effected (for more details see Equipment Manual for the S5–135U).



Allocation of IRA to IRD via DIP switch S1

Interrupt lines	DIP switch S1	
IRA	S1.2	CPU 1
IRB	S1.4	CPU 2
IRC	S1.6	CPU 3
IRD	S1.8	CPU 4

For interrupt processing the IP must be inserted into a slot with interrupt line (slots 43 to 131). See section 8.8.

Interrupts are not possible in the expansion unit unless lines exist there (e.g., ER 701–3 or EG 186U) and the devices are connected via interface IM 307/317.

. Setting for IP 241 without interrupt processing

DIP switch S1: IRA to IRD : OPEN
DIP switch S2: All switches OPEN

- Setting for one IP 241 with interrupt processing

One of the lines IRA to IRD must be selected with DIP switch S1.
The switches for the remaining lines must be openad!

- Setting for two to eight IP 241s with interrupt processing

One of the lines IRA to IRD must be selected with DIP switch S1; (the same line for all master and slave modules).
The switches for the remaining lines must be opened!

The individual modules must be set in accordance with the Master/Slave principle (see section 2.4).

If several IPs are used on one interrupt line, the triggerig IP can be recognized by evaluating the peripheral byte. For more details see the Equipment Manual for your programmable controller.

Evaluation of the peripheral byte O is only possible if the module is addressed in the P–area.

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2.6.1 Interrupt Processing with Standard Function Block FB 157 (PER:WST)

When an interrupt occurs, the interrupt OB2 is called. The call for the function block FB 157 with the parameter assignment BEF = KB is written into this organization block.

After the call by the interrupt OB, parameter ST shows from which channel the interrupt originated (i.e., you can have your specific interrupt program processed then).

If, during the processing of function block FB 157 in the cyclic program, an interrupt occurs, the group interrupt at the bus is cancelled again by FB 157 (or by reading byte 7). This interrupt is not lost when the recommended programming for interrupt OB2 is followed (see example in section 2.3).

2.6.2 Save and Reload Scratchpad Flags

In the S5-135U, OBs with special integrated functions are available for saving and reloading scratchpad flags. For CPU 922 (version A09 or later) and for CPU 928, these OBs are OB 192 (for saving) and OB 193 (for reloading).

> For the S5-135U programmable controller interrupts should only be allowed at block limits, because the alarm inhibit ("IA") and alarm enable ("RA") functions react here only to interrupts and not to timed interrupts.

Because of this, saving and reloading scratchpad flags is necessary only during a warm restart.

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2.7 General Interrupt Processing with S5–150 S/U

The operating system of the programmable controller scans the peripheral byte O (PY0) at each block limit.

When an interrupt occurs, a jump to the correlated interrupt organization block (OB2 to OB9) takes place.

In the programmable controller the bits 0.0 to 0.7 are directly allocated to the OBs 2 to OB9.

Bit 0.0 activates OB2, bit 0.1 activates OB3 and so on.

A bit of byte O can be allocated to any IP 241.

This allows a maximum of 8 IPs with interrupt processing in the expansion unit.

> **!** In the programmable controller S5–150S/U, the IP 241 may only be operated in the expansion unit. **!**

Example:

x = closed – = open

PY0	DIP switch S2..	Jump to oB No.	Master	Slave 1	Slave 6
Bit O	.10 Group interrupt	2	x	–	–
Bit 1	.9 –"-	3	–	x	–
Bit 2	.8 –"-	4	x	–	–
Bit 3	.7 –"-	5	x	–	–
Bit 4	.6 –"-	6	x	–	–
Bit 5	.5 –"-	7	x	–	–
Bit 6	.4 –"-	8	–	–	x
Bit 7	.3 –"–	9	x	–	–
	.2 Enable group interrupt PY0		x	x	x
	.1 Changeover: OB2 only (open) or OB2 to OB9 (closed)		–	x	x

> The DIP switches S1.2, S1.4, S1.6, and S1.8 must be opened, because the programmable controller S5–150S/U does not have interrupt lines.

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2.7.1 Interrupt Processing in PLC S5–150 S/U with Standard Function Block FB 157 (PER:WST)

If one of the setpoints or a zero shift value is supplied with an interrupt identifier, the module must be set to a group interrupt bit of the peripheral byte PYO via jumper adjustment.

The number of this group interrupt bit must be specified at parameter ABIT (in the interrupt OB):

ABIT : KY = x,y x >< 0 No reset of the pertaining interrupt bit in the system data

x = O Reset of the pertaining interrupt bit in the system data

$0 \leq y \leq 7$ Number of the interrupt bit

See the Equipment Manual for the S5–150S/U.

When an interrupt occurs (analog to the jumper setting) the corresponding interrupt OB is called.

The call for the function block FB 157 with the command = KB (read track identifier bit) is entered into this alarm OB. After the call the parameter ST shows from which channel the interrupt originated.

Now you can have your specific interrupt program processed.

A recommendation for interrupt OB programming is shown in the example in section 2.3.

If an interrupt occurs during processing of function block FB 157 in the cyclic program, the group interrupt at the bus is cancelled by FB 157 (or by reading byte 7).

Consequently no interrupt identity bit can be evaluated in the alarm OB.

In the function block, however, the control bits are updated, so that depending on the interrupt identifier bits saved in the flag, your specific interrupt program can be called. This means the information from which channel the interrupt originated is stored in the control byte (ST).

Therefore after each call of FB 157 in the cyclic program, both IP 241 interrupt bits must be scanned!

After being evaluated, the control bits in the interrupt OB must be reset so that the interrupt programs (FBxx and FByy) are not processed in the cyclic program again.

This is taken into account in the example in section 2.3.

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2.8 General Interrupt Processing with PLC S5-155U

The central processor of the programmable controller operates in two operating modes:

–S5–150U mode
–S5–155U mode

The two operating modes process interrupts differently.

	S5–150U Mode	S5–155U Mode
Type of processing	Process interrupt	Interrupt
Acquisition of the interrupt via	Input byte IB0	Interrupt lines
Acquisition of the interrupt at	Block boundaries	Instruction boundaries (level-triggered)
Jumpers on CPU 946	X46 to X49 open	X46 to X49 closed
Organization block	OB2 to OB9	OB2 to OB5
AF and AS commands affect program	Yes	No
Effect of special function OB 122	Yes	Yes

Standard function blocks FB 38 and FB 39 must be used in the interrupt program since these blocks save and load other temporary (system) data. These function blocks must be used with the same data block in all interrupt programs.

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2.8.1 Interrupt Processing in PLC S5–155U with Standard FB 157 (PER:WST)

When an interrupt (process interrupt or interrupt) occurs the appropriate interrupt OB is called depending on operating mode and jumper settings on the IP 241.

Function block FB 157 is then called in the interrupt OB with the command BEF = KB.

Parameter ST indicates from which channel an interrupt was reported. The interrupt bits must be evaluated each time FB 157 is called.

Bit O: channel 1
Bit 1: channel 2.

You can start your own interrupt program when a bit has signal status"1".

A recommendation for interrupt OB2 or FBO programming is shown in the example in section 2.3.

If an interrupt occurs during processing of function block FB 157 in the cyclic program, the group interrupt at the bus is cancelled by FB 157 (or by reading byte 7).

Consequently no interrupt identity bit can be evaluated in the alarm OB.

In the function block, however, the control bits are updated, so that depending on the interrupt identifier bits saved in the flag your specific interrupt program can be called. The information from which channel the interrupt originated is stored in the control byte (ST).

Therefore after each call of FB 157 in the cyclic program, both IP 241 interrupt bits must be scanned!

After being evaluated, the control bits in the interrupt OB must be reset so that the interrupt programs (FBxx and FByy) are not processed in the cyclic program again.

This is taken into account in the example in section 2.3.

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2.9 Sequence for the Start-Up of the IP 241

1) Check for up–to–date software and hardware status.

1.1) Shielding of encoder lines (Shielding with potential (M_{ext}) (e.g., by screw connecting the metal housing of the connector on the IP side).

1.2) Internal encoder supply (from IP 241)
External encoder supply (at encoder)

1.3) Perform potential equalization with sufficient cross sections.

2) Setting the DIP switches on the basic module

Dip Switch:	S1 (Module address = interrupt lines)	see sections 2.1 to 2.8
	S2 (Group interrupt, peripheral byte O)	see sections 2.1 to 2.8

3) Configuring encoder supply voltage for incremental encoders on the IP 241 basic module

Encoder supply	see section 3.3.3

4) Configuring the encoder matching modules for encoder supply voltage and input signals

Encoder matching module	
Incrementa (Preliminary contact/zero mark)	see section 3
Absolute 1 (Excess–3 Gray)	see section 4
Absolute 2 (BCD/Binary)	see section 5
Absolute 3 Analog	see section 6
Absolute 4 Synchronous–Serial	see section 7

5) Insert module into slot of programmable controller (See section 8.8.)

6) Apply voltage supply (24 V external)

7) Setting up the data block DB (IP 241)

Set up a data block with a minimum length of 187 DWS

see section 9" Programming Instructions"

8) Setting up start-up organization blocks (OB20 to OB22)

– Save scratchpad flags
– Parameterize IP 241 with FB 156
– Delete interrupts with FB 157 (BEF = any)
– Reload scratchpad flags
– Consider time requirements according to section 8.3 — see sections 2.3 to 2.8

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9) Setting up a cyclic program in OB1

– Cyclic program depending on programmable controller and task

10) Setting up the interrupt program

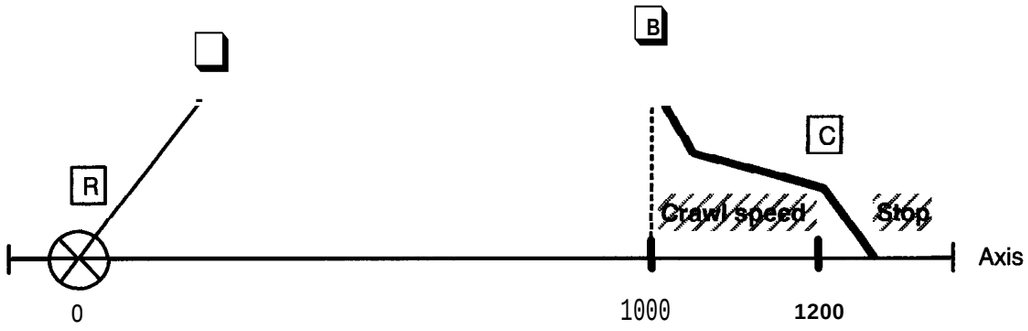
– Save scratchpad flags
– Evaluate interrupts with FB 157 (BEF = KB)
  Scan and evaluate interrupt bit
  In case of interrupt jump to your specific interrupt program
– Reload scratchpad flags

see sections to 2.3 to 2.8

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2.10 Example for Better Comprehension of the IP 241

Controlled positioning with incremental encoders:



Sequence:

- Software synchronization (SS) in point B and thus definition of the coordinate zero point (reference or synchronization point).
- Output Q1.0 (Drive ON) is turned on.
- At point A the final system speed is reached.
- When point B is reached, change over to crawl speed (Q1.1 set).
- When point C is reached, turn off (STOP).

How to proceed:

After successful start-up

1) Specify setpoint in data block (IP 241)

Set up and parameterize data block (IP 241)

2) Setup start-up organization blocks

– Save scratchpad flags – Call FB 156 (parameterize) – Call FB 157 (REF = any) (delete interrupts after start-up) – Software synchronization with FB 157 (REF = SS) – Reload scratchpad flags

3) Cyclic processing in OB1

– START (drive ON) – Read actual value

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4) **Interrupt processing**

OB2
– Save scratchpad flags
- Interrupt processing with FB 157 (BEF = KB)
– Evaluate the interrupt bits; in case of interrupt, jump on interrupt program FBX1 or FBX2
– Reload the scratchpad flags

5) Interrupt programs

FBX1
– Change over to crawl speed
FBX2
– STOP

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3 Matching Module for Incremental Encoders

3.1 Function Description . . . . . 3 – 1

3.2 Block Diagram 3–2

3.3 Putting into Operation 3–3
3.3.1 Setting theOperating Mode 3–3
3.3.2 Conditioningthe InputLevels 3–4
3.3.3 Setting the Encoder PowerSupply 3–4
3.3.4 ConnectorAssignment 3–5
3.3.5 Hardware Synchronization 3–6
3.3.6 Software Synchronization 3–7
3.3.7 Layout 3–8
3.3.8 Switch Diagram of the InputAmplifiers 3–8
3.3.9 Component Sets (Incremental, 6ES5 271 – 1AB11) 3–9

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3.1 Function Description

The signals arriving from the encoders via channel A and B are converted to TTL level in the input–conditioning circuit.

Depending on the selected operating mode, the signals are initialized in the directional logic.

Encoders with the following signals can be used:

– Two pulse trains with 90° displacement
– Neutral pulses (1 pulse train, 1 direction signal)
– Direction–sensitive pulses (1 pulse per direction)

The required settings are shown in section 3.3.1.

Incremental encoders provide pulses only; therefore after initial turn–on or power failure, the IP 241 has no system reference (i.e., no reference point is available). The reference point can be established in two ways:

– By hardware–based synchronization (see section 3.3.5).
– By software-based synchronization (see section 3.3.6).

The drive direction for hardware–based synchronization can be selected on the matching module for the encoder; see section 3.3.1 (switch S2) “sign synchronization”. This presetting is required, for example, to eliminate spindle play of your system when the reference point is approached.

In each data block a zero shift (NV value) can be specified separately for each channel. This value is then stored in the synchronization memory of the matching module for the encoder.

The synchronization enable is activated with the SH command in standard FB 157. The µP of the basic module transfers this enable via “TVS” to directional logic and synchronization logic.

The synchronization logic compares the sync sign, the encoder zero mark and the initiating system pulse with the drive direction detected by the directional logic.

When they coincide, the value of the synchronization memory is accepted by the up/down counter.

When the synchronization is completed (see Time Requirements for Synchronization in section 8.3), additional encoder pulses effect a change of the up/down counter contents.

The value of this fast up/down counter is continuously transferred to a 3– byte scan memory.

The transfer is interrupted only as long as the µP reads the 3 bytes.

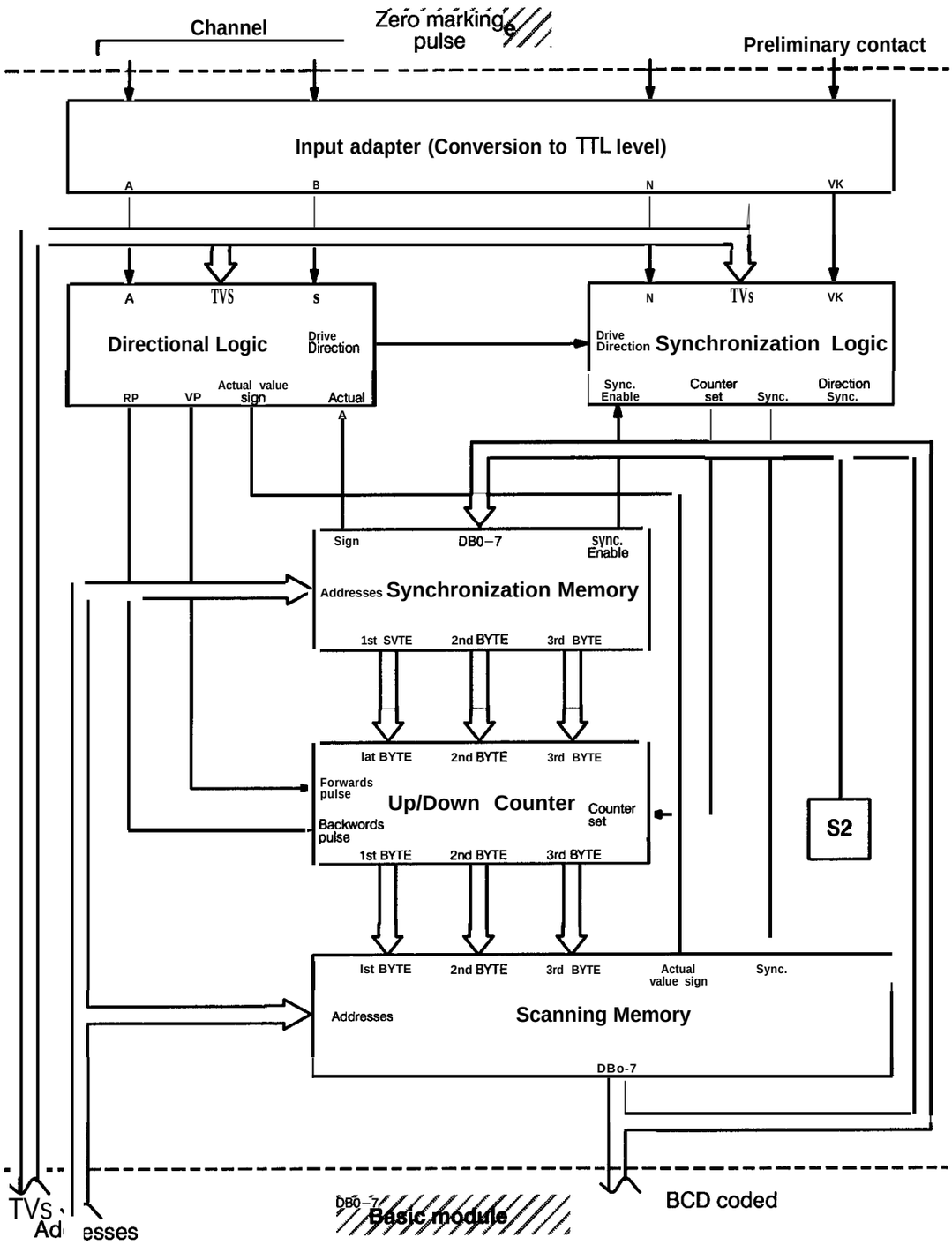
Counter operation and sampling are separated by a clock pulse.

The actual value transferred to the basic module is compared with the track setpoints (cams) there.

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3.2 Block Diagram



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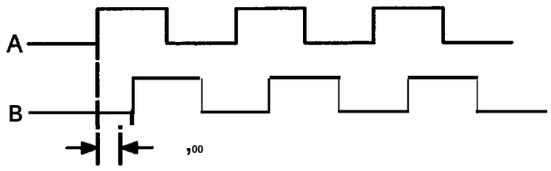
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3.3 Putting into Operation

3.3.1 Setting the Operating Mode

The three possible operating modes are selected with DIP switch S1. The settings apply to symmetrical and asymmetrical operation.

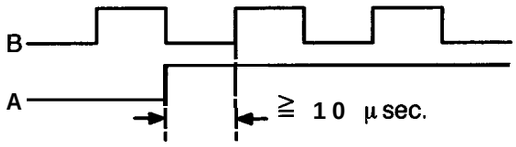
The encoder provides two pulse trains displaced by 90° in relation to each other:



Setting of DIP switch S1:

Closed contacts (x):	1	2	3	4	5	6	7	8
One count pulse evaluated	x				x			
Two count pulses evaluated	x	x			x	x		
Four count pulses evaluated	x	x	x	x	x	x	x	x

The encoder provides neutral pulses (1 pulse train, 1 direction signal):

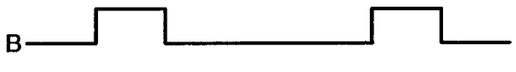


Pulse
Forward direction
Backward direction

Setting of DIP switch S1:

Closed contacts (x)	1	2	3	4	5	6	7	8
	x					x		

The encoder provides direction–sensitive pulses (one pulse per direction):



– Forward pulse

– Backward pulse

Setting of DIP switch S1:

Closed contacts (x)	6	7	8
			x

The specification of the synchronization direction (drive direction) is made by DIP switch S2:

Setting of DIP switch S2:

Contact 1 closed:	Synchronize in backward direction
Contact 1 open:	Synchronize in forward direction

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3.3.2 Conditioning the Input Levels

nput voltage range Incremental encoders)	Input- A A	Input B $\bar{B}$	Input Zero marking pulse $\bar{N}$	Other Components
5 V to + symmetrical ②	R7: Jumper inserted R9: Jumper inserted	R4: Jumper inserted R6: Jumper inserted	R12: Jumper inserted R14: Jumper inserted	CI, C2, C5 = 10 nF soldered in VI, V2, V3: not used
+5 V to + 20 v asymmetrical ①	R9: Jumper inserted	R6: Jumper inserted	R12: Jumper inserted	"1, V2, V3 = IN 4148 solder in diodes CI, C2, C5: not used
+ 10 v to + 30 v symmetrical	R7: 4.7 kΩ R8: 4.7 kΩ ③ R9: 4.7 kΩ ③ RIO: 4.7 kΩ	R3: 4.7 kΩ R4: 4.7 kΩ ③ R5: 4.7 kΩ ③ R6: 4.7 kΩ	R12: 4.7 kΩ R13: 4.7 kΩ ③ R14: 4.7 kΩ ③ R15: 4.7 kΩ	CI, C2, C5 = 10 nF soldered in VI, V2, V3: not used
+ 10 v to + 30 v asymmetrical ①	R9: 4.7 kΩ ③ R1O: 4.7 kΩ	R5: 4.7 kΩ ③ R6: 4.7 kΩ	R12: 4.7 kΩ R13: 4.7 kΩ ③	VI, V2, V3 = IN 4148 solder in diodes C1, C2, C5: not used

Input voltages (incremental encoders) Input initializing pulse	Resistor R11
+ 5 " + 10 V to 18 V + 19 V to 30 v ②	Jumper soldered in 820 Ω 2.2 kΩ

① Attention: Always use when all six encoder signals are not available.

② As delivered.
The mounting locations not defined remain unfitted.

③ If the encoder should not include the low level ≤ 1 ", these resistors can be changed to 2.2 kohm.

See section **3.3.4** for the definition of symmetrical and asymmetrical operation.

3.3.3 Setting the Encoder Power Supply

The required encoder supply voltage must be selected by providing the respective circuitry on the basic module.

Required voltage	Resistors used ④
+ 5 "/0.6A ⑤	R27 =39 kΩ R30 = open R18 = 82 Ω
12 "/0.25A ④	R27/R30 = 124 kΩ/750 kΩ R18 = 220 Ω
15 "/0.2A	R27/R30 = 124 kΩ/750 kΩ R18 = 220 Ω
24 "/2A ④	Not fitted; is output directly from the Faston connector to the sub D connector PIN 49.

④ **See layout for basic module, section 2.1.**
⑤ **Condition as delivered**

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3.3.4 Connector Assignment

Assignment of the sub D connectors (channel 1 or 2)

1	18	34
2	19 _____	35
3	20 Zero marking pulse	36 Zero marking pulse*
4 $\overline{B}$*	21 $\overline{A}$*	37 B
5 A	22	38
6	23	39
7	24	40
8	25	41
9	26	42
10	27	43
11	28	44
12	29	45
13	30	46
14	31 + 5 V/12115	47 + 5 V/12/15
15	32	48
16	33 M	49 + 24 V (output)
17 M		50 M

Pin 31/47 and pin 17/33/50 are parallel and can be used alternatively.

*** For encoders which do not permit all six signals, asymmetrical operation applies! Encoders with only 3 signals must be connected to inputs $\overline{A}$ (pin 21), B (pin 4) and the zero marking pulse (pin 36).**

Symmetrical operation (incremental encoders)

(Improved noise immunity)
Six encoder signals on 50–way sub D connector

Signal A –A PIN 5
Signal $\overline{A}$ – $\overline{A}$ PIN 21
Signal B – B PIN 37
Signal 13 – $\overline{B}$ PIN 4
Signal N – N PIN 36
Signal $\overline{N}$ – $\overline{N}$ PIN 20

- Asymmetrical operation (incremental encoders)

Three encoder signals on 50–way sub D connector

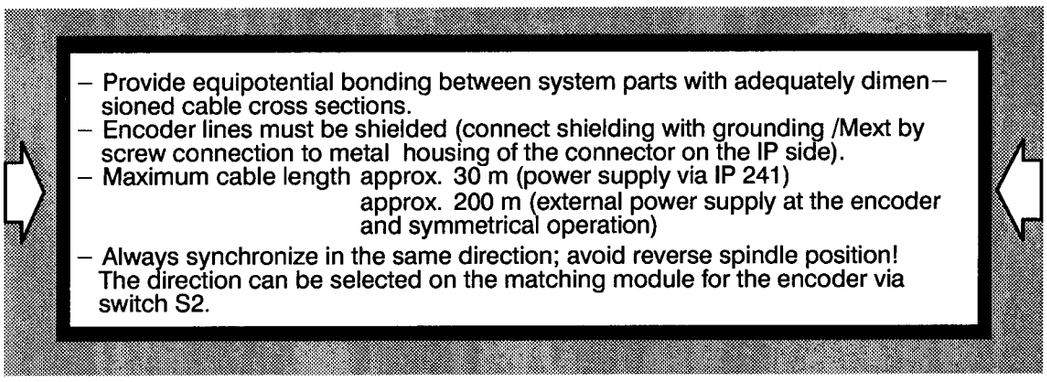
Signal A – $\overline{A}$ PIN 21

Signal B – $\overline{B}$ PIN 4

Signal N – $\overline{N}$ PIN 36

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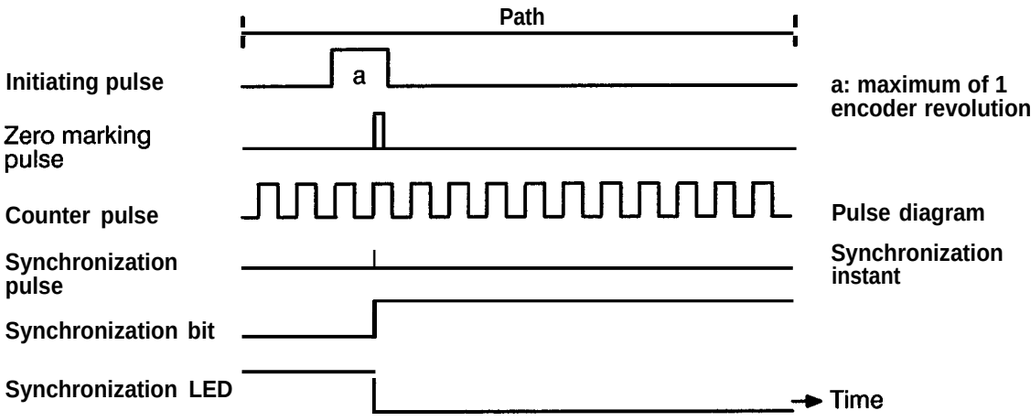
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3.3.5 Hardware Synchronization



The data block (IP 241) is set with an NV value (or left at 0)

The hardware synchronization is called (e.g., by the standard function block with command SH)

The initiating pulse of the sytem is blocked

The encoder pro– vides the zero marking pulse

The encoder pro– vides a pulse

Simultaneously (e.g., by the reference point drive of the system)

yes no

The drive direction coincides with the synchronization direction selected with switch S2

yes no

To update the track identifier bits, the IP 241 requires 1 msec. for each specified start or end setpoint.

The IP 241 sets the synchronization bit
The IP 241 dims the synchronization LED
The IP 241 provides the NV value as actual value

The IP 241 causes an interrupt if the NV value is greater than an entered set value with interrupt identifier, or always when the NV interrupts are enabled. "

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– The area of the external initiating pulse (“a”) must be smaller than one revolution of the encoder. Otherwise, the zero marking pulse of the encoder would be effective twice.

– The zero marking pulse of the encoder (pulse width) should only contain one count pulse. Otherwise, the counter is synchronized as often as the number of pulses contained in the zero marking pulse.

– When the external initiating pulse, the zero marking pulse of the encoder, and a count pulse coincide, the synchronization pulse is generated and the counter is synchronized.

– In the course of synchronization the counter is loaded with the software-based NV value.

– During synchronization the synchronization bit of the respective channel is set and the related synchronization LED on the front plate goes off.

Up to the instant of synchronization the actual value IW = FFFF FFFF.
Up to the instant of synchronization the respective LEDs of the channel are lighting.

3.3.6 Software Synchronization

The data block DB (IP 241) is set with an NV value (or left at zero).

The software synchronization is called (e.g., by a standard function block with the command SS).

To update the result bits (track identification) the IP 241 requires 1 msec for each initial setpoint and each final setpoint specified by the data block (IP 241) contents.

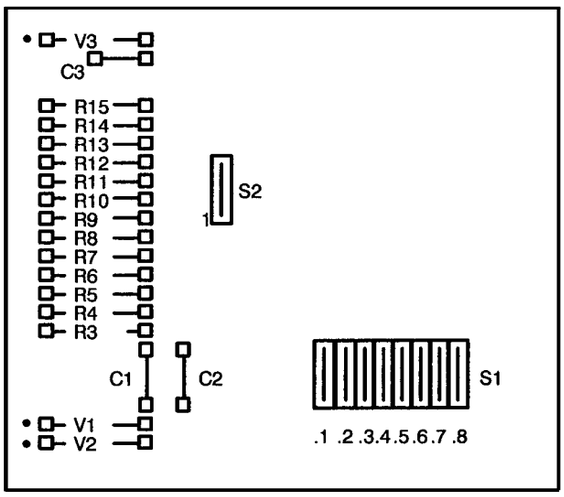
The IP 241 sets the synchronization bit
The IP 241 dims the synchronization LED
The IP 241 provides the NV value as the actual value

The IP 241 causes an interrupt if the NV value is greater than an entered set value with interrupt identifier or always when the NV interrupts are enabled.

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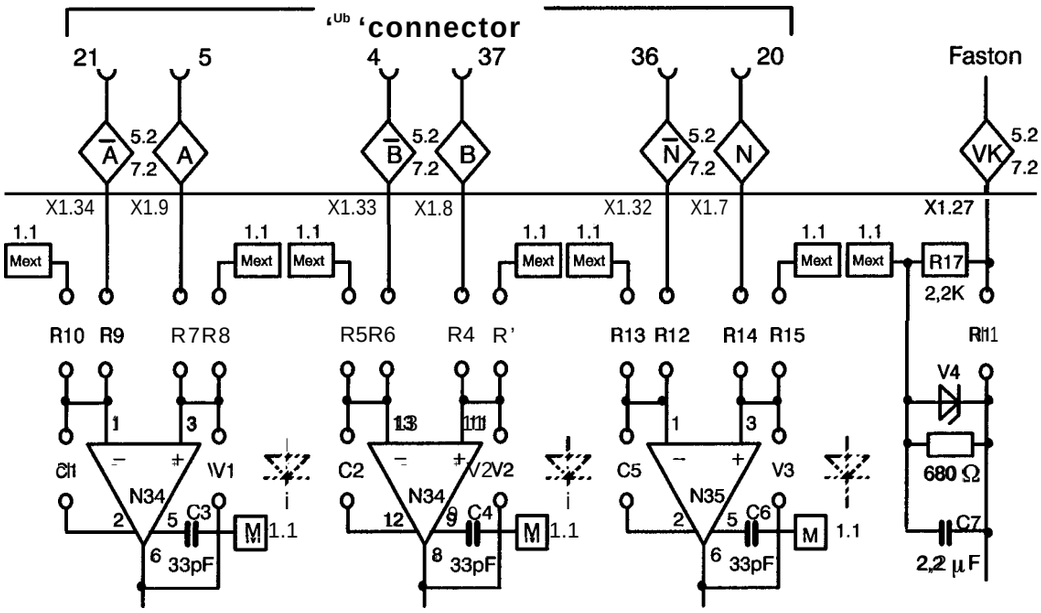
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3.3.7 Layout



The layout shows the position of the configurable elements, jumpers, and switches.

3.3.8 Switch Diagram of the Input Amplifiers



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3.3.9 Component Sets (Incremental, 6ES5 271–IAB11)

Encoder Supply Voltage	Components	Quantity	Value	Designation
+12 V	R27 R30 R18	1 1 1	124 kΩ 750 kΩ 220 Ω	B54311 B54311 W21
+15 V	R27 R30 R18	1 1 1	220 kΩ 390 kΩ 220 Ω	B54311 B54311 W21
Input voltage range				
+10 V to 30 V symmetrical	R3 to R1O R12 to R15	12	4.7 kΩ	B54311
+5 V to 20 V asymmetrical	V1, V2, V3	3	1 N4148	Diode
+10 V to 30 V asymmetrical	R5, R6, R9, R1O, R12, R13 V1, V2, V3	6 3	4.7 kΩ 1 N4148	B54311 Diode
Input voltage of external initiating pulse +10 V to 18 V	R11	1	820 Ω	B54311

The component set allows the conditioning per channel of incremental encoders for IP 241. The set contains the above items and a sub D connector.

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4 Matching Module 1 for Absolute Encoders
(Excess-3 Gray)

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4.3 Putting into Operation 4–3
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4.3.2 Conditioningthe input Levels 4–3
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4.3.8 Switch Diagram of the Input Amplifiers 4–8
4.3.9 Component Sets (Excess–3 Gray, 6ES5 271–1AC11) 4–8

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4.1 Function Description

The actual values arriving in Excess–3 Gray code are converted to TTL level by signal conditioning. A code converter then changes them to BCD code. These actual values are constantly transferred to the output memory and made available to the basic module.

While the actual values are being read, the memory cannot accept new actual values from the encoder.

Encoders for Excess–3 Gray code with up to 5 decades (O – 99999) can be connected.

For Philips glass scales, the system can be switched over to half–step increments (0.5) since the least significant digit with this encoder is not presented as a complete decade but as a binary signal.

If the encoder produces a change–of–value signal, the latter can be evaluated. The change–of–value signal starts the transfer of actual encoder values to the output memory.

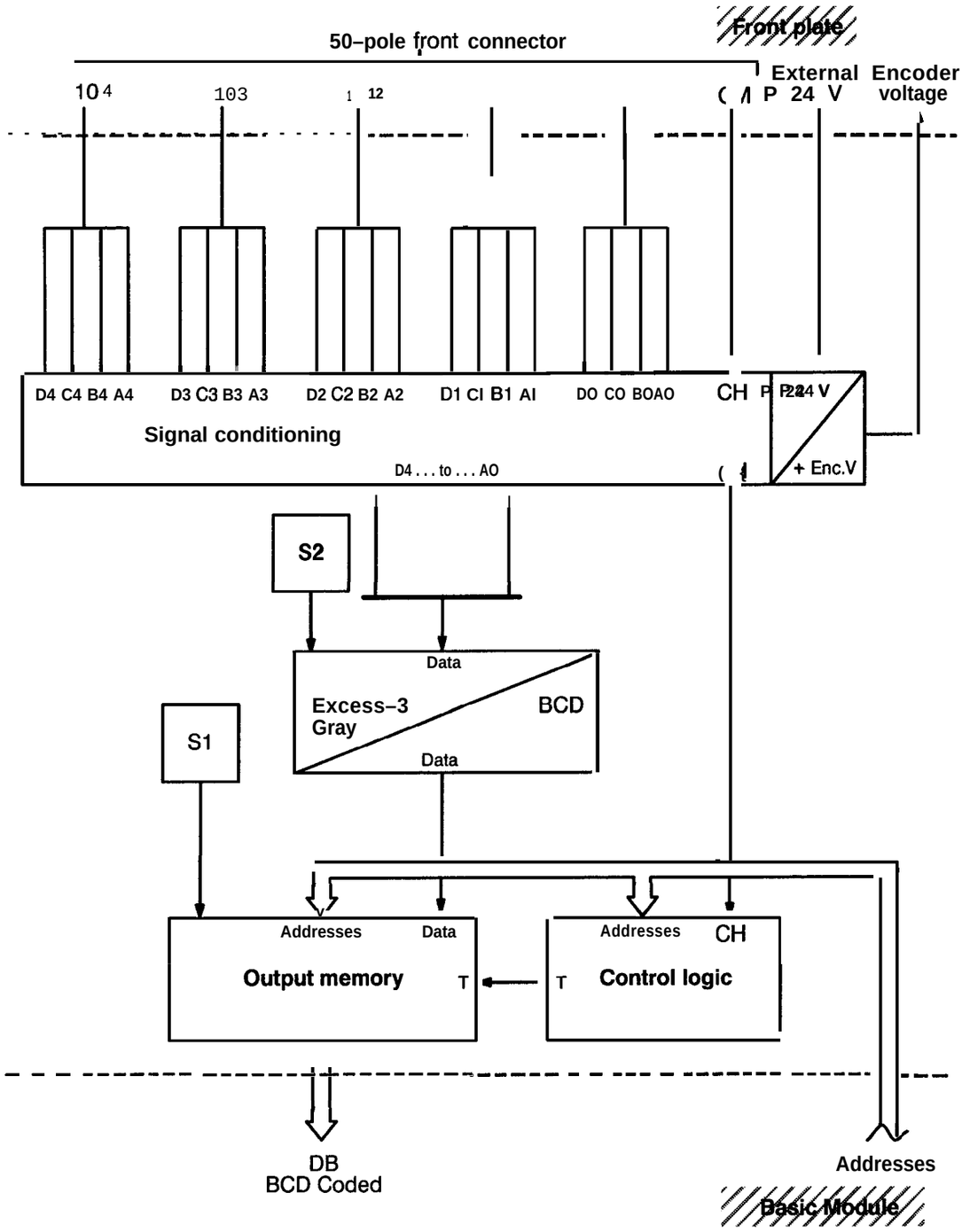
The absolute encoder matching module 1 processes the 3–Excess–Gray code in accordance with the table in section 4.3.5, The connections of the respective sub D connector are assigned to this table.

If the encoder provides a different code table, the connections in the sub D connector must be assigned accordingly (see example in section 4.3.6).

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4.2 Block Diagram



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4.3 Putting into Operation

4.3.1 Setting the Operating Mode

Function	DIP switch S1	DIP switch S2 Contact 1	DIP switch S2 Contact 2
No change signal	——— ① Position 1		
Change signal	– – – ① Position 2		
Philips glass scale with half step increments (0.5)		closed	open
Other encoders		open	closed

① See layout encoder matching module, section 4.3.7.

4.3.2 Conditioning the Input Levels

Input voltage (from Excess–3 gray encoder) = Signal voltage	cl to C21 10 nF	R101/R102 resistor network (joint point)	R103/R104/R105 resistor network (single res.)	R106/R107 resistor network (joint point)
5 V ITL	as required	omitted	wire jumpers	omitted
12 V	as required	omitted	899–3–R 2 K	899-1 –R 1,5 K
15 V	as required	omitted	899=3–R 3,3 K	899-1 -R 1,5 K
24 V	as required	omitted	899–3–R–? K②	899-1 –R 1,5 K
Open Collector	as required	899–1 –R 8,2 K	wire jumpers	899-1 –R 1,5 K

② The resistance depends on the output impedance of the encoder (see note on next page).

Small disturbances occurring in spite of correct wiring and shielding can be sifted off with the capacitors Cl to C21.

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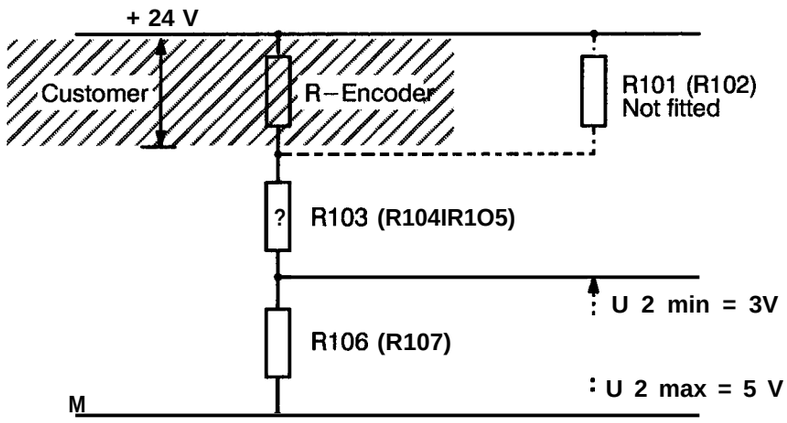
Instructions for Conditioning the Input Circuitry

– In the encoder impedance range from 6 kΩ to 10 kΩ, wire jumpers can be inserted for RI 03/R104/R105.

– Below 6 kΩ encoder impedance, the resistor networks must be computed.

– The high level at R106 or R107 must be between 3 V and 5 V.

– The low level at R106 or R107 must be below or equal to 0.8 V.



$$R = \frac{R2 \times (U - U2)}{U2} - R\text{–Encoder}$$

Explanation:

R	=	R103, R104, R105
R2	=	R106, 107(1,5 kΩ)
U2	=	Voltage at R106,R107 (min. 3 V, max. 5 V)
u	=	Encoder voltage (24 V)
R–Encoder	=	Encoder impedance (see manufacturer's label or encoder data sheet)

How to proceed:

a) Compute the value R max. with U2 minimum (3 V).
b) Compute the value R min. with U2 maximum (5 V).
c) Select the resistor network according to the E series (between R maximum and R minimum).

d) Only resistor networks consisting of single resistors may be used.
" See technical specifications, section 8.6.

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4.3.3 Setting the Encoder Power Supply

The required encoder supply voltage must be provided by suitable adjustment of the circuitry on the encoder matching module.

Required voltage	Circuitry setting ①	
	R5 (3 W)	R12
+ 5 V/0.2 A	180 Ω	33 kΩ
+ 12 V/0.2 A ②	330 Ω	91 kΩ
+ 15 V/0.2 A	330 Ω	120 kΩ

① **See layout of encoder matching module 1 absolute** (Excess–3 gray code) (see **section 4,3.7).**
② **Condition as delivered.**

4.3.4 Connector Pin Assignment

Assignment of the sub D connector pins (channel 1 or 2)

1	18	34 Change signal
2	19	35
3	20	36
4	21	37
5	22	38
6	23104 D	39
7 10^4 c	24 10^4A	40104 B
8103 D	25103 B	41 10^3 c
9 10^3 A	26102 C	42102 D
10102 B	27 10 I D	43 10^2A
11 10' c	28 10^1 A	44 10 I B
12 10° D	29 10° B	45 10'J c
13 10^0 A	30	46
14	31	47
15	32 i- 5 V/12 V/15 V	48+ 5 V/12 V/75 V
16	33 M	49 + 24 V (Input)
17 M		50 M

Pins 32/48 and pins 17/33/50 are parallel and can be used alternatively

If decades are not used, the pertinent signal lines must be permanently preset via the front connector pins. Jumpers must be soldered in accordance with the gray code: A connection to the supply voltage means"1"; a connection to M means "O".

Example: 10^4 not available (12 V signal voltage)

Jumper (12 V) Pin 48 with pin 40
Jumper (M) Pin 33 with pin 23 and 24
Pin 17 with pin 7

Connections 10^4 :

	D	C	B	A
----------			↕	
----------	0			0
----------		0		
Leading "O"	0	0	1	0

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4.3.5 Code Table

CONNECTIONS	Excess-3 Gray Code 10^3 DCBA	10^2 DCBA	10^1 DCBA	10^0 DCBA	BCD Representation
TABLE EVEN	0010	0010	0010	0010	0000
	0010	0010	0010	0011	1
	0010	0010	0010	0111	2
	0010	0010	0010	0101	3
	0010	0010	0010	0001	4
	0010	0010	0010	1001	5
	0010	0010	0010	1101	6
	0010	0010	0010	1111	7
	0010	0010	0010	1011	8
	0010	0010	0010	1010	9
TABLE ODD	0010	0010	0011	1010	10
	0010	0010	0011	1011	11
	0010	0010	0011	1111	12
	0010	0010	0011	1101	13
	0010	0010	0011	1001	14
	0010	0010	0011	0001	15
	0010	0010	0011	0101	16
	0010	0010	0011	0111	17
	0010	0010	0011	0011	18
	0010	0010	0011	0010	19
	0010	0010	0111	0010	20
	0010	0111	1011	0111	0282
Example:	0010	0111	1010	0111	0297
	0 = G	2 = G	9 = U	(1)7 = U	

The module converts the Excess-3 Gray code to BCD.
The internal conversion the number of the preceding decade defines in which table the value for the next decade is found.
If the BCD result is odd, the table "U" odd is used.
If the BCD result is even, the table "G" even is used.
The start is made at the highest digit of the even "G" table.

The prefix (1) is not evaluated.

The above table allows direct connection of a Philips glass scale or of an encoder with the same connection allocation within all applied decades.

If the table for the encoder used deviates from the above table, seethe recommended solution on the next page.

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4.3.6 Encoder with Deviating Code

10^2 DCBA	10^1 DCBA	10^0 DCBA	BCD
0010	0010	0010	0
0010	0010	0110	1
0010	0010	0111	2
0010	0010	0101	3
0010	0010	0100	4
0010	0010	1100	5
0010	0010	1101	6
0010	0010	1111	7
0010	0010	1110	8
0010	0010	1010	9
0010	0110	1010	10
0010	0110	1110	11
0010	0110	1111	12
0010	0110	1101	13
0010	0110	1100	14
0010	0110	0100	15
0010	0110	0101	16
0010	0110	0111	17
0010	0110	0110	18
0010	0110	0010	19
0010	0101	0010	20
0111	1110	0111	0282
0111	1010	0111	0297

The comparison with the absolute encoder matching module 1 table shows that 10 A^x and 10 C^x are reversed in all decades.

Recommended solution:

1.) The encoder connections 10A are reversed for each decade with the connections 10^xC at the sub D connector.

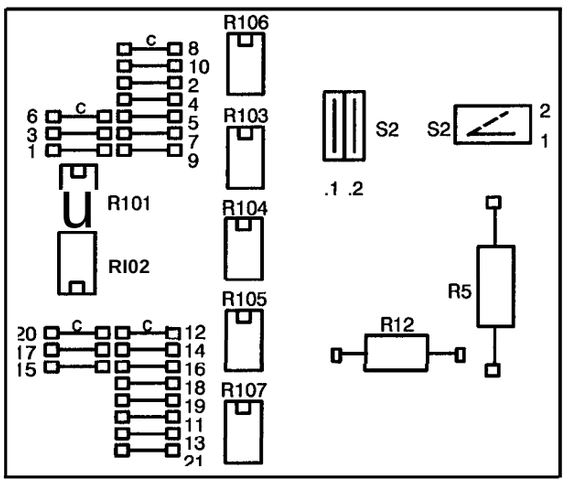
Example: Reverse pin 13 with pin 45.

2.) in all unused decades, 10^xA, 10^xC and 10^xD must be connected to ground!

3.) In all unused decades, 10^xB, should be connected to "+" (e.g., 12 V signal voltage to pin 48 of the sub D connector).

Solutions 2) and 3) offer the module the sample 0010 for a "O" setting in the most significant decade.

4.3.7 Layout



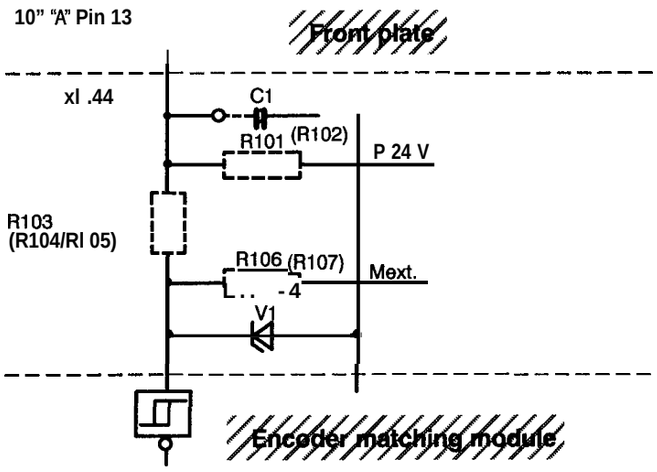
C Corresponds to the capacitors CI to C21

The layout shows the position of the configurable elements, jumpers, and switches.

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4.3.8 Switch Diagram of the Input Amplifiers



The voltage at the respective Schmitt-Trigger (i.e., via R1060r R107), must be < 0.8 V for the low level and a minimum of 3 V or a maximum of 5 V for the high level!

4.3.9 Component Sets (Excess–3 Gray, 6ES5 271–IACII)

Encoder Supply Voltage	Components	Quantity	Value	Designation
+5 v	R5 R12	1 1	180 Ω 33 kΩ	W21 B54311
+15 v	R5 R12	1 1	330 Ω 120 kΩ	W21 B54311
Input Voltage Range				
5 V	R103 toR105	3	Wire jumpers	Augat connector 614DG6
15 v	R103 toR105 R106/Rl 07	3 2	899–3–R 3.3 K 899–1 –R 1.5 K	Resistor network Resistor network
24 V	R103 toR105 Rl 06/R107	3 2	899–3–R K① 899–1 –R 1.5 K	Resistor network Resistor network
OPEN COLLECTOR	R101/R102 R103 to Rl 05 R106/Rl 07	2 3 2	899–1 –R 8.2 K Wire jumpers 899–1 –R 1.5 K	Resistor network Augat connector 614DG6 Resistor network

① In accordance with the encoder impedance; available at WKF.

The component set allows per channel conditioning of Excess–3 gray encoders for the IP 241. The set contains the above items and a Cannon connector.

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5 Matching Module 2 for Absolute Encoders (BCD/BINARY)

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5,3.2 Conditioningthe InputLevels 5–3
5.3.3 Setting the Encoder PowerSupply 5–5
5.3.4 ConnectorPinAssignment 5–5
5.3.5 Layout 5–6
5.3.6 Switch Diagram of the Input Amplifiers 5–6
5.3.7 ComponentSets (BCD/Binary, 6ES5 271 – 1AD11) 5–7

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5.1 Function Description

The arriving actual values (BCD or binary) are converted to TTL level by signal conditioning. These values are transferred to the output memory and made available to the basic module.

This transfer is time delayed and only takes place at each change of the least significant data bit (A0). When the output memory of µP of the basic module is scanned, no transfer takes place.

In order to obtain short processing times, process the actual values and the setpoints in the same format. See section 5.3.1.

Encoders with the following code types can be connected:
BCD maximum representation range O – 99999
Dual (binary) maximum representation range O – 99999[1]
Dual (binary) maximum representation range O – FFFFF[2]

[1] Switch S1.1 open and S1.2 closed (see section 5.3.1): the binary values are converted on the basic module.

[2] Switch S1.1 and S1.2 closed (see section 5.3.1): the binary values are processed further without conversion.

An adjustable time delay insures the acquisition of all bits which have changed. This delay time must be adapted to the maximum encoder frequency.

The delay time should be less than or equal to half the interval between two pulses at maximum encoder frequency.

By increasing C21 on the module, the delay can be increased.

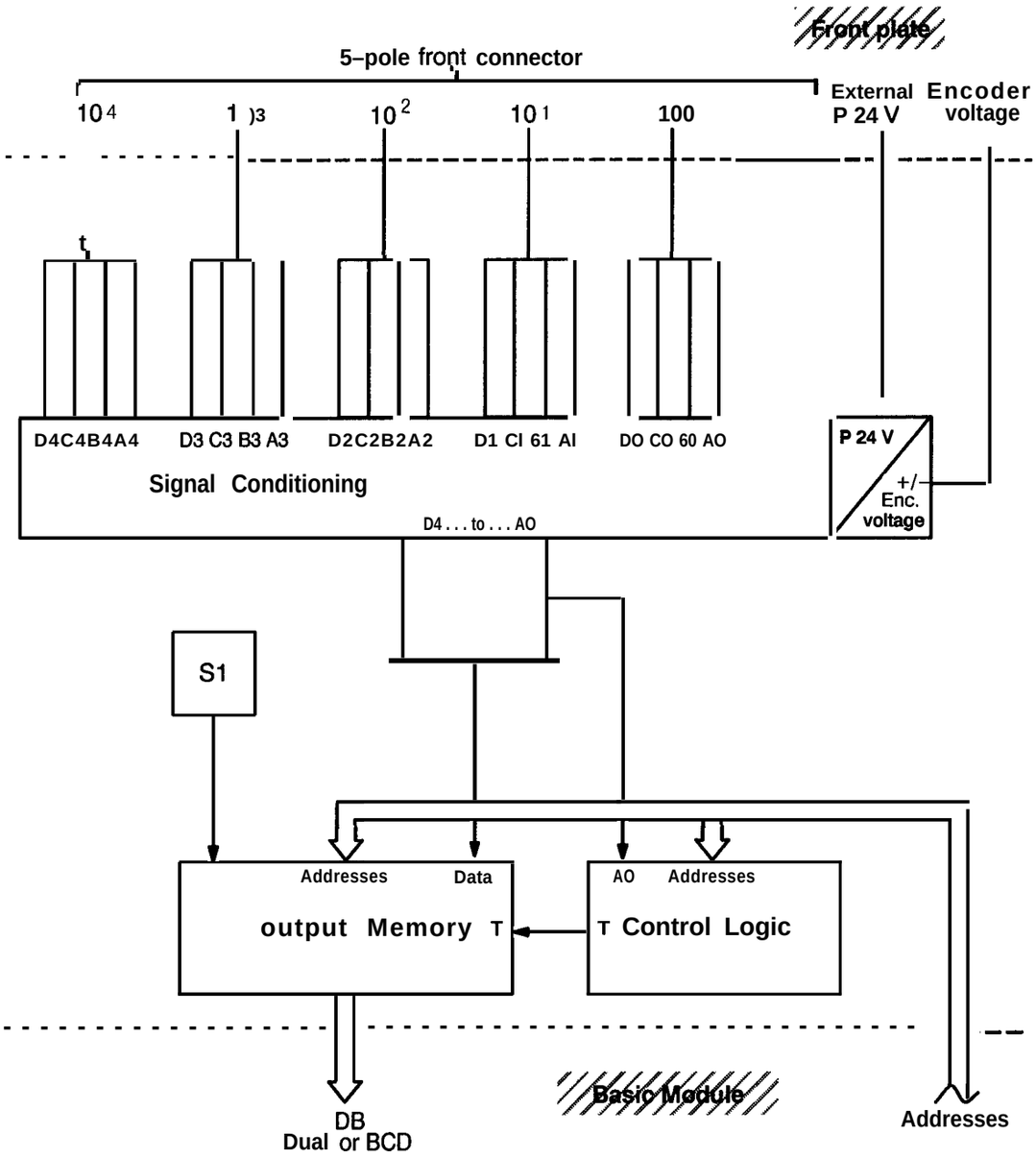
State as delivered: 50 kHz = 10 µsec delay (i.e., C21 = 3.3 nF).

Example: --t maximum encoder frequency f = 1666 Hz
→ Interval I/f = 600 µsec
--t half interval = 300 µsec
-t C21 = 30x 3.3 nF = 100 nF

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5.2 Block Diagram



"The actual current value is immediately taken over after power is switched on if both module and encoder are turned on at the same time. If the encoder is turned on later, however, the current value can assume undefined states and is not taken over correctly until the AO position is changed.
if pseudo –tetrades occur, then the encoder signal maybe too slow.
Correction: Match delay with C21.
Watch out for correct settings in accordance with section 5.3.1.

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5.3 Putting into Operation

5.3.1 Setting the Operating Mode

	DIP switch S1 Contact 1	Contact 2	Typical . processing time
Absolute BCD encoder and BCD parameterization of the setpoints	closed	closed	1 msec.
Absolute binary encoder (maximum of 17 bits) and BCD parameterization of the set–points (conversation by the µP of the basic module)	open	closed	3 to 13 msec. (higher resolu–tion = increased time)
Absolute binary encoder (maximum of 20 bits) and bi–nary parameterization of the setpoints	closed	closed	1 msec.

5.3.2 Conditioning the Input Levels

Input voltage (from the BCD/binary encoder signal voltage)	C1 to C20 10 nF	R101/R102 Resistor network (joint point)	RI 03/R104/R105 Resistor network (sinale resistor)	R106/R107 Resistor network (ioint point)
5“	as required	omitted	Wire jumpers	omitted
12V	as required	omitted	899-3-R2K	899–1 –R 1,5 K
15 v	as required	omitted	699=3-R 3,3 K	899-1 –R 1,5 K
24 V	as required	omitted	899–3–R ? K①	899-1 –R 1,5 K
Open Collector	as required	899–1 -R 8,2 K	Wire jumpers	899-1 -R 1,5 K

① The resistance value depends on the encoder output impedance. See nol on next page.

Small disturbances that occur in spite of correct wiring and shielding can be corrected with the capacitors Cl to C20.

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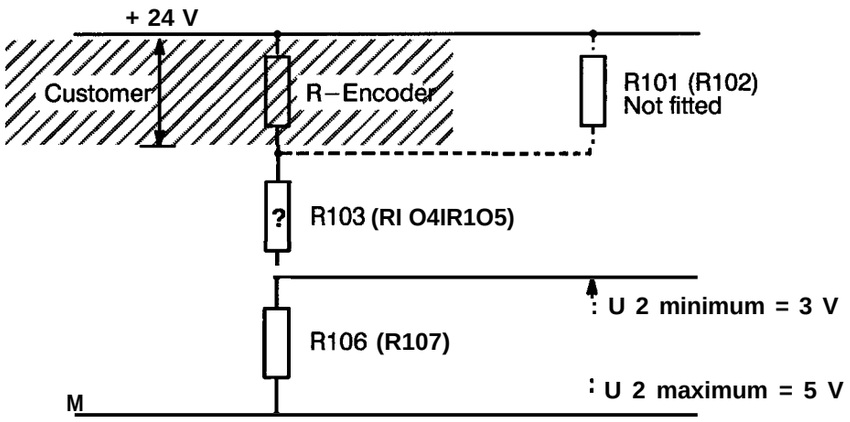
Instructions for conditioning the input circuitry

– In the encoder impedance range from 6 kΩ to 10 kΩ, wire jumpers can be inserted for R103, R104, R105.

– Below 6 kΩ encoder impedance, the resistor networks must be individually computed.

– The high level at R106 or R107 must be between 3 V and 5 V.

– The low level at R106 or R107 must be below or equal to 0.8 V.



$$R = \frac{R2 \times (U - U2)}{U2} - R\text{–Encoder}$$

Explanation:

R = R103, R104, R105
R2 = R106, RI 07 (1 .5 kΩ)
U2 = Voltage at R106, R107 (min. 3 V, max. 5 V)
u = Encoder voltage (24 V)
R–Encoder = Encoder impedance (see label or data sheet)

How to proceed:

a) Compute the value R max. with U2 min. (3 V)
b) Compute the value R min. with U2 max. (5 V)
c) Select the resistor network according to E–series (between R max. and R min.)

Only resistor networks consisting of single resistors maybe used.
See the technical specifications, section 8.6.

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5.3.3 Setting the Encoder Power Supply

The required encoder supply voltage must be provided by suitable adjustment of the circuitry on the absolute encoder matching module 2 (BCD/binary).

Required voltage	Circuitiry setting ①	
	R13 (3W)	R20
+ 5 V/0.2 A	180 Ω	33 kΩ
+ 12 V/0.2 A ②	330 Ω	91 kΩ
+ 15 V/0.2 A	330 Ω	120 kΩ
+ 24 V/2A corresponds to external system voltage from Faston connector		
	R5	R4
- 5 V/0.5 A ②	82 Ω	51 kΩ
– 12 V/0.2 A	330 Ω	120 kΩ
– 15 V/0.16 A	330 Ω	150 kΩ
– 24 V/0.1 A	470 Ω	240 kΩ

① See BCD/binary layout, section 5.3.5.
② State as delivered

A current limiter for 0.2A is available for the positive supply.

5.3.4 Connector Pin Assignment

Pin assignment of the sub D connector (channel 1 or 2)

1	18	34
2	19	35
3	20	36
4	21	37
5	22	38
6	232 19/ 10⁴D	39
7 2 ls 10⁴c	242 16/ 10⁴A	402 17/ 10⁴B
82 15 10³D	252 13/ 10³B	41 2 14/10³ c
9212 10³A	262 ⁽⁰/ 10² C	422 11/ 10²D
102 9 10²B	272 7/10¹ D	432 8/ 10²A
112 6 10¹C	282 4/10¹ A	442 s/ 10¹ B
122 3 10⁰D	292 1/10⁰ B	452 2/10⁰ c
132 0 IO°A	30	46
14	31	47
15 –5 V/–12 V/–15 V/ –24 V	32 +5 V/12 V/15 V	48 + 5 V/12 V/15 V
16 –5 V/–12 V/–15 V/ –24 V	33 M	49 + 24 V (Output!)
17 M		50 M

Unused inputs must be connected to ground (M–potential)!

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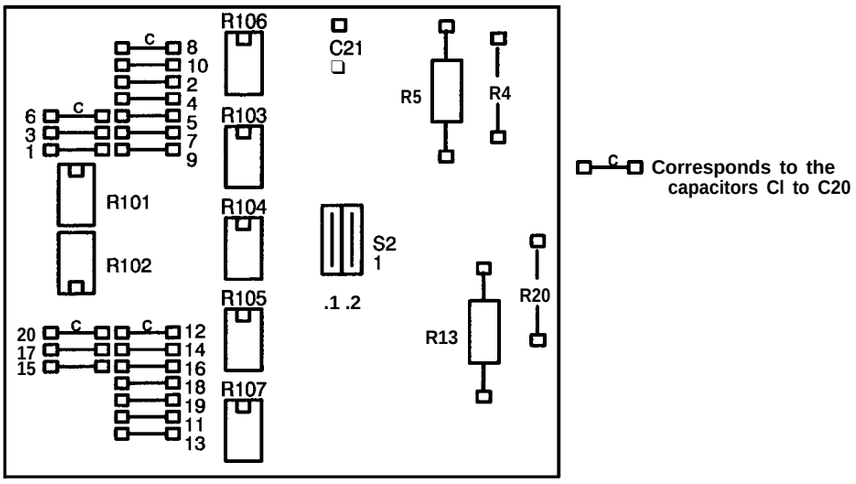
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Pins 15/16 and pins 32/48 as well as pins 17/33/50 are parallel and can be used alternatively.

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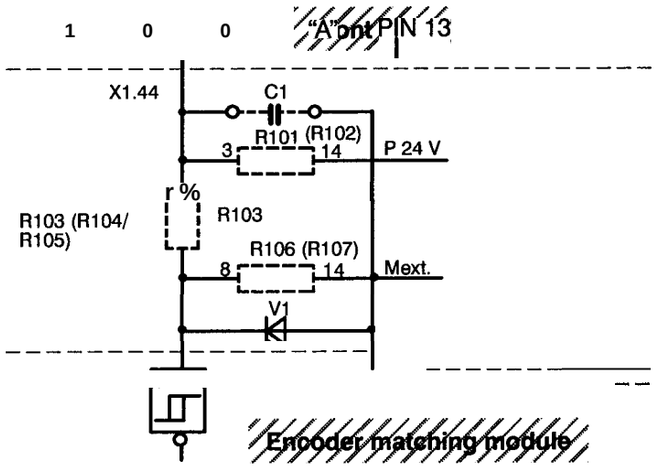
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5.3.5 Layout



The layout shows the configurable elements, jumpers, and switches.

5.3.6 Switch Diagram of the Input Amplifiers



The voltage at the respective Schmitt Trigger (i.e., via R106 or R107) must be < 0.8 V for low level and a minimum of 3 V or a maximum of 5 V for high level!

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5.3.7 Component Sets (BCD/Binary, 6ES5 271–1AD11)

Encoder Supply Voltage	Components	Quantity	Value	Designation
+12 V	R13 R20	1 1	330 Ω 91 kΩ	W21 B54311
+15 V	R13 R20	1 1	330 Ω 120 kΩ	W21 B54311
–12 V	R5 R4	1 1	330 Ω 120 kΩ	W21 B54311
–15 V	R5 R4	1 1	330 Ω 150 kΩ	W21 B54311
–24 V	R5 R4	1 1	470 Ω 240 kΩ	W21 B54311
Input Voltage Range				
12 V	R103 toR105 R106/RI 07	3 2	899–3–R 2 K 899–1 –R 1.5 K	Resistor network Resistor network
15 V	R103 to R105 R106/RI 07	3 2	899–3–R 3.3 K 899–1 –R 1.5 K	Resistor network Resistor network
24 V	R103 toR105 R106/RI 07	3 2	899–3–R K① 899–1 –R 1.5 K	Resistor network Resistor network
OPEN COLLECTOR PNP	R101/R102 R103 to RI05 R106/RI 07	2 3 2	899–1 –R 8.2 K Wire jumpers 899–1 –R 1.5 K	Resistor network Augat connector 614DG6 Resistor network

① In accordance with the encoder impedance, available at WKF.

The component set allows per channel conditioning of BCD/binary encoders for the IP 241. The set contains the above items and a sub D connector.

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6 Matching Module 3 for Absolute Encoders (Analog)

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6.3.5 ComponentSets (Analog, 6ES5 271–1AE11) 6–6

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6.1 Function Description

This module is capable of converting input voltages or currents into a 10–bit binary value (Oto 1023) plus sign.

Thus the maximum representable range covers + 1023 to –1023.

The measured value is amplified accordingly or converted from current into voltage (0 V to 10 V).

This voltage which may be positive or negative, is rectified for the ADC and the sign is derived. This ADC is continuously started by a free–running clock pulse generator and initiates transfer to the output memory with its ready signal.

This transfer operation is disabled while the memory is being scanned by the basic module.

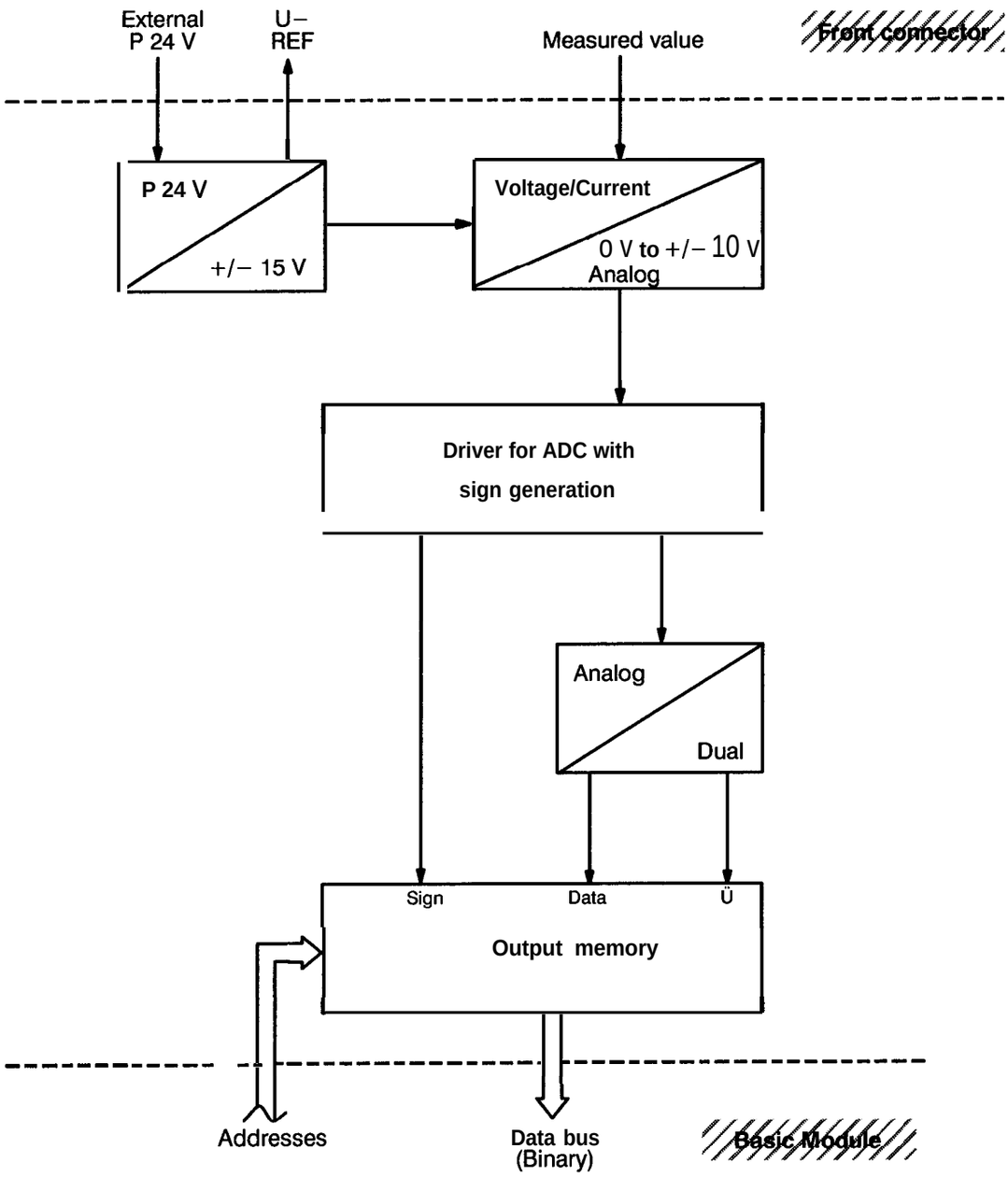
A reference voltage of + 10 V is generated and is available at the front connector.

The operating mode “rotary axis” is not possible with this module. This must be considered under all circumstances when parameters are assigned for the IP 241!

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6.2 Block Diagram



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6.3 Putting into Operation

6.3.1 Parametrizing the Hysteresis

When the IP 241 is operated with the matching module (analog) 3 for absolute encoder, depending on the ripple of the voltage applied, fluctuations of the actual values may occur.

In order to correct this deficiency (starting with firmware version V7.0), a hysteresis value can be preset as follows:

1. Presetting the data block (IP 241) by using the standard function block

DW 177	Enable channel 1		Enable channel 2	
DW 178	10‘	10°	10’	10°

The hysteresis values in DW 178 are given in BCD code.

If the enables for channel 1 (DL 177) or channel 2 (DR 177) are set with KH = FF, the hysteresis value of the respective channel is not transferred to the module.

2. Parameterization of the module by FB 156

After presetting the DB (IP 241), the standard function block FB 156 is usually called in case there is a new start.

3. For a parameter assignment without the standard function block proceed as follows:

1. Specify the channel number by entering the track number into byte O

   (module address + O)
   Track O to 15 corresponds to channel 1
   Track 16 to 31 corresponds to channel 2

2. Specify the hysteresis value (00 to 09) by entry into byte 1 (module address +1).

3. Byte 2 and byte 3 remain free.

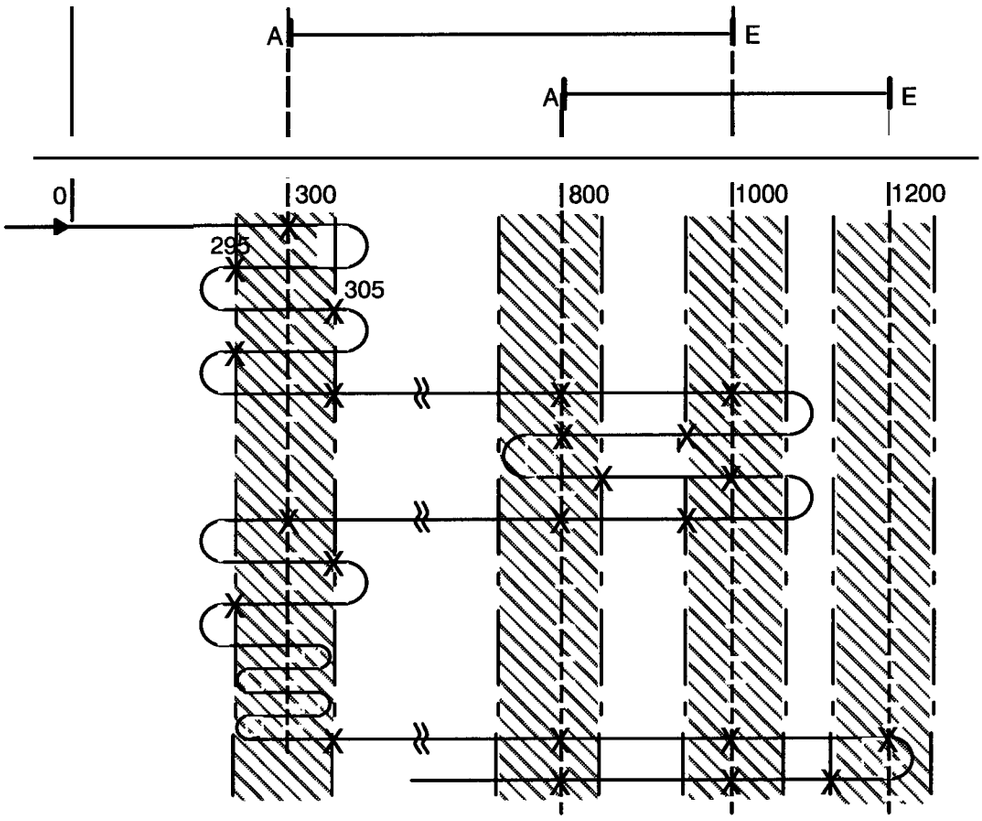
4. Enter the identifier F1 (Hex) into byte 4 (module address +4) to activate the hysteresis.

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Hysteresis Specification

Assumed track distribution:

A = Startingvalues
E = End values
05 = Hysteresis value



An actual value fluctuating within the hysteresis limits will cause only one interrupt, when it reaches a switching point.

All switching points which are reached in one traversing direction cause the exact triggering of an interrupt. When the direction is reversed, the switching point is shifted by the hysteresis value! Then the value is exact again.

Accordingly, high hysteresis values entail high losses of accuracy.

The lowest parameterized track value must exceed the hysteresis value.

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6.3.2 Matching the Measured Value Ranges

Measuring range	Circuitry ①		
	R29	R30	R31
+/– 100 mV	1 kΩ 1%	1 kΩ 1%	100 kΩ 1%
+/–1 V	10 kΩ 1%	9,1 kΩ 1%	100 kΩ 1%
+/– 10 V ②	10 kΩ 1%	5,1 kΩ 1%	10 kΩ 1%
+/– 20 mA	25 Ω 1%	18 Ω 1%	500 Ω 1%

① See layout plan for analog module, section 6.3.4.
② State as delivered.

The reference voltage of + 10 V/0.1 A is available at pin 18 of the front connector.

The input impedance at pin 1 corresponds to R29.

6.3.3 Connector Pin Assignment

Assignment of the sub D connector pins (channel 1 or 2)

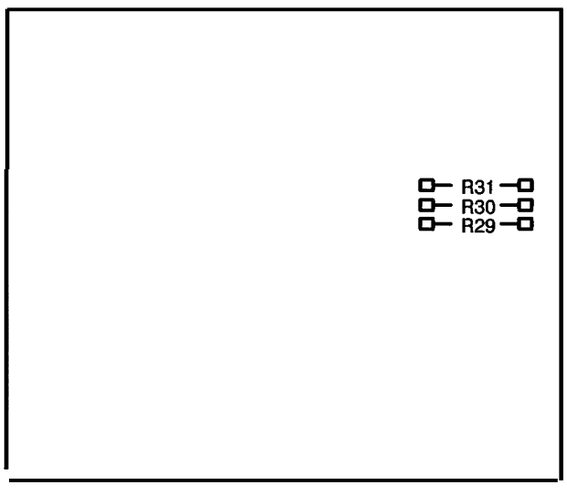
1 U or I (+) connection	18 + 10 V Reference voltage	34
2 Ground reference voltage	19	35 U or 1 (–) connection
3	20	36
4	21	37
5	22	38
6	23	39
7	24	40
8	25	41
9	26	42
10	27	43
11	28	44
12	29	45
13	30	46
14	31	47
15	32	48
16	33 M	49
17 M		50 M

Pins 17/33/50 are parallel and thus can be used alternatively.

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6.3.4 Layout of the Matching Elements



The layout shows the configurable elements.

6.3.5 Component Sets (Analog, 6ES5 271–IAEII)

Measuring range	Components	Quantity	Value	Designation
100 mV	R29, R30	2	1 kΩ	1% B54311
	R31	1	100 kΩ	1% 654311
1 V	R29	1	10 kΩ	1% 654311
	R30	1	9.1 kΩ	1% B54311
	R31	1	100 kΩ	1% B54311
20 mA	R29	1	25 Ω	1% B54311
	R30	1	18 Ω	1% B54311
	R31	1	500 Ω	1% B54311

The component set allows per channel conditioning of analog value encoders for the IP 241. The set contains the above items and a Cannon connector.

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7 Matching Module 4 for Absolute Encoders (Synchronous-Serial)

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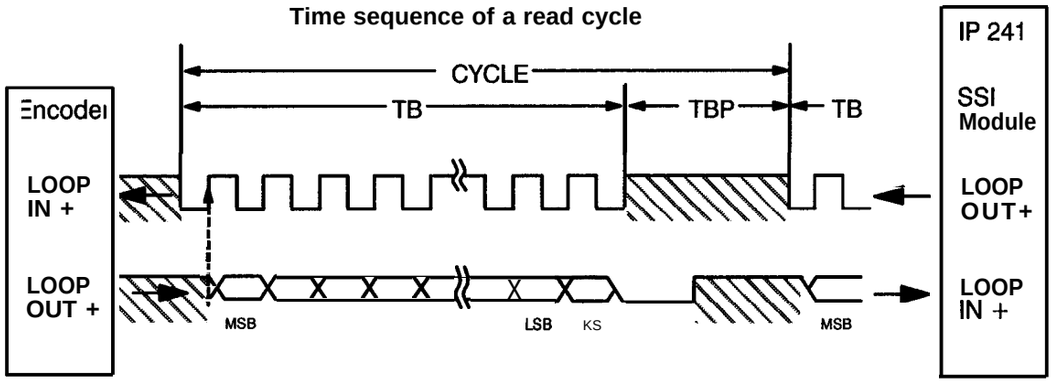
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7.1 Function Description

The serial actual values of an encoder with synchronous–serial interface according to RS 485 or RS 422 are converted to parallel information on the encoder matching module and are transferred to the output memory of the basic module.

Time sequence of a read cycle



LOOP	OUT +	=	OUTPUT "+ " SEND CLOCK PULSE GROUP
LOOP	IN +	=	INPUT "+" ACTUAL ENCODER VALUE
TB		=	CLOCK PULSE GROUP (NUMBER OF CLOCK PULSES) parameterizable
TBP		=	CLOCK PULSE GROUP INTERVAL (DEFINED BY HARDWARE)
MSB		=	MOST SIGNIFICANT BIT
LSB		=	LEAST SIGNIFICANT BIT
KB		=	CONTROL BIT

The encoder matching module fetches the actual encoder values by cyclic emission of a clock pulse group (TB) and transfers them to the basic module via the output memory.

A clock pulse group is a package of single pulses.
The number of clock pulses in a clock pulse group depends on the encoder resolution.

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See the following table for the number of clock pulses (parameter TB).

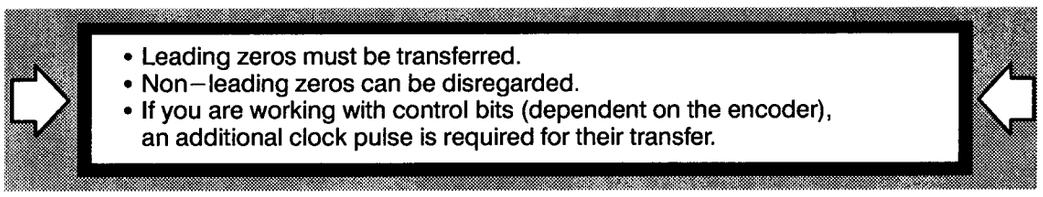
		Data Word with 25 Bits →																									
		MSB	Bit Number in the Data Word																						LSS		
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
4096	12	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	8192	13
2048	11	0	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	0	4096	12
1024	10	0	0	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	0	0	2048	11
512	**9**	**0**	**0**	**0**	**M9**	**M8**	**M7**	**M6**	**M5**	**M4**	**M3**	**M2**	**M1**	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	0	0	0	1024	10
256	8	0	0	0	0	M8	M7	M6	M5	M4	M3	M2	M1	S9	S8	S7	S6	S5	S4	S3	S2	S1	0	0	0	0	512	9
128	7	0	0	0	0	0	M7	M6	M5	M4	M3	M2	M1	S8	S7	S6	S5	S4	S3	S2	S1	0	0	0	0	0	256	8
64	6	0	0	0	0	0	0	M6	M5	M4	M3	M2	M1	**S7**	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**	**0**	**0**	**0**	**0**	**0**	**0**	128	7
32	5	0	0	0	0	0	0	0	M5	M4	M3	M2	M1	S6	S5	S4	S3	S2	S1	0	0	0	0	0	0	0	64	6
16	4	0	0	0	0	0	0	0	0	M4	M3	M2	M1	S5	S4	S3	S2	S1	0	0	0	0	0	0	0	0	32	5
8	3	0	0	0	0	0	0	0	0	0	M3	M2	M1	S4	S3	S2	S1	0	0	0	0	0	0	0	0	0	16	4
4	2	0	0	0	0	0	0	0	0	0	0	M2	M1	S3	S2	S1	0	0	0	0	0	0	0	0	0	0	8	3
2	1	0	0	0	0	0	0	0	0	0	0	0	M1	S2	S1	0	0	0	0	0	0	0	0	0	0	0	4	2
No. of turns	Bit/turn	Multi–turn bits												Single–turn bits													Steps/turn	Bit/turn

Example: **Encoder data: Resolution 128**
Multi–turn operation with 512 rotations

An actual value is transferred with the following bits.

Leading zeros: 3
Multi–turn: 9
Single–turn: 7
19 bits

A clock pulse group with 19 clock pulses is required.



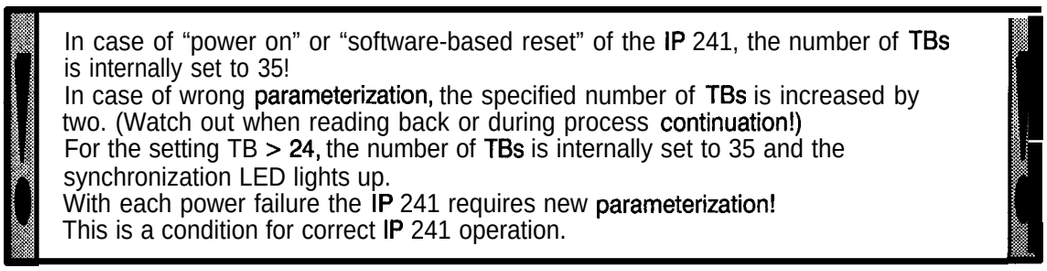
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After turning on, the synchronization LED of the respective channel lights up until the clock pulse group has been transferred to the module. The parameterTB can be transferred in BCD code from the programmable controller, following the example for parameter assignment.

By means of the standard function block, direct specification of the clock pulse groups is possible.

The parameters are transferred from the basic module to the parameter memory of the encoder matching module.

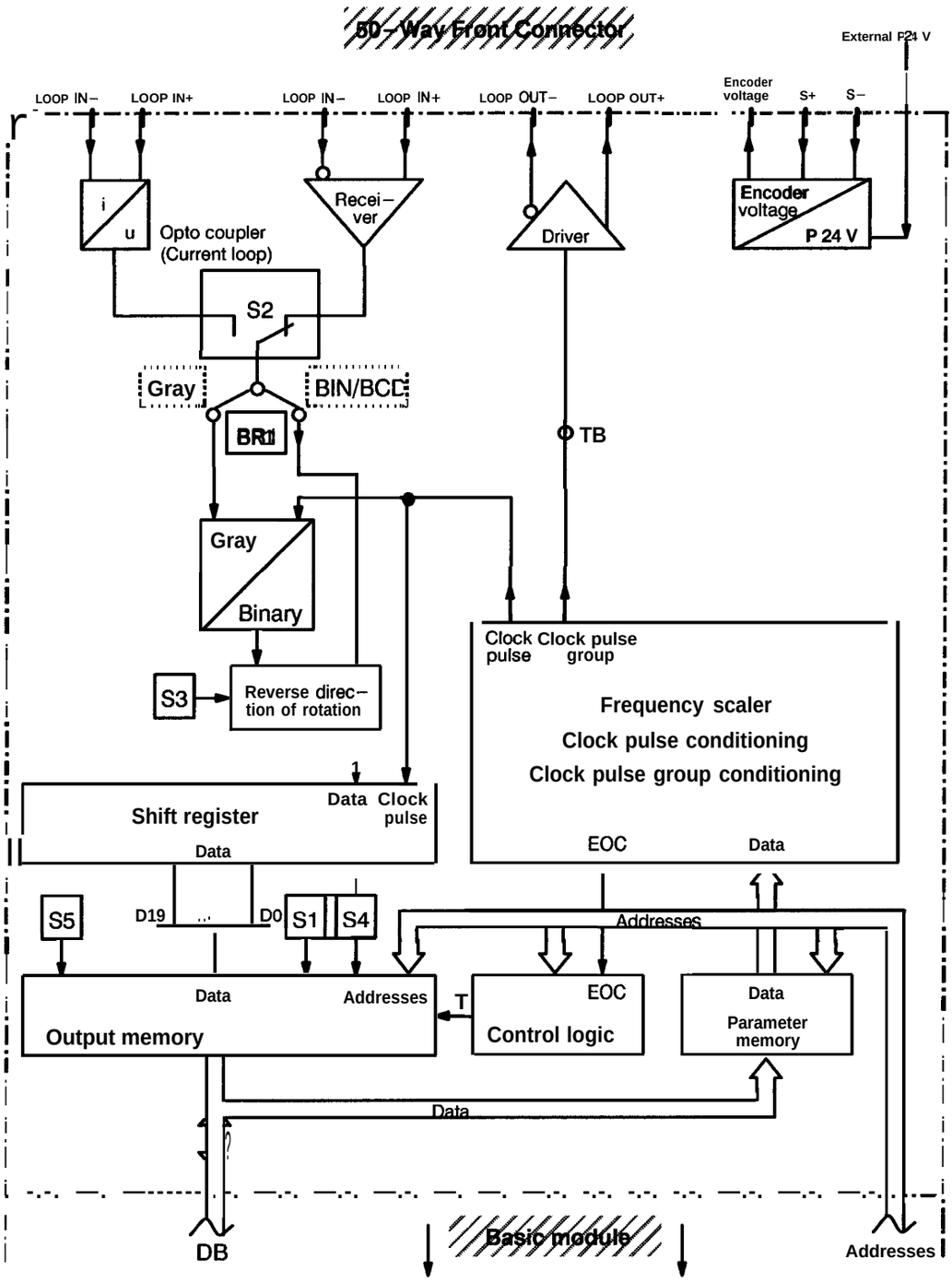


In case of “power on” or “software-based reset” of the IP 241, the number of TBs is internally set to 35!
In case of wrong parameterization, the specified number of TBs is increased by two. (Watch out when reading back or during process continuation!)
For the setting TB > 24, the number of TBs is internally set to 35 and the synchronization LED lights up.
With each power failure the IP 241 requires new parameterization!
This is a condition for correct IP 241 operation.

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7.2 Block Diagram



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7.3 Putting into Operation

Components required:

**Basic module IP 241 (order no.6ES5 241 –IAA11) firmware version A07 or later,
Absolute encoder matching module 4 synchronous–serial
(order no. 6ES5 241 -I AF11) -1 each per channel
Component set absolute 4 synchronous–serial
(order no. 6ES5 271–IAF1I) – 1 each per channel
External voltage supply 24 V (Connection to the Faston connector on the basic module)**

The following settings need to be checked and adjusted if necessary:

- **Shielding (interference suppression)**
- **Encoder supply voltage (resistor R31)**
- **Sense line on encoder connected or open (see 7.3.5)**
- **Selection of input signal interface (via receiver or opto coupler/switch S2)**
- **Wave resistance R2 for operation via receiver**
- **Code setting for encoder (jumper BR1)**
- **Control bit setting (switches S4 and S1)**
- **Actual value transfer mode to the PLC (switches S5.1 and S5.2)**
- **Presetting the number of clock–pulse groups (TB) via the standard function block or according to parameterization example**

7.3.1 Setting the Operating Mode

7.3.1.1 General

COMMENT TO SWITCH "S5"!

The switches "S5.1" and "S5.2" ARE SCANNED BY THE BASIC MODULE ONLY! The switch positions inform THE BASIC MODULE ALONE whether the software-based BCD conversion is to be quick or slow and/or whether no dual (binary) to BCD conversion is to take place at all!

In order to obtain short processing times, it is recommended that you work with the following formats:

Actual values	Setpoints	Jumper BR1 encoder matching module	S5.1	S5.2
Gray Code	Binary	Position "Gray"	Closed	Closed
Binary	Binary	Position "BIN/BCD"	Closed	Closed
BCD	BCD	Position "BIN/BCD"	Closed	Closed

This eliminates the conversion times on the basic module (i.e., no BCD conversion takes place there).

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Up to an encoder resolution of 17 bits maximum, the basic module can execute a software-based binary/BCD conversion (maximum 99999 BCD). This makes it possible to specify setpoints in BCD code. Consider conversion time on the basic module.

DIP switch encoder matching module	S5.1 closed	S5.2 open

With an encoder resolution between 18 and 20 bits no binary/BCD conversion is executed on the basic module. Therefore, the setpoints must be specified in binary code (maximum FFFFF).

DIP switch encoder matching module	S5.1 closed	S5.2 closed

Up to an encoder resolution of 10 bits maximum, an expedited binary/BCD conversion can be executed on the basic module.

DIP switch encoder matching module	S5.1 open	S5.2 open



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7.3.1.2 Gray Code

Maximum resolution = 20 bits + 1 control bit

Encoders with a higher resolution, indicating the respective number of TBs, can be also connected, but the module will only evaluate up to 20 bits (Fault message by sign–bit VZ = 1 (i.e., overflow + synchronization bit = O).

The actual values from the gray code encoder are converted to binary code on the encoder matching module and are transferred to the basic module via the output memory (Solder in jumper BR1 for "Gray").

Offset value K must be considered for encoders with symmetrically capped gray code. The offset value is calculated as follows:

$$K = \frac{2^n - s}{2}$$

n = Number of bits required to represent the maximum desired binary number (e.g., 9 bits for the number 359)
s = Desired step number (e.g., O to 359 = 360 steps)

Our example has an offset value of

$$K = \frac{2^9 - 360}{2} = \frac{512 - 360}{2} = 76.$$

Thus, the encoder will give the value 76 instead of "zero". The area end value is then 76 + 359 = 435.

Encoders with an additional control bit can be evaluated if the control bit is transmitted in the last position (after the LSB) (see "The Time Sequence of a Read Cycle" example in section 7.1).

7.3.1.3 BCD Code

Maximum resolution = 5 decades + 1 control bit

Without being converted on the encoder matching module, the actual values are directly transferred to the basic module via the output memory. (When their setpoints are presented in binary code, the processing time of the basic module must be taken into account.) Solder in jumper BR1 for "BCD/BIN".

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7.3.1.4 Binary Code

Maximum resolution = 20 bits + 1 control bit

Without being converted on the encoder matching module, the actual values are directly transferred to the basic module via the output memory (when setpoints are presented in BCD code, the processing time of the basic module must be taken into account). Solder in jumper BR1 for "BCD/BIN".

7.3.2 Setting the Encoder Power Supply

The required encoder supply voltage must be provided by circuitry of resistor R31 on the absolute encoder matching module.

Required voltage	R31 Circuitry ①	Pin No.
+5 V/1 A ② ③	1.3 kΩ MBB 0207	32/48
+ 12 V/1 A ③	4.3 kΩ MBB 0207	32/48
+ 15 V/I A ③	5.6 kΩ MBB 0207	32/48
+ 24 V/2 A	No change required as the 24 V supply is furnished directly via a line from the Faston connector on the basic module.	49

① See layout of the SS1 submodule in section 7.3.8.
② State as delivered

③

A circuiting of the sense outputs with a suitable encoder is required here or the sense(+) and sense(−) outputs must be left open. Do not connect sense(+) and sense 1 to ground or the encoder power supply since these voltages can otherwise increase (up to 18 V).

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7.3.3 Select Direction of Rotation (for Gray or Binary Code)

Direction of rotation right (cw = clockwise)

When the encoder rotates in a "right-hand" direction (i.e., clockwise with the shaft facing the observer), incrementing actual values are provided if:

Switch S3 

Direction of rotation left (ccw = counterclockwise)

When the encoder rotates in a "left–hand" direction (i.e., counterclockwise with the shaft facing the observer), incrementing actual values are provided if:

Switch S3 

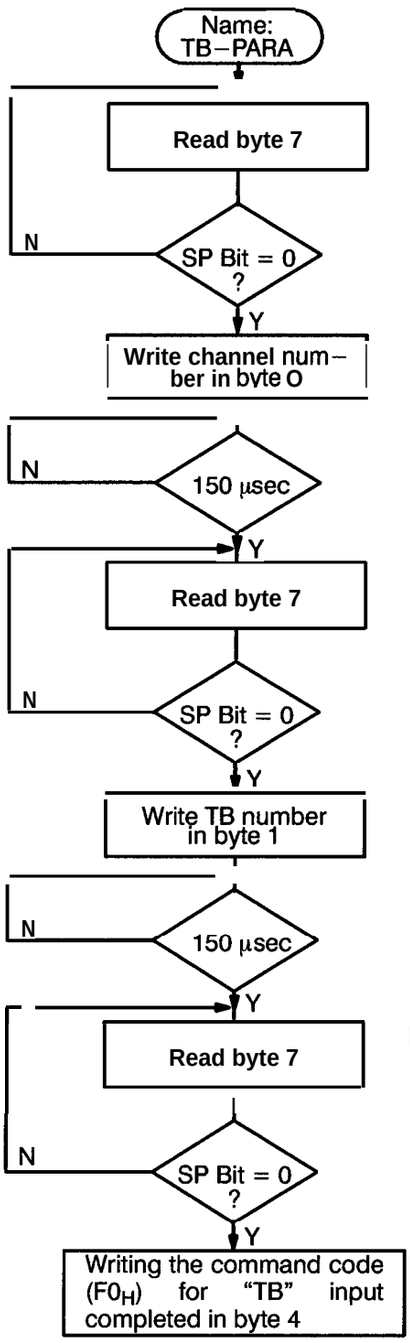
With a resolution of more then 20 bits, a change to counterclockwise rotation is not possible, as the sign bit becomes "1" (internal evaluation in twos' complements).

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7.3.4 Parameterization of Clock Pulse Groups

This procedure is only required when the standard function block is not used.



Name: TB–PARA

Preset: TB = 10
Channel 2
Module address 128

```
M001:  L     PY135      ;Reading byte 7
       T     FY100

       A     F1 00.7    ;Scanning the SP bit
       JC  =  M001

       L     KH0010     ;KHOO1 O corresponds to
       T     PY128       track number 16;
                         Channel 2 is selected

       JC    FB10       ; Enter a delay time of
                         approx. 150 µsec (the
                         processing time for FB1O is
                         approx. 150 µsec

M002:  L     PY135      ;Reading byte 7
       T     FY100

       A     F100.7     ;Scanning the SP bit
       JC  =  M002

       L     KH0010     ;Write number of clock
       T     PY129       pulse groups TB = 10
                         in byte 1

       JC    FB10       ; Enter a delay time of
                         approx. 150 µsec (the
                         processing time for FB1O is
                         approx. 150 µsec

M003:  L     PY135      ;Reading byte 7
       T     FY100

       A     F100.7     ;Scanning the SP bit
       JC  =  M003

       L     KH00F0     ; Writing the command code
       T     PY132       (F0H) for "TB" input
                         completed = OOFO in byte 4
       BE               ;Block end
```


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7.3.5 Instructions for Encoder Connections

The encoders are connected to the 50–way sub D connector of the basic module via a cable with twisted pair conductors, according to RS 422/RS 485 specifications. The encoders can be either connected to the input interface "optocoupler"(i.e., a current loop with approx. 7 mA, or to the input interface "receiver" (set switch S2 accordingly)),

– In case of operation via the optocoupler:

The encoder is supplied via the encoder matching module.With the jumpers A– B and C–D on the basic module, and the grounding connection with the programmable controller, only non-floating operation is possible.

For floating operation, a separate encoder supply is required, galvanically isolated (i.e., without connection to the S5).

– In case of operation via the receiver:

The value of the terminating resistor R2 can be adapted to the wave resistance Zo (see the data sheet of the respective encoder manufacturer) of the cable used.

Floating operation is not possible.

Zo = R2 see RS 485 specifications. The factory setting for Zo = R2 =100 Ω.

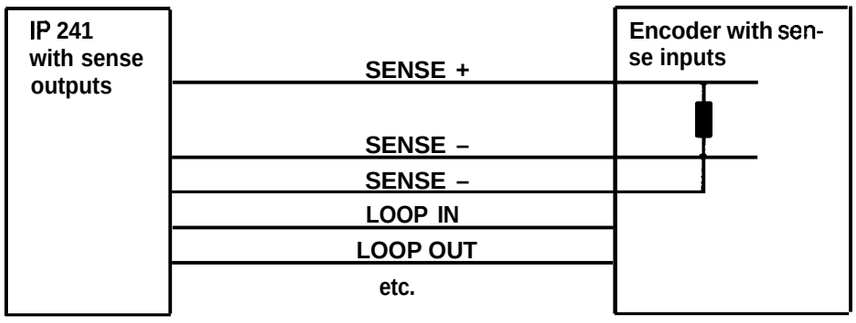
Maximum cable lengths:

The maximum cable length depends on the transfer frequency.

Encoder resolution $\leq$ 10 bits -t transfer frequency=100 kHz → max. cable length 300 m

Encoder resolution > 10 bits → transfer frequency ≈ 200 kHz → max. cable length 150 m

Circuiting of the sense outputs



A circuiting of the sense outputs with a suitable encoder is required here or the sense(+) and sense(–) outputs must be left open. Do not connect sense(+) and sense 1 to ground or the encoder power supply since these voltages can otherwise increase (up to 18 V).

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7.3.6 Fault Messages

By evaluation in the programmable controller, states deviating from normal operation can be recognized.

Normal operation can always be recognized by a synchronization bit set to"1" ("synchronization" LED is not lit up) and a sign bit VZ set to "O".

If the synchronization bit of the IP 241 is set with "O" ("synchronization" LED lights up) and the sign bit VZ is set with "O", then an encoder error has occurred or the control bit polarity has been set wrong! This error can only occur in "operation mode with control bit evaluation" (switch S4 is closed).

If the synchronization bit of the IP 241 is set with "O" ("synchronization" LED lights up) and the sign bit VZ is set with"1", an overflow has occurred!

In the following cases the rotary axis operation mode with the absolute encoder matching module (synchronous serial) is illegal:

- Encoder resolution > 20 bits (overflow)
- Encoder resolution 17 to 20 bits with binary or gray code encoders and BCD conversion setting (see section 7.3.1 .1).
- Software synchronization is illegal for this encoder matching module!

Possible error sources:

Connect only the encoders that can handle the maximum resolution of the respective codes used, in order to avoid some of following errors.

- **After the initial turning on, the number of TBs is missing (the module firmware sets TB = 35)**
- **Loss of parameterization (e.g., the firmware sets TB = 35 in case of power off) until the time of parameter transfer from the programmable controller.**
- **Software reset of the IP 241 (firmware sets TB = 35) until the time the parameter TB is transferred.**
- **A control bit is set on the matching module (S4 closed), but no control bit is output by the connected encoder. (The error message is output independent of a possible overflow.)**
- **The set polarity of the control bit (switch S1) does not match the polarity of the encoder. (The error message is output independent of a possible overflow.)**
- **The control bit is set, but the number of TBs specified is too small.**
- **An overflow occurs (i.e., the sign bit is set with"1 ").**
- **An encoder with more than 20 bits is connected, causing an overflow when the 20 bits are exceeded.**
- **The encoder requires a higher number of clock pulse groups (for TB > 20) than the specified resolution (i.e., internal zeroes are inserted and a wrong direction of rotation is specified (switch S3).**

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7.3.7 Connector Pin Assignment

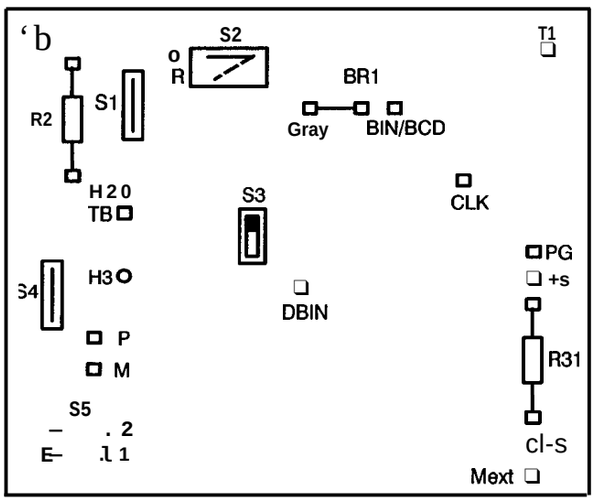
Assignment of the sub D connector pins (channel 1 or 2)

1	LOOP OUT–	18	34
2		19	35 LOOP OUT+
3		20	36
4		21	37
5		22	38
6		23	39
7		24	40
8		25	41
9		26	42
10		27	43
11		28	44
12	LOOP IN+/Opto coupler	29 LOOP IN+/Receiver	45 LOOP IN–/Opto coupler
13	LOOP IN –/Receiver	30 SENSE+	46
14		31	47
15	SENSE–	32 -t- 5 V/12 V/15 V	48 -f- 5 V/12 V/15 V
16	SENSE–	33 M	49 + 24 V Output
17	M		50 M

Pins 15/1 6 as well as pins 32/48 and pins 17/33/50 are parallel and can be used alternatively.

LOOP OUT = Clock pulse group output
LOOP IN = Data input
SENSE+ = Sense(+) output for control of encoder power supply
SENSE– = Sense(–) output for control of encoder power supply

7.3.8 Layout



TB	=	Measuring point for clock pulse groups to the encoder
T1	=	Measuring point for clock pulse from the basic module
CLK	=	Measuring point preprogrammed clock pulse
DBIN	=	Measuring point after gray binary conversion
P	=	Measuring point 5 V supply
M	=	M–potential (ground)
PG	=	Measuring point configured encoder supply
+S/–S	=	Measuring points for sense voltages
HI	=	LED indicates: Enable for transmitting clock pulse groups
H2	=	LED indicates: If continuously lit the input signal is missing.
H3	=	Data flow via opto coupler is available
R2	=	Conditioning resistance (= ripple resistance of cable)
R31	=	Conditioning resistance for encoder power supply

The layout shows the position of the configurable elements, jumpers, and switches.

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7.3.9 Configuration At–A-Glance

Element	As delivered	Function
Jumper BR1		
Gray BCD/BIN	●	Connection to gray code encoders
o - c l Gray BCD/BIN		Connection to encoders with BCD or binary code
Switch S2		Input interface RS 422 or RS 465 with:
Position "R" closed	●	Encoder connection at receiver
Position "O" closed		Encoder connection via current loop (opto coupler)
Switch S3 ①		
in position ↑	●	Incrementing values for encoder shaft in "right" rotation
in position ↓		Incrementing values for encoder shaft in "left" rotation
Switch S4		
open	●	Control bit from encoder not available
closed		Control bit from encoder available
Switch S1		
open	●	Encoder presents fault message "high" for control bit evaluation
closed		Encoder presents fault message "low" for control bit evaluation
Switch S5		Selection of code types for actual encoder values by "BR1" (see section 7.3.1)

S5.1	S5.2		Actual encoder value	Transfer to basic module	Transfer to PLC:
open	open		Gray/Binary < = 10 bits	Binary ② ④ (Quick BCD conv. 1 msec.)	BCD
closed	open	●	Gray/Binary < = 10 bits	Binary ③ ④ (Slow BCD conv. 3) ④	BCD
closed	open	●	Gray/Binary to 17 bits	Binary (Slow BCD conv. 3-13 msec.)	BCD
closed	closed		Gray/Binary > 17 bits	Binary (No BCD conversion possible)	Binary
closed	closed		BCD	BCD	BCD

Resistor R2	100 Ω	Matching as required (see section 7.3.5)
Resistor R31	1.3 k Ω	Matching as required (see section 7.3.2)

Jumper or switch settings deviating from those shown above are illegal!

① Internally a two's complement representation is used; no switch–over during operation!
② Control bit evaluation illegal!
③ Avoid long processing time!
④ BCD conversion can be switched off by closing switches S5.1 and S5.2.

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7.3.10 Component Sets (Synchronous–Serial, 6ES5 271–1AF11)

Encoder Supply Voltage	Components	Quantity	Value	Designation
+12 V	R31	1	4,3 kΩ	MBB0207
+15 V	R31	1	5,6 kΩ	MBB0207

The component set allows the per channel conditioning of synchronous–serial encoders for the IP 241, The set contains the above items and a sub D connector.

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8 Technical Specifications

8.1 Technical Specifications of the Basic Module IP 241 . . . . . 8 – 1

8.2 Technical Specifications of the Encoder Matching Modules ., , ... , ... , 8 – 1

8.3 Time Requirements . . . . . 8 – 3

8.4 Basic Connector Assignment . . . . , ... 8 – 7

8.5 Spare Parts for IP 241 . . . . . 8 – 8

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8.8 Permissible Slots for the Digital Positon Decoder Module . . . . . 8 – 11

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8.1 Technical Specifications of the Basic Module IP 241 (6ES5 241 –1AA12)

Operating temperature	O“c to 55°C
Storage temperature	–40°C to +85°C
Isolation class	“C” (According toVDE0110)
Degree of protection	IP20 for installation in module rack
Power supply voltages and current consumption of the basic module	5 V/1 A 24 V/0.18 A

* The current consumption of the encoder matching modules must be added to the values of the basic module!

8.2 Technical Specifications of the Encoder Matching Modules

Matching module	Incremental	Absolute 1 Excess–3 Gray	Absolute 2 BCD/Binary	Absolute 3 Analog	Absolute 4 Synchronous–Serial
6ES5 241	–1AB12	–1AC12	–1AD12	–1AE12	–IAF12
Supply voltagea Current consumption	5 V/0.8 A	5 V/0.55 A 24 V/0.2 A	5 V/0.4 A 24 V/0.35 A	5 V/0.2 A 24 V/0.18 A	5 V/0.6 A 24 V/0.9 A
Input signals (from encoders) configurable on matching modules	5-20 V sym. 10–30 V sym. 5–20 V asym. 10–30 V asym.	5V 12–15 V 24 V Open Collector	5V 10-15 v 24 V Open Collector	+/– 100 mV +/– 1 v +/– 10 V +/– 20 mA	• Serial interface according to RS 422 or RS 485 • Current loop (approx. 7 mA)
Input signal code (selectable)		–	–	–	• Gray • Binary • BCD
Maximum input frequency	50 kHz	50 kHz	50 kHz	–	Corresponding to transmission frequency

Starting MLFB–..., the basic module and the encoder matching module are UL and CSA approved.

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Technical specifications of the encoder matching modules:

Matching module	Incremental	Absolute 1 Excess–3 Gray	Absolute 2 BCD/Binary	Absolute 3 Analog	Absolute 4 Synchronous–serial
6ES5 241–	–1AB12	–1AC12	–1AD12	–1AE12	–1AF12
Output signal interface	-	–	–	–	sarial according to RS 422 or RS 465 (Transmitting clock pulse groups)
Transmission frequency	-		–	–	•Encoder resolution ≤ 10 bit approx. 100 kHz •Encoder resolution > 10 bit approx. 200 kHz
Representation area	–99999 to +99999	0 to +99999	0 to + 99999	0 to 1023 bits + sign	. with BCD conversion 0 to +99999 (maximum resolution = 17 bits) •without BCD conversion 0 to FFFFF HEX (maximum resolution = 20 bits)
Control bit evaluation	–	–			Configurable
Encoder supply voltages and maximum load	+5 V/0.6 A +12 V/0.25 A +15 V/0.2 A +24 V/2 A ①	+5 V/0.6 A +12 V/0.2 A +15 VI 0.2A +24 V/2 A ①	+5 V/0.2 A –5 V/0.5 A +12 V/0.2 A –12 V/0.2 A +15 V/0.2 A –15 V/0.2 A +24 V/2 A ① –24 V/2 A	+5 V/0.2 A +12 V/0.2 A +15 V/0.2 A +24 V/2 A ①	with remote sensing / maximum line resistance +5 V/1 A 6 Ω +12 V/1 A 2.5 Ω +15 V/1 A 1 Ω +24 V/2 A ①
Clock pulse groups per channel	–	–		–	Configurable from 1 to...
Clock pulse groups break period	–	–	–		≥ Clock pulse groups (generated internally)
Evaluation of encoder rotary direction	–	–		–	Switchable to obtain increasing values

If the encoder is supplied via the encoder matching modules, an external 24 V connection is required at the power supply connector of the IP 241!

① This is a conductor feed-through between the power supply connector and the sub D connector which can carry a maximum load of 2 A (without remote sensing).

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8.3 Time Requirements

1. Power On

The SP bit appears after turn-on or return of thevoltagetothe control. After approx. 100 µsec the SP bit can be scanned by the S5 unit. Its status is "I" until the module is ready to permit write commands (memory initialization). Now the module can be parameterized (i.e., the initial and end setpoints and interrupt identifiers must be allocated to the 32 tracks of the two channels).

When operating with standard function blocks, this is automatically considered.

2. Parameter Assignment

For the transmission of a setpoint, the IP 241 processor requires **8 msec**

Example: For channel 1 with 4 cams set and channel 2 with eight cams set, the total time required is 12x 2 x 8 msec = 192 msec.

This means, the total time required for parameterization of

8 msec x 32 setpoints (initial value) = 256 **msec**
8 msec x 32 setpoints (end value) = 256 **msec**

Total time Σ = 512 **msec**

3. Processing Time

> The processing times in this section refer to a comparison of the setpoint with the actual value.
>
> If identical setpoints are used for several tracks, the matching number of comparisons is required.

3.1 Encoder Matching Module (Incremental)

Typical processing time per setpoint/actual value comparison **1 msec**

3.2 Encoder Matching Module Absolute 1 (Excess–3 Gray)

Typical processing time per setpoint/actual value comparison **1 msec**

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3.3 Encoder Matching Module Absolute 2 (BCD/Binary)

1st **case:** Setpoints binary and actual values binary
Typical processing time per setpoint/actual value comparison **msec**

2nd case: Setpoints BCD and actual values BCD
Typical processing time per setpoint/actual value comparison **msec**

3rd case: Setpoints BCD and actual values binary
Here the processing time depends on the encoder resolution (up to 17 bits) which requires the following time periods for internal IP 241 conversion of the actual value from binary to BCD minimum 3 **msec**
maximum 13 **msec**

Depending on the respective actual encoder value, this entails the following times:

a) Minimum processing time per channel

3 msec x 16 setpoints (initial values)		= 48 **msec**
3 msec x 16 setpoints (end values)		= 48 **msec**
	Z	= 96 **msec**

b) Minimum processing time per channel

13 msec x 16 setpoints (initial values)		= 208 **msec**
13 msec x 16 setpoints (end values)		= 208 **msec**
	Σ	= 416 **msec**

> The setting of the DIP switch S1 must be in accordance with 1 to 3 (see section 5.3.1).

3.4 Encoder Matching Module Absolute 3 (Analog)

Typical processing time (up to version A12)	1.4 **msec**
Typical processing time (version A12 and later, firmware A07)	1 **msec**

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3.5 Encoder Matching Module Absolute 4 (Synchronous–Serial)

Here the switch position (see section 7.3.1) must be considered!

1st case: Binary setpoints and actual binary values (up to 20 bits)
Typical processing time per setpoint/actual value comparison **msec**

2nd case: BCD setpoints and actual BCD values (up to 20 bits)
Typical processing time per setpoint/actual value comparison **msec**

3rd case: BCD setpoints and actual binary values
– ≤ 10 bits typical processing time **1.4 msec**
(Attention: Observe switch position according to section 7.3.1; otherwise up to 3 msec maybe required)
– Up to 17 bits **minimum 3 msec**
maximum 13 msec

4th case: Binary setpoints and actual Gray code values
Typical processing time per setpoint/actual value comparison **msec**

4. General

With the typical processing times of 1 msec per setpoint/actual value comparison, the following (continuous) tolerances can be reached:

–	60 m/min.	+–	2 mm Tolerances
–	6 m/min.	+–	0.2 mm Tolerances
–	0.6 m/min.	+–	0.02 mm Tolerances
–	0.06 m/min.	+–	0.002 mm Tolerances

During transfer of new setpoints to the module, the actual value acquisition is delayed and the indicated tolerances are increased.

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5. Modifying Setpoints

The transfer of a setpoint for each parameterized initial or end value takes **8 msec**

8 msec x 32 (maximum initial values for 2 channels) = 256 **msec**
8 msec x 32 (maximum end values for 2 channels) = 256 **msec**

Σ = 512 **msec**

6. Zero Shift (Incremental Encoders)

For a zero shift (i.e., synchronization of the module), a certain time period per channel is required for updating the result bits. This time requirement for each specified initial or end value (consider parallel operation) is **1 msec**

7. Special Functions

Activation of the "verify–read" and "calculate average value" special functions increases time requirements as shown below.

Verify-read	100 µs x number of "incorrect" read procedures ①
Calculate average value	100 µs x number of actual values for "calculate average value" ①

8. First Start-Up (Worst Case)

For a complete start-up the worst case conditions apply. Time from turning on the power supply until the interrupts and track identifier bits are correctly set:

a) maximum time required for parameter assignment
8 msec x 32 initial values = 256 **msec**
8 msec x 32 end values = 256 **msec**

b) maximum time required for binary/BCD conversion
13 msec x 32 initial values = 416 **msec**
13 msec x 32 end values = 416 **msec**

Worst case Σ = 1344 msec



These time characteristics must be considered during configuring.

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① See also sections 1.10 and 1.11

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8.4 Basic Connector Assignment

	d	b	Z
2		OV (Potential)	P + !5V
4		PESP	
6		AB O	CPKL
8		AB 1	$\overline{\text{MEMR}}$
10		AB 2	$\overline{\text{MEMW}}$
12		AB 3	$\overline{\text{RDY}}$
14	$\overline{\text{IRA}}$	AB 4	DB O
16	$\overline{\text{IRB}}$	AB 5	DB 1
18	$\overline{\text{IRC}}$	AB 6	DB 2
20	$\overline{\text{IRD}}$	AB 7	DB 3
22		AB 8	DB 4
24		AB 9	DB 5
26		AB 10	DB 6
28		AB 11	DB 7
30			
32		OV (Potential)	

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8.5 Spare Parts for IP 241

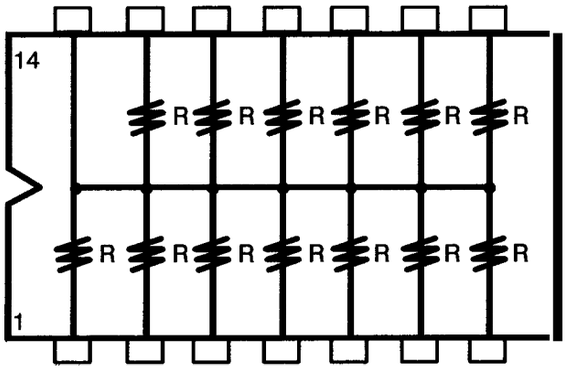
Part	Order No.:
Basic module	6ES5 241–IAA12
Encoder matching module incremental	6ES5 241–IAB12
Encoder matching module absolute 1 (Excess–3 Gray)	6ES5 241–IAC12
Encoder matching module absolute 2 (BCD/Binary)	6ES5 241–IAD12
Encoder matching module absolute 3 (Analog)	6ES5 241–1AE12
Encoder matching module absolute 4 (Synchronous–Serial)	6ES5 241–1AF12
Configuring set incremental	6ES5 271–IAB11
Configuring set absolute 1 (Excess–3 Gray)	6ES5 271–IAC11
Configuring set absolute 2 (BCD/Binary)	6ES5 271–IAD11
Configuring set absolute 3 (Analog)	6ES5 271–IAE11
Configuring set absolute 4 (Synchronous–Serial)	6ES5 271–IAF11

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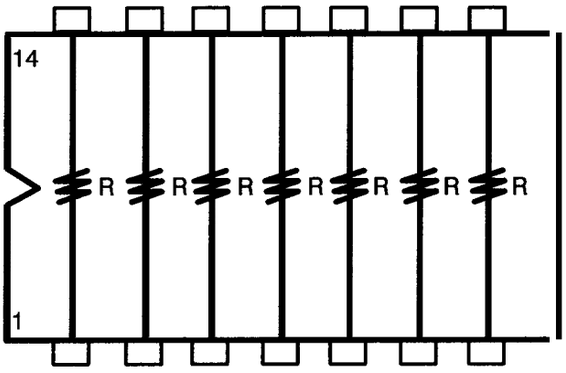
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8.6 Replacement Types for Resistor Networks

Type	Beckmann	Dale	Bourns
Single resistors e.g., 2 kΩ	899–3–R K	MDP14–03–202	14–01 -202
Resistors with joint point e.g., 1.5 kΩ	899–1 –R.5 K	MDP14–01–152	14–02–152
Single resistors e.g., 3.3 kΩ	899–3–R3.3 K	MDP1 4–03332	14–01 –332
Resistors with joint point e.g., 8.2 kΩ	899–1 –f&2 K	MDP14–01-822	14–02-822



Resistors with joint point



Single resistors

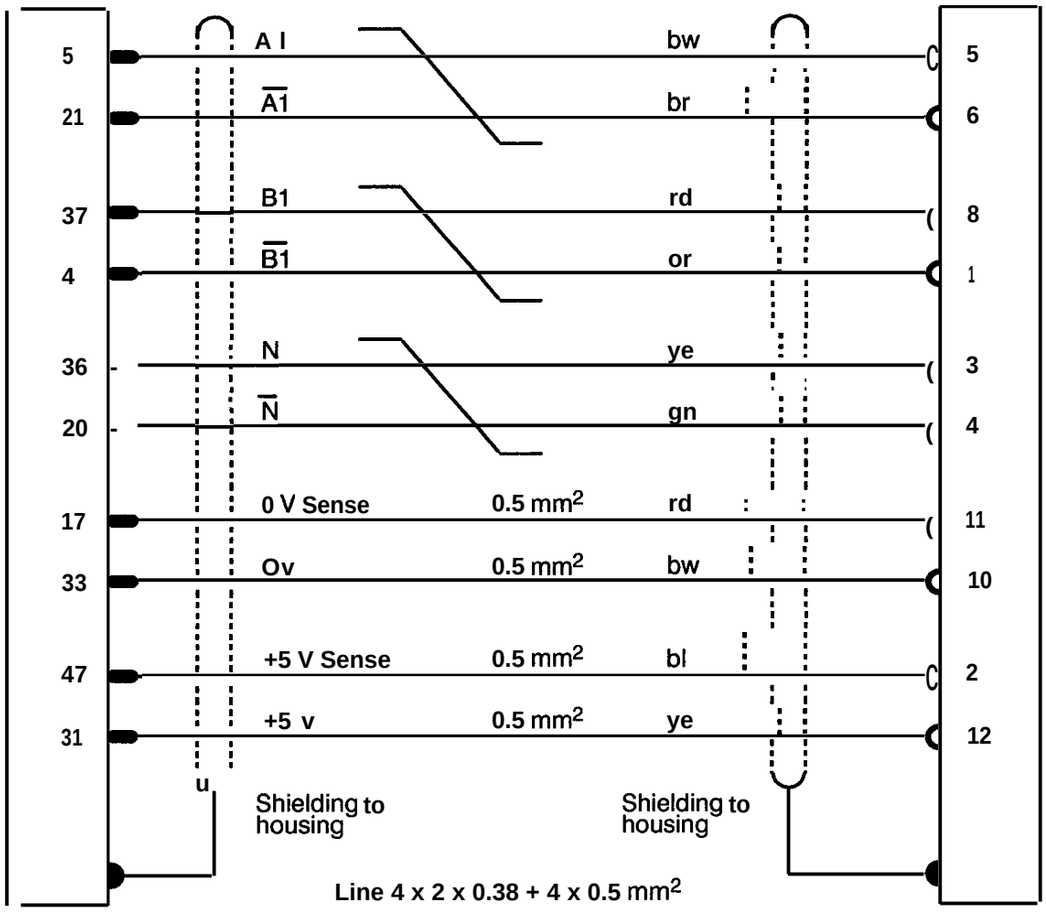
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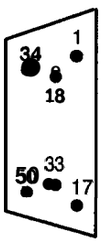
8.7 Cables for Siemens Incremental Encoders

Cable name: IP 241 pulse generator (6FC9320–... with SIEMENS round connector)

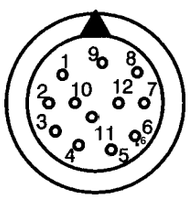
Order no.: 6ES5705–4xx1 (see catalog ST 52.3)

xxx = Length code: 5 m BFO
10 m CBO
20 m CCO
32 m CDO





D–Sub connector
50–way pin (crimp type)
Connection side
Metallized housing with sliding lock

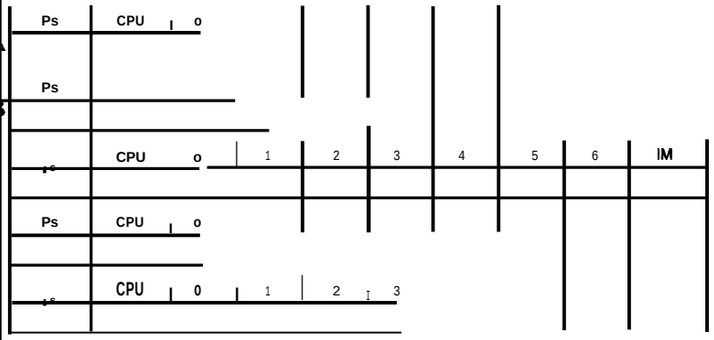
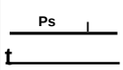
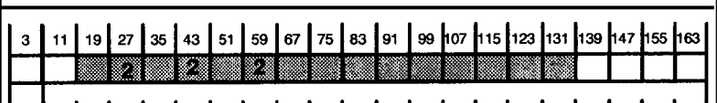
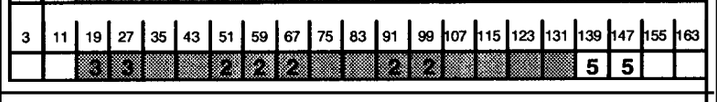
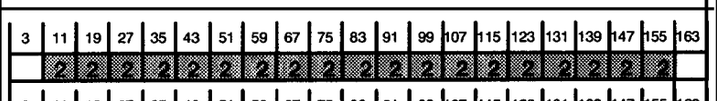
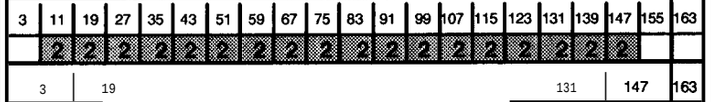
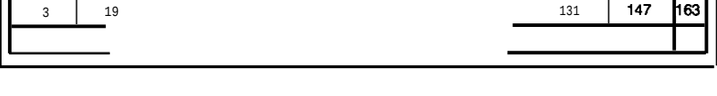


Round connector
12–way socket
Connection side
SIEMENS

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8.8 Permissible Slots for the Digital Position Decoder Module

Programmable Controller in Module Subrack		Slot Designation ▨ ≙ IP 241 can be operated in this slot.
Central device 115U	CR 700–0LA	
	CR 700–0LB	
	CR 700–1	
	CR 700–2	
	CR 700–3	
Expansion device	ER 701 –3[1]	
Central device 135U		
Central device 155U		
Expansion device 183U		
Expansion device 184U		
Expansion device 185U		
Expansion device 186U		

The IP 241 digital position decoder cannot be used in central device S5–150U, and expansion devices ER 701 –1, ER 701–2 and S5–187U.

1) Starting with release status 6ES5 701–3LA13, alarms can be processed in the expansion device when light wave conductor couplings 6ES5 307–3UA11 and 6ES5 317–3UA11 are used.

2) Functionality severely restricted since there are not interrupt lines.

3) Functionality restricted since not all interrupts lines are present.

4) Interrupt only with IM 307/317

5) Jumpers on the bus PCB must be changedd first.

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9.1 Overview

These programming instructions describe the following two standard function blocks:

FB 156 (PER:WPA) "Parameterize position decoder"

FB 157 (PER:WST) "Control position decoder"

FB 158 (PER:WSI) "Control position decoder (indirect parameterization)"

The function blocks are used in connection with the

IP 241 digital position decoder module

in the following programmable controllers:

FB 156	FB 157	FB 158	PLC/CPU
x	x	x	S5–115U CPU 941A/B to 944A/B
x	x	x	S5–135U CPU 922, 928A/B
x	x	x	S5–150U/S
x	x	x	S5–155U

These programming instructions require the user to be familiar with sections 1 to 8 of the operating instructions for the respective programmable controller.

The following example shows a test assembly with the IP 241 digital position decoder for testing the jumper assignments and functions in an easy fashion. This test program can be also used as the basis for an automation task to be realized.

The files of the function blocks with example together with commentary blocks in English and French for the respective programmable controllers are located on the S5–DOS floppy disk.

PLC S5–	Function Block	Commentary Block	
	German	English	French
	S5KxxxST.S5D	ECKxxxST.S5D	FCKxxxST.S5D
115U	S5KA50ST.S5D	ECKA50ST.S5D	FCKA50ST.S5D
135U	S5KB22ST.S5D	ECKB22ST.S5D	FCKB22ST.S5D
150U/S	S5KA40ST.S5D	ECKA40ST.S5D	FCKA40ST.S5D
155U ①	S5KA60ST.S5D	ECKA60ST.S5D	FCKA60ST.S5D

Copy the commentary blocks to file S5KxxST.S5D to obtain the commentaries in your language on the printout of the example.

The pertaining title block files are:

S5KxxxF1.INI
ECKXXXF1.INI
FCKXXXF1.INI

① When a CPU 922 or 928A/B is used in PLC S5–155U, use the xxKB22ST.S5D files.

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9.2 Function Block FB 156 (PER:WPA)

9.2.1 Function Description

The function block "parameterize position decoder" supplies the module with the initial and final track setpoints for both channels including the zero shift. If necessary the interrupt identifier bits are set.

The data to be transferred is stored in a user data block. The required data must be entered there by the user prior to calling the function block.

Prior to parameter assignment, the data on the module is deleted. The firmware contents are read and entered into the data block.

In the S5–115U, the function block is usually called by organization block OB20 (or OB21 programmable controller S5–115U) if there is a cold restart.

Function

Transfer of the specified setpoints from the user data block to the digital position decoder module IP 241.

9.2.2 Calling the Function Block

In the STL (Statement List):

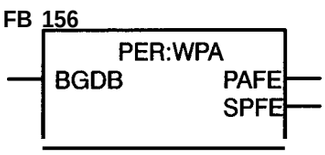
S5-115U

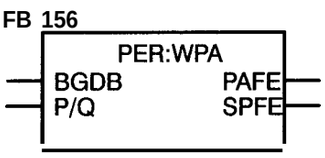
```
      :JU FB156
NAME  :PER:WPA
BGDB  :
PAFE  :
SPFE  :
```

S5–135U
S5–150U/S
S5–155U

```
      :JU FB156
NAME  :PER:WPA
BGDB  :
P/Q   :
PAFE  :
SPFE  :
```

In the LAD/CSF (Ladder Diagram/ Control System Flow Chart)





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9.2.3 Explanation of Parameters

NAME	CLASS	TYPE	DESIGNATION
BGDB	D	KY	Specification of the module address and user data block number
P/Q	D	KS	Specification of 1/0 area[1]
PAFE	Q	BI	Parametererror
SPFE	Q	BI	Module error (SP bit)

[1] Programmable controller S5–1 15U does not have this parameter. It can only be addressed in the P–range.

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9.2.4 Parameter Assignment

BGDB : KY = x, y

x = Module address (BG)
128< x ≤ 248 for P/Q : KS=P
0 ≤ x ≤ 248 for P/Q: KS=Q

x = Data block number (DB)
1< y ≤ 255
2≤ y ≤ 255 for S5–155U and S5–135U
(Specification of a DX data block is not possible)

P/Q : KS = P Normal I/O area
KS = Q Extended 1/0 area

PAFE : In case of illegal parameterization the signal status is"1". The recognized error is then shown by the assignment of the flag byte FY 255:

F 255.0 The module address is outside of the specified area or not within the 8–bit grid pattern (first part of parameter BGDB).

F 255.1 The parameter P/Q is not set with 'P-' or 'Q–'
(not for programmable controller S5-115U)

F 255.2 The specified user data block number is zero or one.
(one only for S5–155U andS5-115U)
(second part of parameter BGDB)

F 255.3 The specified user data block does not exist or is too short.
(second part of parameter BGDB)

F 255.4 QVZ, no module found under this address.
(first part of parameter BGDB)
(only for S5–155U and S5–135U)

F 255.5 When the "verify–read (PR)" or "calculate average value (MB)" special function is enabled, the "number" parameter is located (outside the permissible area from O to 15) in data word DR 182 or DR 184 of the user data block.

F 255.6 –

F 255.7

SPFE : Is set, if after an access the SP bit is not reset by the module within a specified time interval.

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9.2.5 User Data Block Assignment

The data block specified under parameter BGDB is assigned as follows:

From DW	Assignment
o	Work area of the function block
10	Channel 1 Track O
15	Channel 1 Track 1
20	Channel 1 Track 2
25	Channel 1 Track 3
30	Channel 1 Track 4
35	Channel 1 Track 5
40	Channel 1 Track 6
45	Channel 1 Track 7
50	Channel 1 Track 8
55	Channel 1 Track 9
60	Channel 1 Track 10
65	Channel 1 Track 11
70	Channel 1 Track 12
75	Channel 1 Track 13
80	Channel 1 Track 14
85	Channel 1 Track 15
90	Channel 2 Track 16
	Channel 2 Track 17
1%	Channel 2 Track 18
105	Channel 2 Track 19
110	Channel 2 Track 20
115	Channel 2 Track 21
120	Channel 2 Track 22
125	Channel 2 Track 23
130	Channel 2 Track 24
135	Channel 2 Track 25
140	Channel 2 Track 26
145	Channel 2 Track 27
150	Channel 2 Track 28
155	Channel 2 Track 29
160	Channel 2 Track 30
165	Channel 2 Track 31
170	Zero shift
175	Clock pulse group (for SS1 module)
177	Hysteresis (for analog submodule)
179	Rotary axis function
180	Sofware-based parallel switching of K1 and K2
181	Verify-read
183	Calculate average value (for analog submodule)
185	inhibit interrupt depending on direction
187	= Free for user =

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Setting one cam:

DW n	Interrupt for initial value		Interrupt for end value	
DW n+1	S x	x	x	$(2^{9} \ldots 10^{4} \ldots 2^{6})$
DW n+2	$(2^{15} \ldots 10^{3} \ldots)$	10^{2}	10^{1}	$10^{0} \ldots 2^{0})$
DW n+3	S x	x	x	$(2^{19} \ldots 10^{4} \ldots 2^{16})$
DW n+4	$(2^{15} \ldots 10^{3} \ldots)$	10^{2}	10^{1}	$10^{0} \ldots 2^{0})$

S = sign "O": positive "I": negative

Initial setpoint = DW n+1 and DW n+2
Final setpoint = DW n+3 and DW n+4

The setpoints are usually given in BCD code. Only the decades O through 4 are considered. A setpoint entry is also possible, however, in binary representation (depending on the encoder).

If the interrupt identifiers are set with "O", no interrupt entry is made. If this data word is set with KH = FFFF, the track is regarded as not set. The setpoints are not transferred to the module. In all other cases the interrupt is entered for the corresponding setpoint.

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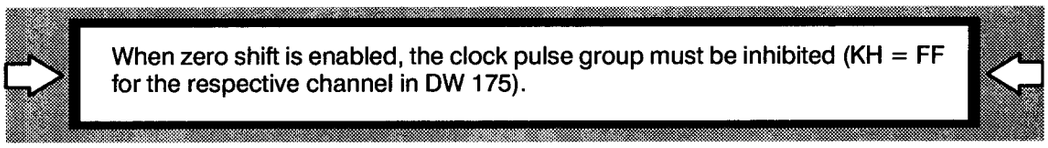
Setting of the zero shift (NV):

DW 170	Interrupt for NV 1			Interrupt for NV 2	
DW 171	S	x	x	x	10^4
DW 172	10^3		10^2	10^1	10^0
DW 173	S	x	x	x	10^4
DW 174	10^3		10^2	10^1	10^0

NV 1 (Channel 1) = DW 171 and DW 172
NV 2 (Channel 2) = DW 173 and DW 174

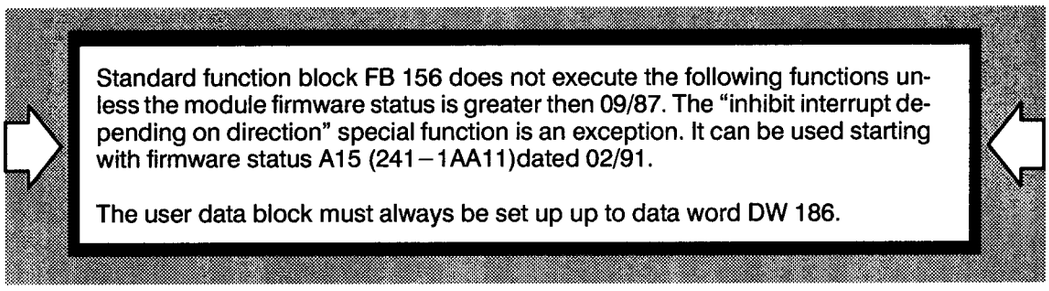
The setpoints for the zero shift are entered in the user data block. The setting is the same as for a normal track.

If the interrupt identifiers are set with "O", no interrupt entry is made. If assigned with KH = FF, no NV value is transferred. In all other cases an interrupt is entered.



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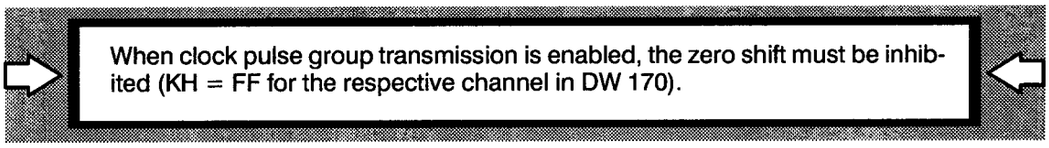
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Setting of the clock pulse groups (for SS1 module)

DW 175	Enable for channel 1		Enable for channel 2	
DW 176	10′	10°	10′	10°

The lengths of the clock pulse groups in data word DW 176 are given in BCD code.



If the enables for channel 1 (DL 175) or channel 2 (DR 175) are set with KH = FF, the clock pulse group length for the respective channel is not transferred to the module.

Setting of the hysteresis (for analog submodule)

DW 177	Enable for channel 1		Enable for channel 2	
DW 178	10′	10°	10′	10°

The hysteresis values in DW 178 are to be given in BCD code.

If the enables for channel 1 (DL 177) or for channel 2 (DR 177) are set with KH = FF, the hysteresis value for the respective channel is not transferred to the module.

Setting of the rotary axis function

DW 179	Enable for channel 1	Enable for channel 2

If the enables for channel 1 (DL 179) or channel 2 (DR 179) are set with KH = FF, the rotary axis function for the respective channel is disabled.

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Setting of the parallel connecting function

DW 180	Enable parallel connection channel 1 and 2

If data word DW 180 is set with KH = FFFF, the function is disabled. In all other cases channels 1 and 2 are switched parallel by the software.

Assignment of the "verify-read" special function

DW 181	Enable for channel 1	Enable for channel 2
DW 182	Channel no: (O or 16)	Number (O to 15)

The "number" parameter is not transferred to the module when the enable character for channel 1 (DL 181) or channel 2 (DR 181) in the user data block is KH = FF. Otherwise an area check of the "number" parameter is performed. If the "number" parameter (DR 182) is outside the range from O to 15, function block FB 156 terminates its processing by setting the parameterization error bit (PAFE) and ERROR bit F255.5. The assignment of the "channel no." parameter in data word DL 182 has significance in relation to function blocks FB 157 and FB 158.

Assignment of the special function for calculate average value

DW 183	Enable for channel 1	Enable for channel 2
DW 184	Channel no: (O or 16)	Number O to 15)

The "number" parameter is not transferred to the module when the enable character for channel 1 (DL 183) or channel 2 (DR 183) in the user data block is KH = FF. Otherwise an area check of the "number" parameter is performed. If the "number" parameter (DR 184) is outside the range from O to 15, function block FB 156 terminates its processing by setting the parameterization error bit (PAFE) and ERROR bit F255.5. The assignment of the "channel no." parameter in data word DL 184 has significance in relation to function blocks FB 157 and FB 158.

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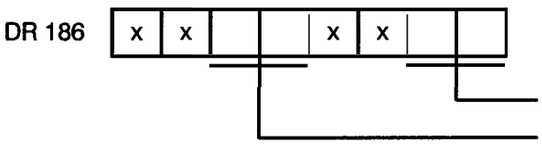
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Assignment of special function for inhibit interrupt depending on direction

DW 185	Enable for interrupt direction specification	
DW 186	Free	Bit pattern for IR–direction

When the current "actual position" exceeds a cam end or cam start setpoint, the module does not generate an interrupt unless the appropriate interrupts were enabled. The interrupt is triggered when the applicable threshold value is reached.

The "inhibit interrupt depending on direction" special function can be used to inhibit the triggering of one interrupt for one or both direction. This function is enabled by entering a number not equal to KH = FFFF in data word DW 185 of the user data block. When this function is enabled, the bit pattern of data word DR 186 is transferred to the IP module and the desired interrupt direction is inhibited for one or both channels. The selection of the desired "interrupt direction" is shown below.



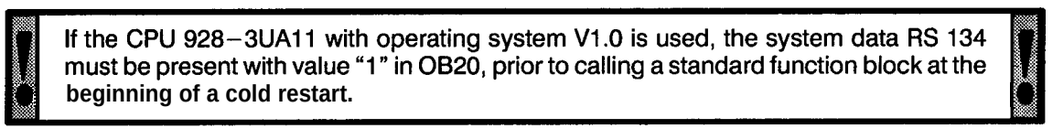
Interrupt, channel 1

Interrupt, channel 2

O 0 Enabled for both directions
O 1 Inhibited, backwards
10 Inhibited, forwards
1 1 Inhibited, both directions

Addressing the module (S5–155U)

For correct operation of the function block, the module "digital position decoder IP 241" must be addressed in the address range from KH = FF080 to KH = FF1 FF. This corresponds to the P–range from KH = FF080 to KH = FFOFF (byte number 128 to 255) and to the Q–range from KH = FF1OO to KH = FF1FF (byte number O to 255).



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9.2.6 Technical Specifications

Block no.	156			
Block name	PER:WPA			
PLC S5–	115U	135U	15ou/s	155U
Library no. P71200–S...	5156–A–6	9156–A–6	4156–A–3	6156–B–3
Call length (in words)	6			
Block length (in words)	934	794	1012	738
Processing time in msec ①				
	CPU 941A/B	CPU 922		
Basic requirement	98.5124.3	30.4	13.9	16.3
Additional per track	35.81 9.8	7.5	6.3	6.2
Maximum (with all special functions)	1435.0 /500.6	388.0	289.0	272.0
	CPU 942A/B	CPU 928A/B		
Basic requirement	65.5/ 24.3	23.2114.2		
Additional per track	22.8/ 9.8	5.9/ 2.4		
Maximum (with all special functions)	935.0 /500.6	339.0 /276.1		
	CPU 943A/B			
Basic requirement	24.1 / 23.3			
Additional per track	11.2/ 9.5			
Maximum (with all special functions)	563.0 /493.5			
	CPU 944A/B			
Basic requirement	13.81 13.8			
Additional per track	4.5/ 2.7			
Maximum (with all special functions)	303.0 /278.5			
Nesting depth	0			
Subordinate blocks	None			
Data area used	User data block specified in BGDB parameter up to and including DW 186			
Flag area used	FY 234 to FY 255		FY 240 to FY 255	FY 236 to FY 255
System area used	–	BS 60 to BS 63	–	BS 180 to BS 183
System instructions	Yes			
Other	–			

① Cycle times can be exceeded in the user program (PLC in stop status) if commands with execution times of over 100 msec are used. If calling the function block several times cannot be avoided, the cycle time must be retriggered (OB 31) when the CPU 941 A (also 942A) is used.

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9.2.7 Function Block Application

FB 156 can be used in programmable controller S5–115U without restrictions. The other programmable controllers may not be used in manual and automatic warm restart operation modes.
For programmable controllers S5–135U and S5–155U, the operation mode "automatic cold restart" must be set in data block DXO (see equipment manuals of the respective programmable controllers). Forthe other programmable controllers, the statement STP (stop) must be programmed in start-up OB22 in case of an automatic warm restart (during resumption of power supply).

Prior to calling function block FB 156, the setpoints must be written on the user data block. The data block must have a minimum length of 181 words (even if the last functions are not required).

At first, the function block erases all parameterized data on the module. Then the firmware contents of the module are read and stored in the user data block. Afterwards the interrupt word of each track is scanned sequentially to see whether

– the track is not set (KH = FFFF),
– no interrupt is entered (KH = 0000),
– an interrupt is entered (all other cases KH = 0101).

If the track is not set, the next track is scanned. When a track is set, the setpoints are conditioned as required by the module and transferred to the module. The module requires up to 8 msec. to file a setpoint, before the next setpoint can be transferred (duration for one channel: approx. 256 msec. when all tracks are set).

Organize the tracks in ascending order of the setpoints to reduce the processing times for the module.

An already preset user data block is available on the floppy disk. With adequately conditioned setting it can be used for user–specific configuring tasks. (For setting of user data block see example.)

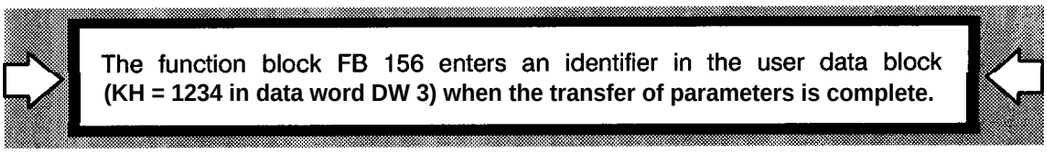
Parameterization of zero shift values is only effective with incremental encoders. The zero shift values are transferred without the SS synchronizing bit. This is the condition for hardware–based synchronization. Up to the moment of synchronization no actual value can be read (actual value = FFFFF).

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When the “calculate average value” or “verify” special function is used, the “number” para-meter must be located in the range from O to 15 in data word DR 184 or DR 182 respectively in the user data block. When zero is entered, the function switches off. Supplying the “channel no.” parameter in data word DL 184 or DL 182 of the user data block is not necessary. This parameter is only used in cyclic operation with function blocks FB 157 and FB 158.

After the processing of function block FB 156, the data block which was valid prior to calling FB 156 remains valid. The user data block with the setpoints is called by the function block FB 156 automatically.



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9.3 Function Block FB 157 (PER:WST)

9.3.1 Function Description

With the function block “control position decoder”, the following functions can be performed:

– Read actual values
– Read track identifier bits
– Read, delete or modify track setpoints
– Synchronize
– Special functions

The function block is usually called in the cyclic program. Prior to calling this function block, the module with the function block FB 156 (PER:WPA, parametrize position decoder) must be supplied with the initial data.

For evaluation of the process alarms or interrupts, the function block PER:WST can be called in a block of the interrupt–controlled processing (OB 2 to 06 9).

Function

Controlling the module “digital position decoder IP 241”

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9.3.2 Calling the Function Block

in the STL (Statement List)

S5-I 15U

```
        :JU FB157
NAME    :PER:WST
SPDB    :
BEF     .
WI      :
W2      :
KB  1   :
KB  2   :
ST      :
PAFE    :
SPFE    :
```

S5–135U

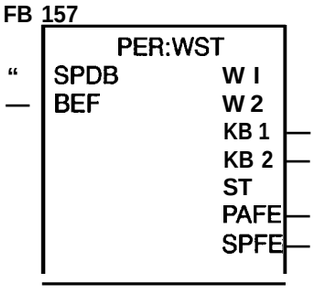
```
        :JU FB157
NAME    :PER:WST
SPDB    :
BEF     :
w       :
KB      .
ST      :
PAFE    :
SPFE    :
```

S5–150U/S
S5-155U

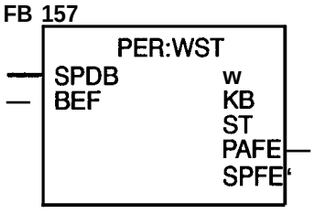
```
        :JU FB157
NAME    :PER:WST
SPDB    :
BEF     :
ABIT    :
w       :
KB      .
ST      :
PAFE    :
SPFE    :
```

In the LAD/CSF (Ladder Diagram/ Control System Flow Chart):

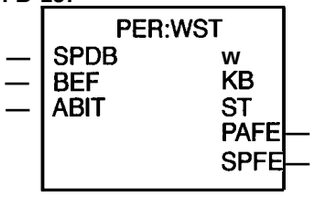
FB 157



FB 157



FB 157



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9.3.3 Explanation of Parameters

NAME	CLASS	TYPE	DESIGNATION
SPDB	D	KY	Specification of the track number and of the user data block
BEF	D	KS	Command; specification of the function to be performed by the block
ABIT	D	KY	Specification of the interrupt bit in case of interrupt processing
W or W 1 W 2	Q or Q Q	D W W	Depending on command, output of – actual value – track setpoint
KB or KB 1 KB 2	Q or Q Q	D W W	Output of track identifier bits
ST	Q	BY	Output of the control bits
PAFE	Q	BI	Parameterization error
SPFE	Q	BI	Module error (SP bit)

[1] Parameter ABIT only with S5–150U/S and S5–155U

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9.3.4 Parameter Assignment

SPDB : KY = x, y

x = Track number
The track number is dependent on the parameter BEF:
BEF = AE, IW, AW, EW
$0 \leq x \leq 31$ track number
BEF = SS, SH
x = 32 Zero shift Channel 1
x = 33 Zero shift Channel 2
BEF = KB
x = any choice

Y = User data block number
1< y $\leq$ 255
2< y $\leq$ 255 with S5-155U and S5-135U

BEF : KS = KB Only output of identifier bits and control bits
KS = AE Modifying the setpoints of a track
KS = SS Software-based synchronizing
KS = SH Hardware- based synchronizing
KS = IW Output of the actual value
KS = AW Output of the initial setpoint
KS = EW Output of the end setpoint
KS = IS Inhibit interrupt
KS = IV Inhibit interrupt for supplying the module with new setpoints
KS = N1 Zero shift, read channel 1
KS = N2 Zero shift, read channel 2
KS = PR Verify read
KS = MB Calculate average value
KS = RV Inhibit interrupt depending on direction

The identifier bits and the control bits are updated at each command.

ABIT : KY = x, y

x = Enable reset
x >< 0 No reset
x = O Reset of the corresponding interrupt bit in the system data

Y = Interrupt bit number
$0 \leq y \leq 7$

Parameter ABIT only with S5-150U/S and S5-155U

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PAFE : In case of illegal parameterization the signal status is"1". The recognized error is then indicated by the assignment of the flag byte FY 255:

F 255.0	–
F 255.1	When special function "verify" or "calculate average value" in data word DR 182 or DR 184 of the user data block is used, the "number" parameter is outside the permissible range of O to 15.
F 255.2	The specified user data block number is zero or one. (one only with S5–135U and S5–155U) (second part of parameter SPDB)
F 255.3	The specified user data block does not exist or is too short. (second part of parameter SPDB)
F 255.4	The parameter BEF cannot be interpreted.
F 255.5	The parameter ABIT is outside the specified range. (not set with S5-115U, S5–135U)
F 255.6	The track number is outside the specified range. (first part of parameter SPDB)
F 255.7	The specified user data block has no parameter identification. (is entered by FB 156)

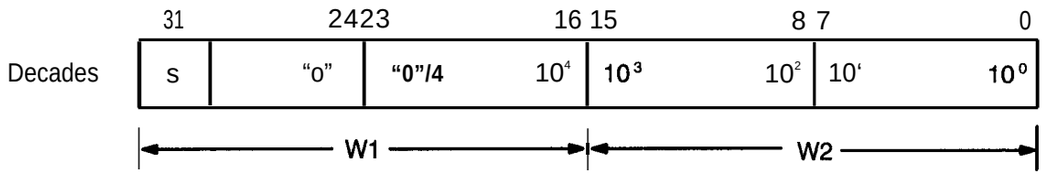
SPFE : is set when the module does not reset the SP bit within a certain period after an access.

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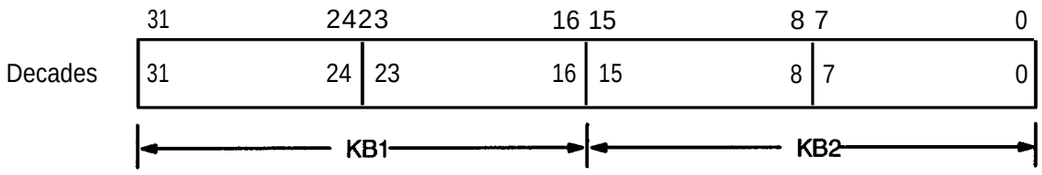
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Assignment of the parameters W, KB, and ST:

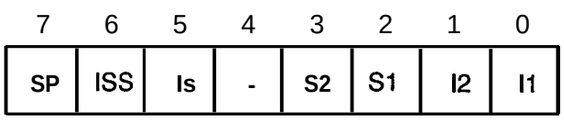
Depending on the setting of parameter BEF, either the actual value, the initial setpoint or the final setpoint are output at parameter W. If a setpoint needs to be supplied with an interrupt, this is shown at parameter W_1 (setpoint with interrupt -t setting of bits 23 through 20: 0100). The bit assignment looks like this:



The track identifier bits are output at parameter **KB**. The setting is as follows:



The synchronization bits and interrupt bits are output at parameter **ST:**



I1/I2	Interrupt in channel 1/2
S1/S2	Channel 1/2 synchronized
IS	All interrupts inhibited (Bits IS and ISS are set by transferring E3.
ISS	Interrupt inhibited for supplying the module with new setpoints (by transfer of E4)
SP	SP bit

9.3.5 User Data Block Assignment

If track setpoints are to be modified, they must be in the same user data block which was used for parameter setting (see description for FB 156, PER:WPA). The same applies to the zero shift values during synchronizing.

Addressing the module (S5–155U)

For proper operation of the function block, the module "digital position decoder IP 241" must be addressed in the range from KH = FF080 to KH = FF1FF. This corresponds to the P–range from KH = FF080 to KH = FFOFF (byte number 128 to number 255) and the Q–range from KH = FF100 to **KH = FFIFF (byte number O to number 255).**

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9.3.6 Technical Specifications

Block number	157			
Block name	PER:WST			
PLC S5–	115U	135U	15ou/s	155U
Library no. P71200–S...	5157–A–7	9157–A–5	4157–A–3	6157–B–3
Call length (in words)	12	9	10	
Block length (in words)	933	782	1095	890
Processing time (in msec)				
For BEF =	CPU 941A/B	CPU 922		
KB	12.5/ 4.5	2.2	0.4	0.7
IW, AW, EW, N1 , N2	29.0/ 9.7	5.8	1.0	1.2
SS, SH	41.1 / 12.8	7.3	1.8	2.0
AE	63.0/ 22.1	14.6	12.5	12.7
PR, MB, RV	37.0/ 12.3	8.2	1.0	1.6
Is, Iv	35.0/ 11.6	5.8	1.0	1.0
For BEF =	CPU 942A/B	CPU 928A/B		
KB	8.31 4.5	1.3/ 0.3		
IW, AW, EW, N1, N2	14.4/ 9.7	3.0/ 0.8		
SS, SH	21.8/ 12.8	4.6/ 1.2		
AE	37.1 I 22.1	9.91 4.1		
PR, MB, RV	19.0/ 12.3	4.7/ 1.1		
Is, Iv	17.0/ 11.6	3.1 / 0.7		
For BEF =	CPU 943A/B			
KB	4.4/ 4.2			
IW, AW, EW, N1, N2	9.31 9.3			
SS, SH	12.5/ 12.3			
AE	22.5/ 21.0			
PR, MB, RV	13.0/ 11.5			
Is, Iv	12.0/ 11.0			
For BEF =	CPU 944A/B			
KB	0.6/ 0.6			
IW, AW, EW, N1 , N2	1.3/ 1.3			
SS, SH	1.8/ 1.7			
AE	6.6/ 5.6			
PR, MB, RV	1.9/ 1.7			
is, Iv	1.6/ 1.4			
Nesting depth	0			
Subordinate blocks	None			

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PLC S5–	115U	135U	150U/S	155U
Assignment in data area	User data block specified in parameter SPDB up to and including DW 186			
Assignments in flag area	FY 234 to FY 255		FY 238 to FY 255	FY 236 to FY 255
Assignments in system area	–	BS 60 to BS 63	–	BS 180 to BS 183
System instructions	Yes			
Other	①	–	–	②

① Interrupts and alarms in the blocks are temporarily inhibited by the commands AS/AF. This cancels an AS command programmed by the user.

② Process alarms, interrupts and alarms are inhibited in the block for approximately 2 msec. This cancels an AS command programmed by the user.

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9.3.7 Function Block Application

FB 157 can be used in programmable controller S5–115U without restrictions. The other programmable controllers may not be used in manual and automatic warm restart operation modes.
For programmable controllers S5– 135U and S5– 155U, the operation mode "automatic cold restart" must be set in data block DXO (see equipment manuals of the respective programmable controllers). For the other programmable controllers, the statement STP (stop) must be programmed in start-up OB 22 in case of an automatic warm restart (during resumption of Dower supply).

Prior to calling the function block FB 157, the module must have been parameterized with function block FB 156.

Via parameter BEF, function block FB 157 receives the function to be performed:

BEF = IW Read actual value

SPDB : KY = x, y
with x < 16 the actual value of channel 1 is read, otherwise channel 2 is read.

W : Output of actual value, or
WI : Output of actual value (High word)
W2 : Output of actual value (Low word)

KB : Output of identifier bits, or
KB1 : Output of identifier bits (High word) -t Channel 2
KB2 : Output of identifier bits (Low word) -t Channel 1

ST : Output of control bits

BEF = KB Read track identifier bits

KB : Output of identifier bits, or
KB1 : Output of identifier bits (High word) → Channel 2
KB2 : Output of identifier bits (Low word) -t Channel 1

ST : Output of control bits

(This command is used with interrupt processing in the interrupt–controlled program; see below).

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BEF = AE Modify **setpoints**

SPDB : KY = x, y 0< x $\leq$ 31 Track number

KB : Output of identifier bits, or
KB1 : Output of identifier bits (High word) -t Channel 2
KB2 : Output of identifier bits (Low word) → Channel 1

ST : Output of control bits

Both setpoints must be specified per track.
The track is deleted for interrupt identifier KH = FFFF.

> Undefined identifier bits and interrupts can occur (despite special function E4!) when setpoints are modified in the "encoder running" process phase.

BEF = SS Software-based synchronizing
BEF = SH Hardware–based synchronizing

SPDB : KY = x, y x = 32: Zero shift, Channel 1
x = 33: Zero shift, Channel 2

KB : Output of identifier bits, or
KB1 : Output of identifier bits (High word) -t Channel 2
KB2 : Output of identifier bits (Low word) → Channel 1

ST : Output of control bits

If BEF=SH, the zero shift values are transferred without an SS bit; this is the precondition for hardware– based synchronizing with preliminary contact and zero mark (see operating instructions).

If BEF=SS, the zero shift values are transferred with an SS bit; this accomplishes software– based synchronization of the counter.

> Synchronization is only meaningful for incremental encoders.

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BEF = AW Read initial **setpoint**
BEF = EW Read end **setpoint**

SPDB: KY = x, y 0< x $\leq$ 31 Track number

W : Output of initial/end value, or
WI : Output of initial/end value (High word)
W2 : Output of initial/end value (Low word)

KB : Output of identifier bits, or
KB1 : Output of identifier bits (High word) → Channel 2
KB2 : Output of identifier bits (Low word) -t Channel 1

ST : Output of control bits

BEF = N1 Read zero shift, channel 1
BEF = N2 Read zero shift, channel 2

SPDB: KY = x, y x= Disregard

W : Output of zero shift, channel 1/2 or
W1 : Output of zero shift, channel 1/2 (high word)
W2 ; Output of zero shift, channel 1/2 (low word)

KB : Output of the identifier bits or
KB1 : Output of the identifier bits (high word) → Channel 2
KB2 : Output of the identifier bits (low word)+ Channel 1

ST : Output of control bits

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BEF = IS **Inhibit interrupt**
BEF = IV **Inhibit interrupt for supplying the module with new setpoints**

SPDB : KY = x, y x = Disregard

w : **Output unchanged, and/or**
WI : **Output unchanged (high word)**
W2 ; **Output unchanged (low word)**

KB **: Output of identifier bits, and/or**
KB1 **: Output of identifier bits (high word) → channel 2**
KB2 **: Output of identifier bits (low word) → channel 1**

ST **: Output control bits**

Special function "inhibit interrupt BEF = IS" or "inhibit interrupt for supplying BEF = IV" is activated by a one–time call and is deactivated again by another call.

The following table shows the assignment of the "ST parameter".

7	6	5	4	3	2	1	0
SP	1ss	Is	–	S2	S1	I2	I1

Activation of the "inhibit interrupt for supplying BEF = IV" command is indicated when bit 6 of the ST parameter is set. The "inhibit interrupt BEF = IS" command has been activated when bit 5 and bit 6 of the ST parameter are set. The module resets bit 5 and bit 6 when the interrupt inhibit is deactivated.

The "read actual value BEF = IW" command is used, for example, to provide current information concerning the module status (ST parameter).

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BEF = RV Inhibit interrupt depending on direction

SPDB: KY = x, y x = Disregard

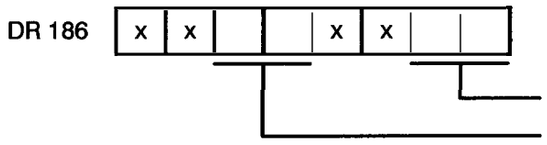
W : Output unchanged, and/or
WI : Output unchanged (high word)
W2 ; Output unchanged (low word)

KB : Output of identifier bits, and/or
KB1 : Output of identifier bits (high word)+ channel 2
KB2 : Output of identifier bits (low word) → channel 1

ST : Output control bits

During cyclic operation, the "inhibit interrupt depending on direction BEF = RV" command can be used to inhibit one of the two interrupt directions. This can also be done when data word DW 185 of the user data block has identifier KH = FFFF.

The assignment of data word DR 186 from the user data block in which the desired "inhibit direction" of the interrupt for one or both channels must be selected before the "BEF =RV" command is activated is shown below.



Interrupt, channel 1
Interrupt channel 2

O 0 Enabled for both directions
O 1 Inhibited, backwards
10 Inhibited, forward
1 1 Inhibited, both directions

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BEF = PR Verify-read
BEF = MB Calculate average value

SPDB : KY = x, y x = Disregard

W : Output unchanged, and/or
WI : Output unchanged (high word)
W2 : Output unchanged (low word)

KB : Output of identifier bits, and/or
KB1 : Output of identifier bits (high word) → channel 2
KB2 : Output of identifier bits (low word) -t channel 1

ST : Output control bits

Selection of the "verification read BEF = PR" or "calculate average value BEF = MB" special function using function block FB 157 during cyclic operation is not dependent on the enable identifier of data word DW 181 or DW 183 in the user data block.

Both commands require valid parameters in data word DW 182 or DW 184 (shown below) of the user data block before they can be activated.

DW 182/184	Channel no: (O or 16)	Number (O to 15)

The "channel no." parameter is used to select the desired channel. Zero must be entered for channel 1 and 16 for channel 2. All other entries cause an error message indicated by the "PAFE" parameterization error bit and by error identifier F 255.1.

The command–related parameter "number" must be supplied with a decimal value between zero and 15. The entry of zero causes the respective special function ("verify–read" or "calculate average value") to be deactivated. Entry of a number outside the permissible range causes the same error indication as when an incorrect channel number is selected.

When a parameterization error occurs, function block FB 157 terminates processing without transferring the parameters to the module.

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9.3.8 Interrupt Processing

If one of the setpoints or a zero shift value is to receive an interrupt identification, the module must be preset to a group interrupt bit of the input byte IB or to an interrupt line by means of jumper setting. (See operating instructions of the individual programmable controllers.)

To ensure that in case of programmable controllers with group interrupt (S5 – 150U/S, S5 – 155U in S5 – 150U mode) the respective interrupt block is processed only once (only for the rising edge of the interrupt signal) via input byte IB O, the number of this group interrupt bit must be specified at parameter ABIT:

ABIT : KY = x, y	x = 255, y = 255	Module without interrupt
	x = 0, y = 0 to 7	Reset of the correlated interrupt bit in the system data

If this bit is not reset in the system data of the respective programmable controllers, the corresponding alarm block is processed again when the interrupt signal disappears. (S5 – 155U: in S5 – 150U – mode an interrupt is evaluated via the input byte IB O depending on the edge; in S5 – 155U –mode the evaluation via the interrupt lines depends on the level).

If an interrupt occurs (in accordance with the jumper setting), a block of the interrupt–controlled processing is called.

The scratchpad flags must be saved in a data block at the start of this block and must be reloaded from there at the end of the block! The same applies to the assigned system data.

This block contains the call for function block FB 157 with the parameter assignment BEF=KB. After the call, the parameter ST indicates from which channel the interrupt arrived. Now a special interrupt program can be processed.

If an interrupt occurs during processing of function block FB 157 in the cyclic program, the group interrupt at the bus is deleted again in FB 157 when byte 7 is read. Consequently no organization block of the interrupt–controlled processing is called. The function block, however, updates the control bits so that subsequently an interrupt program can be called depending on the interrupt bits.

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Example:

Program in062

– Save scratchpad flags

```
        :JU FB157
NAME    :PER:WST
SPDB    :     KY
BEF     :     KSKB
ABIT    :     KY0.0
w       :
KB      :
ST      :     FY 191
PAFE    :
        .
        :O  F  190.0
        :O  F  191.0
        :JC FB xx
        :O  F  190.1
        :O  F  191.1
        :JC FB yy

            KBO
            FY 190
            FY 191
```

- Load scratchpad flags

```
        :BE
```

FB xx – Customer–specific interrupt program for channel 1
FB yy – Customer–specific interrupt program for channel 2

After the control bits in the interrupt–controlled program have been evaluated, they must be reset, as otherwise the interrupt programs (FBxx and FByy) could be processed again in the cyclic program.

Program in 061

```
        :JU FB157
NAME    :PER:WST
SPDB        KY
BEF         KSxx
ABIT        KY0.0
w
KB
ST          FY 190
PAFE
        .
        :A  F 190.0
        :JC FB xx
        :A  F 190.1
        :JC FB yy
```

Saving and loading scratchpad flags

In the blocks for time–controlled processing, saving and loading scratchpad flags (FY200to FY 255) and the assigned system data is absolutely necessary when flags from the mentioned area are used in these blocks.

Saving and loading must take place in a different data area from the one for process interrupts.

The same applies to an automatic or manual restart. This is not required forS5–115U or in the event of faulty 06s.

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9.4 Function Block FB 158 (PER:WSI)

9.4.1 Function Description

Function block FB 158 (PER:WSI) can be used to execute the same functions as function block FB 157 except that function block FB 158 transfers the parameters indirectly using the so–called working data block.

The working data block must beat least seven (eight) data words long for PLCs S5–115U and S5 – 135U (PLCs S5 – 150U and S5 – 155U). The number of the first relevant data word (DW n) can be determined with formal operands DBDW.

Function:

Control the IP 241 digital position encoder module with indirect parameterization

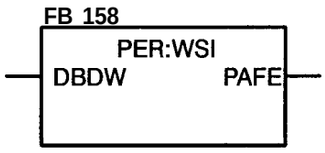
9.4.2 Calling the Function Block

In the STL (statement list)

PLCS5–115U
PLCS5–135U
PLCS5–150U/S
PLCS5–155U

```
      :JU FB158
NAME  :PER:WSI
DBDW  :
PAFE  :
```

in the LAD/CSF (ladder diagram/control system flow chart)



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9.4.3 Explanation of Parameters

NAME	CLASS	TYPE	DESIGNATION
DBDW	D	KY	Specification of the working data block, first data word (DW n) used
PAFE	A	BI	Parameterization error

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9.4.4 Parameter Assignment

DBDW : KY = x, y

x = Number of the working data block
1< x ≤ 255
2< x ≤ 255 for PLCSS5–135U and S5– 155U

Y = Number Of the first data word (DW n) used
When the user data block and the working data block are identical, the first data word used of the working data block must be equal to or greater than data word DW 187.

PAFE : In case of illegal parameterization, the signal status is"1". The recognized error is then shown by the assignment of flag byte FY 255.

F 255.0	SP bit error is set when the SP bit is not reset by the module within a certain period of time after an access.
F 255.1	Data word DR 182 or DR 184 of the "number" parameter to be transferred when the "PR" or "MB" command is selected is outside the range from O to 15 or the channel number in data word DL 182 or DL 184 is not zero or 16 for channel 1 or 2 respectively.
F 255.2	The specified user data block number is zero or one. (One for PLCS S5–135U and S5–155U only)
F 255.3	The specified working data block or user data block does not exist or is too short.
F 255.4	The command in data word DW n of the working data block cannot be interpreted.
F 255.5	The ABIT parameter in data word DW n+7 of the working data block is outside the specified range. (Not assigned for PLCSS5-115U and S5–135U)
F 255.6	The track number is outside the specified range. (Data word DL n+1 of the working data block)
F 255.7	The specified user data block has no parameterization identifier (is entered by FB 156).

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9.4.5 Working Data Block Assignment

The organization of the parameter list in the working data block is shown below.

DW n	Command				KS
DW n+1	Track number		User DB number		KY
DW n+2	V①	x	"0"/4	104	KH
DW n+3	10^3	10^2	10^1	10^0	KH
DW n+4	Track identifier bits, channel 1				KM
DW n+5	Track identifier bits, channel 2				KM
DW n+6	Assigned		Synchro. –interrupt info.		KM
DW n+7	Enable for reset		Number of the alarm bit		KY

The entries shown in bold face boxes in the working data block must be saved during interrupt processing at the beginning of the interrupt organization block, and reloaded before the interrupt organization block is exited if function block FB 158 is called from there.

The meaning of the individual entries is explained below.

Data word DW n must be supplied with the desired command from the following command list.

KS = KB Only output of identifier bits and control bits
KS = AE Change setpoints of one track
KS = SS Software synchronization
KS = SH Hardware synchronization
KS = IW Output of the actual value
KS = AW Output of the initial setpoint
KS = EW Output of the end setpoint
KS = N1 Read zero shift, channel 1
KS = N2 Read zero shift, channel 2
KS = IV Inhibit interrupt for supply
KS = IS Inhibit interrupt
KS = PR Transfer verify-read number to IP
KS = MB Calculate average value
KS = RV Specify interrupt direction

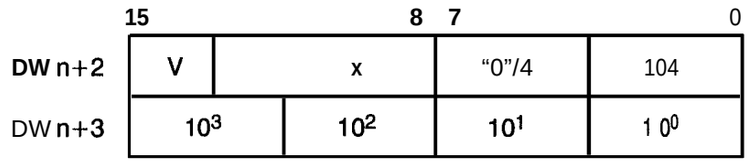
① V = sign, "O" positive
"1" negative

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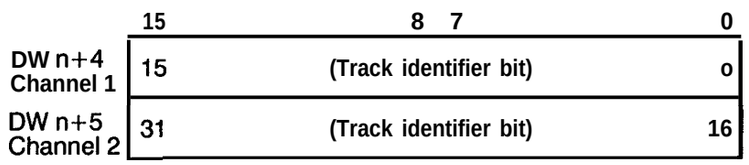
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Depending on whether the command parameter (DW n) contains the command "IW", "AW", "EW", "N1" or "N2", either the actual value, the initial setpoint, the end setpoint, the zero shift of channel 1 or the zero shift of channel 2 is stored in data word DW n+2 or DW n+3.

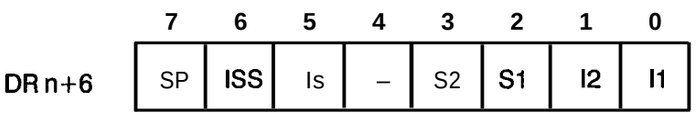
Any interrupt processing of a setpoint is indicated in data word DW n+2 (setpoint with interrupt → assignment of bits 4 to 7 of DW n+2: 0100 = 4). The bit assignment is shown below.



The contents of data word DW n+4 or DW n+5 indicate the track identifier bits of channel 1 or 2. The setup is shown below.



Data word DR n+6 contains the synchronization bits, the interrupt bits for each channel and the status information concerning an alarm inhibit (see operating instructions).



I1/I2	Interrupt in channel 1/2
S1/S2	Channel 1/2 synchronized
IS	All interrupts inhibited (Bits IS and ISS are set when E3 is transferred.)
ISS	Interrupt for supplying the module with new setpoints is inhibited (by transferring E4).
SP	SP bit

Data word DW n+7 must not be supplied unless programmable controller S5–150U/S or S5–155U in 150U mode is used.

DL n+7	Enable for reset	
	x >< 0	No reset
	x = 0	Reset applicable alarm bit in the system data
DR n+7	Number of the alarm bit	
	$0 \leq y \leq 7$	

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9.4.6 Technical Specifications

Block no.	158			
Block name	PER:WSI			
PLC S5–	115U	135U	150U/S	155U
Library no. P71200–S...	5158–A–1	91 58–A–1	41 58–A–1	6158–B–1
Call length (in words)	4			
Block length (in words)	1118	952	1246	738
Processing time in msec				
For BEF =	CPU 941A/B	CPU 922		
KB	8.71 3.5	3.9	0.6	0.6
IW, AW, EW, N1, N2	27.0/ 9.0	8.2	1.3	1.2
SS, SH	32.0/ 10.5	9.7	2.1	1.9
AE	53.0/ 18.2	16.0	6.2	5.9
PR, MB, RV	30.0/ 9.9	9.7	1.8	1.8
Is, Iv	30.0/ 9.3	7.3	1,1	1.2
For BEF =	CPU 942A/B	CPU 928A/B		
KB	7.0/ 3.5	2.5/ 1.3		
IW, AW, EW, N1, N2	13.5/ 9.0	4.7/ 1.9		
SS, SH	18.0/ 10.5	5.9/ 2.3		
AE	31.0/ 18.2	11.1 / 6.0		
PR, MB, RV	16.0/ 9.9	5.71 2.0		
Is, Iv	14.0/ 9.3	4.2/ 1.6		
For BEF =	CPU 943A/B			
KB	3.5/ 3.1			
IW, AW, EW, N1, N2	9.0/ 8.0			
SS, SH	1 1.0/ 10.0			
AE	19.5/ 17.7			
PR, MB, RV	1 1.5/ 9.3			
Is, Iv	9.51 8.7			
For BEF =	CPU 944A/B			
KB	0.7/ 0.7			
IW, AW, EW, N1, N2	2.0/ 2.0			
SS, SH	2.3/ 2.2			
AE	7.5/ 6.2			
PR, MB, RV	2.5/ 2.0			
Is, Iv	2.0/ 1.9			
Nesting depth	0			
Subordinate blocks	None			

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Assignment in data area	User data block up to and including DW 186			
	User data block requires x data words for parameter transfer.			
	x = 7		x = 8	
Assignment in flag area	FY 225 to FY 255			FY 221 to FY255
Assignment in system area	–	BS 60 to BS 63	–	BS 180 to BS 183
System instructions	Yes			
Other	①	–	–	②

① Interrupts (interrupts and alarms) are temporarily inhibited in the block with the AS/AF commands. This also cancels any “AS” command programmed by the user.

② Interrupts (process alarms, interrupts and alarms) are inhibited in the block for approximately 0.2 msec. This also cancels any “AS” command programmed by the user.

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9.4.7 Use of the Function Block

The module must be parameterized with function block FB 156 before function block FB 158 can be called.

The parameter transfer is performed via the working data block. The function to be executed by function block FB 158 is selected by entering the appropriate command code in format KS in data word DW n.

Before a new command is entered in data word DW n in the working data block, a check must be performed to determine whether the contents have been deleted by function block FB 158 (DW n KH = 0000). The procedure is shown in the following pictogram.

Contents of data word DW n in working data block equal zero?	
Yes	No
Write new command in DW n	–
Call function block FB 158	

Calling function block FB 158 with KH = 0000 in data word DW n of the working data block causes the block to be exited without triggering a function (idling).

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Read actual value (IW)

Parametrize the working data block as shown below.

DW n	IW		KS	Input
DW n+1	Track number	User DB	KY	Input
DW n+2	Actual value (sign + dec. 4)		KH	output
DW n+3	Actual value (dec. O to dec. 3)		KH	output
DW n+4	Track identfier bits, channel 1		KM	output
DW n+5	Track identifier bits, channel 2		KM	output
DW n+6	Assigned	ST parameter	KM	Output control bits
DW n+7	O or 255	Alarm bit O to 7	KY	Input *)

*) This parameter is used for PLCs S5–150U/S and S5–155U in 150U mode during interrupt processing (see section 9.4,8),

When the track number (DL n+1) is less than 16, channel 1 is selected, otherwise channel 2.

The data block number of the user data block (DR n+1) must be the same data block number used also during startup in connection with function block FB 156.

Read track identifier bits (KB)

Parametrize the working data block as shown below.

DW n	KB		KS	Input
DW n+1	Track number	User DB	KY	Input
DW n+2				Unaffected
DW n+3				Unaffected
DW n+4	Track identifier bits, channel 1		KM	output
DW n+5	Track identifier bits, channel 2		KM	output
DW n+6	Assigned	ST parameter	KM	Output of control bits
DW n+7	O or 255	Alarm bit O to 7	KY	Input *)

*) This parameter is used for PLCs S5–150U/S and S5–155U in 150U mode during interrupt processing (see section 9.4.8).

Entry of the track number parameter(DL n+ 1) has no effect on the “read track identifier bits” function.

The data block number of the user data block (DR n+1) must be the same data block number used also during startup in connection with function block FB 156.

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Changing the setpoints (AE)

Parameterize the working data block as shown below.

DW n	AE		KS	Input
DW n+1	Track number	User–DB	KY	Input
DW n+2				Unaffected
DW n+3				Unaffected
DW n+4	Track identifier bits, channel 1		KM	output
DW n+5	Track identifier bits, channel 2		KM	output
DW n+6	Assigned	ST parameter	KM	Output of control bits
DW n+7	O or 255	Alarm bit O to 7	KY	Input *)

*) This parameter is used for PLCS S5–150U/S and S5–155U in 150U mode during interrupt processing (see section 9.4.8).

The track number (DL n+1) must be between zero and 31 depending on the desired track.

The data block number of the user data block (DR n+1) must be the same data block number used also during startup in connection with function block FB 156.

The setpoints to be changed are located in the user data block used to parameterize the mo-dule (see FB 156 description for assignment). The initial and the end setpoint must be specified for each track. The track is deleted for interrupt identifier KH = FFFF.

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Software synchronization (SS)
Hardware synchronization (SH)

Parametrize the working data block as shown below.

DW n	SS or SH		KS	Input
DW n+1	Track number	User DB	KY	Input
DW n+2				Unaffected
DW n+3				Unaffected
DW n+4	Track identifier bits, channel 1		KM	output
DW n+5	Track identifier bits, channel 2		KM	output
DW n+6	Assigned	ST parameter	KM	Output of control bits
DW n+7	O or 255	Alarm bit O to 7	KY	Input *)

*) This parameter is used for PLCS S5-150U/S and S5-155U in 150U mode during interrupt processing (see section 9.4.8).

Supply data word DL n+1 with the value 32 (33) to synchronize channel 1 (2).

The data block number of the user data block (DR n+1) must be the same data block number used also during startup in connection with function block FB 156.

When the "SH" command is used, the NV values are transferred without the SS bit; this is required for hardware synchronization with preliminary contact and zero mark (see operating instructions).

When the "SS" command is used, the NV values are transferred with the SS bit; this provides a software synchronization of the counters. Synchronization should only be used for incremental encoders.

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Read initial setpoint (AW)
Read end value (EW)

Parametrize the working data block as shown below.

DW n	AW or EW		KS Input
DW n+1	Track number	User DB	KY Input
DW n+2	Setpoint (sign + dec. 4)		KH Output, inital/end setpoint
DW n+3	Setpoint (dec. O to dec. 3)		KH Output, initial/end sepoint
DW n+4	Track identifier bits, channel 1		KM Output
DW n+5	Track identifier bits, channel 2		KM Output
DW n+6	Assigned	ST parameter	KM Output control bits
DW n+7	O or 255	Alarm bit O to 7	KY Input ●)

*) This parameter is used for PLCs S5-150U/S and S5-155U in 150U mode during interrupt processing (see section 9.4.8).

The track number (DL n+ 1) must be located between zero and 31 depending on the desired track.

The data block number of the user data block (DRn+1) must be the same data block number used also during startup in connection with function block FB 156.

Read zero shift, channel 1 (N1)
Read zero shift, channel 2 (N2)

Parameterize the working data block as shown below.

DW n	N1 or N2		KS Input
DW n+1	Track number	User DB	KY Input
DW n+2	NV (sign + dec. 4)		KH Output NV, channel 1 or 2
DW n+3	NV (dec. O to dec. 3)		KH Output NV, channel 1 or 2
DW n+4	Track identifier bits, channel 1		KM Output
DW n+5	Track identifier bits, channel 2		KM Output
DW n+6	Assigned	ST parameter	KM Output control bits
DW n+7	O or 255	Alarm bit O to 7	KY Input*)

*) This parameter is used for PLCs S5-150U/S and S5-155U in 150U mode during interrupt processing (see section 9.4.8).

The track number (DL n+1) can be disregarded for the output of the zero shift.

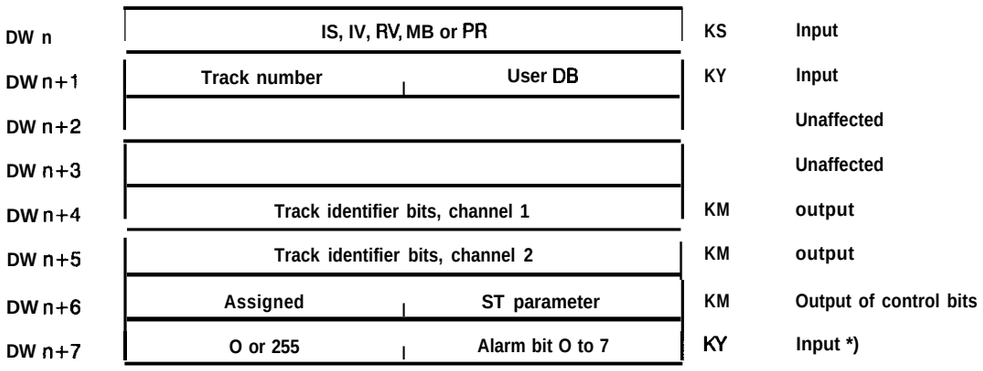
The data block number of the user data block (DRn+1) must be the same data block number used also during startup in connection with function block FB 156.

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Inhibit interrupt (IS)
Inhibit interrupt for supplying new setpoints to the module (IV)
Inhibit interrupt depending on direction (RV)
Calculate average value (MB)
Verify-read (PR)

Parametrize the working data block as shown below.



*) This parameter is used for PLCS S5-150U/S and S5-155U in 150U mode during interrupt processing (see section 9.4.8).

The track number (DL n+1) can be disregarded for the IS, IV, RV, MB and PR functions.

The data block number of the user data block (DR n+1) must be the same data block number used also during startup in connection with function block FB 156.

See the description of function block FB 157 (section 9.3.7) for more details on handling the "inhibit interrupt" and "inhibit interrupt for supply" functions.

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9.4.8 Processing Interrupts

See the description of function block FB 157 for the processing of interrupts. Only the differences will be covered here.

Data word Dw n+7 in the working data block of function block FB 158 corresponds to the ABIT parameter of function block FB 157.

DW n+7:	KY = x, y x = 255, y = 255	Module without interrupt
	x = 0, y = 0 to 7	Reset appropriate alarm bits in the system data

A block of the alarm–controlled processing is called when an interrupt occurs (based on the jumper setting). The scratchpad flags must be saved at the beginning of this block, and reloaded from it again at the end.

If function block FB 158 is to be used in this block with the same working data block as in cycle, the parameters stored in the working data block must be saved in a data block at the beginning, and reloaded again at the end.

DW n	Command		KS
DW n+1	Track number	User DB	KY
DW n+2			
DW n+3			
DW n+4			
DW n+5			
DW n+6	Assigned	ST parameter	KM
DW n+7	0 or 255	Alarm bit 0 to 7	KY

The interrupt processing block contains the call of function block FB 158. Parameter DW n of the working data block must be supplied with the “KB” command before this function block is called. After function block FB 158 is called, the ST parameter indicates which channel triggered the interrupt. A special “interrupt program” can now be processed.

When an interrupt occurs during the processing of function block FB 158 in the cyclic program, the group alarm on the bus is deleted again in FB 158 during reading of byte 7. This means that no organization block of alarm–controlled processing is called. However, function block FB 158 does update the control bits (DR n+6) so that an alarm program can then be called based on the interrupt bits. Evaluation must be performed, however, before the cyclic control information is loaded in data word DR n+6.

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Alarm processing may only be performed at block boundaries (exception: PLCS S5–155U and S5–115U).

Example:

Program in 062:

– Save scratchpad flags

–Save DW n, DL n+1, DR n+6 and DW n+7

```
      : A     DB 158
      : L     KS KB
      : T     DW n
      : L     KY 0,0
      : T     DW n+7

      : JU  FB  158
NAME : PER:WSI
DBDW :        KY  158,n
PAFE :

      : L     DW n+6
      : T     FY 191

      : O     F   190.0
      : O     F   191.0
      : JC    FB  xx
      : O     F   190.1
      : O     F   191.1
      : JC    FB  yy

      : L     KBO
      : T     FY 190
      : T     FY 191
```

- Load DW n, DL n+1, DR n+6 and DW n+7

- Load scratchpad flags

```
      : BE
```

FB xx = Your own alarm program for channel 1
FB yy = Your own alarm program for channel 2

Program in 061:

```
      : A     DB 158
      : L     KS xx
      : T     DW n
      : L     KY 0,0
      : T     DW n+7

      : JU  FB  158
NAME : PER:WSI
DBDW :        KY  158,n
PAFE :

      : L     DW n+6
      : T     FY 190

      : U     F   190.0
      : JC    FB  xx
      : U     F   190.1
      : JC    FB  yy
```

After the control bits have been evaluated in the alarm–controlled program, they must be reset or the alarm programs (FBxx and FByy) might be processed again during the cyclic program.

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9.5 Example

This example shows the operation of the digital position decoder IP 241. By means of a simulator, the individual functions can be selected via digital inputs; the signal states can be displayed via digital outputs. It explains how a channel is parameterized with an incremental encoder module. The actual value and the track identifier bits can be read and, depending on the parameterization, a process interrupt can be triggered.

This example also describes the required jumper settings. It can be used as a test program to check jumper settings or module functions.

9.5.1 Device Configuration

For a test of the digital position decoder IP 241, the following devices can be used:

– One of the mentioned programmable controllers

– Programmer (e.g., PG 750)

– Digital position decoder (basic module) IP 241
(6ES5 241–IAA12) with a 50–way sub D connector

- Encoder matching module, incremental (6ES5 241 -1 AB12)

– Rotary transducer (5 V), symmetrical operation and two-phase displaced pulse sequences

– Digital input module; front connector with screw mounting

– Digital output module; front connector with screw mounting

– 1 Simulator(6ES5788–01A12)

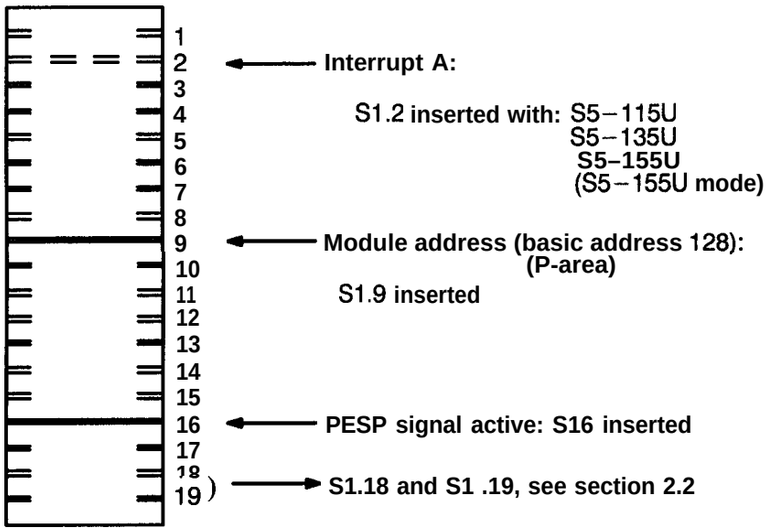
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9.5.2 Jumper Assignment of the Digital Position Decoder

Jumper assignment on the basic module

DIP switch S1



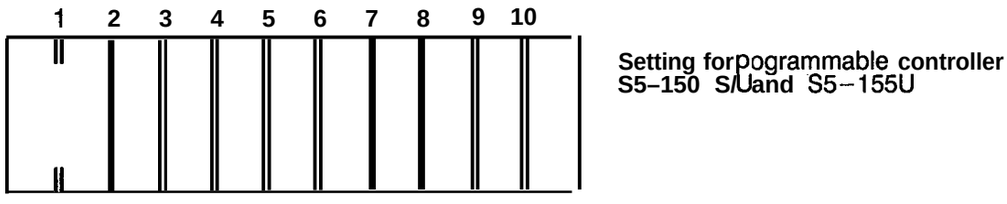
As the transducer voltage is 5 V, the following resistor values must be soldered in on the basic module:

R27	39 kΩ
R18	82 Ω
R30	open

Interrupt processing:

For the interrupt processing (see section 2.4), the digital position decoder IP 241 is coded as a master module.

DIP switch



In this example, all jumpers of switch S2 must be opened for all other programmable controllers.

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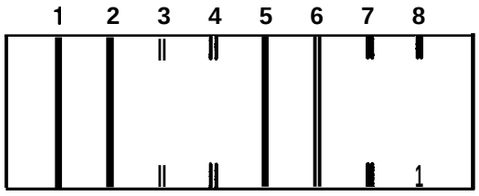
Jumper assignment of the incremental encoder matching module

Assuming that an encoder with a symmetrical line (5 V input voltage) is used (providing two-phase displaced pulse sequences) and that the evaluation of two signal edges is selected, then the following jumpers and components must be soldered in (configuration at delivery):

Solder jumpers:	**R4, R6, R7, R9, R12, R14**
Capacitors:	**Cl, C2, C5 (1 O nF for all)**
Resistor R11:	**2.2 kΩ (for a 24 V voltage at the preliminary contact)**

DIP switch S2.1: **open**

DIP switch S1



S1.1 closed
S1.2 closed
S1.5 closed
S1.6 closed

The encoder matching module is inserted into the slot for channel 1.

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9.5.3 Assignment of the Inputs and Outputs

The program is designed in a way that allows easy adaptation to different input and output assignments. The program blocks PB 11, PB 12, PB 13, FB 11 and FB 12 contain the test program and work with flags only. The inputs and outputs to be used are allocated to these flags in organization blocks (OB 1, OB2, OB20, OB21, and OB 22). Intheexamplethey are input word IW 4 and output word QW4and in case oftheS5–115U, input word IW 4 and output word QW8. The output Q5.7 (Q9.7 with theS5–115U) is firmly assigned as "interrupt output".

14.0	IW	Read actual value channel 1
14.1	AW	Read initial setpoint track 4
14.2	EW	Read end setpoint track 4
14.3	SS	Software-based synchronizing channel 1
14.4	AE	Modify setpoints for track 4
14.5	Is	Inhibit interrupt
14.6	Iv	Inhibit interrupt for supplying the module with new setpoints
14.7	N1	Read zero shift, channel 1
15.0	N2	**Read zero shift, channel 2**
15.1	PR	**Activate "verify-read" special function**
15.2	MB	**Activate "calculate average value" special function**
15.3	RV	Inhibit interrupt depending on direction
15.4	–	
15.5	–	
15.6	"O": indirect parameterization (FB 158), "1": direct parameterization (FB 157)	
15.7	Reset alarm output Q5.7	
Q4.0 / Q8.0	**Parameter PAFE (FB 156 in start-up)**	
Q4.1 / Q8.1	**Parameter SPFE (FB 156 in start-up)**	
Q4.2 / Q8.2	**Parameter PAFE (FB 157 or FB 158 in interrupt program)**	
Q4.3 I Q8.3	**Parameter SPFE (FB 157 or FB 158 in interrupt program)**	
Q4.4 / Q8.4	–	
Q4.5 / Q8.5	–	
Q4.6 I Q8.6	Group signal parameter PAFE (FB 157 or FB 158 in cyclic program)	
Q4.7 / Q8.7	Group signal parameter SPFE (FB 157 or FB 158 in cyclic program)	
Q5.0 / Q9.0		
Q5.1 / Q9.1		
Q5.2 / Q9.2	–	
Q5.3 / Q9.3	–	
Q5.4 / Q9.4	–	
Q5.5 / Q9.5	Channel 1 synchronized	
Q5.6 / Q9.6	–	
Q5.7 I Q9.7	Interrupt output (has signal status"1" after an interrupt)	

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9.5.4 Turn–On, Start-Up Behavior

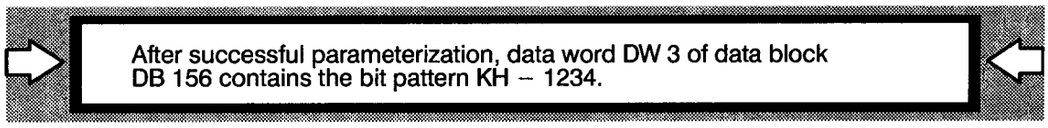
The program is completely loaded from the floppy disk to the user memory of the programmable controller.

For the start-up the digital position decoder is supplied with the respective setpoints for the individual tracks and with the zero shift. This is done with function block FB 156. The setpoints are contained in the user data block; in our example it is data block DB 156 which is already full and available on the floppy disk.

If the programmable controller is turnedon when all simulator inputs are in switch position “O”, no output may be set after the start-up of the programmable controller. If the output Q 4.0/ Q 8.0 is set, a parameterization error occurred during start-up (parameter PAFE).

The exact error cause can then be read at flag byte FY 18. This flag byte is assigned in accordance with the error byte FY 255 of the standard function block FB 156 (see programming instructions). At the output Q 4.1/Q 8.1 the SPFE parameter (SP bit error) in function block FB 156 is shown.

All enabled track setpoints in user data block DB 156 are transferred to the module; in the example these are the setpoints for tracks O to 5.



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9.5.5 Cyclic Operation

During cyclic operation, input 15.6 in the organization block can be used to choose between indirect parameterization (15.6 = "O") and direct parameterization (15.6 ="1 "). Function block FB 11 is called for indirect parameterization and program block PB 11 for direct parameterization.

The "parameterization error" bit in the "PAFE" parameter is set if the parameters are modified incorrectly when function block FB 157 is called. The same applies when working data block DB 158 is supplied with incorrect entries before function block FB 158 is called. In both cases, this parameterization error is indicated by the set output Q 4.6/Q 8.6.

Direct parameterization (PB 11)

A bit in flag byte FY 17 or FY 35 with signal status"1" indicates the call during which the error occurred (see program block PB 11). The detected error can then be read by the assignment of the applicable flag bytes (FY 20 to FY 31).

The SP bit errors occurring during the cycle are imaged in flag bytes FY 16 and FY 34 (SPFE parameter). Output Q 4.7 (Q 8.7) is set as the group signal when an error occurs here.

Indirect parameterization (FB 11)

When a parameterization error occurs, the cause of the error can be read in flag byte FY 20 (image of flag byte FY 255).

An SP bit error can be recognized by the set output Q 4.7/Q 4.8 in flag bit F 20.0 which has signal status"1".

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9.5.6 Reading the Actual Value

Direct parameterization (PB 11)

The actual value can be indicated on the PG monitor screen in flag double word FD 134 with the "control variable" PG function. Function block FB 157 can be called with BEF = IW via input 14.0, and the actual value can be viewed as follows:

FD 134 KH = 800F FFFF

Indirect parameterization (FB 11)

Using the "control variable" PG function, the actual value can also be monitored herein DD 3 of working data block FB 158. When input 14.0 is activated, the "IW" command is entered in DW 1 of working data block FB 158. The subsequent call of function block FB 158 outputs the actual value in data double word DD 3 as shown below.

DB 158
DD 3 KH = 800F FFFF

In both cases, the actual is not yet output after switchon (indication KH = 800F FFFF) since the incremental encoder matching module must be synchronized first. This is also indicated by the lighted red LED SYN.1 on the front of the module.

9.5.7 Synchronizing the Encoder Matching Module

During synchronization, the encoder matching module is set to the value which indicates the zero shift (in user data block DB 156 in data double word DD 171 for channel 1).

Software-based synchronization is activated by the input 14.3.

Successful synchronization is indicated by the module, when the red synchronization LED on the front goes off. If the read actual value display is still on the programmer screen and the reading operation for actual values is still activated (via input 14.0), output Q5.5/Q9.5 is set ("channel 1 synchronized") and immediately after synchronization the actual value displays the zero shift value, In the example the value –250 is shown:

FD 134 KH = 80000250 (direct parameterization)

DB 158
DD 3 KH = 80000250 (indirect parameterization)

To observe changes in the actual values continuously, input 14.0 should be turned on permanently.

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9.5.8 Reading Track Identifier Bits

Direct parameterization (PB 11)

The track identifier bits are located in flag double word FD 130. The track identifier bits for channel 1 are found in flag word FW 132, and can be displayed on the monitor screen of the programmer using the "control variable" PG function (it is best to use the KM format as bit pattern). They are updated each time function block FB 157 is called.

Indirect parameterization (FB 11)

The track identifier bits are located in data double word DD 5 of working data block DB 158. Data word DW 5 contains the track identifier bits of channel 1; data word 6 contains those from channel 2. The track identifier bits are also updated in function block FB 158 if function block FB 158 was supplied with a valid command via working data block FB 158.

Depending on the actual value, the track identifier bits are set sequentially:

Track O:	from –00100 to –00050	track identifier bit O
Track 1:	from –00050 to 00000	track identifier bit 1
Track 2:	from 00000 to 00100	track identifier bit 2
Track 3:	from 00100 to 00200	track identifier bit 3
Track 4:	from 00200 to 00300	track identifier bit 4
Track 5:	from 00300 to 00400	track identifier bit 5

The remaining tracks are not parameterized, as the respective first data words do not contain an enable (see assignment of user data block DB 156).

After synchronization the actual value is –250. If pulses in positive direction are acquired now, then starting at value –100, the track identifier bit O is set; at value –50, bit O is reset, and so on. In our example, the tracks are assigned in a way that the track identifier bits continuously have signal status"1" one after the other. Also, any other different values for the setpoints can be written into the user data block. These values are transferred to the module during start-up.

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9.5.9 Reading Setpoints

Direct parameterization (PB 11)

By means of input 14.1, the initial setpoint for track 4 can be read; input 14.2 gives the end setpoint. Both setpoints are shown in the flag double words FD 138 and FD 142. By setting input signal 14.7 or 15.0, the zero shift for channel 1 or 2 stored in the module can be assigned to flag double word FD 150 or FD 154. With the programmer function "control variable" this looks as follows:

FD 134	KH = 00000225	(actual value)
FW 132	KH = 0000000000010000	(track identifier bit 4 set)
FD 138	KH = 00000200	(initial setpoint track 4)
FD 142	KH = 00000300	(end setpoint track 4)
FD 150	KH = 80000250	(zero shift, channel 1)
FD 154	KH = 00000000	(zero shift, channel 2)

If inputs 14.0,14.1, and 14.2 are permanently on, the changing of the actual value, the identifier bits and the track setpoints for track 4 can be observed directly on the viewing screen.

Indirect parameterization (FB 11)

The assignment for triggering the setpoint output to inputs 14.0, 14.1, 14.2, 14.7 and 15.0 corresponds to that for direct parameterization. With the exception of the track identifier bits, all setpoints and actual values are stored in data double word DD 3 in working data block DB 158. Data word DW 5 indicates information concerning the track identifier bits of channel 1.

In contrast to direct parameterization, only one setpoint or actual value can be monitored in data double word DD 3 of working data block DB 158.

9.5.10 Modifying Setpoints for Track 4

The setpoints for track 4 are contained in user data block DB 156 in the data words DW 30 through DW 34. In order to supply these with new values easily, the screen display of the programmer can be expanded as follows:

DB 156		(User data block)
DW 30	KH – 0000	(Interrupt preelection)
DD 31	KH – 00000200	(initial setpoint)
DD 33	KH – 00000300	(End setpoint)

Now the new setpoints in the module can be monitored as shown below based on the type of parameterization selected.

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Direct **parameterization (PB 11)**

FD 134	KH – 00000225	(Actual value)
FW 132	KM – 0000000000010000	(Track identifier bit 4 set)
FD 138	KH – 00000200	(Initial setpoint track 4)
FD 142	KH – 00000300	(End setpoint track 4)

Indirect **parameterization (FB 11)**

The information about the actual value or the setpoints can be read in data double word DD 3 of working data block DB 158. Their contents are identical to those of direct parameterization. In contrast, the track identifier bits are located in data word DW 5 of the same data block.

The programmer can now be used to specify new setpoints for track 4. For example:

DB 156		(User data block)
DW 30	KH – 0000	(Interrupt preelection)
DD 31	KH – 00000250	(Initial setpoint)
DD 33	KH – 00000350	(End setpoint)

After the values in user data block DB 156 are changed with the "control variable" PG function and the status display is activated, the setpoints in the flag double words (direct parameterization) or in the data words of working data block DB 158 (indirect parameterization) still show the old values. The setpoints are transferred to the module only when input 14.4 is activated.

If, as shown above, the actual value is between the old initial value (200) and the new initial value (250), no track identifier bit is set after the parameterization:

Direct **parameterization (PB 11)**

FD 134	KH – 00000225	(Actual value)
FW 132	KM – 0000000000000000	(Track identifier bit 4 not set)
FD 138	KH – 00000250	(Initial setpoint track 4)
FD 142	KH – 00000350	(End setpoint track 4)

Indirect **parameterization (FB 11)**

The desired information can also be obtained here, as described above, from data double word DD 3 or data word DW 5 in working data block DB 158.

If positive pulses are acquired, starting with value 250, track identifier bit 4 is set. Starting with value 300, two track identifier bits (bit 4 and bit 5) have the signal status"1". Above value 350, only bit 5 is left.

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9.5.11 Control Interrupt Triggering

If the interrupts assigned to the applicable tracks were enabled during startup, they can be temporarily inhibited during the cycle. All interrupts can be inhibited by setting input 14.5. Another activation of input 14.5 cancels the interrupt inhibit. The status byte then has the following bit pattern.

Direct parameterization (PB 11)

FY 132	KM = 0110XXM	(Control information: interrupts inhibited x = "O" or"1" depending on the processing point)
FY 132	KM = 0000xxxx	(Control information: interrupts not inhibited x = "O" or"1" depending on the processing point)

Indirect parameterization (FB 11)

DB 158		(Working data block)
DR 7	KM = 01 10xxxx	(Control information: interrupts inhibited x = "O" or"1" depending on the processing point)
DR 7	KM = 0000xxxx	(Control information: interrupts not inhibited x = "O" or "I" depending on the processing point)

Input 14.6 can only be used to affect the interrupt generated by the module while modifying track setpoints. This interrupt is also inhibited by a one–time activation of input I 4.6; the interrupt is enabled by repeating the procedure. The status information is as follows:

Direct parameterization (PB 11)

FY 132	KM = OO1O)O(XX	(Control information: interrupt inhibited for supply, x = "O" or"1" depending on the processing point)
FY 132	KM = 0000xxxx	(Control information: interrupt not inhibited for supply, x = "O" or"1" depending on the processing point)

Indirect parameterization (FB 11)

DB 158		(Working data block)
DR 7	KM = OO1Oxxxx	(Control information: interrupt inhibited for supply, x = "O" or"1" depending on the processing point)
DR 7	KM = 0000xxxx	(Control information: interrupt not inhibited for supply, x = "O" or"1" depending on the processing point)

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9.5.12 Inhibit Interrupt Depending on Direction

This function requires that the desired interrupts have been enabled in user data block DB 156 during startup. The desired inhibit direction must first be stored in data word DW 186 of user data block FB 156 before this function can be activated with input 15.3.

```
DB  156                                  (User data block)
DW  186      KM = 0000000000000001       (interrupt inhibited for backwards direction)
```

9.5.13 Special Function: Verify–Read and Calculate Average Value

This special function requires two parameters each which must be supplied in user data block DB 156, These parameters are “channel no.” and “number”. The “channel no.” parameter is used to select channel 1 with the value zero, and channel 2 with the value 16. The supply range of the “number” parameter is between zero and 15, and classifies the range of activity of the special function.

The parameters of the desired special function are transferred to the module by setting input 15.1 for “verify–read” and 15.2 for “calculate average value”.

Verify-read/calculate average value

```
DB  156                                  (User data block)
DW  182      KY = 0,13                   (Verify-read)
DW  184      KY = 0,7                    (Calculate average value)
```


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9.5.14 Process Alarm Processing

The interrupt processing for this example is programmed in organization block062.

Depending on the type of programmable controller used, the process interrupts are acquired via the input byte IB 0 (with S5–150U/S, S5–155U in S5–150U mode) or via an interrupt line (with S5–115U, S5–135U, and S5–155U in S5–155U mode).

At the start of an interrupt block, the scratchpad flags must be saved and reloaded prior to leaving the block. With the S5– 155U this is accomplished with the standard function blocks FB 38 and FB 39. These function blocks are part of the standard function block package “basic functions”.

Saving and reloading of the scratchpad flags must be performed for all types of interrupt–controlled program processing (also in the organization blocks for restart and error evaluation). In each case a different data area must be used. (This is taken into consideration in the example.)

Exception PLCS5-155U:

Function blocks FB 38 and FB 39 establish a stack in the data block, where the status of the scratchpad flags and some system data words are stored. (Also stored are the system data RS 60 to RS 63, enabled for the user.) The data block can be set up to data wordDW816. Function blocks FB 38 and FB 39 must be used in pairs under all circumstances (i.e., an organization block programmed with these blocks may not be left prematurely with the conditional block end BEC).

In interrupt processing organization block062, function block FB 12 (call FB 158) is activated for indirect parameterization and program block PB 12 (call FB 157) for direct parameterization. The track identifier bits are updated in both blocks with the “KB” command. Input bit 15.6 can be used to choose between indirect (1 5.6 = “O”) and direct parameterization (1 5.6 = “1 “).

Interrupt for end setpoint of track 4

The end setpoint of track 4 is supplied with an interrupt identifier. For this purpose the value of the right data byte DR 30 in user data block DB 156 must be other than zero. This can be performed with the programmer function “control variable”. After parameterization via input 14.4, the screen display appears as follows:

Direct parameterization (PB 12)

FD 134	KH – 00000572	(Actual value)
FW 132	KM – 0000000000000000	(Track identifier bits)
FD 138	KH – 00000250	(Initial setpoint track 4)
FD 142	KH – 00400350	(End setpoint track 4)

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Indirect **parameterization (FB** 12)

```
DB 158                                    (Working data block)
DD 3        KH = 00000572                 (Actual value)
DD 5        KM = 0000000000000000         (Track identifier bits)
DD 3        KH = 00000250                 (Initial setpoint track 4)
DD 3        KH = 00000350                 (End setpoint track 4)
```

The actual value, initial cam value and end cam value cannot be output simultaneously when indirect parameterization is used.

```
DB 156                                    (User data)
DW 30       KH = 0001                     (Interrupt preelection)
DD 31       KH = 00000250                 (Initial setpoint)
DD 33       KH = 00000350                 (End setpoint)
```

During parameterization an interrupt can be triggered, depending on the position of the actual value. If this occurs, the output Q 5.7/Q 9.7 is set. Via input 15.7, the output Q 5 .7/Q 9.7 can be reset.

When (in the example) the actual value reaches the end cam value for track 4, an interrupt is triggered. This occurs independently from the direction from which the actual value approaches when no interrupt direction is inhibited with the "inhibit interrupt depending on direction" special function.

It is also possible to supply both setpoints with interrupt identifiers. Then, whenever the actual value enters or leaves track 4, an interrupt is triggered. The screen display then appears as follows:

Direct **parameterization** (PB 12)

```
FD 134      KH – 00000311                 (Actual value)
FW 132      KM – 0000000000110000         (Track identifier bits)
FD 138      KH – 00400250                 (Initial setpoint track 4)
FD 142      KH – 00400350                 (End setpoint track 4)
```

Indirect **parameterization (FB** 12)

```
DB 158                                    (Working data block)
DD 3        KH = 00000311                 (Actual value)
DW 5        KM = 0000000000110000         (Track identifier bits)
DD 3        KH = 00000250                 (Initial setpoint track 4)
DD 3        KH = 00000350                 (End setpoint track 4)
```

The actual value, initial cam value and end cam value cannot be output simultaneously when indirect parameterization is used.

```
DB 156                                    (User data block)
DW 30       KH – 0101                     (Interrupt preelection)
DD 31       KH – 00000250                 (Initial setpoint)
DD 33       KH – 00000350                 (End setpoint)
```

In accordance with the above example, all functions and all operating modes of the digital position decoder IP 241 can be tested by specific entries into data block DB 156.

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9.5.15 Parameterization Data Block for the Digital Position Decoder

In the example, data block DB 156 is used.

```
DB156                                                    LE= 193

                    PARAMETERIZATION DATA BLOCK
 0:    KH =  0000;   #########  ########################
 1:    KH =  0000;   # OPERATING AREA FB 156, FB 157, FB 158    #
 2:    KH =  0000;   # ------------------------------#------
 3:    KH =  0000;   # PARAMETER IDENTIFICATION KH=1234
 4:    KH =  0000;   # ------------------------------#------
 5:    KH =  0000;   # MAY NOT BE CHANGED            #
 6:    KH =  0000;   #  ------------------------  --#------
 7:    KH =  0000;   # MW-STATUS: MONTH - YEAR       #
 8:    KH =  0000;   # MW-STATUS: DAY - /            #
 9:    KH =  0000;   ######  #########  ###################
10:    KH =  0000;   INTERRUPT ENABLE TRACK O
11:    KH =  F000;     INITIAL VALUE SIGN + DEC. 4
12:    KH =  0100;     INITIAL VALUE DEC. 3 + 2 + 1 + O
13:    KH =  F000;     END VALUE     SIGN + DEC. 4
14:    KH =  0050;     END VALUE     DEC. 3 + 2 + 1 + O
15:    KH =  0000;   INTERRUPT ENABLE TRACK 1
16:    KH =  F000;     INITIAL VALUE SIGN + DEC. 4
17:    KH =  0050;     INITIAL VALUE DEC. 3 + 2 + 1 + O
18:    KH =  0000;     END VALUE     SIGN + DEC. 4
19:    KH =  0000;     END VALUE     DEC. 3 + 2 + 1 + O
20:    KH =  0000;   INTERRUPT ENABLE TRACK 2
21:    KH =  0000;     INITIAL VALUE SIGN + DEC. 4
22:    KH =  0000;     INITIAL VALUE DEC. 3 + 2 + 1 + O
23:    KH =  0000;     END VALUE     SIGN + DEC. 4
24:    KH =  0100;     END VALUE     DEC. 3 + 2 + 1 + O
25:    KH =  0000;   INTERRUPT ENABLE TRACK 3
26:    KH =  0000;     INITIAL VALUE SIGN + DEC. 4
27:    KH =  0100;     INITIAL VALUE DEC. 3 + 2 + 1 + O
28:    KH =  0000;     END VALUE     SIGN + DEC. 4
29:    KH =  0200;     END VALUE     DEC. 3 + 2 + 1 + O
30:    KH =  0000;   INTERRUPT ENABLE TRACK 4
31:    KH =  0000;     INITIAL VALUE SIGN + DEC. 4
32:    KH =  0200;     INITIAL VALUE DEC. 3 + 2 + 1 + O
33:    KH =  0000;     END VALUE     SIGN + DEC. 4
34:    KH =  0300;     END VALUE     DEC. 3 + 2 + 1 + O
35:    KH =  0000;   INTERRUPT ENABLE TRACK 5
36:    KH =  0000;     INITIAL VALUE SIGN + DEC. 4
37:    KH =  0300;     INITIAL VALUE DEC. 3 + 2 + 1 + O
38:    KH =  0000;     END VALUE     SIGN + DEC. 4
39:    KH =  0400;     END VALUE     DEC. 3 + 2 + 1 + O
40:    KH =  FFFF;   INTERRUPT ENABLE TRACK 6
41:    KH =  0000;     INITIAL VALUE SIGN + DEC. 4
42:    KH =  0000;     INITIAL VALUE DEC. 3 + 2 + 1 + O
43:    KH =  0000;     END VALUE     SIGN + DEC. 4
44:    KH =  0000;     END VALUE     DEC. 3 + 2 + 1 + O
45:    KH =  FFFF;   INTERRUPT ENABLE TRACK 7
46:    KH =  0000;     INITIAL VALUE SIGN + DEC. 4
47:    KH =  0000;     INITIAL VALUE DEC. 3 + 2 + 1 + O
48:    KH =  0000;     END VALUE     SIGN + DEC. 4
49:    KH =  0000;     END VALUE     DEC. 3 + 2 + 1 + O
```


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50:	KH = FFFF:	INTERRUPT ENABLE TRACK 8
51:	KH = 0000:	INITIAL VALUE SIGN + DEC. 4
52:	KH = 0000:	INITIAL VALUE DEC. 3 + 2 + 1 + O
53:	KH = 0000:	END VALUE SIGN + DEC. 4
54:	KH = 0000:	END VALUE DEC. 3 + 2 + 1 + O
55:	KH = FFFF:	INTERRUPT ENABLE TRACK 9
56:	KH = 0000:	INITIAL VALUE SIGN + DEC. 4
57:	KH = 0000:	INITIAL VALUE DEC. 3 + 2 + 1 + O
58:	KH = 0000:	END VALUE SIGN + DEC. 4
59:	KH = 0000:	END VALUE DEC. 3 + 2 + 1 + O
60:	KH = FFFF:	INTERRUPT ENABLE TRACK 10
61:	KH = 0000:	INITIAL VALUE SIGN + DEC. 4
62:	KH = 0000:	INITIAL VALUE DEC. 3 + 2 + 1 + O
63:	KH = 0000:	END VALUE SIGN + DEC. 4
64:	KH = 0000:	END VALUE DEC. 3 + 2 + 1 + O
65:	KH = FFFF:	INTERRUPT ENABLE TRACK 11
66:	KH = 0000:	INITIAL VALUE SIGN + DEC. 4
67:	KH = 0000:	INITIAL VALUE DEC. 3 + 2 + 1 + O
68:	KH = 0000:	END VALUE SIGN + DEC. 4
69:	KH = 0000:	END VALUE DEC. 3 + 2 + 1 + O
70:	KH = FFFF:	INTERRUPT ENABLE TRACK 12
71:	KH = 0000:	INITIAL VALUE SIGN + DEC. 4
72:	KH = 0000:	INITIAL VALUE DEC. 3 + 2 + 1 + O
73:	KH = 0000:	END VALUE SIGN + DEC. 4
74:	KH = 0000:	END VALUE DEC. 3 + 2 + 1 + O
75:	KH = FFFF:	INTERRUPT ENABLE TRACK 13
76:	KH = 0000:	INITIAL VALUE SIGN + DEC. 4
77:	KH = 0000:	INITIAL VALUE DEC. 3 + 2 + 1 + O
78:	KH = 0000:	END VALUE SIGN + DEC. 4
79:	KH = 0000:	END VALUE DEC. 3 + 2 + 1 + O
80:	KH = FFFF:	INTERRUPT ENABLE TRACK 14
81:	KH = 0000:	INITIAL VALUE SIGN + DEC. 4
82:	KH = 0000:	INITIAL VALUE DEC. 3 + 2 + 1 + O
83:	KH = 0000:	END VALUE SIGN + DEC. 4
84:	KH = 0000:	END VALUE DEC. 3 + 2 + 1 + O
85:	KH = FFFF:	INTERRUPT ENABLE TRACK 15
86:	KH = 0000:	INITIAL VALUE SIGN + DEC. 4
87:	KH = 0000:	INITIAL VALUE DEC. 3 + 2 + 1 + O
88:	KH = 0000:	END VALUE SIGN + DEC. 4
89:	KH = 0000:	END VALUE DEC. 3 + 2 + 1 + O
90:	KH = FFFF:	INTERRUPT ENABLE TRACK 16
91:	KH = 0000:	INITIAL VALUE SIGN + DEC. 4
92:	KH = 0000:	INITIAL VALUE DEC. 3 + 2 + 1 + O
93:	KH = 0000:	END VALUE SIGN + DEC. 4
94:	KH = 0000:	END VALUE DEC. 3 + 2 + 1 + O
95:	KH = FFFF:	INTERRUPT ENABLE TRACK 17
96:	KH = 0000:	INITIAL VALUE SIGN + DEC. 4
97:	KH = 0000:	INITIAL VALUE DEC. 3 + 2 + 1 + O
98:	KH = 0000:	END VALUE SIGN + DEC. 4
99:	KH = 0000:	END VALUE DEC. 3 + 2 + 1 + O
100:	KH = FFFF:	INTERRUPT ENABLE TRACK 18
101:	KH = 0000:	INITIAL VALUE SIGN + DEC. 4
102:	KH = 0000:	INITIAL VALUE DEC. 3 + 2 + 1 + O
103:	KH = 0000:	END VALUE SIGN + DEC. 4
104:	KH = 0000:	END VALUE DEC. 3 + 2 + 1 + O
105:	KH = FFFF:	INTERRUPT ENABLE TRACK 19
106:	KH = 0000:	INITIAL VALUE SIGN + DEC. 4
107:	KH = 0000:	INITIAL VALUE DEC. 3 + 2 + 1 + O
108:	KH = 0000:	END VALUE SIGN + DEC. 4
109:	KH = 0000:	END VALUE DEC. 3 + 2 + 1 + O

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110:	KH = FFFF:	INTERRUPT ENABLE TRACK 20
111:	KH = 0000:	INITIAL VALUE SIGN + DEC. 4
112:	KH = 0000:	INITIAL VALUE DEC. 3 + 2 + 1 + 0
113:	KH = 0000:	END VALUE SIGN + DEC. 4
114:	KH = 0000:	END VALUE DEC. 3 + 2 + 1 **+ 0**
115:	KH = FFFF:	INTERRUPT ENABLE TRACK 21
116:	KH = 0000:	INITIAL VALUE SIGN + DEC. 4
117:	KH = 0000:	INITIAL VALUE DEC. 3 + 2 + 1 **+ 0**
118:	KH = 0000:	END VALUE SIGN + DEC. 4
119:	KH = 0000:	END VALUE DEC. 3 + 2 + 1 + 0
120:	KH = FFFF:	INTERRUPT ENABLE TRACK 22
121:	KH = 0000:	INITIAL VALUE SIGN + DEC. 4
122:	KH = 0000:	INITIAL VALUE DEC. 3 + 2 + 1 + 0
123:	KH = 0000:	END VALUE SIGN + DEC. 4
124:	KH = 0000:	END VALUE DEC. 3 + 2 + 1 **+ 0**
125:	KH = FFFF:	INTERRUPT ENABLE TRACK 23
126:	KH = 0000:	INITIAL VALUE SIGN + DEC. 4
127:	KH = 0000:	INITIAL VALUE DEC. 3 + 2 + 1 +0
128:	KH = 0000:	END VALUE SIGN + DEC. 4
129:	KH = 0000:	END VALUE DEC. 3 + 2 + 1 + 0
130:	KH = FFFF:	INTERRUPT ENABLE TRACK 24
131:	KH = 0000:	INITIAL VALUE SIGN + DEC. 4
132:	KH = 0000:	INITIAL VALUE DEC. 3 + 2 + 1 +0
133:	KH = 0000:	END VALUE SIGN + DEC. 4
134:	KH = 0000:	END VALUE DEC. 3 + 2 + 1 + 0
135:	KH = FFFF:	INTERRUPT ENABLE TRACK 25
136:	KH = 0000:	INITIAL VALUE SIGN + DEC. 4
137:	KH = 0000:	INITIAL VALUE DEC. 3 + 2 + 1 + 0
138:	KH = 0000:	END VALUE SIGN + DEC. 4
139:	KH = 0000:	END VALUE DEC. 3 + 2 + 1 **+ 0**
140:	KH = FFFF:	INTERRUPT ENABLE TRACK 26
141:	KH = 0000:	INITIAL VALUE SIGN + DEC. 4
142:	KH = 0000:	INITIAL VALUE DEC. 3 + 2 + 1 **+ 0**
143:	KH = 0000:	END VALUE SIGN + DEC. 4
144:	KH = 0000:	END VALUE DEC. 3 + 2 + 1 + 0
145:	KH = FFFF:	INTERRUPT ENABLE TRACK 27
146:	KH = 0000:	INITIAL VALUE SIGN + DEC. 4
147:	KH = 0000:	INITIAL VALUE DEC. 3 + 2 + 1 +0
148:	KH = 0000:	END VALUE SIGN + DEC. 4
149:	KH = 0000:	END VALUE DEC. 3 + 2 + 1 **+ 0**
150:	KH = FFFF:	INTERRUPT ENABLE TRACK 28
151:	KH = 0000:	INITIAL VALUE SIGN + DEC. 4
152:	KH = 0000:	INITIAL VALUE DEC. 3 + 2 + 1 + 0
153:	KH = 0000:	END VALUE SIGN + DEC. 4
154:	KH = 0000:	END VALUE DEC. 3 + 2 + 1 + 0
155:	KH = FFFF:	INTERRUPT ENABLE TRACK 29
156:	KH = 0000:	INITIAL VALUE SIGN + DEC. 4
157:	KH = 0000:	INITIAL VALUE DEC. 3 + 2 + 1 **+ 0**
158:	KH = 0000:	END VALUE SIGN + DEC. 4
159:	KH = 0000:	END VALUE DEC. 3 + 2 + 1 **+ 0**
160:	KH = FFFF:	INTERRUPT ENABLE TRACK 30
161:	KH = 0000:	INITIAL VALUE SIGN + DEC. 4
162:	KH = 0000:	INITIAL VALUE DEC. 3 + 2 + 1 +0
163:	KH = 0000:	END VALUE SIGN + DEC. 4
164:	KH = 0000:	END VALUE DEC. 3 + 2 + 1 + 0
165:	KH = FFFF:	INTERRUPT ENABLE TRACK 31
166:	KH = 0000:	INITIAL VALUE SIGN + DEC. 4
167:	KH = 0000:	INITIAL VALUE DEC. 3 + 2 + 1 **+ 0**
168:	KH = 0000:	END VALUE SIGN + DEC. 4
169:	KH = 0000:	END VALUE DEC. 3 + 2 + 1 **+ 0**

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170:	KH = OOFF:	ZERO SHIFT
171:	KH = FOOO:	CHANNEL 1 SIGN + DEC. 4
172:	KH = 0250:	DEC. 3 + 2 + 1 + 0
173:	KH = 0000:	CHANNEL 2 SIGN + DEC. 4
174:	KH = 0000:	DEC. 3 + 2 + 1 + 0
175:	KH = FFFF:	CLOCK PULSE GROUP ENABLE
176:	KH = 0000:	CLOCK PULSE GROUP LENGTH
177:	KH = FFFF:	HYSTERESIS ENABLE
178:	KH = 0000:	HYSTERESISVALUE
179:	KH = FFFF:	ROT.AXIS FUNCTION ENABLE
180:	KH = FFFF:	PARALLELSWITCHING ENABLE
181:	KH = FFFF:	VERIFY–READ NUMBER ENABLE
182:	KY= 0.13	CHANNEL NO:/NO. OF VERIFY–READ
183:	KH = FFFF:	ENABLE/AVERAGE VALUE
184:	KY= 0.7	CHANNELNO:/NO. OF AVERAGE VALUES
185:	KH= FFFF:	DIRECTION–DEPENDENT INTERR. ENABLE
186:	KH = 0001:	DIRECTION SPEC. FOR INTERRUPT
187:	KH = 0000:	Free

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9.6 Direct Programming of the IP 241 (without the Standard Function Block)

The intelligent 1/0 module “digital position decoder” is addressed by a central processor like an 1/0 module.

Processors for SIMATIC S5 technology are programmed in STEP 5 programming language. Via byte–based (8 bits) load and transfer commands, this language allows parameterization of the module or processing of available identifiers in the working range of the central processor.

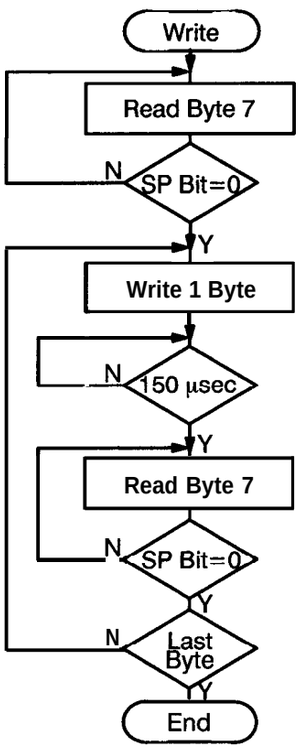
The module does not have its own buffer.
This means that after a voltage failure, all parameters must be transfer–red to the module again.

9.6.1 Parameterization

Approximately 100 µsec after turning on or returning control voltage, the SP bit can be scanned. It has status “1” until the module is ready to accept write commands (memory initialization). Now the module can be parameterized (i.e., initial and end setpoints), and if necessary, interrupt identifiers must be assigned to the 32 tracks of the two channels.

With incremental encoder modules, the internal counter must be defined as shown in example C on next page. The other encoder modules accept the absolute actual value of the connected encoder directly.

Normally, parameters are assigned in a new start-up routine or for STEP 5 programs, depending on the processor type, in accordance with conditional control statements.



The SP bit must be scanned for “0” before every write command. If the SP bit = “1”, IP 241 cannot be accessed.

NV (zero shift) value must only be written once per channel.

When the S5 is used, the module must be erased prior to parameterization (see section 9.6.4). When working with ETA 80/85/86, etc., after each write or read command an address other than that of the module must be read.

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9.6.1.1 Byte Structure

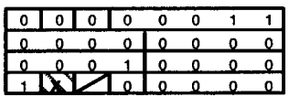
Byte O specified below corresponds to the hardware–based setting of the module address.

NV = Zero shift
IR = Interrupt identifier bit
Anf = Initial setpoint
End = End setpoint
Vz = Sign
B = Erase set track
X = ALWAYS 0
SS = Software–based synchronizing

Bit	7 6 5 4	3	2 1	0
Byte 0	NV, IR	Anf= 0 End= 1	Track No. 0–31	
1	Setpoint 10^1		Setpoint 10^0	
2	Setpoint 10^3		Setpoint 10^2	
3	VZ	X, SS, B	Setpoint 10^4	

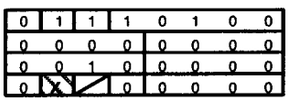
Examples:

A) Specifiy bit pattern for track 3 with
– Initial setpoint = –1000
– No interrupt assignment



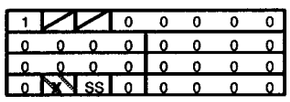
Note:
NV must be O
B must be O
X ALWAYS O

B) Specify bit pattern for track 20 with
– End setpoint = +2000
– Interrupt when this value is reached



Note:
NV must be O
B must be O
X ALWAYS O

C) Zero shift
(required for defined setting of the internal timer when incremental encoders are used) for a channel (IR possible when synchronizing)



Channel selection with any track number:

– for channel 1 track number 0...15
– for channel 2 track number 16...31

Example: – Channel 1 (track number:0)
– Zero point = O

Note: – Start/End, B not relevant
X ALWAYS O

After completed synchronization and new zero shift value specification, the synchroniza–tion bit and the synchronization logic are reset.

When “SS” bit is set, the counter is synchronized following writing of bytes 0.1, and 2 and subsequent writing of byte 3.

For updating of the result bit, a time period of 1 msec per supplied initial or end value is required (see section 8.3).

In this case no “SP” bit is set!

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9.6.2 Modification of Parameterized Initial and End Values

Meaning of the B bit: At the first parameterization of an initial or an end setpoint the B bit is irrelevant.

If a track needs to be modified, there are the following possibilities:

- **The set B bit erases the initial or end value in the selected track. A possible assigned setpoint is irrelevant.**

  This method is for modifying single tracks. The software-based erasing in section 9.6.4 is recommended for erasing all tracks.

- **B bit= "O" replaces the old setpoint with a new setpoint (in the selected track).**

Notes for parameterization
During the transfer of new setpoints to the module, the actual value acquisition is delayed and the indicated tolerances are increased.

	KH	KM
Rotary axis, only channel 1	F4	11110100
Rotary axis, only channel 2	F5	11110101
Rotary axis, channels 1 and 2	E7	11100111

Example: rotary axis on channel 2 only and IP module address at 128

OB 20:

```
JU FB xx                128
   SP-bit-scan        + 4
   LKH F5             ---
   TPY 132 <--------  132

   BE
```

Example: parallel switching mode and module address at 144

OB 21 :

```
JU FB xx                144
   SP-bit-scan        + 4
   LKH F6             ---
   TPY 148 <--------  148

   BE
```


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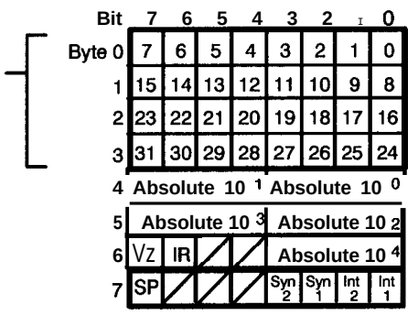
9.6.3 Reading the Result Tracks

In order to evaluate the current track bit assignment, bytes O to 3 and byte 7 can be read at all times.

Result track bits are set when an internal counter value is within a specified initial and end setpoint. In case of incremental encoders, synchronization bits are set when a synchronization pulse is active (via an external preliminary contact in connection with a zero mark and a count pulse) or synchronized by the software.

Track identifiers
(result track bits)

VZ = Sign
Syn. = Identifier, indicating whether synchronizing took place
Int. = Identifier of the channel where the interrupt was triggered
SP = Enable bit for write and read absolute value
IR = Track parameterized with IR identifier bit



An SP bit scan is not necessary to read the result tracks.

interrupt bits indicate which channel has triggered an interrupt (group signal) when an initial or end setpoint or a zero shift value, parameterized with an interrupt identifier, was exceeded.

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9.6.3.1 Interrupt Processing

Starting with firmware status R08, the interrupt behavior of the module can be modified by writing the block address +4 as follows:

KH = EI – Interrupt identifier bits deleted after reading byte 7
KH = E2 – Interrupt identifier bits not deleted after reading byte 7
– Bit 4 is set by byte 7 during the read access

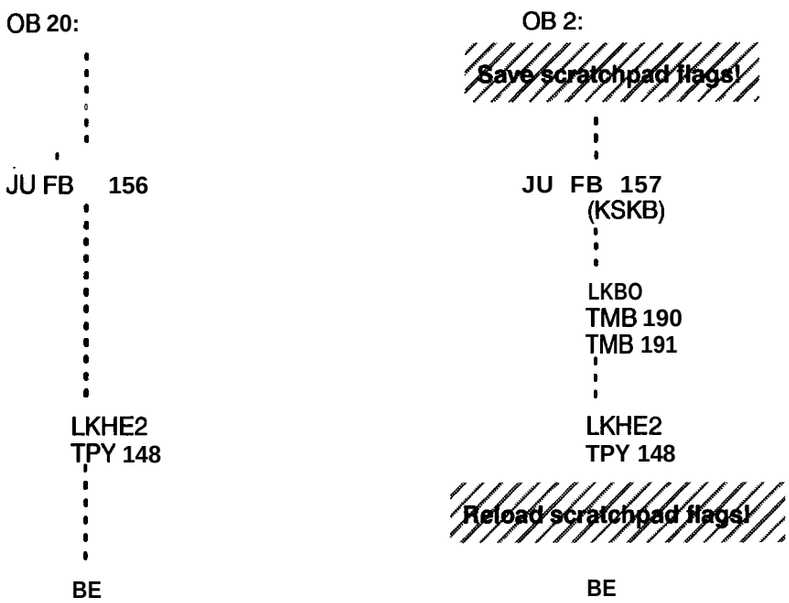
When a second write access to the module address +4 is performed with KH = E2, bit 4 becomes "0" again. This can also be a accomplished by resetting the module.

Interrupt line IR is always reset however.

Point in time of the write access for:

KH = EI – Interrupt program (otherwise no further interrupt possible)
KH = E2 – Startup OB
For use be standard function blocks after calling FB 156
(Call performs reset of the module.)

Example for module address 144:



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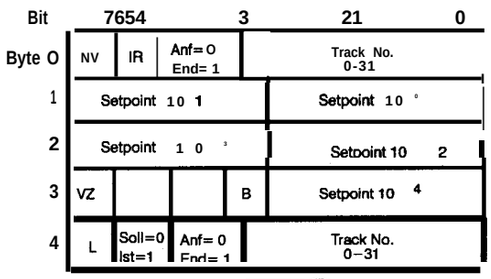
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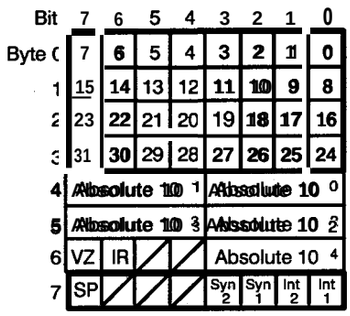
9.6.4 Reading the Absolute Value (Actual Value)

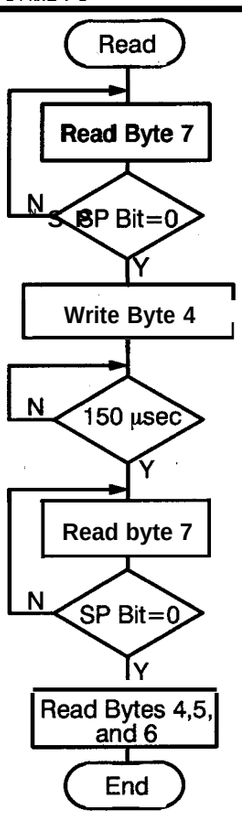
To read and evaluate actual absolute values, parameterized tracks or initial and end setpoints, a prompt for updating bytes 4,5, and 6 of the output register must be given.

Byte 4 must provide an L read prompt.

L = Read
Soll = Setpoint display
Ist = Actual value display
Anf = Initial setpoint
End = End setpoint
VZ = Sign







When byte 4 is switched to the data bus, the following bit patterns are ossible for prompting the absolute values in the following read cycle: Read the current actual value of a channel via any track number.

For channel 1 track number O to 15 (any)
For channel 2 track number 16 to 31 (any)
Example: Channel 2 (track number = 16)

Byte 4	1	1	0	1	0	0	0	0

Note: Initial bit must be “O”.

Software-based deletion:

If the read bit = “1”, the actual value bit = “1” and the end bit = “1”, all parameterized data is deleted. Even when the track identifier changes, no interrupt is triggered.

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Example: module address set at 128

SP bit scan

```
L KM     11010000
T PY     132 (MOD address +4)
– Waiting time 150 µsec
– SP bit scan
L PY     132 (MOD address + 4)
T . .    FY
L PY 133 (MOD address + 5)
T FY
L PY 134 (MOD address + 6)
T FY . . .
```

Reading the firmware state:

If the module has been erased (i.e., the module is not parameterized or has not been erased by software), the firmware state can be recognized by reading bytes 4,5, and 6 without read prompting

whereby: **Byte 4 = Year**
Byte 5 = Month
Byte 6 = Day

Reading the initial or end setpoint of a track:

Example: Track number = 20
Read end value (as a check)

Byte 4

1	0	1	1	0	1	0	0
L	S	E	. . . 20 . . .			S	E

1 = Read
O = Set point indicator
1 = End value

After definition of (in a write cycle via byte 4) what is to be read from bytes 4,5, and 6 in a read cycle, the read operation can start after a scan of the SP bit = "O".

Sequence:
– Read SP bit
– Write, specify byte 4
– Read, SP bit
If "O", read bytes 4,5, and 6

for every initial or end track setpoint or for every actual channel value to be read.

IR = "1" for parameterization with interrupt.

If a track is not present (parameterized) or if the synchronization bits 1 and 2 for incremental encoders are not set, then bytes 4, 5, and 6 = FFHex. (11111111).

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9.6.5 Special Functions

	Entry in Byte No: (Module Address +n)		
	n = 0 Hex	n = 1 BCD	n = 4 Hex
Clock pulse group			
Channel number	1 or 2		
TB number		O to 24	
Code			F0
Hysteresis			
Channel number	1 or 2		
Hysteresis value		o to 9	
Code			F1
Rotary axis			
Channel 1			F4
Channel 2			F5
Both channels			E7
Parallel switching			
Code			F6
NV (zero shift)			
Channel number	1 or 2		
NV values		See Sec. 9.2.5	
Code			F7 ①
Read NV value			
Channel 1			E8
Channel 2			E9
Verify-read			
Channel number	1 or 2		
Number of verify-reads		o to 15	
Code			F2
Calculate average value (analog submodule)			
Channel number	1 or 2		
Number		o to 15	
Code			F3

① A new NV value can be transferred by writing F7 (NV value) to address +4, without the SYN LED going on (i.e., operation is still possible). The new NV value is not accepted until hardware synchronization is performed.

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	Entry in Byte No: (Module Address +n)		
	n = 0 Hex	n = 1 BCD	n = 4 HEX
Inhibit interrupt depending on direction			
Channel 1, backwards inhbited	xl		
Channel 1, forward inhibited	x2		
Channel 1, both directions inhibited	x3		
Channel 2, backwards inhbited	l x		
Channel 2, forward inhibited	2x		
Channel 2, both directions inhibited	3x		
Code			F8
Inhibit interrupts			
Code			**E3**
Inhibit interrupts for supply			
Code			**E4**

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10 Glossary

Definitions and explanations for the IP 241 Equipment Manual

Actual value	**The actual position information from the encoder which arrives at the IP 241**
Average value calculation	**Special function for calculating an average value from up to 15 consecutive actual values (for analog submodule)**
Basic connector	**Connection to the device bus of the PLC**
BCD coding	**Four bits of a measured value indicating a decimal exponent (units of thousand, hundred, ten, and one)**
BERO	**Proximity switch**
Buffering	**Battery back-up for memory; not available with the IP 241; the battery back- up of the programmable controller is not used for the IP 241.**
Byte O	**Relative byte O (i.e., the hardware-based setting of the module address)**
Cam	**The range between a selectable start and end value, where a reaction is desired**
Clock pulse group	**Group of single pulses with which the actual value is read in for synchronous-serial encoders**
Component set	**Elements and connectors required for the per channel signal conditioning**
CPKL	**Central processor clear (if CPKL = 1, a reset is made)**
CPU	**Central module**
Data block	**Data list for the function block**
DB	**Data block**
Encoder matching module	**Plug-in type of module that allows the conditioning of the signals for each channel of the connected position encoder and allows the conditioning of the encoder supply voltages**
Firmware	**Program stored on the module**
High byte	**Most significant part of a 16-bit word**
Hysteresis	**Adjustable "unfocus" for "jumpy" actual values (only for analog submodules)**

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Incremental encoder	An encoder which emits individual pulses when its axis rotates
Interrupt	The possibility of obtaining a quick reaction from the programmable controller when an alarm is triggered
1/0 area	Address area for peripheral modules in the programmable controller
L+	24 V connection, positive terminal
L–	24 V connection, reference point
Linear axis operation	Traversing between fixed limits
Low byte	Least significant part of a 16–bit word
Master/Slave operation	The possibility of detecting the triggering module, when several interrupt–capable modules are used on one interrupt line
NV value	Zero shift value
Operation in parallel mode	Operating mode in which an encoder can handle a maximum of 32 reactions in pseudo single–channel operation
Parameterization	Supplying the used tracks with start and end values and with interrupt identifiers and for the selection of operating modes
P–area	Address area for peripheral modules in the programmable controller
Peripheral byte O	Address byte O in the 1/0 area which is used for interrupt processing in some programmable controllers
PESP	Address group signal for addressing peripheral modules (peripheral memory)
PLC	Programmable logic controller
Position encoders	Encoders providing position information in form of pulses (incremental) or coding (absolute)
Preliminary contact	A switch installed on the system or a reference point provided by the S5
PYO	See peripheral byte O
Q–area	Extended address area for peripheral modules in the programmable controller
Relative byte	See byte O
Rotary axis operation	Cyclic traversing as used with rotary plates or continuous conveyors
S5	SIMATIC S5 Programmable Controller

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Scratchpad flags	Flags which are also used by the standard function block (FY 200 to FY 255); the scratchpad flag area must be saved during interruptions that are caused by timed interrupts or interrupts.
Setpoints	Desired start and end values of a cam
Standard function block	Program package in the SIMATIC S5 programmable controller
ST FB	Standard function block
Synchronization	With incremental encoders this means the timing coincidence of an encoder pulse, a zero mark, and an initiating pulse
Track	Any reaction track where a cam can be set. The IP 241 has a maximum of 16 tracks per channel (32 with single-channel operation)
TB	See clock pulse group
Track identifier bit	The result of a comparison between the actual value and the setpoint of a track is made available here.
Traversing direction	The direction from which a cam of the system is reached
Verify-read	Special function to eliminate brief disturbances (e.g., on the encoder line)
Zero shift	By specifying a value, the reference point (mostly O) can be changed to this value for incremental encoders.

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