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2 Processing master programs / MP Edit and MP Compile

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2.1 Generating and changing the master program / MP Edit

The master program (MP) defines the system hardware configuration: The subracks used, subrack equipping (inserted boards) and the bus structure. The distribution of the complete tasks to the processor boards as well as data transfer between the processor boards is also defined by the master program. Execution is realized in two steps, editing and compilation.

2.1.1 Calling-up

The editor is called-up from the basic dialog (**MP Edit / Configure**). Before this, the master program must be selected from the available master programs of the selected project.

2.1.2 Editing the master program

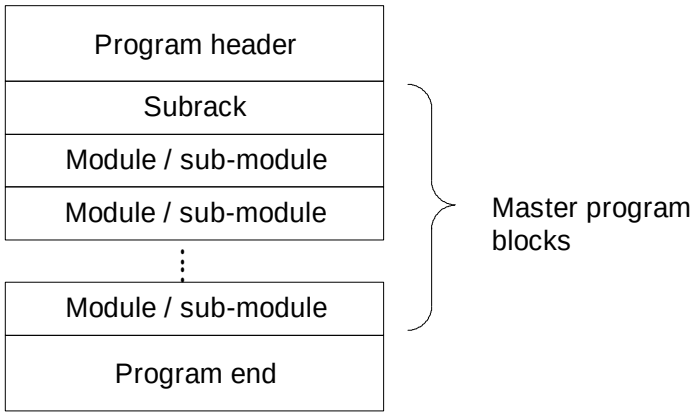
An editor with various functions is available to edit the master program. The editor and functions are described in detail in Section 1.

Here is an overview of the functions:

INSLIN	Insert line	CONTLN	Continuation line
ERAELE	Delete element	SETRNG	Mark range
ERARNG	Delete range	RENUMB	Re-number lines
MOVRNG	Shift range	NEXT ?	Next question mark
CPYRNG	Copy range	APPEND	Attach
SUBTXT	Replace text	EXIT	Save and terminate
SUBMSK	Replace mask	QUIT	End without saving
CHGMSK	Change mask	FIND	Search

2.1.3 Master program structure

A master program is structured as follows:



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2.1.4 Program header / footer

After a new MP is called-up, the following header mask is displayed:

```
 1 MP-HANDMP
 &    V4.2.1   MP-DIA UNC 19.05.95 16:44
 &      IBSLIB 940815V400     A:
 &    B:                      C:
 2    CT1 4S = '                                ' "Inhalt/Content"
 3    CT2 4S = '                                '
 4    CT3 4S = '                                '
 5    HLD 3S = '                           '"Anlagenkennz./Higher lev. desig"
 6    DLP 3S = '                           '"Zeichn.Nr./Draw. No List prefix"
 7    DLS 1S = '        '                   "    .        .       .   suffix"
 8    DGP 3S = '                           '"    .        .   Graphic prefix"
 9    DGS 1S = '        '                   "    .        .       .   suffix"
10    DPP 3S = '                           '"  .  Besteller/Purchaser prefix"
11    DPS 1S = '        '                   "  .      .         .     suffix"
12    LCD 3S = '                           '"Ortskennz./Location designation"
13    OI1 2S = '                 '          "Auftragskennz./Order identific."
14    OI2 2S = '                 '
15    CN1 2S = 'Siemens AG       '          "Firmenname / Company name"
16    CN2 2S = '                 '
17    UP1 4S = '                                      '"Betr.,Anlage/User,plant"
18    UP2 4S = '                                      '
19    UP3 4S = '                                      '
20    CDA DA = ?                           "Projektdatum / Date of project"
21    DES 2S = '                 '          "Bearbeiter   / Designer"
22    CHK 2S = '                 '          "Pruefer      / Checked by"
23    ORD 4S = '                                      '"Urspr/Original document"
24    MD3 4S = '      /            /        /   '"Modification"
25    MD2 4S = '      /            /        /   '
26    MD1 4S = '      /            /        /   '
27    SYS 1N =  @SIMD                        "System-FP"
28    DIM DL = [kVA],[MVA],[%],[kW],[MW]
 &             ([ms],[s],[min],[A],[V],[1/min],[m/min],[m/s],[GRAD],[Hz])
29 ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
```


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The cursor is positioned at the start of the entered MP name (HAND MP = user name) in line 1. This name can be changed and the MP can be stored under new names once processing has been exited.

The STRUC version (V4.2.1) is located after the 1st line, as well as a code, which specifies the components this file last processed (MP-DIA), the processing status (UNC = unchecked master program) and the last changed data. For example:

```
&   V4.2.1   MP-DIA UNC 19.05.95 16:44
```

Information for up to a max. of 4 usable mask libraries follow in the next two lines. This information comprises the library name, status and version.

These three lines, which follow the header line, cannot be changed. The entries are made from the particular components.

The header mask must be completed as follows:

Lines 2 to 4 are available for user comments. The text entered here, in inverted commas (' '), is stored in the EPROM and is kept during reverse compilation. This is true for all other texts in inverted commas.

The entry in lines 5 to 26 includes all important system data and should be realized corresponding to the specified comments.

Line 27 presently includes as standard the system function package, pre-assigned with @SIMD.

Line 28 contains the dimension list. Standard dimension information is already provided here. Additional dimension information which the user requires, must be additionally entered. However, the first 5 dimensions, entered as standard, may not be overwritten. The 10 dimensions, entered in the continuation line, cannot be overwritten.

Dimension information must be entered in square brackets ([ ]), separated by a comma. A dimension can be up to a max. of 8 characters. Upper case and lower case letters are handled the same internally, which means that, for example, [MIN] = [min]. Dimension information, which is used for signal attributes LOG1 and LOG0 (refer to Section 3.1.10), must be entered in pairs one after another in the sequence LOG1, LOG0.

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Here is an example of a completed header mask:

```
 1 MP-HANDMP
 &   V4.2.1   MP-COP CHK 19.05.95 16:44
 &     IBSLIB 940815V400     A:
 &   B:                      C:
 2   CT1 4S = 'STRUC L 4.0 P32/P16             ' "Inhalt/Content"
 3   CT2 4S = 'EXAMPLE Sawtooth/Sine function  '
 4   CT3 4S = '                                '
 5   HLD 3S = '=DB50.W00              '  "Anlagenkennz./Higher lev. desig"
 6   DLP 3S = '(4) E8831-G4569-       '  "Zeichn.Nr./Draw. No List prefix"
 7   DLS 1S = 'K001    '                "    .        .       .   suffix"
 8   DGP 3S = '(3) E8831-G4569-       '  "    .        .   Graphic prefix"
 9   DGS 1S = 'K000    '                "    .        .       .   suffix"
10   DPP 3S = 'ASI 1 D V 122 T3       '  "  .  Besteller/Purchaser prefix"
11   DPS 1S = '00      '                "  .      .         .     suffix"
12   LCD 3S = '+H7                    '   "Ortskennz./Location designation"
13   OI1 2S = 'E121-840403     '        "Auftragskennz./Order identific."
14   OI2 2S = 'Erl             '
15   CN1 2S = 'Siemens AG      '        "Firmenname / Company name"
16   CN2 2S = '                '
17   UP1 4S = 'Siemens AG,Erl., ASI 1 D V122T3 ' "Betr.,Anlage/User,plant"
18   UP2 4S = 'SIMADYN-D V4.0                  '
19   UP3 4S = 'STRUC G EXAMPLE                 '
20   DAT DA = '17.10.94                   "Projektdatum / Date of Project"
21   DES 2S = 'ASI 1 D V122 T2 '        "Bearbeiter   / Designer"
22   CHK 2S = 'ASI 1 D V122 T3 '        "Pruefer      / Checked by"
23   ORD 4S = 'MP-HANDMP 17. december 1993     '"Urspr./Original document"
24   MD3 4S = '      /            /        /   ' "Modification"
25   MD2 4S = '      /            /        /   '
26   MD1 4S = '      /            /        /   '
27   SYS 1N = @SIMD                       "System-FP"
28   DIM DL = [kVA],[MVA],[%],[kW],[MW]
 &            ([ms],[s],[min],[A],[V],[1/min],[m/min],[m/s],[Grad],[Hz])
29 ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
```

"END" must be entered at the end of the master program. The compiler ignores all other data entries after "END". For example:

```
    235     END
```


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2.1.5 Master program blocks

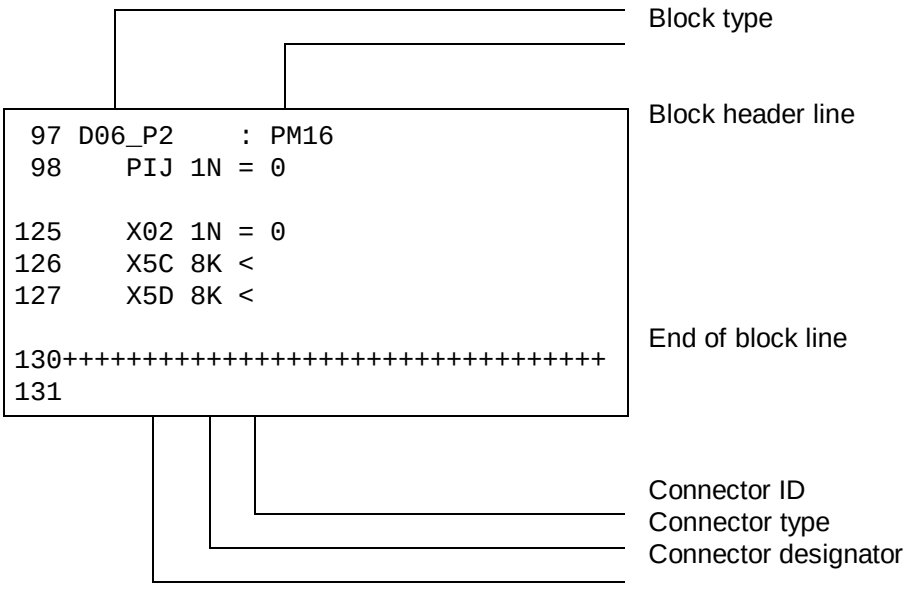
Master program blocks can be called-up in interactive dialog **MP Edit / Configure** (Section 1.1). An accurate block description can be taken from the master program component catalog.

The following blocks are available:

- subrack
- module
- submodule

A differentiation is made between processors-, peripheral boards, buffer memories and special-peripheral boards. Submodules are components, which are located on a board (block).

Every master program must describe a subrack and all of the associated boards and submodules. The structure of the board blocks can be taken from the following example:



The connector designators are listed in the board description and can consist of a maximum of 3 characters.

The connector type defines the permissible information to be entered to the right.

There are 3 different ways of identifying the connectors:

Connector ID	Connector type
<	Hardware addresses for inputs
>	Hardware addresses for outputs
=	Configured assignments

Input/output function blocks can access hardware addresses.

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The configuring engineer can freely assign block names, with the exception of the restrictions imposed on the processor boards. Further, it is recommended that the names are selected according to the following designation schematic for system components:

Subrack:	Axxx	xxx	≥	3 digits, e.g. 100
PN names:	Dxx_Pn	xx	=	slot No.
		n	=	processor No. 1 - 8
Submodule names:	Dxxy	xx	=	slot No.
		y	=	connector No.
Board names:	Dxx	xx	=	slot No.
Communication board names:	Dxxzzk	xx	=	slot No.
		zz	=	any character (upper case letters, digits)
		k	=	board ID A = MMxy (buffer memory) B = CS11 or CS21 (parallel rack coupling) C = CSH11/CS7 with SS4 or SS5 (bus coupling)

The subracks are numbered in a particular project (e.g. 100, 101, etc.).

The slot number designates the slot where the associated board is configured ('01' ... '24'). The connector number represents the last digit of the connector, at which the associated submodule is inserted ('0' for connector X50 - EPROM, '1' for connector X01 and '2' for connector X02 - serial interfaces).

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¨ **Subracks**

Example:

```
30 A100      : SR8                   "Subrack 24 slots,L+C-bus"
31    L01 6S = 'PM3     .     MM21    CS7/SS4 .       PM16    '"Beschrif."
32    L07 6S = '.       .      .       .       .       .      '"streifen/"
33    L13 6S = '.       .      .       .       .       .      '"Lettering"
34    L19 6S = '.       .      .       .       .       .      '"    strip"
35    S01 8N = D01_P1,D01010        "PM3 with memory submodule MS5
)"
36    S02 8N = 0
37    S03 8N = D0300A               "Interface memory module MM21 (L-bus )
"
38    S04 8N = D0400C,D04010,0,0      "CS7 with SS4"
39    S05 8N = 0
40    S06 8N = D06_P2,D06010,D06020,D06030 "PM16 with memory submodule MS41"
41    S07 8N = 0
42    S08 8N = 0
43    S09 8N = 0
44    S10 8N = 0
45    S11 8N = 0
46    S12 8N = 0
47    S13 8N = 0
48    S14 8N = 0
49    S15 8N = 0
50    S16 8N = 0
51    S17 8N = 0
52    S18 8N = 0
53    S19 8N = 0
54    S20 8N = 0
55    S21 8N = 0
56    S22 8N = 0
57    S23 8N = 0
58    S24 8N = 0
59 ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
60
```

Entries for the labeling field of the subrack can be made at connectors L01 ... L19. S01 ... S24 designate the particular rack slot of the subrack (from left to right). The user names of the inserted boards, and all associated submodules, separated by a comma, must be entered here. An 0 can be entered if a sub-module is not present. A '0' must be entered at slots where there is not board.

For double-width boards, such as processor boards, a 0 should be entered for the second occupied slot.

If the communications bus (C bus) is to be used, processor boards with C bus connection (e.g. PM16) and a C bus buffer memory board must be used. In this case, a C-bus processor board must be inserted at slot 1. The C-bus buffer memory module must be inserted before additional processor boards, and preferably, directly next to the first processor board.

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If there is an additional processor board, then the following peripheral boards are assigned to the second processor board. If a peripheral board is accessed during configuring, which is not assigned to the processor board, a warning is entered in the appropriate function package. However, if the peripheral board cannot be accessed on a common L bus, then an error message is issued. This warning is issued, as the additional access to other processor peripherals is not included in the PN-MAP listing of the processor program. It can be ignored, if the user actually wishes to access peripherals which are outside the jurisdiction of the particular processor.

If there are several processor boards connected to a local bus, which exchange data between one another, an L bus buffer memory is required on the L bus. For processor boards, without integrated L bus buffer memory, a separate L bus buffer memory board should be used in front of the second processor board. The L-bus buffer memory is preferably located directly next to the first processor board.

Processor boards which exchange data must be connected through a bus. This connection is established, if board connectors are available at all slots between the processor boards. For double-width boards, such as processor boards, this is not available at the righthand slot. For this reason, there, and also at free slots, daisy chain jumpers must be inserted to establish a continuous bus. It should be observed that most peripheral boards do not have a C bus connector, and therefore, if data transfer is required between C-bus processors, then the appropriate slots, where such peripheral boards are inserted, must also have daisy chain jumpers.

The C bus runs, if available, through the complete rack (above) and when supplied, is not provided with a bus terminating connector. This must be inserted by the user if there is no C bus buffer memory. The buffer memory includes a terminating connector. The same is true for the L bus as for the C bus.

The layout diagram belonging to the graphic documentation shows where daisy chain jumpers and bus terminating connectors must be provided.

¨ **Processor boards**

All processor boards have similar structures. Processor boards have a special name convention. The board name must be 6 characters long, whereby the last 3 characters are the underline, the letter "P" and the logical processor number n = 1 ... 8. The logical processor number appears, in operation, on the processor board 7-segment display.

Examples for processor board names:

D01_P1	Processor 1 at slot 1
D04_P2	Processor 2 at slot 4
D07_P3	Processor 3 at slot 7

The required inputs will now be explained using processor board PM16 as an example:

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Example:

```
 97 D06_P2    : PM16                "processor module 1 standard, L+C-bus"
 98    PIJ 1N = 0                  "alarm processing FP"
 99    SFJ 1N = 0                  "system error FP"
100    PRX 1N = 0                  "special communications FP receive"
101    PJ1 1N = SAEG16             "sawtooth signal generator  "
102    PJ2 1N = 0
103    PJ3 1N = 0
104    PJ4 1N = 0
105    PJ5 1N = 0
106    PJ6 1N = 0
107    PJ7 1N = 0
108    PJ8 1N = 0
109    PTX 1N = @SDP21             "special communication FP transmit"
110    ILS IK = 0                  "L-Bus-Interrupt transmit"
111    ICS IK = 0                  "C-Bus-Interrupt transmit"
112    T0  TG = 1[MS]              "basic sampling time"
113    T1  TS = 1                  "1.s.t.*T0,produced LB- and CB-conn."
114    T2  TS = 8                  "2.s.t.          ''               "
115    T3  TS = 32                 "3.s.t.          ''               "
116    T4  TS = 64                 "4.s.t.          ''               "
117    T5  TS = 256                "5.s.t.          ''               "
118    TY  TX = T4                 "sampling time of system FP"
119    SSM 2C = 0                  "Length SAVE-area, (n*1+2) kbyte"
120    ISE 1C = N                  "Ignore syst. except.(RDYINT)(Y/N)?"
121    CCT 8R = 0                  "transmitter communication names Tx"
122    CCR 8R = 0                  "receiver communication names.Tx"
123    COP 8R = 0                  "service communication names.Tx"
124    X01 1N = 0                  "1st serial interface"
125    X02 1N = 0                  "2nd serial interface"
126    X5C 8K < *D06X5C            "binary inp. 1, intrpt ctr."
127    X5D 8K < *D06X5D            "binary inp. 2, intrpt ctr."
128    X5A 8K > *D06X5A            "binary outputs 1"
129    X5B 8K > *D06X5B            "binary outputs 2"
130 ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
131
```


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Line number and connector designator	Explanation
98, PIJ (IJ1 ...IJ2)	The name of the interrupt-processing function package is entered here (P16). P32: max.2 × 8
99, SFJ	The user can define an FP here, which executes a system error handling and is processed per interrupt. This is presently still not implemented.
100, PRX	The user must specify an FP here if he wishes to configure central receive blocks (must start with @).
101-108, PJ1 ... PJ8	All FPs (max. 8 for P16 and 8 × 8 for P32), which are not interrupt-controlled, but are processed in sampling times (permanent processing FP), must be listed here.
109, PTX	The user must specify an FP here if he wishes to configure central send blocks (must start with @).
110-111, ILS,ICS	Processor board synchronization information is possible here. It is possible to specify whether an interrupt event, and which (C1, C2, S1..S8, E1, E2), is to be switched to the interrupt line of the L or C bus.
112-116 I1 ... I5 (I8)	Assignement of the alarm tasks P32: max. 8, P16: max. 5 to the alarm events with additional sampling time defaults for time parameters.
117, T0	The processor board base sampling time must be specified here in ms. The base sampling time should be as high as possible (1 ms), to prevent excessive processor loading. Further, it is possible to provide information regarding the processor board synchronization here (refer to Section 2.1.6).
118-122 T1 ... T5	Further, it must be defined 5 sampling times in rising succession. Additionally a factor must be entered, which, multiplicated with the basic sampling time, result in the corresponding sampling time. In this examplr means: sampling time T4 = 64 ∗ 1.0 ms = 64.0 ms. Only square steps are allowed for this factor (max. 2 15 = 32768). Besides all in a sampling time created (Almost-) L bus and (almost) C bus connections (LBC and CBC or FLBC and FCBC) must, divided with commas, be enumerated (Example see sector 2.1.6) Often the place of one line is not sufficient to enumerate all (F)LB and (F)CCB connections, so that continuation lines (function `CONTLN´) must be definded.
123, TY	The sampling time, in which FP system shall be proccessed (time between 30 and 100 ms), must be defined.A maximum of 64 communication names for operator panel control blocks, with sampling time information, can be specified in this line.
124, SSM	Here, the length of the SAVE area can be configured. The value, which is denounced here, will additioned to the permanent existing 2ks.
125 ISE	Here, it can be defined as to whether the failure signal (RDYINT), should be ignored (Y) or not (N).
126-127 CCT, CCR	Here maximal 64 transmit or receive communication names with sampling time instruction can be configured.
128 COP	In this line can maximal 64 communication names for dialogu blocks for sampling time remark be announced.
129-130, X01, X02	The names of the serial interfaces can be entered in these two lines. These names can be freely selected.
126-129, X5A ... X5D	Symbolic hardware addresses for the partial connectors can be entered here. (also refer to the peripheral board).

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¨ **Peripheral boards**

```
201 D07       : EB11               "Binary I/O module 1, L-Bus"
202    ISE 1C = N                  "Fail mess., ignore(RDYINT)(Y/N) ?"
203    X5C 8K <*BINA_1             "Binary inputs 1"
204    X5D 8K <*BINA_2             "Binary inputs 2"
205    X6C 8K <                    "Binary inputs 3"
206    X6D 8K <                    "Binary inputs 4"
207    X5A 8K >                    "Binary inputs 1"
208    X5B 8K >                    "Binary inputs 2"
209    X6A 8K >                    "Binary inputs 3"
210    X6B 8K >                    "Binary inputs 4"
211 ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
212
```

The input- and output hardware address symbolic designations can be defined here, which can be used in the function packages (also refer to Section 6.1.8). If no information is entered, then the hardware address in the function package can be addressed under the board names, together with the partial connector designation, i.e., e.g. D07.X5C corresponds to *BINA_1. The symbolic designation allows function diagrams to be standardized.

¨ **Buffer memory boards**

```
86 ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
87 D0300A    : MM21                   "Interface module, L+C bus"
88    CIP 1C = N                       "set-up CIP (Y/N)"
89 ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
```

For buffer memory boards (also known as interface modules), it is only necessary to specify whether the buffer memory should be initialized with its communications structure (Y).
It should be noted, that precisely one buffer memory module is required for the C- and L bus.

¨ **Submodules**

```
130 ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
131 D060      : MS41                   "Memory submodule MS4/44, 512k, 0 WS"
132 ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
```

All submodules, which are listed in the subrack with their user names, must be specified here. When initializing the board at switch-on, not all submodules are checked to ensure that they are available.

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2.1.6 Connector types, master program

Depending on the connector type, various inputs are possible, which can be taken from the following summary:

Connector type	Assignments, hardware addresses and serial interfaces
nC	Upper case letters and digits n = No. characters (≤ n) Example: `184 TWU 3C = 64`
jK	*name or no specification j = No. of input signals of a hardware address; the actual number of pins can be < j. Example: `203 X5C 8K < *BINA_1`
1N	name or 0 Example: `19 PJ1 1N = FP1P1`
8N	Module name,submodule name, ... ,submodule name (max 7*submodule names) or 0 Example: `57 S13 8N = D13_P3,D130,D131,D132`
8R	name.sampling time number or 0, up to 64 consecutive numbers, separated by commas possible Example: `92 CCT 8R = S5SEND.T4`
DA	Date: tt.mm.jj Example: `18 CDA DA = 20.04.94`
DL	Dimensions: [max 8 characters], ... ,[max 8 characters] Example: `27 DIM DL = [mA],[kA],[up],[down]`
IK	Interrupt event: C1, C2, E1, E2, S1..S8 This entry causes an interrupt signal to be set on the L- or C bus. It can also be specified, whether the interrupt is initiated at the start or at the end of the transmit task. Entry: C1 (initiated at the start of the send task) C1 END (initiated at the end of the send task) Example: `91 ICS IK = C2 END`
IT	Alarm event entry for alarm task P16: E1, E2, C1, C2, S1 ... S8, IL, IC, TL, TC P32: E1 .. E4, C1, C2, S1 .. S8, IL, IC, TL, TC, L1 .. L4, X1 ..X32 Substitute sampling time entry for quasi cyclic for alarm tasks Example:

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Connector type	Assignments, hardware addresses and serial interfaces
TG	Basic sampling time and synchronization information: 'Time' [MS] {,SRC='Event'} {,TDL='Time'[MS]} {,SEND='Bus'} 'Time': The basic sampling time should always be specified as first parameter. It either involves its own basic sampling time, or for an interrupt-controlled clock, information specifying the equivalent sampling time. For a sampling time receiver, the same information is required as for the transmitter. Permissible entry: 0.1... 1 ... 16.0 [MS] realistic >= 1 [MS] SRC='Event': Its own basic cyclic clock is not used when this parameter is specified, but the specified event is taken as the clock source. Permissible entries: TL, TC (basic clock of another PN) IL, IC (basic clock via the bus interrupt) C1, C2, E1, E2, S1..S8 TDL='Time' : Time shift between the basic send- and receive clocks (must be less than the basic sampling time) SEND='Bus' : This specifies whether the basic clock should be switched to the L- and/or C bus; Permissible entries: TL (basic clock on the L bus) TC (basic clock on the C bus) TLC (basic clock on the L- and C-bus) Example: `85 T0 TG = 4.2[MS],SRC=C1,TDL=2[MS]`
TX	System FP sampling time: Tn n = sampling time number `91 TY TX = T4`

TS	Sampling time
	Multiple of the basic sampling time (only powers of 2 permitted), and a listing of all L- and C bus connections, which are used in these sampling times.
	Connector format
	1...32768(2**15), $name, L bus connection 1 and 2
	C$name,... C bus connection 1 and 2
	4$name,... L bus connection 4
	C4$name,... C bus connection 4
	F$name, Fast L bus connection 1 and 2
	FC$name,.. Fast C bus connection 1 and 2
	F4$name,.. Fast L bus connection 4
	FC4$name,.. Fast C bus connection 4
	Powers of two: 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, 2048, 4096, 8192, 16384, 32768
	`89 T4 TS = 16,$EXT2,C$EXT3,F$ISOLL, &`
	`& $EXT4,C$EXT5,FC$EXT6,C$EXT2`

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2.1.7 Terminating

The "EXIT" function is used to terminate entry into the master program editor and to save on the hard disk. A prompt first asks whether the data is to be archived or only saved (refer to Section 1). The master program is stored on the hard disk and the dialog system is exitted if the "archive" option is selected. A message window appears showing how many incomplete lines with question mark (?) are still contained in the MP, e.g.:

```
MP-DIA: finished 3 incomplete line(s)
```

The program returns to the basic dialog after this is confirmed with "OK".

2.2 Compiling the master program / MP Compile

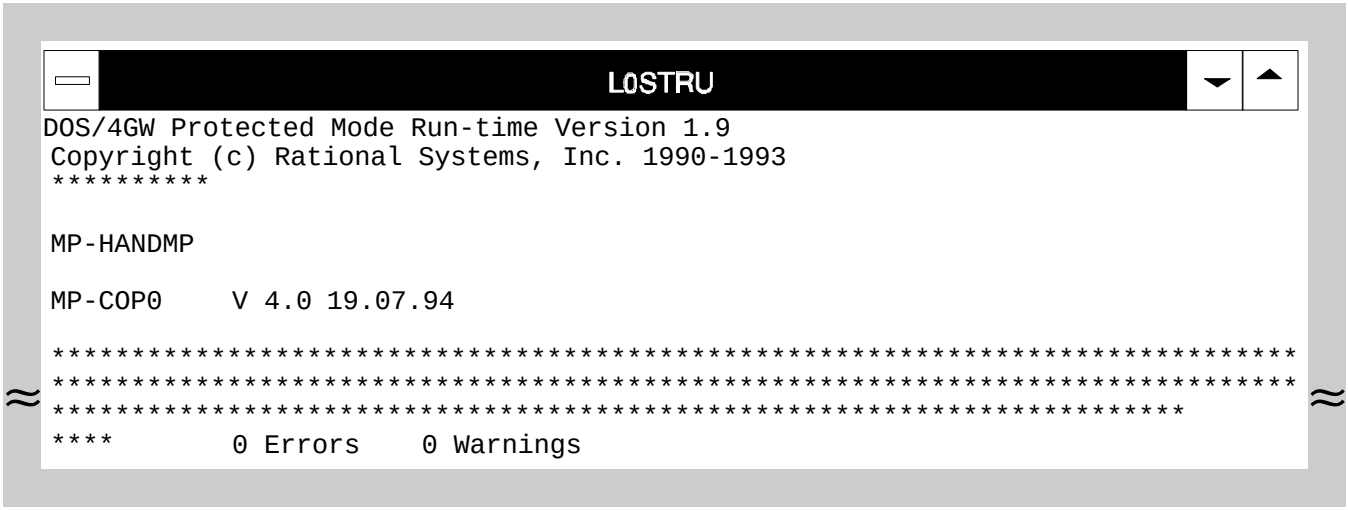
Master programs, generated in dialog are compiled using the **MP Compile** service program. The **MP Compile** service program is automatically included when the **Auto-Comp** service program is called-up.

2.2.1 Calling-up

Before the compiler is called-up, the master program must be selected from the available master programs of the selected project. The compiler is called-up from the basic dialog (**MP compile / Selected Master Program**).

2.2.2 Compiling

The MP name and the compilation program version are displayed on the screen. The number of existing errors and warnings is displayed after compilation has been completed, e.g.:



A message window with the following message appears after compilation has been completed:

```
MP-COP:  finished
```

This should be confirmed with "OK" and the program then returns to the basic dialog.

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2.2.3 Error messages / handling

The following errors are identified during compilation

- if several boards (submodules, subracks) have the same names
- if several communication initialization blocks have the same names
- incorrect processor program name
- illegal subrack layout
- erroneous FP connections
- erroneous communication configuring etc.

If errors are to be rectified, then **MP Edit / Configure** must be called-up again. In the source text, the compiler has inserted message lines, identified with ****?, to precisely localize and describe the particular error. For example:

```
****? EMOD1 multiple name definitions
```

The "NEXT ?" function (Section 1.9.2) can be used to quickly find these message lines. These errors can now be corrected, and **MP Compile** re-started after **MP Edit** is exited.

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