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SIEMENS

SIMATIC TI405

User Manual

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Preface

How to Use this Manual

This manual is a combination tutorial and reference manual for your SIMATIC® TI405™ products. The organization was chosen to help you install, maintain, and program your Series 405™ system. A detailed Table of Contents and Index provide you with the tools for fast reference to the facts you need.

A Quick Start section is provided following this Preface. This short chapter provides the steps for unpacking the system, as well as installing and entering a simple program.

Chapter 1 provides the environmental and electrical specifications for the TI405 products.

Chapter 2 provides the details for installing your TI405 system. Details from I/O configuration to wiring diagrams are included in this chapter.

Chapter 3 provides the instructions for performing preventive maintenance and troubleshooting your TI405 products. Error messages and steps for forcing I/O points are included in this chapter.

Chapter 4 provides the details for operating the Machine Interface Unit (MIU), a hand-held programming device, and for programming your Series 405 system.

Chapter 5 provides the details for designing relay ladder logic (RLL) programs.

Chapter 6 provides the details for designing Stage™ programs. Stage is a set of operators that combines with RLL to provide the tools for efficient machine control.

Chapter 7 provides examples of applications specific to the machine control industry.

Chapters 8 through 22 are reference sections for the TI405 instruction set.

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Key Terms and Abbreviations

Definitions for some of the terms used in this manual follow. Refer to the glossary for additional terms.

Central Processing Unit (CPU)	The unit that stores and executes the logic program.
Accumulator	The memory location where the CPU stores the intermediate results of an arithmetic or logical operation.
Machine Interface Unit	A simplified type of hand-held programming device. It provides you with the ability to enter and edit programs, save and restore programs on data tapes or memory cartridges, control system operation, and to monitor system status.
Memory Cartridge (MC)	A cartridge-type device consisting of either CMOS RAM, EEPROM, or UVPROM for storing programs or other memory values. They can be inserted or removed from the SIMATIC® TI435™ CPU or the MIU.
Machine Stage Program	A machine control program that combines relay ladder logic and the sequential function programming elements called Stage.
Stage	A program segment that only executes when made active by another Stage.

Technical Assistance

If you need information that is not included in this manual, or if you have problems using the system, contact your Siemens Industrial Automation, Inc. distributor or sales office. If you need assistance in contacting your distributor or sales office in the United States, call 1–800–964–4114.

Ordering Replacement Parts

To order replacement parts, or to obtain an Authorization Number for returning units, contact your Siemens Industrial Automation, Inc. distributor or sales office. If you need assistance in contacting your distributor or sales office in the United States, call 1–800–964–4114. Please be prepared to provide the part and PLC model numbers when you call.

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Quick Start

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Introduction

The steps listed in this Quick Start section allow you to install and operate a simple machine control program. The complete details for Series 405 product installation are given in Chapter 2. This section provides the details necessary for this demonstration. In this demonstration, you install a CPU, an input module, an output module, and a toggle switch. Then, you enter a simple program that turns an output module status LED on and off, whenever the input switch is toggled.

What You Need for a Quick Start

You need the following items for this demonstration.

- A SIMATIC® TI425™ or TI435 CPU.
- A CMOS RAM Memory Cartridge, if using the TI435.
- Any Series 405 Base.
- A PPX:U-50N 16-point 24-48 VDC Input module.
- A PPX:U-15T 24 VDC Output module.
- Wiring for 110 VAC line supply voltage.
- Hook-up wire.
- A 24 VDC toggle switch.
- A small Phillips-head screwdriver.

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Insert the CPU

Insert the CPU (with power supply) into the base as follows (see Figure i):

1. Tilt the CPU forward, and hook the tabs at the bottom rear into the slots at the bottom of the base frame.
2. Push the CPU toward the base until it is securely seated.
3. Tighten the securing screw.

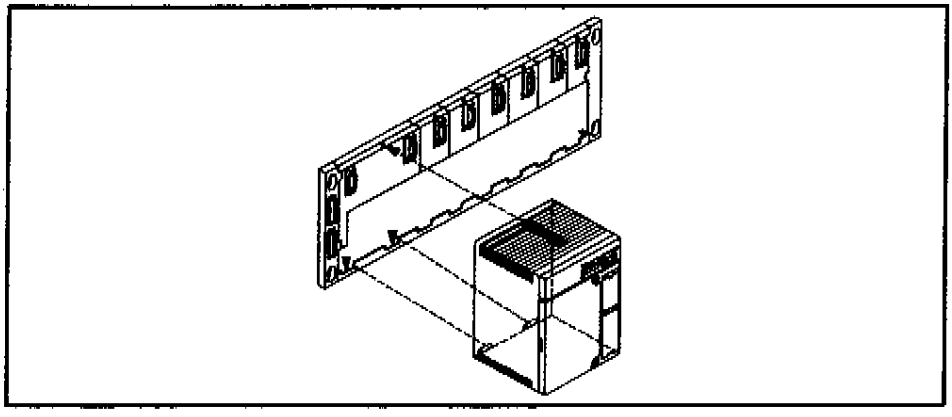


Figure i Inserting the CPU

If you have a TI435, insert a PPX:G-03M CMOS RAM cartridge in the CPU:

1. Remove the left panel cover on the CPU.
2. Insert the Memory Cartridge as shown in Figure ii.
3. Press firmly to ensure that the cartridge is seated in the CPU.

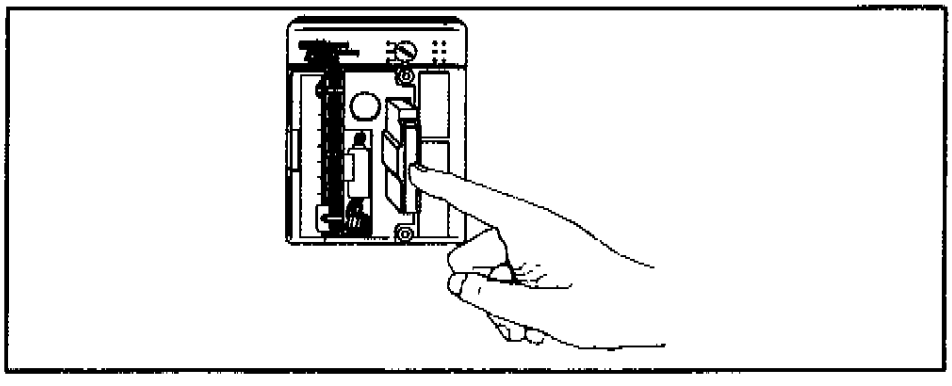


Figure ii Inserting a Memory Cartridge in the TI435

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Select the Supply Voltage

To operate from a 110 VAC supply voltage, install the shorting bar (included with the CPU) on the bottom two terminals, as shown in Figure iii. (To operate from a 220 VAC supply voltage line, do not install the shorting bar.)

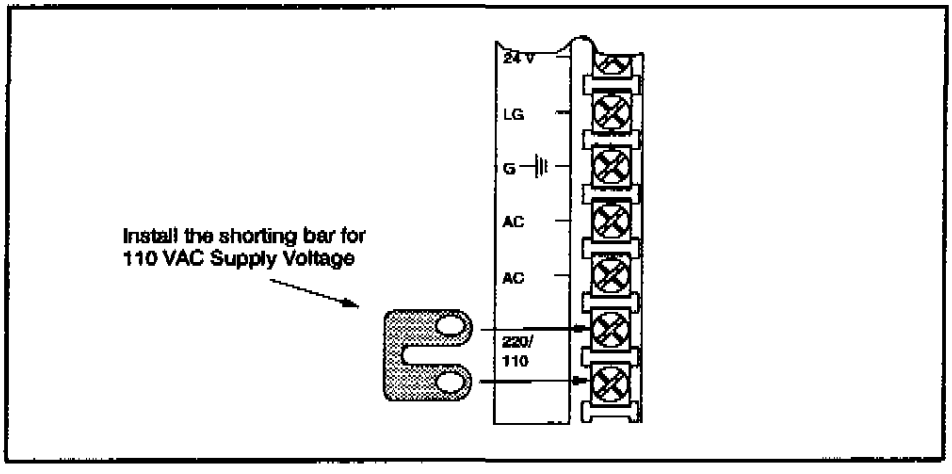


Figure iii 110 VAC Shorting Bar Installation

Insert the I/O Modules

Insert an Input and an Output module into the base as follows (see Figure iv):

1. Tilt these modules and hook their rear tab into the base as you did with the CPU.
2. Push the modules toward the base to seat them securely.
3. Tighten the securing screw.

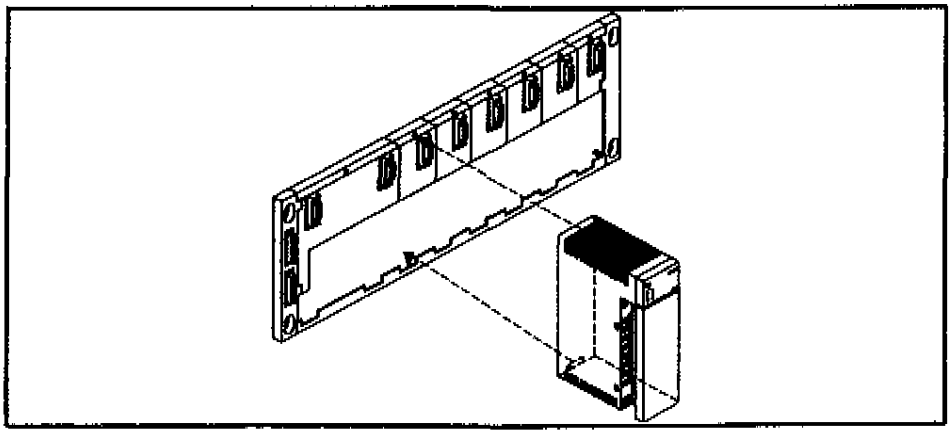


Figure iv Inserting the I/O Modules

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Connect the Wires for Line Power

1. Remove the large front panel on the left half of the CPU.
2. Ensure that the line power is off, then connect the 110 VAC line voltage supply wires to the terminals shown in Figure v.

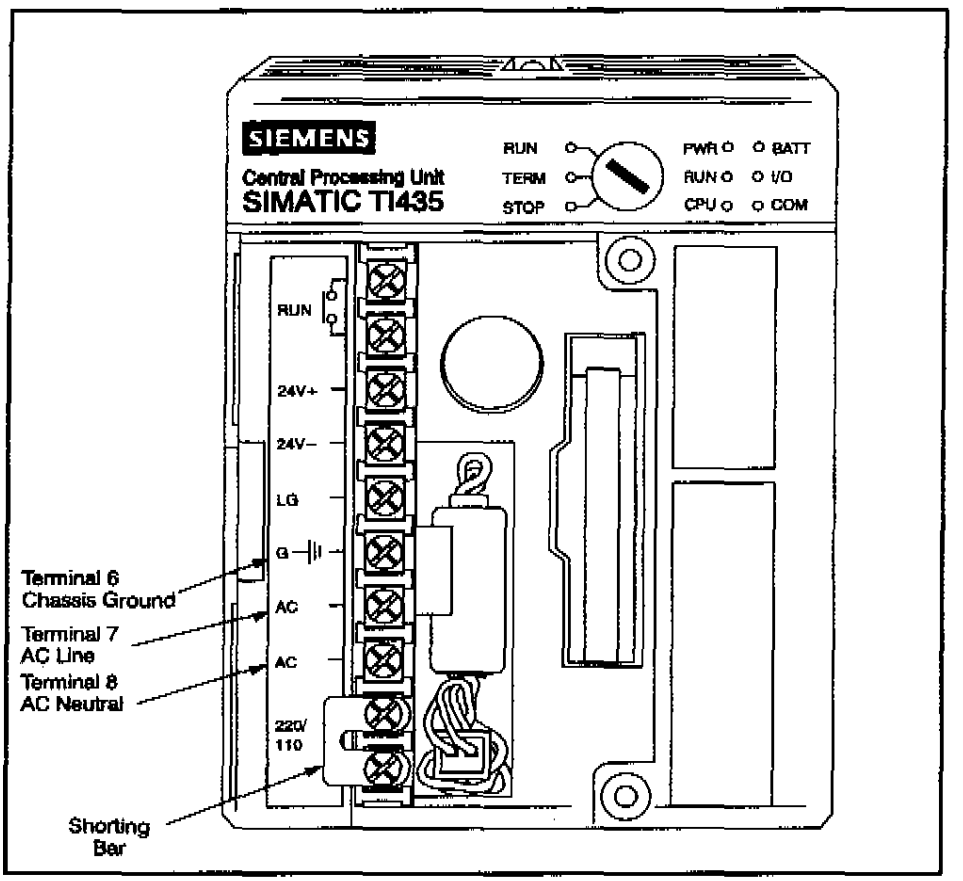


Figure v Connecting the CPU Line Power Wiring

⚠WARNING

To minimize risk of potential shock hazard and injury to personnel, be sure the unit is properly installed in an enclosure in order to minimize access to electrically live terminals. Only persons knowledgeable in the safe use of high voltage should perform this operation.

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Connect the I/O Module Wiring

Connect terminal 3 (24 VDC +) of CPU to the "CA" terminal of the first DC input in the base. This is the top screw terminal on the right half of the input module terminal strip, as shown in Figure vi.

Connect an Input Switch

1. Connect a single pole/single throw switch to terminal 4 (24 VDC–) of the CPU and to "0" of the first DC input module. This is the top screw terminal on the left half of the input module strip, as shown in Figure vi.

2. Replace the front panel on the CPU.

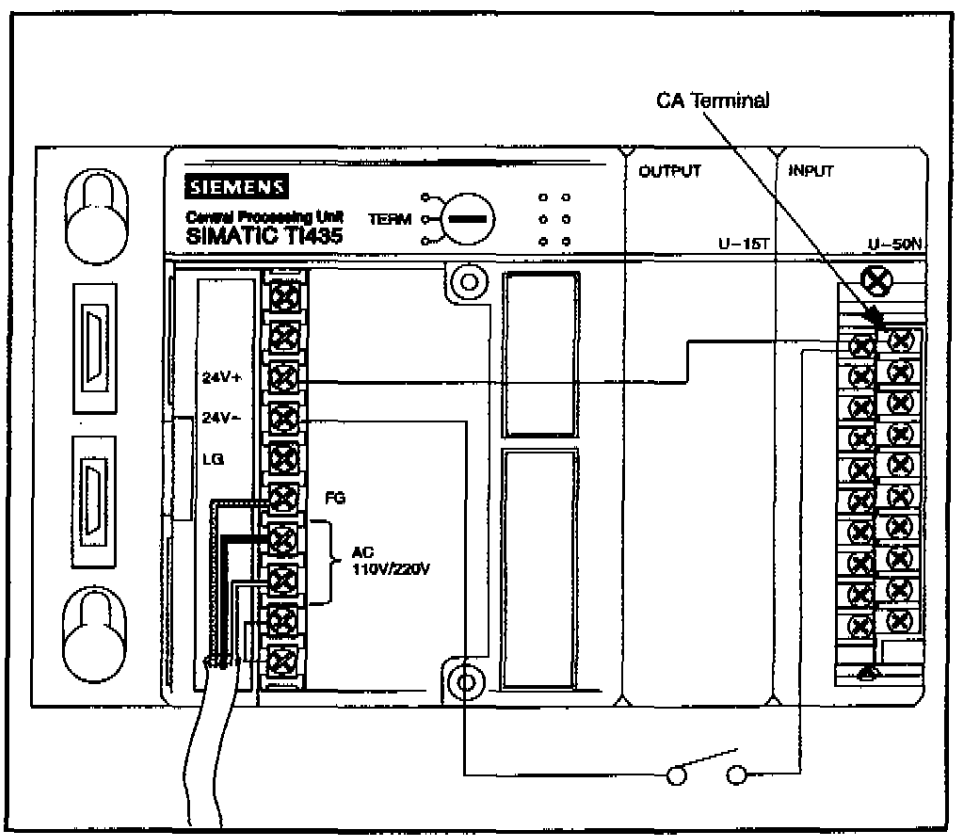


Figure vi Wiring the I/O Modules

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Attach the MIU

1. Remove the connector cover on the upper right hand side of the CPU.

2. Attach the connecting cable between the MIU and the CPU, as shown in Figure vii, or attach the MIU directly to the front of the CPU by mating the 15 pin connectors.

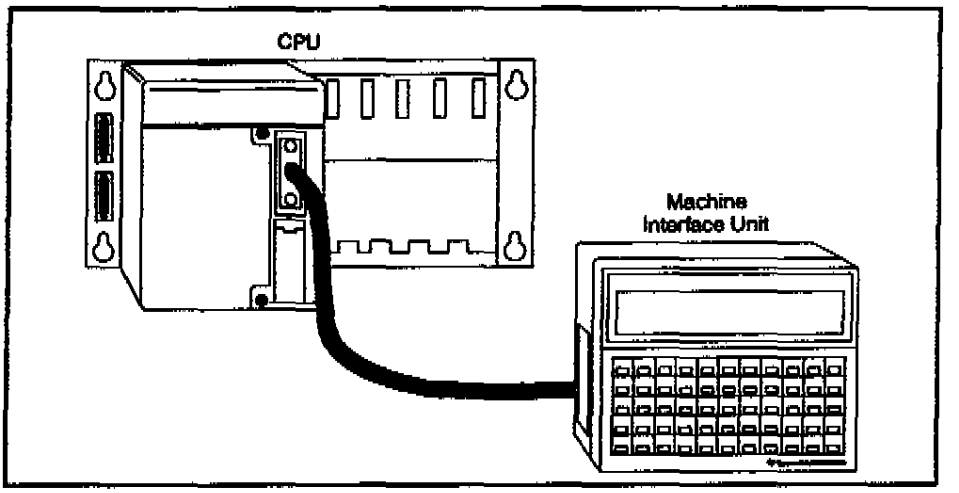


Figure vii Connecting the MIU

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Clear the Memory

To clear the memory, follow these steps.

1. Apply line power to the PLC.
2. Insert the key, then turn the keylock switch to the TERM position as shown in Figure viii.

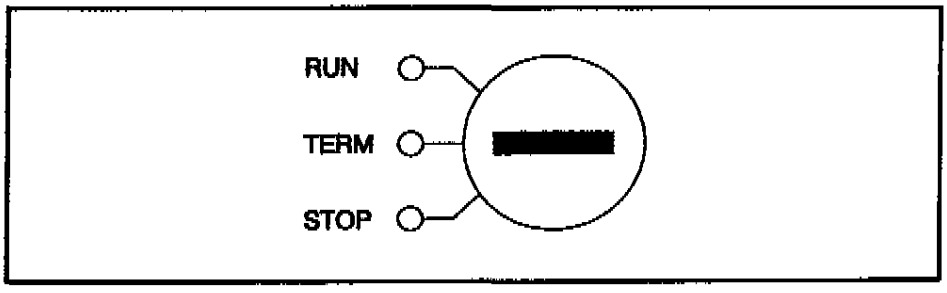


Figure viii Setting the Keylock Switch to TERM

3. Enter the following key sequences.

Key Sequence	Display
CLR CLR 1 3 AUX	AUX 1* Operating Mode AUX 13 Go To Pgm Mode
ENT	Pgm Mode?
ENT	Mode = Pgm
CLR 2 4 AUX	AUX 2* RLL Operations AUX 24 Clear Ladders
ENT	CLR All Ladders?
ENT	OK

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Enter A Program

Use the following key sequences to enter a test program into the CPU. This simple ladder program causes output "0" on the output module to turn on when you toggle the switch wired to the input module.

Key Sequence	Display
CLR (MAD) NXT	$ 0 NOP
STR (XIM) 0 ENT	STR X0
OUT (YOUT) 0 ENT	OUT Y0
END ENT	End
CLR CLR 1 1 AUX	AUX 1* Operating Mode AUX 11 Go To Run Mode
ENT	Run Mode?
ENT	Mode = Run

When you are finished, the CPU will be in RUN mode. Shaded keys represent the blue colored symbol identification keys on the MIU.

If you have difficulty entering your program, refer to Chapter 4 for more detailed instructions about using the Machine Interface Unit. If an error message is displayed on the MIU, refer to Chapter 3 for an explanation of the message and troubleshooting help.

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Chapter 1
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1.1 Product Summary

TI425 CPU

The TI425 CPU has a built-in power supply with an auxiliary 24 VDC power source (400 mA). It offers built-in 3.5K program RAM and includes a CPU battery. The TI425 CPU can be expanded to include up to 4 bases, and up to 640 I/O.

TI430 CPU

The TI430 CPU has a built-in power supply with an auxiliary 24 VDC power source (400 mA). It offers built-in 3.5K program EEPROM and includes a CPU battery. The TI430 CPU can be expanded to include up to 4 bases, and up to 640 I/O.

TI435 CPU

The TI435 CPU has a built-in power supply with an auxiliary 24 VDC power source (400 mA), and it offers a built-in network port. It can be expanded to include up to 4 bases and 640 I/O. A CPU battery is included. The TI435 CPU requires a memory cartridge.

TI405 Expansion Unit

The TI405 Expansion Unit has a built-in power supply with an auxiliary 24 VDC power source (400 mA). The TI405 bases are available in 4-, 6-, and 8-slots. Expansion models are available in those densities for connecting up to four bases in a single TI405 system, like the configuration in Figure 1-1.

Machine Stage Programming

The CPUs have Machine Stage built-in. Machine Stage is a machine control language that is combined with relay ladder logic (RLL) to create programs in less than one-third the time required with RLL only.

Handheld Programmer

The PPX:S-10P Machine Interface Unit (MIU) is a hand-held programming device that provides more than just programming features. The MIU:

- Displays messages. It displays 96 preprogrammed error messages or messages that you create.
- Monitors actual values of timers and counters.
- Programs memory cartridges.
- Uploads and downloads programs from/to the PLC and cassette tape.
- Uses TEST mode to help get your machine online faster and more safely.
- Can be mounted directly on the CPU or attached with a PPX:S-30JP 3-meter (9 foot) cable or a PPX:S-15JP 1.5-meter (4.5 foot) cable.
- Offers a full range of program entry and editing operations including search and replace.

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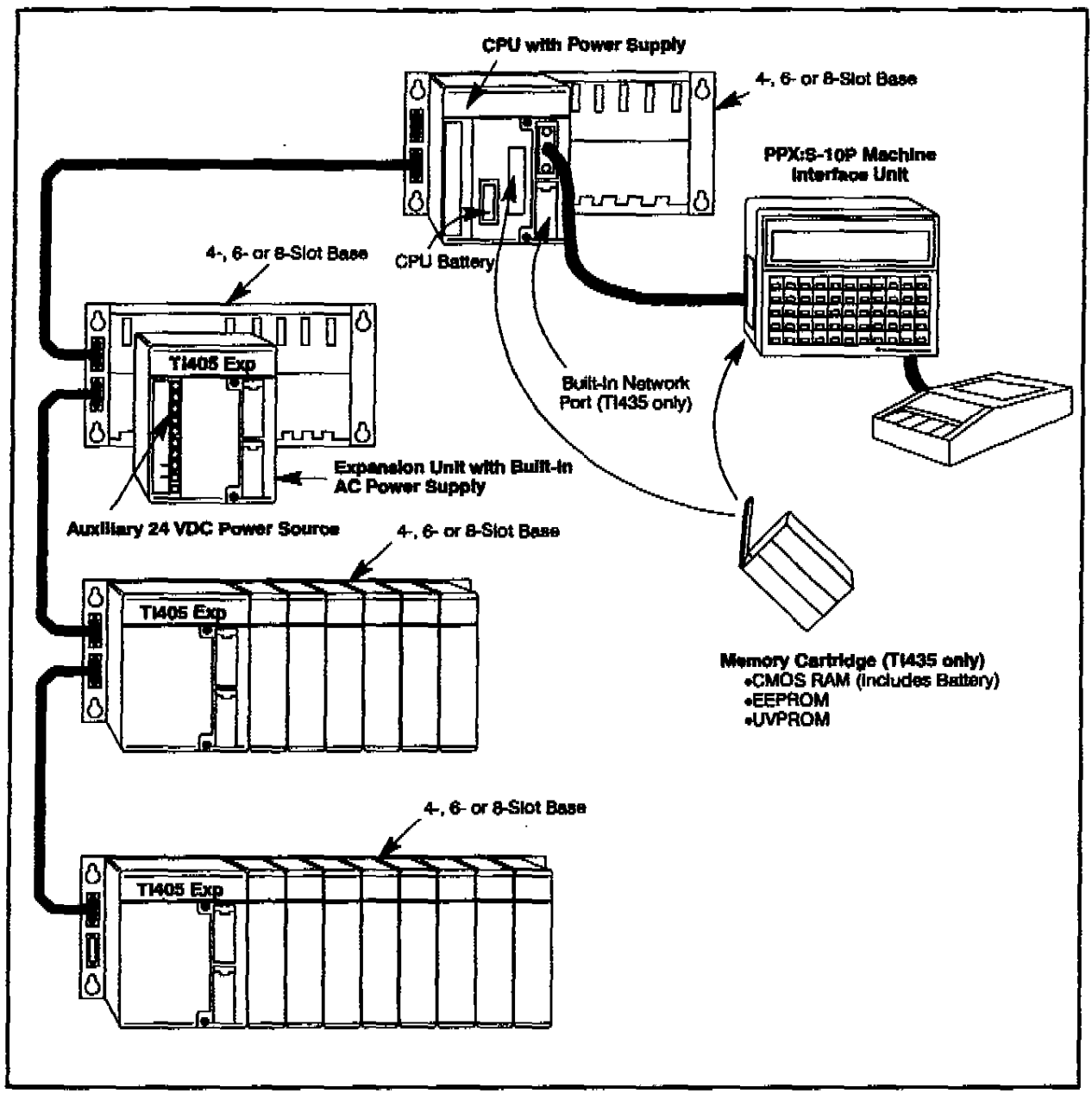


Figure 1-1 TI405 Product Family

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Product Summary (continued)

Memory Cartridges	Removable Memory Cartridges are available in CMOS RAM, EEPROM, and UVPROM types. The CMOS RAM cartridge is useful for fast program and system parameter backup.
Base Units	Bases are available with 4, 6, or 8 slots, and with or without expansion connections. Up to four expansion type bases can be connected in series. The bases are connected using either a PPX:U-01J 1.0-meter (3 foot) expansion cable or a PPX:U-05J 0.5-meter (1.5 foot) expansion cable. On any base, the maximum number of modules is determined by the total power consumption of the components used in the base.
TI405 I/O	The TI405 I/O consists of modules for 12/24 VDC input/output, 110/220 VAC input/output, and Relay output in 8- and 16-point densities. Each module has its own diagnostic LEDs and two commons per module for better isolation. Their thermal dissipation characteristics allow them to drive outputs at 2 A for each channel (8-point modules) over their entire operating temperature range.
Cassette Program Storage	Programs and system parameters can be stored on digital cassette tapes with a customer-supplied data recorder attached to the MIU by the PPX:S-08JR Cassette Interface cable.

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1.2 CPU Specifications

Table 1-1 Environmental Specifications for PPX:425-CPU, PPX:425DC-CPU, PPX:430-CPU, PPX:435-CPU, PPX:435DC-CPU, and PPX:435DC1-CPU

Specification	CPU
Operating temperature	0° – 60° C
Storage temperature	-20° – 70° C
Humidity	5–95% non-condensing
Dielectric strength	1500 VAC 1 min. between primary , secondary, FG, and RUN contacts
Insulation	20M ohms 500 VDC between primary, secondary, FG, and RUN contact (PPX:435DC1-CPU = >100M ohms)
Vibration	MIL STD 810C 514.2
Shock	MIL STD 810C 516.2
Noise immunity	NEMA ICS3–304 Impulse 1000 V 1 µs
Dimensions (mm)	108 (W) x 150 (H) x 110 (D)
Environmental air	No corrosive gases

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Table 1-2 CPU General Specifications

Specification	PPX:425–CPU	PPX:425DC–CPU	PPX:430–CPU
I/O points	640	640	640
Base density	4/6/8 slots	4/6/8 slots	4/6/8 slots
Module density	8/16/32 points	8/16/32 points	8/16/32 points
Analog I/O Input Output	 40 channels 20 channels	 40 channels 20 channels	 40 channels 20 channels
Remote I/O base distance max.	3300 feet (1000 m)	3300 feet (1000 m)	3300 feet (1000 m)
Remote I/O points	512	512	512
Battery life	5 years	5 years	5 years
Memory (total) Ladder Variable	6.5K 3.5K 3K	6.5K 3.5K 3K	6.5K 3.5K 3K
Program storage RAM (battery backed) UVPROM EEPROM Cassette tape backup	Built-in Yes No No Yes	Built-in Yes No No Yes	Built-in No No Yes (standard or built-in) Yes
Scan rate per 1K boolean	3 ms	3 ms	3 ms
Programming Language Instruction Set	RLL and Machine Stage Boolean and Data operation	RLL and Machine Stage Boolean and Data operation	RLL and Machine Stage Boolean and Data operation
Total number of instructions	122	122	122
Integer math	Yes	Yes	Yes
Program security CPU mode keylock Password Program name	 Yes No Yes	 Yes No Yes	 Yes No Yes
Total number of control relays	480 (can use unused local outputs and remote I/O as CRs)	480 (can use unused local outputs and remote I/O as CRs)	480 (can use unused local outputs and remote I/O as CRs)
Retentive memory (CRs etc.)	Configurable	Configurable	Configurable
Special relays	62	62	62
Timers/counters (4-digit BDC)	128/128	128/128	128/128
Program stages	384	384	384
Subroutines	No	No	No
For/next loops	No	No	No
Immediate I/O update	Yes	Yes	Yes
Built-in diagnostics	Yes	Yes	Yes
TISOFT IBM® PC software	Yes	Yes	Yes
Machine interface unit	Yes	Yes	Yes
Agency approvals	UL, FCC	UL, FCC	UL, FCC

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Table 1-2 CPU General Specifications (continued)

Specification	PPX:425–CPU	PPX:425DC–CPU	PPX:430–CPU
Power required	85 to 132 VAC 170 to 264 VAC 47 to 63 Hz 50 VA 20 A maximum inrush	20 to 28 VDC 3 A input current 20 A maximum inrush 38 W power	85 to 132 VAC 170 to 264 VAC 47 to 63 Hz 50 VA 20 A maximum inrush
Power supplied	3700 mA at 5 VDC to base 400 mA at 24 VDC external	3700 mA at 5 VDC to base	3700 mA at 5 VDC to base 400 mA at 24 VDC external
Discrete I/O	320 inputs/320 outputs	320 inputs/320 outputs	320 inputs/320 outputs
Bases/system	4	4	4
Removable connectors	Yes	Yes	Yes
Commons per module	2	2	2
CPU run mode relay	250 VAC/1 A 50/60 Hz 30 VDC 1 A	250 VAC/1 A 50/60 Hz 30 VDC 1 A	250 VAC/1 A 50/60 Hz 30 VDC 1 A
Diagnostics			
Programmed diag. messages	74	74	74
User-defined messages	4-digit	4-digit	4-digit
CPU diagnostic LEDs	6	6	6
I/O module diag. LEDs	3	3	3
System diag. special relays	14	14	14
Debug			
"N" scan	Yes	Yes	Yes
Search and replace	No	No	No
Hold selected outputs during TEST STOP	Yes	Yes	Yes
Programmable watchdog	Yes	Yes	Yes
Program support relays	60	60	60
Clock relays	7	7	7
CPU status relays	9	9	9
System check relays	15	15	15
Accumulator relays	13	13	13
Data communications relays	16	16	16
Communications master/slave	Yes*	Yes*	Yes

* U–01DM required for network interface.

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Table 1-2 CPU General Specifications (continued)

Specification	PPX:435–CPU	PPX:435DC–CPU	PPX:435DC1–CPU
I/O points	640 (320 in, 320 out)	640 (320 in, 320 out)	640 (320 in, 320 out)
Base density	4/6/8 slots	4/6/8 slots	4/6/8 slots
Module density	8/16/32 points	8/16/32 points	8/16/32 points
Analog I/O Input Output	 40 channels 20 channels	 40 channels 20 channels	 40 channels 20 channels
Remote I/O base distance	3300 feet (1000 m) max.	3300 feet (1000 m) max.	3300 feet (1000 m) max.
Remote I/O points	512	512	512
Battery life Memory cartridge battery	5 years 3 years	5 years	5 years
Memory (total) Ladder Variable	10.5 K 7.5 K 3 K	10.5 K 7.5 K 3.0 K	10.5 K 7.5 K 3.0 K
Program storage RAM (battery backed) UVPROM EEPROM Cassette tape backup	Cartridge Yes Yes Yes Yes	Cartridge Yes Yes Yes Yes	Cartridge Yes Yes Yes Yes
Scan rate per 1 K boolean	0.49 ms	0.49 ms	0.49 ms
Programming Language Instruction Set	RLL and Machine Stage Boolean and Data operation	RLL and Machine Stage Boolean and Data operation	RLL and Machine Stage Boolean and Data operation
Total number of instructions	174	174	174
Integer math	Yes	Yes	Yes
Program security CPU mode keylock Password Program name	 Yes Yes Yes	 Yes Yes Yes	 Yes Yes Yes
Total number of control relays	480 (can use unused local outputs and remote I/O as CRs)	480 (can use unused local outputs and remote I/O as CRs)	480 (can use unused local outputs and remote I/O as CRs)
Retentive memory (CRs etc.)	Configurable	Configurable	Configurable
Special relays	62	62	62
Timers/counters (4-digit BDC)	128/128	128/128	128/128
Program stages	384	384	384
Subroutines	Yes	Yes	Yes
For/next loops	Yes	Yes	Yes
Immediate I/O update	Yes	Yes	Yes
Built-in diagnostics	Yes	Yes	Yes
TISOFT IBM® PC software	Yes	Yes	Yes
Machine interface unit	Yes	Yes	Yes
Agency approvals	UL, FCC	UL, FCC	UL, FCC

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Table 1-2 CPU General Specifications (continued)

Specification	PPX:435–CPU	PPX:435DC–CPU	PPX:435DC1–CPU
Power required	85 to 132 VAC 170 to 264 VAC 47 to 63 Hz 50 VA 20 A maximum inrush	20–28 VDC 3 A input current 20 A maximum inrush 38 W power	90 to 146 VDC ± 10% ripple 30 W maximum 2 A maximum 20 A maximum inrush
Power supplied	3700 mA at 5 VDC to base 400 mA at 24 VDC external	3700 mA at 5 VDC to base	3700 mA at 5 VDC to base
Discrete I/O	320 inputs/320 outputs	320 inputs/320 outputs	320 inputs/320 outputs
Bases/system	4	4	4
Removable connectors	Yes	Yes	Yes
Commons per module	2	2	2
CPU run mode relay	250 VAC/1 A 50/60 Hz 30 VDC 1 A	250 VAC/1 A 50/60 Hz 30 VDC 1 A	250 VAC/1 A 50/60 Hz 30 VDC 1 A
Diagnostics			
Programmed diag. messages	98	98	98
User-defined messages	23 character	23 character	23 character
CPU diagnostic LEDs	6	6	6
I/O module diag. LEDs	3	3	3
System diag. special relays	14	14	14
Debug			
"N" scan	Yes	Yes	Yes
Search and replace	Yes	Yes	Yes
Hold selected outputs during TEST STOP	Yes	Yes	Yes
Programmable watchdog	Yes	Yes	Yes
Program support relays	62	62	62
Clock relays	7	7	7
CPU status relays	11	11	11
System check relays	15	15	15
Accumulator relays	13	13	13
Data communications relays	16	16	16
Communications master/slave	Yes	Yes	Yes

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1.3 Base Specifications

Base Environmental Specifications

The following table lists the environmental specifications for the 4-, 6-, and 8-slot bases.

Operating temperature	0° to 60° C (32° to 140°F)
Storage temperature	-20° to 70° C (4° to 158°F)
Operating humidity	5% to 95% (noncondensing)
Environmental air	No corrosive gases permitted
Voltage withstand	600 VAC, 1 min. between ground and circuit. Note: No voltage withstand if shorted between ground and circuit.
Insulation resistance	10M ohms. 500 VDC between ground and circuit. Note: No insulation if shorted between ground and circuit.
Noise immunity	NEMA ICS3-304. Impulse 1000 V 1 µs

Overall Base Dimensions

The following table lists the overall base dimensions.

	PPX: U-04BJ	PPX: U-04B	PPX: U-06BJ	PPX: U-06B	PPX: U-08BJ	PPX: U-08B
Number of Slots	4	4	6	6	8	8
Expansion Capability	No	Yes	No	Yes	No	Yes
Length	293 mm	293 mm	367 mm	367 mm	441 mm	441 mm
Width	150 mm	150 mm	150 mm	150 mm	150 mm	150 mm

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1.4 Discrete Input Module Specifications

Specifications	PPX:U-05N 12-24 VDC Input (Negative logic)	PPX:U-50N 24-48 VDC Input (Isolated)	PPX:U-55N 12-24 VAC/VDC Input
Circuits per module	16	8	16
Commons per module	2	8	2
Normal input voltage range	10.2-26.4 VDC	20-52.8 VDC	10.2-26.4 VAC/VDC
AC frequency	N/A	N/A	47-63 Hz
Maximum input voltage	26.4 VDC	52.8 VDC	37.5 VAC/VDC
Input current	3.8 mA (12 V) 8.3 mA (24 V)	5 mA (24 V) 10 mA (48 V)	3.8 mA (12 V) 8.3 mA (24 V)
Input switching characteristics On level Off level Off to On response On to Off response	 9.5 V 4.0 V 1-7 ms 2-12 ms	 >18 V <7 V 3-10 ms 3-12 ms	 9.5 V 3.0 V 5-40 ms 10-50 ms
Status Indicator Maximum Off current Minimum On current	 Logic side 1.5 mA 3.5 mA	 Logic side 1.5 mA 3.5 mA	 Logic side 1.5 mA 4.0 mA
Internal power consumption (max.) @ +5 V	150 mA	100 mA	150 mA
Weight	250 g	250 g	250 g
Removable connector	Yes	Yes	Yes
Temperature derating	No	No	No

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Discrete Input Module Specifications (continued)

Specifications	PPX:U-20N 115/230 VAC Input (Negative/positive logic)	PPX:U-25N 115 VAC Input
Circuits per module	8	16
Commons per module	2	2
Normal input voltage range	80-265 VAC	80-132 VAC
AC frequency	47-63 Hz	47-63 Hz
Maximum input voltage	265 VAC	132 VAC
Input current	8.5 mA (100 V, 60 Hz) 20 mA (230 V, 60 Hz)	12.5 mA (100 V, 60 Hz) 14.5 mA (115 V, 60 Hz)
Input switching characteristics On level Off level Off to On response On to Off response	 >70 V <30 V 5-30 ms 10-50 ms	 >70 V <30 V 5-30 ms 10-50 ms
Status Indicator Maximum Off current Minimum On current	Logic side 2 mA 7 mA	Logic side 2 mA 7 mA
Internal current consumption (max.) @ +5 V	100 mA	150 mA
Weight	240 g	270 g
Removable connector	Yes	Yes
Temperature derating	No	No

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1.5 Discrete Output Module Specifications

Specifications	PPX:U-01T Relay Output	PPX:U-05T Relay Output	PPX:U-12T 12/24 VDC Output (Negative logic, Sinking)	PPX:U-55T 12/24 VDC Output (Positive logic, Sourcing)
Output type	N. O. relay	N. O. relay	NMOS FET Open drain	NPN
Circuits per module	8	16	8	16
Commons per module	2	2	2	2
Operating voltage	5-250 VAC 5-30 VDC	5-250 VAC 5-30 VDC	10.2 - 26.4 VDC	10.2 - 26.4 VDC
Peak voltage	265 VAC	265 VAC	40 V	40 VDC
Maximum current (resistive)	2 A 5 A/common	1 A 5 A/common	2 A 5 A/common	0.5 A 3 A/common
Maximum leakage current	0.1 mA @ 265 VAC	0.1 mA @ 265 VAC	0.1 mA @ 40 VDC	0.1 mA @ 40 VDC
ON voltage drop	N/A	N/A	0.5 V @ 2 A	1.5 V @ 0.5 A
Smallest recommended load	5 mA @ 5 VDC	5 mA @ 5 VDC	0.2 mA @ 5 VDC	0.2 mA @ 5 VDC
Maximum inrush	2 A	4 A	6 A for 100 ms 12 A for 10 ms	1 A for 100 ms 2 A for 10 ms
Off to On response	12 ms	10 ms	1 ms	1 ms
On to Off response	12 ms	10 ms	1 ms	1 ms
Status Indicator	Logic side	Logic side	Logic side	Logic side
Internal fuses	2 @ 8 A	2 @ 8 A	2 @ 7 A	2 @ 5 A
Replaceable fuses	No	No	No	No
Internal current consumption (max.) @ +5 V	550 mA	1000 mA	150 mA	350 mA
Weight	260 g	310 g	240 g	280 g
Removable connector	Yes	Yes	Yes	Yes
Temperature derating	No	No	No	Yes
External power source required	No	No	35 mA max @ 26.4 VDC	No

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Discrete Output Module Specifications (continued)

Specifications	PPX:U-15T 24 VDC Output (Negative logic, Sinking)	PPX:U-20T 115/230 VAC Output	PPX:U-25T 115/230 VAC Output
Output type	NPN Open collector	SSR	SSR
Circuits per module	16	8	16
Commons per module	2	2	2
Operating voltage	4.5 - 26.4 VDC	15 - 265 VAC	15 - 265 VAC
Peak voltage	40 V	265 V	265 VAC
Maximum current (resistive)	0.5 A 3 A/common	2 A 5 A/common	0.5 A 3 A/common
On voltage drop	0.1 mA @ 40 VDC	5 mA @ 265 VAC	4 mA @ 265 VAC
Smallest recommended load	0.2 mA	10 mA @ 15 V	10 mA @ 15 V
Maximum inrush	1 A for 100 ms 2 A for 10 ms	10 A for 100 ms 30 A for 10 ms	10 mA @ 100 V 15 A for 10 ms
Off to On response	0.5 ms	1 ms	1 ms
On to Off response	0.5 ms	1 ms + 1/2 cycle	1 ms + 1/2 cycle
Status Indicator	Logic side	Logic side	Logic side
Internal fuses	2 @ 5 A	2 @ 8 A	2 @ 5 A
Replaceable fuses	No	No	No
Internal current consumption (max.) @ +5 V	200 mA	250 mA	450 mA
Weight	270 g	330 g	350 g
Removable connector	Yes	Yes	Yes
Temperature derating	No	Yes	Yes
External power source required	125 mA @ 24 VDC	No	No

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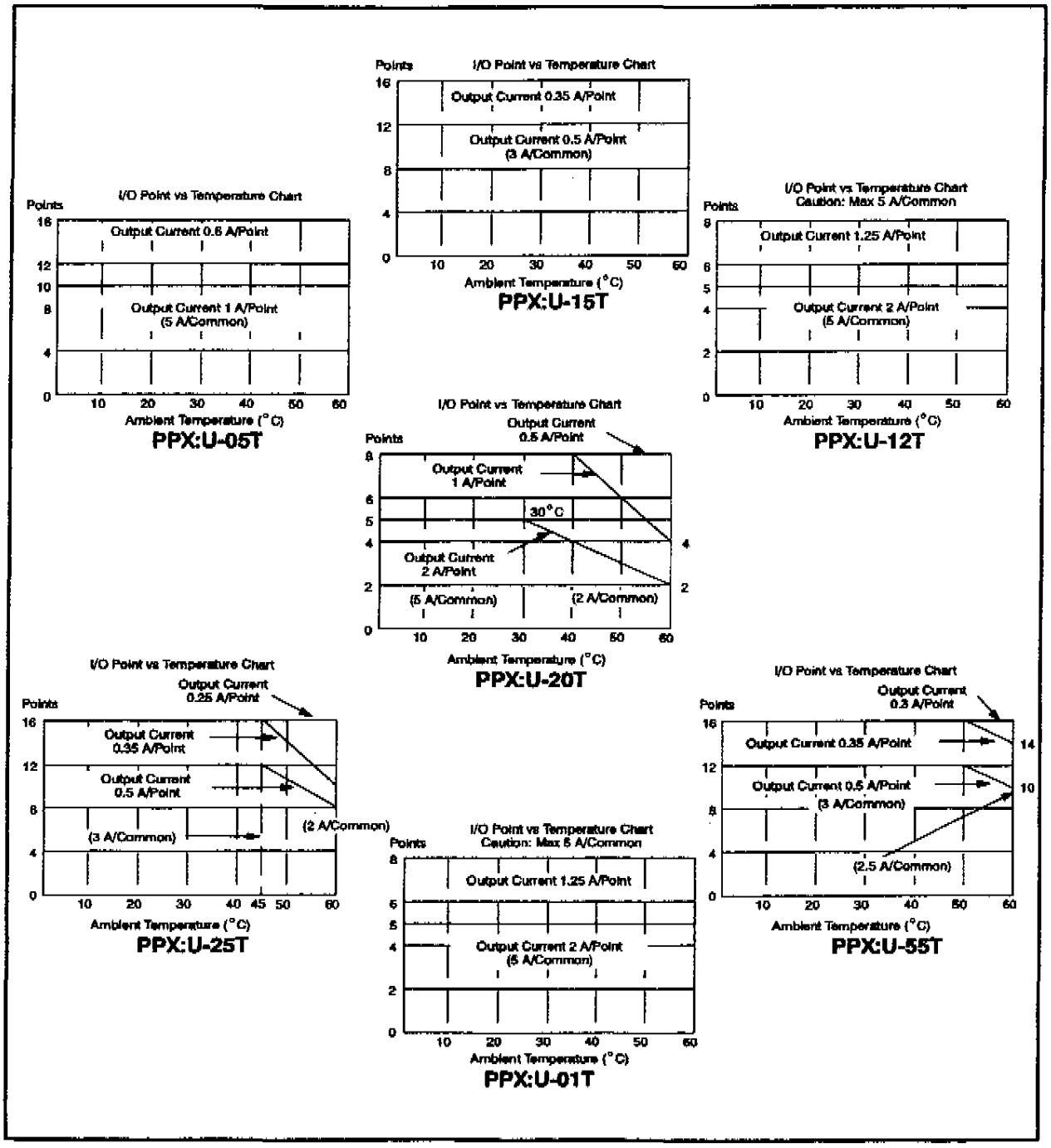


Figure 1-2 Discrete Output Module Derating Charts

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1.6 Input Simulator Module Specifications

The Input Simulator module, PPX:U-05S, provides a tool that can simulate either eight or sixteen discrete input points.

Operating temperature	0° to 60°C (32° to 140°F)
Humidity	5 to 95%, noncondensing
Power Supply Requirements External supply Current Consumption on internal 5 V	 N/A 4 mA/circuit, maximum 150 mA

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1.7 Expansion Unit Specifications

Expansion Unit Specifications for PPX:U-IOEX

Table 1-3 lists the environmental and operational specifications for the TI405 Expansion Unit.

Table 1-3 PPX:U-IOEX General Specifications

Operating temperature	0° to 60°C (32° to 140°F)		
Storage temperature	–20° to 70°C (4° to 158°F)		
Operating humidity	5% to 95% (noncondensing)		
Environmental air	No corrosive gases permitted		
Vibration	MIL STD 810C 514.2		
Shock resistance	MIL STD 810C 516.2		
Voltage withstand	1500 VAC 1 min. between primary, secondary, FG and RUN contact.		
Insulation resistance	20M ohms. 500 VDC between primary, secondary, FG and RUN contact.		
Noise immunity	NEMA ICS3-304. Impulse 1000 V 1 μs		
Dimensions (mm)	108 (W) x 150 (H) x 110 (D)		
Weight	640 g		
Plastic material	ABS		
Voltage range	85 to 132 VAC; 170 to 264 VAC		
Frequency range	47 to 63 Hz		
Input current	1.3 A		
Inrush current	20 A maximum		
Input power	50 W maximum		
Output voltage	5.1 V ± 0.25	20 to 28 V	+12 V –12 V
Ripple	Less than 100 mVp-p	More than 1 Vp-p	Less than 100 mV
Output current	0.1 to 3.7 A	0 to 0.4 A	24 mA
Input/output protection	Current limiter: Input and output Voltage limiter: Output		

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1.8 Calculating Power Requirements

Table 1-4 through Table 1-7 list the power requirements in milliamps for the TI405 CPUs, bases, input and output modules, and the handheld programmer (PPX:S-10P Machine Interface Unit).

Table 1-4 Power Available for TI405 CPUs

TI405 CPUs	Description	Power Supplied (mA)
TI425 CPU	TI425 CPU with AC Power Supply[1] (Includes 3.5K words of program RAM)	3700
TI425DC CPU	DC Power Supply [2] (Includes 3.5K words of program RAM)	
SIMATIC® TI430™ CPU	AC Power Supply [1] (Includes 3.5K words of program EEPROM)	
TI435 CPU	TI435 CPU with AC Power Supply[1] (Requires memory cartridge)	3700
TI435DC CPU	DC Power Supply [2] (Requires memory cartridge)	
TI435DC1 CPU	DC Power Supply [2] (Requires memory cartridge)	
TI405 Expansion Unit (PPX:405-IOEX)	Expansion unit with AC power supply[1]	4000

[1] These devices can also provide power to external devices (24 VDC @ 400 mA).
[2] Does not provide external 24 VDC.

Table 1-5 Power Requirements for TI405 Bases

TI405 Bases	Description	Power Required (mA)
PPX:U-04B	4-slot base with expansion	80
PPX:U-06B	6-slot base with expansion	80
PPX:U-08B	8-slot base with expansion	80
PPX:U-04BJ	4-slot base without expansion	80
PPX:U-06BJ	6-slot base without expansion	80
PPX:U-08BJ	8-slot base without expansion	80

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Table 1-6 Power Requirements for TI405 I/O Modules

TI405 I/O Modules	Description	Power Required (mA)
TI405 DC Input Modules		
PPX:U-50N	24/48 VDC input module, 8 points (–/+ logic)	100
PPX:U-05N	12/24 VDC input module, 16 points (– logic)	150
PPX:U-55N	12/24 VDC/AC input module, 16 points	150
TI405 AC Input Modules		
PPX:U-20N	110/220 VAC input module, 8 points	100
PPX:U-25N	110 VAC input module, 16 points	150
TI405 DC Output Modules		
PPX:U-12T	12/24 VDC output module, 8 points, 2 A (– logic)	150
PPX:U-15T	12/24 VDC output module, 16 points, 0.5 A (– logic)	200
PPX:U-55T	12/24 VDC output module, 16 points, 0.5 A (+ logic)	350
TI405 AC Output Modules		
PPX:U-20T	110/220 VAC output, 8 points, 2 A	250
PPX:U-25T	110/220 VAC output, 16 points, 0.5 A	450
TI405 Relay Output Modules		
PPX:U-01T	Relay output module, 8 points, 2 A	550
PPX:U-05T	Relay output module, 16 points, 1 A	1000

Table 1-7 Power Requirements for TI405 Handheld Programmer

TI405 Handheld Programmer	Description	Power Required (mA)
PPX:405-MIU	Machine Interface Unit (Includes PROM burner) (963 mA to write EPROM)	320

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Calculating Power Requirements Using a CPU

Figure 1-3 illustrates how to calculate the power requirements in a system with a CPU and the listed module types.

1. Enter the total power supplied, which is 3,700 mA with a CPU as the source.
2. Find the power consumption values for each module type from the chart in Table 1-4. If the PPX:S-10P MIU will be left attached while the CPU is in RUN mode, you must include the MIU's power consumption.
3. Total the individual module consumptions and place that in the total power consumed box. The configuration will only work if the total power consumed is less than the total power supplied.

Base Number *0* **Location** _____

Module Position	Module Type	Power Consumption (mA)
Slot 0	*PPX:U-25N 110 VAC In—16pt*	*150*
Slot 1	*PPX:U-25N 110 VAC In—16pt*	*150*
Slot 2	*PPX:U-25N 110 VAC In—16pt*	*150*
Slot 3	*PPX:U-25N 110 VAC In—16pt*	*150*
Slot 4	*PPX:U-15T 12/24 VDC Out—16pt*	*200*
Slot 5	*PPX:U-25T 110/220 VAC Out—16pt*	*450*
Slot 6	*PPX:U-25T 110/220 VAC Out—16pt*	*450*
Slot 7	*PPX:U-25T 110/220 VAC Out—16pt*	*450*
	PPX:S-10P Machine Interface Unit	*320*
	Base	*80*

Total Power Supplied is 3700 mA if a CPU/Power Supply is being used
OR
4000 mA if a PPX:405-IOEX Expansion Unit is being used

Total Power Supplied: *3700*

Total Power Consumed: *2550*

This module combination is valid only if the Total Power Consumed number is less than the Total Power Supplied number.

Figure 1-3 Power Budget Worksheet Example #1

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Calculating Power Requirements in Expansion Bases

Figure 1-4 illustrates how to calculate the power requirements in an expansion base with the Expansion Unit and the listed module types.

1. Enter the total power supplied, which is 4,000 mA with an Expansion Unit as the source.
2. Find the power consumption values for each module type from the chart in Table 1-4.
3. Total the individual module consumptions and place that in the total power consumed box. The configuration will only work if the total power consumed is less than the total power supplied.

Base Number *1* **Location** _____

Module Position	Module Type	Power Consumption (mA)
Slot 0	*PPX:U-55N 12/24 VDC In—16pt*	*150*
Slot 1	*PPX:U-55N 12/24 VDC In—16pt*	*150*
Slot 2	*PPX:U-55T 12/24 VDC Out—16pt*	*350*
Slot 3	*PPX:U-05T Relay Out—16pt*	*1000*
Slot 4	*PPX:U-05T Relay Out—16pt*	*1000*
Slot 5	*PPX:U-05T Relay Out—16pt*	*1000*
Slot 6	*N/A*	
Slot 7	*N/A*	
	PPX:S-10P Machine Interface Unit	*N/A*
	Base	*80*

Total Power Supplied is
3700 mA if a CPU/Power Supply is being used
OR
4000 mA if a PPX:405-IOEX Expansion Unit is being used

Total Power Supplied: *4000*

Total Power Consumed: *3730*

This module combination is valid only if the Total Power Consumed number is less than the Total Power Supplied number.

Figure 1-4 Power Budget Worksheet Example #2

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Base Number ____ **Location** _____

Module Position	Module Type	Power Consumption (mA)
Slot 0		
Slot 1		
Slot 2		
Slot 3		
Slot 4		
Slot 5		
Slot 6		
Slot 7		
	PPX:S-10P Machine Interface Unit	
	Base	

Total Power Supplied is
3700 mA if a CPU/Power Supply is being used
OR
4000 mA if a PPX:405-IOEX Expansion Unit is being used

Total Power Supplied [ ]

Total Power Consumed [ ]

This module combination is valid only if the Total Power Consumed number is less than the Total Power Supplied number.

Figure 1-5 Power Budget Worksheet

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MIU Peripheral Port

The MIU has a peripheral port, shown in Figure 1-6, for connecting data recorders and serial devices. Table 1-9 lists the signals for each pin.

Table 1-8 lists the environmental and operational specifications for the PPX:S-10P Machine Interface Unit (MIU). Table 1-10 lists the specifications the CMOS, EEPROM, and UVPROM Memory Cartridges.

Table 1-8 PPX:S-10P Machine Interface Unit Specifications

Operating Temperature	0° to 60°C (32° to 140°F)
Storage Temperature	–10° to 65°C (14° to 149°F)
Humidity	20 to 90%, noncondensing
Environmental air	No corrosive gases
Vibration	MIL STD 810C 514.2
Shock Resistance	MIL STD 810C 516.2
Noise immunity	NEMA ICS3-304. Impulse 1000V 1 µs.
Dimensions	145 mm x 118 mm x 30 mm
Weight	380 g (excludes memory cartridge)
Display type	LCD
Display size	24 characters by 2 lines
Display LEDs	Run, Test, Pgm
Keypad	55 keys
Power Supply Requirements UVPROM External supply Internal power consumption Write to memory cartridge	 12.5 VDC, 6 VDC 5 VDC ±5% 200 mA + 120 mA for back-light 843 mA + 120 mA for back-light
CPU Communications Data format Data transfer rate	RS-232-C asynchronous, half-duplex, 1 start bit, 8 data bits, 1 odd parity bit, and 1 stop bit 9600 bps
Cassette Interface Baud rate Transfer time Interface requirements Frequency range Wow and flutter	 680 1 minute per K 1 microphone input; 1 earphone output 300 to 4000 Hz (minimum) < 0.5%

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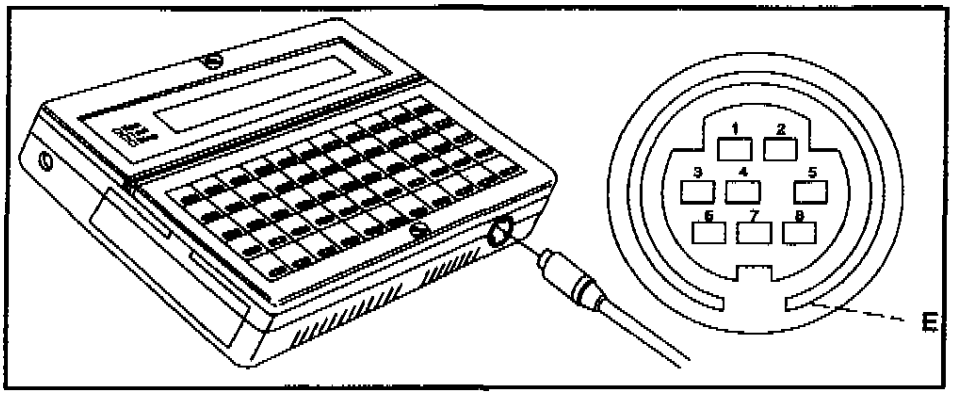


Figure 1-6 MIU Peripheral Port

Table 1-9 MIU Peripheral Port Pin Descriptions

Pin	Name	Description
1	0V	Logic Ground
2	TX0	Transmit Data (RS-232-C)
3	RX0	Receive Data (RS-232-C)
4	CSTI	Input from Cassette (5V p-p max)
5	CSTO	Output to Cassette (100 mV p-p max)
6	RDY	External Device Ready (RS-232-C)
7	—	Not used
8	—	Not used
E	0V	Logic Ground

Table 1-10 Memory Cartridge Specifications

	CMOS RAM PPX:G-03M	EEPROM PPX:G-23M	UVPROM PPX:G-14M
Memory capacity	8K words	8K words	16K words*
Backup battery	Lithium	Not required	Not required
Write-disable function	Terminal jumper	Terminal jumper	Not required
Writing life	N/A	More than 10,000 times	1,000 times
Memory deletion method	N/A	Electrically erased	Ultraviolet irradiation
Weight	42 g	60 g	60 g
Cartridge insertion frequency	More than 10,000 times for all types		

*Only 8K is usable.

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Programmer Port

The top port on the CPUs, shown in Figure 1-7, is the interface for the programming devices. The MIU connects to this port either directly by mating the connector on the back of the MIU to this port, or by the PPX:S-30JP or PPX:S-15JP cables. Table 1-11 lists the signals for each pin.

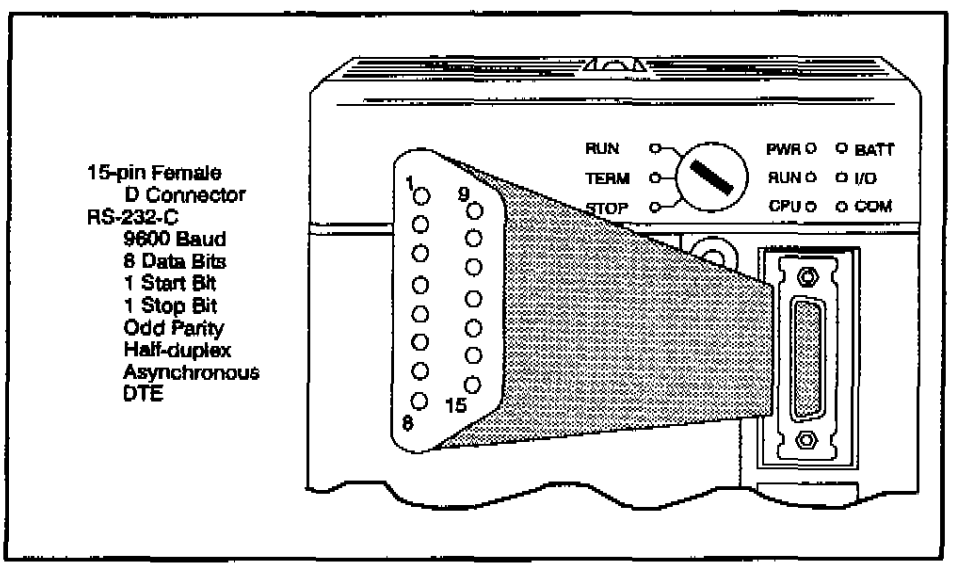


Figure 1-7 MIU Port Specifications

Table 1-11 MIU Port Pin Descriptions

Pin	Name	Description
1	YOP	Sense connection between MIU and CPU
2	TX1	Transmit Data (RS-232-C)
3	RX1	Receive Data (RS-232-C)
4	$\overline{\text{ONLINE}}$	Request Communication (TTL)
5	$\overline{\text{ABNO}}$	CPU Error (TTL)
6	$\overline{\text{PRDY}}$	CPU ready to communicate (TTL)
7	CTS	Clear To Send (RS-232-C)
8	YOM	Sense connection between MIU and CPU
9	—	Not used
10	LCBL	Sense cable connection (TTL)
11	5V2	5 VDC for MIU logic
12	5V2	5 VDC for LCD backlight
13	0V	Logic ground
14	0V	Logic ground
15	0V	Logic ground

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Serial Interface Port

The lower port on the TI430 and TI435 CPUs, shown in Figure 1-8, is a serial interface connector that operates with either RS-232-C or RS-422 signals. Table 1-15 lists the signals for each pin.

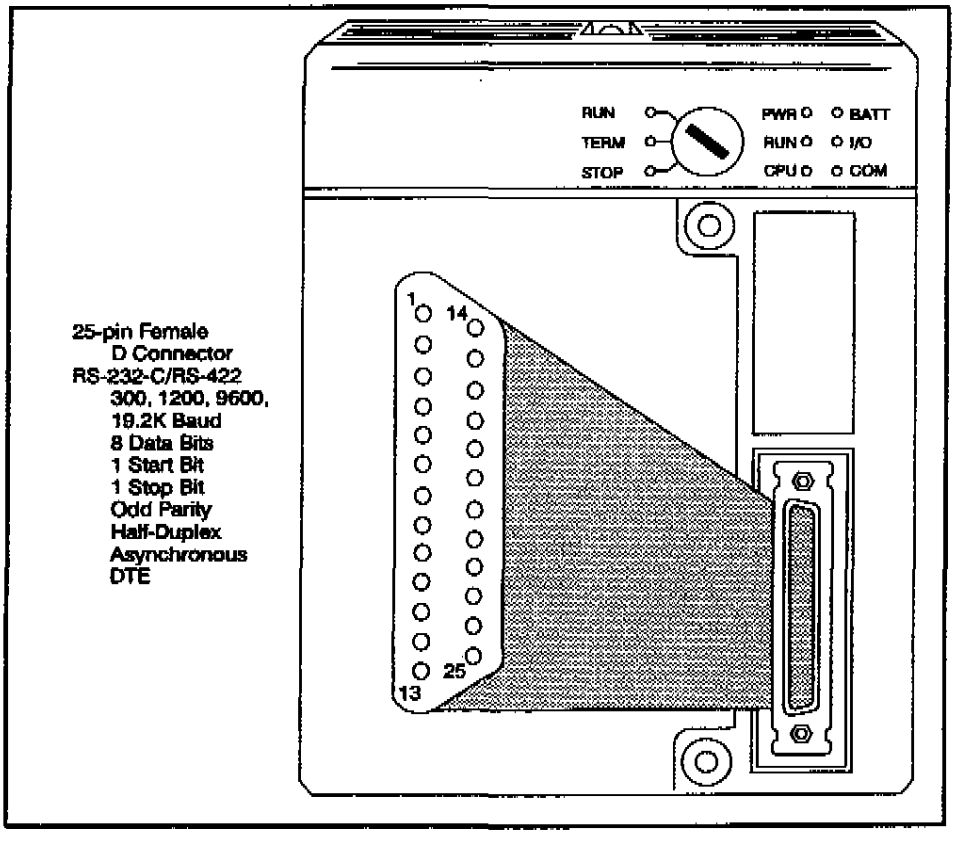


Figure 1-8 TI435 Serial Interface Port Specifications

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Table 1-12 Serial Interface Port Pin Descriptions

Pin	Name	Description
1	—	Not used
2	TXD	Transmit Data (RS-232-C)
3	RXD	Receive Data (RS-232-C)
4	RTS	Request to Send (RS-232-C)
5	CTS	Clear to Send (RS-232-C)
6	—	Not used
7	SG	Signal ground (RS-232-C/RS-422)
8	—	Not used
9	RXD+	Receive Data + (RS-422)
10	RXD–	Receive Data – (RS-422)
11	CTS+	Clear to Send + (RS-422)
12	—	Not used
13	—	Not used
14	TXD+	Transmit Data + (RS-422)
15	—	Not used
16	TXD–	Transmit Data – (RS-422)
17	—	Not used
18	RTS–	Request to Send – (RS-422)
19	RTS+	Request to Send + (RS-422)
20	—	Not used
21	—	Not used
22	—	Not used
23	CTS–	Clear to Send – (RS-422)
24	—	Not used
25	—	Not used

Table 1-13 Communication Port Specifications

Type	RS-232C/RS-422
Baud rate	300, 1200, 9600, 19.2K BPS
Data format	Hex mode or ASCII mode
Connector	25-pin D, socket
Protocol	N-sequence/K-sequence
Isolation	No
Addressing	Set to 1 or configurable from 1 to 90

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Use AUX 56 with MIU (PPX:S–10P) or AUX 26 with TISOFT to configure station address, mode, and parity.

Table 1-14 Software Selectable Station Address, Mode, and Parity Selections

Parameter	Range
Station address	1 through 90
Mode	ASCII or HEX
Parity	None or odd

CPU Protocols

Operator interface devices use one or both of the following communication protocols to communicate with TI405 CPUs. See Table 1-15.

- K-sequence – Commands CPU directly with proprietary command codes
- N-sequence (Hostlink) – Reads and writes memory using published protocol, commands CPU indirectly by writing to scratchpad memory, limited to operations which can be initiated from scratchpad memory.

Table 1-15 Protocols Used by TI405 Interface Devices

Device	Type Protocol
PPX:S–10P MIU	K
CVU 100	K
TISOFT Rel 1.0	K
TISOFT Rel 2.01	K or N
JNet 2	N

NOTE: The bottom port on the TI435 can be configured for station address (network #), Hex or ASCII mode, and odd or no parity using AUX 26 with TISOFT Release 2.01 or AUX 56 with the PPX:S–10P MIU (MIU Firmware V3.2 or greater). To enable the station address and configure baud rate, set the CPU dipswitches as shown in Chapter 2.

Protocols Supported by each Port

TI405 CPUs with firmware prior to V2.1 support K-sequence only on the top (15-pin) port, and N-sequence only on the bottom 25-pin) port (TI435 only). See Figure 1-9. V2.1 adds K-sequence to the bottom port of the TI435 so that it can now support N or K. See Figure 1-10.

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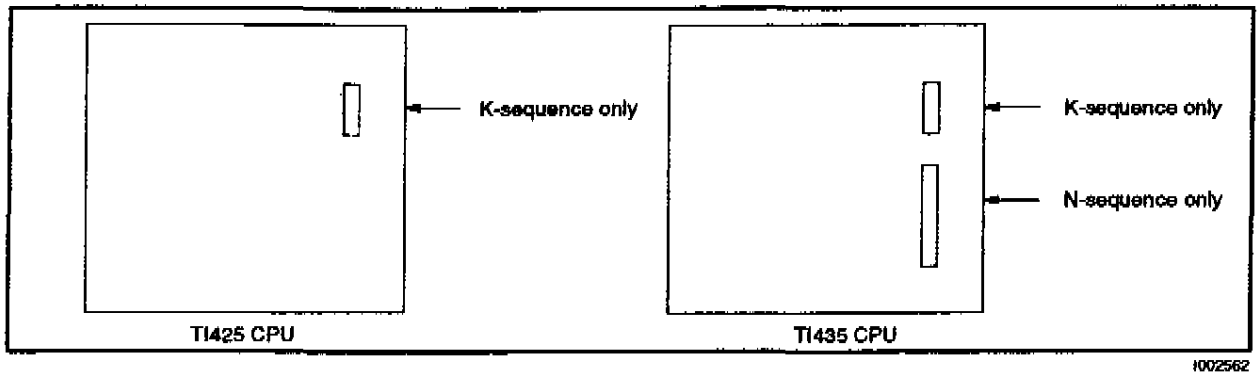


Figure 1-9 Protocols Supported Before V2.1

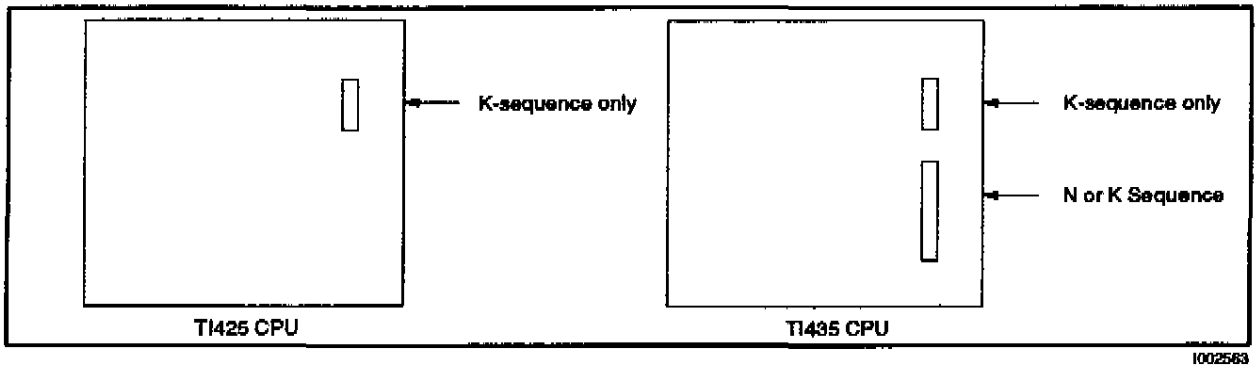


Figure 1-10 Protocols Supported by V2.1

CPU Restrictions when Using K-sequence

Because the TI435 CPU contains only one K-sequence buffer and handler, K-sequence protocol cannot be used on both TI435 CPU ports at the same time.

⚠CAUTION

Attempts to use both TI435 CPU ports with K-sequence at the same time can result in communication timeouts and incorrect data transfers.

Because the TI435 CPU contains independent buffers and handlers for N and K, no communication interference problems arise from using K on the top port and N on the bottom port at the same time.

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Using 10-bit Modems

K-sequence protocol was added to the bottom port to allow K-sequence devices to communicate through more types of MODEMs. The top port is fixed at 9600 baud, 1 start bit, 8 data bits, odd parity (1 bit), and 1 stop bit, for a total of 11 bits. Many MODEMs cannot support 11 bits, but can support 10 bits. The top port is unsuitable for these MODEMs.

The bottom port can be configured by the user to have no parity. This removes one bit and allows the use of 10-bit MODEMs. Additionally, the bottom port can be configured for 19,200 baud, resulting in faster data transfer than the 9600 baud top port.

Using TISOFT Release 2.01 in Bottom Port

TISOFT Release 1.0 for TI405 supported K-sequence protocol only and was intended for use in the top port. TISOFT Release 2.01 for TI405 added the ability to communicate with either K- or N-sequence protocol.

When invoking Release 2.01 TISOFT with TI405, TISOFT tries K-sequence first. If the CPU responds correctly with K-sequence, then TISOFT connects and begins normal online operations. If K-sequence does not work, TISOFT tries N-sequence.

This method of invoking TISOFT is generally acceptable, except when trying to use TISOFT on the bottom port of a TI435 CPU containing V2.1 firmware while the top port is in use. In this specific case, TISOFT attempts to come online with K-sequence, resulting in both ports communicating with K-sequence. As described in "CPU Restrictions When Using K-sequence", the CPU does not support both ports using K-sequence at the same time.

NOTE: TISOFT cannot use K-sequence in the bottom port if the top port is in use. TISOFT can use N-sequence in the bottom port if the top port is in use.

To instruct TISOFT to try N sequence, first, add **CA** or **CB** to the normal prompt to invoke TISOFT. **CA** looks for ASCII N-sequence first while **CB** looks for Hexadecimal (binary) N-sequence first. See Figure 1-11.

NOTE: If N-sequence is not found, K-sequence will be tried.

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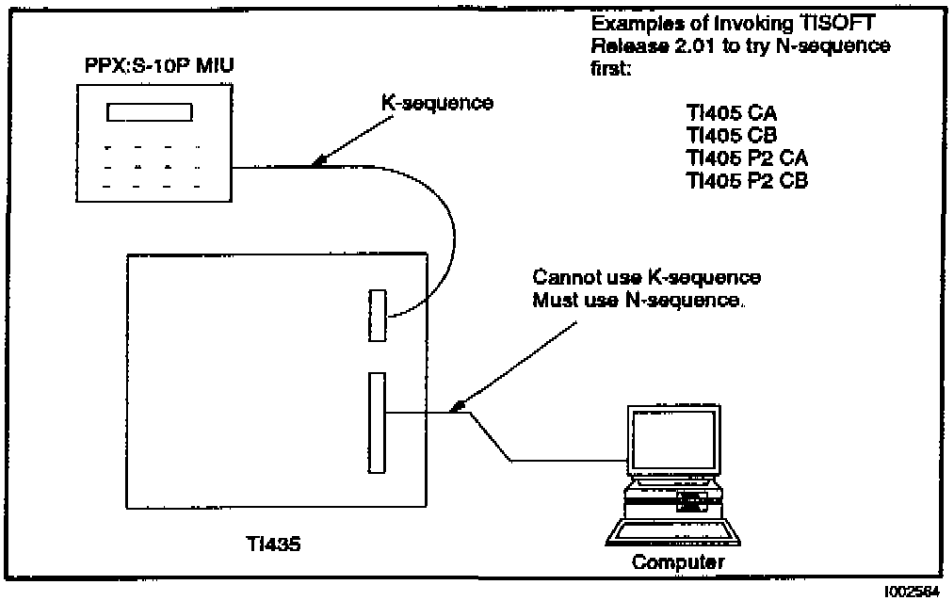


Figure 1-11 Obtaining N-sequence on TISOFT Release 2.01

Determining TISOFT Protocol

To determine which protocol TISOFT is using, perform AUX 10, Syntax Check. Press either SYNTAX-F2 or DUPLIC-F3. If the operation succeeds, then TISOFT is communicating with K-sequence. If the error message, **COMMUNICATIONS ERROR – BAD PROTOCOL SELECTION** is received, then TISOFT is communicating with N-sequence.

TISOFT Restrictions

The following restrictions apply to TI405 TISOFT.

- N-sequence is an option on TISOFT Release 2.01 for TI405, but is not available on TISOFT Release 1.0.
- The following TISOFT Release 2.01 operations are not available when N-sequence protocol is used:

  AUX 10 Syntax Check

  STATUS/CHART CHGVAL (change value) except for V-memory

  Constant Editor in STATUS/CHART CHGVAL

- Because TISOFT STATUS and CHART use CPU memory to define which data to read, only 1 TISOFT for each TI405 CPU can monitor status or chart at a time. This is true regardless of which communication protocol is used (N or K).

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⚠CAUTION

Attempts to view status and/or charts with more than one TISOFT for each TI405 CPU can result in incorrect data on the TISOFT screens. However, the actual memory in the CPU is not adversely affected by this condition.

Subroutine or FOR/NEXT Loop in Stage (TI435 Only)

In previous TI435 CPU releases, OUT and TMR instructions contained in subroutines or FOR/NEXT Loops did not operate properly in Stage programs. If the stage containing the GTS or FOR/NEXT instructions becomes inactive, the OUT instructions remain on, and timers are not reset.

Solution: TI435 CPU V2.1 corrects this problem; OUTs are turned off and timers are reset.

UVPROM Cartridge with TI435

In previous TI435 CPU releases, the UVPROM cartridge (PPX:G–14M) would reference only the default memory assignments for retentive ranges and system parameters.

Solution: Release 2.1 TI435 CPU firmware corrects this problem. For further information on problem, see Technical Advisory PPX:405–004.

TI425 with HSC

TI425 Version 1.6 firmware failed to report the number of points in I/O configuration for the PPX:U–01Z High-Speed Counter (HSC) module.

Solution: This problem was corrected to report 16 input and 32 output points for the HSC.

SP53 with FIND Instruction

In previous firmware releases, error indicator SP53 was not reset immediately prior to the FIND instruction (TI435 only). If SP53 was on prior to a FIND instruction, it would remain on after the FIND instruction, even if no error was encountered.

Solution: This problem was corrected so that SP53 is reset before executing the FIND instruction.

Serial Port on TI435

The 25-pin serial port on the TI435 continues to be a slave port only.

Solution: The serial port was modified to function more like the PPX:U–01DM Data Communication Module (DCM). Also, the serial port now supports data type 39, network status.

MOVMC Instruction

In previous, firmware releases, executing the MOVMC (TI435 only) instruction would occasionally result in a CPU fatal error.

Solution: This and other problems with the MOVMC instruction were corrected.

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2.1 Safety Guidelines

This chapter presents recommended installation practices and procedures. Since no two applications are identical, these recommendations should be considered as guidelines.

⚠WARNING

Control devices can fail in an unsafe condition. This means that, unless proper safeguards are incorporated by the user, certain malfunctions of these devices could lead to a sudden equipment start-up. Such a start-up could result in property damage and/or severe physical injury to the equipment operator.

If you, or your company, use any programmable controllers with equipment which requires an operator or attendant, you should be aware that this potential safety hazard exists and take appropriate precautions. Although the specific design steps depend on your particular application, the following precautions generally apply to installation of solid-state programmable control devices.

In addition, these precautions conform to the guidelines for installation of Programmable Controllers as recommended in the NEMA ICS 3-304 Programmable Control Standards.

ICS 3-304.81 Safety Recommendations:

Consideration should be given to the use of an emergency stop function which is independent of the programmable controller.

Where the operator is exposed to the machinery, such as in loading or unloading a machine tool, or where the machine cycles automatically, consideration should be given to the use of an electromechanical override or other redundant means, independent of the programmable controller, for starting and interrupting the cycle.

If provision is required for changing programs while the equipment is in operation, consideration should be given to the use of locks or other means of assuring that such changes can be made only by authorized personnel.

*These recommendations are intended as safeguards against the failure of critical components and the effects of such failures or the inadvertent errors that might be introduced if programs are changed while the equipment is in operation.**

* The ICS 3-304.81 Safety Recommendations are reproduced by permission of the National Electrical Manufacturers Association from NEMA ICS 3-304, Programmable Controller Standard.

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2.2 Safety Considerations

Pre-installation planning and site preparation must include consideration of hazards to personnel during a system failure. The equipment connected to the TI425/TI435 PLC should include interlocks and safety switches to prevent operation during a system failure. Although the specific steps depend on the application, the general precautions include the following topics.

Disconnecting Power

Provide a means for disconnecting power—independent of the PLC—from the output loads when a machine is not operating, or when it is necessary for the operator to reach into the machine. Power must be removed by a non-semiconductor switch or a physically-wired relay contact, placed to interrupt power to the output. It is not sufficient to rely solely on the PLC for this function. Figure 2-1 illustrates an operator safety switch.

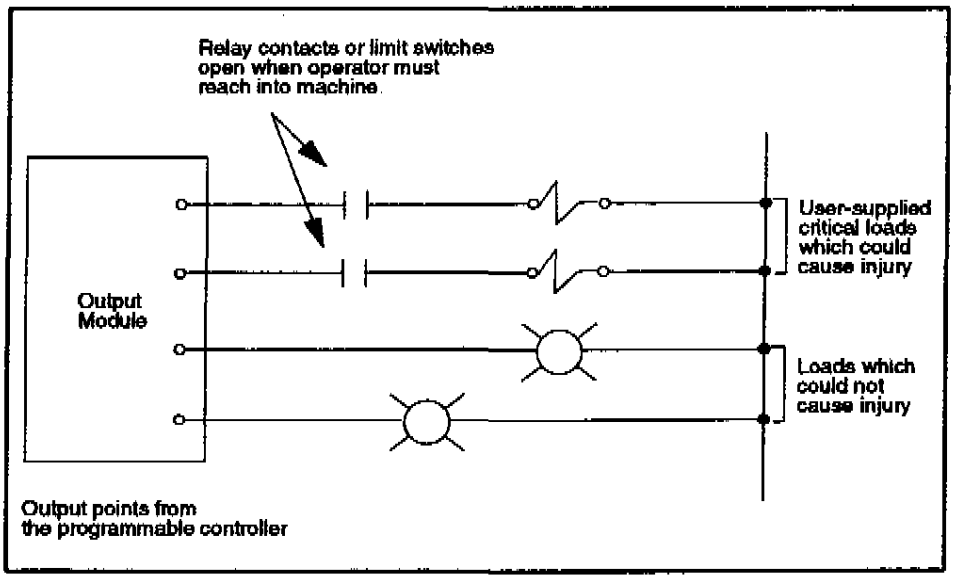


Figure 2-1 Operator Safety Switch

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Disconnecting Power for Emergency Conditions

Provide a means for removing power from the output if an emergency condition occurs during operation. Do this by disconnecting output power with a non-semiconductor switch or hardwired relay contact, not through the programmable control system. This type of switch is shown in Figure 2-2.

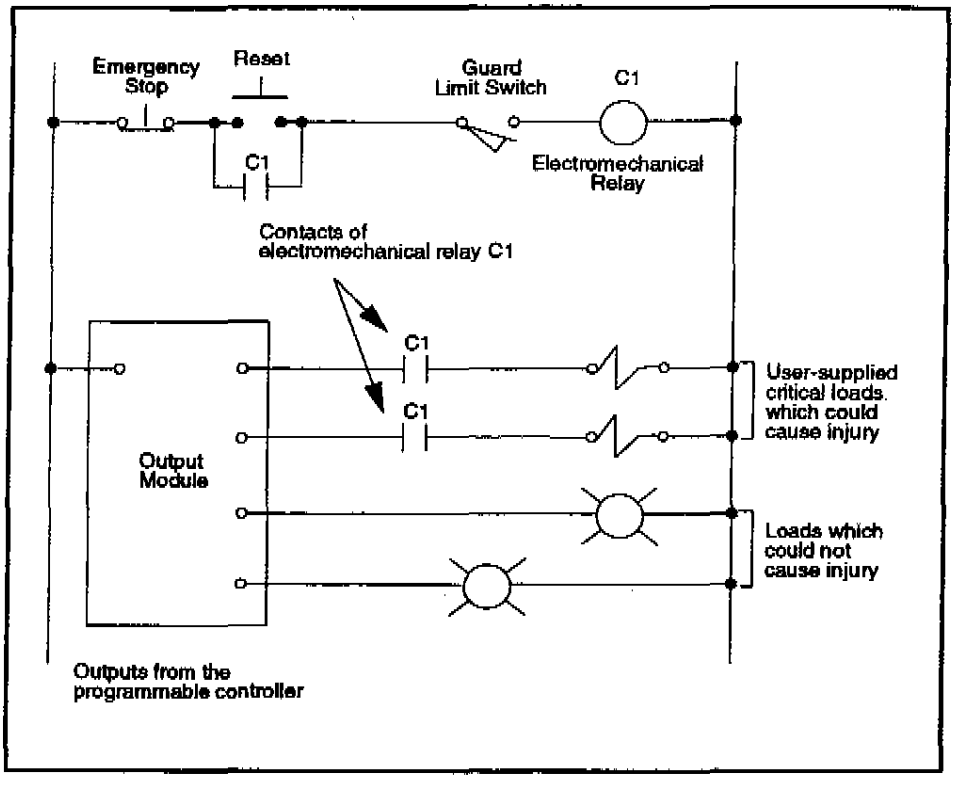


Figure 2-2 Emergency Stop Switch

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Bypassing PLC for Machine Loading

Bypass the programmable control system with an external JOG or INCH switch during machine loading or setup operations. See Figure 2-3.

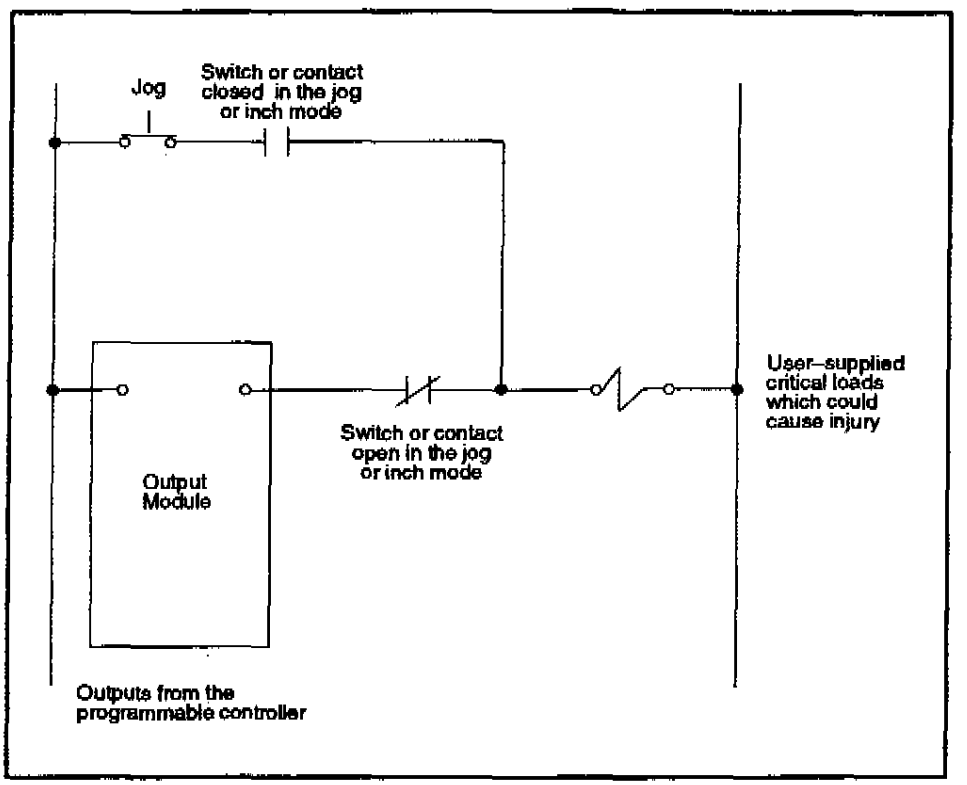


Figure 2-3 JOG or INCH Switch

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Enclosure Selection

As a minimum, an enclosure for a TI425/TI435 should provide the following:

- Easy access to components.
- A common ground potential on the cabinet.
- A secure vertical panel or rails.
- Conformance to electrical standards.
- An electromagnetic shield.
- Access restricted to authorized personnel only.
- Protection from dust and dirt in an industrial environment.

Mount the TI425/TI435 components in a suitable enclosure for your environment. If the components are in a severe environment, you should consider the use of a dustproof and drip tight enclosure such as a NEMA Type 5 enclosure. The enclosure must provide a minimum depth of 12.7 cm (5 in) from the panel to the inside surface of the enclosure door. A minimum of 15.3 cm (6 in) is required if the MIU is to be left attached to the CPU when the door is closed. The enclosure should be located so that the doors may be opened fully, permitting easy access to the PLC, wiring, and components. If environmental conditions permit, a 19-inch rack may be used instead of a NEMA enclosure.

Temperature Considerations

When preparing your installation, plan for an adequate air flow to ensure proper cooling of equipment. Do not permit the convective cooling of the PLC to be hindered. Mount the PLC in an upright position, so that cooling vents are at the top and bottom of the device rather than on the sides. This permits the maximum convective air flow around the modules.

House the PLCs in a cabinet having enough clearance to prevent the accumulation of hot air. Unless ambient temperatures are extremely high, a fan or air-conditioned cooling is unnecessary to keep TI425/TI435 PLCs below their maximum-rated operating temperature of 60°C, measured above the modules inside the enclosure.

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2.3 Grounding

Grounding the Equipment

A good grounding system is essential for proper operation of a TI425/TI435 system and should be one of the most important considerations in planning your installation.

The structural ground present in many industrial environments does not provide an adequate ground return where direct wire connection is not feasible. This section is a discussion of grounding, electromagnetic interference (EMI), and other electrical considerations. Follow the guidelines to be certain to meet all wiring requirements.

As a minimum, use #12 AWG stranded copper wire for the ground return. Minimum wire sizes, color coding, and general safety practices should comply with all appropriate electrical standards and codes. Screw connections between enclosures and bases provide grounds and should be tightened properly.

Single-Point Grounding

Connect any TI405 component with an external chassis or external ground terminal on its power connectors to the subpanel ground bus. This connection should exhibit very low DC resistance (0.05 ohm) and low high-frequency impedance.

Connect the sub-panel ground bus to a single-point ground, such as a copper bus bar to a good earth ground reference. The single point ought to be the center of a "star" configuration to minimize device-to-ground distances.

To achieve low impedance from device to single-point termination, 0.65 centimeter or larger ground braid should be used. A good rule of thumb is to require less than 0.1 ohm of DC resistance between device and single-point ground. This is accomplished by removing the anodized finish and using copper lugs and star washers.

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Guidelines for Ground Connections

Use particular care when establishing the ground connections. The following techniques establish good electrical connections and increase system noise immunity.

- Terminate grounding braid and green wires at both ends with copper eye lugs to provide a good contact surface. Lugs should be crimped and soldered.
- Use #10 copper bolts (or equivalent) for those fasteners providing electrical connections to the single-point ground. This applies to device-mounting bolts and braid termination bolts for subpanel and user-supplied single points. Tapped holes for these fasteners are better than nut-bolt arrangements.
- Paints, coatings, and corrosion can prevent good electrical contact at ground points. Remove these impediments in the area of contact and use external toothed lock washers (star washers) to ensure good continuity and low impedance. This practice should be used for all terminations—lug to subpanel, device to lug, device to subpanel, subpanel to conduit, etc. Examples of ground connections are shown in Figure 2-4.

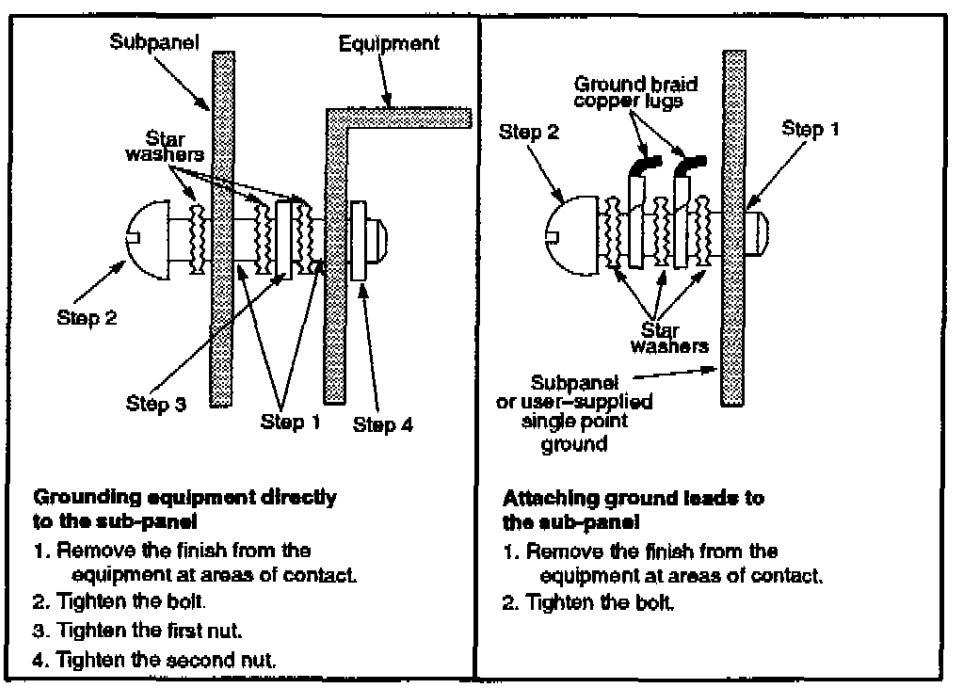


Figure 2-4 Sample Ground Connections

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2.4 Wiring Guidelines

Consider the following guidelines before installing any system or power wiring.

- Always use the shortest possible cable.
- Use a single length of cable between components.
- Do not connect short pieces of cable to obtain additional length.
- Avoid placing system and field wiring in the vicinity of high-energy wiring.
- Keep field input wiring, output wiring, and all other types of wiring in the panel physically separated.
- Consider separating DC field wiring from AC field wiring wherever possible.
- Avoid sharp bends to power and data cables. Use 7.6 cm (3 inch) radius on all bends.
- A good low ground impedance of 0.1 ohm or less must exist for all components in the system.
- Use wireways for wire and cable routing when possible.
- Keep wire strippings from falling into modules, controllers, or bases.
- For long return lines to the power supply, do not use the same wire for input and output modules. Using separate return wiring for these modules minimizes the voltage drop on the return lines of the input connections.

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2.5 Avoiding Electrical Noise

Definition and Source

Electrical noise is defined as any unwanted electrical signal that enters the control equipment. Noise signals cover the entire spectrum of frequencies and may have any wave shape. The largest single difficulty with noise is that it is not always present. Continuous, or frequent, periodic noises generally are easy to detect and remedy. Intermittent noise sources that produce short, high-energy bursts at irregular and widely spaced intervals cause the majority of difficulties.

Noise has a number of different pathways into control equipment. It can be conducted through signal or power wiring or can be radiated by electromagnetic waves. Conducted noise typically is coupled with the signal or power wiring, either electrostatically or magnetically. Electrostatic coupling occurs through parasitic capacitance between the noisy line and the signal/power line. This requires high voltage or high rate of change of voltages in the noisy line and high parasitic capacitance between lines. This typically is the case for long wire runs in the same conduit.

Magnetic coupling occurs through parasitic mutual inductances between lines. This requires high currents or high rates of change of current, as well as significant mutual inductance, which may result from proximity of wiring.

Electromagnetically radiated noise typically is high frequency (radio waves). The control system and its wiring may act as antennas in picking up noise signals. This pathway is least likely to present problem levels of noise, but its sources are common in industrial applications.

The primary sources of noise in industry are those devices (and their wiring) that produce and switch high voltage and current. Typical examples include large motors, welders and contactors that switch heavily inductive loads such as brakes or clutches.

Handling Noise Problems

When potential noise sources are identified, two general methods are available to handle them. These methods are noise suppression and noise isolation.

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Noise Suppression

You can use noise suppression (snubbing) to reduce noise at its source. Applicable only to devices driven by mechanical contacts, snubbing suppresses arcing at electrical contacts caused by turnoff of inductive loads (e.g., relays, motors, motor starters, solenoids). Load side suppression reduces voltage transients at the load, preventing them from traveling back to the contacts where they would produce a showering arc and couple with adjacent wiring.

You may achieve an alternative type of suppression by placing an RC or varistor circuit (shown in Figure 2-5) across the contacts, parallel to the switch.

Both types of snubbing cause the physical devices to come on or go off more slowly. The RC and varistor elements should have minimal effect on system timing: their time constants are substantially less than 1 millisecond.

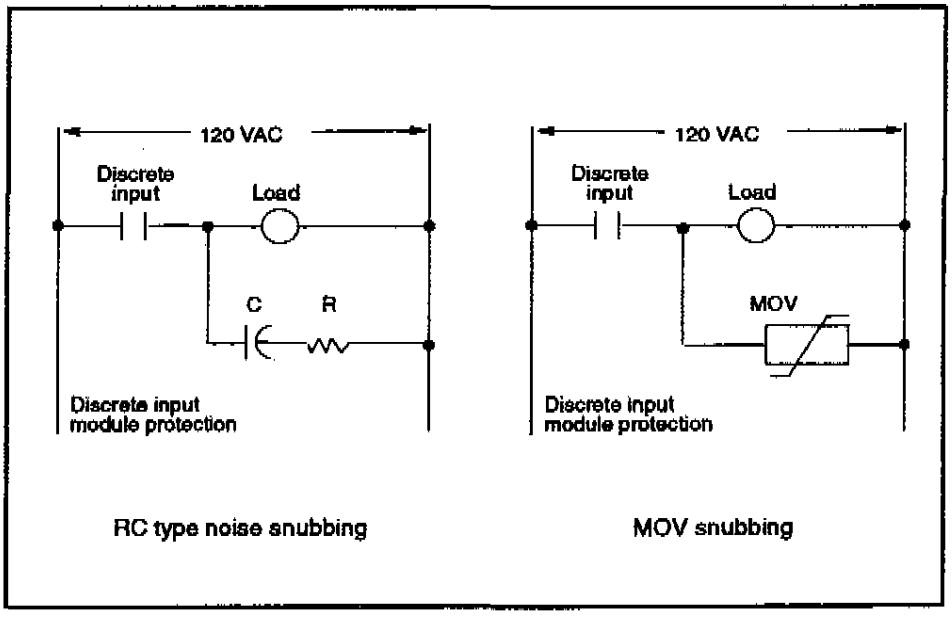


Figure 2-5 Examples of Noise Snubbing

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Isolation

The second approach to reducing noise is to isolate the problem device and its wiring from the electronics and associated signal wiring. You may accomplish this by increasing the physical distance from some types of noisy devices. For extreme cases, electrostatic (metal) shielding may be required. This is true for noise sources outside as well as inside the mounting cabinet (NEMA-type recommended).

Two cases of field wiring warrant special attention:

- Wiring that enters the harsh noise area to enable monitoring and control of those devices, and
- TTL or low-level (less than 24 V) wiring.

In these cases, supplement the physical separation between control and noise-prone wiring with shielded, twisted-pair wiring (12 twists/ft) for the control signals.

Ground the shield at the electronics side only to the single-point ground.

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2.6 Base Installation

Base Configuration Rules

Use the following guidelines for connecting expansion bases in a daisy-chain group.

- Up to four bases can be connected in series.
- Bases are connected using either a PPX:U-10J 1.0 meter (3 ft) expansion cable or a PPX:U-05J 0.5 meter (1.5 ft) expansion cable.
- The cable coming from the preceding base plugs into the top expansion connector as shown in Figure 2-6.
- The cable going to the following base plugs into the bottom expansion connector as shown in Figure 2-6.
- TI405 can support up to 320 input points and 320 output points, but when using 16-point modules, the maximum number of I/O points is
  16 points per module x 8 modules per base x 4 bases = 512 points
- If only eight point modules are used, the maximum number of I/O is 8 points per module x 8 modules per base x 4 bases = 256 points
- 8 and 16 point discrete modules may be mixed *in any order* on the base.
- On any base, the maximum number of I/O modules is determined by the total power consumption of the modules used. Figure 1-5 is a chart that you can copy and use to calculate the power consumption for a proposed base configuration.

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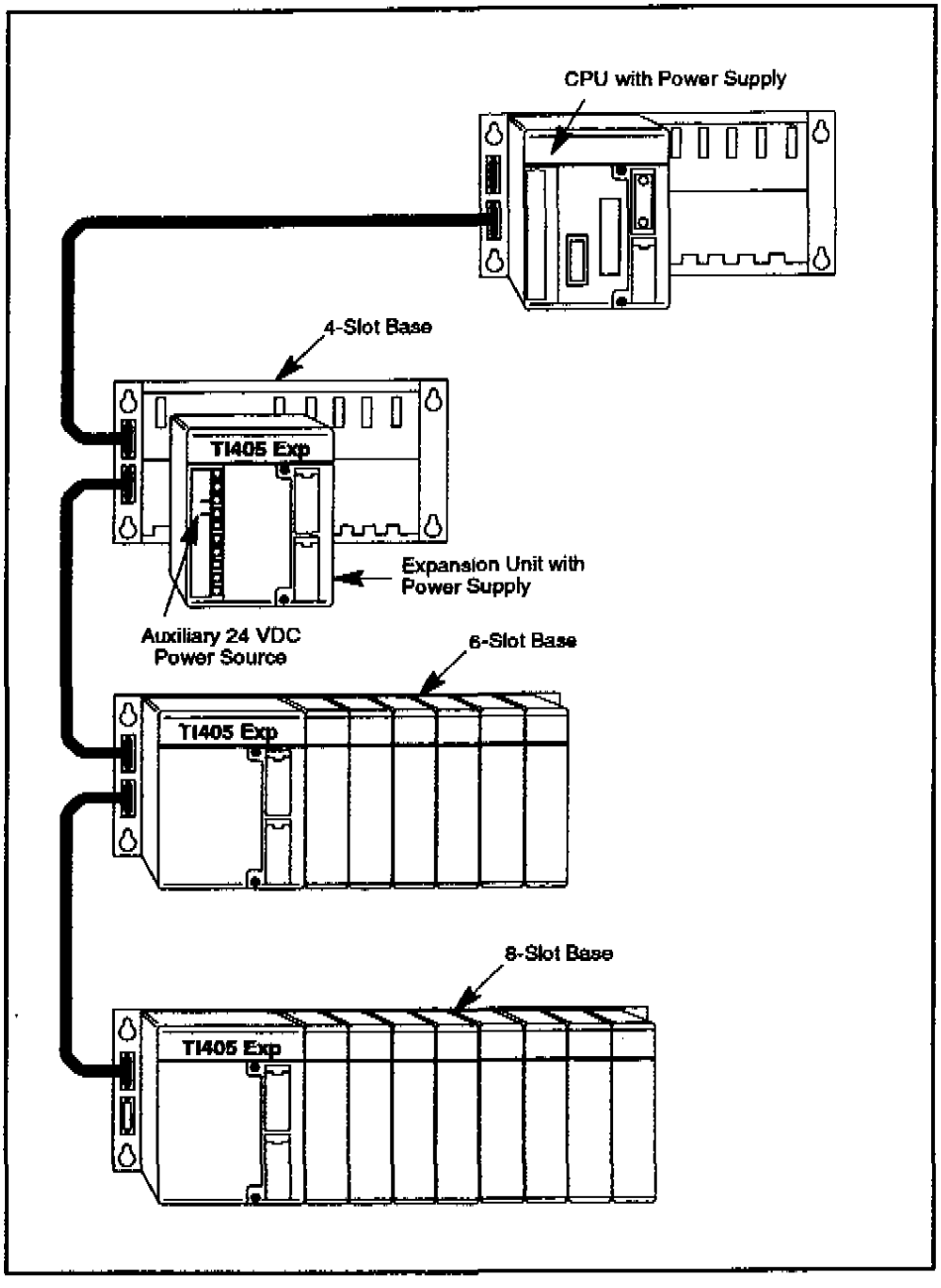


Figure 2-6 Base Configuration Example

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Base Mounting Dimensions

All dimensions in the following base diagrams are specified in millimeters.

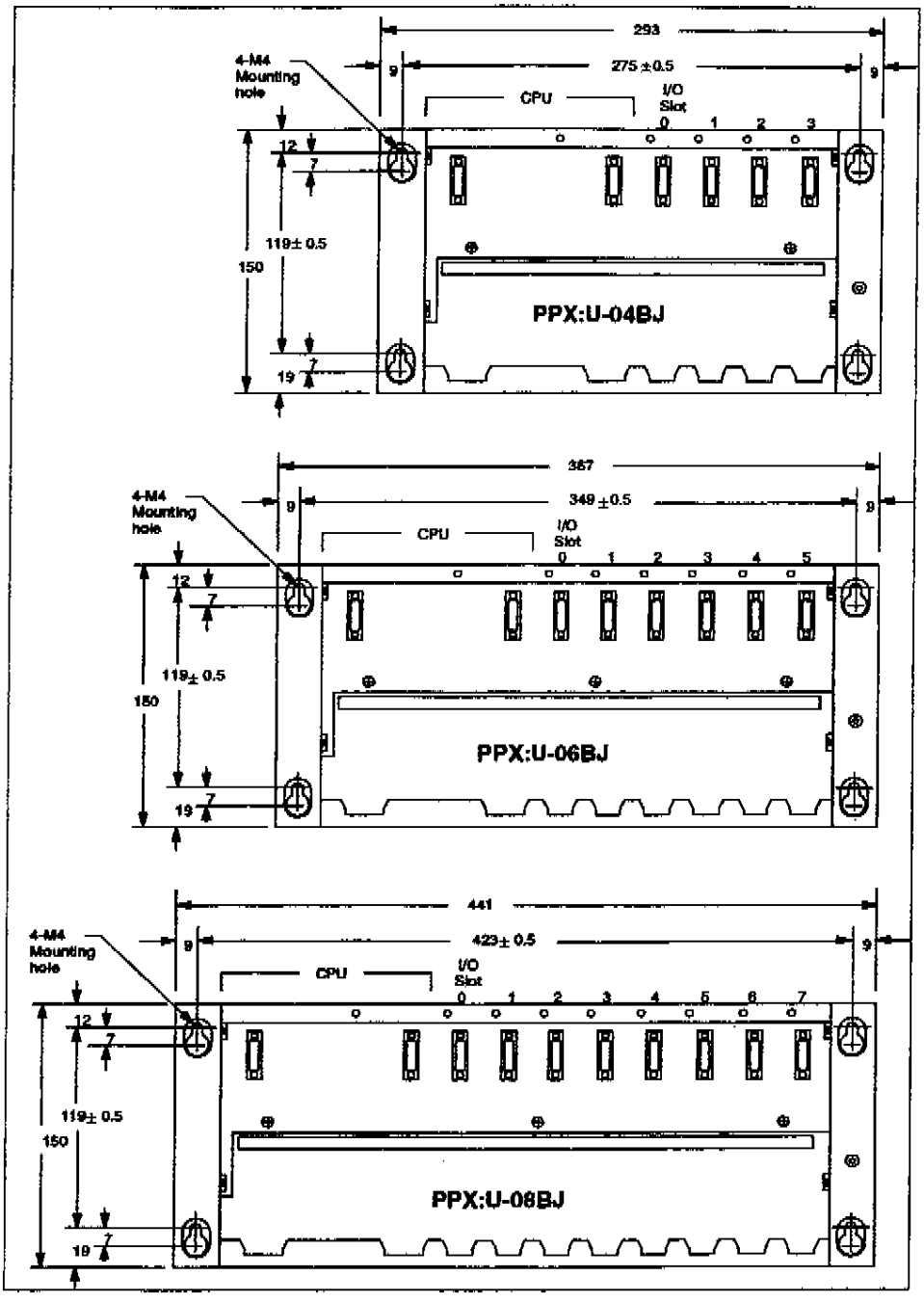


Figure 2-7 Base Mounting Dimensions

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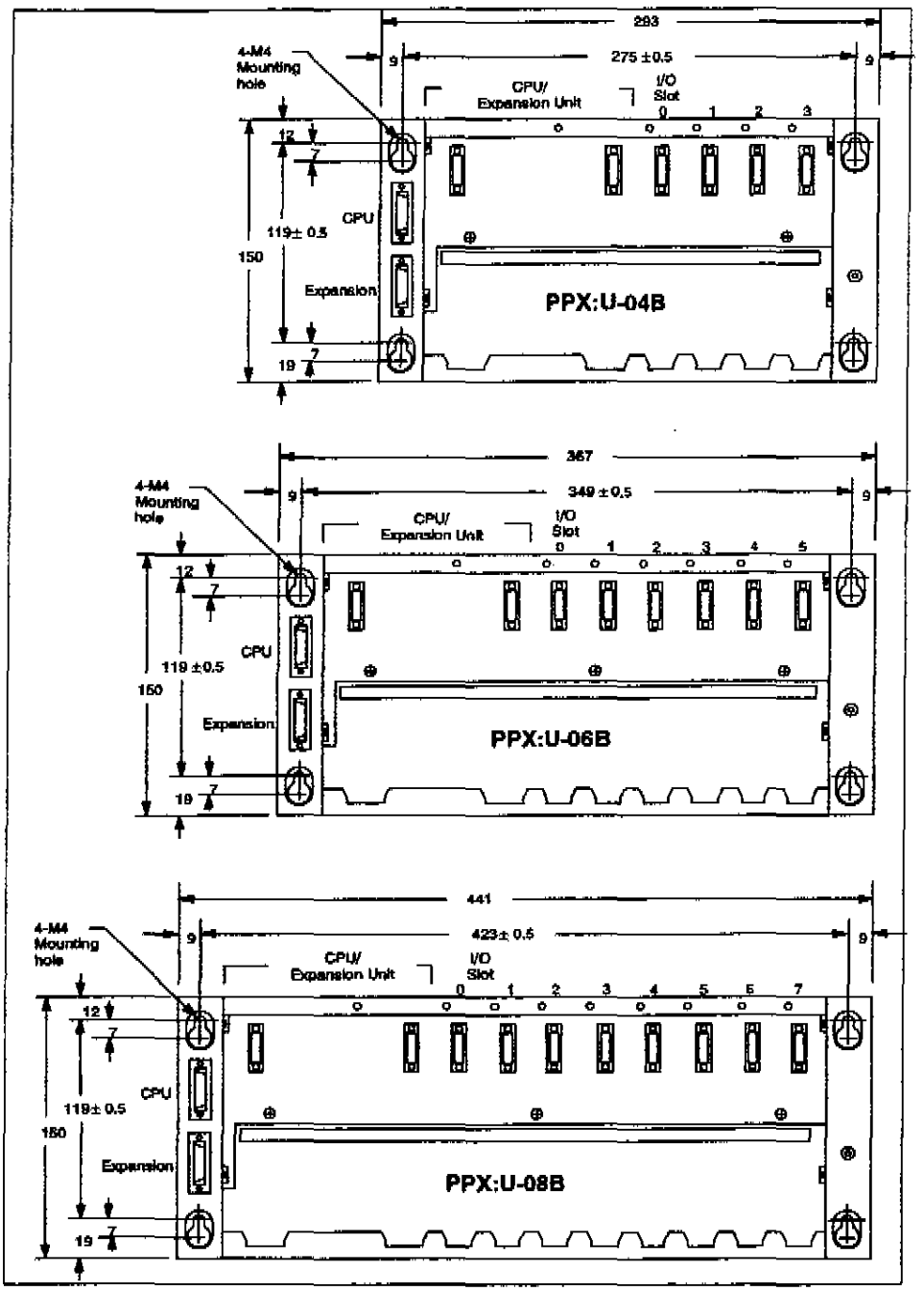


Figure 2-8 Expansion Base Mounting Dimensions

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2.7 Setting the CPU Dipswitch

Table 2-1 summarizes the dipswitch settings for the CPU dipswitch located in the rear of the CPU as shown in Figure 2-9.

Table 2-1 CPU Dipswitch Settings

Switch	Selection	
SW1	On—CPU battery disabled	Off—CPU battery enabled
SW2	On—Station address is 1	Off—Station address set via MIU
SW3	Baud rate selection for the general purpose port	
SW4	Baud rate selection for the general purpose port	

Selecting the CPU Battery Backup

The dipswitch block is located at the rear of the CPU as shown in Figure 2-9. When SW1 is Off, the CPU backup battery is enabled. This backup battery maintains the contents of the system parameters when the external power is turned off. On the TI425, the backup battery also maintains the contents of the CPU program.

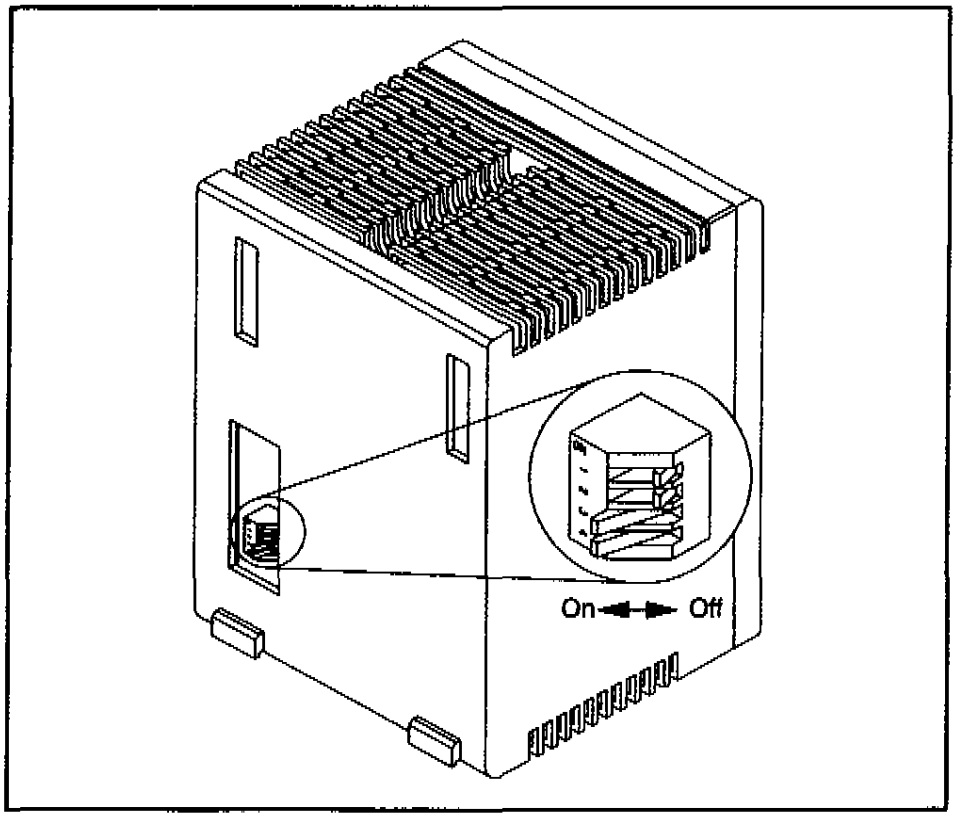


Figure 2-9 CPU Dipswitch

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Selecting the Network Address Default

SW2 on the dipswitch shown in Figure 2-9, controls the default network address used on the serial interface port of the TI435 and the TI430. The TI425 does not use this switch. When SW2 is On, the CPU defaults to address "1". When SW2 is Off, the address is set with the MIU.

Selecting the Serial Port Baud Rate

SW3 and SW4 on the dipswitch, shown in Figure 2-9, control the baud rate at which the serial interface port operates. Table 2-2 lists the baud rates corresponding to the settings of SW3 and SW4.

Table 2-2 Serial Interface Port Baud Rates

Baud	SW3	SW4
300	Off	Off
1200	Off	On
9600	On	Off
19200	On	On

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Installing the CPU and Expansion Unit

Insert the CPU or Expansion Unit into leftmost slots of the base, as shown in Figure 2-10.

1. Tilt the top of the CPU or Expansion Unit forward so that you can hook the tabs at the bottom rear into the slots at the bottom of the base frame.
2. Push the CPU or Expansion Unit toward the base until it is securely seated.
3. Tighten the securing screw.

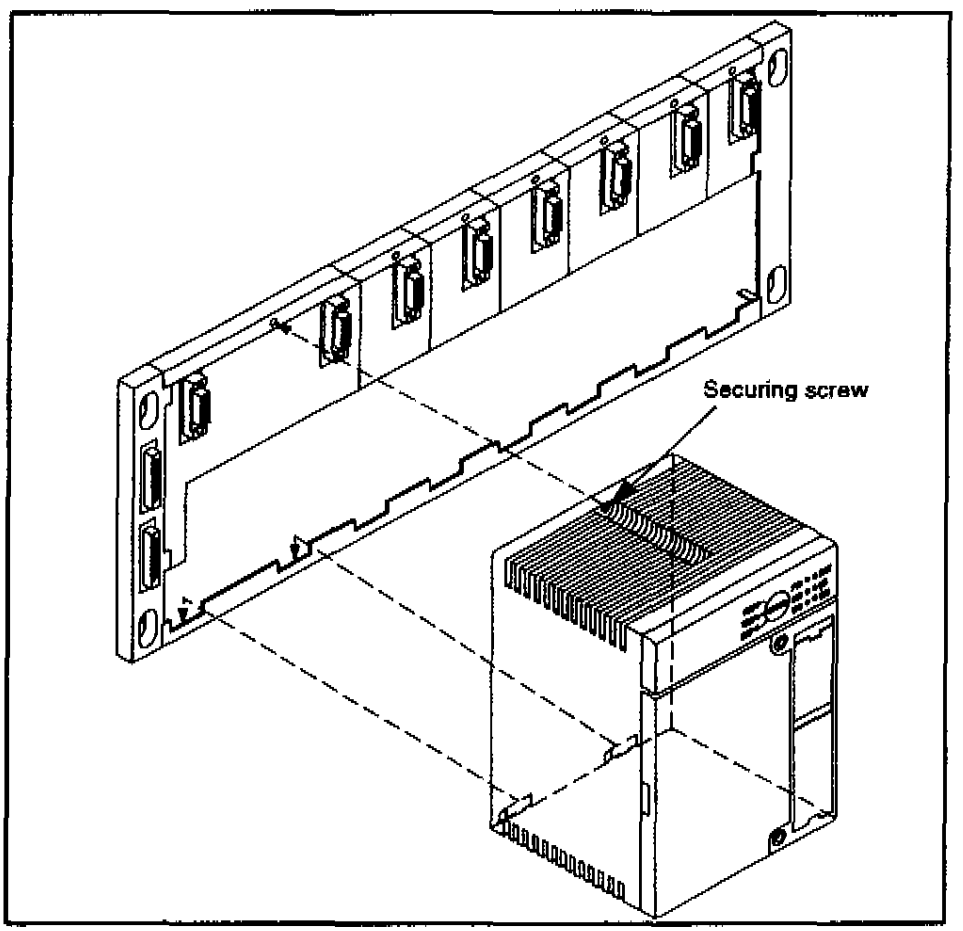


Figure 2-10 Inserting the CPU

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Connecting the Line Power Wiring

Remove the large front panel on the left half of the CPU or Expansion Unit module. Insure that line power is off, then connect line voltage supply wires to terminals 6, 7, and 8, as shown in Figure 2-11.

Connect or remove the shorting bar for either 110 VAC or 220 VAC line supply voltage as discussed in the rest of this section. Finally, replace the large front panel to cover the line wiring.

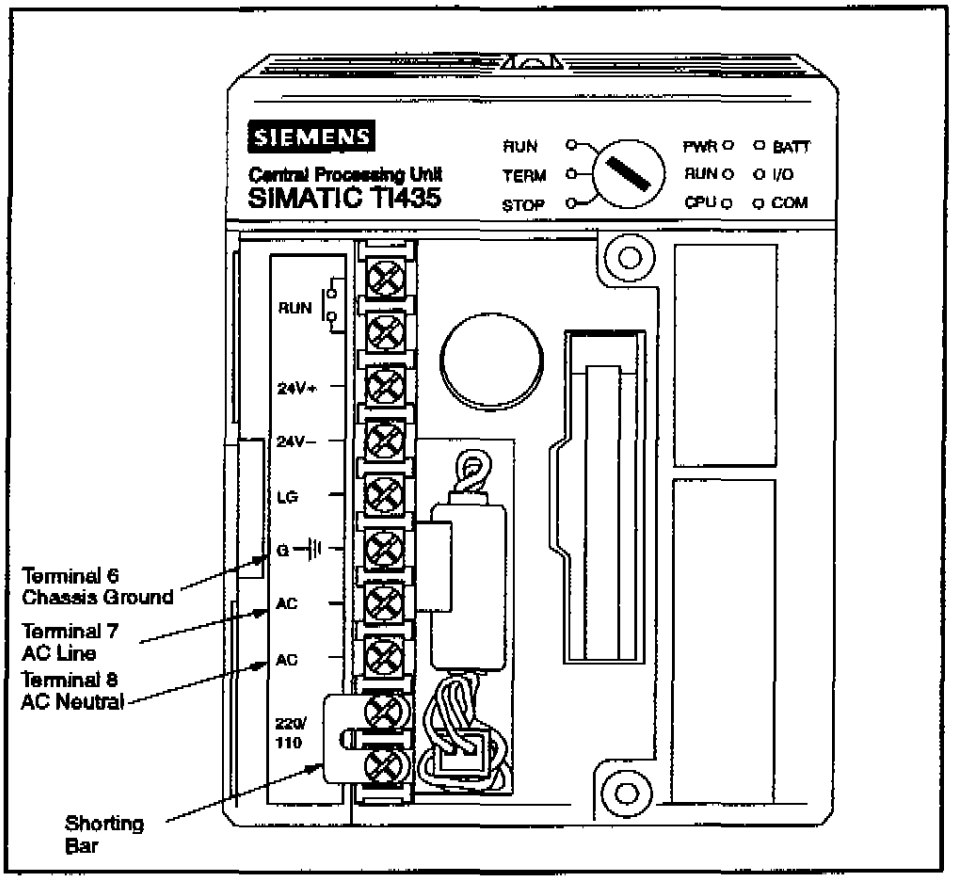


Figure 2-11 Connecting the CPU Line Power Wiring

⚠WARNING

To minimize risk of potential shock hazard and injury, be sure the unit is properly installed in an enclosure to minimize access to electrically live terminals. Only persons knowledgeable in the safe use of high voltage should perform this operation.

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Selecting 110 VAC Supply Voltage

To operate your CPU or Expansion Unit from a 110 VAC supply voltage, install the shorting bar in place as shown in Figure 2-12.

Selecting 220 VAC Supply Voltage

To operate your CPU or Expansion Unit from a 220 VAC supply voltage, do not install the shorting bar. See Figure 2-12.

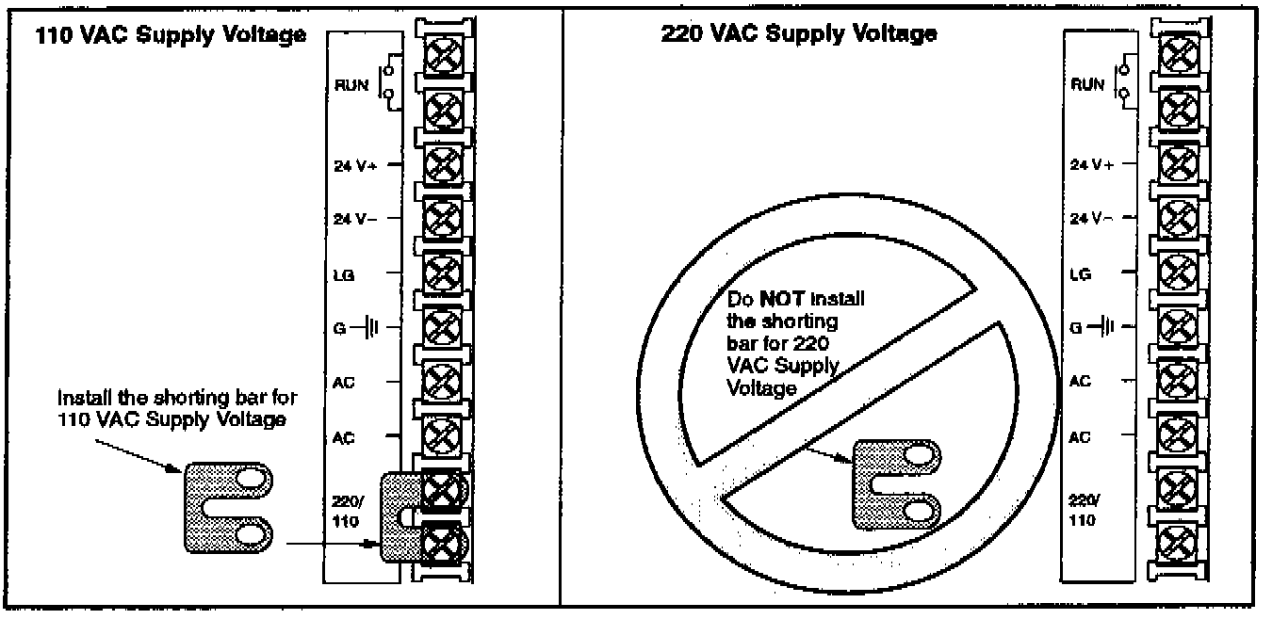


Figure 2-12 Selecting 110 or 220 VAC Supply Voltage

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The PPX:435DC-CPU does not require the shorting bar as discussed in this chapter. Insure that the DC line power is off and connect the chassis ground and DC line supply wires to terminals 6, 7, and 8 as shown in Figure 2-13.

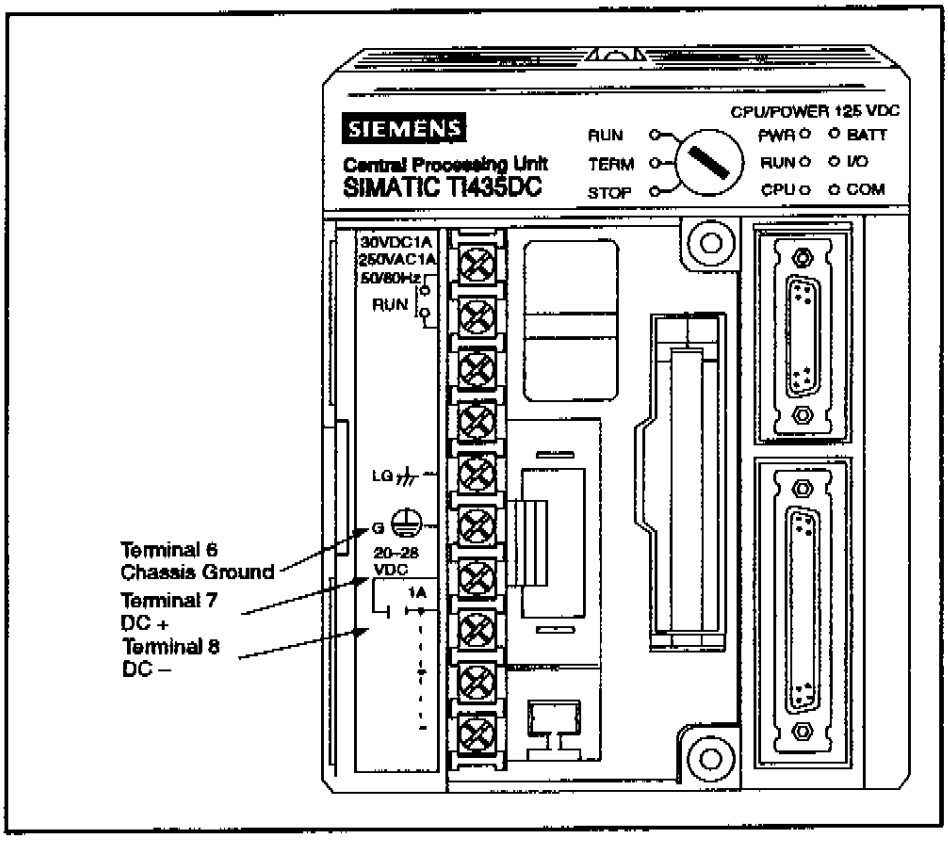


Figure 2-13 TI405 (PPX:435DC–CPU)

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The PPX:435DC1-CPU does not require the shorting bar as discussed in this chapter. Insure that the DC line power is off and connect the chassis ground and DC line supply wires to terminals 6, 7, and 8 as shown in Figure 2-14.

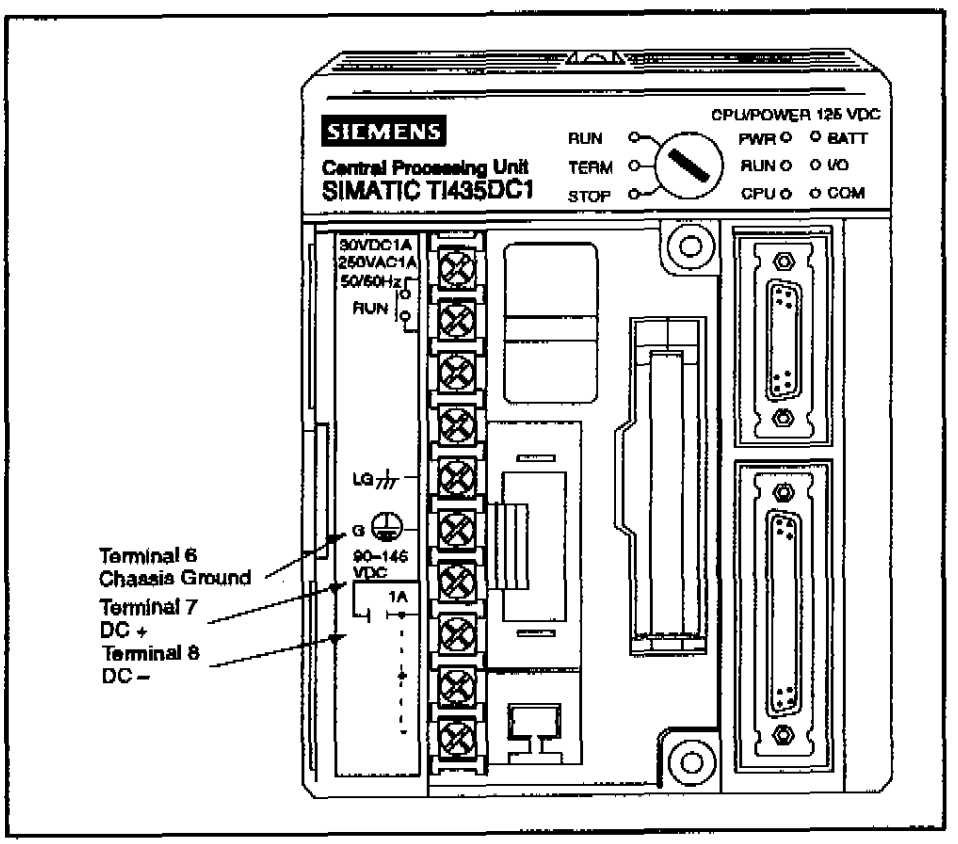


Figure 2-14 TI405 (PPX:435DC1–CPU)

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Inserting the I/O Modules in the Base

Insert the Input and Output modules into the base, as shown in Figure 2-15.

1. Tilt these modules and hook their rear tab into the base in a similar manner as the CPU.
2. Push the modules toward the base to seat them securely.
3. Tighten the securing screw.

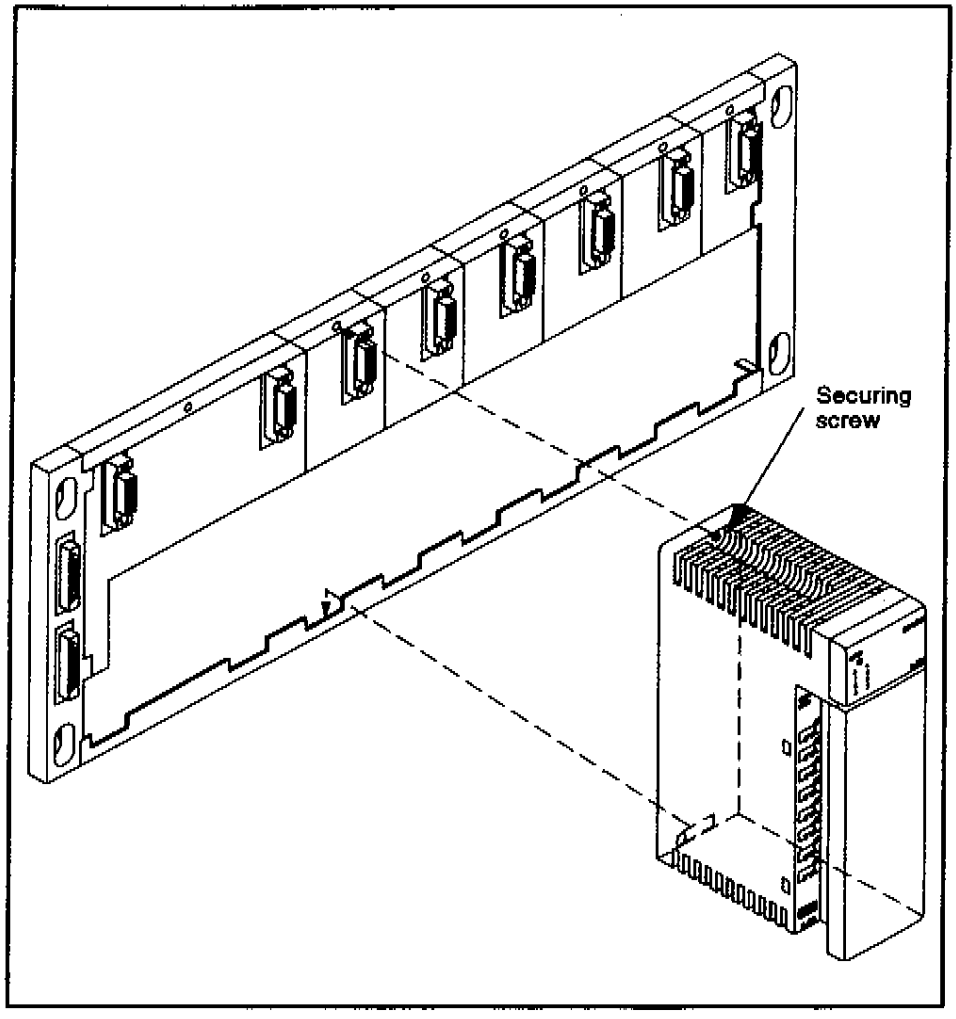


Figure 2-15 Inserting the I/O Modules

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Wiring the I/O Modules

The TI405 I/O modules feature a removable terminal block to make wiring easier. As illustrated in Figure 2-16, to remove the terminal block:

1. Remove the I/O module cover.
2. Loosen the terminal block retaining screws.
3. Pull the terminal block away from the module.

The actual wiring terminal functions for each I/O module are listed in Section 2.14.

To reinstall the terminal block:

1. Insert the terminal block onto the I/O module edge card connector.
2. Tighten the retaining screws.
3. Replace the I/O module cover.

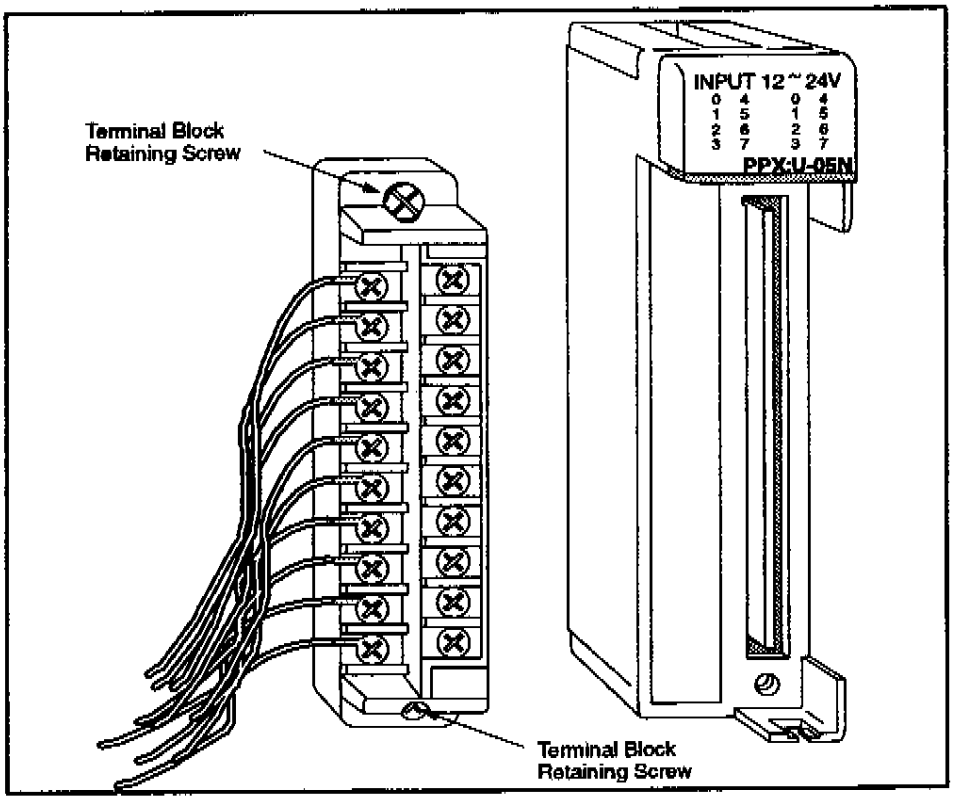


Figure 2-16 Removing the Terminal Block

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2.10 Installing the MIU

Connecting the MIU to the CPU

You can connect the Machine Interface Unit (MIU) to the CPU either directly as shown in Figure 2-17 or with the PPX:S-30JP or PPX:S-15JP cables as shown in Figure 2-18.

1. Remove the connector cover on the upper right hand side of the CPU.
2. Attach the MIU directly to the front of the CPU by mating the 15-pin connectors, or attach the connecting cable between the MIU and the CPU.

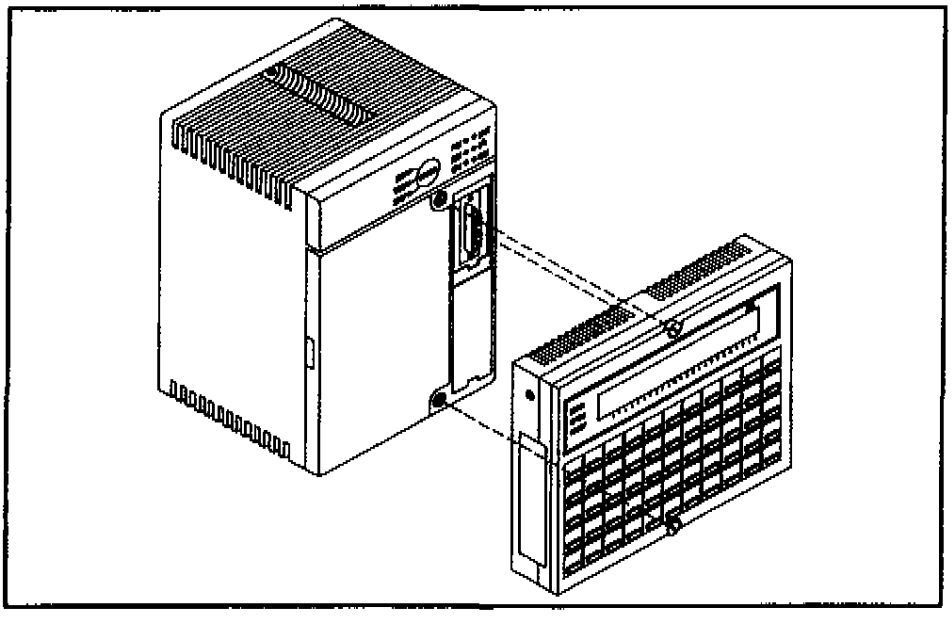


Figure 2-17 Connecting the MIU Directly to the CPU

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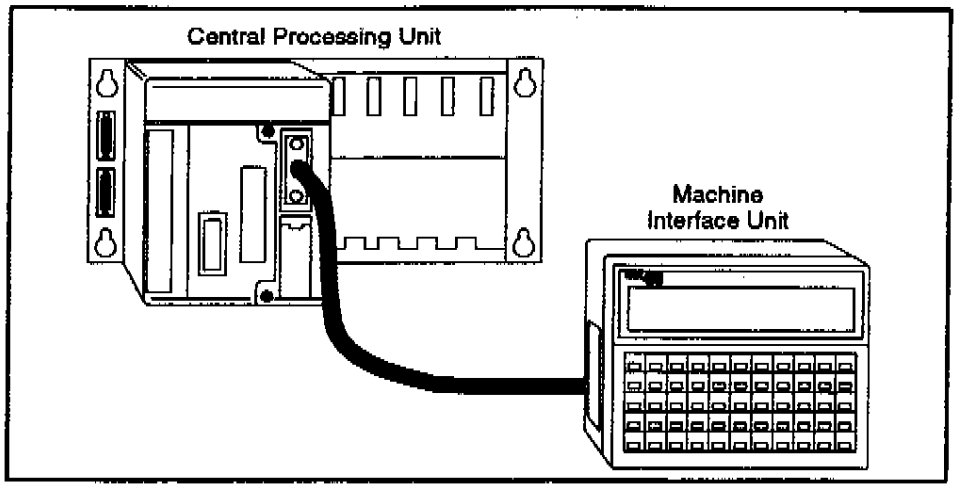


Figure 2-18 Connecting the MIU to the CPU with a Cable

Adjusting the MIUs Contrast

In addition to the backlight, the MIU has a contrast adjustment control as shown in Figure 2-19. Using a small Phillips-head screwdriver, follow the steps below to adjust the contrast.

1. To increase the contrast, turn the contrast adjustment control counter-clockwise.
2. To decrease the contrast, turn the contrast adjustment control clockwise.

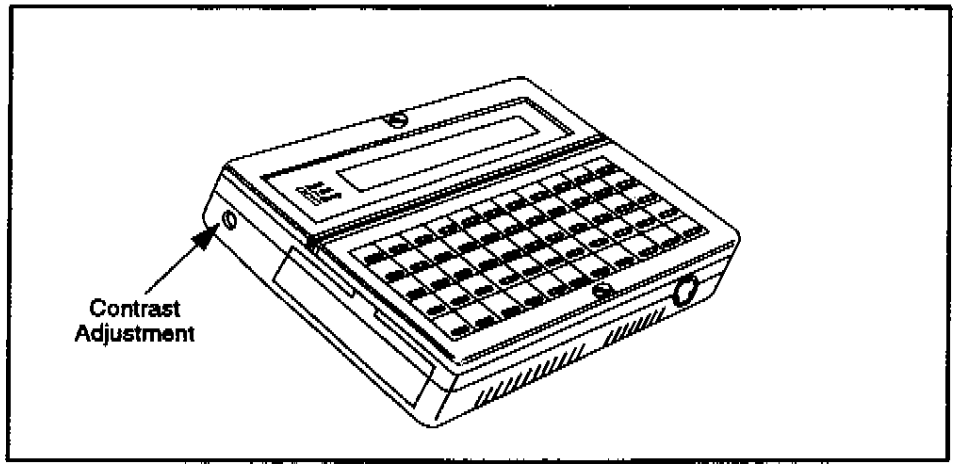


Figure 2-19 MIU Contrast Adjustment Location

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2.11 Setting the CPU Operating Mode

CPU LEDs

The TI425, TI430, and TI435 CPUs have six LEDs that provide a visual status of the operation of the TI405 system. These LEDs are located in the upper-right of the module as shown in Figure 2-20.

- The PWR LED lights when the power supply is producing +5 VDC.
- The RUN LED lights when the CPU is executing the program.
- The CPU LED lights when a CPU error is detected.
- The BATT LED lights when the backup battery voltage is low.
- The I/O LED lights when an I/O error is detected.
- The COM LED lights when a communication error is detected.

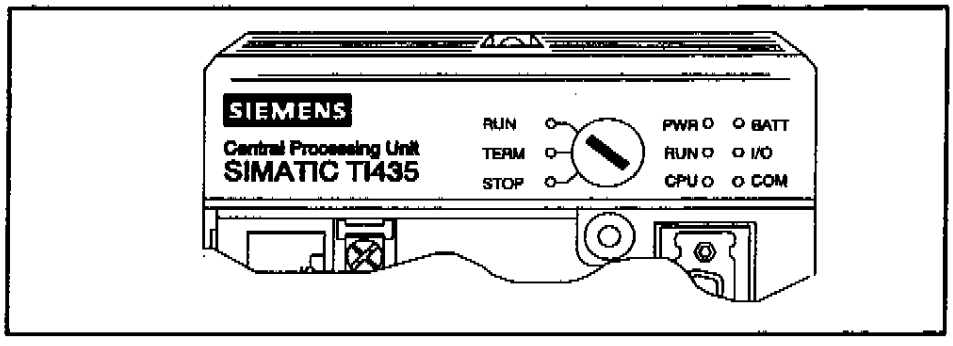


Figure 2-20 The CPUs Keyswitch and LEDs

CPU Keyswitch

The TI425, TI430, and TI435 CPUs have a keyswitch located near the top front center of the module as shown in Figure 2-20. The keyswitch has three settings that control forcing the module into RUN mode, forcing the module to stop, and the normal terminal mode for operation from a programming device.

To prevent an accidental start-up when you are working on wiring in remote locations, set the keyswitch to stop and remove the key.

TERM Mode

In addition to the force RUN and force STOP modes, you will normally set the keyswitch to the TERM or terminal mode. This mode accepts instructions from a programming device such as the Machine Interface Unit (MIU).

In TERM mode, you can use the MIU to set the CPU to RUN mode, STOP mode, or TEST mode. TEST mode allows you to execute a single scan of a program and perform other operations for debugging your program. TEST mode is described in more detail in Chapter 3—Troubleshooting.

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Automatic I/O Configuration

The TI405 CPU is able to sense the I/O modules in its bases and automatically assign addresses. The input module closest to the CPU is assigned a starting address of X0. The output module closest to the CPU is assigned Y0. The CPU assigns consecutive blocks of 8, 16, or 32 octal (base 8) addresses to each module. The input and output modules may be intermixed in any sequence.

> For example, suppose a 16-point input module was installed in base 0 adjacent to the CPU. It is followed by two 16-point output modules and another 16-point input. The first input module is assigned addresses X0 through X17 (octal). The first output is assigned Y0 through Y17. The next module is Y20 through Y37 and the fourth is X20 through X37.

The CPU automatically configures the I/O when power is applied, unless the POWERUP CFG CHECK is turned on using AUX Function 44. The best way to make sure that the I/O configuration is recorded is to press [4] [6] [AUX] [ENT] and look at the resulting display as shown in Figure 2-21.

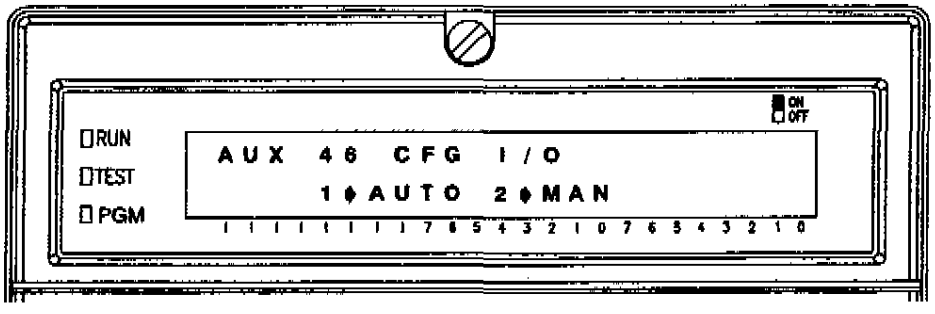


Figure 2-21 I/O Configuration Menu

To select automatic configuration, press [1] [ENT] and wait for the message OK to appear. Press [SHFT] [EXIT] to leave AUX 46. As an alternative to cycling power to record the changed configuration, you can select the new configuration by pressing [4] [5] [AUX] [ENT] [ENT] and seeing the message CFG = NEW displayed. You can then press [4] [1] [AUX] [ENT] to view the I/O configuration. A display similar to the one below appears.

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Use [NXT] and [PREV] to step through the configured modules. When you are satisfied with the configuration, press [SHFT] [EXIT] to leave AUX Function 41.

It is good practice to turn on the POWERUP CFG CHECK using AUX Function 44 once the I/O has been configured. This alerts you to whether or not the I/O module arrangement was modified while power to the system was turned off. It also prevents the possibility of the changed configuration being automatically saved as correct, once power is applied.

From a cleared display, press [4] [4] [AUX] [ENT] and you see the display shown in Figure 2-22.

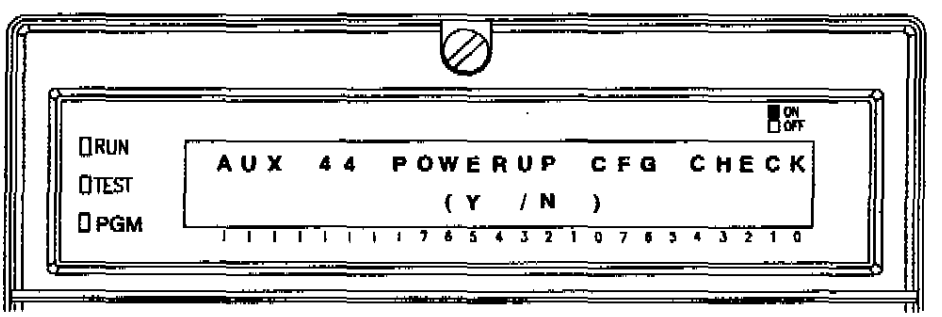


Figure 2-22 Power-up Configuration Check Display

A flashing cursor is positioned over either the Y or the N. Use [ENT] to move the cursor over the Y, if it is not already there, and press [ENT]. The message PWRUP CHK ON is displayed. Press [ENT] again to exit the AUX function.

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Defining Your I/O Configuration (TI435 only)

If your application requires an unusual I/O configuration, such as having X0 and X300 on adjacent input modules in the CPU base, you need to use the manual configuration option in AUX 46. From a cleared display, press [4] [6] [AUX] [ENT] to display the message shown in Figure 2-23.

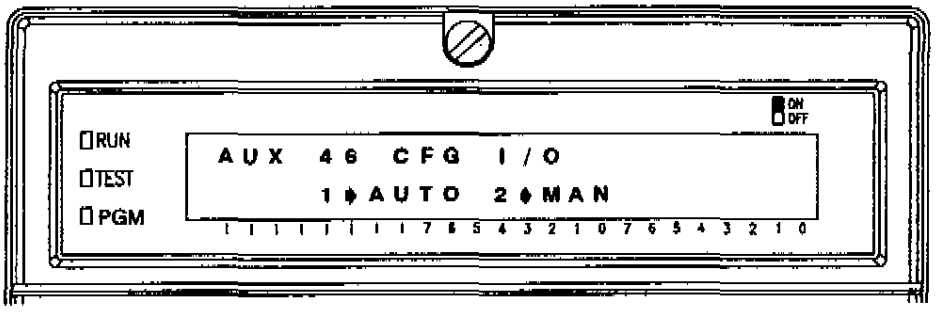


Figure 2-23 AUX 46 Function Menu

Press [2] [ENT] to select manual configuration, and a display similar to 0/0 ——— X 0 will appear. This shows that base 0/slot 0 contains an input module with a starting address of X0. Use [NXT] and [PREV] to step through the modules until you reach the one that you want to modify. You may also step directly to a particular base and slot position by pressing [CLR] and the base and slot number.

> For example, to select base 1/slot 3, press [CLR] [1] [3] [NXT]. To assign a starting address of Y300 to the output module at that position, press [Y/OUT] [3] [0] [0] [ENT]. You could assign a starting address of X140 to the input module in base 1/slot 2 by pressing [PREV] [PREV] [X/INP] [1] [4] [0] [ENT].

Although the automatic configuration function recognizes 8-point I/O modules, and assigns starting addresses accordingly, the manual configuration operation assumes that all modules have at least 16 points. This means that manually assigned addresses must be an even multiple of 20 (octal), such as X20, Y60, or Y300. Addresses such as X10 or Y50 are not allowed as manual configuration entries.

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Once you have entered the desired configuration, press SHIFT EXIT to exit the AUX function and save your configuration to memory. Your configuration is saved until you use AUX 46 again to manually modify the configuration, or to automatically configure the I/O.

If you save your program to memory cartridge or cassette tape, be sure that you also save the system parameters by repeating the save function and selecting the SYS option. If you do not do this, your memory configuration is not saved along with your program, and may be lost. If you save the system parameters to memory cartridge or tape, your I/O configuration can be retrieved by using the SYS option in the appropriate load function. This saves having to manually configure the I/O after the program is loaded.

⚠WARNING

Manual configuration of a single module causes the I/O configuration of the preceding and following modules to change. The TI405 does not allow you to assign duplicate point numbers. The completed I/O configuration must be checked using AUX 41 to help ensure that all I/O address assignments are correct before selecting RUN mode. Failure to check and correct I/O configuration errors before switching to RUN mode could cause equipment damage and potential injury to personnel.

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2.13 I/O Module Numbering Notation

The TI405 I/O modules incorporate two methods of module identification. Each module has a color strip (located just below the module number)

- Blue for all input modules
- Red for all output modules, and
- White for all special modules. (See Figure 2-24.)

The second identification method is incorporated into the module's unique number.

- The first digit of the number indicates the circuit type.
- The second digit indicates the number of points.
- The third digit indicates whether the module is an input or output module.

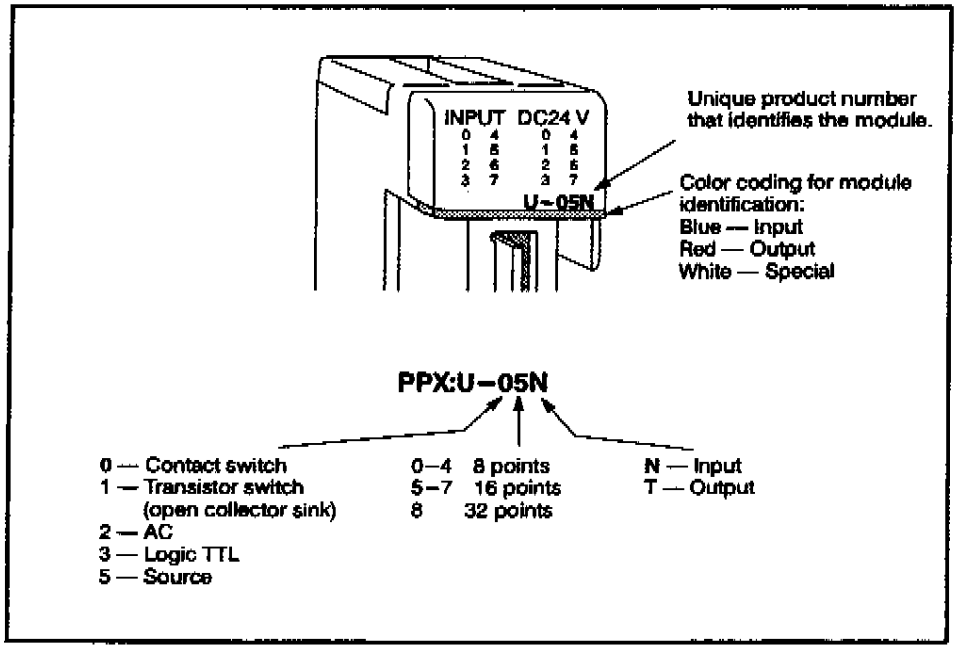


Figure 2-24 Identifying the I/O Modules

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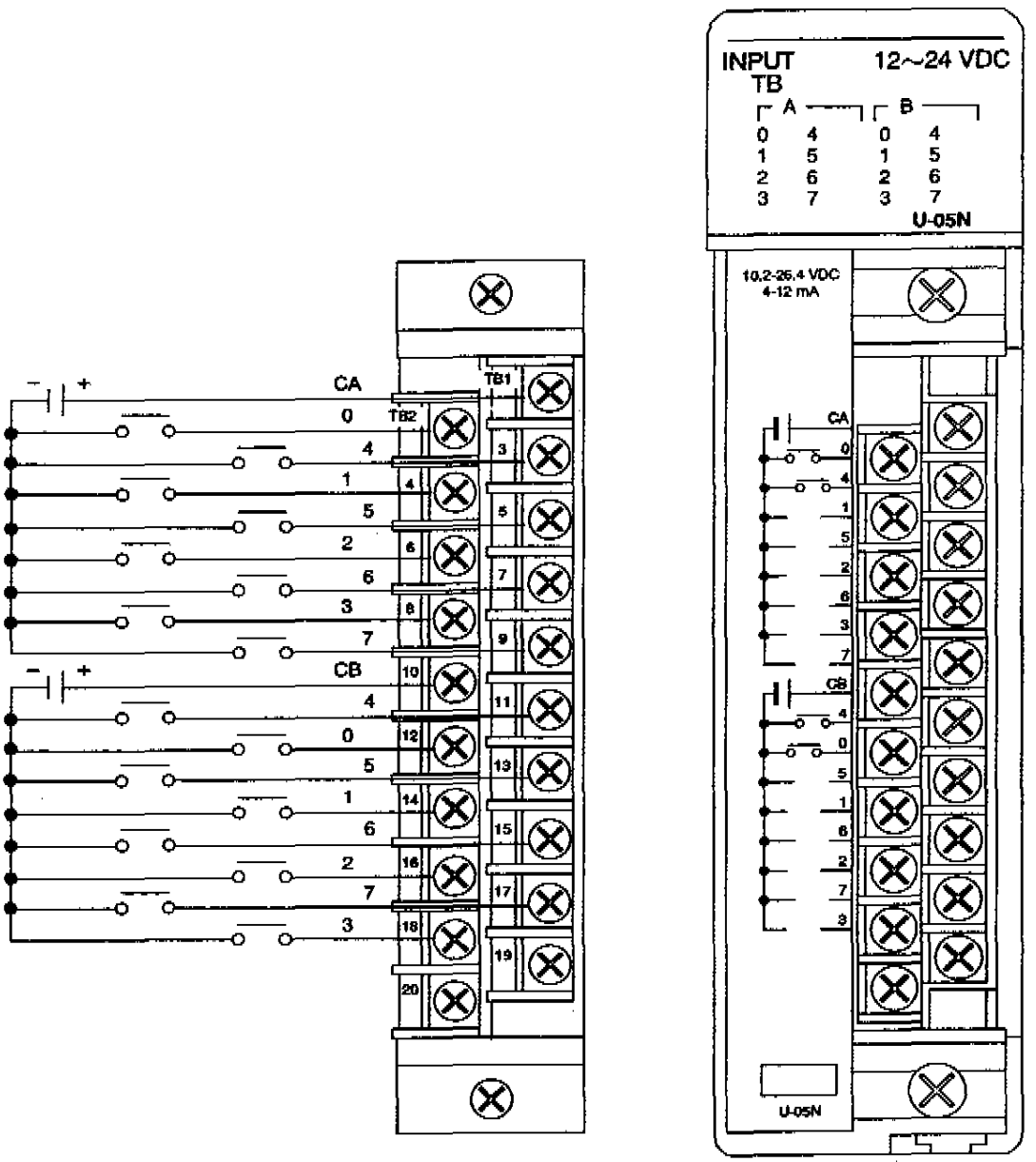


Figure 2-25 PPX:U-05N 12–24 VDC Input Module (Negative Logic)

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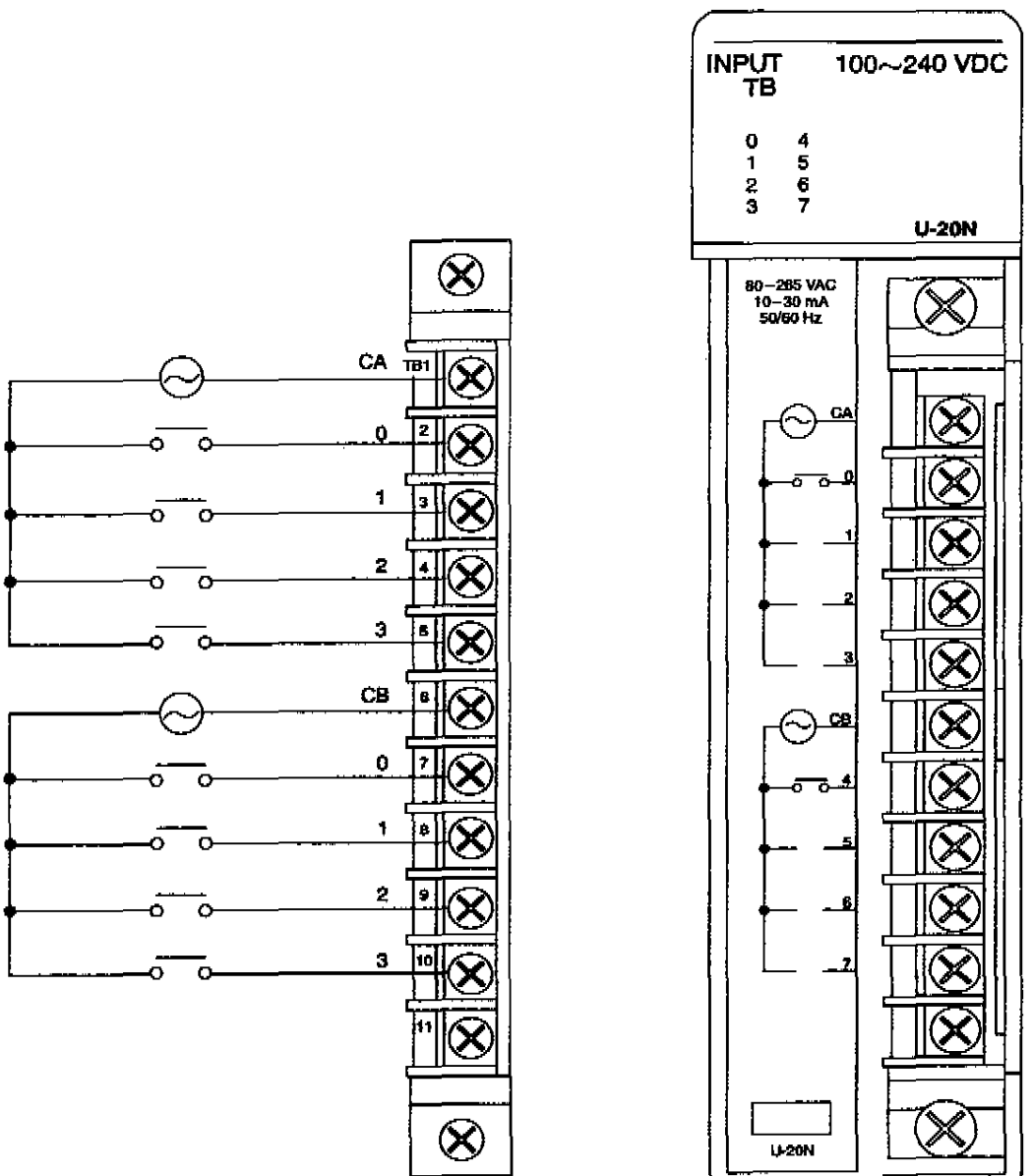


Figure 2-26 PPX:U-20N 115/230 VAC Input Module (Negative/Positive Logic)

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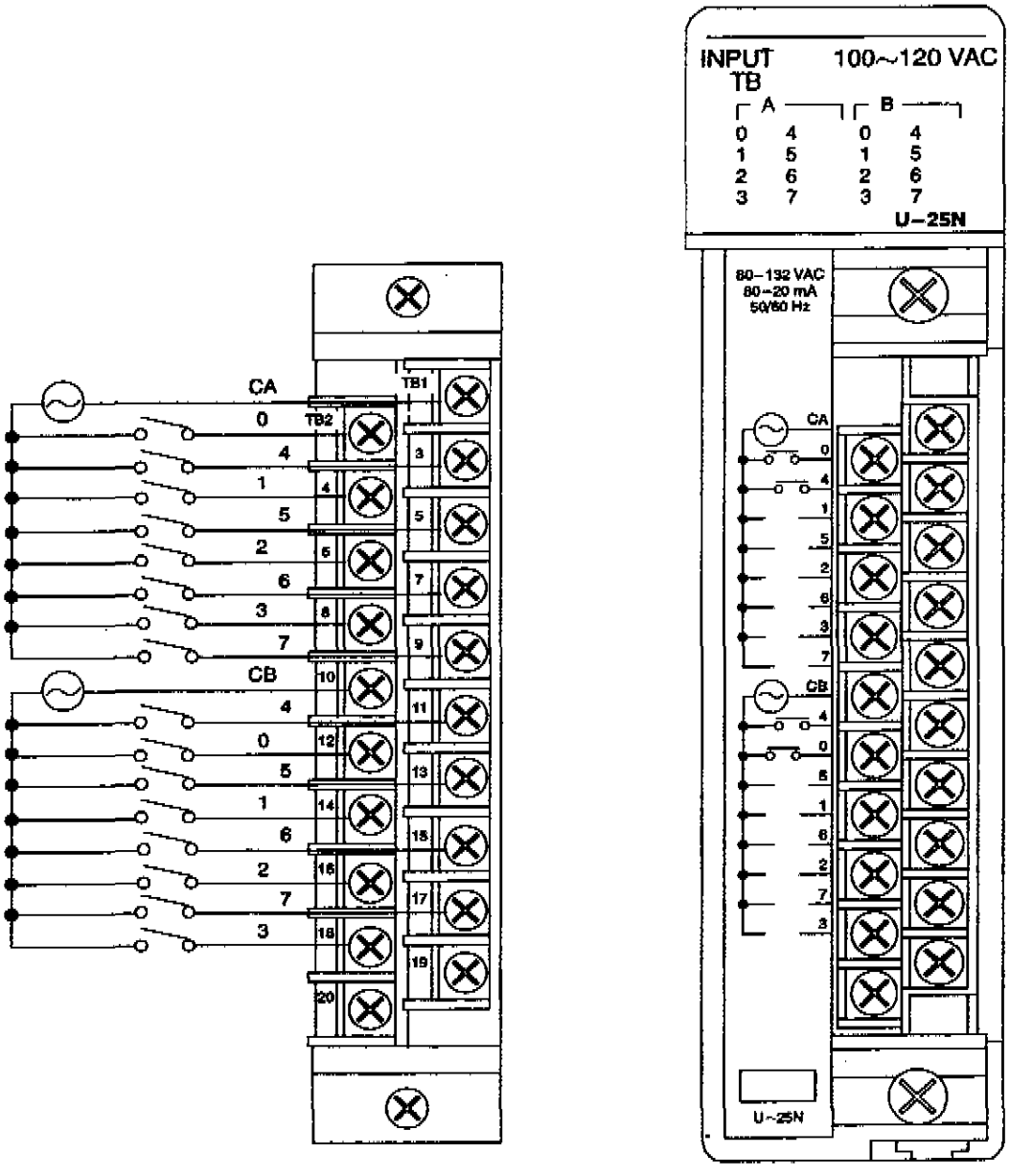


Figure 2-27 PPX:U-25N 115 VAC Input Module

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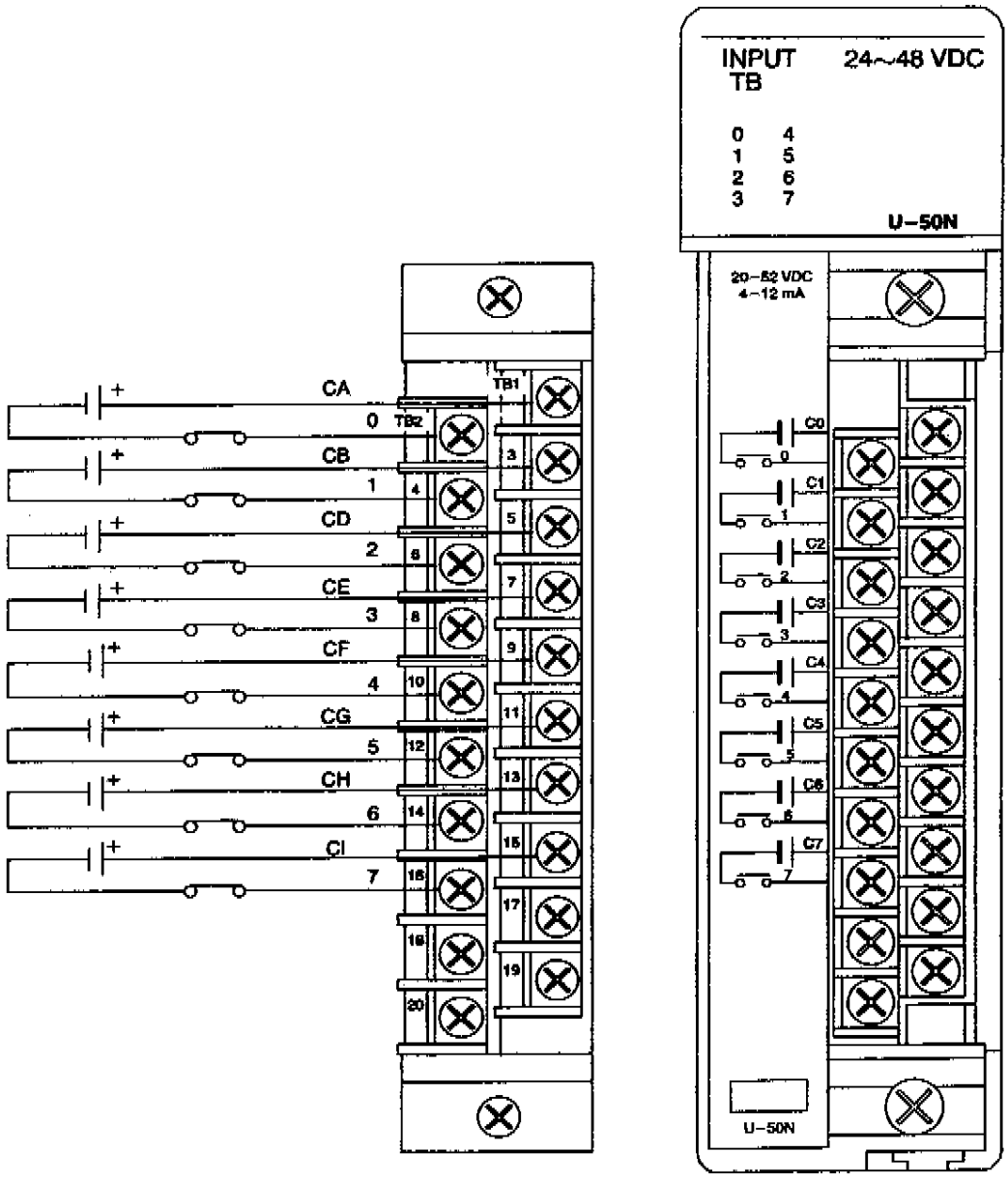


Figure 2-28 PPX:U-50N 24-48 VDC Input Module (Isolated)

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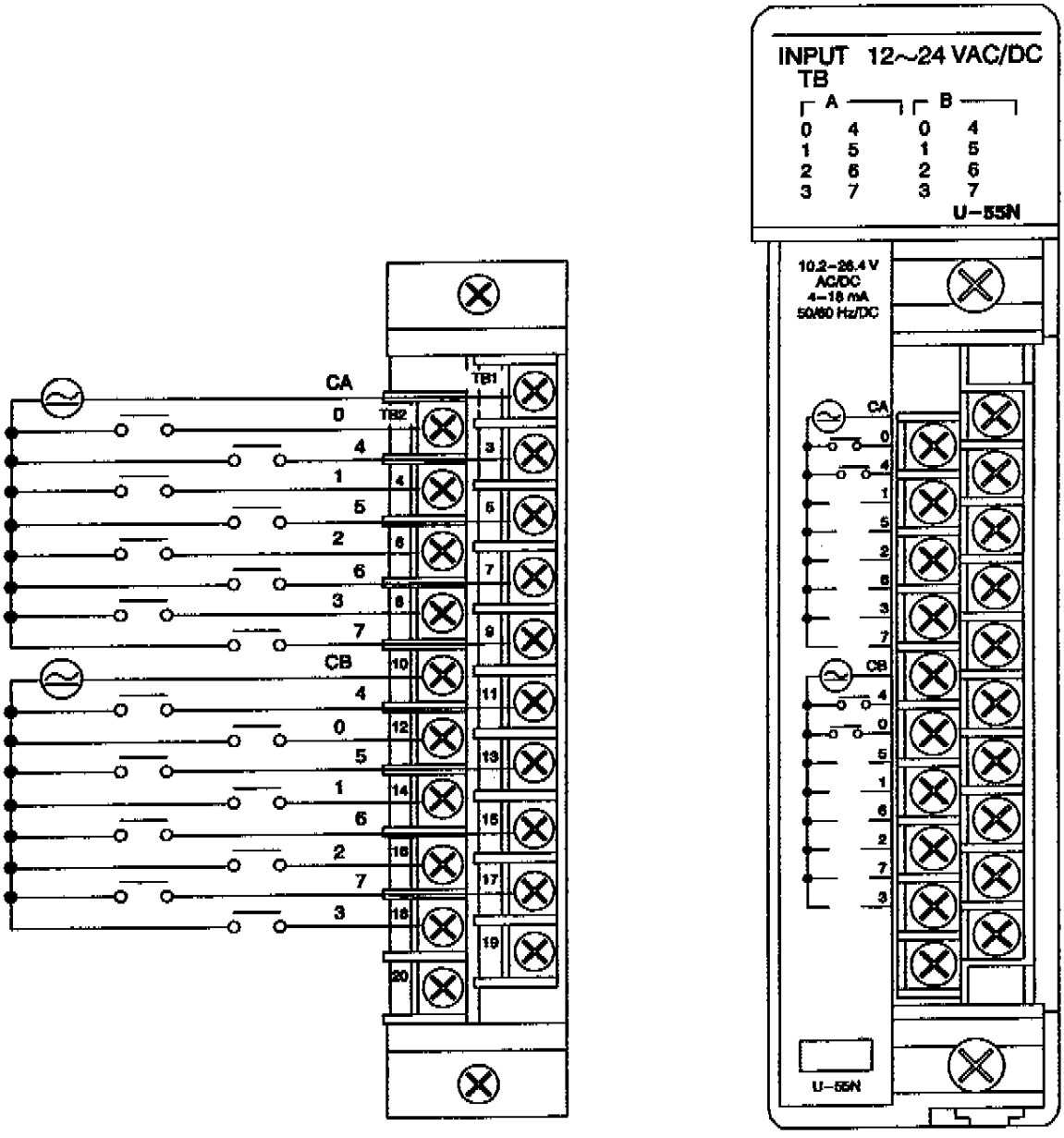


Figure 2-29 PPX:U-55N 12-24 VAC/VDC Input Module

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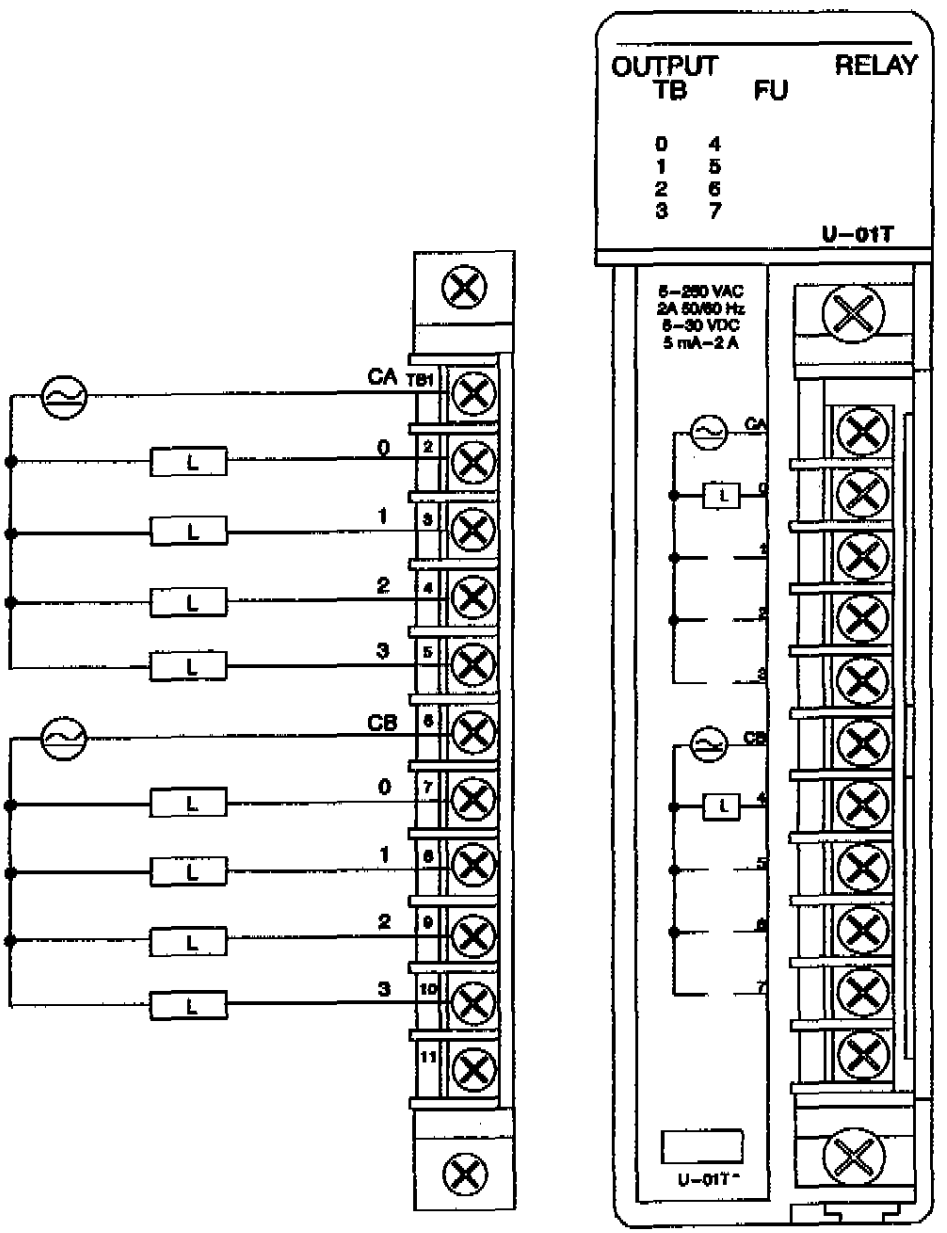


Figure 2-30 PPX:U--01T 8-Point Relay Output Module

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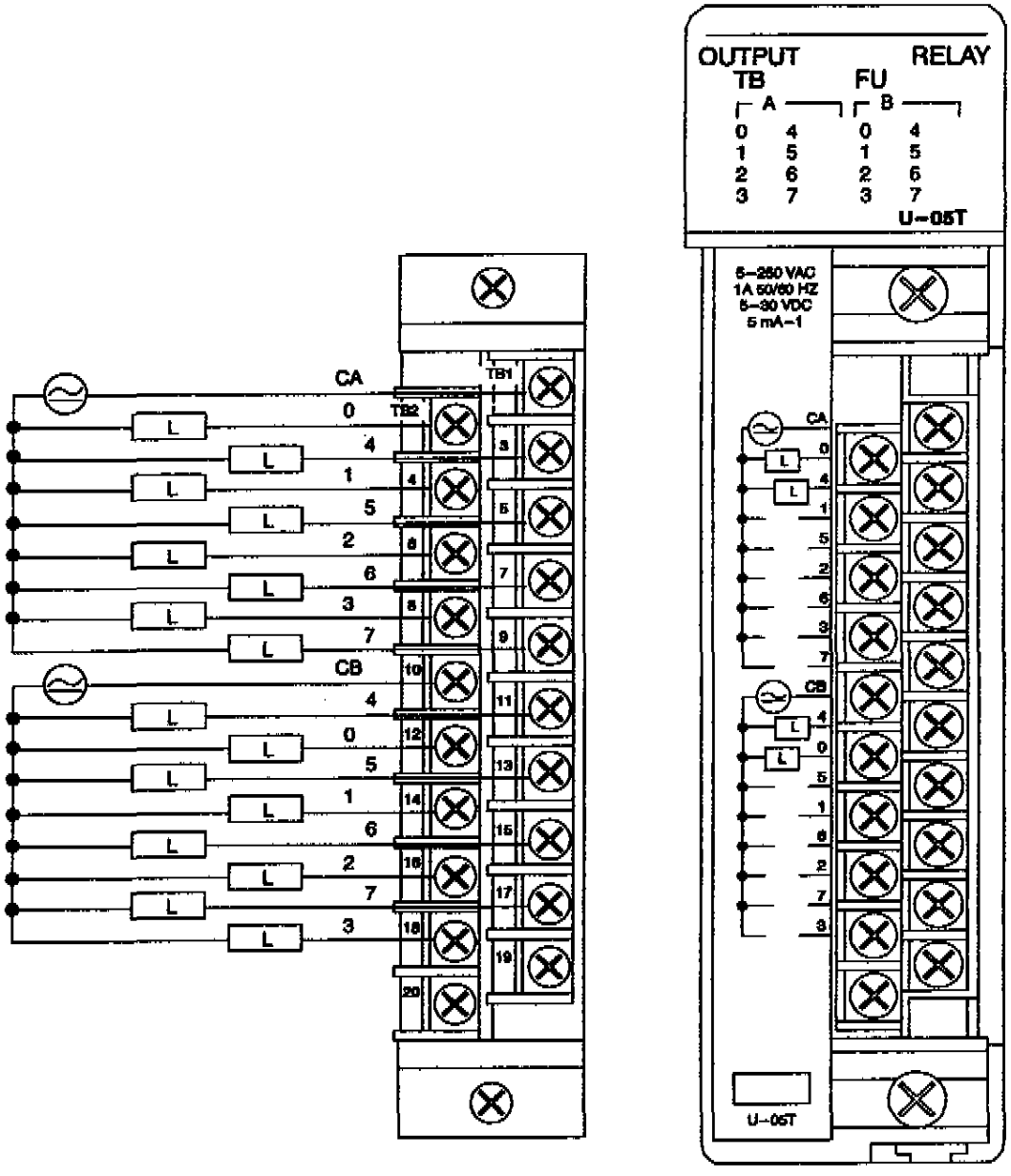


Figure 2-31 PPX:U-05T 16-Point Relay Output Module

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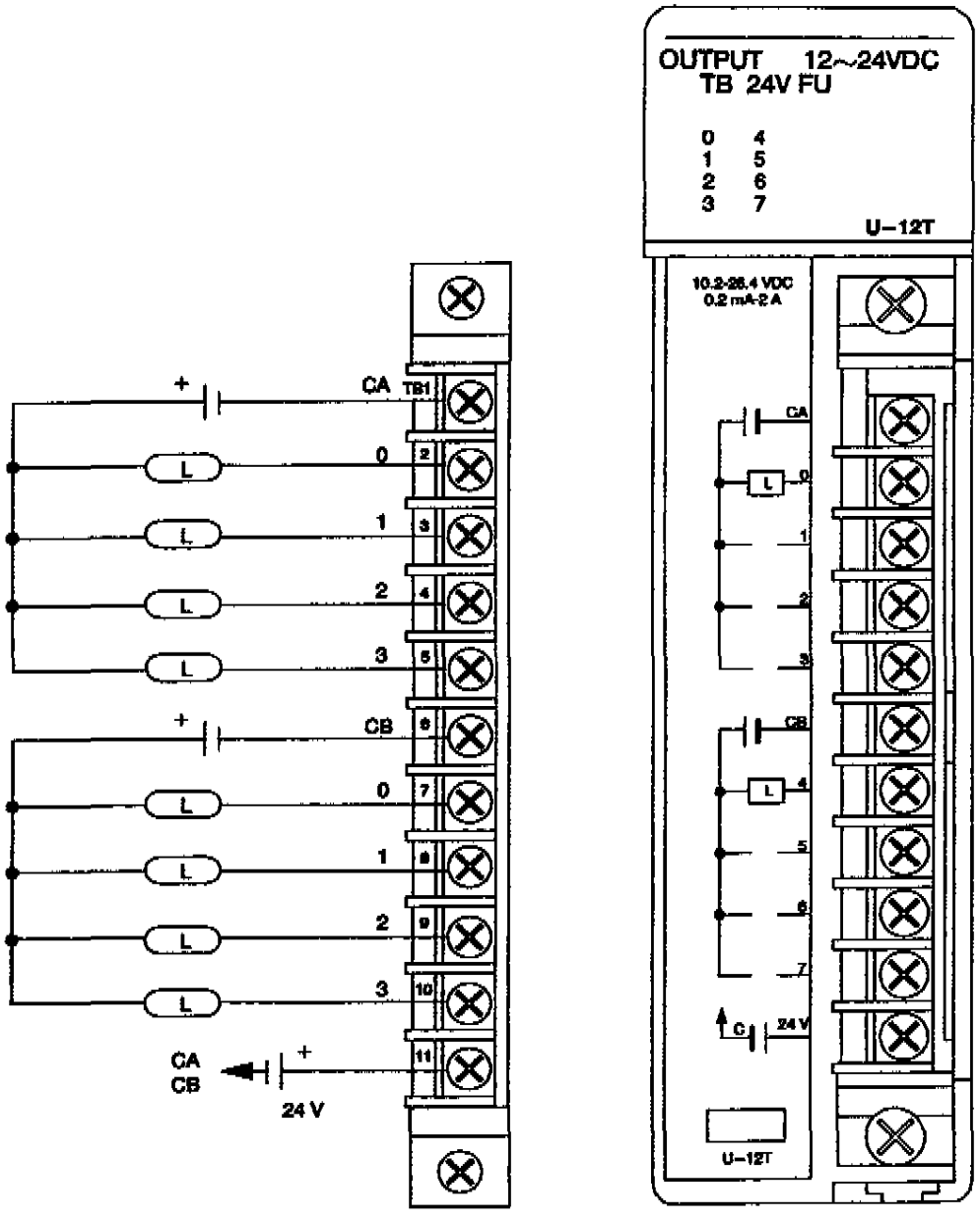


Figure 2-32 PPX:U–12T 12/24 VDC Output Module (Negative Logic, Sinking)

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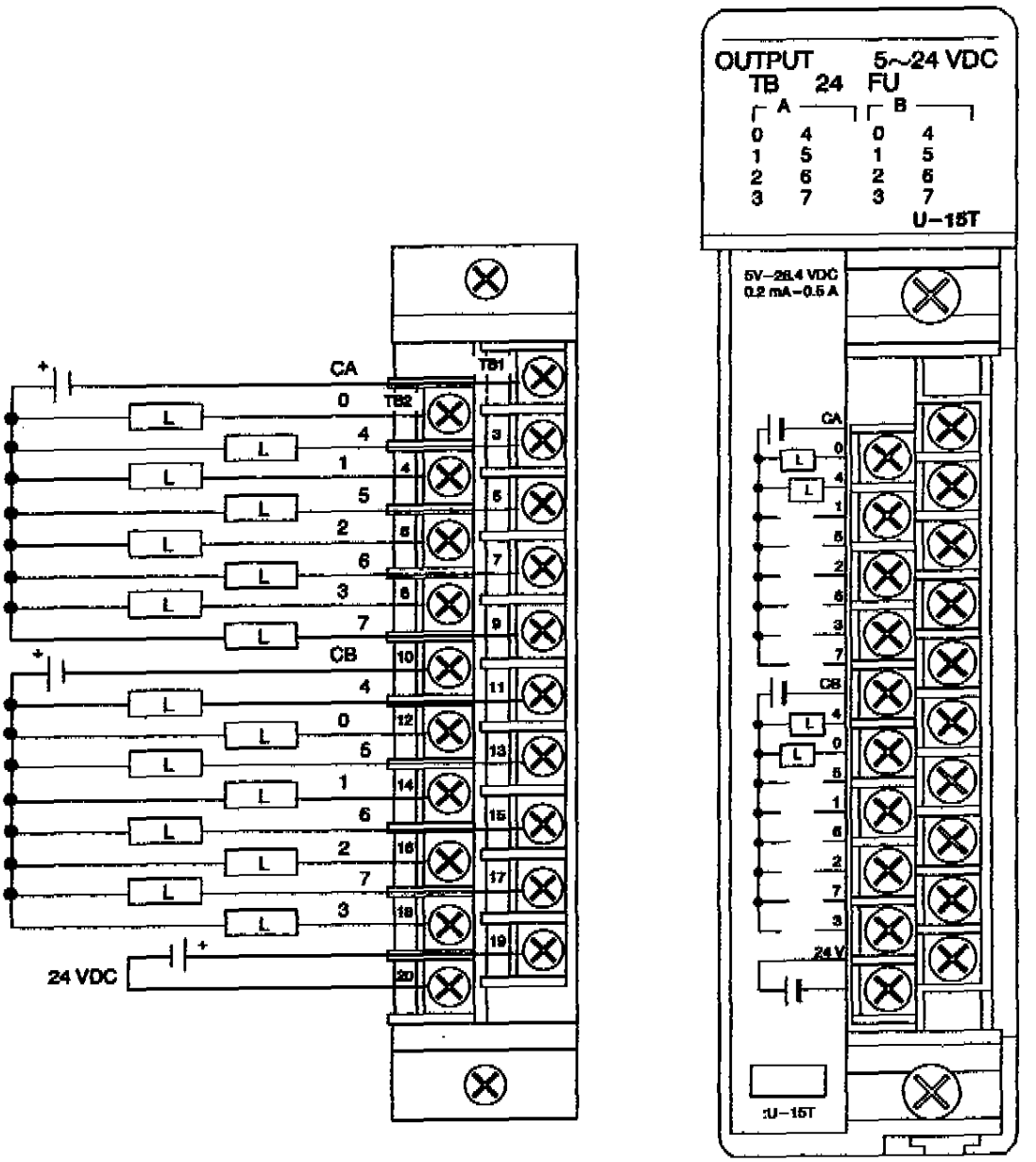


Figure 2-33 PPX:U-15T 24 VDC Output Module (Negative Logic, Sinking)

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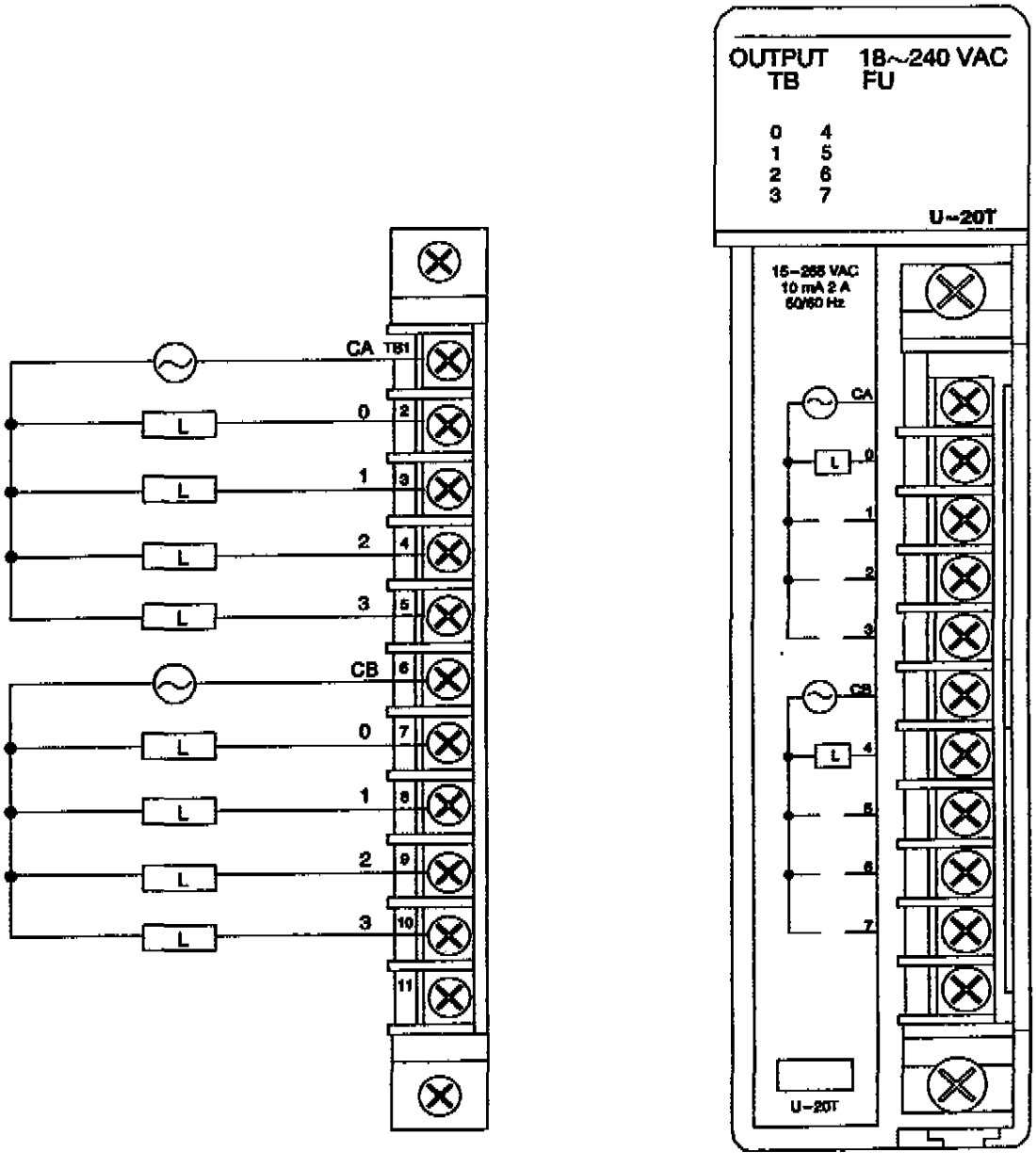


Figure 2-34 U–20T 8-Point 115/230 VAC Output Module

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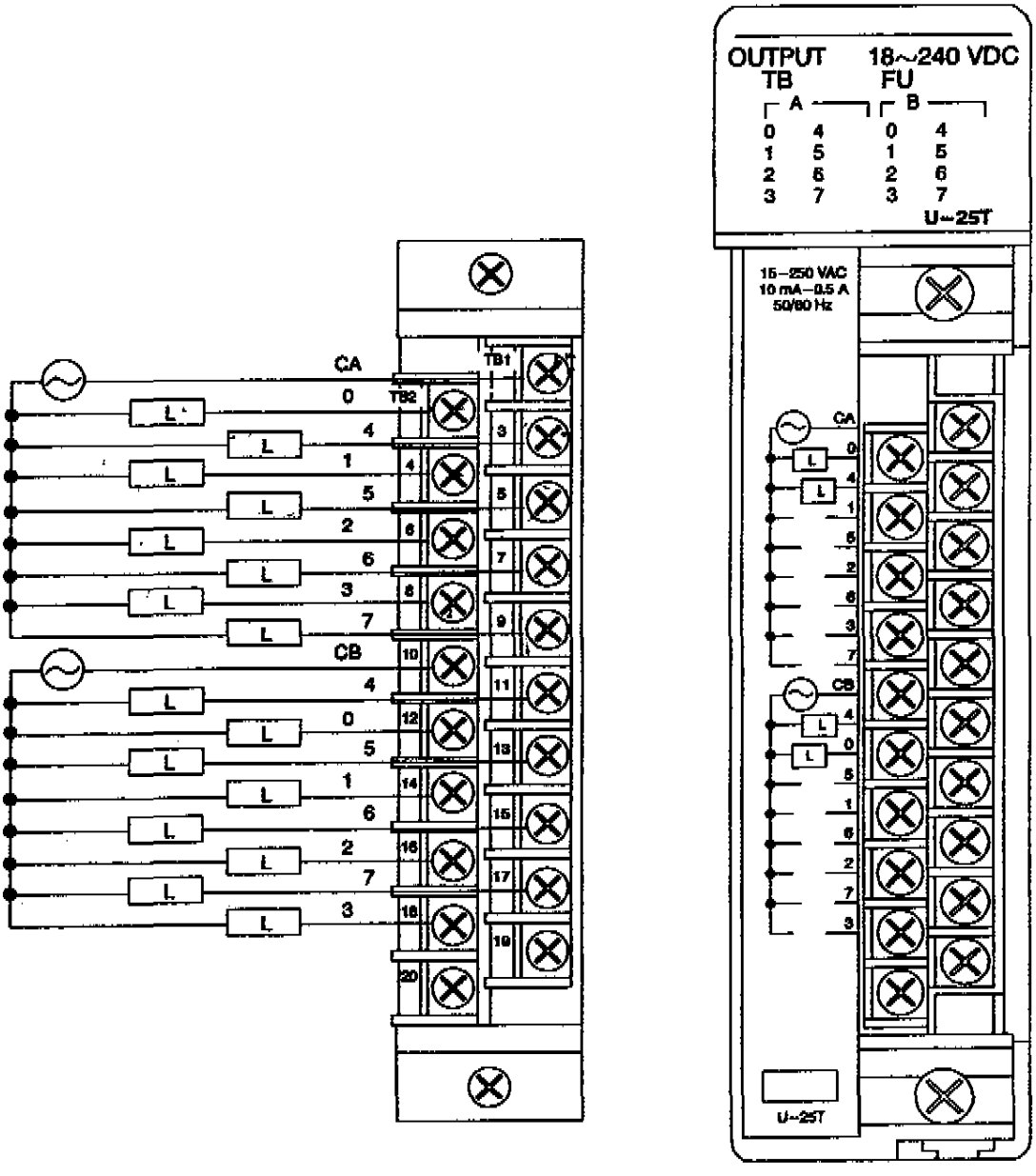


Figure 2-35 PPX:U~25T 16-Point 115/230 VAC Output Module

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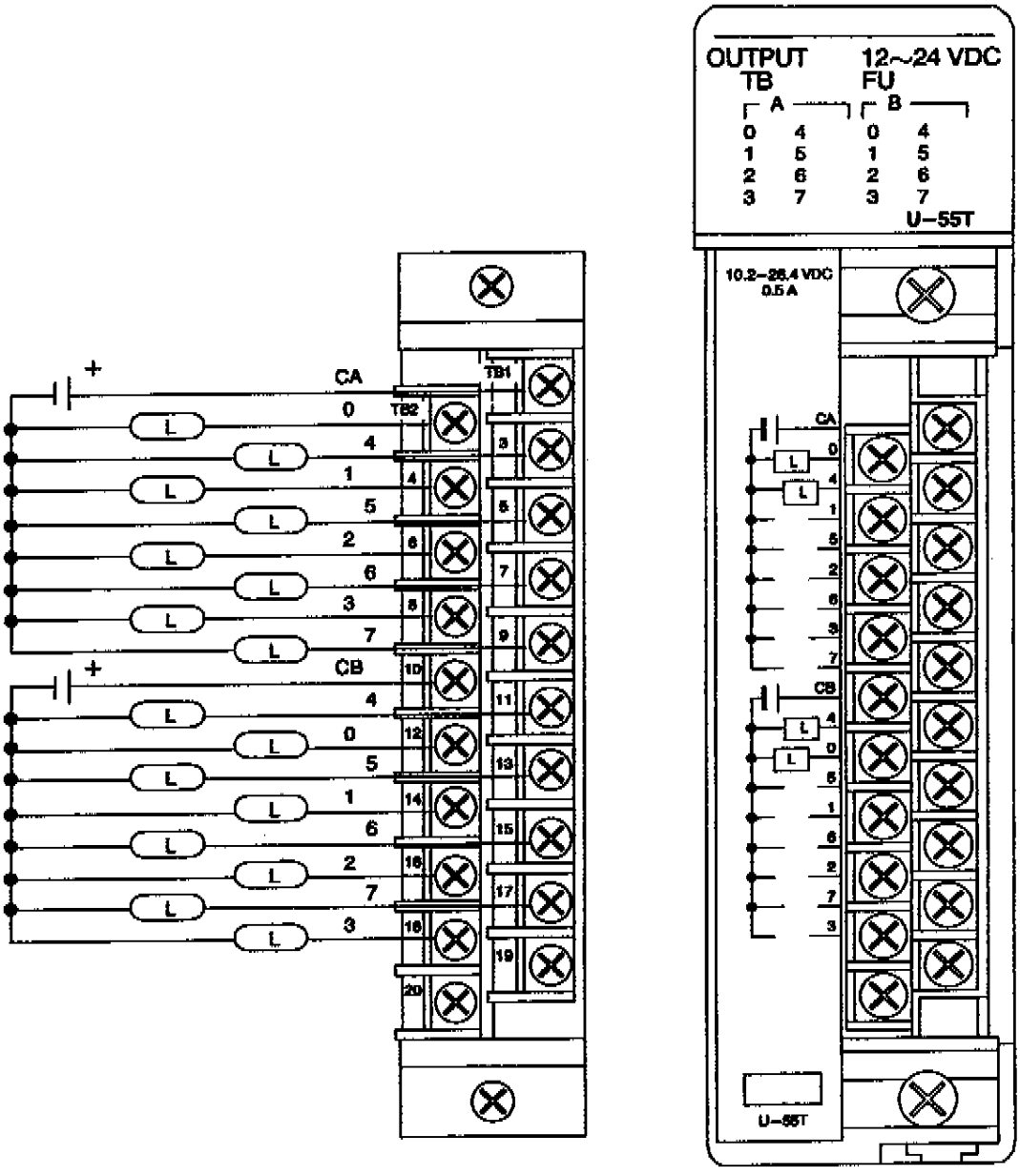


Figure 2-36 U–55T 12/24 VDC Output Module (Positive Logic, Sourcing)

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PPX:U-05S Input Simulator Module

The Input Simulator module can operate as either 8 or 16 input points by setting the selector switch to the desired number of points, as shown in Figure 2-37. If you select the 8 input mode, A0 through A7 are active and LED #8 lights when power is applied to the system. If you select the sixteen input mode, all inputs are active and LED #16 lights when power is applied to the system.

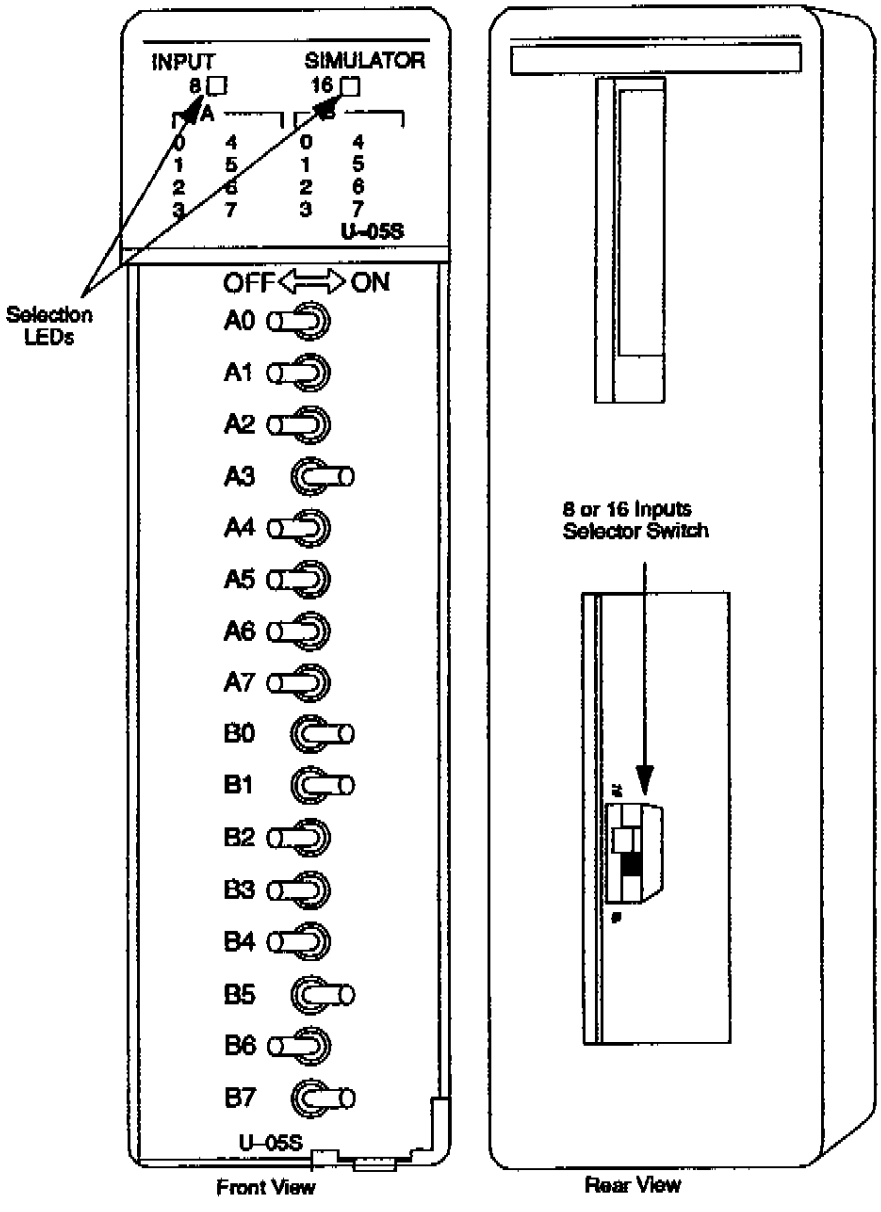


Figure 2-37 PPX:U-05S Input Simulator Module

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Chapter 3

Troubleshooting and Maintenance

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3.1 Introduction

Troubleshooting methods for any machine control system usually rely heavily on isolation techniques. The TI405 system provides several isolation techniques for quick problem identification and resolution. The Machine Interface Unit (MIU), coupled with the LED indicators on all modules, provide an instant visual indication of the system and individual module status.

One isolation technique is to determine the power flow status of a discrete point. The MIU, functioning as an operator interface, displays the power flow status of any discrete point referenced in a program. This is useful for isolating points located in a remote base.

The MIU can also be used to monitor program progress, view operand values, and set operand values. Section 3.4 describes several methods for using the MIU as a troubleshooting tool.

Self-test diagnostics provide another isolation technique. The MIU contains a complete set of self-test diagnostic routines to determine the operational status of its features. The TI405 CPUs provide internal diagnostics during run-time, and specific services when the system is in program mode. By using the system supplied Special Relays, a program can detect and respond to problems that may occur in a TI405 system.

An often overlooked troubleshooting method is preventive maintenance. The TI405 system requires very little preventive maintenance. The only requirement is to replace the CPU and Memory Cartridge (MC) battery periodically. Battery replacement details are provided later in this chapter.

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3.2 PPX:U–01NI Interrupt Input Module, & Read/Write Shared RAM on MIU

PPX:U–01NI Interrupt Input Module

TI425 CPU V2.1 and TI435 CPU V2.1 are the first firmware releases compatible with the PPX:U–01NI Interrupt Input Module.

This module is an 8-channel, isolated-input module that provides TI405 controllers with interrupt capability. These interrupt inputs, used in conjunction with immediate inputs and outputs, are particularly useful in applications that require data to be acted upon in less than full program scan time.

When an interrupt signal is received, the CPU immediately goes to the interrupt routine with the same label number as the input point, and begins execution. The routine is executed, and the CPU resumes the normal scan until another interrupt signal is received.

For more information, refer to the *SIMATIC TI405 Interrupt Module Manual* (PPX:405–8109).

Read and Write Shared RAM (AUX 47 on MIU)

AUX 47 was added for the MIU to allow reads and writes to shared RAM on I/O modules that use the I/O (serial) bus. This function is available on TI425 and TI435 CPUs, V2.1 or greater, using MIU V3.6 or greater. Up to four bytes can be read or written each time.

NOTE: Currently, the PPX:U–01Z High-Speed Counter module is the only TI405 I/O module with shared RAM that uses the I/O (serial) bus. The PPX:U–01DM Data Communication Module, PPX:405–LIC Link Interface Controller, and the PPX:U–03RM Smart Slice Master all use the parallel bus rather than the serial bus.

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For example, Figure 3-1 shows how to read the preset value from a High-Speed Counter (PPX:U–01Z) module located in base 0 slot 2 and then change this value.

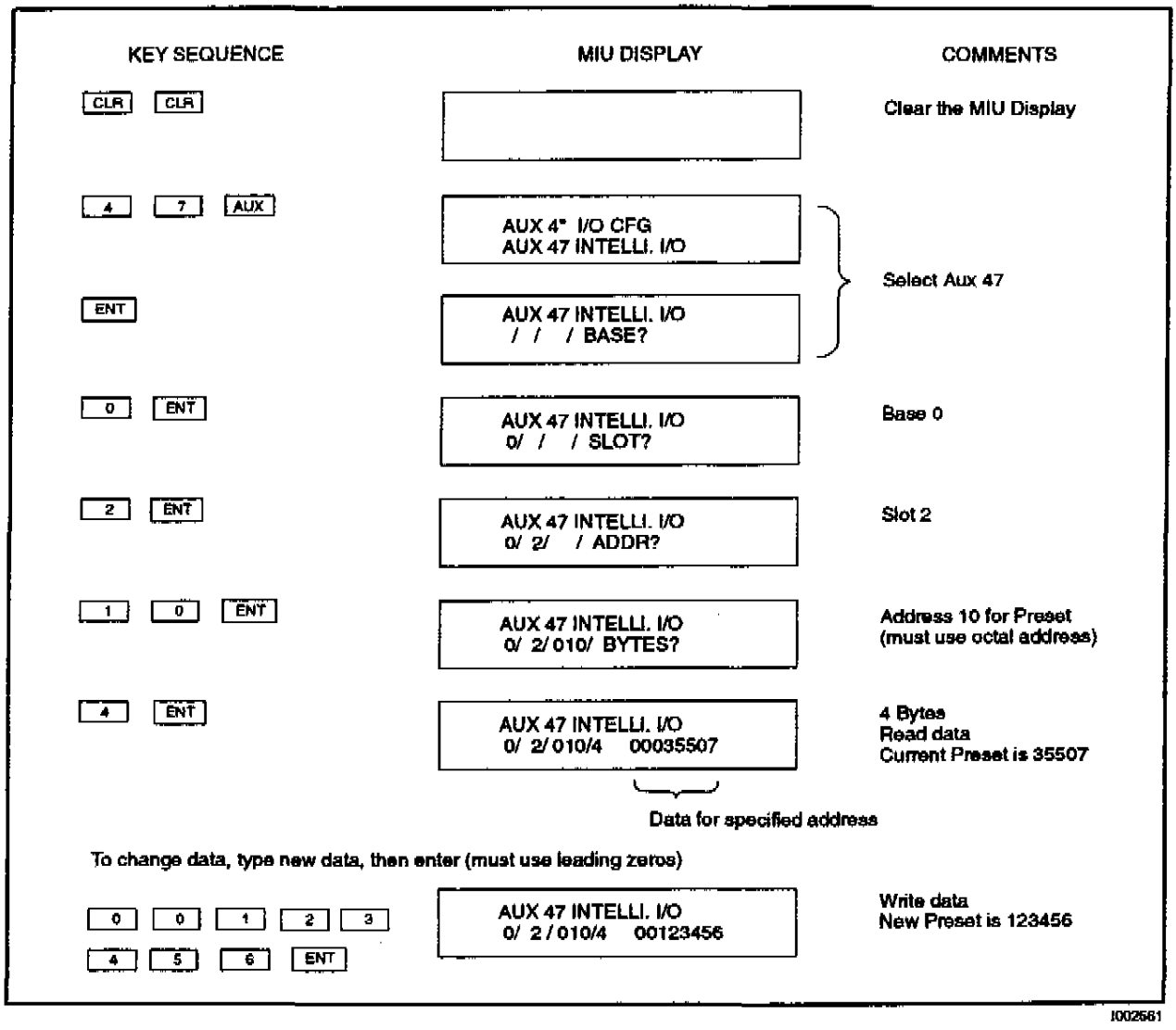


Figure 3-1 Example Read and Write Shared RAM (AUX 47 on MIU)

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The MIU has an I/O status indicator in the upper right corner of its display, which appears when the CPU is in either the RUN mode or RUN-TEST mode. Whenever an instruction is displayed that contains an X, Y, C, S, T, CT, SP or GX reference, an S appears as an indicator if the point is turned off. See Figure 3-2.

If the referenced point is turned on, a solid black rectangle appears. See Figure 3-2. The I/O status indicator only shows the state of the displayed point, and does not reflect the cumulative power flow through a network of contacts.

If a timer or counter instruction is displayed, an S appears until the preset is reached, then the black rectangle takes its place until the timer or counter is reset.

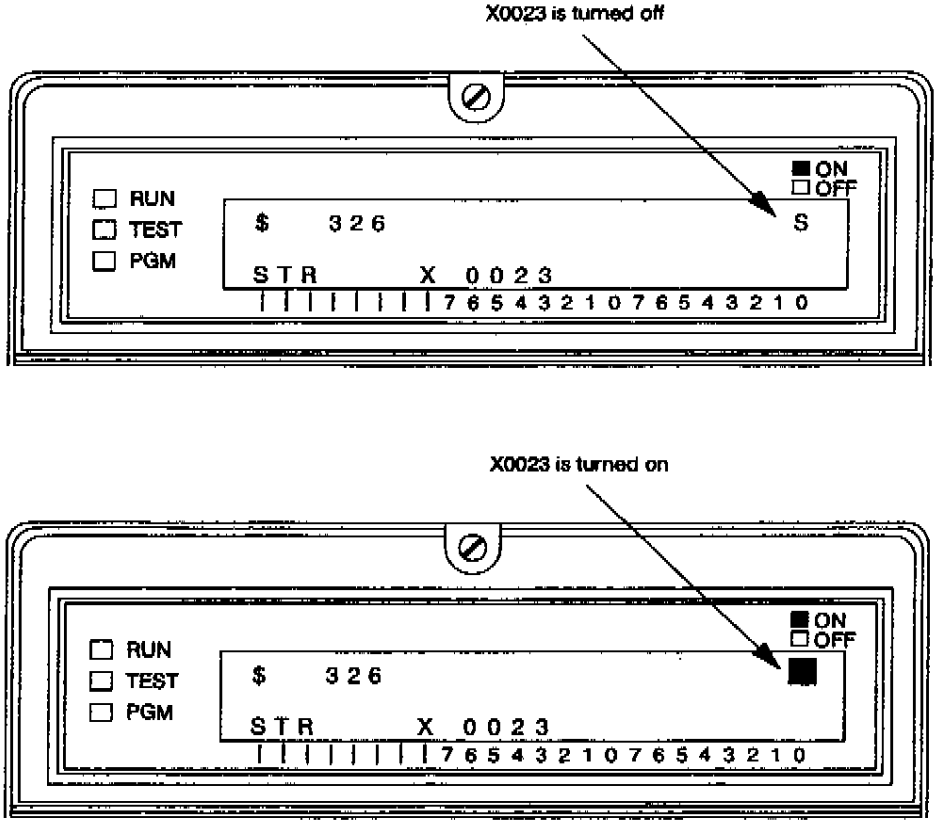


Figure 3-2 Power Flow Indications on the MIU

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3.4 Using the MIU to Troubleshoot Your System

Displaying Error Messages

The S-10P Machine Interface Unit (MIU) allows access to many of the TI405 diagnostic and error reporting features. If a system problem is suspected, the MIU should be connected to the CPU so that any error messages generated by the TI405 are displayed on the MIU. These error messages often pinpoint the source of the problem and save a considerable amount of time compared with traditional PLC troubleshooting techniques.

Error Analysis

If an error message is displayed, refer to Appendix C for a complete list of TI405 error messages, along with typical causes and actions to clear the error condition. Some errors also cause Special Relays to turn on, and error codes to be loaded into specific V-memory locations. These relay numbers and memory locations are noted, along with the error description, in cases where they are used.

Monitoring V-Memory with the MIU

The MIU can be used to monitor and to modify V-memory locations while the program is running. To monitor location V7757, press [V] [7] [7] [5] [7] [WRITE]. The display shown in Figure 3-3 appears on the MIU. Use [PREV] and [NXT] to step through adjacent V-memory locations.

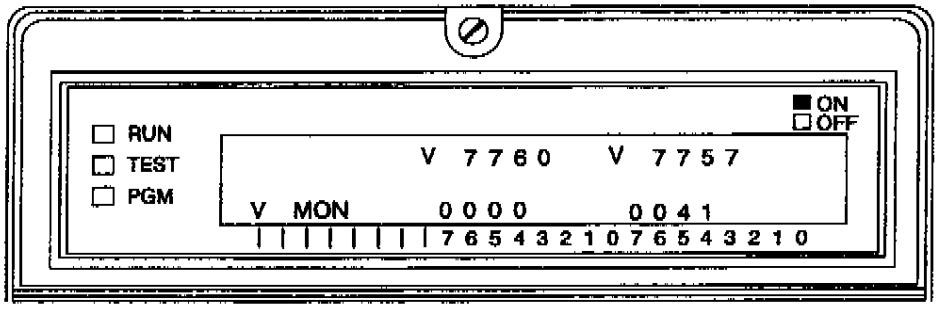


Figure 3-3 Monitoring a V-memory Address in Run Mode

In this case a value of 0041 is in location V7757. This shows that a minor error E0041 has occurred, which indicates a CPU battery low condition.

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Monitoring Timer Current Values with the MIU

Timer current values can be monitored by displaying the V-memory locations with the same numbers as the timers. The current value of timer 12 is stored at location V12. Counter current values are stored at the V-memory locations that are 1000 greater than the counter number. For example, the current value of counter 7 is stored at V1007.

Changing V-memory Values with the MIU

The value in the V-memory location on the right side of the display can be modified from the word status display. This can be useful while troubleshooting by allowing you to load known values into specific memory locations. To enter a value of 342 into location V4000, press [V] [4] [0] [0] [0] [WD ST] and see the display shown in the top illustration in Figure 3-4.

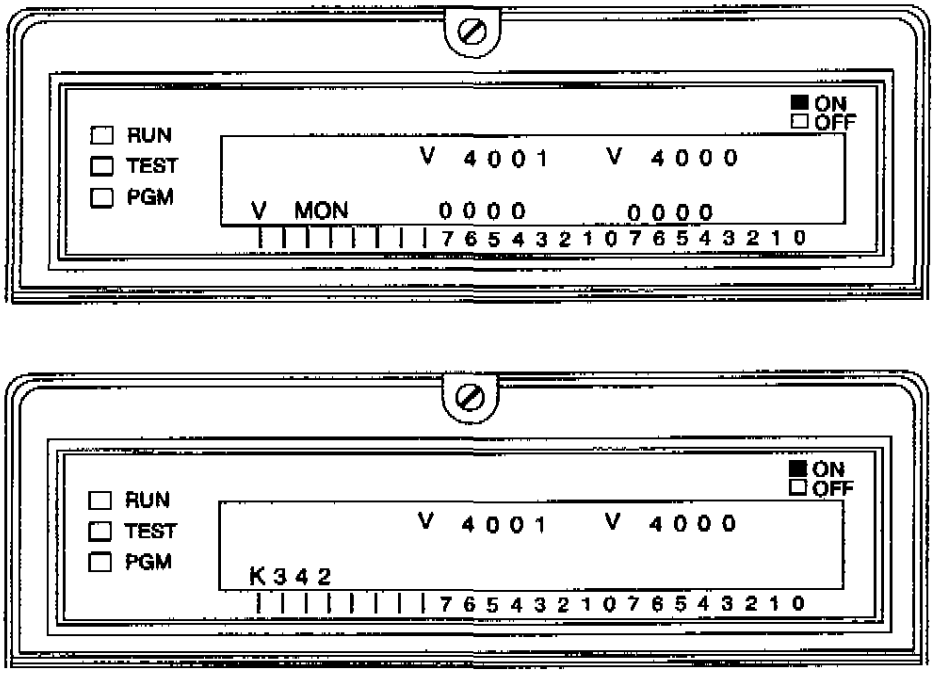


Figure 3-4 Storing a Constant in V-memory

Press [SHIFT] [3] [4] [2], and the display appears as shown in the bottom illustration of Figure 3-4. Once [ENT] is pressed, 0342 appears under V4000 on the display.

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Monitoring Discrete I/O Points with the MIU

It is also possible to monitor sixteen discrete I/O points at once with the MIU. X inputs, Y outputs, GX remote I/O, control relays, timer and counter contacts, stages and special relays can each be monitored in groups of sixteen. A black rectangle appears to indicate that a specific point is turned on. Input and output status can be monitored on the MIU and compared against the actual I/O module states to help find failed I/O points or programming errors.

To monitor Y0 through Y17, press [MONITR] [0] [INT ST]. Figure 3-5 shows how the display would appear if Y1, Y7, and Y13 were all on.

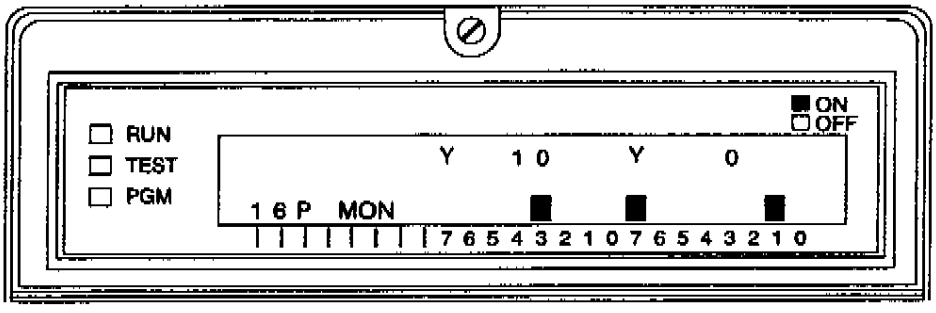


Figure 3-5 Monitoring Output Points

Forcing Points---Points may be forced on or off from this display in RUN mode, TEST-RUN mode, or PGM mode. To force Y1 on, press [MONITR] [1] [SHIFT] [ON]. To force C27 off, press [CNSTN] [2] [7] [SHIFT] [OFF]. See Section 3.8 for more information on forcing I/O points.

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Using Test Mode

TEST mode allows you to either run a given number of scans of your program and stop, or go into TEST-RUN mode and run continuously until you request TEST-PGM mode. To enter TEST mode, perform AUX Function 12 by pressing [1] [2] [AUX]. The message in Figure 3-6 is displayed.

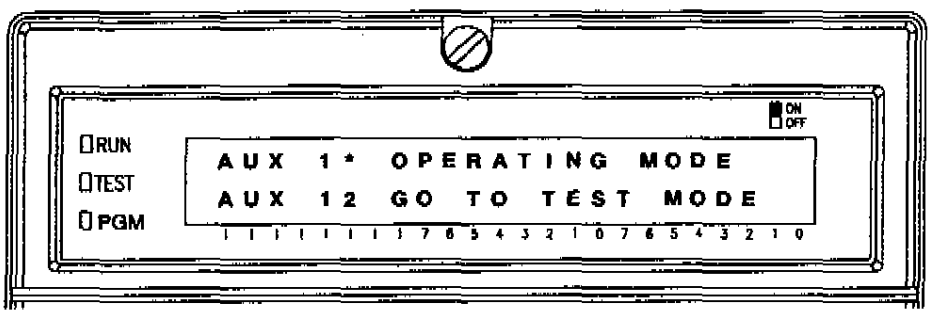


Figure 3-6 Test Mode MIU Display

Press [ENT], and `TEST MODE?` appears on the display. Press [ENT] again, and either `MODE = TEST-PGM` or `MODE = TEST-RUN` is displayed, depending on whether the CPU was in PGM mode or RUN mode when TEST mode was selected. While TEST mode is selected, the CPU is always be in either TEST-PGM or TEST-RUN mode, depending on whether or not the program is currently executing.

Specifying the Number of Scans—You have two options while in the TEST-PGM mode. You may specify the number of times that you want your program to scan and then stop by beginning with a cleared display and pressing [1] [SHIFT] [TEST] [ENT]. The message `NO. OF SCANS?` is displayed. Enter a number from 1 through 65535 and press [ENT]. The mode changes to TEST-RUN until the scanning is complete. Your other option is to press [3] [SHIFT] [TEST] [ENT] and go into the TEST-RUN mode.

The only test function that you can request in TEST-RUN mode is to stop scanning. This is done from a cleared display by pressing [2] [SHIFT] [TEST] [ENT]. This will return the CPU to TEST-PGM mode.

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Using Test-Run Mode

While in TEST-RUN mode, a different display is available when viewing program instructions than when the CPU is in RUN mode. Section 3.3 describes the power flow indication which is available in the RUN mode. Figure 3-7 shows the TEST-RUN mode display for an instruction using a discrete point for an operand.

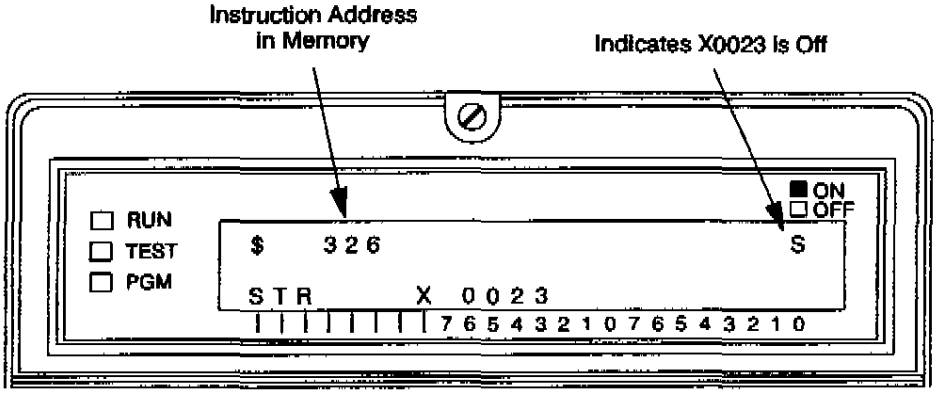


Figure 3-7 Test-Run Mode Instruction Display

If a timer or counter instruction, or contact is displayed in the TEST-RUN mode, its current value is shown continually updating, along with the contact status. Figure 3-8 shows how this display would appear.

This display also shows the power flow status coming into and going out of the instruction operand.

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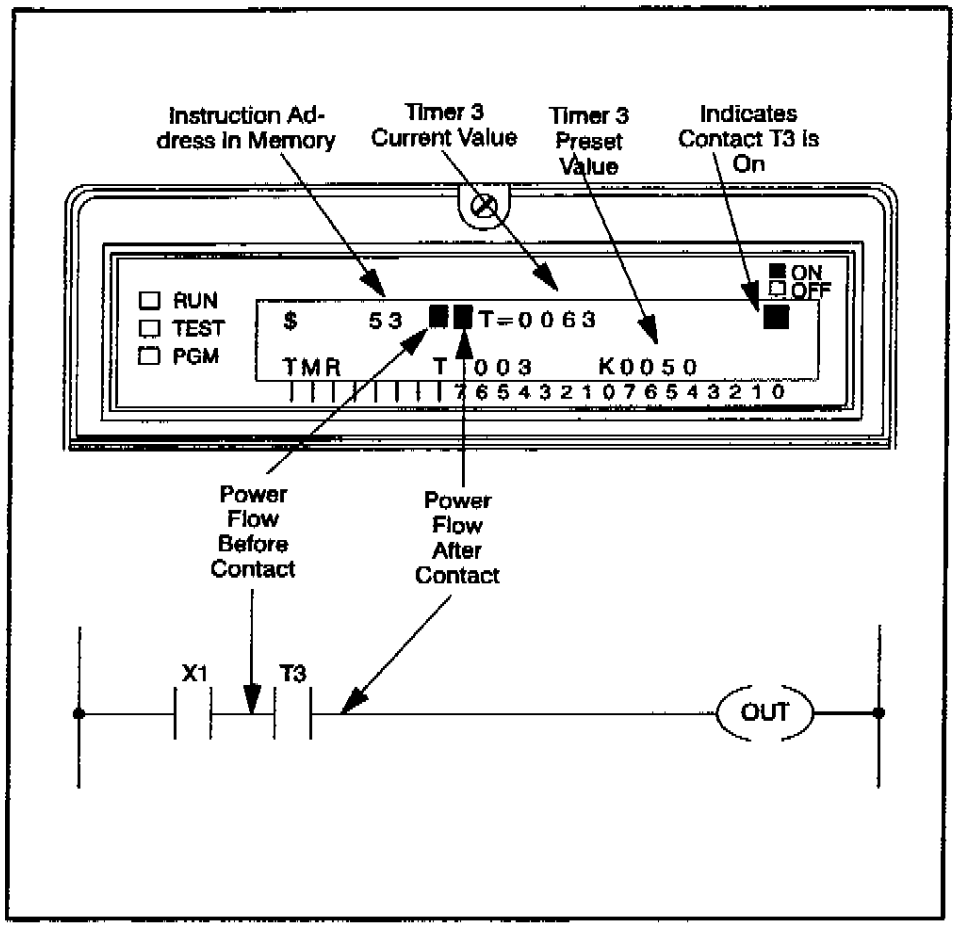


Figure 3-8 Monitoring a Timer

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Holding Output States

In addition to the enhanced MIU displays, the TEST-RUN mode offers another aid for troubleshooting. Each Y output can be individually set to either hold its last state or be forced off when the CPU transitions from TEST-RUN to TEST-PGM. AUX Function 58 is used to select the action for each output. To configure the outputs, from a cleared display press [5] [8] [AUX]. The message in Figure 3-9 is displayed.

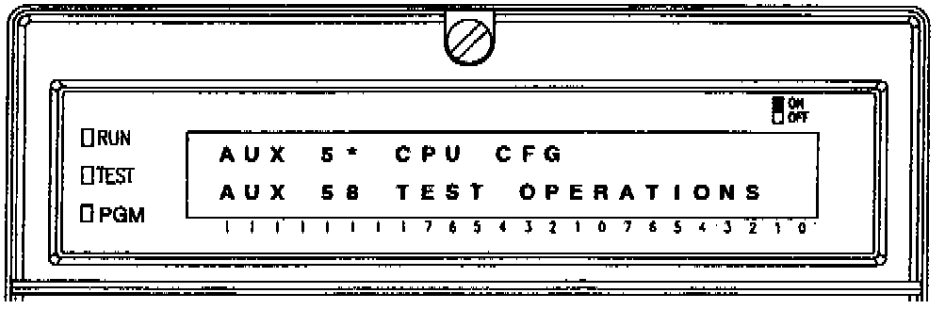


Figure 3-9 AUX 58 Menu Display

Press [ENT] and Y0000 is displayed along with its current configuration. If Y0 is set to be forced off when in TEST-PGM mode, the MIU display shows the message in Figure 3-10.

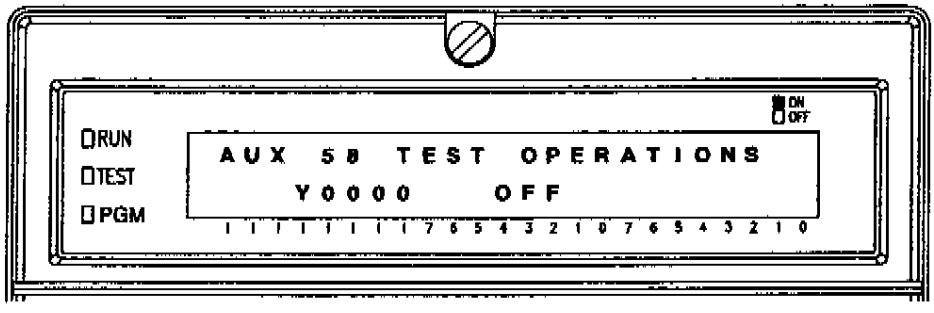


Figure 3-10 Y0000 Configuration Display

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- To configure Y0 so that it holds its last state in TEST-PGM mode, press [SHFT] [ON].
- To configure Y0 back to being forced off, press [SHFT] [OFF]. Use [PREV] and [NXT] to step from Y0 to Y477 in sequence, or you can directly select an output to configure.
- To select Y42, press [CLR] [I/O/UTIL] [4] [2] [NXT].
- To leave AUX 58, press [SHFT] [EXIT].

Holding outputs on while stopping the program scan is an advantage in troubleshooting machine control applications, since it is often desirable to keep some outputs active when the machine is stopped. Outputs connected to cooling pumps, material heaters, mixers, oil pumps, or clamps holding material in work are some of the possibilities that might need to be left in their last state when the PLC controlling the machine is stopped for troubleshooting purposes.

⚠CAUTION

Only qualified personnel, aware of industry standard safety practices, should use these techniques in order to minimize risk of personal injury or damage.

Displaying the Current Scan Time

Two other AUX Functions display useful troubleshooting information on the MIU. AUX 53 displays the current, maximum, and minimum PLC scan time in milliseconds. This is helpful when searching for program timing problems or watchdog timeouts.

Displaying the Firmware Level

AUX 61 displays the MIU and CPU firmware revision numbers, which are needed if a call for technical assistance is made.

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3.5 Self-test Functions for the MIU

Starting the MIU Tests

Several tests can be run from the MIU, both to check MIU operation and to test items in the CPU and I/O system. To test all of the MIU operations, select AUX Function 65 by starting with a cleared display and pressing [6] [5] [AUX] [ENT]. The message in Figure 3-11 is displayed.

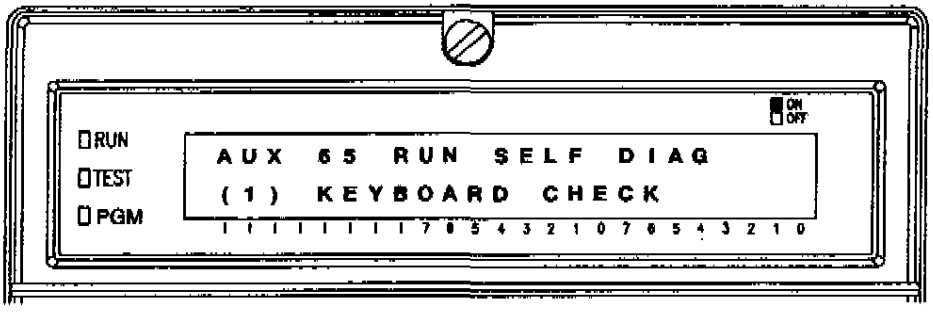


Figure 3-11 Keyboard Check Self-test

Testing the Keyboard

Press [ENT] and the message `PRESS KEY TO TEST-->` is displayed. Pressing any key except [ENT] displays a code associated with that key. For example, pressing [STR] displays the code 10H. Continuing across the top row, each key displays a code that is one greater than the key to its left. Moving down a row increases the displayed code by 10. When you have tested as many keys as you wish, press [ENT] to end the test.

Testing the Display

The next display shows the message `(2) DISPLAY CHECK?`. Press [ENT] and the message `ASCII CODE -->30H=0` should appear. Press [ENT] again to advance to the next test.

Testing the Backlight

The message `(3) LED/BACKLIGHT CHECK?` appears. Press [ENT] and the yellow display backlight flashes on and off along with the three LED indicators to its left. After five or six cycles, this test ends and advances to the next message.

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Testing the Cassette Port

The display `(4) TAPE PORT CHECK?` appears, and if you press [ENT], the direction `INSTALL LOOP-BACK` is displayed. A loop-back connector must be installed on the MIU peripheral port, located on the bottom edge of the MIU, before you proceed. This loop-back connects pin 2 to pin 3 of the port. Once the loop-back is installed, press [ENT] to start the test. The letters A through X are displayed, and when this test ends, the next test choice is offered.

Testing the Memory Cartridge

When `(5) MC OPERATIONS CHECK?` appears, press [ENT] and choose between testing a RAM or UVPROM memory cartridge with the display `MC TYPE (RAM/UVPROM)`. A flashing cursor appears on RAM, and you may use [←] or [→] to move the cursor to the type memory cartridge that is currently installed in the MIU. Refer to Chapter 5 if you need directions for removing or inserting a memory cartridge. Press [ENT] and a `BUSY` message is displayed for about one minute while the test is performed. When this test completes, you are back to the beginning of the test cycle.

Exiting the MIU

To exit the MIU diagnostics, press [SHFT] and [EXIT] anytime a numbered test message, such as `(1) KEYBOARD CHECK?`, is displayed. If any of the tests fail, you will need to replace the MIU.

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Checking the Syntax of a Program

You may also use the MIU to check the program stored in the CPU. Press [2] [1] [AUX] and [ENT] to select AUX Function 21, CHECK PROGRAM. The message `1:SYN 2:DUP REF` is displayed. To check the syntax of your program, press [1] [ENT]. If no errors are found, the message `NO SYNTAX ERROR` is displayed. If you see this message, press [ENT] to continue. If an error was found, the instruction in question is displayed along with an error code. Refer to Appendix C for descriptions of the error codes. Continue to run syntax checks and correct the program until the `NO SYNTAX ERROR` message appears.

Checking for Duplicate References

Another program check may be run from the `1:SYN 2:DUP REF` display. Press [2] and [ENT] to check for multiple use of the same output coil. If a duplication is found, the second occurrence is displayed along with an error message. If no duplication is found, the message `NO DUP REFS` is displayed. Press [ENT] to continue. To exit AUX Function 21, press [SHFT] and [EXIT].

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The MIU may be used to test the I/O system by using AUX Function 42. You are prompted to run AUX 42 whenever an I/O error is detected by the TI405 internal run-time diagnostics, but you may use AUX 42 at any time by pressing [4] [2] [AUX]. The message in Figure 3-12 appears.

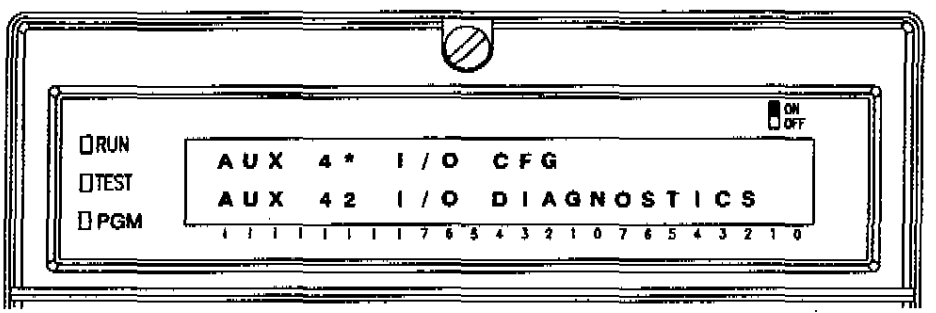


Figure 3-12 AUX 42 Menu Display

Unless you were prompted to run AUX 42 because of a detected error, when you press [ENT], you see the message `I/O CHECK OK`. Otherwise, you see an error message describing the problem, and specifying in what base and slot the module in question is located. A typical error message is shown in Figure 3-13.

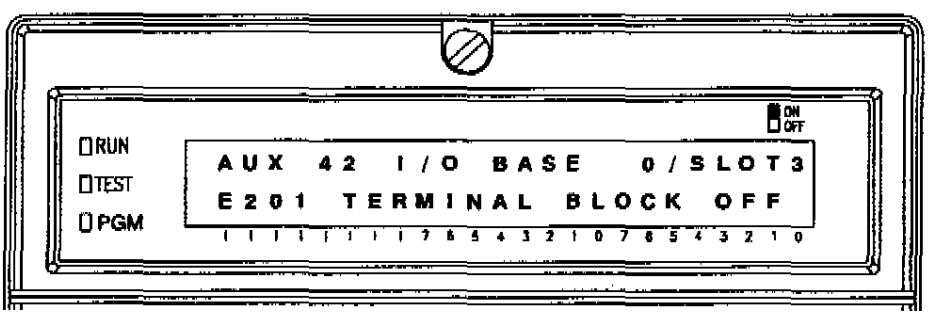


Figure 3-13 Example of an Error Message Display

This example shows that the I/O module in slot 3 of the CPU base has a loose or missing wiring terminal block. If you need further explanation of the displayed error code, refer to Appendix C. To exit AUX 42, press [SHIFT] [EXIT].

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3.8 Forcing I/O Points

I/O points can be forced on or off with the MIU when the CPU is in the RUN or TEST-RUN mode. This is especially useful during startup of a new system, or when repairs have been made and you want to test the operation of certain I/O points.

⚠CAUTION

Only qualified personnel, aware of industry standard safety practices, should use these techniques in order to minimize risk of personal injury or damage.

If there is a program in your TI405 CPU, and the I/O point being forced is used in the program, the point IS controlled by the program and may not stay in the state to which it was forced. Control relays, stages, counters, and timers can be forced as well as physical inputs and outputs, but they are also subject to having their forced state overridden by the program.

I/O points can be forced from a blank display on the MIU, or from the word or bit status displays. The following key sequences demonstrate how to force I/O points.

Key Sequence	Display
X/INS 0 SHIFT ON	X0
C/CTR 4 2 SHIFT ON	C42
Y/OUT 2 5 SHIFT OFF	Y25

Setting the CPU to PGM or TEST-PGM mode returns all points to an Off state.

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3.9 Detecting Failed I/O Modules

I/O Error LED

The TI405 offers several ways to detect failed I/O modules. The CPU has an I/O indicator LED that illuminates whenever a defined I/O problem is detected, as shown in Figure 3-14. This may be caused by certain failures of an individual module, a module being removed from a base, or a module being replaced with one of a different type.

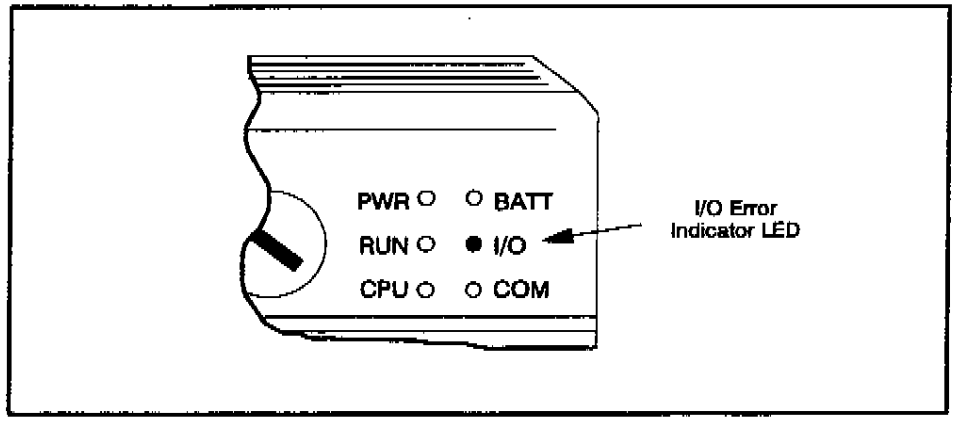


Figure 3-14 CPU Indication of Failed I/O Modules

Terminal Block LED and Fuse LED

Each module has at least one LED labeled TB to indicate that its terminal block is loose or disconnected. Modules with internal fuses have an LED labeled FU to indicate a blown fuse. See Figure 3-15. Modules that use external 24 VDC power supplies have another LED labeled 24 V that illuminates whenever the voltage drops below tolerance.

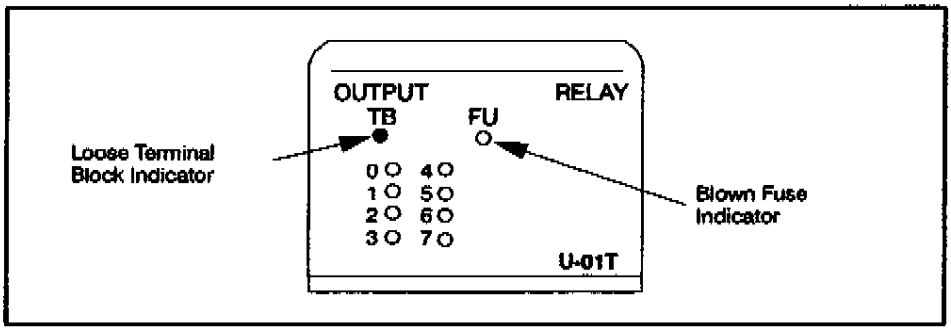


Figure 3-15 Loose Terminal Block and Blown Fuse Indicators

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I/O Error Messages on the MIU

Internal diagnostics in the TI405 also keep a constant watch for defined I/O errors. For example, if a terminal block was not screwed down on the module in slot 3 on the first base and had vibrated loose, the MIU would display the message shown in Figure 3-16.

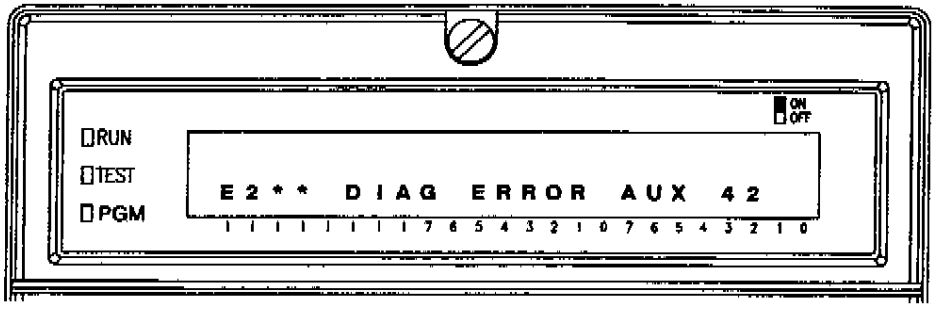


Figure 3-16 Diagnostic Error Message Display

This informs the operator that an error has occurred and that AUX 42 should be run to pinpoint that problem. Running the AUX 42 I/O diagnostics would display the message shown in Figure 3-17. Attention is focused directly on the problem. Similar messages are displayed for other I/O errors.

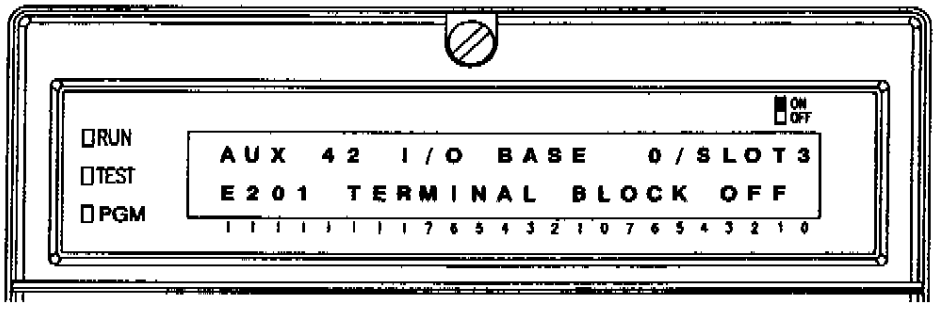


Figure 3-17 AUX 42 Message Display

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Trapping I/O Errors in a Program

The program in the CPU can also monitor defined I/O errors. Special relay SP45 turns on when such I/O errors are detected. Special relay SP40 turns on to indicate a critical error. These contacts can be used in your program to trigger certain actions to help shut down a machine or signal an operator.

The program could also search for more detailed information before taking action by examining location V7756. This V-memory location is set aside to hold critical error codes, and, in this case, would hold the value 201. This indicates that an error 201 has been detected, meaning that an I/O module is missing a terminal strip.

For example, if memory location V7760 contains the value 0003, indicating that the problem is in base 00, slot 03. V7762 holds the value 201, verifying that error 201, missing terminal strip, is causing all the problems. With all this information, the TI405 program can react intelligently to most I/O problems that are detected. Refer to Appendix C for a complete list of TI405 error codes, their meanings and how they are displayed.

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CPU Battery Replacement

The CPU uses a battery to maintain the contents of V-Memory, program memory, and system parameters when power is turned off. Replace this battery at least once every five years.

NOTE: Be sure to save your system parameters and V-Memory to a Memory Cartridge or cassette tape before removing the battery.

1. To remove the battery, grasp the battery between your thumb and forefinger and pull it loose from the retaining clip.
2. Grasp the leads from the battery close to the battery connector with one hand.
3. Grasp the battery connector with the other hand, and gently pull to disconnect the battery.

To install a new battery, connect the battery connector and insert the new battery under the retaining clip. See Figure 3-18.

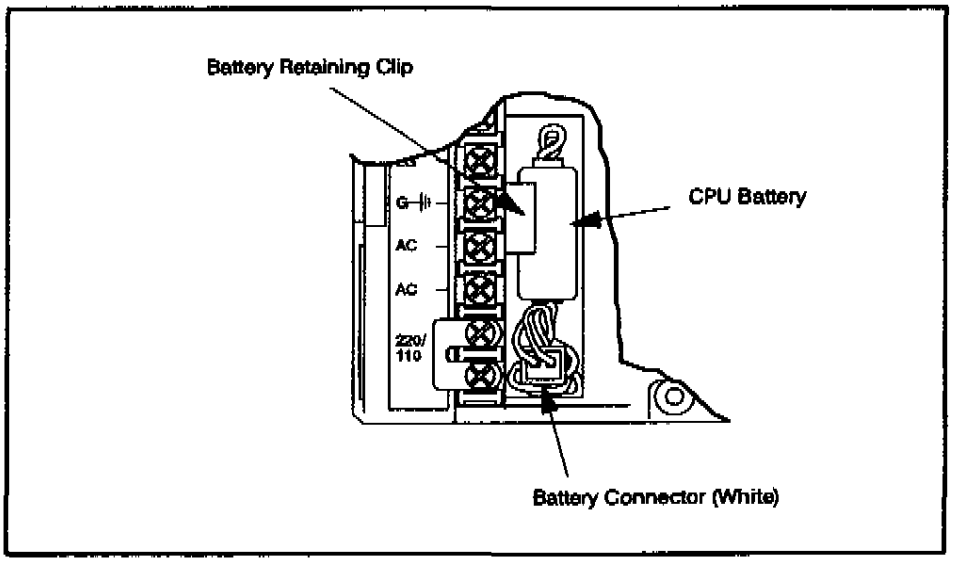


Figure 3-18 CPU Battery Replacement

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Memory Cartridge Battery Replacement

The CMOS RAM Memory Cartridge contains a battery that maintains the contents of the Memory Cartridge RAM when power is turned off. You need to replace this battery at least once every three years.

NOTE: The contents of the memory cartridge should be saved to another cartridge or cassette tape before removing the battery. The current contents of the cartridge are lost when the battery is removed.

1. To replace the battery, remove the cover retaining screw from the bottom of the cartridge as shown in Figure 3-19.
2. Remove the top cover.
3. Using a small flat-blade screwdriver, gently pry the battery up until there is enough clearance to grasp the battery.
4. Grasp the battery between your thumb and forefinger and pull up.
5. To insert the new battery, align the battery leads with holes in the circuit board. The battery leads and circuit board holes are keyed such that the battery can only be inserted one way to ensure the proper polarity.
6. Press firmly on the top of the battery.

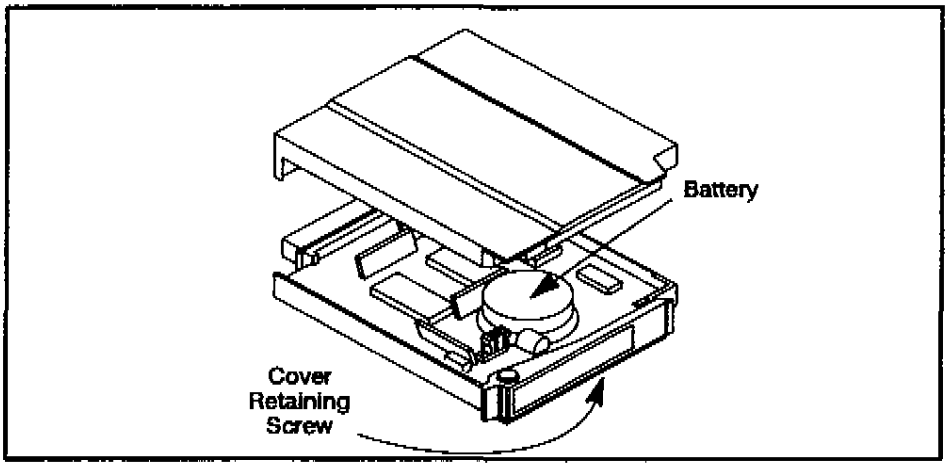


Figure 3-19 Memory Cartridge Battery Replacement

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Chapter 4
Programming the SIMATIC TI405

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4.1 Identifying the MIU Keys

The PPX:S-10P Machine Interface Unit

The PPX:S–10P Machine Interface Unit (MIU), shown in Figure 4-1, is a simplified type of hand-held programming device. It provides you with the ability to enter and edit programs, save and restore programs on data tapes or memory cartridges, control system operation, and monitor system status. The MIU keys are divided into four groups as illustrated in Figure 4-2. Within these groups there are first and second level keys.

- First level keys are functions activated when the key is depressed without preceding it with the shift key.
- Second level keys are the functions activated when the key is preceded by the shift key.

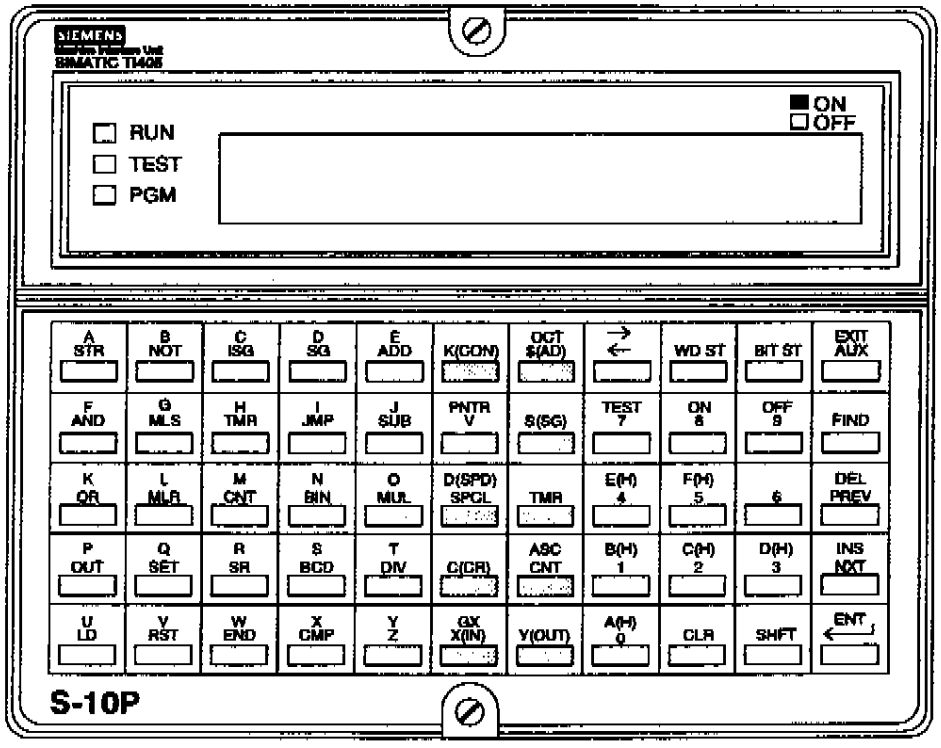


Figure 4-1 The PPX:S–10P Machine Interface Unit

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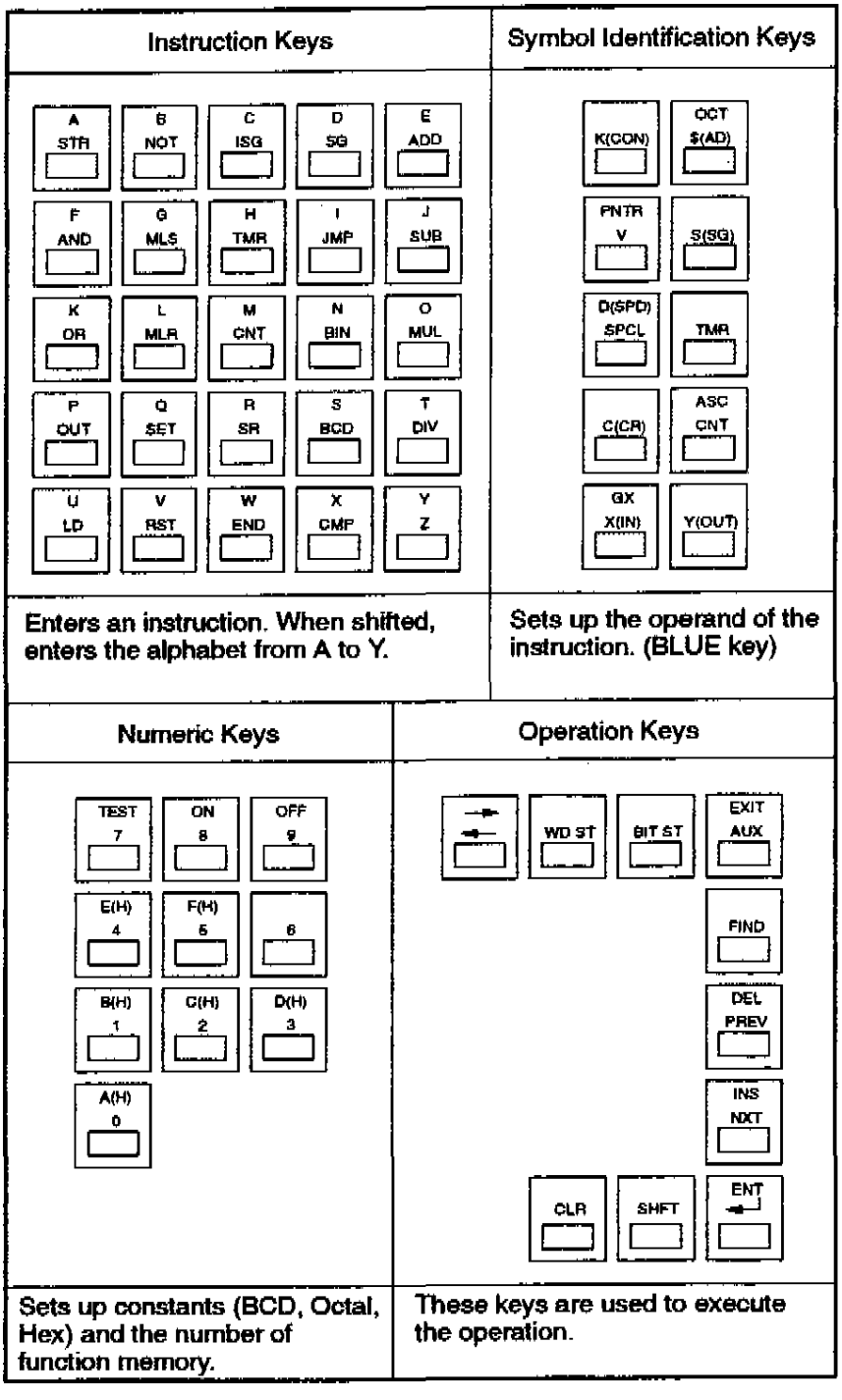


Figure 4-2 MIU Key Groups

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First Level Key Functions

The location of the first-level MIU programmer keys are depicted in Figure 4-3. The basic function of each key is listed in Table 4-1. Shaded keys [ ] represent the blue colored symbol identification keys on the MIU.

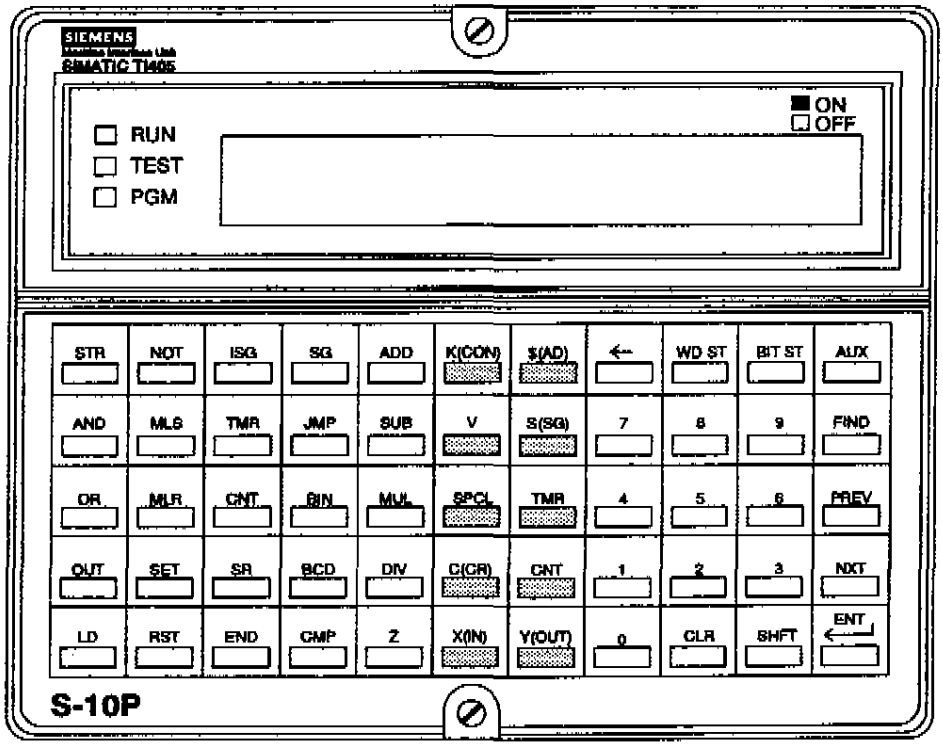


Figure 4-3 First Level MIU Keys (Unshifted)

Table 4-1 First Level MIU Key Definitions

Key	Function
←	Moves the cursor one character to the left
0 - 9	Use to enter a numerical value
$(AD) *	Use to specify an address location the user wants to access
ADD	Initiates an ADD instruction
AND	Initiates an AND instruction
AUX	Selects Auxiliary function
BCD	Indicates Binary Coded Decimal instruction
BIN	Indicates binary instruction

* Shaded keys [ ] represent the blue colored symbol identification keys on the MIU.

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Table 4-1 First-level MIU Key Definitions (continued)

Key	Function
BIT ST	Initiates Bit Status monitoring
C(CTR) *	Selects C (control relay) identifier
CLR	Clears previous entry or blanks display
CMP	Initiates Compare instruction
CNT	Initiates Counter instruction
CNT *	Precedes a counter identification number
DIV	Initiates Divide instruction
END	Initiates unconditional End instruction
ENT	Enters displayed data
FIND	Initiates search function
ISG	Initiates Initial Stage instruction
JMP	Initiates Jump to Stage instruction
K(CONS) *	Precedes number when specifying a constant value
LD	Initiates Load Accumulator instruction
MLR	Initiates Master Line Read instruction
MLS	Initiates Master Line Set instruction
MUL	Initiates Multiply instruction
NOT	Initiates NOT operator
NXT	Displays next data element
OR	Initiates OR instruction
OUT	Initiates OUT instruction
PREV	Displays previous data element
RST	Initiates Reset instruction
S(SEQ) *	Precedes a Stage Identification number
SET	Initiates Set instruction
SG	Initiates any stage except the initial stage
SHFT	Selects the upper level programmer keys
SPCL *	Selects Special Relay identifier
SR	Initiates Shift Register instruction
STR	Initiates STR (store) instruction
SUB	Initiates Subtract instruction

* Shaded keys [ ] represent the blue colored symbol identification keys on the MIU.

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Table 4-1 First-level MIU Key Definitions (continued)

Key	Function
TMR	Initiates Timer instruction
TMR *	Precedes a Timer identification number
V *	Precedes number when specifying a V-memory value
WD ST	Initiates Word Status monitoring
X### *	Selects Input (contact) identifier
Y###(OUT) *	Selects Output (coil) identifier
Z	Alpha character required to enter complex functions

* Shaded keys [ ] represent the blue colored symbol identification keys on the MIU.

Second Level Key Functions

The location of the second-level MIU programmer keys are depicted in Figure 4-4. The basic function of each key is listed in Table 4-2.

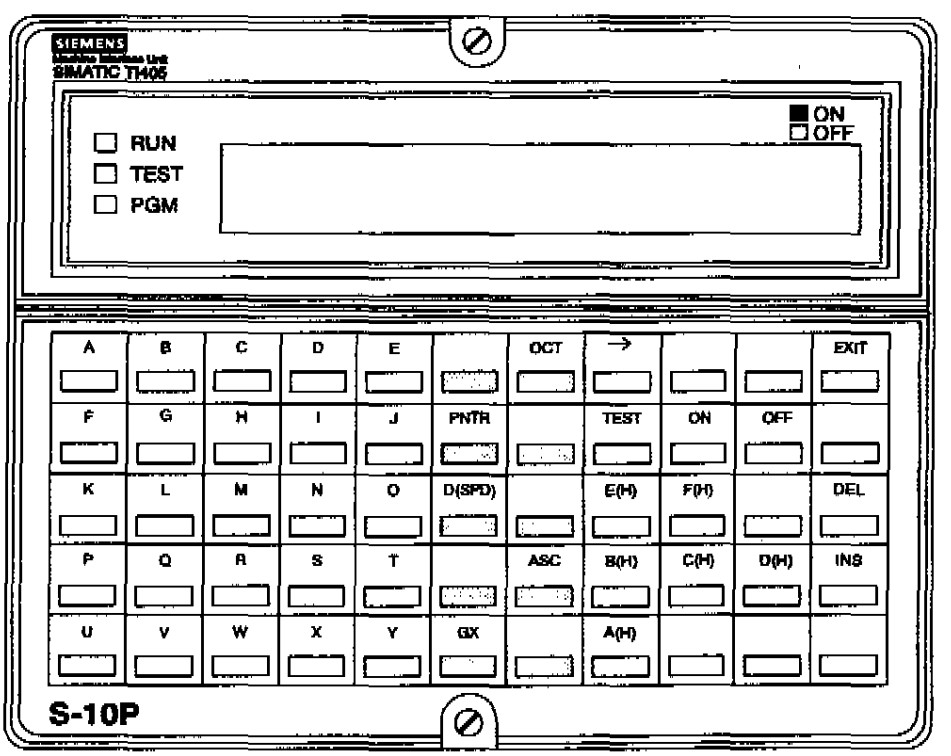


Figure 4-4 Second Level MIU Keys

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Table 4-2 Second-level MIU Key Definitions

Key	Function
→	Moves cursor one character to the right
A - Y	Alpha characters required to enter complex functions
A(0) - F(0)	Used to enter hexadecimal values
ASC *	Selects ASCII data type
DEL	Used prior to ENT to delete a program element
D(SPD)	Precedes number when specifying Scratch Pad Data
EXIT	Exits the auxiliary function menu
GX *	Selects GX (Remote I/O) Identifier
INS	Used prior to ENT to delete a program element
OCT *	Selects octal data type
OFF	Forces selected point Off
ON	Forces selected point On
PNTR *	Indicates a Pointer location for indirect addressing
TEST	Selects scan control in Test Mode

* Shaded keys [ ] represent the blue colored symbol identification keys on the MIU.

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4.2 Entering Programs

Key Sequence Termination

When you enter an instruction, it is held in a buffer until you press [ENT]. The MIU automatically increments to the next address location when you press [ENT]. In the examples in this chapter, the message in the display column is shown before [ENT] is pressed.

Displaying the Program Contents

Press [CLR] [#/ADD] [0] [NXT] or [CLR] [#/ADD] [NXT] or [0] [ENT] or [ENT] to display and step through the contents of your program starting at address zero. If you want to display the contents of a particular program address, enter the program address instead of zero like [CLR] [#/ADD] [2] [1] [3] [0] [NXT].

To look at the next program address, press [NXT]. To look at the previous program address, press [PREV].

Correcting Errors

If you make a mistake by pressing the wrong key, you can correct the error by pressing [CLR], to clear that entry.

Inserting Instructions

Press [PREV] or [NXT] until you reach the instruction in front of which you want to insert another instruction. Enter the key sequence for the instruction, except, instead of using [ENT], press [SHIFT] [INS]. Then press [ENT] to verify the insert.

Deleting Instructions

Press [PREV] or [NXT] until you reach the instruction that you want to delete. Then press [SHIFT] [DEL]. Press [ENT] to verify the delete prompt.

Locating a Specific Instruction

Use [FIND] to locate a specific instruction. For example, to locate the store instruction that stores X100, press [STR] [X/R9] [1] [0] [0] [FIND].

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Searching and Replacing Instructions (TI435 Only)

In addition to the general search function provided by [FIND], the MIU also provides a global search and replace function. This function is provided by AUX menu 22. For example, to change all occurrences of Y0 to Y4, enter the following key sequence.

Key Sequence	Display
[CLR] [CLR] [2] [2] [AUX]	AUX 2* RLL OPERATIONS AUX 22 CHANGE REFERENCE
[ENT]	OLD
[Y/OUT] [0] [ENT]	TO
[Y/OUT] [4] [ENT]	Y0000 ---> Y0004?
[ENT]	REFERENCE CHANGE OK OLD
[SHIFT] [EXIT]	

Formatting Numbers

The MIU accepts all numeric entries without leading zeros. When displayed, all I/O designators and numeric values are shown with leading zeros. Address fields are displayed without leading zeros. The following key sequences illustrate how to enter values in different numeric formats.

To enter the octal value 037.

[V] [2] [0] [0] [0] [WD ST] [SHIFT] [OCT] [3] [7] [ENT]

To enter the ASCII value PT.

[V] [3] [0] [0] [0] [WD ST] [SHIFT] [ABC] [SHIFT] [P] [T] [ENT]

To enter the hexadecimal value A7.

[V] [4] [0] [0] [0] [WD ST] [K/CONS] [SHIFT] [A/H] [SHIFT] [7] [ENT]

Error Codes

The MIU shows all error codes from the PLC as a decimal value with the format EXXX (where XXX represents 3 numeric digits). See Chapter 3 for an explanation of the messages displayed by the MIU.

Range Correction

The MIU checks the range of all entries against the ranges supported by the PLC. If you enter a number that is out of range, the programmer returns an error.

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4.3 Auxiliary Menu Functions

Figure 4-5 shows the auxiliary function menus for the TI405. The auxiliary functions provide operations that do not have a specific MIU key for that operation.

To perform an AUX function, press [AUX] followed by the numeric digits for the function. For example, to rename your program, press: [AUX] [5] [1] [ENT] or [5] [1] [AUX].

If you do not know the number of the AUX function that you wish to execute, press [AUX] and use [PREV] and [NXT] to step through the auxiliary function headings. Pressing [ENT] accesses the functions under the displayed heading.

Pressing [PREV] and [NXT] scrolls through the functions for that heading shown in the shaded boxes. Once the desired AUX function has been found, press [ENT] to execute that function. To exit the AUX menus, press [SHIFT] [EXIT].

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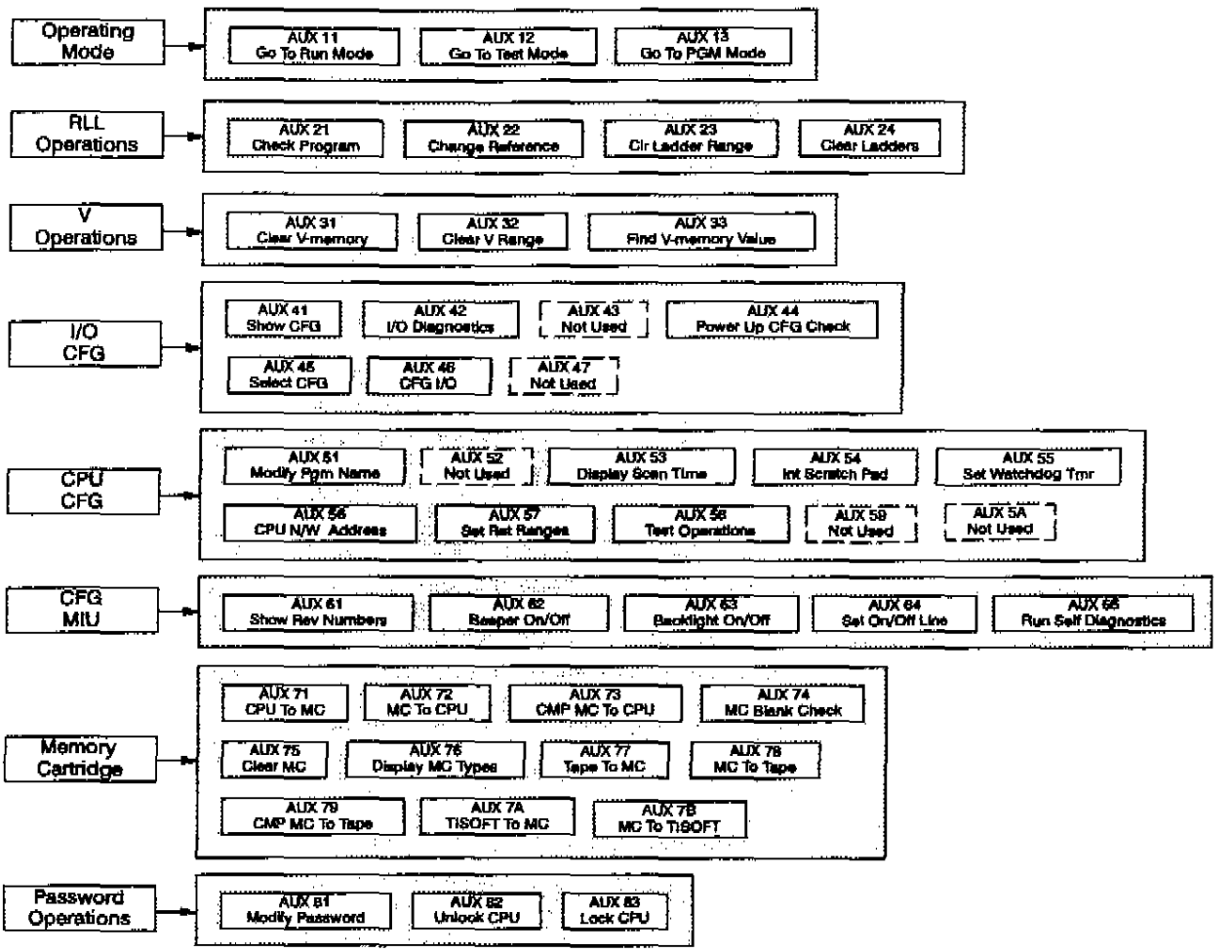


Figure 4-5 AUX Function Menu Hierarchy

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Inserting a Memory Cartridge

To insert a memory cartridge in the MIU, first remove the MIU from the CPU or disconnect the CPU cable from the MIU. Then, open the cover of the left side of the MIU and insert the memory cartridge (as shown in Figure 4-6). Be sure that the memory cartridge is aligned in the same way as Figure 4-6, and that you firmly seat the cartridge.

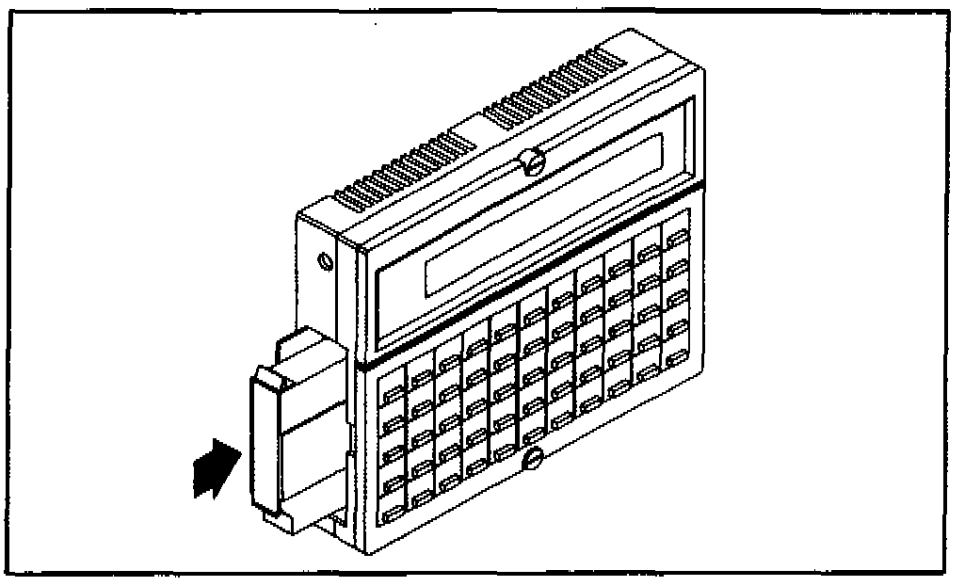


Figure 4-6 Inserting a Memory Cartridge in the MIU

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⚠CAUTION

Do not insert a Memory Cartridge in the CPU while the power is applied to the CPU. Your program or password may be corrupted if this is done.

To insert the memory cartridge in the TI435, remove the left panel cover. Insert the memory cartridge into the cartridge slot, as shown in Figure 4-7. Be sure that the memory cartridge is aligned in the same way as Figure 4-7, and that you firmly seat the cartridge.

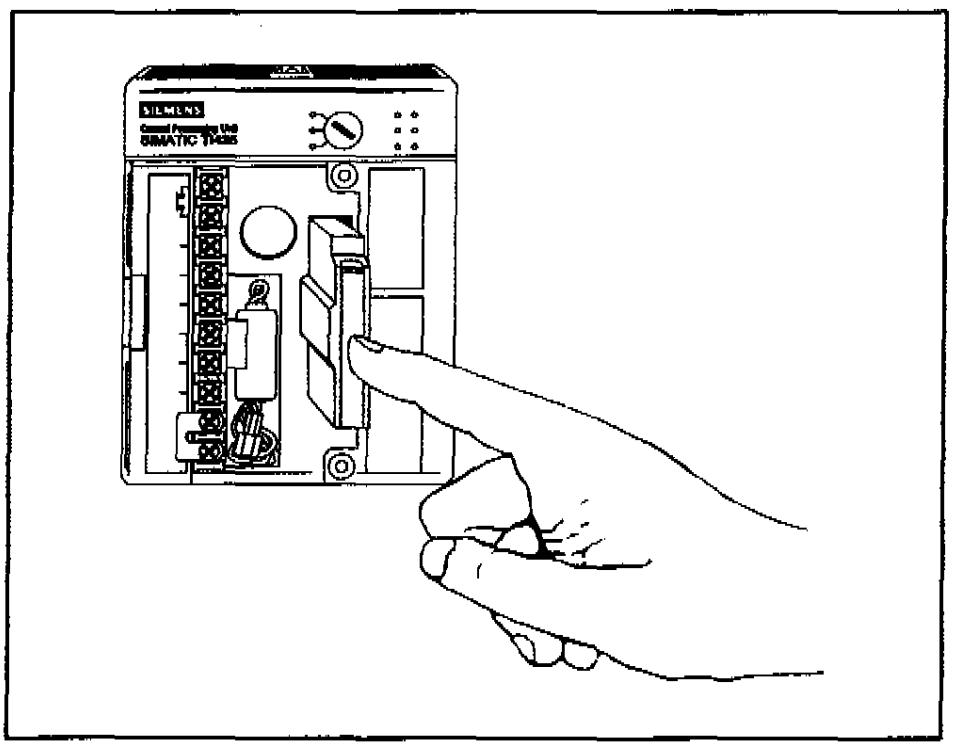


Figure 4-7 Inserting a Memory Cartridge in the CPU

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Removing a Memory Cartridge

To remove the memory cartridge from the MIU, open the cover on the left side of the MIU and gently pull up on the memory cartridge lever. See Figure 4-8. As you pull the lever, the cartridge disconnects from the MIU and becomes loose. You can then pull the memory cartridge out of the MIU as shown in Figure 4-9.

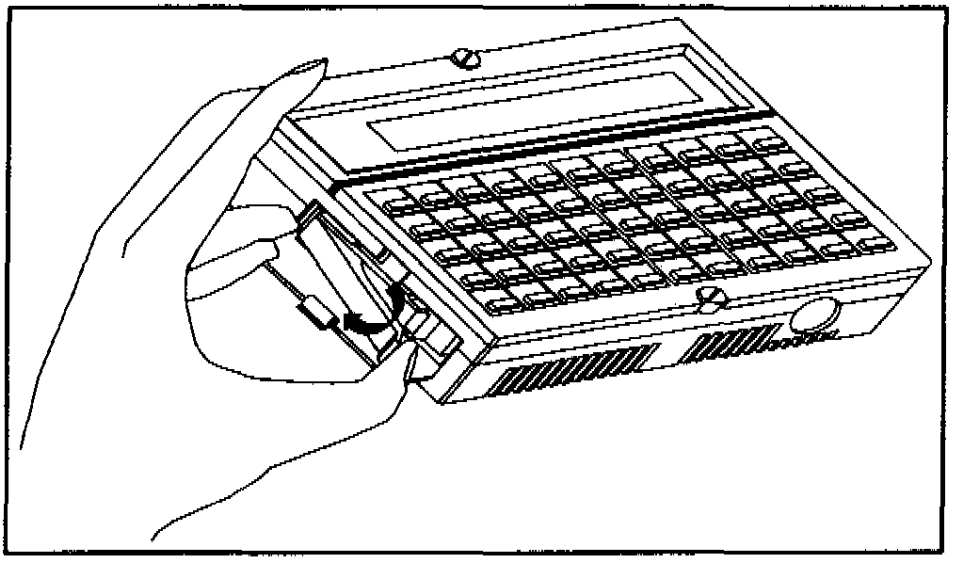


Figure 4-8 Disconnecting the Memory Cartridge from the MIU

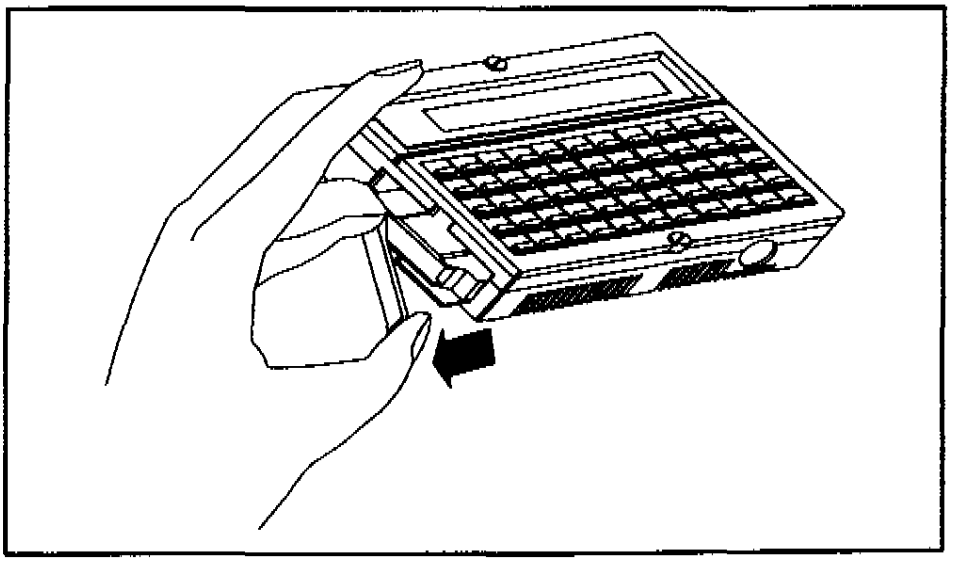


Figure 4-9 Removing the Memory Cartridge from the MIU

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⚠CAUTION

Do not remove a Memory Cartridge from the CPU while the power is applied to the CPU. Your program or password may be corrupted if this is done.

To remove the memory cartridge from the TI435, remove the left panel cover. Then, gently pull out on the cartridge lever until it is disconnected from the CPU. See Figure 4-10. As you pull the lever, the cartridge disconnects from the CPU and becomes loose. You can then pull the memory cartridge out of the CPU as shown in Figure 4-11.

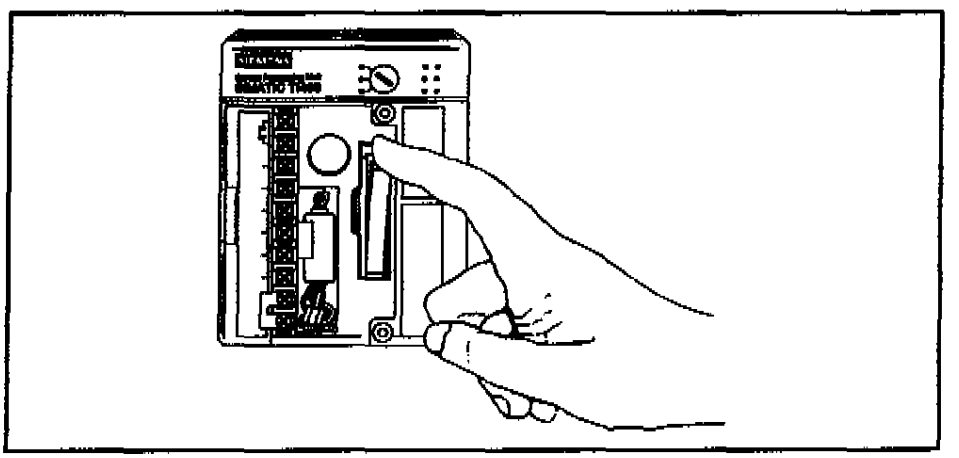


Figure 4-10 Disconnecting the Memory Cartridge from the CPU

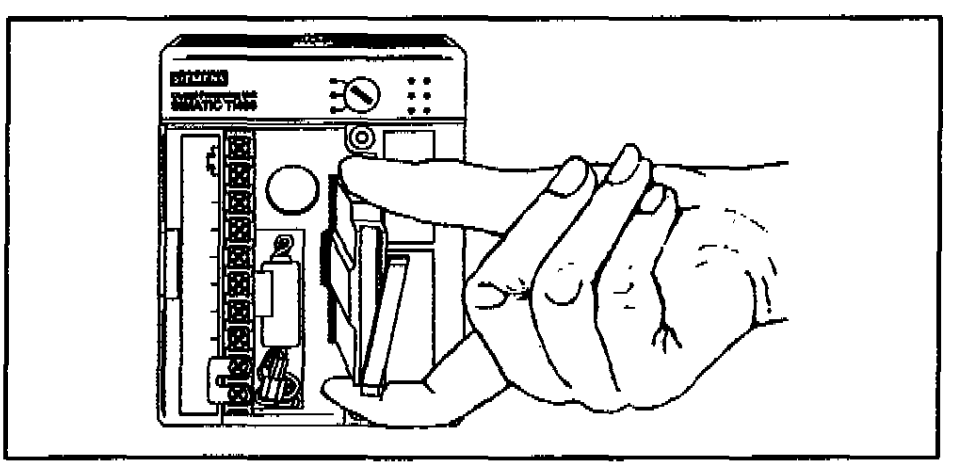


Figure 4-11 Removing the Memory Cartridge from the CPU

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Write-protecting a Memory Cartridge

The CMOS RAM and EEPROM memory cartridges, PPX:G–03M and PPX:G–23M, include a write-protect jumper terminal as shown in Figure 4-12. To write-protect either type of memory cartridge, move the jumper over to pins 2 and 3. To allow programs to be written to the cartridge, move the jumper to pins 1 and 2.

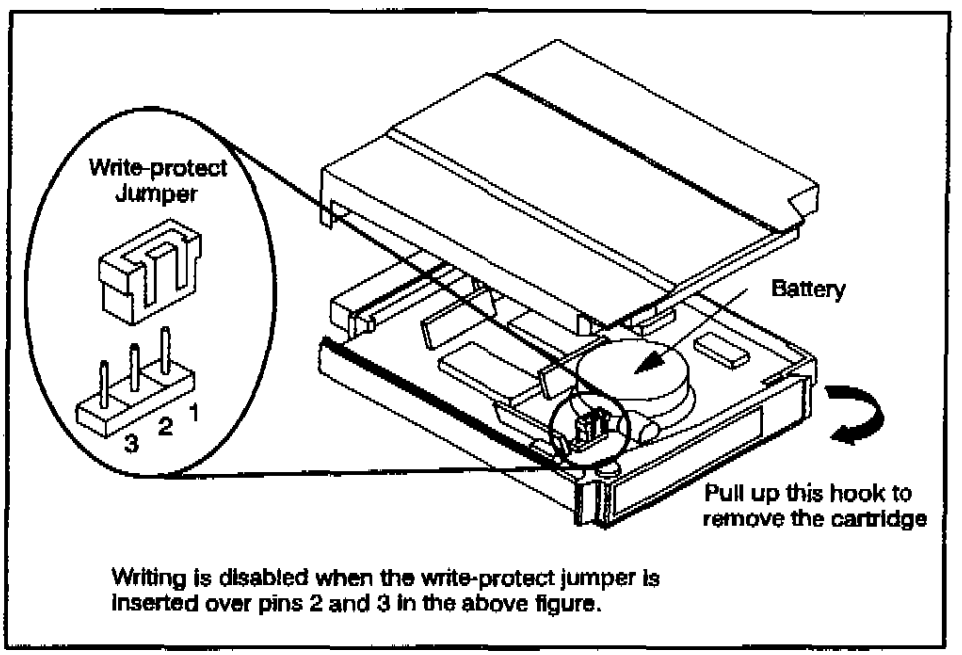


Figure 4-12 Write-protect Terminal on the Memory Cartridge

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4.5 Naming Your Programs

To help you identify your programs, the TI405 CPUs provide a program naming function for programs stored on a Memory Cartridge or cassette tape. This feature is particularly useful with cassette tapes where you can store multiple programs sequentially on a single tape. You are prompted to enter a program name when storing or retrieving a program from cassette tape.

The program name may contain any combination of the alphabetic letters or the digits 0–9. Press [SHFT] before pressing the A–Z keys. You can also store a program name in CPU memory. This name is only a reference to make program identification easier, and does not need to be the same as the program name used when storing to tape. For example, to give a program in the CPU the name MACHINE1, enter the following key sequence.

Key Sequence	Display
[5] [1] [AUX]	AUX 5* CPU CFG AUX 51 MODIFY PGM NAME
[ENT]	AUX 51 MODIFY PGM NAME
[SHFT] [M] [A] [C] [H] [1] [N] [E] [SHFT] [1] [ENT]	PROGRAM MACHINE 1
[CLR]	

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4.6 Using Passwords

The TI435 allows you to set an eight-digit password that can be used to prevent certain operations from being performed. The password must be eight digits and will only accept the 0–9 numeric keys. For example, to set the password to 12345678, press the following key sequence.

Key Sequence	Display
8 1 AUX	AUX 8* PASSWORD OPS AUX 81 MODIFY PASSWORD
ENT	CODE IS 00000000
1 2 3 4 5 6 7 8 ENT	CODE IS 12345678
ENT	

To modify the password to some other value, such as 00004321, press the following key sequence.

Key Sequence	Display
8 1 AUX	AUX 8* PASSWORD OPS AUX 81 MODIFY PASSWORD
ENT	CODE IS 12345678
0 0 0 0 4 3 2 1 ENT	CODE IS 00004321
ENT	

If you decide to stop using the password, it can be cleared by entering a password of eight zeros or 00000000.

Once a password is set, the CPU can be locked using Auxiliary Function 83. Locking the CPU prevents anyone who does not enter the correct password from modifying, copying, or viewing your program.

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Since the password is stored in the memory cartridge, if the cartridge is removed and transferred to another CPU or MIU, the password protection remains in effect. Before locking the CPU, be sure that you remember your password, because once the CPU is locked, you are not able to view your password or program, or erase the memory cartridge and start over. To lock the CPU, enter the following key sequence.

NOTE: Once a password is entered, the CPU is always locked when it is powered up. Accessing most TI405 functions after a power cycle will require unlocking the CPU with the password.

Key Sequence	Display
[8] [3] [AUX]	AUX 8* PASSWORD OPS AUX 83 LOCK CPU
[ENT]	CPU LOCKED – LOCK?
[ENT]	CPU LOCKED
[ENT]	

If no password is set when you attempt to lock the CPU, the message `NO PASSWORD` is displayed. To unlock the CPU, enter the following key sequence.

Key Sequence	Display
[8] [2] [AUX]	AUX 8* PASSWORD OPS AUX 82 UNLOCK CPU
[ENT]	CPU LOCKED – PASSWORD:
[0] [0] [0] [0] [4] [3] [2] [1] [ENT]	CPU UNLOCKED
[ENT]	

If you enter the wrong password, error message `E541 WRONG PWORD` is displayed. Press [CLR] and enter the correct password.

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Retrieving a Program from the CPU

To transfer the program in the CPU to a Memory Cartridge in the MIU, enter the following key sequences.

Key Sequence	Display
CLR AUX 7 1 ENT	AUX 71 CPU TO MC
ENT	1: PG 2: V 3:SYS
1 ENT	1 $00000 The user may enter a selected address instead of zeros.
ENT	END $07679 ($03583 if using TI425 CPU)
ENT	$00000 – $07679? ($03583 if using TI425 CPU) Are you sure?
ENT	If MC is blank, CMOSRAM 08K** ** represents the 8K of memory. The display will count from 00 through 07 twice.
	OK The program successfully transferred from MIU to CPU.
ENT	If MC contains data, AUX 71 CPU TO MC MC IS NOT BLANK
You can either press ENT to continue or SHFT EXIT to cancel the transfer and exit.	

NOTE: If no MC (memory cartridge) is present in the MIU, the MC in the CPU may be physically transferred to the MIU instead of using this procedure.

You can also store the system parameters, which are items such as a non-standard I/O configuration, on the same MC by repeating the procedure selecting option `3:SYS` at the first prompt. If you want to store V-Memory, you will need another MC, then follow the steps above selecting option `2:V` at the first prompt.

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Storing a Program in the CPU

To transfer a program in the Memory Cartridge in the MIU to the CPU, enter the following key sequences.

Key Sequence	Display
CLR AUX 7 2 ENT	AUX 72 MC to CPU
ENT	1: PG 2: V 3:SYS
1 ENT	1 $00000
ENT	END $07679 ($3583 if using TI425 CPU)
ENT	$00000 – $07679 ($3583 if using TI425 CPU) Are you ready?
ENT	CMOSRAM 08K ** ** represents the 8K of memory. The display will count from 00 through 07 twice.
	OK The program successfully transferred from MIU to CPU.

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Storing a Program on Cassette Tape

This procedure lists the steps necessary to store a program in the MIU on a cassette tape. First, connect the DIN connector to the port on the MIU. Next, connect the microphone plug (red connector) to the microphone jack of a data recorder as shown in Figure 4-13. Follow the example below.

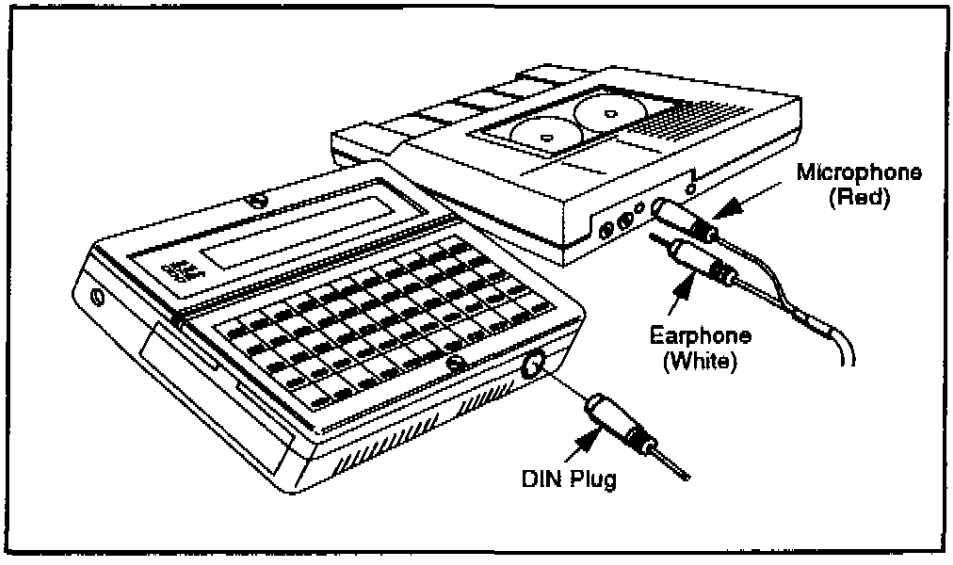


Figure 4-13 Connecting the Cassette Cable

Key Sequence	Display
CLR AUX 7 8 ENT	AUX 78 MC to TAPE
ENT	TAPE NAME:
Here you may enter an optional eight character name for your program. The program name may contain any combination of the alphabetic letters or the digits 0–9. Press SHIFT before pressing the A–Z keys, then press SHIFT again to enter the numeric keys.	

NOTE: If you plan to store several programs on the same tape, you should name each program to allow the correct program to be found when you reload it. Also remember that a tape is a serial access device, meaning that multiple programs are stored on the tape one after the other. It is possible to lose programs by manually positioning the tape at a point that will cause the program to be overwritten or by trying to save an edited program that is larger that the tape version.

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Key Sequence	Display
ENT	`1: PG 2: V 3: SYS`
1 ENT	`1 $00000`
ENT	`END $07679` ($3583 if using TI425 CPU)
ENT	`$00000 -- $07679? START?` ($3583 if using TI425 CPU) `Begin recording?`
ENT (On recorder: **Press Record and Play**)	`BUSY` The program is now transferring. The transfer requires approximately one minute per K of program, up to a maximum of eight minutes.
(On recorder: **Press Stop**)	`OK` The transfer operation has ended. You should now use AUX 79 to compare the program on tape to the program in the MC.

You can also store the system parameters, which are items like a non-standard I/O configuration, on the same cassette tape by repeating the procedure selecting option `3:SYS` at the first prompt. If you want to store V-Memory, follow the example above, selecting option `2:V` at the first prompt. Be sure to use different names for each, such as *SYSPRM6* for the system parameters.

NOTE: Use a Personal Computer type data recorder for storing and retrieving programs. Most audio recorders do not accurately record and playback the digital information. Some data recorders will not operate properly when both the earphone and microphone plugs are inserted. In this case, just remove the plug for the operation that you are not currently performing.

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Retrieving a Program from the Cassette Tape

This procedure lists the steps necessary to retrieve a program from a cassette tape. First, connect the DIN plug of the cassette cable to the MIU. See Figure 4-13. Next, connect the earphone plug (white plug) into the earphone jack of the data recorder. Follow the example listed below.

Key Sequence	Display
Rewind the cassette tape to its beginning or position it at the point just preceeding the program that you want to load.	
CLR AUX 7 7 ENT	AUX 77 TAPE TO MC
ENT	TAPE USED: (If used)
ENT	1: PG 2: V 3: SYS
1 ENT	1 $00000
ENT	$00000 START? (Begin playback?) $00000 BUSY
At this point, set the tone control of the recorder at midway and turn the volume control to its off setting.	
ENT (On recorder: **Press Play**)	*
After the recorder is placed in the "Play" mode, increase the volume until the "*" symbol appears in the lower right corner of the MIU display. If the volume is too high, the star will disappear. Try to adjust the volume to the midrange of these two points. The transfer allows ten seconds for this adjustment.	
	PGM FOUND The program is being transferred to the MIU.
(On recorder: **Press Stop**)	OK The program successfully transferred from the tape to the MIU.

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Storing a Program in an EEPROM

The TI405 CPU provides you with the capability of storing your programs on electrically erasable programmable read-only memory, also called EEPROM. Once a program is written to EEPROM, no battery is needed to retain the program in memory, and the program cannot be modified.

NOTE: The program must be completely erased from the EEPROM before another program can be stored in it.

The EEPROM cartridge must be inserted into the MIU as shown in Figure 4-6, before a program is stored from the CPU. To transfer and store a program in EEPROM, enter the following key sequence.

Key Sequence	Display
[7] [1] [AUX]	AUX 7* MEM CARTRIDGE AUX 71 CPU TO MC
[ENT]	1:PGM/2:V/3:SYS
[1] [ENT]	1st $00000
[ENT]	END $07679 ($03583 if using TI425 CPU)
[ENT]	$00000 – $07679?
[ENT]	If the EEPROM is blank, EEPROM 08K ** **represents the 8K of memory. The display will count from 00 to 07 twice.
[ENT]	OK If the EEPROM contains data, AUX 71 CPU TO MC MC IS NOT BLANK

When the program is stored on EEPROM, you can remove the cartridge from the MIU as shown in Figure 4-8 and Figure 4-9, then insert it into a TI435 CPU as shown in Figure 4-7. If a TI425 program was stored on a EEPROM cartridge, you must transfer it from the MIU to another TI425 using the procedure described earlier in this Chapter.

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Erasing the EEPROM Program

To erase the program from the EEPROM, enter the following key sequence.

Key Sequence	Display
7 5 AUX	AUX 7* MEM CARTRIDGE AUX 75 CLEAR MC
ENT	CLEAR MC?
ENT	BUSY
CLR	MC CLEARED

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Storing a Program in a UVPROM

The TI405 provides you with the capability of storing your programs on ultraviolet erasable programmable read-only memory, also called UVPROM. Once a program is written to UVPROM, no battery is needed to retain the program in memory, and the program can not be modified. The program must be completely erased from the UVPROM before another program can be stored in it.

The UVPROM cartridge must be inserted into the MIU as shown in Figure 4-6, before a program is stored from the CPU. To transfer and store a program in UVPROM, enter the following key sequence.

Key Sequence	Display
7 1 AUX	AUX 7* MEM CARTRIDGE AUX 71 CPU TO MC
ENT	1:PGM/2:V/3:SYS
1 ENT	1st $ 00000
ENT	END $ 07679 ($03583 if using TI425 CPU)
ENT	$ 00000 - $ 07679?
ENT	If the UVPROM is blank, UVEPROM 16K ** ** represents the 8K of memory. The display will count from 00 to 07 twice.
ENT	OK If the UVPROM contains data, AUX 71 CPU TO MC MC IS NOT BLANK

When the program is stored on UVPROM, you can remove the cartridge from the MIU as shown in Figure 4-8 and Figure 4-9, then insert it into a TI435 CPU as shown in Figure 4-7. If a TI425 program was stored on a UVPROM cartridge, you must transfer it from the MIU to another TI425 using the procedure described earlier in this Chapter.

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Erasing the UVPROM Program

To erase the program from the UVPROM, remove the retaining screw from the bottom of the cartridge, and remove the top cover from the cartridge, as shown in Figure 4-14. Place the bottom half of the cartridge, with the windows on the UVPROM ICs facing up, in a commercially available UVPROM erasing unit. It normally takes 20 to 30 minutes of exposure to fully erase the program, but this may vary according to the erasing unit. Read the documentation or manual for recommended erasing times.

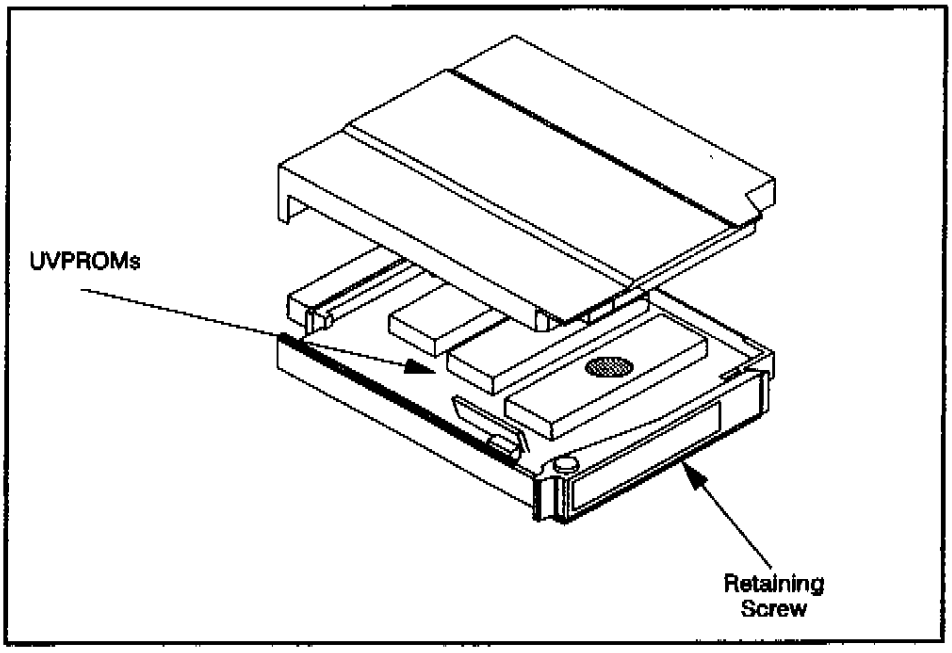


Figure 4-14 Removing the Memory Cartridge Cover

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Specifying a V-Memory Address

V-Memory (variable memory) is the collective area consisting of 16-bit words that store the values for timers, counters, and others. V-Memory addresses are specified in octal numbers like V7746. The CPU memory map, shown in Figure 4-16, lists the specific addresses for the various data types.

The double-word instructions (e.g. ADDD and MULD) use two consecutive V-Memory locations for the operand. You specify the first location, V7746, and the CPU assumes the next location, or V7747, as the next 16-bit value. The first V-Memory location is the low-order 16 bits of the 32-bit double-word and the second location is the high-order 16 bits. See Figure 4-15.

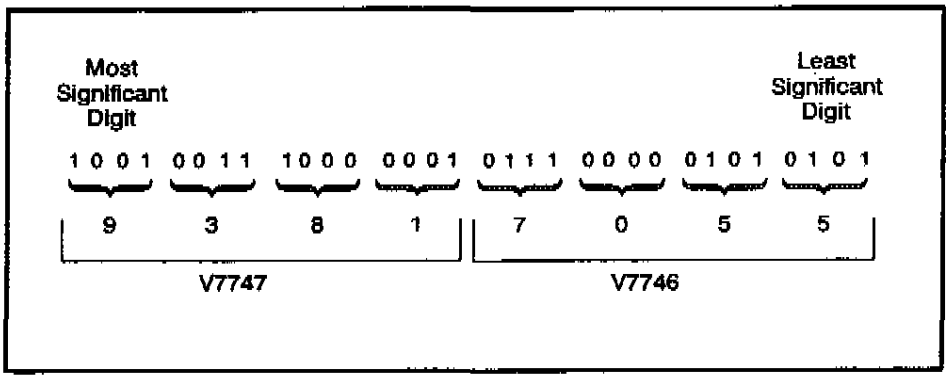


Figure 4-15 32-bit Double Word Format

Interpreting V-Memory Contents

Figure 4-15 illustrates how to interpret a 32-bit double word as eight BCD digits. Address V7746 holds the lower four digits and address V7747 holds the upper four digits. If you use one of the 16-bit instructions, you could interpret V7746 and V7747 as two four-digit BCD values.

You can also treat the contents of the locations as binary values by using one of the binary instructions to process its value. The instruction that you use to process the V-Memory address determines how the CPU interprets that location's contents.

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4.9 Memory Map and Register Layout

All program references to Timers, Counters, V-Memory addresses, and other operands are specified with octal addresses as shown in Figure 4-16.

Operands	Quantity	Octal Numbering	V-memory Octal Word Address
Timer – Tn n	128	T0-T177	V00000-V00177
Counter CNT: PRE:	128	CT0-CT177	V01000-V01177
User Data (V-memory) V01400	3072	V01400-V07377	V01400-V07377
System Parameters V07400	256	V07400-V07777	V07400-V07777
Remote Inputs/Outputs GX GX -| |- -( )-	512	GX0-GX777	V40000-V40037
Inputs X -| |-	320	X0-X477	V40400-V40423
Outputs Y -( )-	320	Y0-Y477	V40500-V40523
Control Relays C -| |-	480	CR0-CR737	V40600-V40635
Stages 001	384	S0-S577	V41000-V41027
Timer Relays T: -| |-	128	T0-T177	V41100-V41107
Counter Relays CT: -| |-	128	CT0-CT177	V41140-V41147
Special Relays SP -| |-	96 192	SP0-SP137 SP320-SP617	V41200-V41205 V41215-V41230

Figure 4-16 TI425/TI435 Memory Map

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Several V-Memory locations are used by the CPU to store diagnostic information and system parameters.

Communications Error—When a communications error occurs, the CPU stores the base and slot numbers of the faulty communications module in V-memory address V7746 and the error code in V-memory address V7747.

User Defined Diagnostic Error—When a user defined FAULT instruction executes, the CPU stores the four-digit code in V-memory address V7751. If a numeric error code was used with the FAULT instruction, that code is stored at V7751. If an ASCII message was used, the data label (DLBL) reference number of that message is stored in V7751.

I/O Configuration Error—The module identification code at V-memory address V7752 identifies the conflicting modules, the code at V7753 identifies correct modules, and V7754 identifies base/slot conflicts. When a module differing from arrangement data registered is detected while the PLC is switched on and is running, the lowest base number and slot number are displayed in hexadecimal form.

System Errors—System error diagnostics identify errors and their severity. Self-diagnostic error codes at V7755, V7756, and V7757 classify errors as fatal, major, and minor, respectively.

Module Error—A code showing the base and slot location of the problem module is stored at memory location V7760. V-memory address V7762 contains the error code that identifies the problem type.

Syntax Check—V-memory address V7763 identifies the location of a syntax error in the program code when the CPU is switched to RUN mode, or the AUX 21 Program Check is run. V-memory address V7764 contains the error code that identifies the problem type.

Scan Counter—A tally of the number of program scans performed since starting the RUN mode is kept at V-memory address V7765.

Scan Time—The current scan time is stored at V-memory address V7775. The minimum scan time since the start of the RUN mode is in V-memory address V7776, and maximum scan time is in address V7777.

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4.10 Setting Retentive Memory Ranges

Selecting Ranges

You may select the ranges of memory that retain their previous states or values after CPU power has been cycled by using Auxiliary Function 57. The types of memory that can be selected are control relay status (C), V-memory (V), timer contact status (T), counter contact status (CT), and stage status (S).

The operation of retentive and non-retentive control relays is illustrated in Figure 4-17 and Figure 4-18.

The starter circuit shown in Figure 4-17 requires a manual start. The normally open push button #1 must be pressed. In the event of a power loss, manual restart is required. The equivalent RLL design, built with non-retentive control relays, functions the same way.

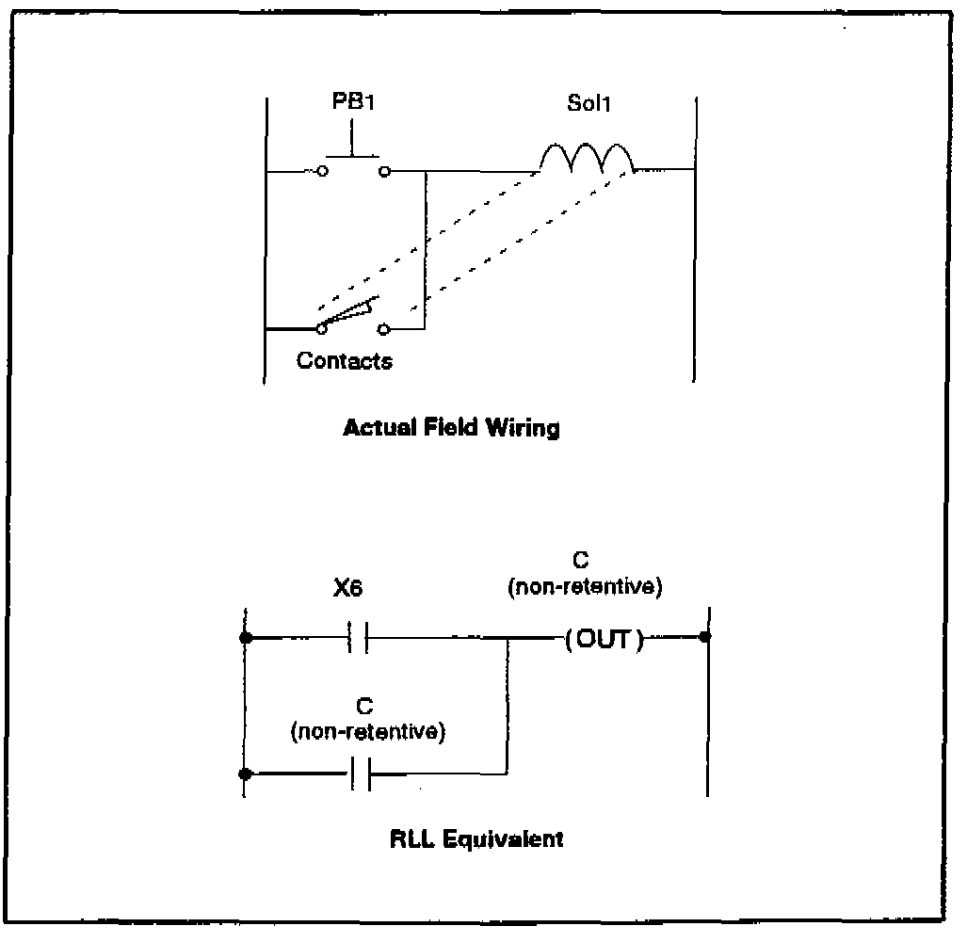


Figure 4-17 Operation of Non-retentive Control Relays

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The starter circuit, shown in Figure 4-18, requires a manual start – but, in the event of a power loss, restart occurs automatically. Push button #2 breaks the circuit. The equivalent RLL design, built with retentive control relays, functions the same way. When built with non-retentive control relays, the RLL circuit requires a manual re-start after a power loss.

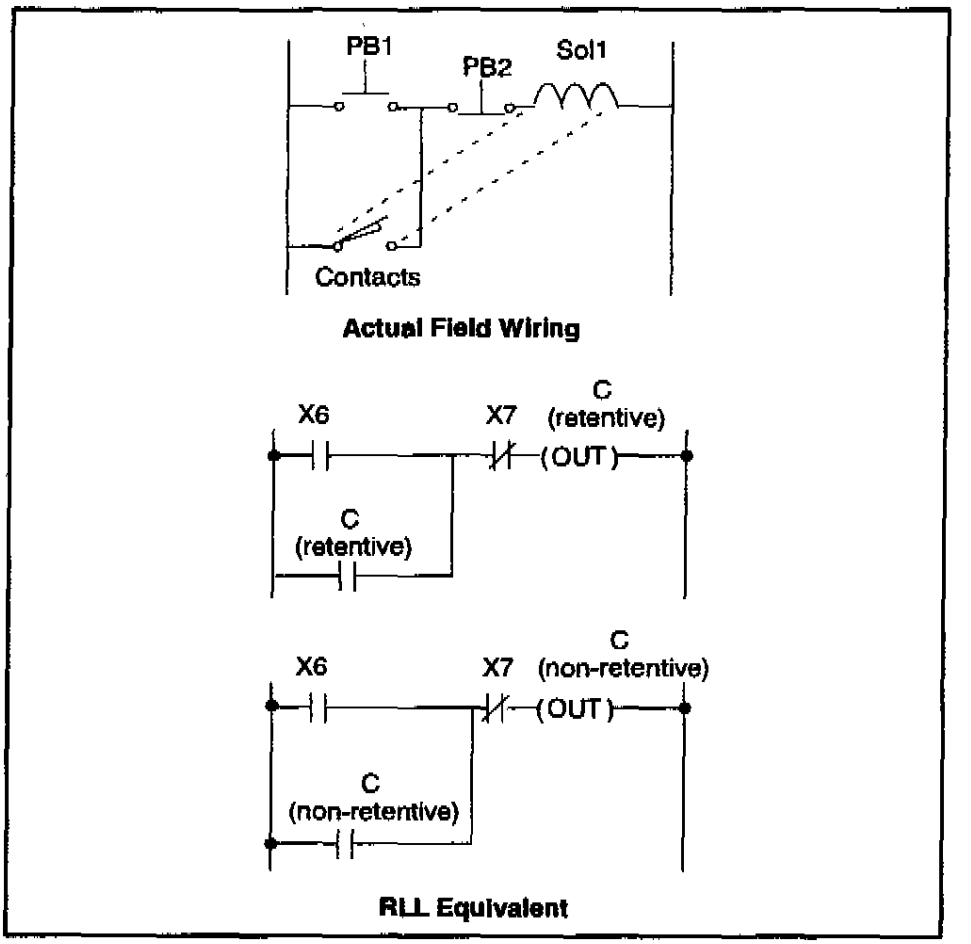
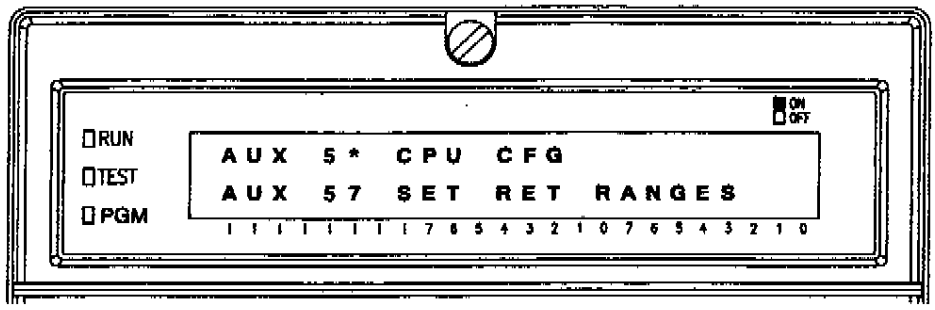


Figure 4-18 Operation of Retentive and Non-Retentive Control Relays

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Setting Retentive Memory

When AUX 57 is selected by pressing [5] [7] [AUX], the following display appears on the MIU.



Pressing [ENT] advances you to the display to set your retentive control relays. If no retentive control relays are presently set, you see the following display. Table 4-3 lists the default retentive ranges for the different operands.

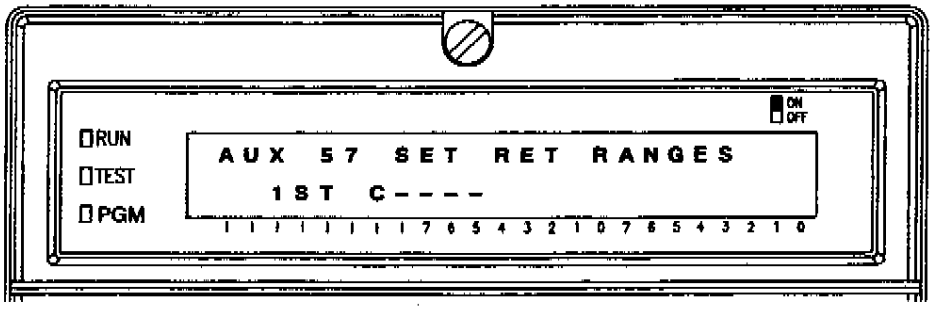


Table 4-3 Default Retentive Memory Ranges

Operand Type	Default Retentive Range
Control relays (C)	C600 – C737
V-memory (V)	V2000 – V7377
Timers (T)	No retentive timers
Counters (CT)	CT0 – CT177
Stages (S)	No retentive stages

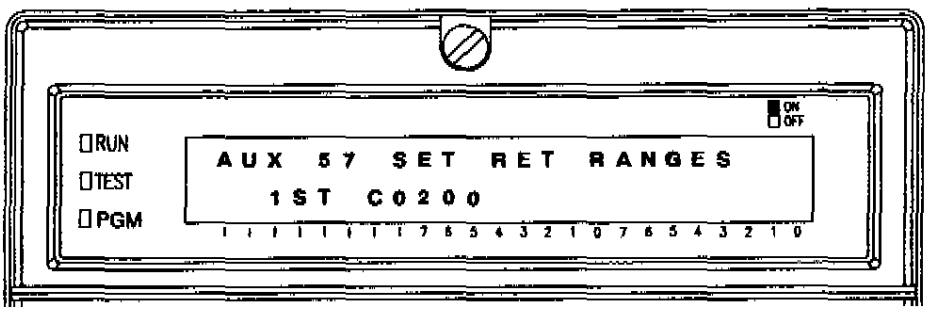
Using a UVPROM cartridge (PPX: G–14M) in a TI405 controller results in default retentive memory ranges as shown in Table 4-3. Control relays and other functions outside these ranges are non-retentive.

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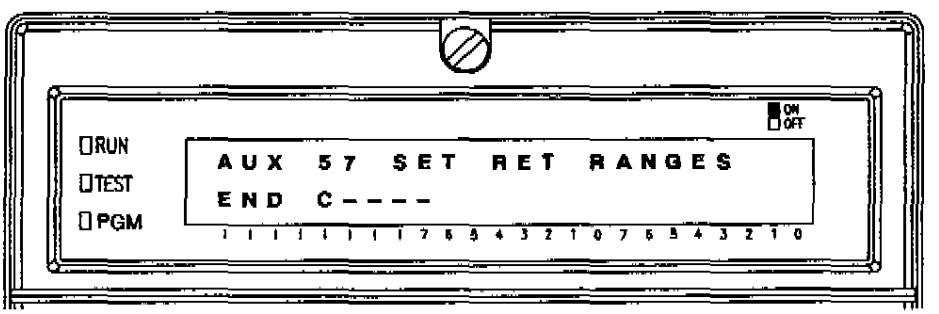
⚠WARNING

To help avoid potential property damage or personal injury, assure that control relays or other critical functions that are normally non-retentive are not assigned to retentive memory locations. Failure to observe retentive memory ranges could result in personal injury or equipment damage.

If C200 had previously been selected as the first retentive control relay, you would instead see this display.



In either case, to enter a new starting value for the range of retentive control relays, enter the control relay number and press ENT. To retain the current starting value, just press ENT. You then see the end of the retentive control relay range displayed as shown below.



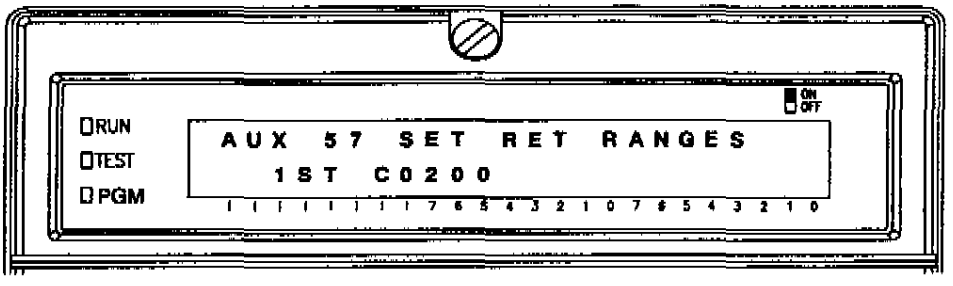
Either enter a new ending value, or, just press ENT, to retain the current value. If you entered a starting value, you must enter an ending value or retain a valid current value. Otherwise, **E504 BAD REF/VAL** is displayed.

Proceed from setting the control relay range through V-memory, timers, counters, and stages, in order. You cannot change one specific group unless you step through each of them in this order. If you do not wish to change a particular range, step through it by pressing ENT twice.

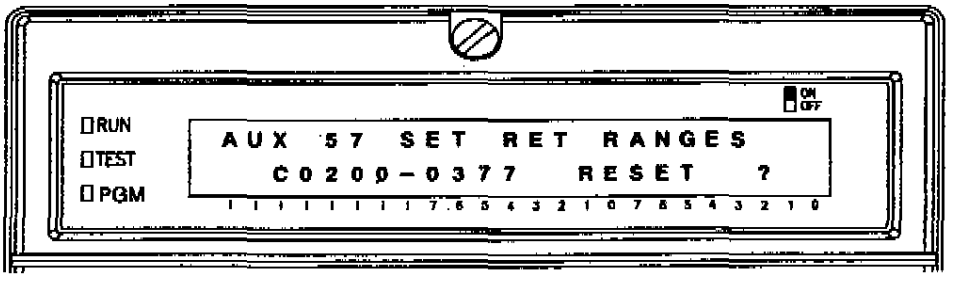
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All ranges, except V-memory, must be set on even eight-bit boundaries, such as 0 through 7 or 100 through 147. If you do not specify an even number of locations, the MIU adjusts the starting and ending locations for you, in order to include your selected locations within a properly sized range.

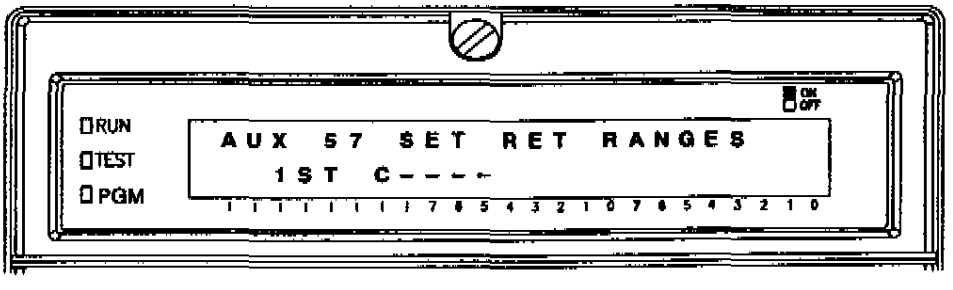
To reset any range of retentive values and make the group completely non-retentive, press [SHFT] [DEL] while either the starting or ending value of that group is displayed. For example, to switch from having C200 through C377 retentive to having all control relays non-retentive, first display the following.



Press [SHFT] then [DEL], and the following display appears.



Press [ENT] and you see this display.



Press [ENT] twice to retain all control relays as non-retentive.

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Chapter 5

Relay Ladder Logic Programming

5.1 Programming Guidelines **5-2**

5.2 Entering Common Ladder Logic Networks **5-3**

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5.6 Calculating Scan Time **5-13**

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5.1 Programming Guidelines

To program your PLC with the MIU, you must enter only complete networks. Use the following general guidelines illustrated in the programming examples in this chapter.

- Use **STR** to begin each network that contains multiple elements.
- Use **STR** to begin a network segment that has parallel branches.
- Use **STR** at the beginning of each branch that contains contacts in series.
- Use **AND** to join one element in series with a previous element or group of elements.
- Use **AND STR** to combine a group of elements in series with a previous element or group of elements.
- Use **OR** to join one element in parallel to a previous element or group of elements.
- Use **OR STR** to combine parallel branches that began with a **STR** instruction.
- Use at least one output (X, Y, or C) or box instruction at the end of each network.
- Press [Enter] when you have entered an element in a network.

The MIU programmer buffers the key sequences until you press [Enter], then it checks to be sure that the instruction is legal and can be compiled without error.

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5.2 Entering Common Ladder Logic Networks

Entering a Simple Network

Each network containing contacts and coils must begin with a STR instruction and end with at least one output (X, Y, C, or GX) or box instruction. The example in Figure 5-1 and other examples in this chapter assume that this is a new program and illustrate how the programmer handles the display of the instructions.

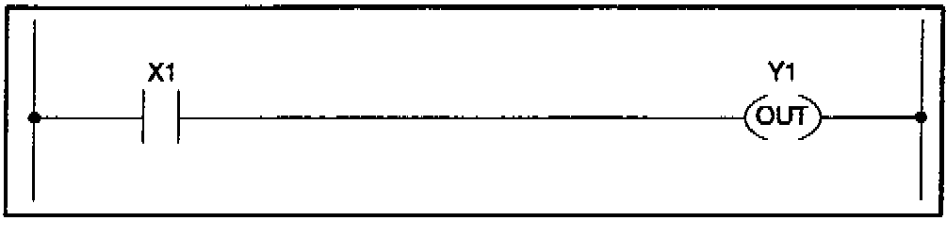


Figure 5-1 A Simple Network Example

Table 5-1 Key Sequence for a Simple Network

Key Sequence	Display	Description
CLR	(Display blank)	Begin with CLR key.
S(ADD) NXT	NOP	Go to the first address.
STR X(INS) 1 ENT	STR X1	Begin the network with STR.
OUT Y(OUT) 2 ENT	OUT Y2	End the network with an output.
END ENT	END	Then end the program.

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Entering Contacts in Series (AND)

To combine a single element in series with the previous element(s), use the AND instruction as shown in Figure 5-2.

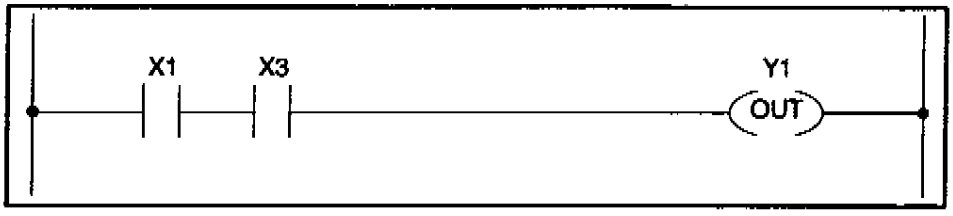


Figure 5-2 Entering Contacts in Series (AND)

Table 5-2 Key Sequence Using AND

Key Sequence	Display	Description
CLR	(Display blank)	Begin with CLR key.
READ NXT	NOP	Go to the first address.
STR X/Y/M 1 ENT	STR X1	Begin the network with STR.
AND X/Y/M 3 ENT	AND X3	Join X3 in series with X1.
OUT Y/OUT 1 ENT	OUT Y1	End the network with an output.
END ENT	END	Then end the program.

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Entering Series Branches in Parallel (OR STR)

The example in Figure 5-3 contains three branches. The instructions are used for the following reasons.

- The first branch A begins with a **STR** because it is the beginning of a network as well as the beginning of a set of parallel branches.
- The second branch B uses the **OR** instruction because it contains only one element.
- The third branch C begins with the **STR** instruction because it contains a series of elements.
- The **OR STR** instruction combines branch C with B.

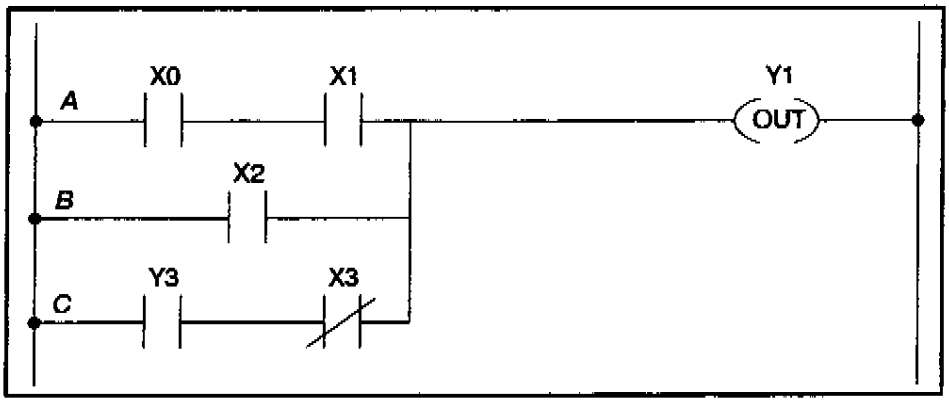


Figure 5-3 Entering Series Branches in Parallel (OR STR)

Table 5-3 Key Sequence Using OR STR

Key Sequence	Display	Description
CLR	(Display blank)	Begin with CLR key.
HARD NXT	NOP	Go to the first address.
STR X/GRP 0 ENT	STR X0	Begin branch A with STR.
AND X/GRP 1 ENT	AND X1	Join X0 in series with X1.
OR X/GRP 2 ENT	OR X2	Begin branch B by joining X2 in parallel with branch A.
STR Y/OUT 3 ENT	STR Y3	Begin branch C with STR.
AND NOT X/GRP ENT	ANDN X3	Join NOT X3 in series with Y3.
OR STR ENT	OR STR	Join branch C in parallel with X2.
OUT Y/OUT 1 ENT	OUT Y1	End the network with an output.
END ENT	END	Then end the program.

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Entering Parallel Contacts In Series (AND STR)

Figure 5-4 contains a program segment with the parallel contacts X0 and X1. To begin this group of parallel contacts, use the STR instruction as shown in Step 4. To combine the group of parallel contacts with the previous element (X2), use the AND STR instruction as shown in Step 6.

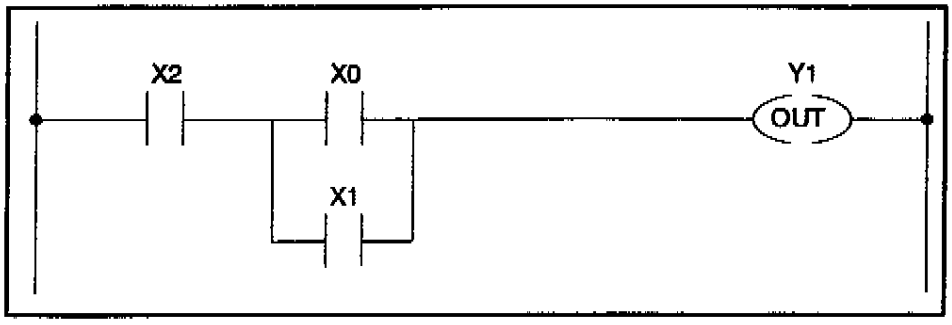


Figure 5-4 Entering Parallel Branches

Table 5-4 Key Sequence Using AND STR

Key Sequence	Display	Description
CLR	(Display blank)	Begin with CLR key
READ/ NXT	NOP	Go to the first address
STR X/WR 2 ENT	STR X2	Begin the network with STR
STR X/WR 0 ENT	STR X0	Begin the parallel segment with STR
OR X/WR 1 ENT	OR X1	Join X1 in parallel with X0
AND STR ENT	AND STR	Join the parallel segment in series with X2
OUT Y/WR/DEL 1	OUT Y1	End the network with an output
END ENT	END	Then end the program

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Entering a Complex Ladder Program

Figure 5-5 shows how to enter a complex network and illustrates all of the guidelines presented in this chapter.

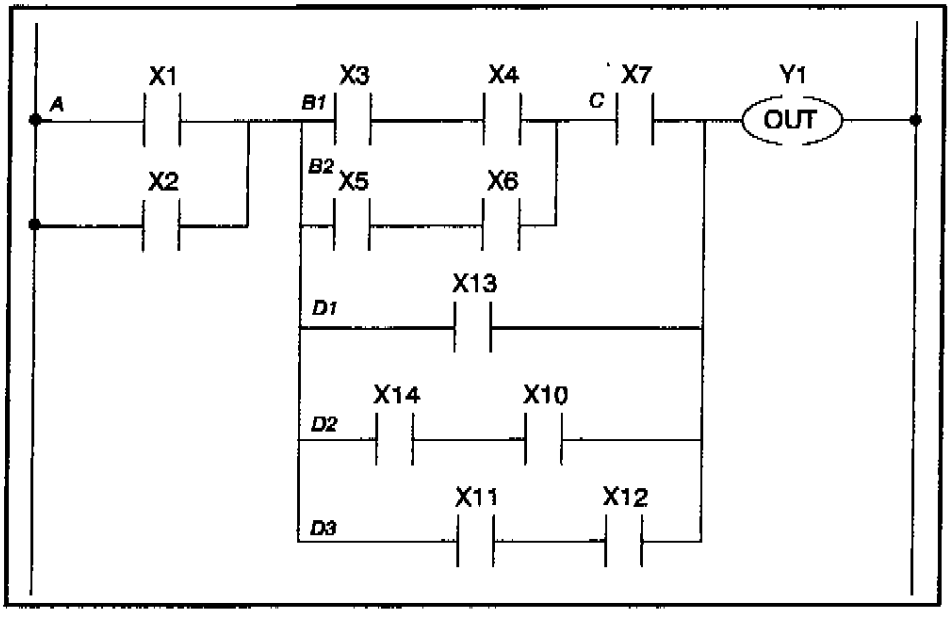


Figure 5-5 Entering a Complex Ladder Program

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Table 5-5 Key Sequence for Ladder Program

Key Sequence	Display	Description
CLR	(Display blank)	Begin with CLR key
S(ADD) NXT	NOP	Go to the first address
STR X(IN) 1 Enter	STR X1	Begin the network with STR
OR X(IN) 2 Enter	OR X2	Join X2 in parallel with X1
STR X(IN) 3 Enter	STR X3	Begin branch B1 with STR
AND X(IN) 4 Enter	AND STR	Join X4 in series with X3
STR X(IN) 5 Enter	STR X5	Begin branch B2 with STR
AND X(IN) 6 Enter	AND X6	Join X6 in series with X5
OR STR Enter	OR STR	Join branch B2 in parallel with branch B1
AND X(IN) 7 ENT	AND X7	Join X7 in series with branches B1 and B2
OR X(IN) 1 3 ENT	OR X13	Join X13 in parallel with branch C
STR X(IN) 1 4 ENT	STR X14	Begin branch D2 with STR
AND X(IN) 1 0 ENT	AND X10	Join X10 in series with X14
OR STR ENT	OR STR	Join branch D2 with X13
STR X(IN) 1 1 ENT	STR X11	Begin branch D3 with STR
AND X(IN) 1 2 ENT	AND X12	Join X12 in series with X11
OR STR ENT	OR STR	Join branch D3 in parallel with branch D2
AND STR ENT	AND STR	Join segment D with segment A
OUT Y(OUT) 1 ENT	OUT Y1	Enter an output
END ENT	END	Then end the program

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5.3 Using the Accumulator

The accumulator in the TI405 CPU is a 32-bit data register where the CPU stores the intermediate results of an arithmetic or logical operation. Many of the instruction set groups, including accumulator data manipulation, bit manipulation and BCD operations, must use the accumulator to perform their functions. The accumulator may be used to store values to be operated upon, or the result of an operation.

One of the most basic instructions that uses the accumulator is LD. One form of the load accumulator instruction places a 16-bit value from a V-memory location into the accumulator. The reverse operation is performed by the OUT instruction, which places a 16-bit value from the accumulator into a V-memory location. Between executing the LD and OUT instructions, any of the BCD operation or bit manipulation functions can be used to modify the value in the accumulator. The following program loads the value from V4000, adds 5 to it and places the result into memory location V4001, whenever X0 is on.

```
STR     X0
LD      V 4000
ADDB    K 5
OUT     V 4001
END
```

If more than one LD instruction is used sequentially, the accumulator stack is brought into use. The stack is a group of eight 32-bit data registers that accept values as they are pushed out of the accumulator by another value being loaded into the accumulator. Up to eight values may be pushed onto the stack. If you try to push any more values onto the stack, the bottom stack element is lost. See Figure 5-6.

Some instructions, such as those in the table function group, use values directly from the accumulator stack. Values on the stack may also be used by popping them back into the accumulator, in a last-in first-out order, using the POP instruction. When the POP instruction is executed the following actions occur as illustrated in Figure 5-6.

- The top stack element is placed in the accumulator.
- All lower stack elements move up one level.
- The top stack value that was placed in the accumulator is placed in the bottom stack element.

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The program shown in Figure 5-6 loads the values from V4000 through V4003 into the accumulator and accumulator stack, then places those values in reverse order into memory locations V4004 through V4007.

```
STR     X0
LD      V4000
LD      V4001
LD      V4002
LD      V4003
OUT     V4004
POP
OUT     V4005
POP
OUT     V4006
POP
OUT     V4007
END
```

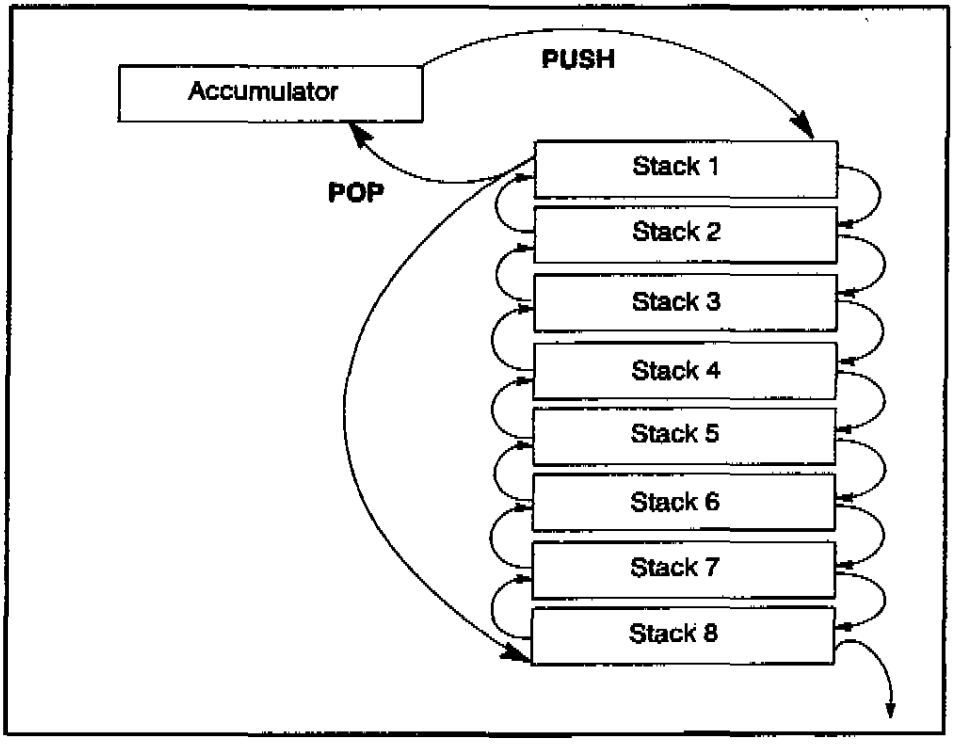


Figure 5-6 Accumulator and Stack Operation

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5.4 Subroutine Programming

The TI435 offers the opportunity to include up to 64 subroutines in your relay ladder logic or Machine Stage program. Subroutines are small programs that are executed when certain conditions in the main program are met. When the subroutine is called, execution of the main program stops until the subroutine has finished, then execution of the main program resumes with the next instruction after the GTS. Figure 5-7 shows all the instructions needed to call and return from a subroutine. Refer to Chapter 21 for detailed descriptions of each instruction used.

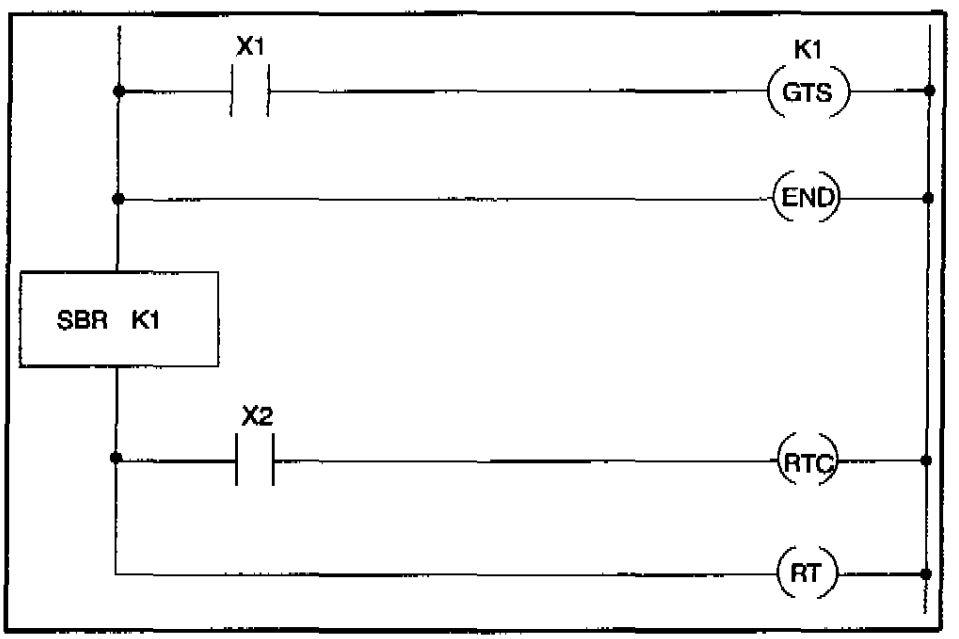


Figure 5-7 Subroutine Instructions

Subroutines may be nested, or placed inside other subroutines, up to eight levels deep. Since subroutines are placed after the **END** instruction in your program, they are not scanned unless called by the main program. This means that they do not add to the scan time unless they are being executed. This makes a subroutine an excellent spot to place math or table instructions that are rarely used. These instructions are often lengthy and execute more slowly than your main program. Placing them in a subroutine keeps your main program as short and fast as possible, and the scan time is only affected by the infrequent subroutine calls.

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Special instructions are available in the TI405 to use with a hardware interrupt input module. When one of the interrupt inputs turns on, the interrupt routine that corresponds to that input is executed immediately. After the interrupt routine has completed, execution resumes where it was interrupted in the main program. Figure 5-8 shows all of the instructions used with an interrupt routine. Refer to Chapter 21 for a detailed description of each instruction involved.

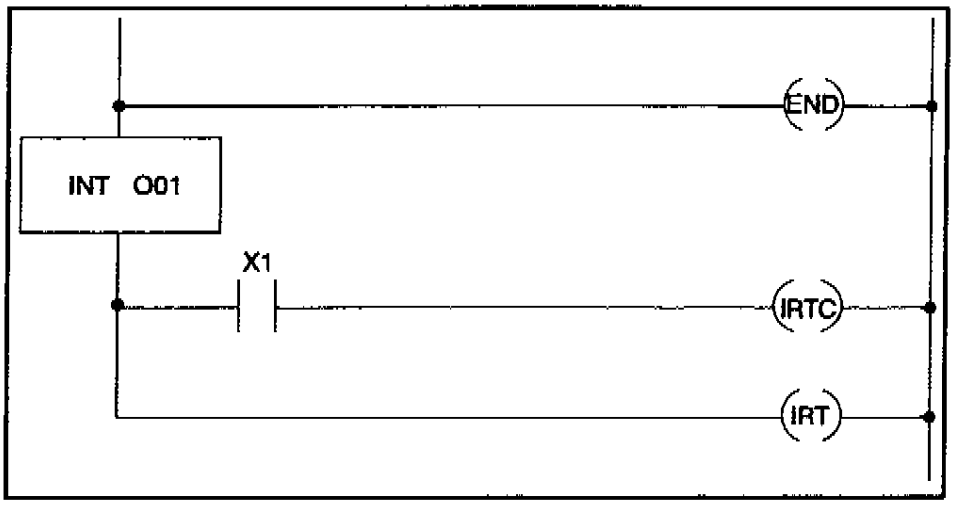


Figure 5-8 Interrupt Routine Instructions

Two instructions are included to allow you control over what sections of the program may be interrupted and what sections should be allowed to complete before an interrupt routine is executed.

- The **ENI** instruction enables the interrupt module to immediately transfer program execution to an interrupt routine. Interrupts are enabled until the program scan encounters a **DISI** instruction.
- The **DISI** disables interrupts while some critical portion of the program executes. Once the critical section ends, another **ENI** instruction enables the interrupt module again.

An interrupt routine may be used with immediate I/O instructions to give a high speed response to a given input. Once the interrupt input turns on, immediate I/O instructions in the interrupt routine can evaluate other inputs and activate outputs without being delayed by the main program's scan time.

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Each component in a CPU scan adds a time factor to the total scan cycle. Figure 5-9 illustrates these components. Table 5-6 lists time factors for each component in TI425, TI430, and TI435 CPUs.

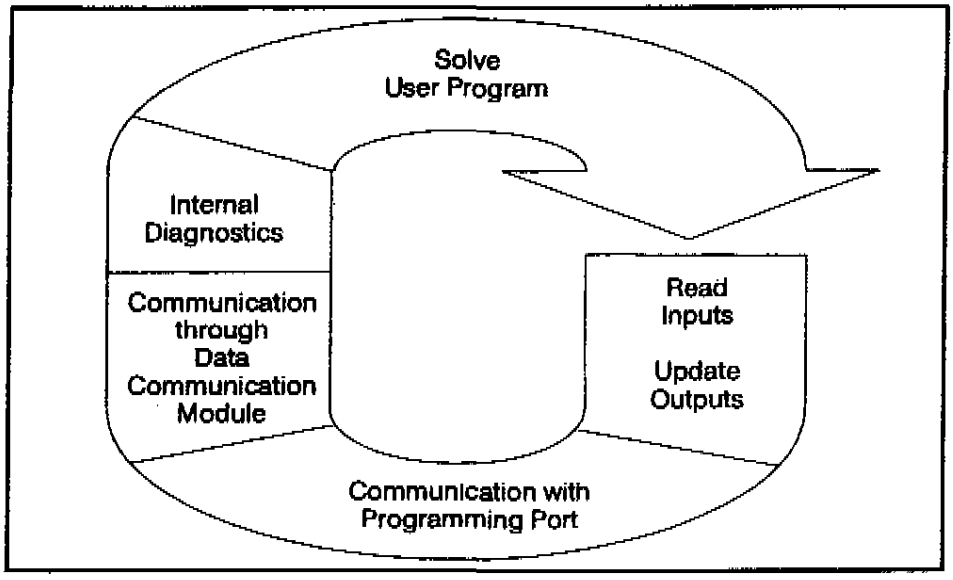


Figure 5-9 Scan Time Components

The following example shows the calculation of scan time for a TI435 with two 16-point input modules, two 16-point output modules, no data communication module, nothing connected to the programming port, 1K of high speed boolean instructions, and 0.5K of other instructions. All times come from Table 5-6.

Read Inputs	=	11.0 µs	Overhead	
		85.6 µs	16-point Module	
		85.6 µs	16-point Module	
		182.2 µs	=	.02 ms
Update Outputs	=	11.0 µs	Overhead	
		90.7 µs	16-point Module	
		90.7 µs	16-point Module	
		192.4 µs	=	.02 ms
Programming Port			0 ms	
Data Communications			0 ms	
Internal Diagnostics				1.6 ms
User Program:				
High Speed Boolean (1 K)			0.49 ms	
Other Instructions (0.5 K)			1.5 ms	
			1.99 ms	1.99 ms
				3.63 ms

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Table 5-6 Calculating Scan Time

Operation	Time	
	TI425, TI430	TI435
Read Inputs:		
Overhead	11.0 µs	11.0 µs
Read each 8-point module	31.3 µs	57.9 µs
Read each 16-point module	62.5 µs	85.6 µs
Read each 32-point module	125.6 µs	141.6 µs
Update Outputs:		
Overhead	11.0 µs	11.0 µs
Read each 8-point module	31.3 µs	62.7 µs
Read each 16-point module	62.5 µs	90.7 µs
Read each 32-point module	125.6 µs	146.6 µs
Programming Port Communications	0.2 – 3.0 ms*	0.2 – 3.0 ms*
Data Communications Module/ Per Module	1.1 – 1.8 ms**	1.1 – 1.8 ms**
Internal Diagnostics	1.1 – 1.5 ms	1.1 – 1.6 ms
User Program (per K)	3.0 ms	0.49 ms† 3.0 ms††

* If no programming device is connected to the programming port, this time is 0 ms.
** If no data communications module is installed, this time is 0.05 ms in the TI425 and 0.16 ms in the TI435.
† High speed boolean instructions
†† All instructions other than high speed boolean (average)

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Chapter 6
Stage Programming

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6.1 Stage Programming

Introduction

Stage programming combines relay ladder logic elements with a sequential function chart of the machine to be controlled in order to develop a control program. The familiar ladder elements are used, but they now control the movement of program execution through the various stages, as well as serving their traditional control roles within each stage. Figure 6-1 shows the four basic components of each stage.

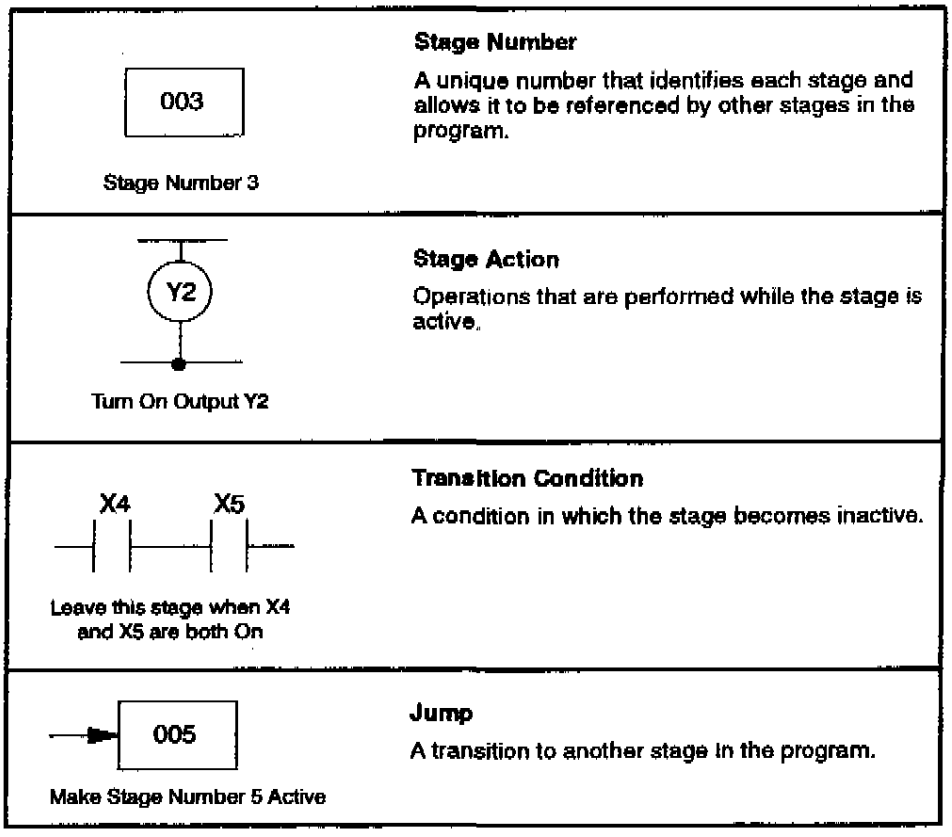


Figure 6-1 Four Basic Components of Stage Programming

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NOTE: Program execution starts at the initial stage when power is applied to the machine. It is usually given the stage number 000, and a special symbol (000) identifies it as the initial stage. More than one initial stage may be used in a program, and each is active when the CPU makes the transition to run mode, but for clarity and for easier troubleshooting, it is recommended that only one initial stage be used. The initial stage may be followed by jumps to multiple stages to achieve the same effect as multiple initial stages.

Figure 6-2 combines the four basic components to make one complete stage.

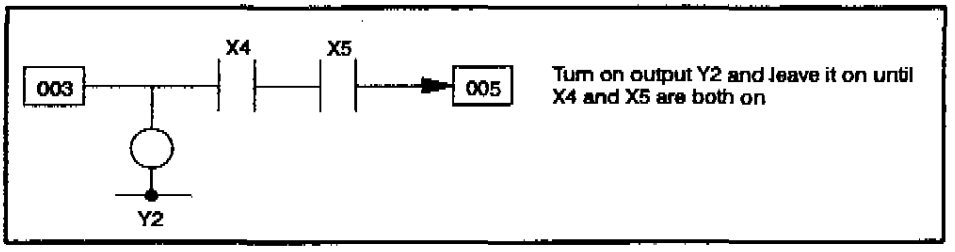


Figure 6-2 One Complete Stage

Only the first component is necessary, since a stage can be used as a flag to indicate that a certain point in the program has been reached. This only requires that a stage number, such as 040, be assigned. See Figure 6-3.

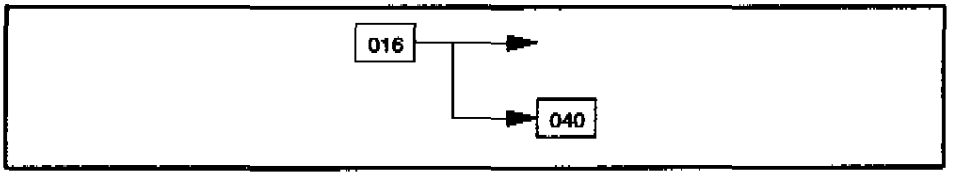


Figure 6-3 Stage Used as a Flag

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Continuously Running Stage

It is also possible to have a stage that runs continuously, and never jumps to another stage. This stage only needs a stage number and stage action, like Stage 011 and output Y4. See Figure 6-4.

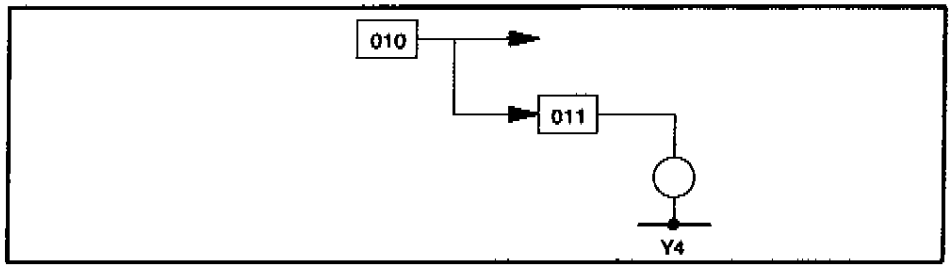


Figure 6-4 Stage Running Continuously

Stage Numbering

In the TI405 CPU, stages are numbered in octal (or base eight) just like the I/O points. This means that the numerals 8 and 9 are not used in stage numbers. See Figure 6-5(A). The next stage number after Stage 7 is Stage 10, and the Stage following Stage 17 is Stage 20.

The stage numbers do not have to be assigned sequentially. You can choose any order that makes sense to you. The TI405 has 384 stage numbers available: 000 to 577 in octal; however, only one stage can be assigned any given stage number. See Figure 6-5(B).

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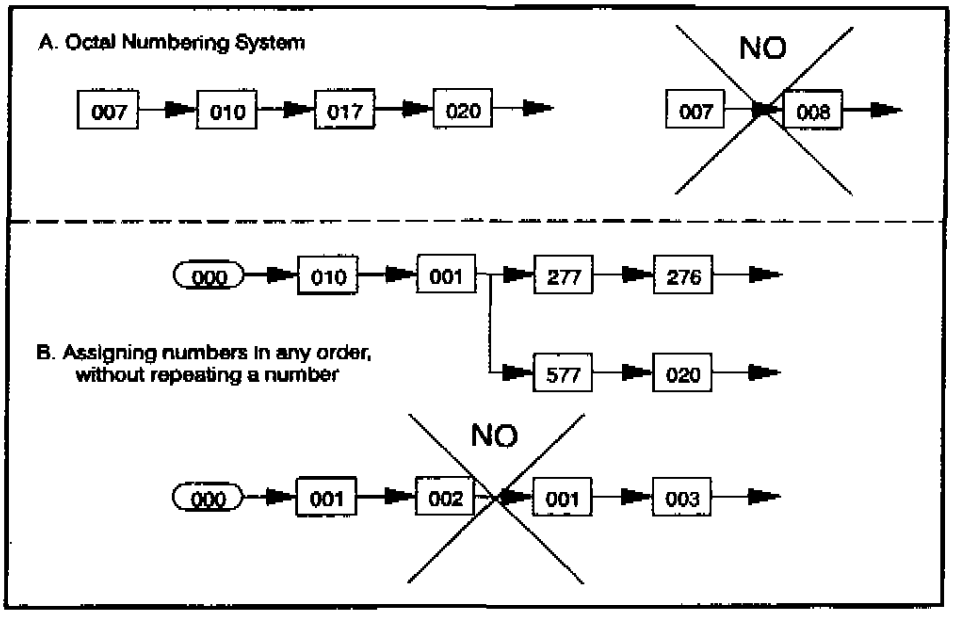


Figure 6-5 Assigning Stage Numbers in Octal

Connecting Stages

Stages can be connected in a simple, straight-line configuration that executes much like scanning through a relay ladder logic program. The main difference is that only the I/O points in the active stage can control the program's execution. See Figure 6-6.

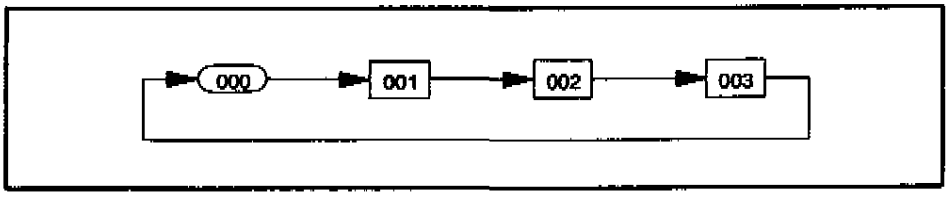


Figure 6-6 Stages Connected Sequentially

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Stage Controlling the Same Points

Once Stage 1 jumps to Stage 2, none of the I/O in Stage 1 is active, unless the same points are being used in Stage 2. See Figure 6-7. This can be done because inactive stages cannot control program execution.

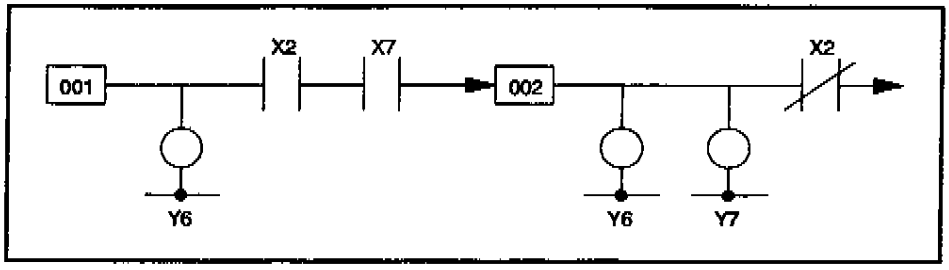


Figure 6-7 Stages Controlling the Same Points

Passing Status Between Stages

To ease the transition between stages, outputs from the previous stage remain on for one scan of the newly activated stage. Therefore, an output energized by two consecutive stages cannot turn off for one scan during the transition between stages. See Figure 6-8.

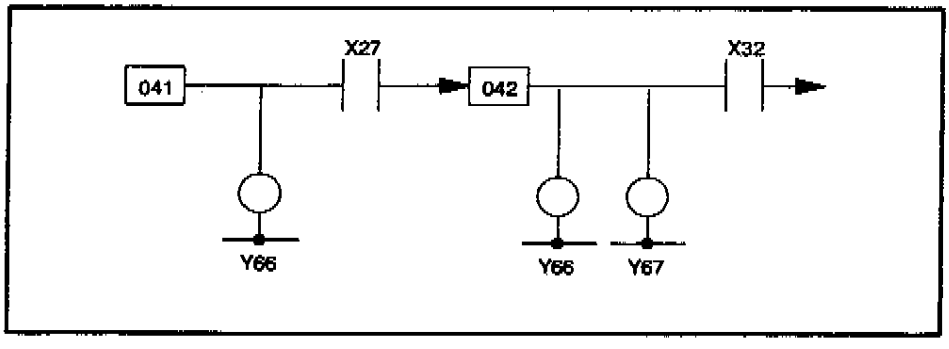


Figure 6-8 Passing Status Between Stages

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Outputs

More than one active stage can use the same output points without interference. See Figure 6-9. The stages are considered to be connected in parallel to the shared output: so if one or multiple stages turn on an output, it comes on—even if other stages have it turned off. For duplicate outputs used in different stages, always use the **OR OUT** instruction.

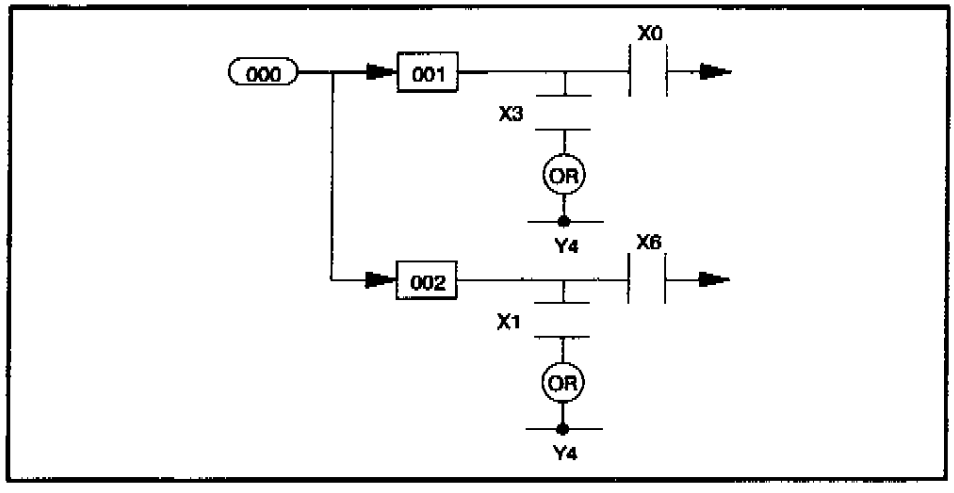


Figure 6-9 Active Stages Sharing Output

It is possible, and often desirable, to have multiple stages active at the same time. You can have several chains of stages looping at once, or stages can branch to multiple other stages and create parallel operations that may or may not rejoin. See Figure 6-10.

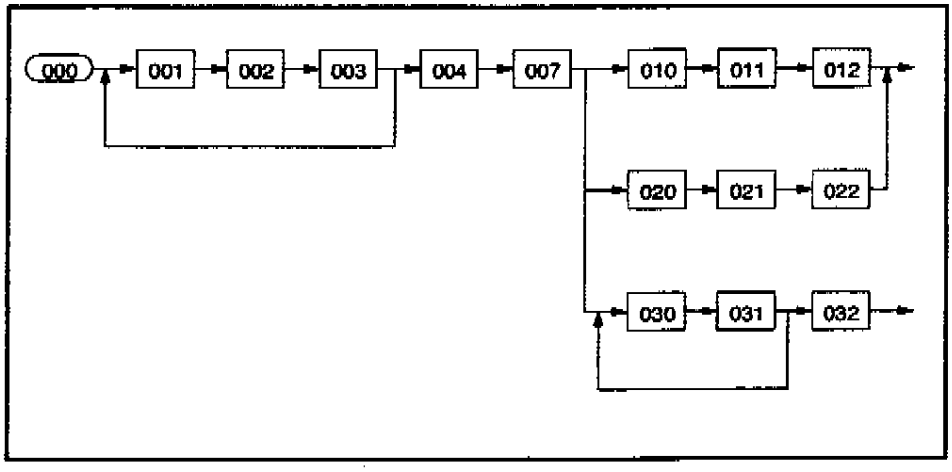


Figure 6-10 Sample of Multiple Active Stages

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Stage Condition

The active or inactive condition of a stage can be used as a ladder logic contact to control the flow of program execution in other stages, as shown in Figure 6-11. When multiple stages are active, this can be a very useful way for each stage to monitor what the others are doing, and react accordingly. Stage 3 has to be active before Stage 1 can transition to Stage 10, but then Stage 3 has to become inactive before Stage 10 can jump to Stage 11.

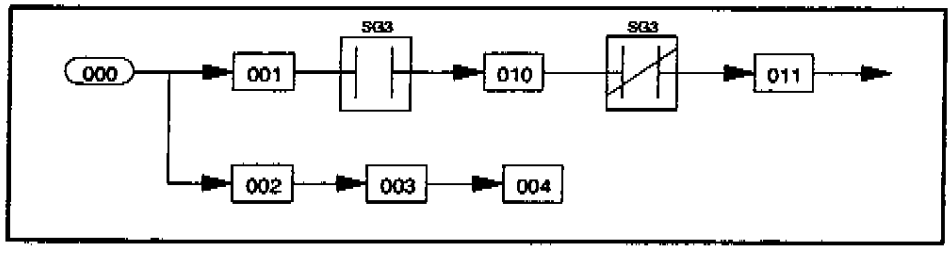


Figure 6-11 Using Stage Condition to Control Flow

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Using Stage is Simple

The main advantage of stage programming is its simplification. This simplification can save you time at each step in the life of an industrial automation project. Design, programming, startup, and maintenance times can be significantly reduced through the use of stage.

Designing

Drawing a sequential function chart aids in understanding the operation of the machine that you are going to automate. Figure 6-12 provides a sequential function chart describing the operation of a machine that clamps a part, drills a hole in the part, and then ejects it. See Figure 6-13.

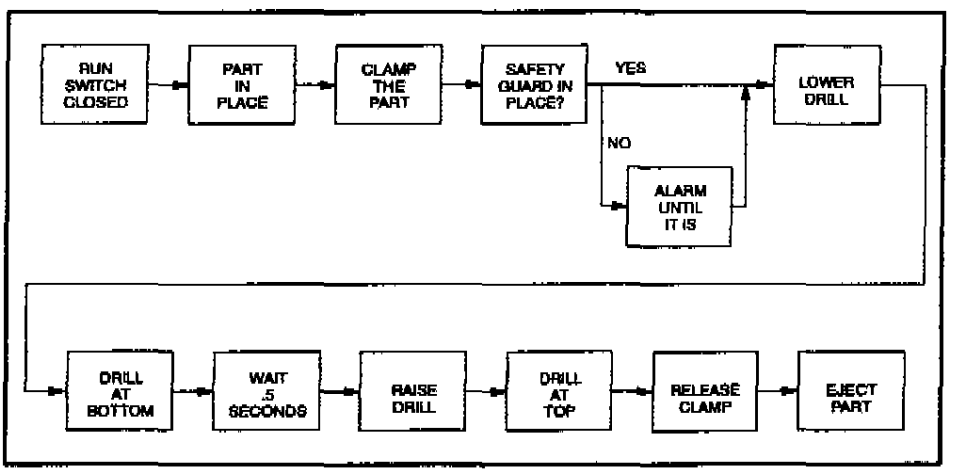


Figure 6-12 Sequential Function Chart

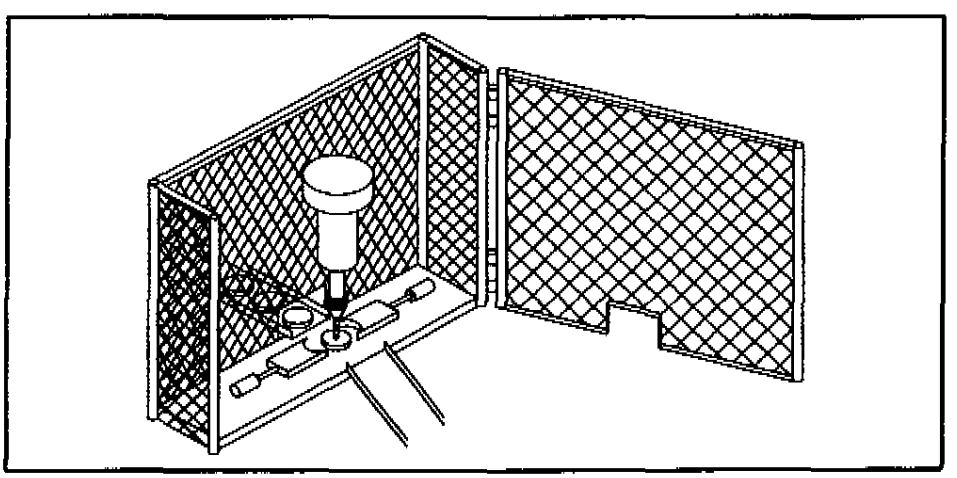


Figure 6-13 Typical Clamp/Drill Press Operation

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Adding I/O Points

Once the operation of the machine is understood, the next job is to decide what I/O points are needed to control the machine as it steps through its functions. These can be added to the sequential function chart. Putting the I/O symbols right on the chart can help ensure that no points are overlooked. See Figure 6-14.

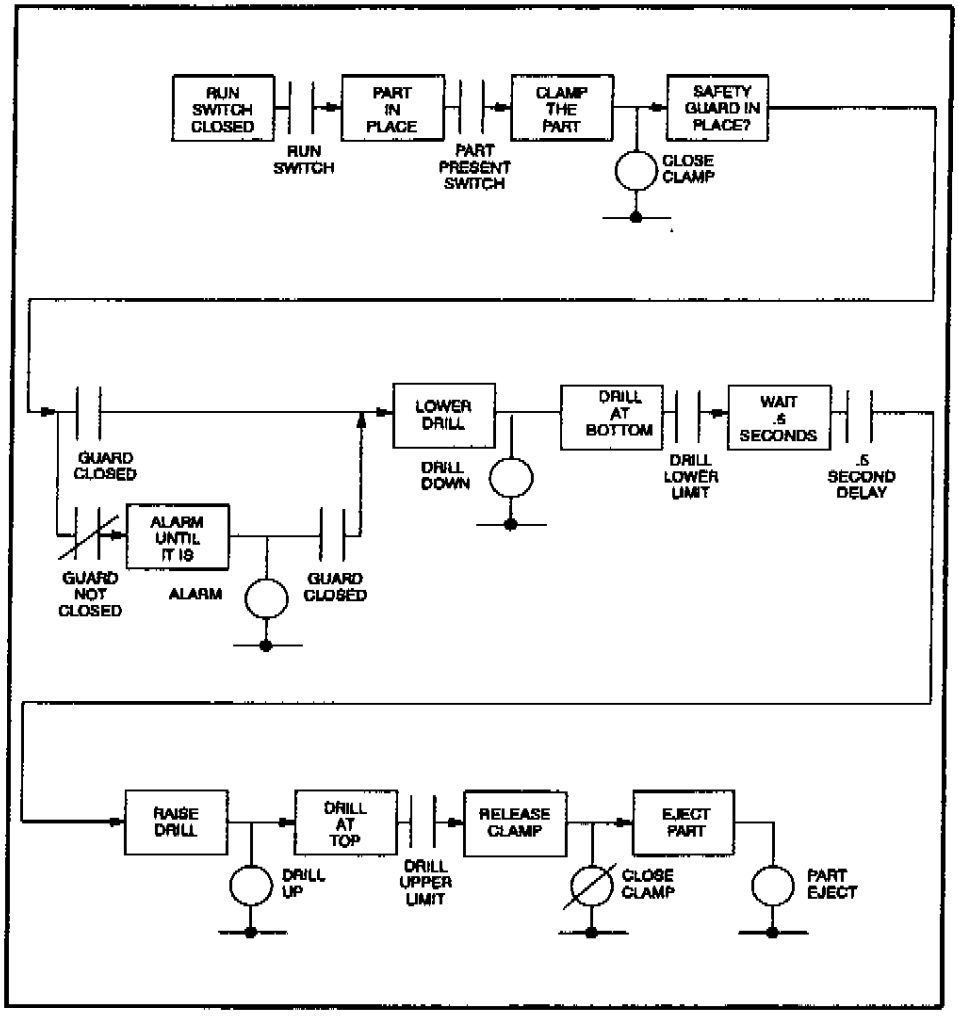


Figure 6-14 Adding I/O Points

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After the I/O points have been added to the sequential function chart, the last design job is to assign numbers to each of the points. See Figure 6-15

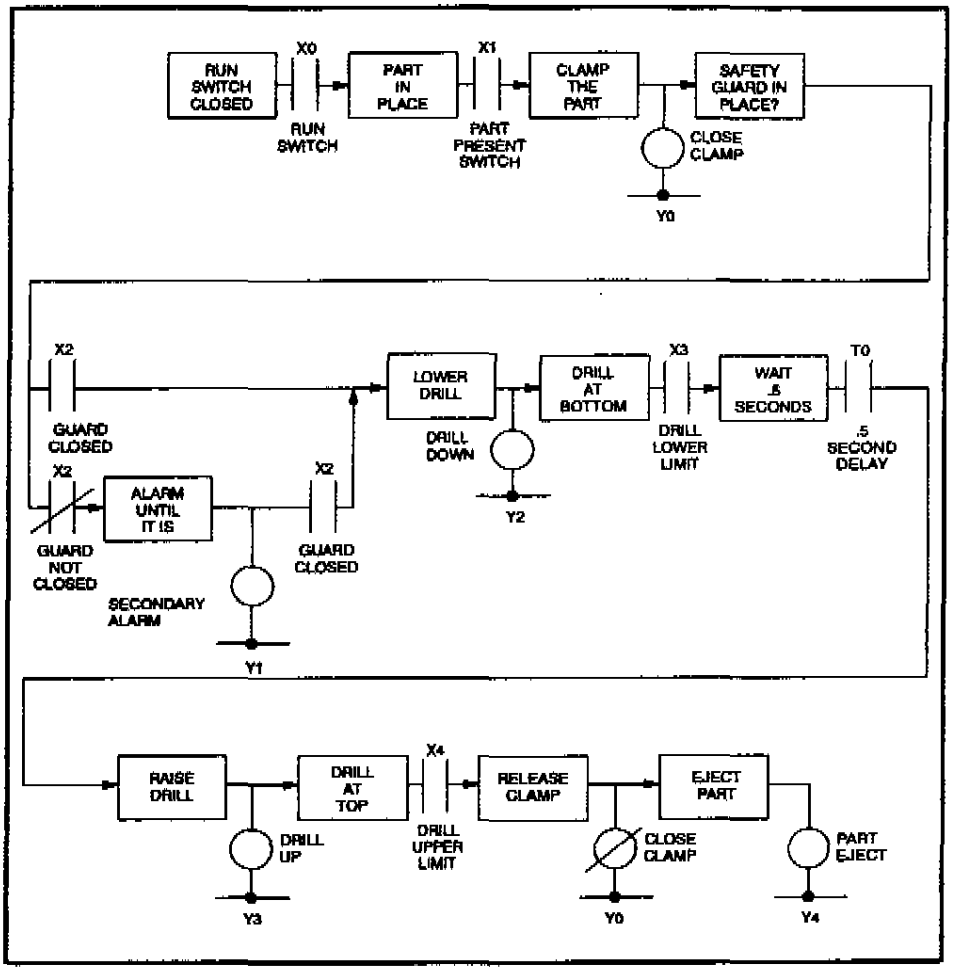


Figure 6-15 Assigning Numbers to I/O Points

NOTE: This is an example application only. Actual applications require PLC external circuits for primary/critical safety protection.

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Programming

If you are programming in ladder logic, study the chart and carefully consider the timing and order of the program scan. You can then decide what I/O points and operations need to be latched on or off to preserve the required states while the entire program is scanned over and over. You must also find and decide what points need permissive contacts in series, in order to prevent something from happening until conditions are right. Figure 6-16 shows a sample ladder logic program.

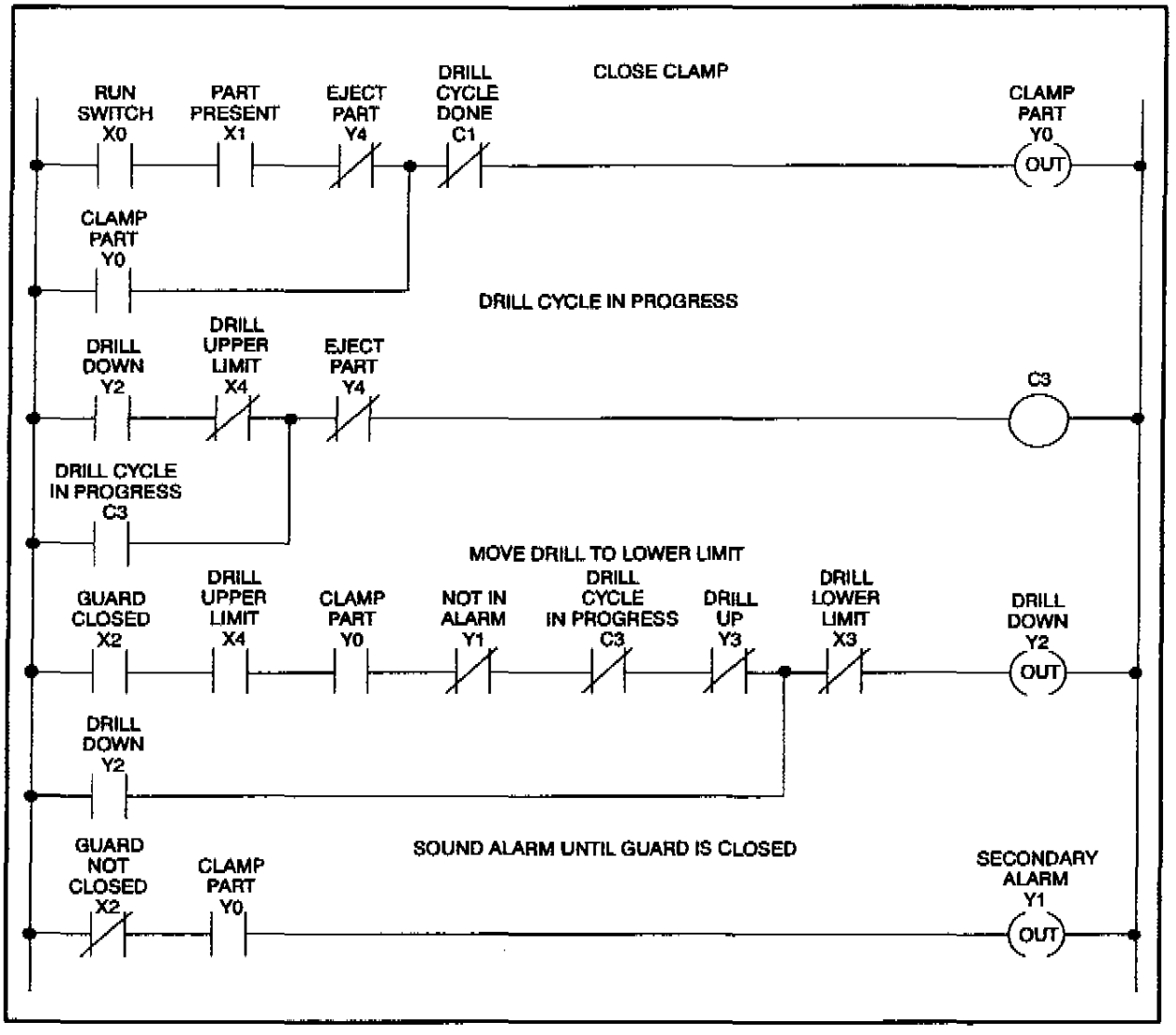


Figure 6-16 Example of a Ladder Logic Program

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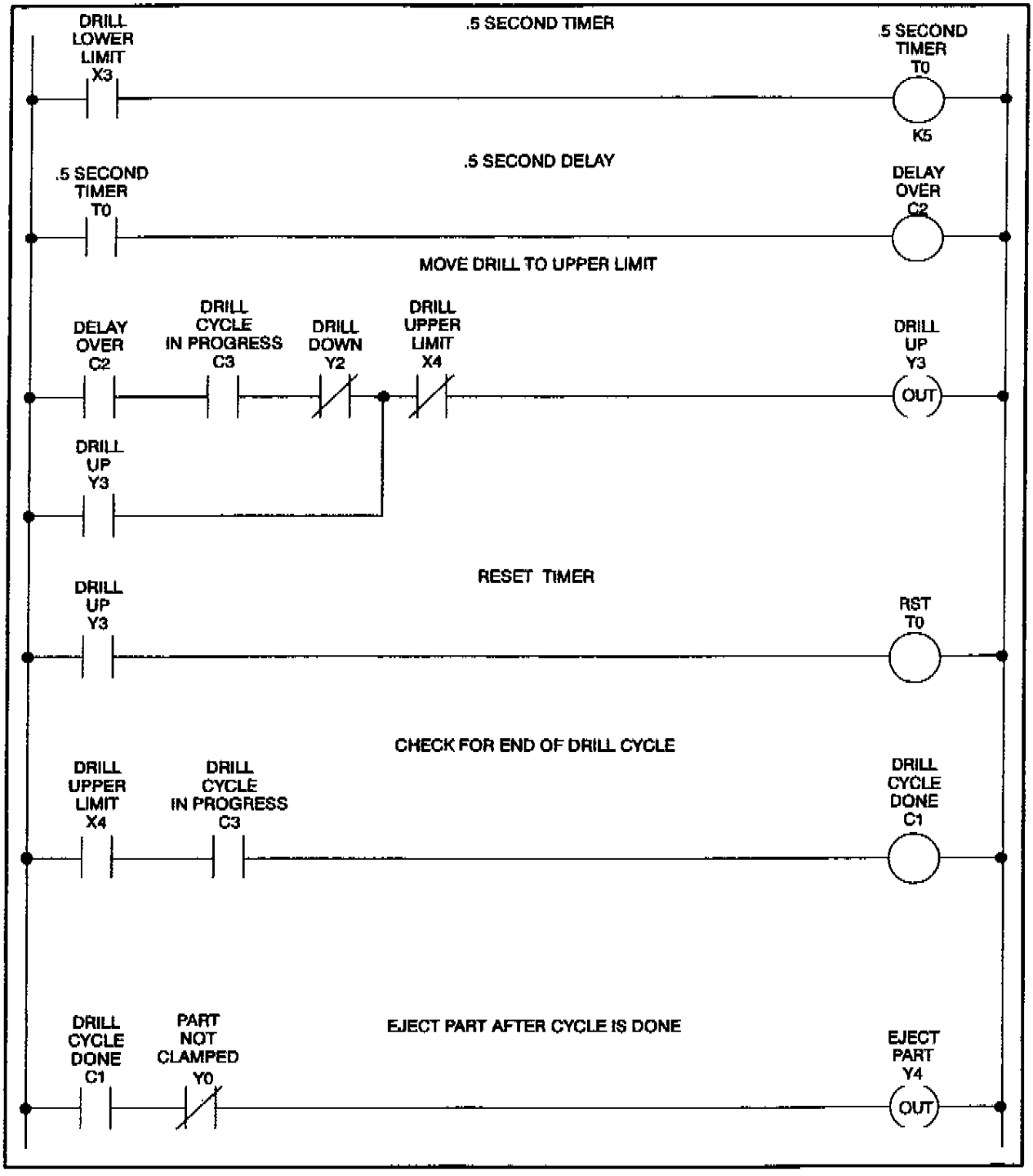


Figure 6-16 Example of a Ladder Logic Program (continued)

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Programming in Stage

If you are programming in stage, by the time you reach the programming step you have almost completed it. A few modifications and the addition of stage numbers are all that is necessary. See example in Figure 6-17.

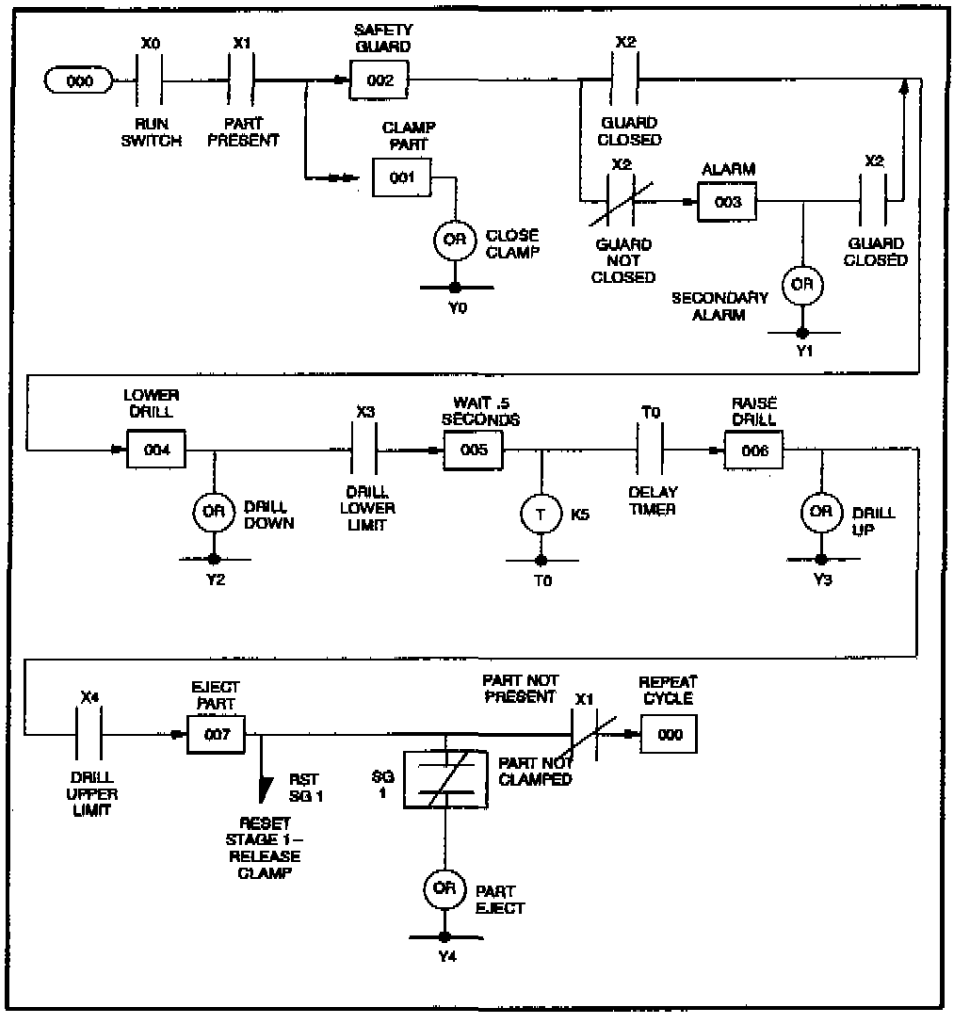


Figure 6-17 Example of Stage Programming

NOTE: This is an example application only. Actual applications require PLC external circuits for primary/critical safety protection.

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As you can see, some of the blocks defining stage actions were combined with blocks defining the transition conditions needed to leave the stages. See Figure 6-17. A branch was added where the part clamp closes. Since the clamp output must be kept on until the drilling is completed, a set stage instruction is used to allow the clamp stage to stay on while the rest of the program executes. After the drill reaches its upper limit, the clamp stage is reset to turn off the output and release the part for ejection. The jump back to Stage 0 at the end allows the machine to run continuously, as long as the run switch is closed.

The stage program requires fewer steps than the ladder logic program. This means fewer instructions to enter and fewer instructions to search through during the startup step. See Figure 6-18.

Ladder Logic	Stage Programming
STR X0	ISG S0
AND X1	STR X0
AND NOT Y4	AND X1
STR Y0	SET S1
OR STR	JMP S2
AND NOT C1	SG S1
OUT Y0	OR OUT Y0
STR Y2	SG S2
AND NOT X4	STR X2
STR C3	JMP S4
OR STR	STR NOT X2
AND NOT Y4	JMP S3
OUT C3	SG S3
STR X2	OR OUT Y1
AND X4	STR X2
AND Y0	JMP S4
AND NOT Y1	SG S4
AND NOT C3	OR OUT Y2
AND NOT Y3	STR X3
STR Y2	JMP S5
OR STR	SG S5
AND NOT X3	TMR T0 K5
OUT Y2	STR T0
STR NOT X2	JMP S6
AND Y0	SG S6
OUT Y1	OR OUT Y3
STR X3	STR X4
TMR T0 K5	JMP S7
STR T0	SG S7
OUT C2	RST S1
STR C2	STR NOT S1
AND C3	OR OUT Y4
AND NOT Y2	STR NOT X1
STR Y3	JMP S0
OR STR	END
AND NOT X4	
OUT Y3	
STR Y3	
RST T0	
STR X4	
AND C3	
OUT C1	
STR C1	
AND NOT Y0	
OUT Y4	
END	

Figure 6-18 RLL versus Stage Programming Instructions

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The main differences in Figure 6-18 that you notice are the JMP and SG instructions and the OR OUT instructions. The JMP instruction is the way the program transitions between stages. JMP S2 means to jump to Stage 2 and start executing. The line SG S2 marks the beginning of what is executed once the jump to Stage 2 is made. The other way to start a stage executing is to use the set instruction. This activates the stage being set, but unlike a jump, setting a stage does not stop the current stage from executing.

The OR OUT instruction is used, but not required, in this example. It is not required since there are no cases where multiple stages attempt to control the same outputs. The OR OUT allows multiple active stages to control the same output without interfering with each other. This is the equivalent of having the active stages connected in parallel before being joined to the output. If one of the active stages turns on the output, it will come on, even if one of the other active stages has the output turned off. This way, several active stages can control the same output without having to be concerned with which one is last in the scan.

While Stages 1, 2 and 3 are active, the stage program shown in Figure 6-19 controls Y0 in the same manner as the ladder logic program shown in Figure 6-20.

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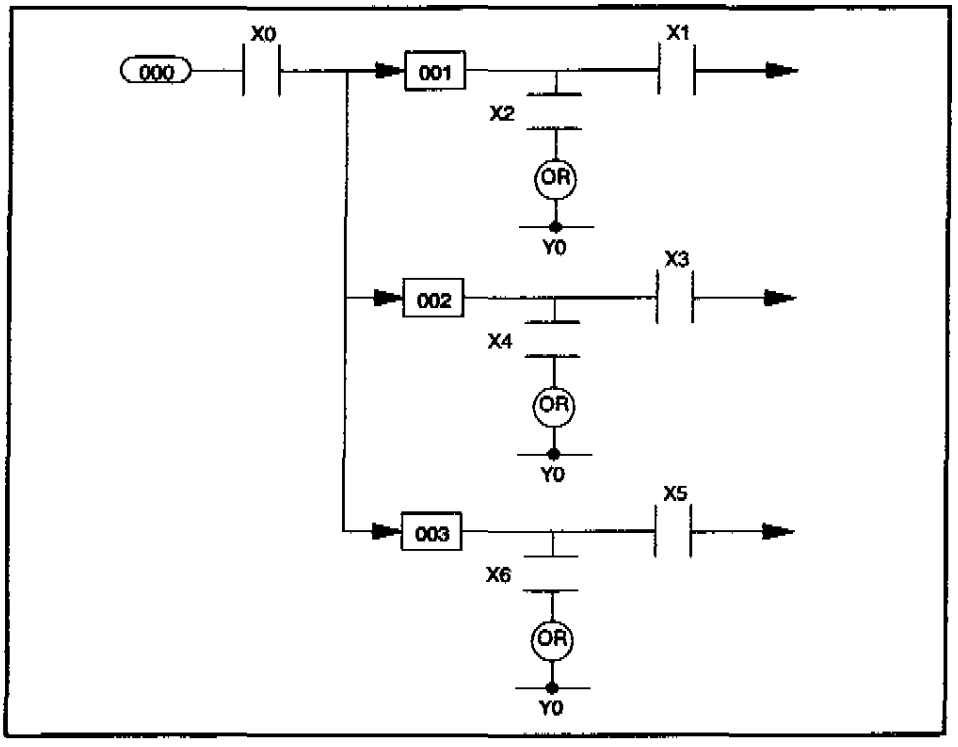


Figure 6-19 Multiple Stages Controlling an Output

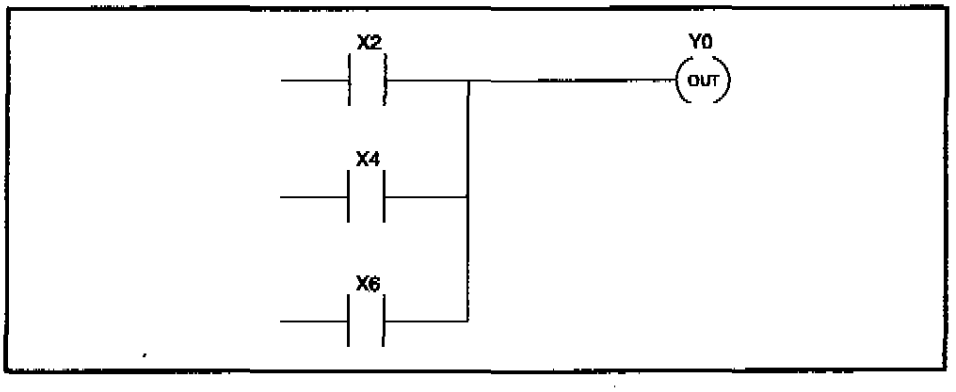


Figure 6-20 Ladder Logic Equivalent (All Stages Active)

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6.3 Advantages of Stage Programming

Since stage programming gives you control over which sections of the program are active at any given time, the use of latching circuits and permissive contacts to control events relative to the program scan is eliminated. The **SET** and **RESET** instructions replace the latch and release circuits of ladder logic, and give the ability to control the outputs of multiple stages from any other stage in the program by making the stages active or inactive. Control relay usage is practically eliminated, since control relays in ladder logic synchronize the execution of several rungs from scan to scan. Leaving out the control relays naturally makes a shorter program.

Documentation

One advantage of stage programming over ladder logic is that with stage, the program is practically documented by the time it is written. If the stages and I/O points are labeled as the design step progresses, you can follow the flow of the program. With ladder logic, documentation is a step that can be overlooked.

Modular Design

Stage programming promotes modular development of control programs. A stage program is composed of modules, each controls a specific function in the program. By developing and reusing program modules, made of individual or groups of stages, program development time is cut. Modular programs are easy to troubleshoot, since all the operations that control a given function are grouped together.

Debugging Programs

In the startup step, you must make changes to adjust the program to how the machine actually works. Since you know what stages are active at any given time, searching for problems is restricted to a limited and defined area.

It is easier to step through a stage program, one stage at a time, than to control the continuous scan of a ladder logic program. A stage program has a well defined path that the program execution follows.

You can make program changes in a stage program with confidence. Any change made to a stage can only affect program execution while that stage is active.

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Maintenance

Once the startup step is successfully completed, the maintenance step begins. The direct correspondence of a program stage to a machine operation is helpful for troubleshooting since the maintenance person is familiar with how a machine operates.

As in the startup step, it is easier to narrow the search for problems when you only have a limited number of active stages. The limited use of control relays simplifies the construction of a stage program, makes it much easier to follow, and gives it a closer correspondence to the machine that it controls.

If a modular approach to writing the program was used, another common maintenance problem can be addressed. If a library of stage operations is developed and reused throughout a plant, the same control stages perform the same operations in whatever machine is being worked on. Since the maintenance personnel see the same stages in several machines, they see them more often.

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6.4 Setting the CPU to Program Mode

Before entering any of the example programs, use the following steps to put the CPU in Program (PGM) mode and clear its memory. The CPU keyswitch must be in the **TERM** position.

Key Sequence	Display
CLR CLR 1 9 AUX	AUX 1* Operating Mode AUX 13 Go To PGM Mode
ENT	PGM Mode?
ENT	Mode = PGM
CLR 2 4 AUX	AUX 2* RLL Operations AUX 24 Clear Ladders
ENT	Clear all Ladders?
ENT	OK
CLR $\uparrow$(ADJ) NXT	$ 0 NOP

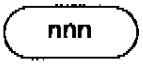
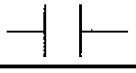
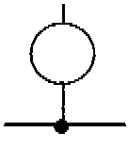
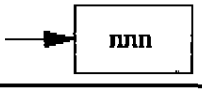
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6.5 A Simple Stage Programming Example

Diagram Symbols

Table 6-1 shows the symbols used in the first stage example in this section. The sequence nnn represents a three-digit stage number.

Table 6-1 Diagram Symbols

Symbol	Name	Description
	Initial Stage	This is the stage where program execution starts when the CPU is switched to RUN mode.
	Stage	Subsequent stages following the initial stage in the program.
	Contact	Equivalent to a normally open ladder logic contact.
	Coil	Equivalent to a ladder logic coil.
	Jump	Leave the current stage and start executing the indicated stage when power flow reaches this point.

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Start-Stop Example

Figure 6-21 shows a simple start-stop program in stage. Once the home position (X0) and oil pressure (X1) switches are made, an OK to start (Y0) light is illuminated in Stage 0. As long as X0 and X1 are closed, Y0 will remain lit until the start switch (X2) is closed.

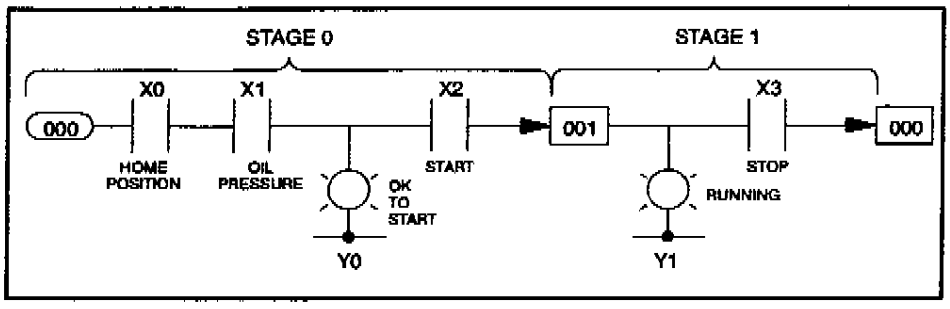


Figure 6-21 Simple Stage Programming Example

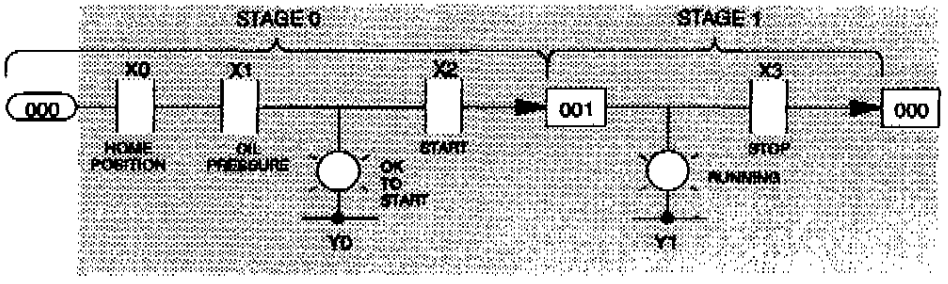
Activating the start switch allows a jump to Stage 1 to occur; this disables the output in Stage 0, causing Y0 to be turned off. The running light (Y1) in Stage 1 stays on, and program execution remains in Stage 1 until the stop switch (X3) is closed.

Closing the stop switch allows a jump back to Stage 0; this disables the output in Stage 1. Figure 6-22 illustrates the key sequence for entering this example. The unshaded area of the logic diagram is the part of the program entered by the key sequence that precedes it.

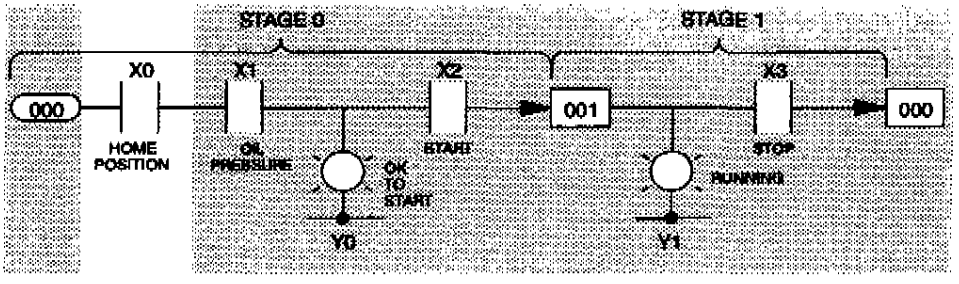
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Shaded keys [ ] represent the blue colored symbol identification keys on the IU.

Key Sequence	Display
[ISG] [S(SG)] [0] [ENT]	ISG S0



[STR] [X(IN)] [0] [ENT]	STR X0



[AND] [X(IN)] [1] [ENT]	AND X1

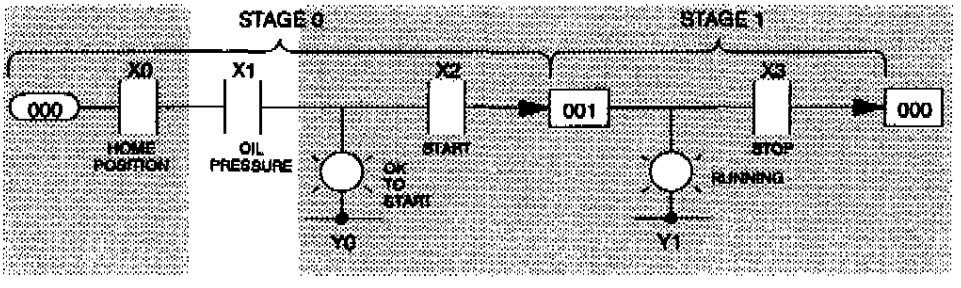
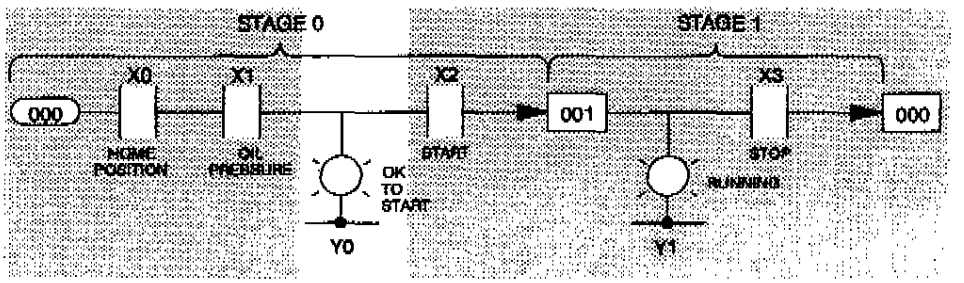


Figure 6-22 Entering a Stage Program

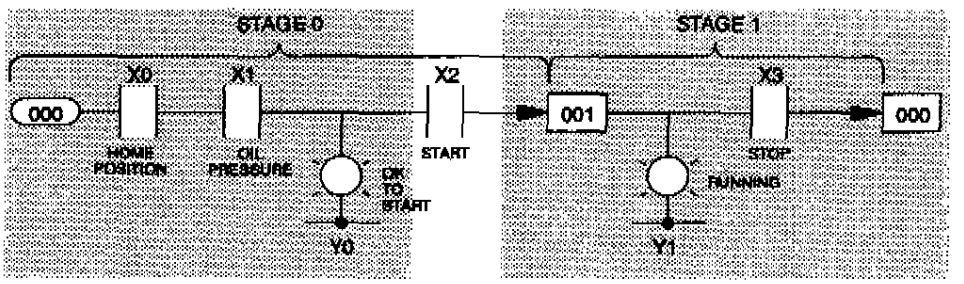
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Key Sequence **Display**

OUT Y(OUT) 0 ENT — OUT Y0



AND X(IN) 2 ENT — AND X2



JMP S(SEG) 1 ENT — JMP S1

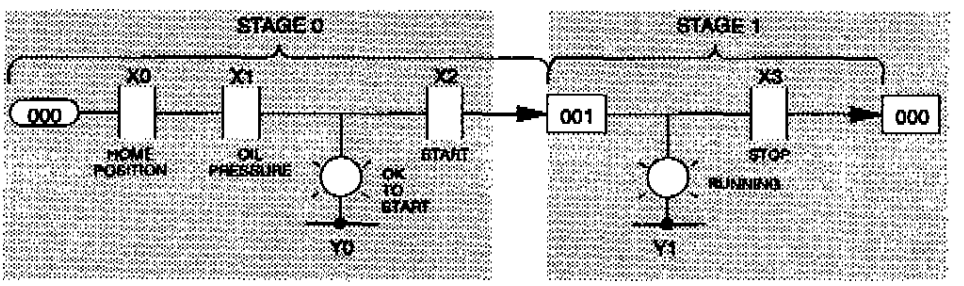
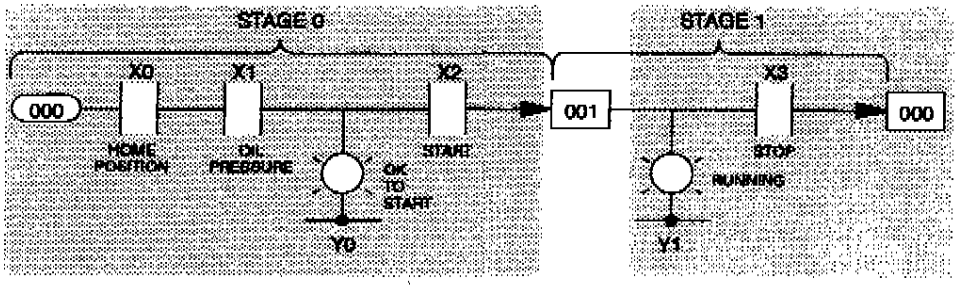


Figure 6-22 Entering a Stage Program (continued)

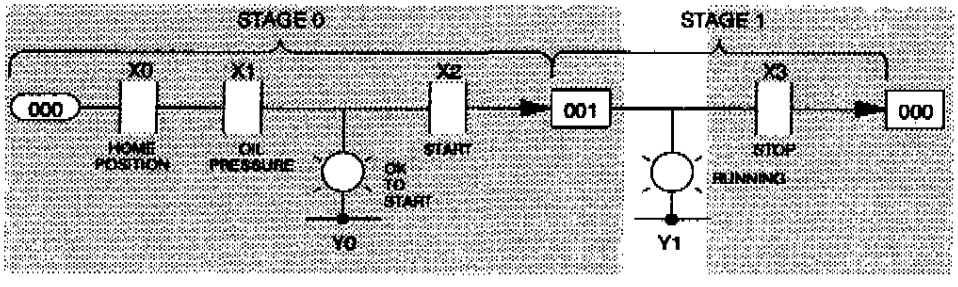
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Key Sequence **Display**

SG 0 ENT SG S1



OUT 0 ENT OUT Y1



STR 3 ENT STR X3

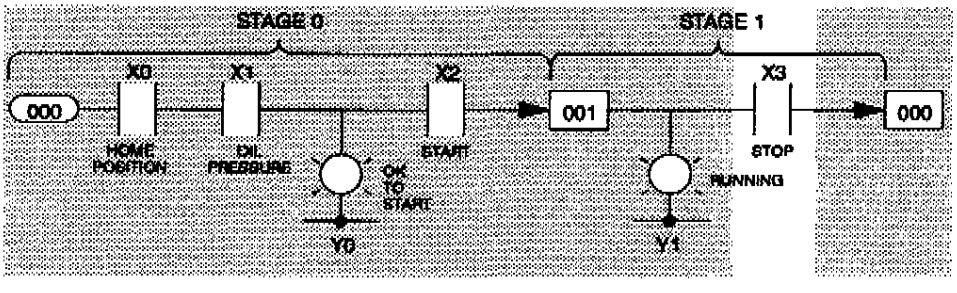
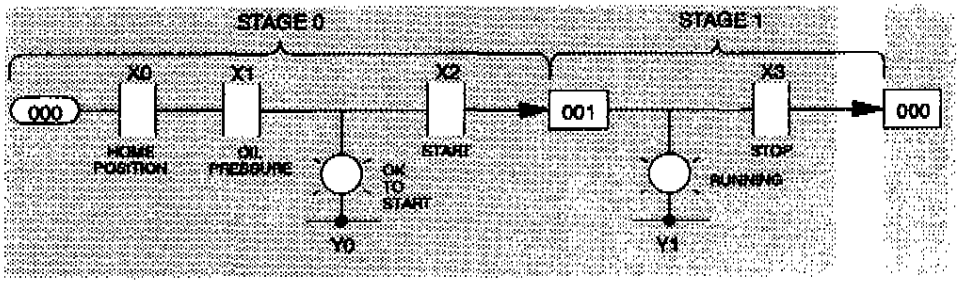


Figure 6-22 Entering a Stage Program (continued)

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Key Sequence	Display
JMP (SHIFT) 0 ENT	JMP S0



Key Sequence	Display
END ENT	END

Figure 6-22 Entering a Stage Program (continued)

Running the Program

To run the program, press the following key sequence.

Key Sequence	Display
CLR (SHIFT) CLR 1 1 AUX	AUX 1* Operating Mode AUX 11 Go To RUN Mode
ENT	RUN Mode?
ENT	Mode = RUN

Details of Program Operation

The program starts executing at initial Stage 0. X0 and X1 control the state of Y0 until X0, X1, and X2 are all closed at the same time. Having all three closed simultaneously allows the jump from Stage 0 to Stage 1.

Once the jump to stage 1 is made, X3 and Y1 are the only active I/O points. X0, X1, and X2 are not used in Stage 1, and may be switched on or off without affecting program execution. Y0 remains off, and Y1 is on, until X3 is closed.

Closing X3 allows a jump back to Stage 0; this causes Y1 to turn off and enables X0, X1, and X2 to control program execution once again.

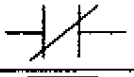
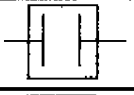
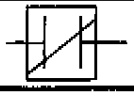
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6.6 An Intermediate Stage Programming Example

Diagram Symbols

The intermediate stage programming example uses four additional symbols. See Table 6-2. The sequence nnn represents a three-digit stage number.

Table 6-2 Intermediate Stage Diagram Symbols

Symbol	Name	Description
	Reset Stage	Disable the indicated stage when power flow reaches this point.
	NOT Contact	Equivalent to a normally closed ladder logic contact.
	Stage Contact	This contact passes power flow when the indicated stage is active.
	NOT Stage Contact	This contact passes power flow when the indicated stage is not active.

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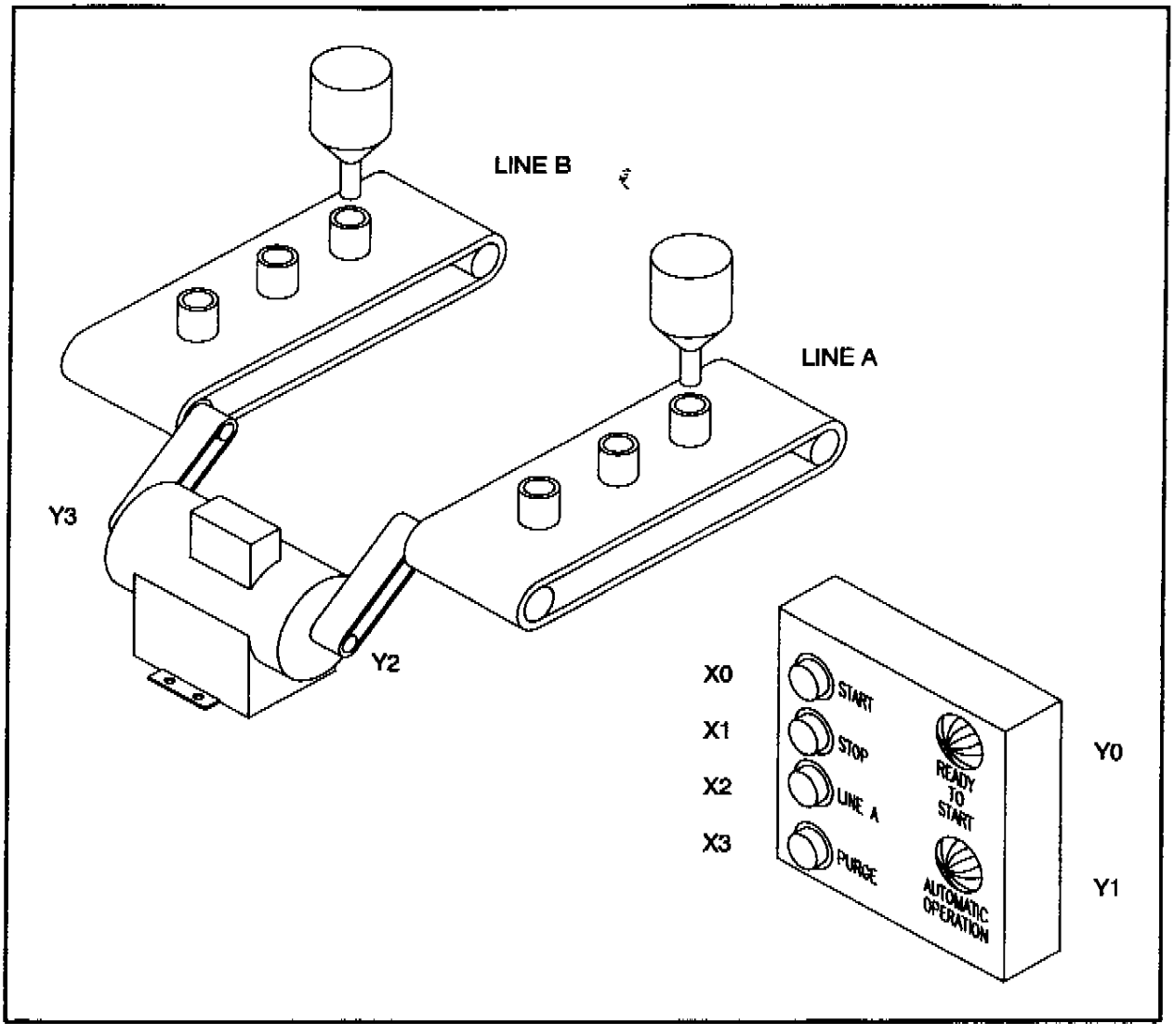


Figure 6-23 Conveyor Line

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Conveyor Line Example

In the example shown in Figure 6-24, a stage program controls a typical conveyor line. See Figure 6-23. The program example has four stages.

- Stage 0 illuminates the Ready to Start light until X0, the Start button, is closed. This allows a jump to both Stage 1 and Stage 2.
- Stage 1 turns on the Automatic Operation light and then waits until the Stop button (X1) is closed.

  While X1 is open, Stage 1 remains active, and its state can be used to control program execution in other stages through State Contact SG 1.

  When X1 is closed, Stage 1 is reset; this turns Y1 off until the next jump to Stage 1. The inactive state of Stage 1 is then reflected by the state of Stage Contact SG 1.
- The operation of Stage 2 is controlled by X2 and X3. As long as X3 is open, X2 selects either conveyor A or B to run. Special relay SP4 continuously pulses on for 0.5 seconds and off for 0.5 seconds.

  This engages one of the clutches and allows the selected conveyor to move for 0.5 seconds and stop for 0.5 seconds. This operation might be used to move empty containers under a filling spout and pause as each one is filled.

  When X3 is closed to request continuous running of both conveyors, a jump to Stage 3 is allowed. If the stop button is closed at any time, Stage Contact SG 1 forces a jump to Stage 0.
- Stage 3 engages the clutches on both conveyors at the same time. This might be used to purge all product from both conveyors. Notice that both Stage 2 and Stage 3 use the same Y2 and Y3 outputs.

  Since only one of these stages is active at any given time, this does not cause a problem as it might in a conventional ladder logic program. The effect is much the same as using jumps in relay ladder logic to allow selective control of an output by different sections of the program.
- Once X3 is opened, Stage 2 resumes pulsed operation of one of the conveyors, until either X1 or X3 is once again closed.

  If X1 is closed while either Stage 2 or Stage 3 is in control, Stage Contact SG 1 forces a jump to Stage 0, where execution waits until start button X0 is closed.

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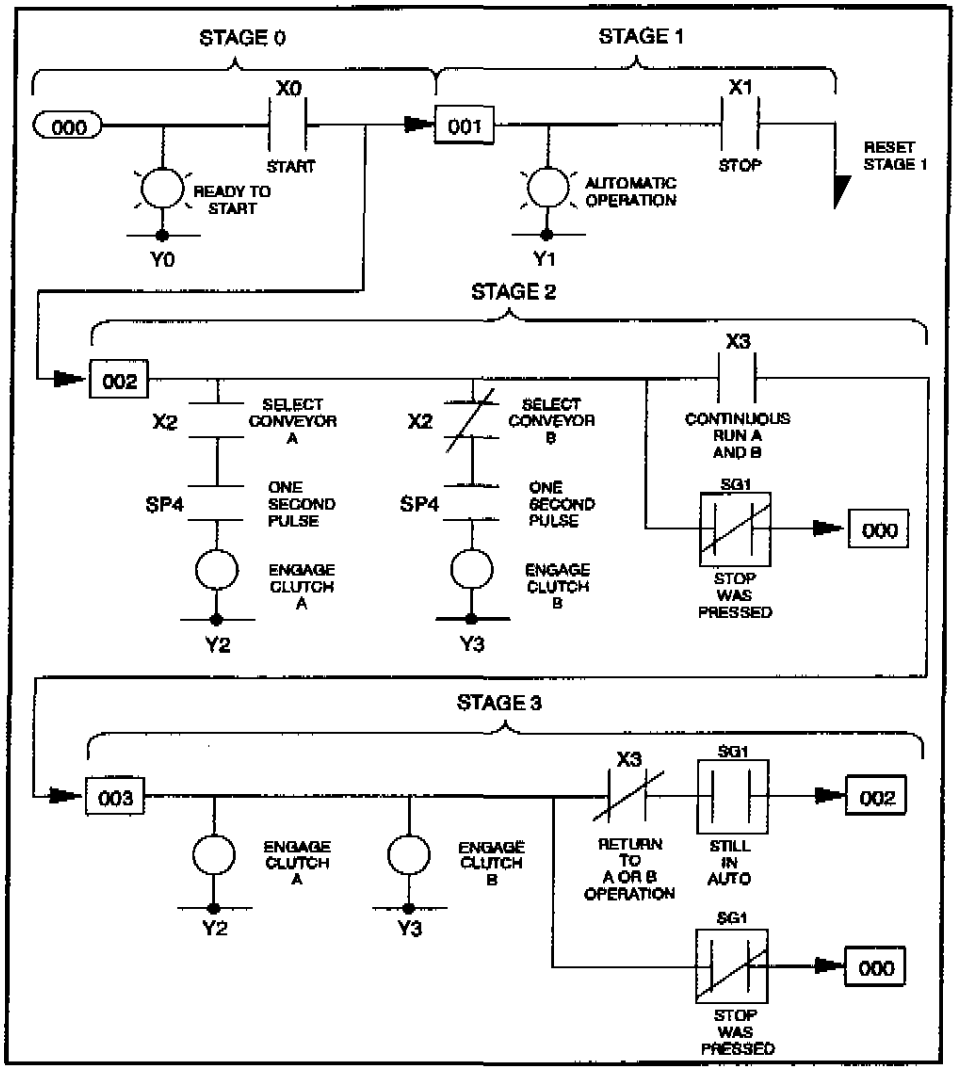


Figure 6-24 An Intermediate Stage Programming Example

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Entering Stage 000

Figure 6-25 shows the complete Stage 0 program.

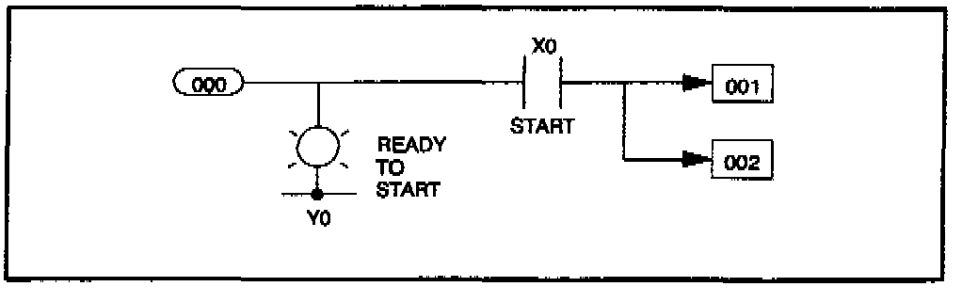


Figure 6-25 Intermediate Example—Stage 000

Enter the following key sequence to program Stage 0. Shaded keys [ ] represent the blue colored symbol identification keys on the MIU.

Key Sequence	Display
ISG (SHIFT) 0 ENT	ISG S0
OUT (SHIFT) 0 ENT	OUT Y0
STR (SHIFT) 0 ENT	STR X0
JMP (SHIFT) 1 ENT	JMP S1
JMP (SHIFT) 2 ENT	JMP S2

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Entering Stage 001

Figure 6-26 shows the complete Stage 1 program.

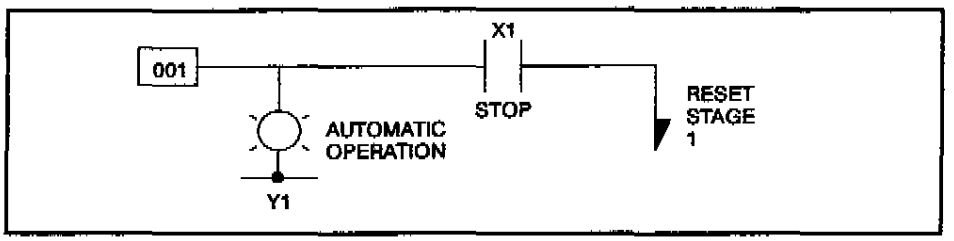


Figure 6-26 Intermediate Example—Stage 001

Enter the following keystrokes to program Stage 1.

Key Sequence	Display
SG (STAGE) 1 ENT	SG S1
OUT (YOUT) 1 ENT	OUT Y1
STR (XIN) 1 ENT	STR X1
RST (STAGE) 1 ENT	RST S1

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Entering Stage 002

Figure 6-27 shows the complete Stage 2 program.

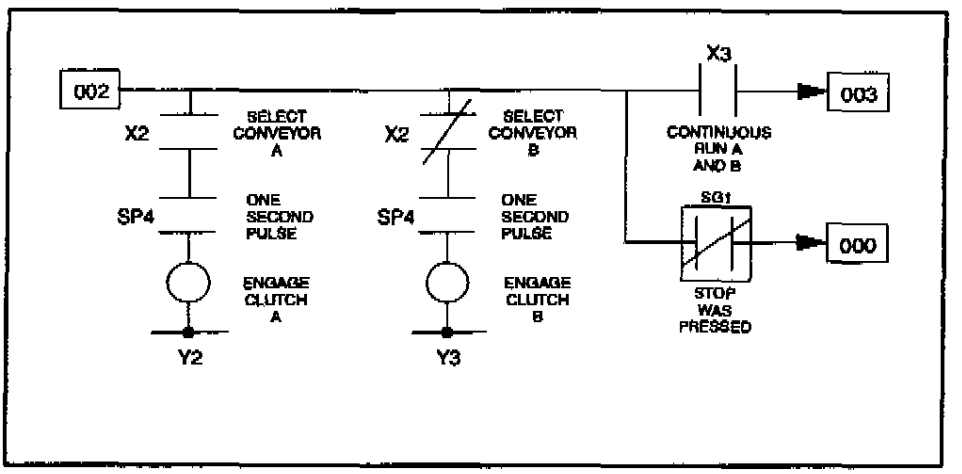


Figure 6-27 Intermediate Example—Stage 002

Enter the following keystrokes to program Stage 2.

Key Sequence	Display
SG [S(SG)] 2 ENT	SG S2
STR [X(IN)] 2 ENT	STR X2
AND [SP/CL] 4 ENT	AND SP4
OUT [Y(OUT)] 2 ENT	OUT Y2
STR NOT [X(IN)] 2 ENT	STRN X2
AND [SP/CL] 4 ENT	AND SP4
OUT [Y(OUT)] 3 ENT	OUT Y3
STR [X(IN)] 3 ENT	STR X3
JMP [S(SG)] 3 ENT	JMP S3
STR NOT [S(SG)] 1 ENT	STRN S1
JMP [S(SG)] 0 ENT	JMP S0

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Entering Stage 003

Figure 6-28 shows the complete Stage 3 program.

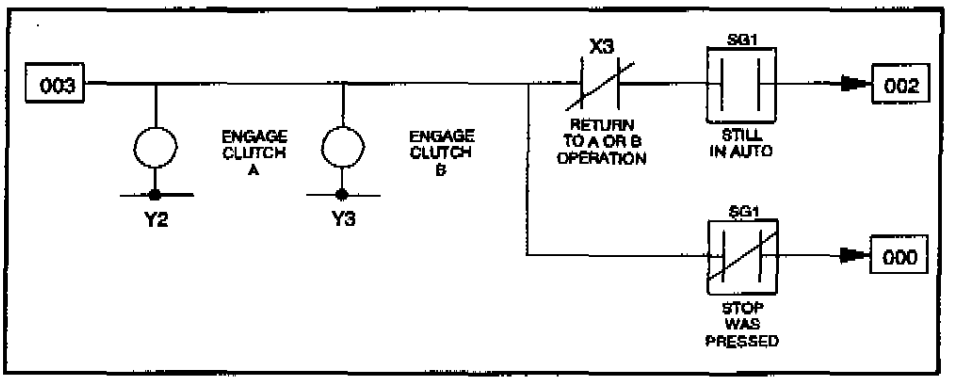


Figure 6-28 Intermediate Example—Stage 003

Enter the following keystrokes to program Stage 3.

Key Sequence	Display
SG [SHIFT] 3 ENT	SG S3
OUT Y(OUT) 2 ENT	OUT Y2
OUT Y(OUT) 3 ENT	OUT Y3
STR NOT X(IN) 3 ENT	STRN X3
AND [SHIFT] 1 ENT	AND S1
JMP [SHIFT] 2 ENT	JMP S2
STR NOT [SHIFT] 1 ENT	STRN S1
JMP [SHIFT] 0 ENT	JMP S0

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Running the Program

To run the program, enter the following key sequence.

Key Sequence	Display
CLR CLR 1 1 AUX	AUX 1* OPERATING Mode AUX 11 Go To RUN Mode
ENT	RUN Mode?
ENT	Mode = RUN

Program Operation

The program starts executing at initial Stage 0 (S0). Y0 is on until the X0 Start switch is closed. Closing X0 allows a jump to both Stage 1 (S1) and Stage 2 (S2). Stage 1 turns on Y1 and waits until the X1 Stop switch is closed. When X1 is closed, Stage 1 is reset and Y1 is turned off until the next jump to Stage 1.

Stage 2 pulses either Y2 or Y3, depending on the state of X2. SP4 is a special relay that is on for 0.5 seconds and off for 0.5 seconds. Closing X3 allows a jump to Stage 3. If Stage 1 becomes inactive at any time, program execution is forced back to Stage 0.

Stage 3 turns on both Y2 and Y3 continuously until either X3 is turned off and that allows a jump back to Stage 2, or Stage 1 becomes inactive, and that forces a jump back to Stage 0.

Ending the Program

To end programming, enter the following key sequence.

Key Sequence	Display
End ENT	End

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Diagram Symbols

The advanced stage programming example uses five additional symbols. See Figure 6-29. The sequence nnn represents a three-digit stage number.

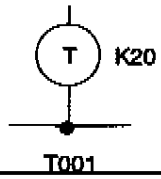
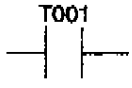
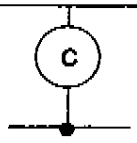
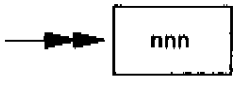
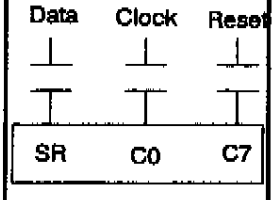
Symbol	Name	Description
	Timer	The timer times up from zero in 0.1-second intervals. The K20 gives this timer a preset of 20 intervals, or two seconds. A timer is reset when the stage containing it becomes inactive.
	Timer Contact	This contact closes when the current value in the timer with the corresponding reference number (T001) is greater than or equal to its preset.
	Counter	The counter increments once every time it sees a low to high transition on its input. Counters retain their current counts until reset by the RST instruction.
	Set Stage	Activate the indicated stage without leaving the current stage. The set stage remains active until it is reset, or a jump to another stage is made from the set stage.
	Shift Register	When a low to high transition is seen on the clock input, the current on or off states of the contacts in the chain defined by the two C numbers in the SR box are shifted to the next higher contact. The state of the data contact is shifted into the first contact (C0) and the previous state of the last contact (C7) is lost. Closing the reset contact turns off all the contacts in the chain.

Figure 6-29 Advanced Stage Diagram Symbols

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Product Finishing Example

Figure 6-30 shows the machine to be controlled by this example program.

- Two different products arrive intermixed on a conveyor. One product of either type arrives each second.
- Each requires a different set of finishing operations. The taller of the two products trips a diverter switch at the end of the infeed conveyor. This swings a diverter gate to its extended position and allows the tall product to be moved onto the appropriate finishing line.
- The gate remains extended for one second, and then returns to its retracted position, ready to divert the next product onto the short finishing line.

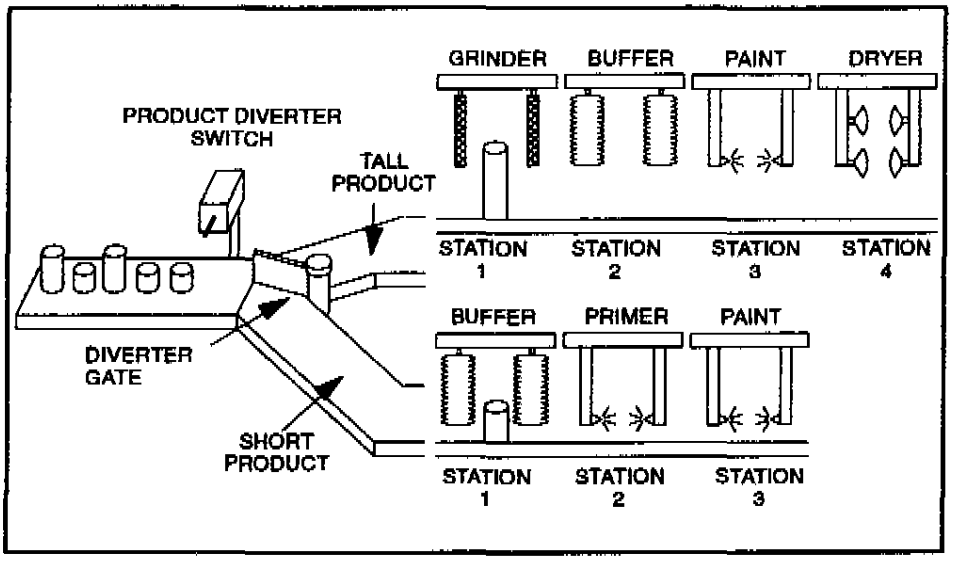


Figure 6-30 Product Finishing Example

The finishing line conveyors advance for one second, then stop for two seconds while each operation takes place. The operation at each finishing station only takes place if a product is present at that station.

The tall product finishing line has four stations. The product is first run through a grinder to remove rough edges. The conveyor then advances for one second to move it to the buffer station where the product is polished. The next station paints the product, and the last bakes the paint to dry it. Every time a drying operation takes place, the count of finished tall product is incremented.

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The short product finishing line has only three stations. The product is buffed, primed and painted in three two-second operations at stations that are one second of conveyor travel apart. Every time a product is painted at station three, the finished short product count is incremented.

Figure 6-31 shows a stage program to control the example machine. Stage 0 illuminates the Ready to Start light (Y0) until the start button (X0) is pressed. This resets the finished product counters and allows a jump to Stage 1 and Stage 2. Y0 is turned off when the jump occurs.

- Stage 1 starts timer T0, that is used in Stage 2 to provide a two second delay for the conveyor motors to start. An Automatic Operation light (Y4) is illuminated, and the conveyor motor output (Y5) is turned on. These stay on until the stop button (X1) is pressed, and resets all stages, allowing the jump back to Stage 0.

- Stage 2 delays the operation of the rest of the machine for two seconds, until timer T0 in Stage 1 reaches its preset, and closes timer contact T0. This allows a jump to Stage 3.

- Stage 3 resets Stage 10, that turns off all outputs in that stage. This has no effect the first time Stage 3 is active, since Stage 10 has yet to be activated. However, on subsequent jumps to Stage 3, both conveyor clutches controlled by Stage 10 are turned off to stop conveyor movement, and the diverter gate is retracted.

- Stage 4 starts timer T1, and then sets Stages 11 through 17 (if the corresponding control relays are energized). The control relays are turned on or off by the product shift registers in Stages 6 and 7, so the result is that the output (Y10 through Y16) controlling the operation at any station is activated only if a product is present at that station. When a stage is set, its I/O points become active, but, unlike a jump to a stage, the previous stage remains active and executing. Stage 20 is also set, and activates the finished product counters. These increment whenever the last operation on the appropriate product line occurs. After the selected operations have run for two seconds, timer contact T1 closes and allows a jump to Stage 5. When Stage 4 becomes inactive, timer T1 is reset until the next jump into this stage.

- Stage 5 resets Stages 11 through 17. This disables the outputs in these seven stages, and stops all finishing operations on both lines, in preparation for conveyor movement. A one-second timer (T2) is started, and Stages 6, 7, and 10 are set. Stages 6 and 7 enable the appropriate shift register to record the entry of a product onto one of the finishing lines. Stage 10 engages the clutches to advance the conveyor, and extends the diverter gate if a tall product is being loaded. After one second of conveyor movement, timer contact T2 closes and allows a jump back to Stage 3, that disengages the conveyor clutches and starts another two second finishing operation cycle.

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- Stages 6 and 7 are both active at the same time, since when one line shifts in an on-state to indicate receiving a product, the other line has to shift in an off-state to indicate a gap in its row of products. This keeps track of products present at each finishing station on both lines. The state of X2, on when a tall product is loaded, and off when a short product is loaded, determines which shift register records receiving the product. The state of Stage 10 is used as a clock signal to shift the on and off states through the chain of control relays, indicating the presence or absence of a product at each station. This is a natural choice, since Stage 10 is active when the conveyor is moving (physically shifting the products between finishing stations). Closing X3 clears both shift registers. This could be used to reset the machine if it had been stopped, and the unfinished parts have been manually removed from both lines.

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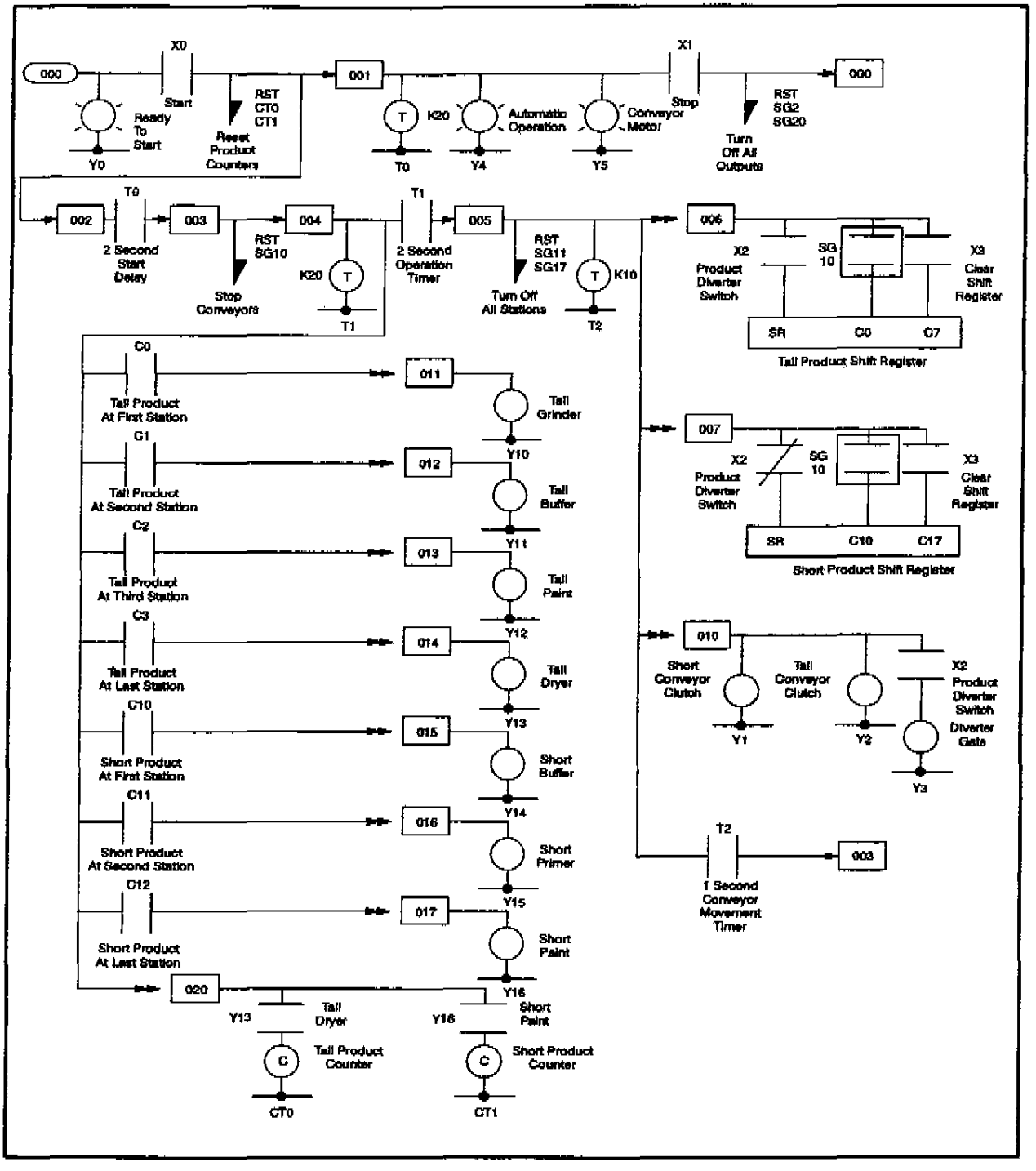


Figure 6-31 Stage Program for Product Finishing

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Entering Stage 000

Figure 6-32 shows the complete Stage 0 program.

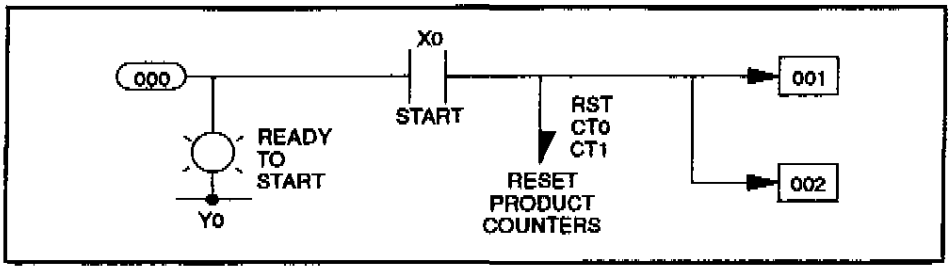


Figure 6-32 Advanced Example—Stage 000

Enter the following keystrokes to program Stage 0. Shaded keys [ ] represent the blue colored symbol identification keys on the MIU.

Key Sequence	Display
[ISG] [SHIFT] [0] [ENT]	ISG S0
[OUT] [SHIFT] [Y] [0] [ENT]	OUT Y0
[STR] [SHIFT] [X] [0] [ENT]	STR X0
[RST] [CNT] [0] [CNT] [1] [ENT]	RST CT0 CT1
[JMP] [SHIFT] [S] [1] [ENT]	JMP S1
[JMP] [SHIFT] [S] [2] [ENT]	JMP S2

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Entering Stage 001

Figure 6-33 shows the complete Stage 1 program.

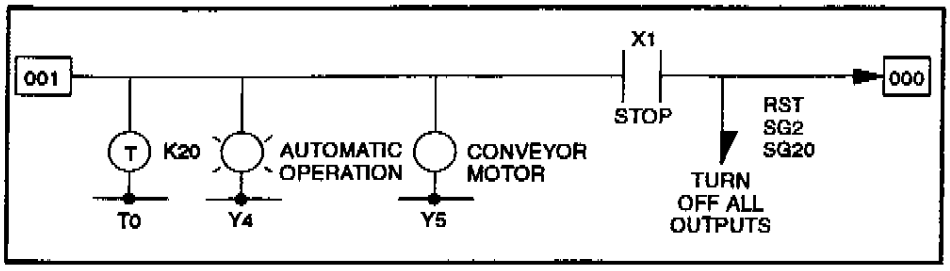


Figure 6-33 Advanced Example—Stage 001

Enter the following keystrokes to program Stage 1.

Key Sequence	Display
SG (SHIFT) 1 ENT	SG S1
TMR (TMR) 0 (K/CONS) 2 0 ENT	TMR to K20
OUT (Y/OUT) 4 ENT	OUT Y4
OUT (Y/OUT) 5 ENT	OUT Y5
STR (X/NO) 1 ENT	STR X1
RST (SHIFT) 2 (SHIFT) 2 0 ENT	RST S2 S20
JMP (SHIFT) 0 ENT	JMP S0

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Entering Stage 002

Figure 6-34 shows the complete Stage 2 program.

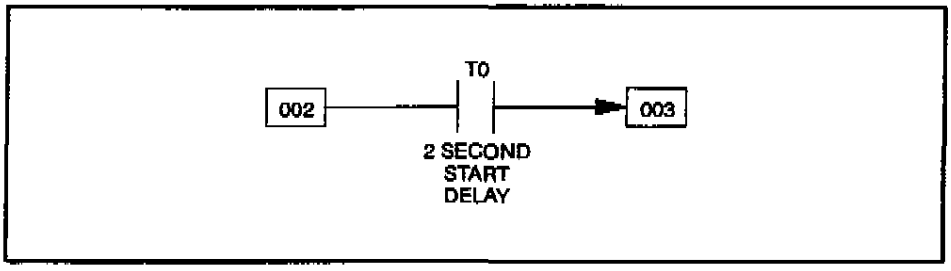


Figure 6-34 Advanced Example—Stage 002

Enter the following keystrokes to program Stage 2.

Key Sequence	Display
SG S(SG) 2 ENT	SG S2
STR TMR 0 ENT	STR T0
JMP S(SG) 3 ENT	JMP S3

Entering Stage 003

Figure 6-35 shows the complete Stage 3 program.

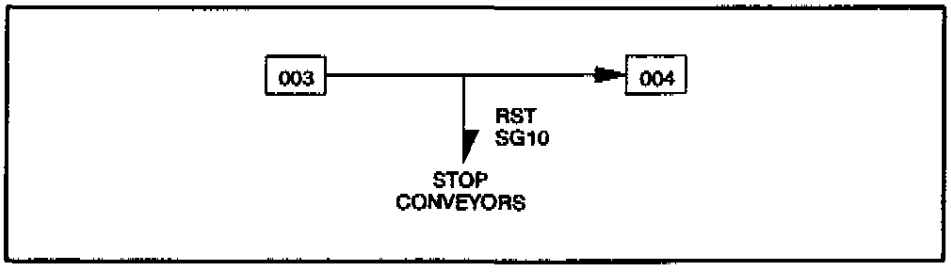


Figure 6-35 Advanced Example—Stage 003

Enter the following keystrokes to program Stage 3.

Key Sequence	Display
SG S(SG) 3 ENT	SG S3
RST S(SG) 1 0 ENT	RST S10
JMP S(SG) 4 ENT	JMP S4

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Entering Stage 004

Enter the following keystrokes to program Stage 4. Figure 6-36 shows the complete Stage 4 program.

Key Sequence	Display
SG S(SG) 4 ENT	SG S4
TMR TMR 1 K(CON) 2 0 ENT	TMR T1 K20
STR TMR 1 ENT	STR T1
JMP S(SG) 5 ENT	JMP S5
STR C(CR) 0 ENT	STR C0
SET S(SG) 1 1 ENT	SET S11
STR C(CR) 1 ENT	STR C1
SET S(SG) 1 2 ENT	SET S12
STR C(CR) 2 ENT	STR C2
SET S(SG) 1 3 ENT	SET S13
STR C(CR) 3 ENT	STR C3
SET S(SG) 1 4 ENT	SET S14
STR C(CR) 1 0 ENT	STR C10
SET S(SG) 1 5 ENT	SET S15
STR C(CR) 1 1 ENT	STR C11
SET S(SG) 1 6 ENT	SET S16
STR C(CR) 1 2 ENT	STR C12
SET S(SG) 1 7 ENT	SET S17
SET S(SG) 2 0 ENT	SET S20

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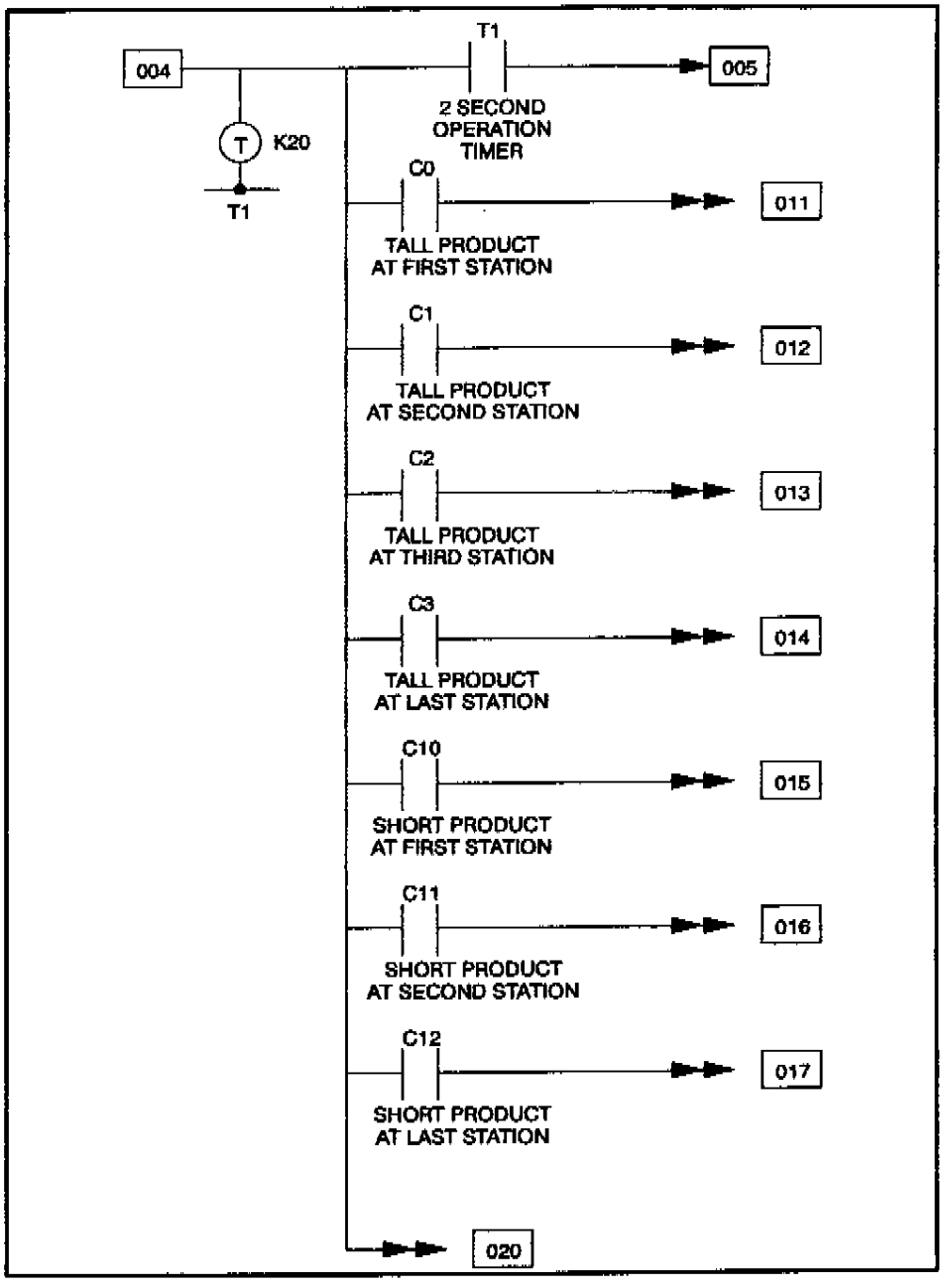


Figure 6-36 Advanced Example—Stage 004

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Entering Stage 005

Figure 6-37 shows the complete Stage 5 program.

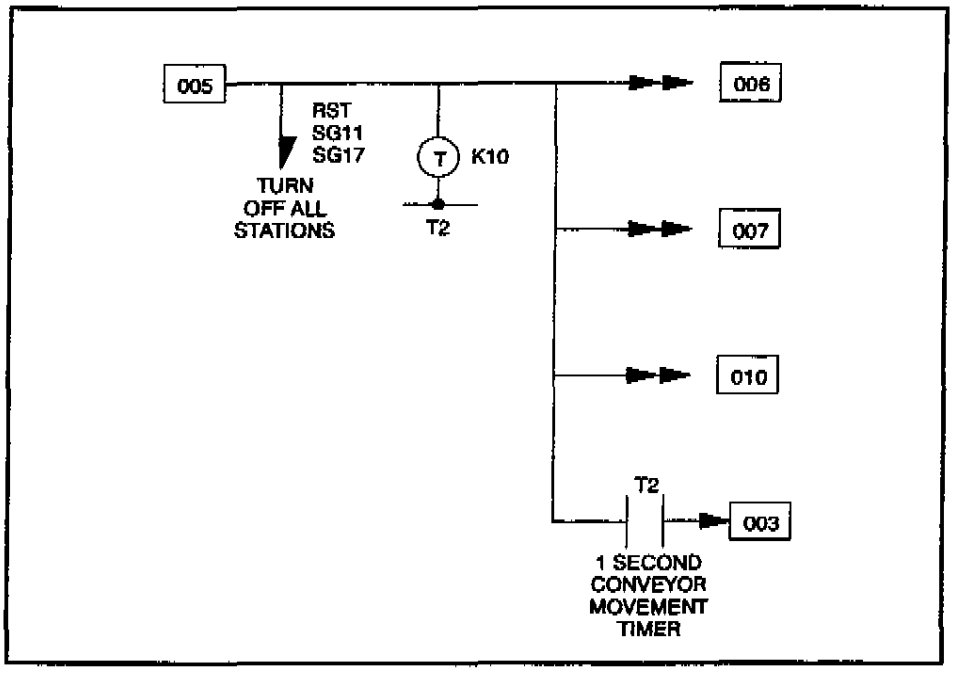


Figure 6-37 Advanced Example—Stage 005

Enter the following keystrokes to program Stage 5.

Key Sequence	Display
SG [S(SG)] 5 ENT	SG S5
RST [S(SG)] 1 1 [S(SG)] 1 7 ENT	RST S11 S17
TMR TMR 2 [K(CONS)] 1 0 ENT	TMR T2 K10
SET [S(SG)] 6 ENT	SET S6
SET [S(SG)] 7 ENT	SET S7
SET [S(SG)] 1 0 ENT	SET S10
STR TMR 2 ENT	STR T2
JMP [S(SG)] 3 ENT	JMP S3

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Entering Stage 006

Figure 6-38 shows the complete Stage 6 program.

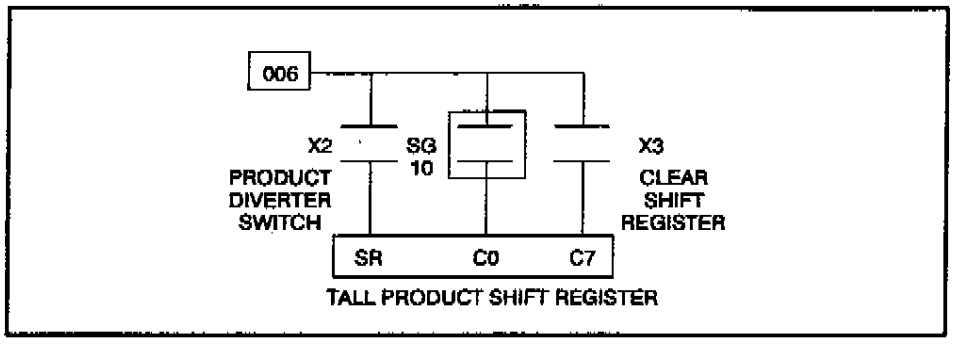


Figure 6-38 Advanced Example—Stage 006

Enter the following keystrokes to program Stage 6.

Key Sequence	Display
SG (SHIFT) 6 ENT	SG S6
STR (X/INS) 2 ENT	STR X2
STR (S/SHIFT) 1 0 ENT	STR S10
STR (X/INS) 3 ENT	STR X3
SR (C/CR) 0 (C/CR) 7 ENT	SR C0 C7

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Entering Stage 007

Figure 6-39 shows a complete Stage 7 program.

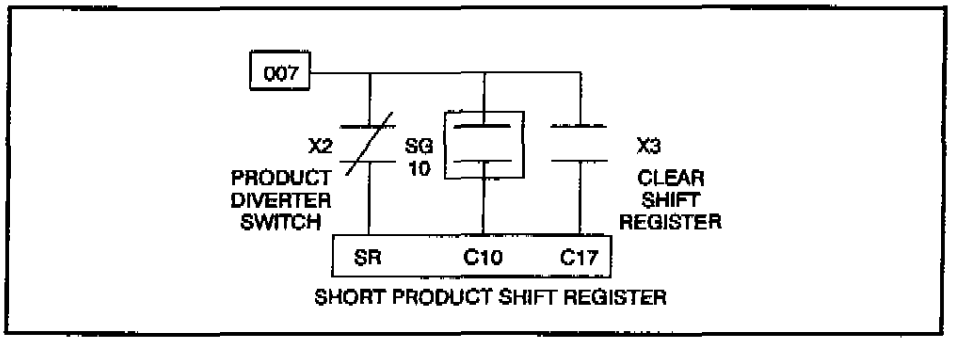


Figure 6-39 Advanced Example—Stage 007

Enter the following keystrokes to program Stage 7.

Key Sequence	Display
SG S(SGI) 7 ENT	SG S7
STR NOT X(INP) 2 ENT	STRN X2
STR S(SGI) 1 0 ENT	STR S10
STR X(INP) 3 ENT	STR X3
SR C(CR) 1 0 C(CR) 1 7 ENT	SR C10 C17

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Entering Stage 010

Figure 6-40 shows a complete Stage 10 program.

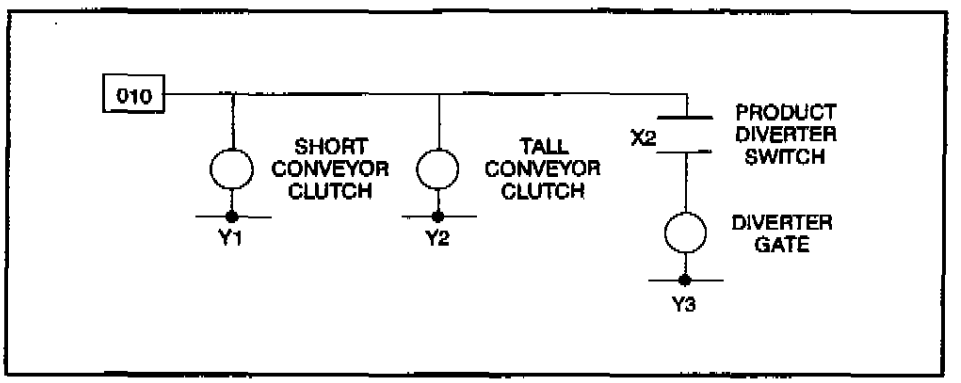


Figure 6-40 Advanced Example—Stage 010

Enter the following keystrokes to program Stage 10.

Key Sequence	Display
SG S(SET) 1 0 ENT	SG S10
OUT Y(OUT) 1 ENT	OUT Y1
OUT Y(OUT) 2 ENT	OUT Y2
STR X(RD) 2 ENT	STR X2
OUT Y(OUT) 3 ENT	OUT Y3

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Entering Stage 011

Figure 6-41 shows a complete Stage 11 program.

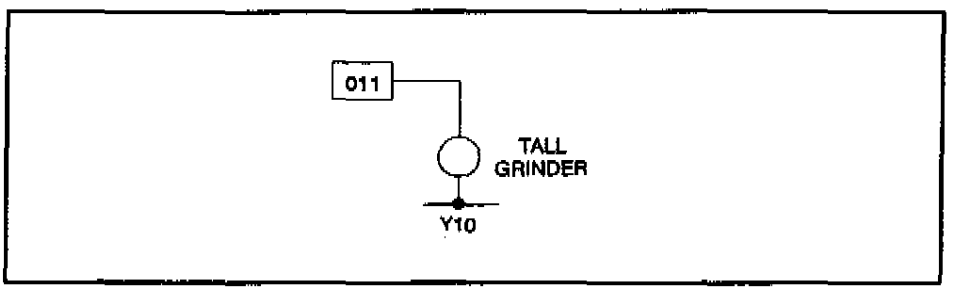


Figure 6-41 Advanced Example—Stage 011

Enter the following keystrokes to program Stage 11.

Key Sequence	Display
SG (SHIFT) 1 1 ENT	SG S11
OUT (SHIFT) 1 0 ENT	OUT Y10

Entering Stage 012

Figure 6-42 shows a complete Stage 12 program.

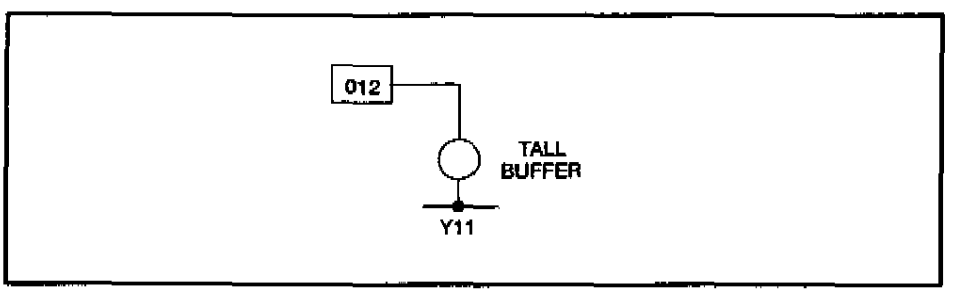


Figure 6-42 Advanced Example—Stage 012

Enter the following keystrokes to program Stage 12.

Key Sequence	Display
SG (SHIFT) 1 2 ENT	SG S12
OUT (SHIFT) 1 1 ENT	OUT Y11

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Entering Stage 013

Figure 6-43 shows the complete Stage 13 program.

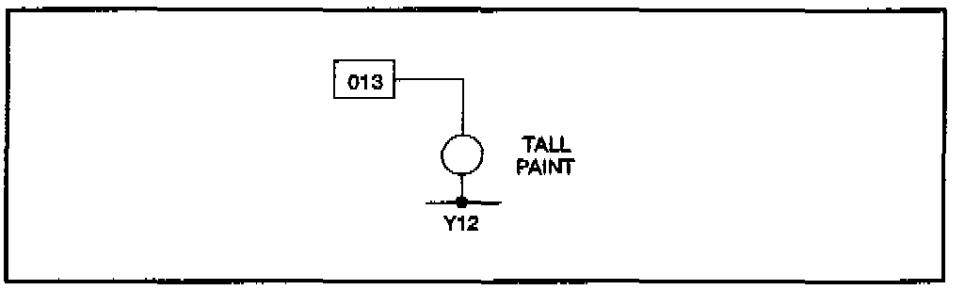


Figure 6-43 Advanced Example—Stage 013

Enter the following keystrokes to program Stage 13.

Key Sequence	Display
SG (#SG) 1 3 ENT	SG S13
OUT (#OUT) 1 2 ENT	OUT Y12

Entering Stage 014

Figure 6-44 shows the complete Stage 14 program.

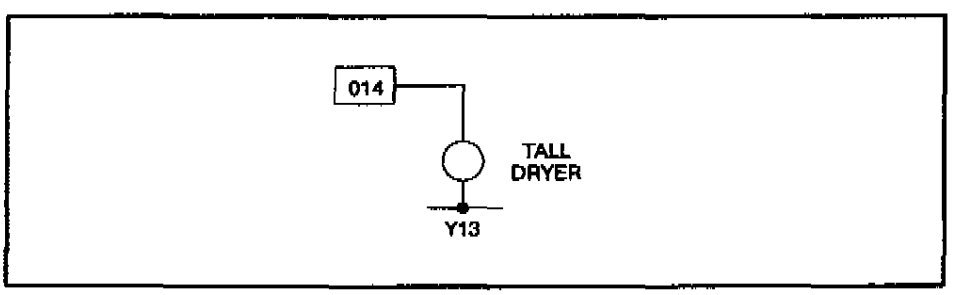


Figure 6-44 Advanced Example—Stage 014

Enter the following keystrokes to program Stage 14.

Key Sequence	Display
SG (#SG) 1 4 ENT	SG S14
OUT (#OUT) 1 3 ENT	OUT Y13

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Entering Stage 015

Figure 6-45 shows the complete Stage 15 program.

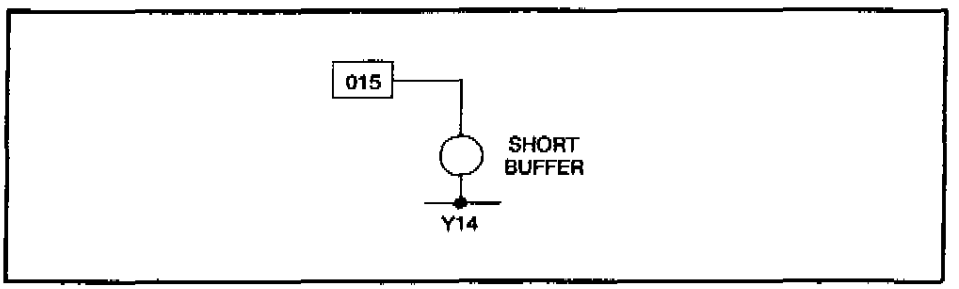


Figure 6-45 Advanced Example—Stage 015

Enter the following keystrokes to program Stage 15.

Key Sequence	Display
SG S(SG) 1 5 ENT	SG S15
OUT Y(OUT) 1 4 ENT	OUT Y14

Entering Stage 016

Figure 6-46 shows a complete Stage 16 program.

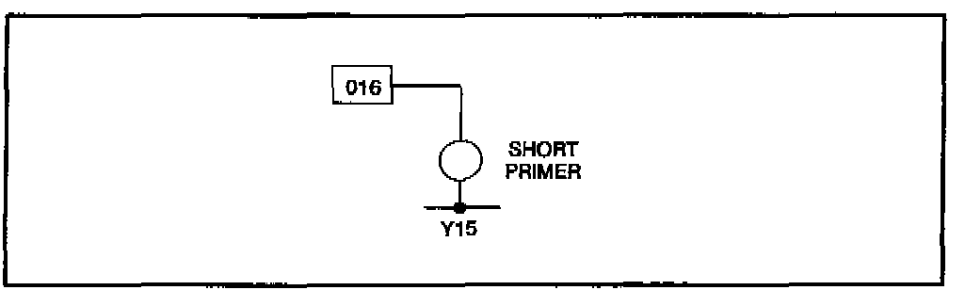


Figure 6-46 Advanced Example—Stage 016

Enter the following keystrokes to program Stage 16.

Key Sequence	Display
SG S(SG) 1 6 ENT	SG S16
OUT Y(OUT) 1 5 ENT	OUT Y15

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Entering Stage 017

Figure 6-47 shows a complete Stage 17 program.

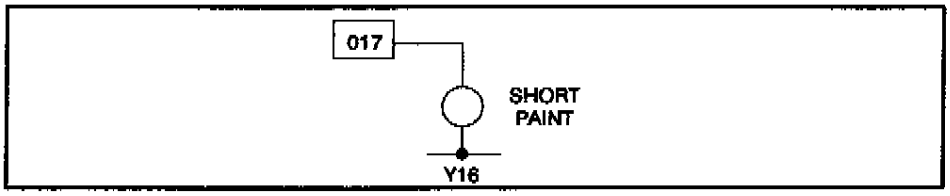


Figure 6-47 Advanced Example—Stage 017

Enter the following keystrokes to program Stage 17.

Key Sequence	Display
SG S/(S1) 1 7 ENT	SG S17
OUT Y/(OUT) 1 6 ENT	OUT Y16

Entering Stage 020

Figure 6-48 shows a complete Stage 20 program.

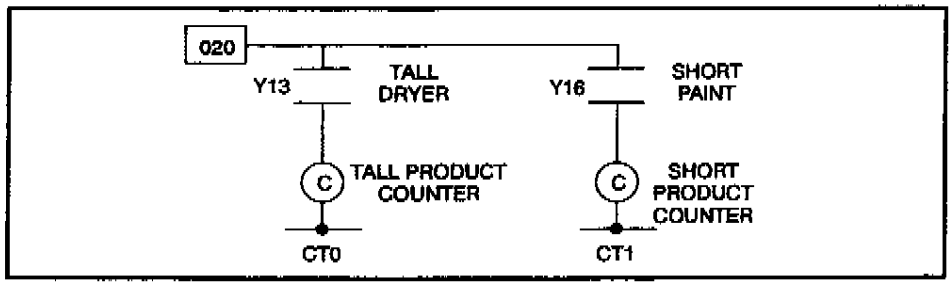


Figure 6-48 Advanced Example—Stage 020

Enter the following keystrokes to program Stage 20.

Key Sequence	Display
SG S/(S1) 2 0 ENT	SG S20
STR Y/(OUT) 1 3 ENT	STR Y13
SG CNT CNT 0 K/CON 9 9 9 9 ENT	SGCNT CT0 K9999
STR Y/(OUT) 1 6 ENT	STR Y16
SG CNT CNT 1 K/CON 9 9 9 9 ENT	SGCNT CT1 K9999

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Running the Program

To run the program, enter the following key sequence.

Key Sequence	Display
CLR CLR 1 1 AUX	AUX 1* Operating Mode AUX 11 Go To Run Mode
ENT	Run Mode
ENT	Mode = Run

Program Operation

The program starts executing at initial Stage 0 (S0). Y0 is on until the X0 start switch is closed. Closing X0 allows a jump to both Stage 1 (S1) and Stage 2 (S2). Stage 1 starts the two-second timer T0 and turns on outputs Y4 and Y5. Stage 1 then waits until the X1 stop switch is closed. When X1 is closed, Stage 1 resets all stages; this turns off all output points, and jumps to Stage 0. Figure 6-49 shows the input module indicators used in this example.

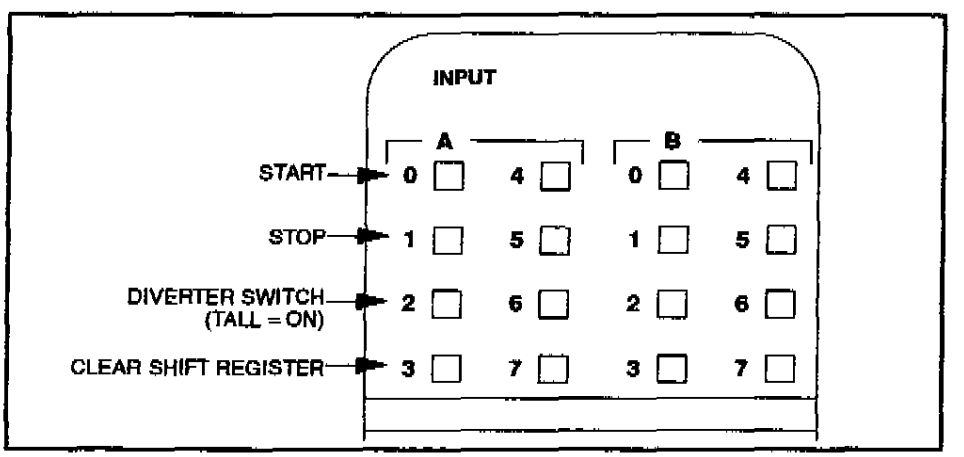


Figure 6-49 Input Module Indicators

Ending the Program

To end programming, enter the following key sequence.

Key Sequence	Display
END ENT	End

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Executing the Program

Stage 2 delays operation of the machine for two seconds until timer contact T0 closes. This ends the startup section of the program, and execution jumps to Stage 3, where the main flow of the operation begins.

Stage 3 has no effect on machine operation the first time it executes, but on subsequent jumps to this stage, the conveyors are stopped by the reset of Stage 10.

Stage 4 starts the two-second timer, T1, that controls the length of time this stage is active. For two seconds, until timer contact T1 closes, any of the finishing stations that have a product present are activated. Control relays C0 through C12 are turned on or off by the shift registers in Stages 6 and 7, that keep track of the position of each product on the finishing lines. The set stage instructions used to activate the finishing operation stages allow Stage 4 to activate other stages without jumping to them. This allows Stage 4 to continue executing after it has activated the other stages. Timer T1 is reset when the jump to Stage 5 is made. Figure 6-50 shows the output module indicators used in this example.

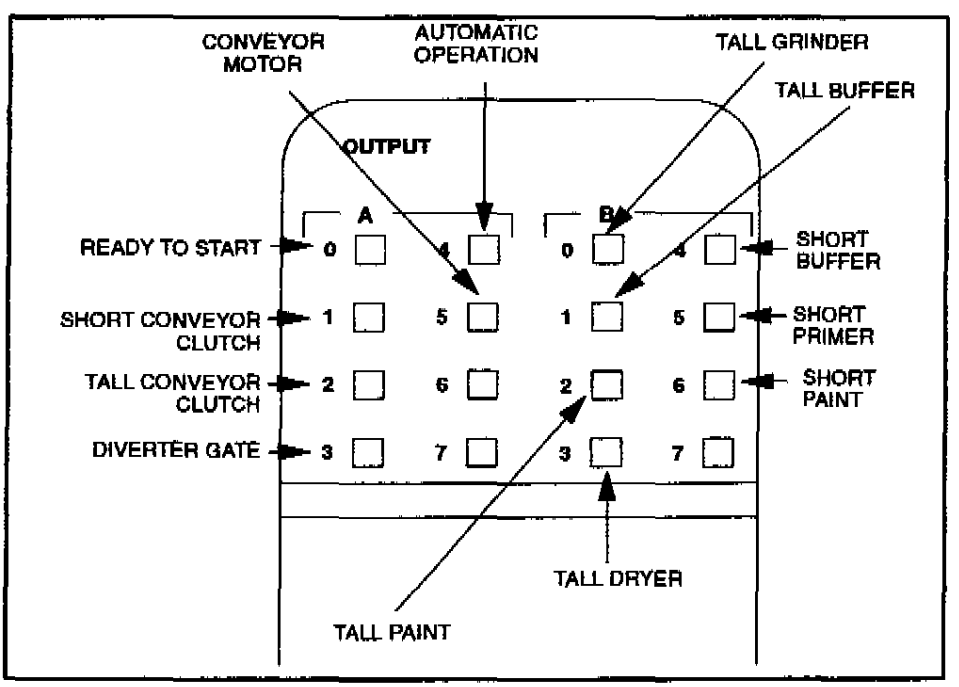


Figure 6-50 Output Module Indicators

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Stage 5 resets the stages that were set by Stage 4. This turns off any of the finishing operation outputs in preparation for moving the conveyor. One-second timer T2 is started; this controls the time that this stage is active before jumping back to Stage 3. Stages 6, 7 and 10 are set, and Stage 5 remains active until timer contact T2 closes and the jump to Stage 3 is made. Timer T2 is reset with the jump.

Stage 6 activates the shift register that records the position of the product on the tall line. Each time a tall product is loaded, X2 is closed. The on state of this contact is clocked into the tall shift register when Stage 10 becomes active and the product is moved to the first finishing station. At the same time, an off state is clocked into the short shift register in Stage 7. Since both conveyors advance together, and the tall product was diverted onto the tall finishing line, a gap is left in the row of product on the short finishing line. By shifting an off state through the short shift register, none of the finishing operations is activated as the empty space passes. Closing X3 resets all the control relays in the shift registers to an off state.

Stage 7 operates the same as Stage 6, except that the opposite state of X2 is clocked into the short product shift register. Since X2 is only closed when a tall product is loaded onto the finishing line, when a short product passes the switch is open, and an on state is clocked into the short shift register. An off state is clocked into the tall product shift register, since this time a gap is left in the row of tall products. Notice that both shift registers are programmed with eight control relays, even though not all of them are needed. Shift registers in the TI405 CPU must use control relays in groups of eight, and the first relay number in the shift register must be a multiple of eight (0, 10, 20, 30, etc.). Remember that all TI405 I/O points are numbered in octal, and that is why control relay number 10 is a multiple of eight.

Since stages are numbered in octal, the numerals 8 and 9 cannot be used in stage numbers. This means that the next stage after Stage 7 is Stage 10. When active, this stage turns on Y1 and Y2, and engage the clutches to run both conveyors. If a tall product is being loaded, X2 is closed and Y3 is turned on to extend the diverter gate and guide the product onto the correct conveyor. These outputs stay on for one second, until execution jumps back to Stage 3 and Stage 10 is reset.

Stages 11 through 17 each simply turn on an output when set, and turn it back off when reset.

Stage 20 activates the finished product counters. When a product reaches the last finishing operation, the appropriate counter is incremented. Since stage counters retain their current counts, even when their stage is not active, the product count is retained after the machine is stopped. The counters are only reset after the start button (X1) is pressed.

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After the stage example program is running, its status can be monitored several ways. Figure 6-50 shows the indicators on the TI405 output module that correspond to the program operation. Figure 6-49 shows the same information for the input module.

The active stages can be monitored with the MIU by entering the following key sequence.

Key Sequence

CLR CLR [illegible] 0 BIT ST

Figure 6-51 shows how the MIU display appears if stages 1, 4, 6, 7, 12, 15, and 17 were active.

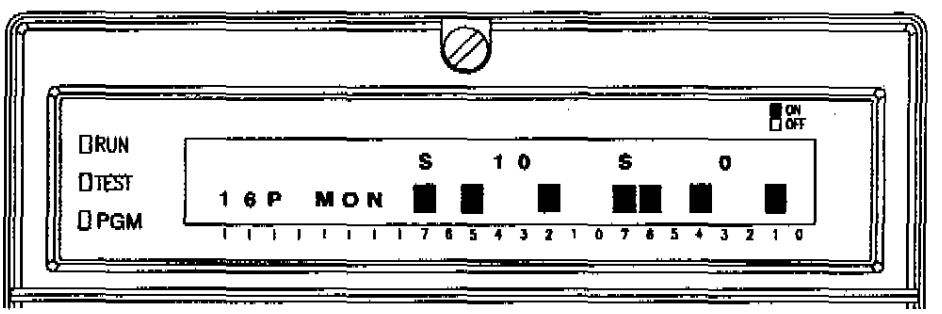


Figure 6-51 Active Stages Monitor Display

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Current counter values are stored in V-memory locations that are 1000 greater than the counter number. Counter 000's current count is found at V1000, and counter 001 at V1001. The finished product count can be viewed by entering the following key sequence.

Key Sequence

CLR CLR V 1 0 0 0 WD ST

Figure 6-52 shows how the MIU display appears if 9 tall products and 23 short products had been finished.

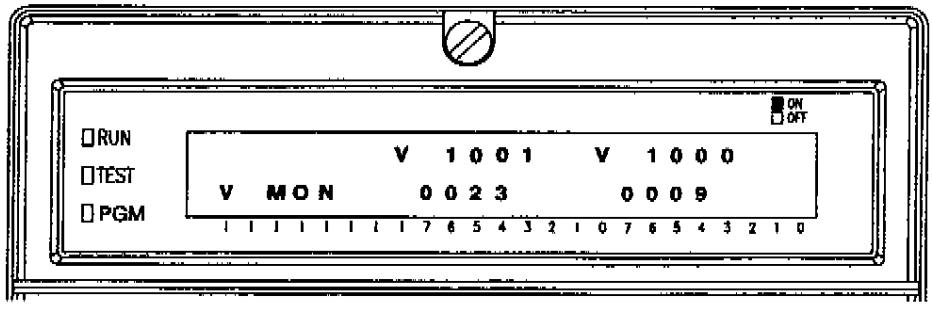


Figure 6-52 Product Count Display

Current timer values are stored in V-memory locations that are equal to the timer number. The current timer values for timer 000 and 001 can be viewed on the MIU by entering the following key sequence.

Key Sequence

CLR CLR V 0 WD ST

Notice that timer 000 does not stop at its preset of 20, but continues to time up to 9999. You may use NXT and PREV to view other timer current values on the MIU. Figure 6-53 shows how the display appears if timer 000 had been running for 68.3 seconds and timer 001 for 1.3 seconds.

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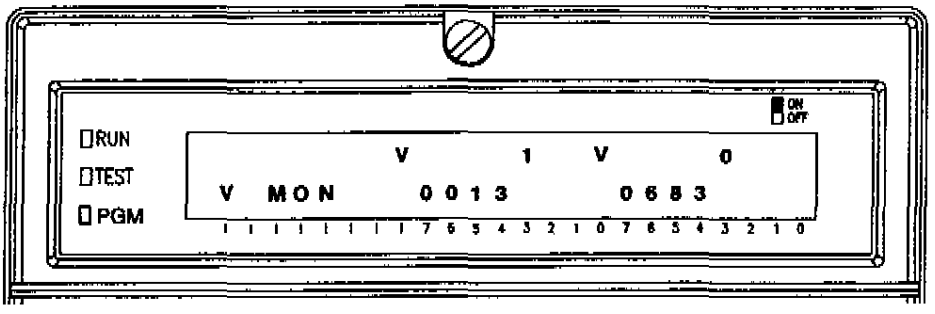


Figure 6-53 Current Timer Values Display

Groups of sixteen I/O points can be monitored on the MIU. The following key sequence shows how to monitor Y0 through Y17.

Use [NXT] and [PREV] to view the status of other Y points. Figure 6-54 shows how the MIU display appears if Y1, Y2, Y4, Y5 and Y14 were on.

Key Sequence

[CLR] [CLR] [Y(OUT)] [0] [INT ST]

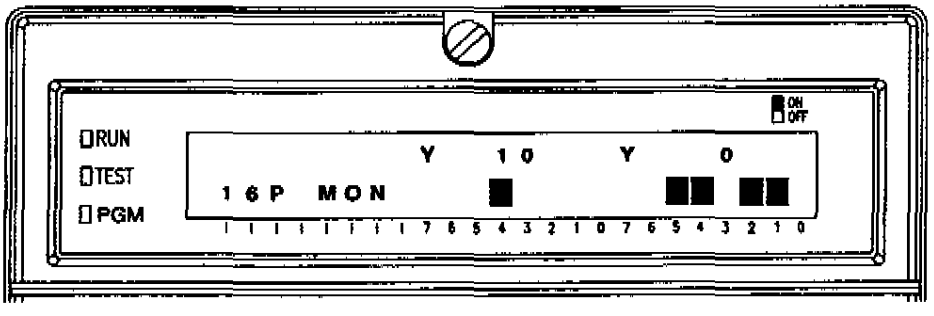


Figure 6-54 I/O Monitor Display

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Chapter 7
Application Examples

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Figure 7-1 and Figure 7-2 illustrate a simple Start/Stop circuit. Switch X1 is a normally closed switch that has power flowing until it is pressed. When Switch X0 is pressed and released, power flows to the coil Y1, controlling current to the motor. On the following scans, the circuit continues to supply power flow to Y1, until Switch X1 is pressed.

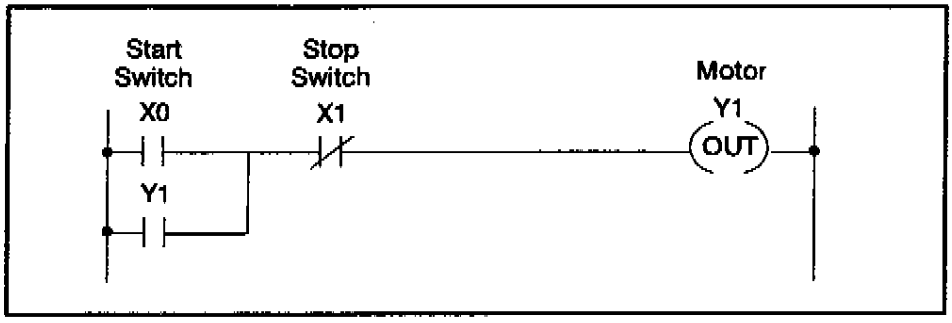


Figure 7-1 Start/Stop RLL Circuit

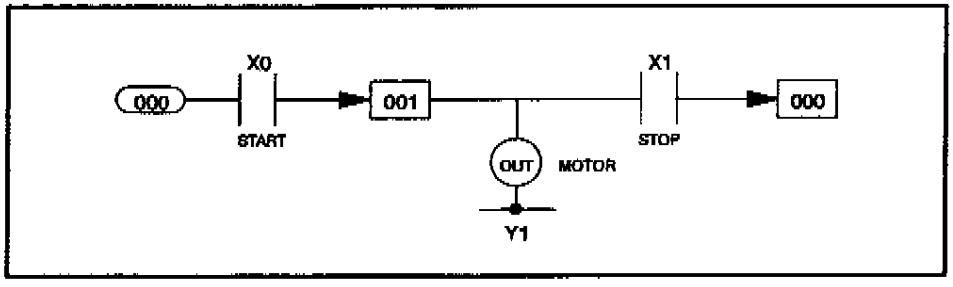


Figure 7-2 Start/Stop Stage Circuit

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7.2 System Start-up Horn

Figure 7-3 and Figure 7-4 illustrate a system start-up horn RLL program. When the operator presses the start switch, the timer T4 begins counting for five seconds and the horn output coil is energized. When the timer times out or the reset switch is pressed, the horn output coil is turned off.

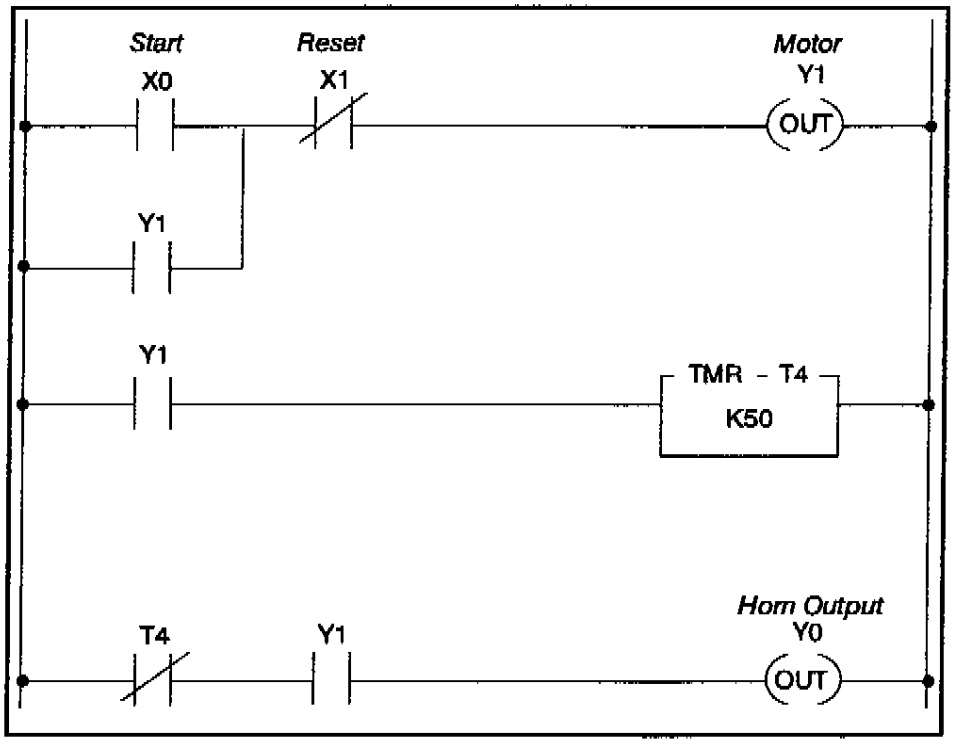


Figure 7-3 System Start-up Horn (RLL)

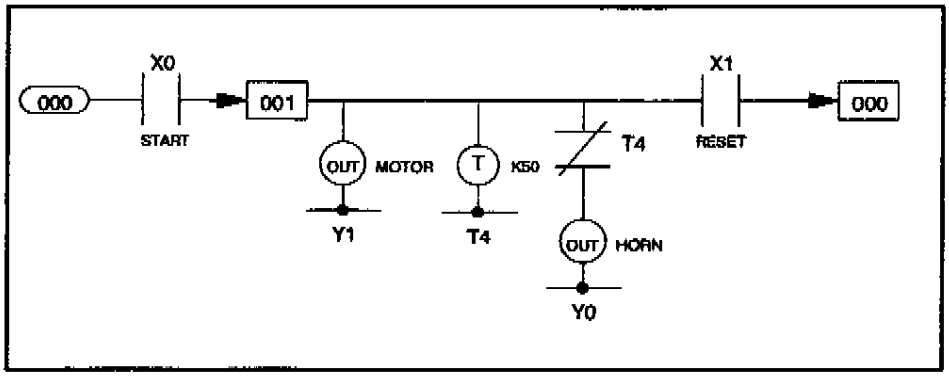


Figure 7-4 System Start-up Horn (Stage)

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7.3 Run/Jog Control

This example shows how run/jog control for a machine's main drive motor can be implemented with a Machine Stage program. You can follow this description of how the program operates by referring to the Machine Stage diagram in Figure 7-5 and the program instruction listing in Figure 7-6.

Main instructions used:

- ISG to indicate the Initial Stage
- SG to indicate all other Stages

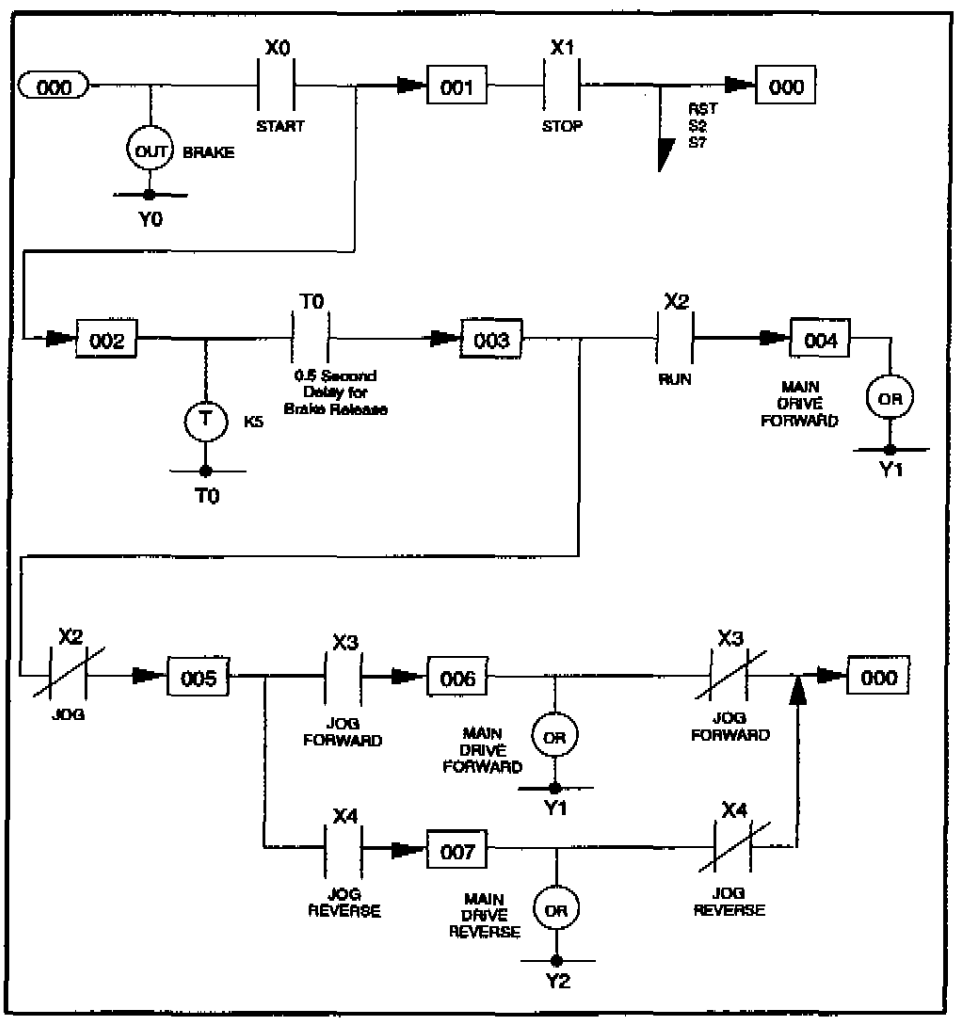


Figure 7-5 Run/Jog Control Stage

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```
$  0    ISG       S  0000
$  2    OUT       Y  0000
$  3    STR       X  0000
$  4    JMP       S  0001
$  5    JMP       S  0002
$  6    SG        S  0001
$  8    STR       X  0001
$  9    RST       S  0002   S  0007
$  11   JMP       S  0000
$  12   SG        S  0002
$  14   TMR       T  000    K  0005
$  17   STR       T  000
$  18   JMP       S  0003
$  19   SG        S  0003
$  21   STR       X  0002
$  22   JMP       S  0004
$  23   STRN      X  0002
$  24   JMP       S  0005
$  25   SG        S  0004
$  27   OROUT     Y  0001
$  28   SG        S  0005
$  30   STR       X  0003
$  31   JMP       S  0006
$  32   STR       X  0004
$  33   JMP       S  0007
$  34   SG        S  0006
$  36   OROUT     Y  0001
$  37   STRN      X  0003
$  38   JMP       S  0000
$  39   SG        S  0007
$  41   OROUT     Y  0002
$  42   STRN      X  0004
$  43   JMP       S  0000
$  44   END
```

Figure 7-6 Run/Jog Control Program Listing

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When the PLC is placed in RUN mode, program execution begins at initial stage S0. This engages the brake to keep the drive from moving until the start switch is pressed. When start is pressed, program execution jumps to Stages S1 and S2. This deactivates Stage S0 and releases the brake.

Stage 001 Operation

Stage S1 continuously monitors the stop switch. If the stop switch is pressed, all other stages in the program are reset with the RST S 0002 S 0007 instruction. This disables all the outputs in stages S2 through S7. Program execution is transferred back to Stage S0 by the JMP S 0000 instruction, that turns on the brake and stops the drive.

Stage 002 Operation

Stage S2 provides a 0.5 second delay to allow the brake to fully release before the main drive tries to put the machine into motion. This is accomplished by using the timer T0 that starts timing toward 0.5 seconds as soon as Stage S2 becomes active. After 0.5 seconds, contact T0 is turned on, energizing the JMP S 0003 instruction to activate Stage S3, and to deactivate Stage S2. Timer T0 is reset when Stage S2 is deactivated.

Stage 003 Operation

Stage S3 makes the decision to go into run or jog operation, depending on the on or off state of input X2. If X2 is on, a jump is made to Stage S4. If X2 is off, program execution jumps to Stage S5. In order to go into continuous run operation, the X2 run switch has to be pressed either before the start switch is pressed, or within 0.5 seconds afterwards. This reduces the possibility of accidentally selecting continuous run operation.

Stage 004 Operation

Stage S4 turns on output Y1, causing the main drive to run the machine forward. Since there is no contact to provide a transition condition out of Stage S4, Y1 remains on until the stop button is pressed and Stage S4 is reset. Although using an OROUT Y1 instruction, instead of an OUT Y1 instruction, is not required in this case, it is a good practice to use OROUT instructions in Machine Stage programs (in case two stages with the same output become active simultaneously).

Stage 005 Operation

Stage S5 makes the decision to jog the machine forward or backward. If X3 is turned on, a jump is made to Stage S6. If X4 is on, the jump is made to Stage S7.

Stage 006 Operation

Stage S6 energizes output Y1 and keeps it on until the jog forward switch (X3) is released. When X3 is released, program execution jumps back to Stage S0, that activates the brake and stops the machine.

Stage 007 Operation

Stage S7 energizes output Y2, that runs the machine in reverse, until the jog reverse switch is released. When input X4 turns off, program execution jumps back to Stage S0, that once again activates the brake and stops the machine.

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This following example shows how either a Machine Stage program module, or a relay ladder logic program, can display the current value of a counter on four seven-segment displays (as illustrated in Figure 7-7). This description of the operation applies equally to either method, so you can follow the Machine Stage diagram in Figure 7-8, or the relay diagram in Figure 7-10. Figure 7-9 is the Machine Stage program listing, and Figure 7-11 is the RLL program listing.

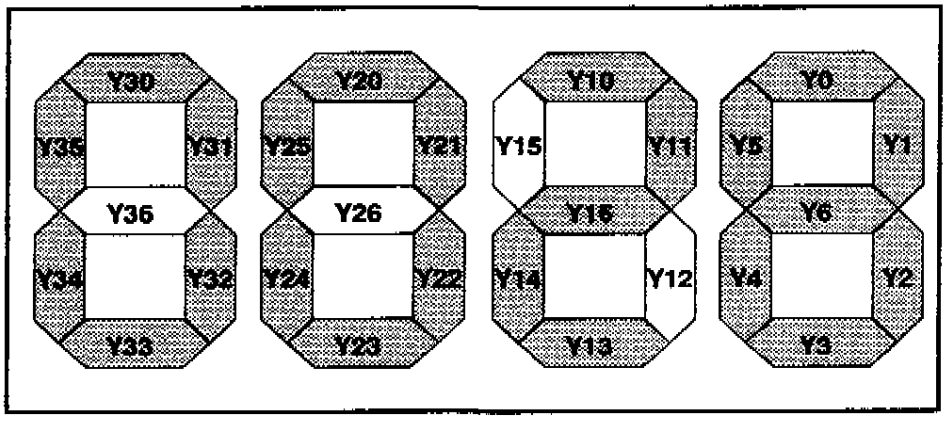


Figure 7-7 Seven-Segment Display Example

Main instructions used:

- SEG to convert a BCD number to a seven-segment display bit pattern
- OUTF to move the bit pattern to the physical outputs

Program Operation

Each time X0 makes an off-to-on transition, the current value of counter CT0, which is located in the V-memory location 1000 greater than the counter number, increases by one. This value in V1000 increments up to a maximum of 9999, unless X1 is turned on to reset the counter to zero.

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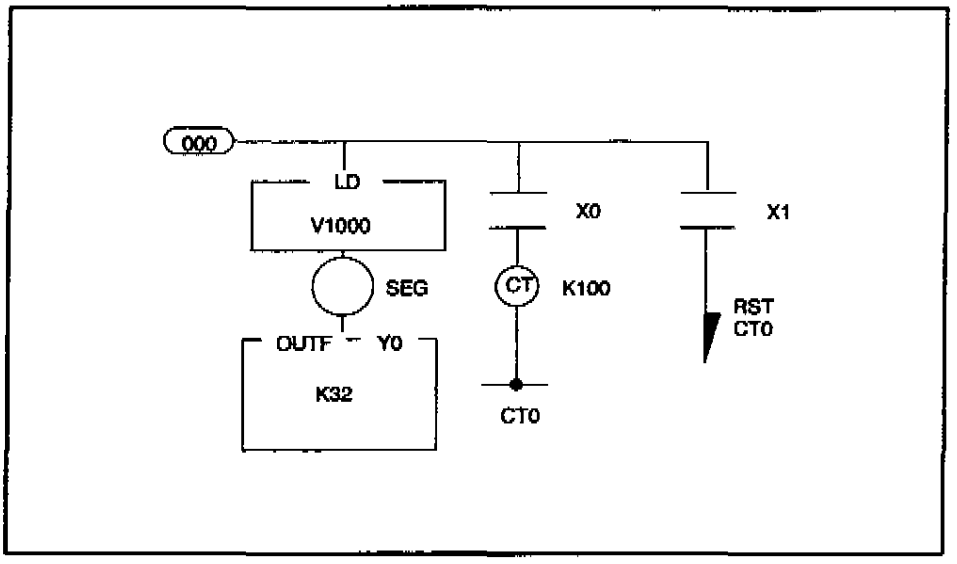


Figure 7-8 Seven-Segment Display (Stage)

```
$  0    ISG       S    0000
$  2    LD        V    01000
$  3    SEG
$  4    OUTF      Y    0000   K 32
$  6    STR       X    0000
$  7    SGCNT     CT   000    K 0100
$  10   STR       X    0001
$  11   RST       CT   000
$  12   END
```

Figure 7-9 Seven-Segment Display (Stage) Listing

The LD V 01000 instruction moves the current value of counter CT0 into the accumulator, where the SEG instruction converts the Binary Coded Decimal count into a bit pattern that corresponds to the segments of the four seven-segment displays needed to represent the count. If the current count is 28, then the bit pattern in the accumulator after the SEG instruction executes is

00111111 00111111 01011011 011111111

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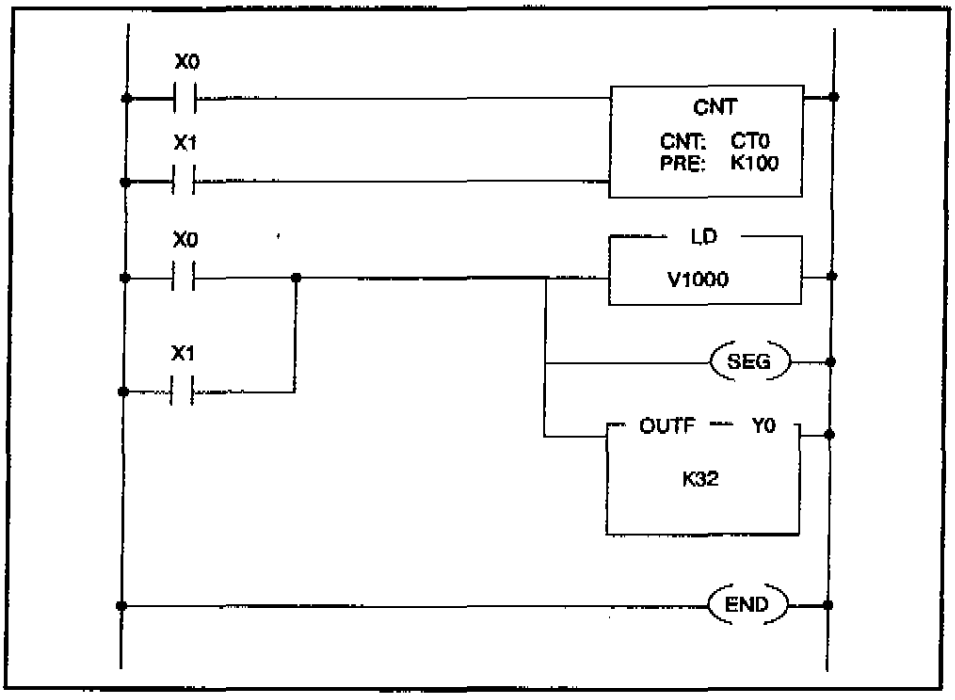


Figure 7-10 Seven-Segment Display (RLL)

$	0	STR	X	0000	
$	1	STR	X	0001	
$	2	CNT	CT	000	K 0100
$	5	STR	X	0000	
$	6	OR	X	0001	
$	7	LD	V	01000	
$	8	SEG			
$	9	OUTF	Y	0000	K 32
$	11	END			

Figure 7-11 Seven-Segment Display (RLL) Listing

The OUTF Y 0000 K32 instruction moves this 32-bit pattern to the image register for Y0 through Y37, with the rightmost bit moving to Y0. Each 1 in the pattern turns on the corresponding image register point, and each 0 turns off its point.

At the end of each program scan, these image register values are output through the first two 16-point output modules in the first base to four seven-segment displays. Figure 7-7 shows how the display appears with a current value of 28 in counter CT0, and that output point is wired to each display segment.

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7.5 High-Speed Count Subroutine (TI435 Only)

In this section, an example shows a segment of a Machine Stage program that is used within a larger control program. This program module can be used to count a batch of parts coming (by a sensor) at high speed, and can check that the correct number of parts was in the batch. By using a subroutine, the count routine can act as a small program scan within the larger program scan, enabling it to operate with a much faster response time than the overall control program. You can follow the example on the Machine Stage diagram in Figure 7-12, and in the program listing in Figure 7-13.

Main instructions used:

- GTS to Go To the Subroutine
- SBR to indicate the start of the subroutine
- RT to return from the subroutine
- FOR/NEXT to define a looping operation within the subroutine
- STRI to immediately read an input without waiting for the program scan to end

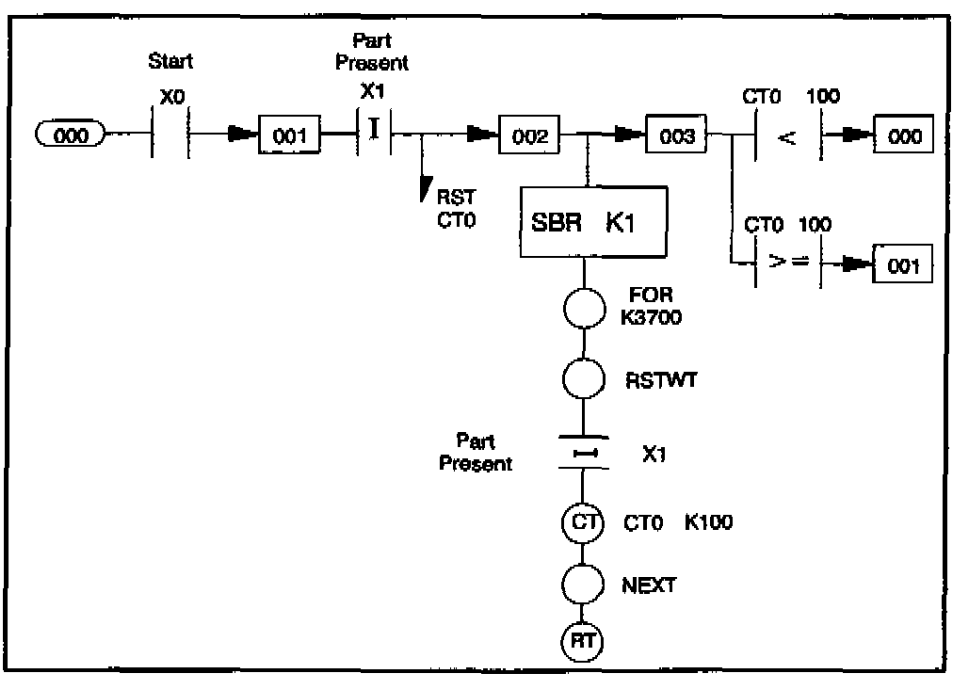


Figure 7-12 High-Speed Count Subroutine

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```
$  0    ISG     S   0000
$  2    STR     X   0000
$  3    JMP     S   0001
$  4    SG      S   0001
$  6    STRI    X   0001
$  7    RST     CT  000
$  8    JMP     S   0002
$  9    SG      S   0002
$  11   GTS     K   0001
$  13   JMP     S   0003
$  14   SG      S   0003
$  16   STRN    CT  000   K0100
$  18   JMP     S   0000
$  19   STR     CT  000   K0100
$  21   JMP     S   0001
$  22   END
$  23   SBR     K   0001
$  25   FOR     K   3700
$  27   RSTWT
$  28   STRI    X   0001
$  29   SGCNT   CT  000   K0100
$  32   NEXT
$  33   RT
```

Figure 7-13 High Speed Count Subroutine Program Listing

Stage 000 Operation

Stage S0 is the initial stage where execution starts. Nothing happens until input X0 is turned on. Once X0 closes, program execution jumps to stage S1 and starts to watch for the first part in the batch to pass the proximity switch connected to X1.

Stage 001 Operation

Stage S1 contains a STRI X1 instruction, that is an immediate I/O instruction. This means that, instead of only reading the state of X1 at the beginning of each program scan and using the value stored in the image register for the entire scan, the state of X1 is read from the input module each time the STRI instruction is executed within the program. This allows a faster response to the input signal. Once a part is sensed, the parts count is reset by the RST CT0 instruction and execution jumps to Stage S2.

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Stage 002 Operation

Stage S2 calls the subroutine with a GTS K1 instruction. The subroutine, following the END instruction in the program listing, consists of a FOR/NEXT loop that executes 3700 times. This makes the subroutine run for one second, since you want to count the number of parts that pass the proximity switch for one second after the first part appears.

An RSTWT instruction is used to reset the watchdog timer every time the FOR/NEXT loop executes. This is necessary since regular scans through the main program are suspended while the FOR/NEXT loop is executing, and a software timeout occurs if the watchdog timer is not reset.

The STRI X1 instruction is used to sense the parts passing the proximity switch and increment counter CT0. The immediate input instruction is required here because without it, the X1 input is not read until the current scan ends, after all the parts to be counted have passed.

Stage 003 Operation

Program execution jumps to Stage S3 after the subroutine completes its task. The two comparison contacts in this stage, control machine operation depending upon how many parts were counted by the subroutine. The STRN CT 000 K0100 instruction jumps program execution back to Stage S0 if fewer than 100 parts were counted. The machine then halts until the operator finds out why the batch was short, and presses the start button again. If 100 or more parts were counted, the STR CT 000 K0100 instruction transfers program execution back to Stage S1, where the program waits until the first of the next batch of parts is sensed.

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The example in this section uses a FAULT instruction to display a machine-performance report message to the operator when pushbutton X0 is pressed, as shown in Figure 7-14. Two versions of the program are shown. One uses Machine Stage programming and the other uses TI405 relay ladder logic with a subroutine. Either version gives the same result with similar scan times.

Main instructions used:

- FAULT message with embedded variables.
- HTA hex to ASCII conversion.
- MOVMC to move V-memory to program memory.
- SBR subroutine to reduce scan time.
- DLBL storage with ACON and NCON.
- BCD Math and Accumulator instructions.

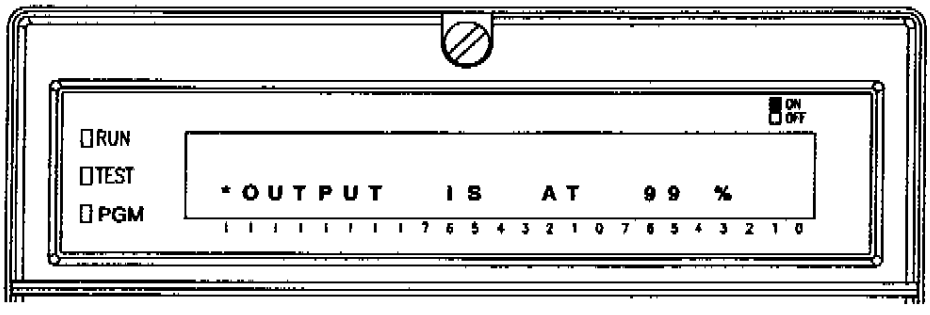


Figure 7-14 Message Displayed on the MIU

In both programs, the PLC scans and waits until X0 is closed. Once this happens, the Machine Stage program transitions to Stage 1, and displays the message. The relay ladder logic program branches to its subroutine and performs the same operations. Both programs continue to execute the math instructions, and show an increased scan time, until X0 is released. The following discussion of the program applies to either version, and may be followed in the Stage diagram in Figure 7-15, or in the ladder diagram in Figure 7-17.

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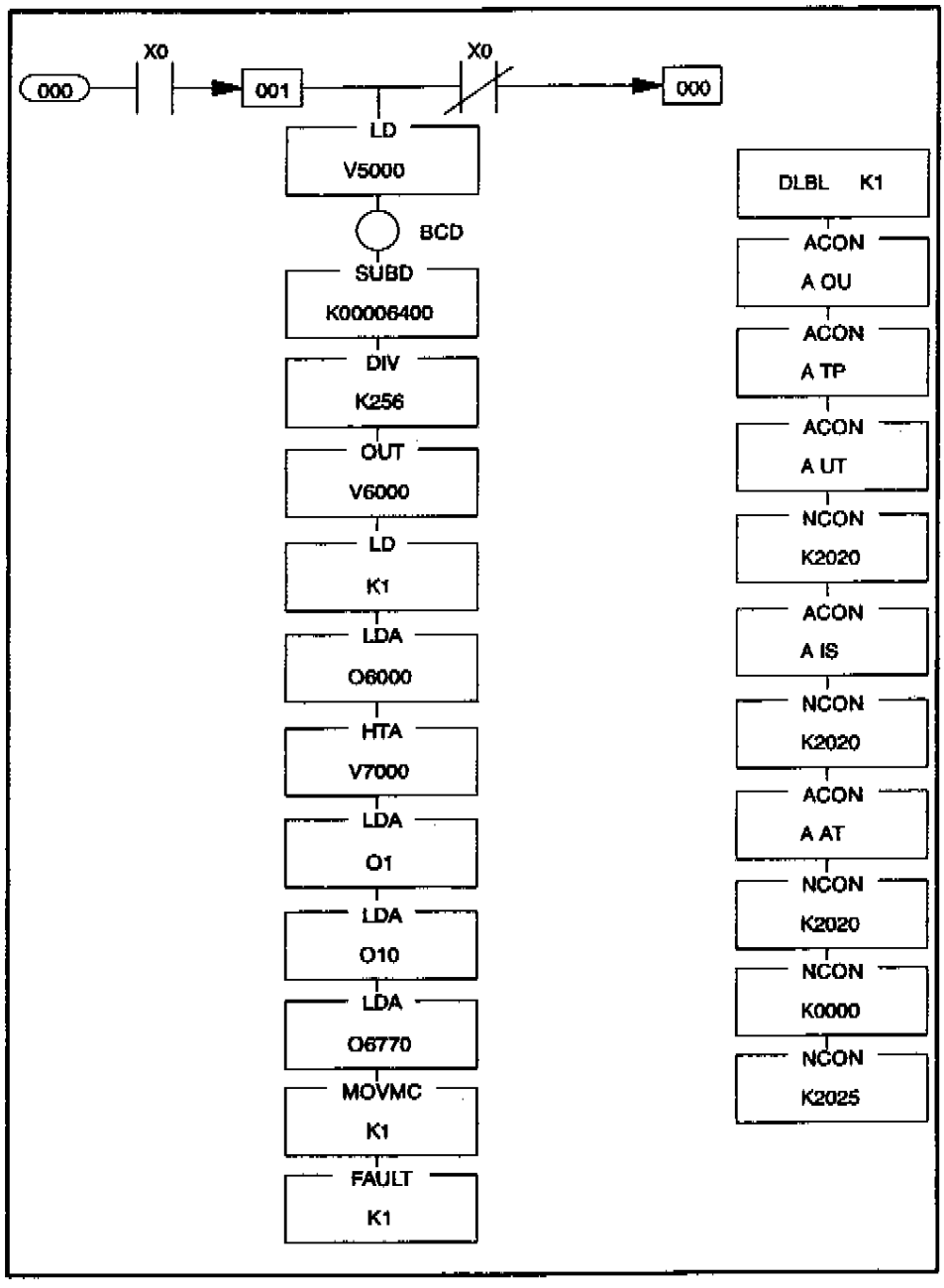


Figure 7-15 MIU Operator Interface (Stage)

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The performance of the machine is gauged by a number in memory location V5000 that can range from 6400 to 32000; 6400 is considered to be 0 percent output and 32000 is 100 percent output. Before you can do any calculations, the performance number must first be loaded into the accumulator. The LD V 05000 instruction moves the binary value that can range from 0 to 7CFF, into the accumulator. 7CFF is the hexadecimal number that is stored in V-Memory to represent a value of 31999, or 99% of full output. The BCD instruction is then used to convert the binary number into a Binary Coded Decimal number for use with the math instructions.

Use the SUBD K 00006400 instruction to subtract 6400 from the accumulator in order to remove the offset from zero, since 6400 is equal to zero percent output. Divide the number in the accumulator by 256 with a DIV K 0256 to scale the performance value to a percentage between 0 and 99. The OUT V 06000 instruction moves this result from the accumulator to memory location V6000.

A percentage is now stored in V6000, but the number is in BCD format. It must be converted into ASCII characters before it can be displayed on the MIU. Use the instruction sequence LD K 0001, LDA O 06000 and HTA V 07000 to convert it. This sequence specifies that one word of hex data located at V6000 is converted to ASCII characters and stored starting at V7000.

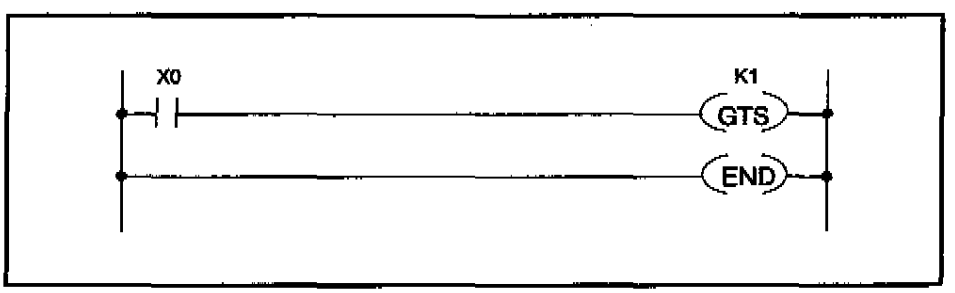


Figure 7-16 MIU Operator Interface (RLL) Main Program Segment

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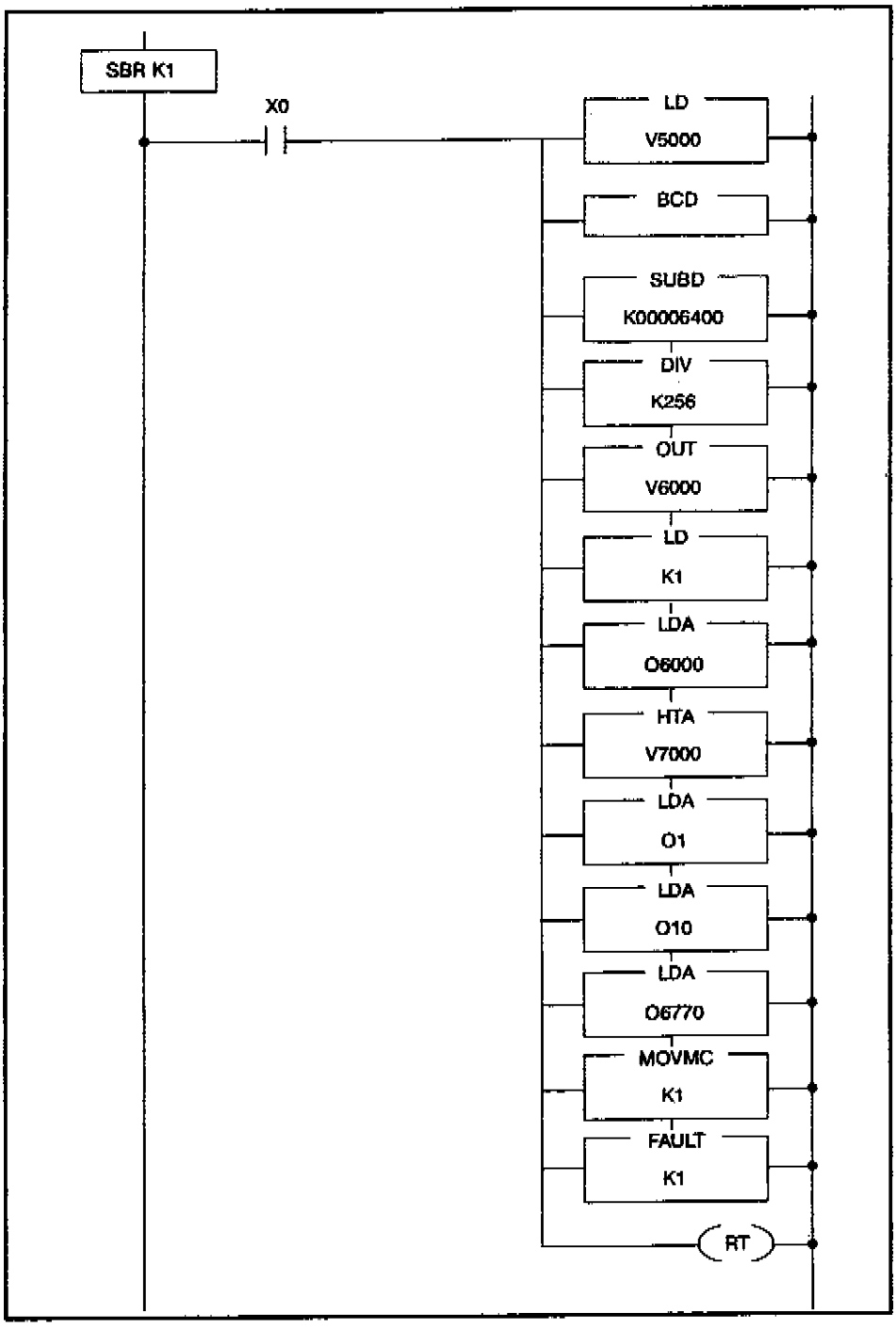


Figure 7-17 MIU Operator Interface (RLL)—Subroutine Segment

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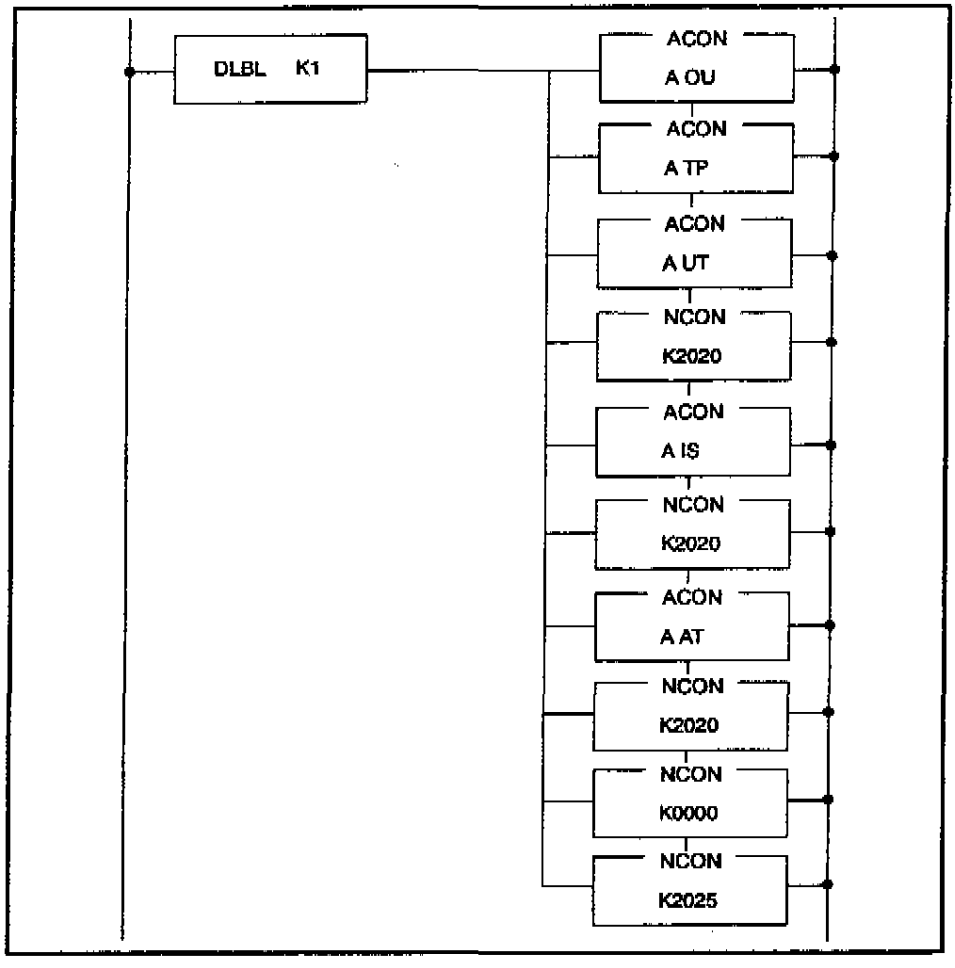


Figure 7-17 MIU Operator Interface (RLL) (continued)

Now that the percentage is converted to ASCII, move it from V-memory into a DLBL storage area in program memory where it can be displayed by the FAULT instruction using the MOVMC. The three LDA instructions that precede it set up the move. The LDA O 00001 means that one word of data is moved. The LDA O 00010 specifies that the move is made at an offset of eight (octal 10) into a table of values. In this case, the move is being made into DLBL K1. If you look at the boxes under the DLBL in either of the figures, and start counting from zero with the first ACON A OU, you see that number eight is an NCON K 0000. This numeric constant instruction has been programmed with zeros since it is overwritten by the performance percentage from V-memory.

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The LDA O 06770 loads the starting address of the source data table. The number that we want to move is at location V7000, but since the offset is fixed by the location that we want to move into following the DLBL, we have to back up eight locations (10 octal) to make the MOVMC move the value that we want. None of the values that precede V7000 is affected by this; we are using this method to save memory by not storing the entire message in V-memory and moving it all to get the one location that we want. The MOVMC K 0001 instruction actually makes the transfer to DLBL K1.

```
$   0    ISG      S   0000
$   2    STR      X   0000
$   3    JMP      S   0001
$   4    SG       S   0001
$   6    LD       V   05000
4   7    BCD
$   8    SUBD     K   00006400
$   10   DIV      K   0256
$   11   OUT      V   06000
$   12   LD       K   0001
$   13   LDA      O   06000
$   14   HTA      V   07000
$   16   LDA      O   00001
$   17   LDA      O   00010
$   18   LDA      O   06770
$   19   MOVMC    K   0001
$   21   FAULT    K   0001
$   23   STRN     X   0000
$   24   JMP      S   0000
$   25   END
$   26   DLBL     K   0001
$   28   ACON     A   OU
$   29   ACON     A   TP
$   30   ACON     A   UT
$   31   NCON     K   2020
$   32   ACON     A   IS
$   33   NCON     K   2020
$   34   ACON     A   AT
$   35   NCON     K   2020
$   36   NCON     K   0000
$   37   NCON     K   2025
```

Figure 7-18 MIU Operator Interface (Stage) Listing

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The FAULT K 0001 instruction then displays the characters from DLBL K 1 on the MIU. The ACON instructions each hold two ASCII characters, so the first three combine to spell OUTPUT. The NCON instructions hold ASCII codes for characters that are not on the MIU keyboard. NCON K 2020 causes two spaces (ASCII 20) to be displayed, and NCON K 2025 displays a space and a percent sign (ASCII 25). The complete display, as shown in Figure 7-14 is seen if a value of 7CFF is placed in memory location V5000, and X0 is closed.

```
$  0    STR     X  0000
$  1    GTS     K  0001
$  3    END
$  4    SBR     K  0001
$  6    STR     X  0000
$  7    LD      V  05000
$  8    BCD
$  9    SUBD    K  00006400
$  11   DIV     K  0256
$  12   OUT     V  06000
$  13   LD      K  0001
$  14   LDA     O  06000
$  15   HTA     V  07000
$  17   LDA     O  00001
$  18   LDA     O  00010
$  19   LDA     O  06770
$  20   MOVMC   K  0001
$  22   FAULT   K  0001
$  24   RT
$  25   DLBL    K  0001
$  27   ACON    A  OU
$  28   ACON    A  TP
$  29   ACON    A  UT
$  30   NCON    K  2020
$  31   ACON    A  IS
$  32   NCON    K  2020
$  33   ACON    A  AT
$  34   NCON    K  2020
$  35   NCON    K  0000
$  36   NCON    K  2025
```

Figure 7-19 MIU Operator Interface (RLL) Listing

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Chapter 8
Instruction Operands

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An X corresponds to a point in the discrete image register. When the image register point is on (high, closed, or = 1) the X is on. When the image register point is off (low, open, or = 0) the X is off. Xs are indicated in the RLL program by the normally open contact —| |— or by the normally closed contact —|/|—. See Figure 8-1.



Figure 8-1 The X Format

The n is the reference number and refers to the image register point that corresponds to the contact. The range of n is octal 0–477. To enter an X using the MIU, you press [X(n)] followed by the octal reference number.

X Operation: The X contact on the RLL rung represents a field device, for example, a limit switch.

- When the field device turns on, the image register point assigned to that device is set to 1 before starting the next scan, and the X normally open contact is closed. This completes the circuit to the next instruction on the RLL rung.
- When the field device turns off, the image register point is cleared to 0 before starting the next scan, and the normally open contact is opened. This opens the circuit to the next instruction, but it is not executed.
- The normally closed X contact in an RLL program's state is opposite that of the image register point. That is, if the image register point is 0, for example, the normally closed X contact is on.

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A Y corresponds to a point in the discrete image register. When the Y is on (high, closed, or = 1), the image register point is set (= 1). When the Y is off (low, open, or = 0), the image register point is cleared (= 0). Ys are indicated in the RLL program by the normally open coil —( )— or contact —| |—. See Figure 8-2.



Figure 8-2 The Y Format

The n is the reference number and refers to the image register point that corresponds to the contact or coil. The range of n is octal 0–477. To enter a Y using the MIU, you press [Y/OUT] followed by the octal reference number.

Y Operation: The Y coil on the RLL rung represents a field device, for example, a pilot light.

- When the Y coil turns on, the image register point referenced by that Y is set to 1, and the field device is turned on at the end of the scan.
- When the Y coil turns off, the image register point referenced by that Y is cleared to 0 during the next scan, and the field device is turned off at the end of the scan.
- A contact can be designated as a Y. The status of a Y contact is determined by the status of the Y output coil having the same reference number as the Y contact.

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Control relays are internal memory locations and do not represent actual hard-wired field devices. A C represents a point in the control relay image register. When the image register point is on (high, closed, or = 1) the C is on. When the image register point is off (low, open, or = 0) the C is off. Cs are indicated in the RLL program by the normally open coil —( )— or contact —| |— or by the normally closed contact —|/|—. See Figure 8-3.

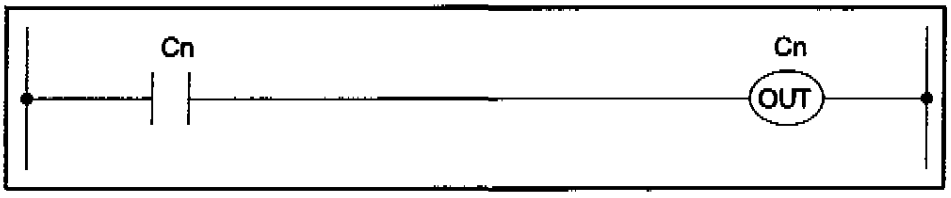


Figure 8-3 The C Format

The n is the reference number and refers to the image register point that corresponds to the control relay. The range of n is octal 0–737 giving you access to 480 control relays. To enter a C using the MIU, you press [GCN] followed by the octal reference number.

C Operation: The control relay is used to provide control for other RLL instructions. When used as a contact, the control relay functions as follows.

- When the image register point corresponding to a C is set to 1, the C normally open contact is closed. This completes the circuit to the next instruction on the RLL rung.
- When the image register point corresponding to a C is cleared to 0, the C normally open contact is opened. This opens the circuit to the next instruction, but it is not executed.

When used as a coil the control relay functions as follows.

- When the C coil is turned on, the image register point corresponding to the C is set to 1.
- When the C coil is turned off, the image register point corresponding to the C is cleared to 0.

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Normally, all input relays are read and the image register is updated at the beginning of the CPU scan cycle, as shown in Figure 8-4. Immediate inputs are a special form of the X input relay. Their state is read during the RLL Program Execution phase of the scan cycle rather than waiting until the end of the scan. Reading an immediate input does not update the image register.

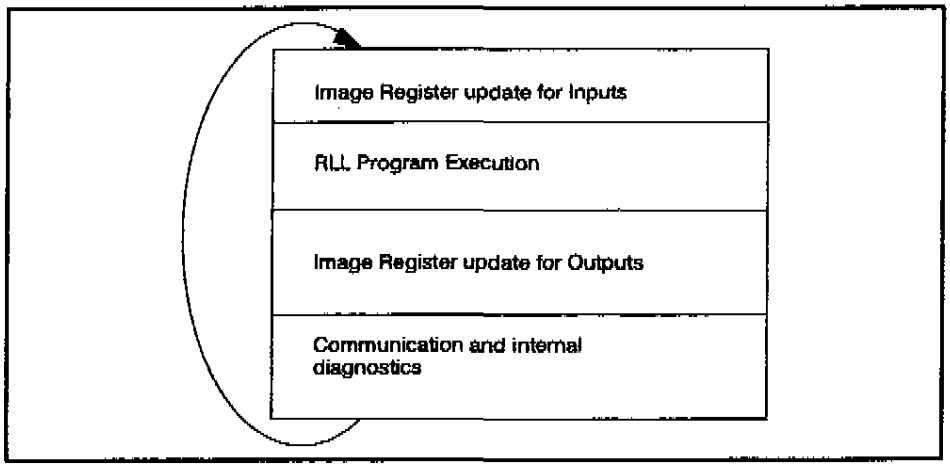


Figure 8-4 CPU Scan Cycle

An immediate input is represented by the normally open contact —|I|— symbol and the normally closed contact —|I/|—symbol. Figure 8-5 shows an example of normally open and normally closed immediate input contacts. After pressing the operation key, you may enter a normally open immediate input with the MIU. To do so, press [SHIFT] [I] [SHIFT] [X(IN)] followed by the octal input reference number.

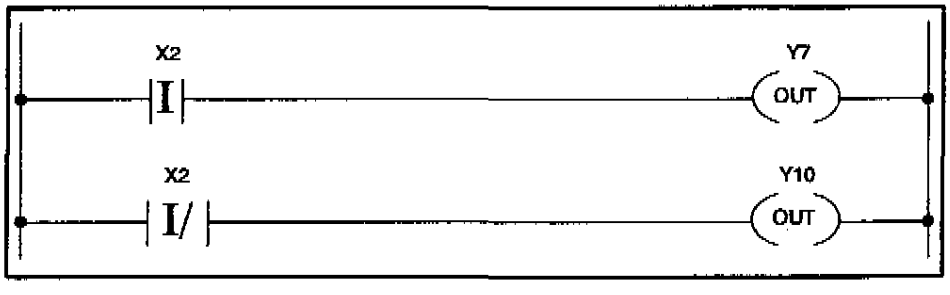


Figure 8-5 Immediate Input Examples

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8.5 Immediate Outputs

Immediate outputs are a special form of Y output coils. You can shorten the time it takes to update an output by using an immediate instruction, because immediate outputs do not update the image register. The immediate instructions cause the single output point to be read and updated during the RLL Program Execution phase of the scan cycle. An immediate output is represented by the —(OUT)— symbol, as shown in Figure 8-6. To enter a normally open immediate output with the MIU, after pressing the operation key, press SHIFT [ ] SHIFT WOUT followed by the octal input reference number.

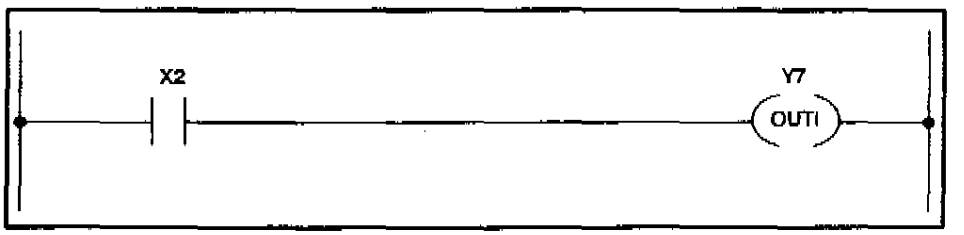


Figure 8-6 Immediate Output Example

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8.6 Special Relays

Special relays are internal discrete points that are set and reset by the CPU depending on certain operating conditions. You can use these relays in your RLL program to time functions, alert you to diagnostic conditions, etc. SPs are indicated in the RLL program by the normally open contact —| |— or by the normally closed contact —|/|—. See Figure 8-7.

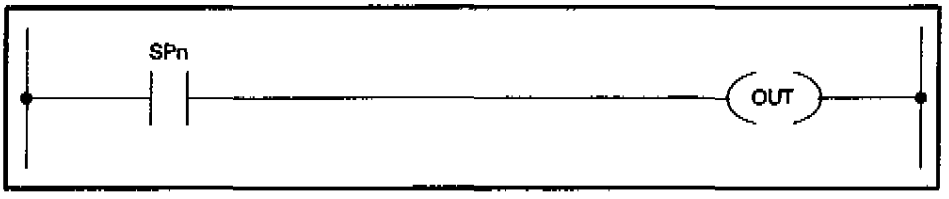


Figure 8-7 Special Relay Example

The n is the reference number and refers to the image register point that corresponds to the relay. The range of n is octal 0–137 and 320–617. To enter an SP using the MIU, you press SPCL followed by the octal reference number.

SP000 This Special relay is on if this is the first scan after the CPU is reset. It is reset on the second scan.

SP001 Normally On. You can use this special relay when you need a condition to always be true.

Clock Relays

The special clock relays cycle on and off once for the specified time period.

SP003 1-minute clock—Duration is 30 seconds on, 30 seconds off.

SP004 1-second clock—Duration is 0.5 seconds on, 0.5 seconds off.

SP005 100 millisecond clock—Duration is 50 milliseconds on, 50 off.

SP006 50 millisecond clock—Duration is 26 milliseconds on, 24 off.

SP007 Scan clock—SP007 is energized on alternate scans.

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CPU Status Relays

These Special relays provide an indication of the CPU status.

SP011	Forced running state—SP011 is on when the CPU is switched to the RUN mode using the keyswitch. Otherwise, it is off.
SP012	TERM RUN state—SP012 is on when the CPU is set to the RUN mode when the keyswitch is set to TERM. Otherwise, it is off.
SP013	TEST RUN state—SP013 is on when the CPU is set to TEST RUN mode. Otherwise, it is off.
SP015	TEST PGM state—SP015 is on when the CPU is set to TEST PGM mode. Otherwise, it is off.
SP016	TERM PGM state—SP016 is on when the CPU is set to the PGM mode when the keyswitch is set to TERM. Otherwise, it is off.
SP017	Forced STOP state—SP017 is on when the CPU is switched to the STOP mode using the keyswitch. Otherwise, it is off.
SP020	PGM relay—SP020 is on when the CPU is in the PGM mode. Otherwise, it is off.
SP022	Interrupt enable relay—SP022 is on when the hardware interrupts are enabled with the ENI instruction. It is off when the hardware interrupts are disabled with the DISI instruction.
SP025	CPU battery disabled—SP025 is on if CPU dipswitch 1 is on, disabling the CPU battery. The relay is off if dipswitch 1 is off.
SP026	Disable I/O update (TI435 only)—SP026 is on when I/O updating is disabled. Otherwise, it is off.
SP027	Disable I/O update (TI435 only)—Disable I/O update to modules with missing terminal strips. SP027 is on when updating is disabled. Otherwise, it is off.
SP030	Dipswitch 1 status—SP030 is on if CPU dipswitch 1 is on.
SP031	Dipswitch 2 status—SP031 is on if CPU dipswitch 2 is on.
SP032	Dipswitch 3 status—SP032 is on if CPU dipswitch 3 is on.
SP033	Dipswitch 4 status—SP033 is on if CPU dipswitch 4 is on.

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System Check Relays

These Special relays provide an indication of the system status.

SP040 Critical error relay—SP040 is on when a critical error such as a missing I/O module terminal strip is detected. Otherwise, it is off.

SP041 Non-critical error relay—SP041 is on when a non-critical error such as a low CPU battery is detected. Otherwise, it is off.

SP043 Battery low relay—SP043 is on when the CPU or Memory Cartridge backup battery falls below 3 volts or is missing. You can use this relay to display a message to the operator to replace the battery. The specific error code is stored at V7757. Otherwise, it is off.

SP044 Memory error relay—SP044 is on when an error is detected in memory that could be an invalid instruction, a missing or failed Memory Cartridge, or a memory parity error. The specific error code is stored at V7755. Otherwise, it is off.

SP045 I/O error relay—SP045 is on when an I/O error is detected. This could be a missing terminal block, a missing I/O module, a blown fuse, a different I/O configuration, or several other conditions. The specific error code is stored in either V7755 or V7756. Otherwise, it is off.

SP046 Communications error relay—SP046 is on when a communications error is detected. The specific error code is stored at V7756. Otherwise, it is off.

SP047 I/O configuration error relay—SP047 is on when an I/O configuration error is detected. Otherwise, it is off.

SP050 External diagnostic instruction (EDI) relay—SP050 is on when the FAULT instruction is executed. Otherwise, it is off.

SP051 Arithmetic time out relay—SP051 is on when the arithmetic operation has timed out. Otherwise, it is off.

SP052 Syntax error relay—SP052 is on when the CPU encounters an instruction that is syntactically incorrect. Otherwise, it is off. The syntax error is detected either while the CPU is in RUN mode or as a result of requesting a program check with AUX 21. The specific error code is stored at V7755.

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SP056	Table overrun relay—SP056 is on if the operand in a table instruction specifies an address outside the range of the table. Otherwise, it is off.

Accumulator Relays

These Special relays indicate the results of arithmetic and logical operations that are performed with the accumulator.

SP053	Arithmetic error flag—SP053 is on when the value of the operand is greater than the operation can work with.
SP060	Less than flag—SP060 is on when the value in the accumulator is less than the operand value.
SP061	Equal to flag—SP061 is on when the value in the accumulator is equal to the operand value.
SP062	Greater than flag—SP062 is on when the value in the accumulator is greater than the operand value.
SP063	Zero flag—SP063 is on when the operation causes the value in the accumulator to be zero.
SP064	Half-borrow flag—SP064 is on when the 16-bit arithmetic subtraction operation results in a borrow because the operand was larger than the accumulator value.
SP065	Borrow flag—SP065 is on when the 32-bit arithmetic subtraction operation results in a borrow because the operand was larger than the accumulator value.
SP066	Half-carry flag—SP066 is on when the 16-bit arithmetic addition operation results in a carry because the sum of the operand and the accumulator is larger than 65,535.
SP067	Carry flag—SP067 is on when the 32-bit arithmetic addition operation results in a carry because the sum of the operand and the accumulator is larger than 4,294,967,293.
SP070	Sign flag—SP070 is on when the results of the arithmetic or logical operation cause the accumulator's value to be negative. SP070 is off when the results cause the accumulator's value to be positive.
SP073	Overflow—SP073 is on when a signed addition or subtraction produces a result with an incorrect sign bit.

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SP075	Data error—SP075 is on when a BCD instruction is performed and the accumulator does not contain valid BCD digits. Otherwise, it is off.
SP076	Read flag—SP076 is on when the value loaded into the accumulator, by any of the load instructions, is zero. Otherwise, it is off.

Data Communications Relays

These special relays indicate the status of data communication modules in any of the CPU base slots.

SP120	Base number 0/Slot number 0. SP120 is on when the DCM, Base 0/Slot 0, is transmitting. Otherwise, it is off.
SP121	Base number 0/Slot number 0. SP121 is on when a transmission error is detected by the DCM in Base 0/Slot 0. Otherwise, it is off.
SP122	Base number 0/Slot number 1. SP122 is on when the DCM, in Base 0/Slot 1, is transmitting. Otherwise, it is off.
SP123	Base number 0/Slot number 1. SP123 is on when a transmission error is detected by the DCM in Base 0/Slot 1. Otherwise, it is off.
SP124	Base number 0/Slot number 2. SP124 is on when the DCM, in Base 0/Slot 2, is transmitting. Otherwise, it is off.
SP125	Base number 0/Slot number 2. SP125 is on when a transmission error is detected by the DCM in Base 0/Slot 2. Otherwise, it is off.
SP126	Base number 0/Slot number 3. SP126 is on when the DCM, in Base 0/Slot 3, is transmitting. Otherwise, it is off.
SP127	Base number 0/Slot number 3. SP127 is on when a transmission error is detected by the DCM in Base 0/Slot 3. Otherwise, it is off.
SP130	Base number 0/Slot number 4. SP130 is on when the DCM, in Base 0/Slot 4, is transmitting. Otherwise, it is off.
SP131	Base number 0/Slot number 4. SP131 is on when a transmission error is detected by the DCM in Base 0/Slot 4. Otherwise, it is off.

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SP132	Base number 0/Slot number 5. SP132 is on when the DCM, in Base 0/Slot 5, is transmitting. Otherwise, it is off.
SP133	Base number 0/Slot number 5. SP133 is on when a transmission error is detected by the DCM in Base 0/Slot 5. Otherwise, it is off.
SP134	Base number 0/Slot number 6. SP134 is on when the DCM, in Base 0/Slot 6, is transmitting. Otherwise, it is off.
SP135	Base number 0/Slot number 6. SP135 is on when a transmission error is detected by the DCM in Base 0/Slot 6. Otherwise, it is off.
SP136	Base number 0/Slot number 7. SP136 is on when the DCM, in Base 0/Slot 7, is transmitting. Otherwise, it is off.
SP137	Base number 0/Slot number 7. SP137 is on when a transmission error is detected by the DCM in Base 0/Slot 7. Otherwise, it is off.
SP320-SP617	SP320 through SP617 are currently disabled. Their functions are reserved for future enhancements.

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8.7 Timer Relays

Timer relays are internal discrete points that are set when the associated timer has timed-out. Timer relays are indicated in the RLL program by the normally open contact —| |— or by the normally closed contact —|/|—. See Figure 8-8.

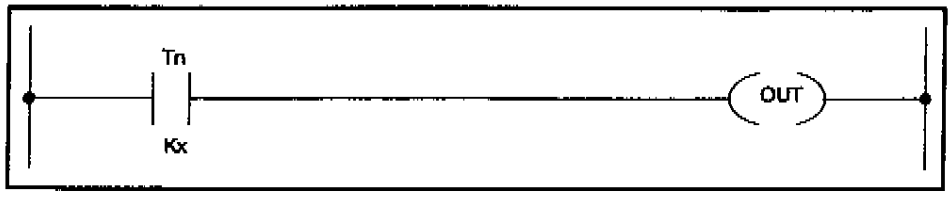


Figure 8-8 Timer Relay Example

In the figure, the n is the reference number for the image register point corresponding to the relay. The range of n is octal 0–177. To enter a timer relay using the MIU, press [TMR] and the octal reference number. You may also specify a different preset with the timer relay. A timer relay with a preset turns on when the timer current value equals that preset, and remains on until the timer is reset. The x is the constant value for the preset.

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8.8 Counter Relays

Counter relays are internal discrete points that are set when the associated counter has counted to its preset value. Counter relays are indicated in the RLL program by the normally open contact —| |— or by the normally closed contact —|/|—. See Figure 8-9.

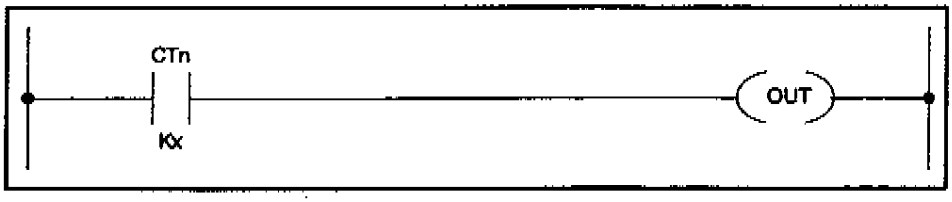


Figure 8-9 Counter Relay Example

The n is the reference number and refers to the image register point that corresponds to the relay. The range of n is octal 0–177. To enter a counter relay using the MIU, you press [CNT] and the octal reference number. You may also specify a different preset with the counter relay. A counter relay with a preset turns on when the counter current value equals that preset, and remains on until the counter is reset. The x is the constant for the preset.

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Some of the TI405 instructions accept a V-Memory pointer as an operand. Rather than using the contents of the V-Memory in the operation, the CPU uses the contents of the V-Memory address contained in the V-Memory pointer.

For example, the OUT instruction accepts a V-Memory pointer as its operand, as shown in Figure 8-10. In this example, V-Memory location, V2142, is used as a pointer. Its contents, 3247, represent the actual location of where the low order 16 bits of the accumulator are stored: V3247.

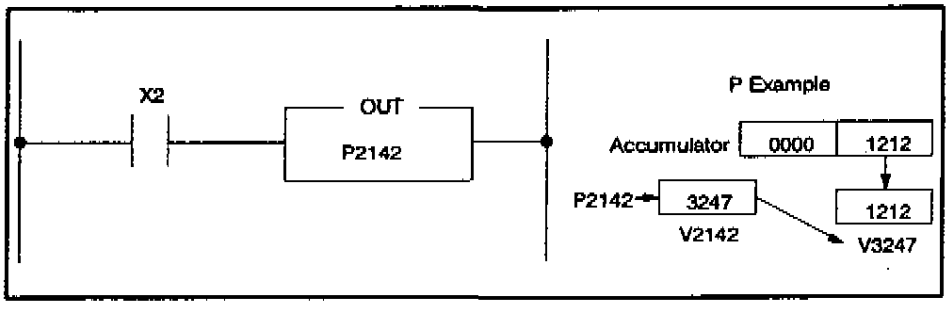


Figure 8-10 V-Memory Pointer Example

To enter a pointer reference using the MIU, press PNTR followed by the V-memory pointer address.

Key Sequence

STR X(IN) 2 ENT

OUT PNTR 2 1 4 2 ENT

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8.10 Indirect Addressing

Overview

Indirect Addressing uses the P operand as a V-memory pointer. Instructions LD, LDD, OUT, and OUTD supported indirect addressing (P operand) on previous firmware releases for the TI425 and TI435. These four instructions continue to support indirect addressing with TI425 CPU V2.1 and TI435 CPU V2.1. Additionally, indirect addressing is expanded on the TI435 to include the following instructions:

LD	LoaD accumulator with word
LDD	LoaD accumulator with Double word
OUT	OUTput accumulator right-most word
OUTD	OUTput accumulator Double word
STR	SToRe greater than or equal
STRN	SToRe less thaN
AND	AND greater than or equal
ANDN	AND less thaN
OR	OR greater than or equal
ORN	OR less thaN
STRE	SToRe Equal
STRNE	SToRe Not Equal
ANDE	AND Equal
ANDNE	AND Not Equal
ORE	OR Equal
ORNE	OR Not Equal
TMR	TiMeR
TMRF	TiMeR Fast
TMRA	TiMeR Accumulating
TMRAF	TiMeR Accumulating Fast
CNT	CouNTer
SGCNT	StaGe CouNTer
UDC	Up/Down Counter
LDX	LoaD accumulator indeXed
OUTX	OUTput accumulator indeXed
ADD	ADD
ADDD	ADD Double
SUB	SUBtract
SUBD	SUBtract Double
MUL	MULtiply
DIV	DIVide
ADDB	ADD Binary
ADDBD	ADD Binary Double
SUBB	SUBtract Binary
SUBBD	SUBtract Binary Double
MULB	MULtiply Binary
DIVB	DIVide Binary
AND	AND accumulator with word
ANDD	AND accumulator with Double word
OR	OR accumulator with word
ORD	OR accumulator with Double word
XOR	eXclusive OR accumulator with word
XORD	eXclusive OR accumulator with Double word

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CMP	CoMPare accumulator with Single word
CMPD	CoMPare accumulator with Double word
INC	INCrement
DEC	DECrement
INCB	INCrement Binary
DECB	DECrement Binary
MOV	MOVe table
FILL	FILL V-memory table
RX	Read data from network
WX	Write data to network

Error Flag

An error flag, SP71, is available with TI425 CPU V2.1 and TI435 CPU V2.1 to indicate improper indirect addressing. This flag is affected by each instruction that uses a P operand. If the P operand points to a valid V location, SP71 is turned off. However, if the V-memory location pointed to by the P operand is not valid, SP71 is turned on.

For example, if a LD P1000 is used in a RLL program, changes in the value stored in V1000 create changes in SP71. See Table 8-1.

Table 8-1 Values of Contents of V1000

Contents of V1000 (hexadecimal)	Octal Equivalent	Specified Register	Result	SP71
0000	0	V 0	OK	OFF
029C	1234	V1234	not valid	ON
4180	40600	V40600	OK	OFF
5000	50000	V50000	not valid	ON

You can use SP71, following each indirect addressing instruction, to take an action if improper indirect addressing occurs. Figure 8-11 shows SP71 used to stop execution of the user program if an error is detected.

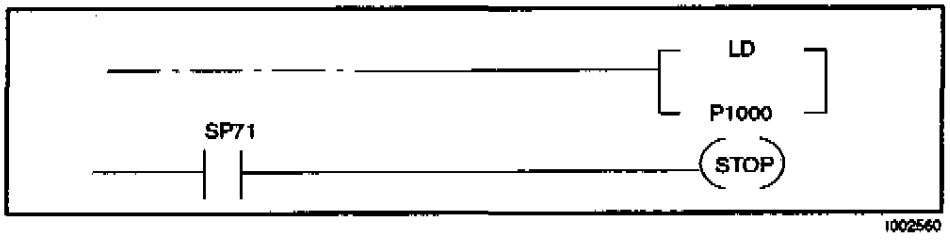


Figure 8-11 Stopping Program Execution if Error Detected

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Chapter 9

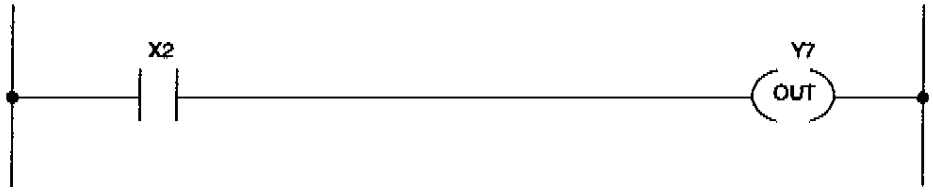
High-Speed Boolean Instructions

STR 9-2
STRN 9-2
AND 9-3
OR 9-3
ANDN 9-4
ORN 9-4
AND STR 9-5
OR STR 9-6
OUT 9-7
OR OUT 9-8

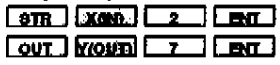
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STR

Store (STR) begins a new line of logic. The on/off state of the STR contact is the same as the state of its associated image register point.



Key Sequence



Valid Data Types: X, Y, C, S, T, CT, SP, and GX

STRN

Store NOT (STRN) begins a new line of logic. The on/off state of the STRN contact is opposite the state of its associated image register point.



Key Sequence

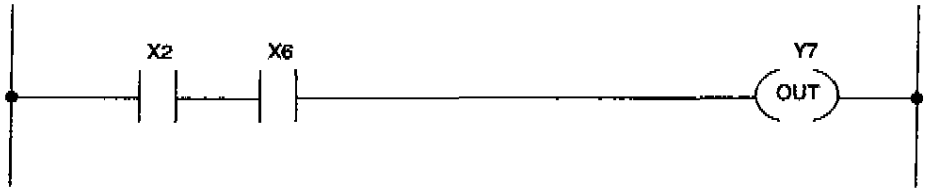


Valid Data Types: X, Y, C, S, T, CT, SP, and GX

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AND

AND (AND) connects two logic elements in series. The on/off state of the contact following the AND is the same as the state of its associated image register point.



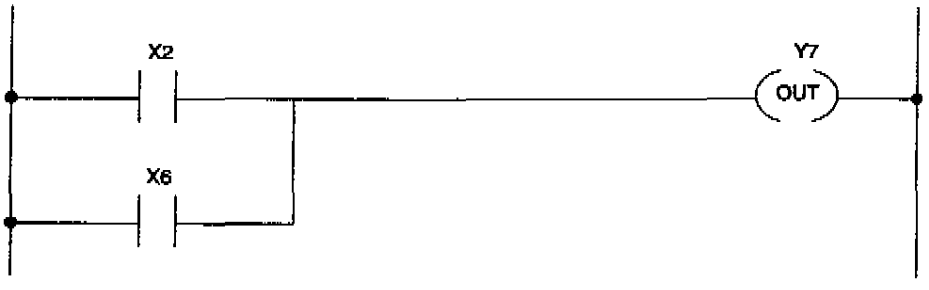
Key Sequence

STR	X(IN)	2	ENT
AND	X(IN)	6	ENT
OUT	Y(OUT)	7	ENT

Valid Data Types: X, Y, C, S, T, CT, SP, and GX

OR

OR (OR) connects two logic elements in parallel. The on/off state of the contact following the OR is the same as the state of its associated image register point.



Key Sequence

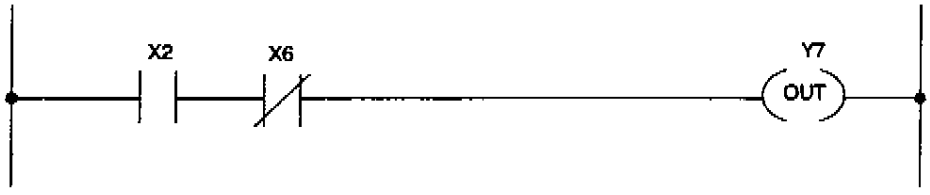
STR	X(IN)	2	ENT
OR	X(IN)	6	ENT
OUT	Y(OUT)	7	ENT

Valid Data Types: X, Y, C, S, T, CT, SP, GX

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ANDN

AND NOT (ANDN) connects two logic elements in series. The on/off state of the contact following the ANDN is opposite the state of its associated image register point.



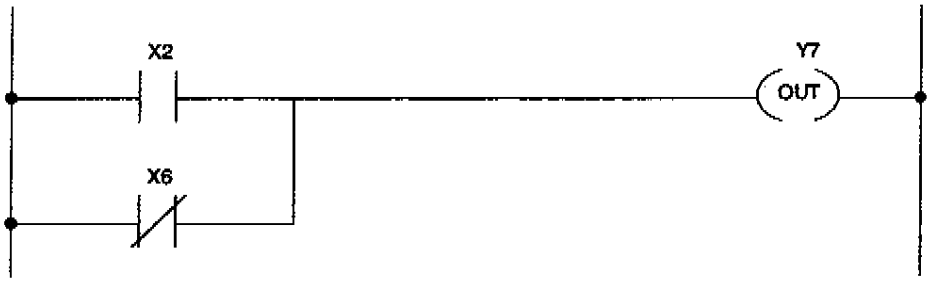
Key Sequence

STR	X/IN0	2	ENT	
AND	NOT	X/IN0	6	ENT
OUT	Y/OUT0	7	ENT	

Valid Data Types: X, Y, C, S, T, CT, SP, and GX

ORN

OR NOT (ORN) connects two logic elements in parallel. The on/off state of the contact following the ORN is opposite the state of its associated image register point.



Key Sequence

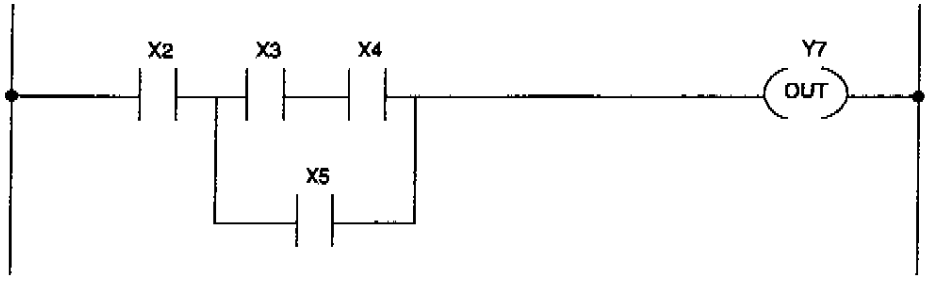
STR	X/IN0	2	ENT	
OR	NOT	X/IN0	6	ENT
OUT	Y/OUT0	7	ENT	

Valid Data Types: X, Y, C, S, T, CT, SP, and GX

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AND STR

AND Store (AND STR) connects two groups of logic elements in series. Each group must begin with an STR instruction.



Key Sequence

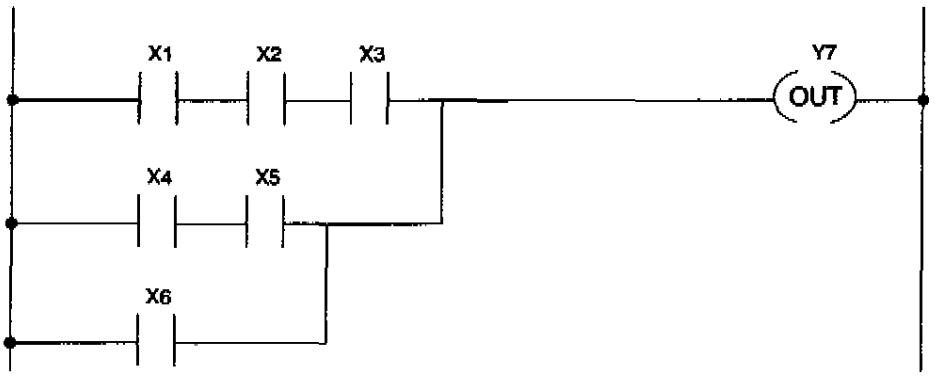
STR	X/B0	2	ENT
STR	X/B0	3	ENT
AND	X/B0	4	ENT
OR	X/B0	5	ENT
AND	STR	ENT	
OUT	Y/O1/T	7	ENT

Valid Data Types: None

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OR STR

OR Store (OR STR) connects two groups of logic elements in parallel. Each group must begin with a STR instruction.



Key Sequence

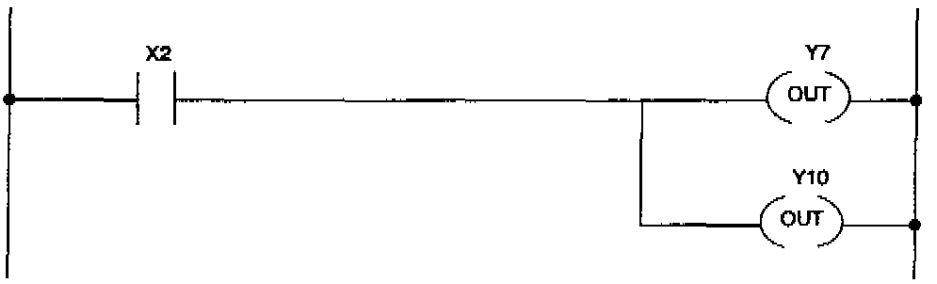
STR	X/IN	1	ENT
AND	X/IN	2	ENT
AND	X/IN	3	ENT
STR	X/IN	4	ENT
AND	X/IN	5	ENT
OR	X/IN	6	ENT
OR	STR	ENT	
OUT	Y/OUT	7	ENT

Valid Data Types: None

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OUT

Out (OUT) ends a line of logic. The on/off state of the corresponding image register point is updated when the instruction is executed. If the same point is used as an output more than once in a program, the state of the last occurrence of that output is the state that is written to the physical output point at the end of the scan.



Key Sequence

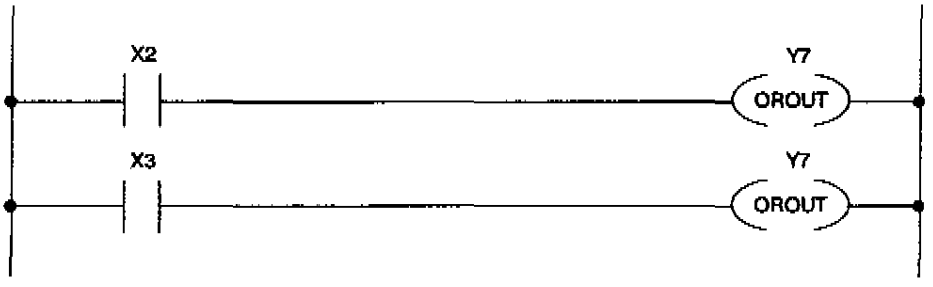
STR | X/IN0 | 2 | ENT
OUT | Y/OUT0 | 7 | ENT
OUT | Y/OUT0 | 1 | 0 | ENT

Valid Data Types: X, Y, C, GX

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OR OUT

OR OUT (OR OUT) ends a line of logic. The on/off state of the corresponding image register point is updated when this instruction is executed. If the same point is used as an output more than once in a program, the outputs are considered to be ORed together, so that an inactive occurrence of an output later in the program scan will not override an active occurrence.



Key Sequence

STR	X(IN)	2	ENT	
OR	OUT	Y(OUT)	7	ENT
STR	X(IN)	3	ENT	
OR	OUT	Y(OUT)	7	ENT

Valid Data Types: X, Y, C, and GX

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Chapter 10

Comparative Boolean Instructions

STRE 10-2
ORE 10-2
ANDE 10-3
STRNE 10-3
ORNE 10-4
ANDNE 10-4
STR 10-5
OR 10-5
AND 10-6
STRN 10-6
ORN 10-7
ANDN 10-7

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STRE

Store Equal (STRE) begins a new line of logic. The contact turns on when the first V-memory value is equal to the second value.



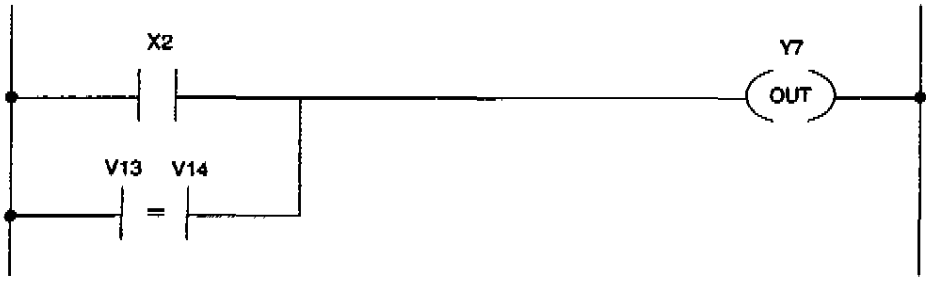
Key Sequence

STR SHIFT E
SHIFT V 1 0 K(CONT) 5 0 ENT
OUT Y(OUT) 7 ENT

Valid Data Types: First value V
Second value V and K

ORE

OR Equal (ORE) connects this contact in parallel with another. The contact turns on when the first V-memory value is equal to the second value.



Key Sequence

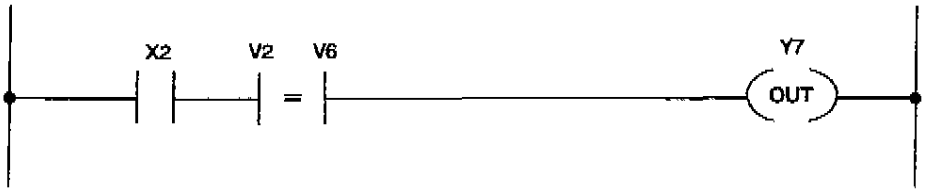
STR X(INPUT) 2 ENT
OR SHIFT E
SHIFT V 1 3 V 1 4 ENT
OUT Y(OUT) 7 ENT

Valid Data Types: First value V
Second value V and K

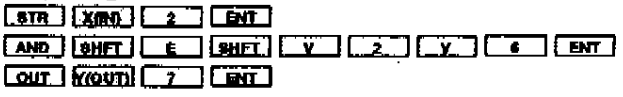
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ANDE

AND Equal (ANDE) connects this contact in series with another. The contact turns on when the first V-memory value is equal to the second value.



Key Sequence



Valid Data Types: First value V
Second value V and K

STRNE

Store Not Equal (STRNE) begins a new line of logic. The contact turns on when the first V-memory value is not equal to the second value.



Key Sequence

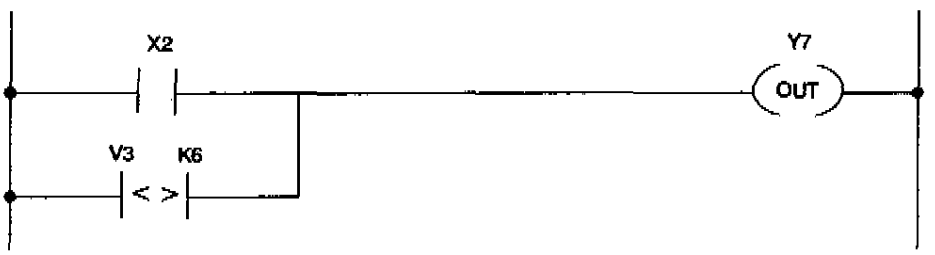


Valid Data Types: First value V
Second value V and K

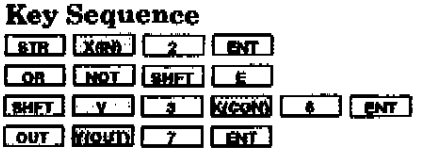
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ORNE

OR NOT Equal (ORNE) connects this contact in parallel with another. The contact turns on when the first V-memory value is not equal to the second value.



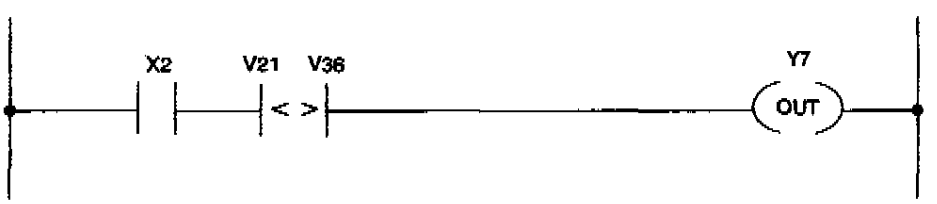
Key Sequence



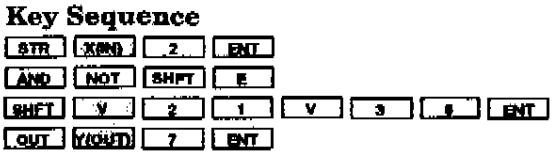
Valid Data Types: First value V
Second value V and K

ANDNE

AND NOT Equal (ANDNE) connects this contact in series with another. The contact turns on when the first V-memory value is not equal to the second value.



Key Sequence

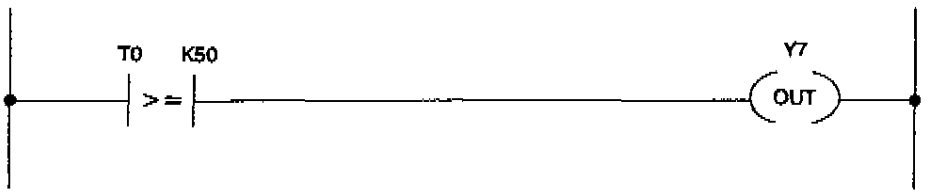


Valid Data Types: First value V
Second value V and K

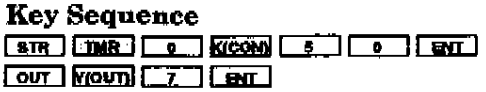
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STR

Store Greater Than or Equal (STR) begins a new line of logic. The contact turns on when the first value is greater than or equal to the second value.



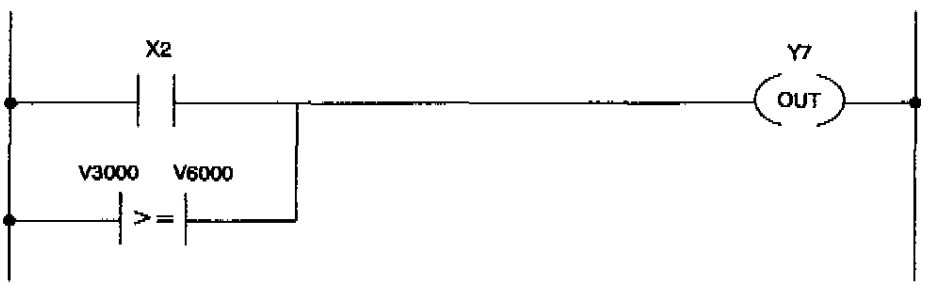
Key Sequence



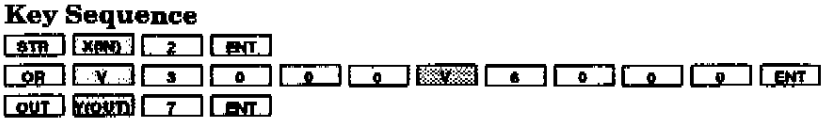
Valid Data Types: First value T, CT, V (1400-41027)
Second value V and K

OR

OR Greater Than or Equal (OR) connects this contact in parallel with another. The contact turns on when the first value is greater than or equal to the second value.



Key Sequence



Valid Data Types: First value T, CT, V (1400-41027)
Second value V and K

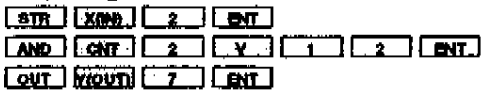
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AND

AND Greater Than or Equal (AND) connects this contact in series with another. The contact turns on when the first value is greater than or equal to the second value.



Key Sequence



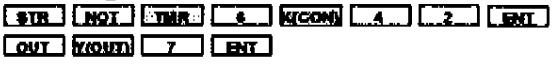
Valid Data Types: First value T, CT, V (1400-41027)
Second value V, K

STRN

Store Less Than (STRN) begins a new line of logic. The contact turns on when the first value is less than the second value.



Key Sequence

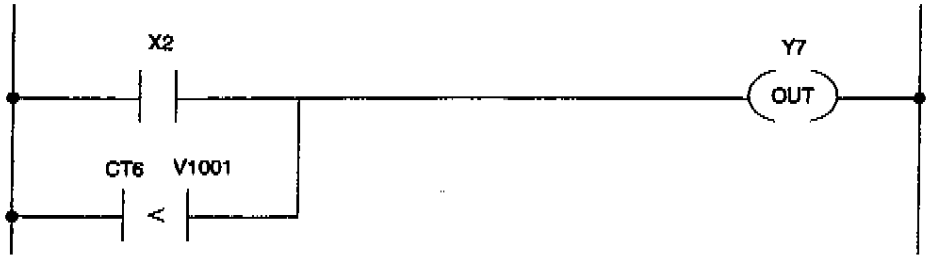


Valid Data Types: First value T, CT, V (1400-41027)
Second value V, K

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ORN

OR Less Than (ORN) connects this contact in parallel with another. The contact turns on when the first value is less than the second value.



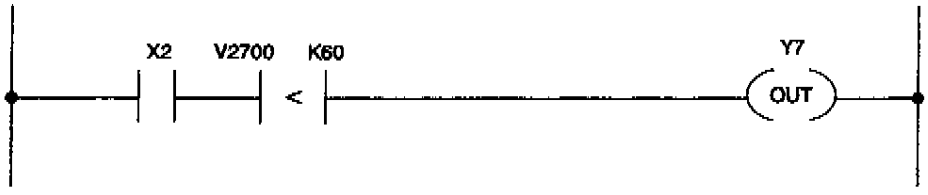
Key Sequence



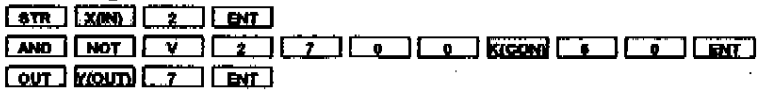
Valid Data Types: First value T, CT, V (1400-41027)
Second value V, K

ANDN

AND Less Than (ANDN) connects this contact in series with another. The contact turns on when the first value is less than the second value.



Key Sequence



Valid Data Types: First value T, CT, V (1400-41027)
Second value V, K

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Chapter 11
Immediate Instructions

STRI 11-2
STRNI 11-2
ORI 11-3
ORNI 11-4
ANDI 11-4
ANDNI 11-5
OUTI 11-5
OR OUTI 11-6
SETI 11-7
RSTI 11-7
LDIF (TI435 Only) 11-8
OUTIF (TI435 Only) 11-9

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STRI

Store Immediate (STRI) begins a new line of logic. The on/off state of the STRI contact is the same as the state of its physical input point, which is read immediately, not at the end of the scan.



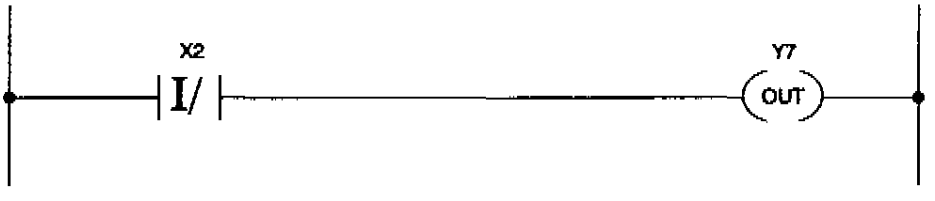
Key Sequence

STR | SHIFT | I | SHIFT | X(IN) | 2 | ENT
OUT | Y(OUT) | 7 | ENT

Valid Data Types: X

STRNI

Store NOT Immediate (STRNI) begins a new line of logic. The on/off state of the STRNI contact is opposite the state of its physical input point, which is read immediately, not at the end of the scan.



Key Sequence

STR | NOT | SHIFT | I | SHIFT | X(IN) | 2 | ENT
OUT | Y(OUT) | 7 | ENT

Valid Data Types: X

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ORI

OR Immediate (ORI) connects two logical elements in parallel. The on/off state of the contact following the ORI is the same as the state of its physical input point, which is read immediately, not at the end of the scan.



Key Sequence

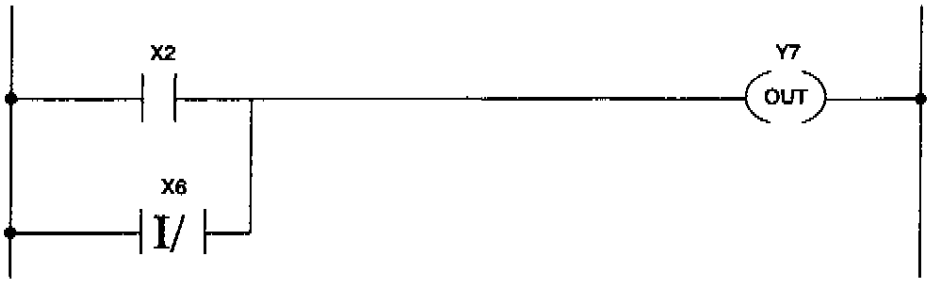
STR | X(IN) | 2 | ENT
OR | SHIFT | I | SHIFT | X(IN) | 6 | ENT
OUT | Y(OUT) | 7 | ENT

Valid Data Types: X

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ORNI

OR NOT Immediate (ORNI) connects two logic elements in parallel. The on/off state of the contact following the ORNI is opposite the state of its physical input point, which is read immediately, not at the end of the scan.



Key Sequence

STR | X(IN) | 2 | ENT
OR | NOT | SHFT | 1 | SHFT | X(IN) | 6 | ENT
OUT | Y(OUT) | 7 | ENT

Valid Data Types: X

ANDI

AND Immediate (ANDI) connects two logic elements in series. The on/off state of the contact following the ANDI is the same as the state of its physical input point, which is read immediately, not at the end of the scan.



Key Sequence

STR | X(IN) | 2 | ENT
AND | SHFT | 1 | SHFT | X(IN) | 6 | ENT
OUT | Y(OUT) | 7 | ENT

Valid Data Types: X

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ANDNI

AND NOT Immediate (ANDNI) connects two logic elements in series. The on/off state of the contact following the ANDNI is opposite the state of its physical input point, which is read immediately, not at the end of the scan.



Key Sequence

STR | X(IN) | 2 | ENT
AND | NOT | SHIFT | I | SHIFT | X(IN) | 6 | ENT
OUT | Y(OUT) | 7 | ENT

Valid Data Types: X

OUTI

OUT Immediate (OUTI) ends a line of logic. The on/off state of the physical output point is updated immediately, not at the end of the scan. If the same point is used as an immediate output more than once in a program, it is possible for the state of that physical output point to change several times during one program scan.



Key Sequence

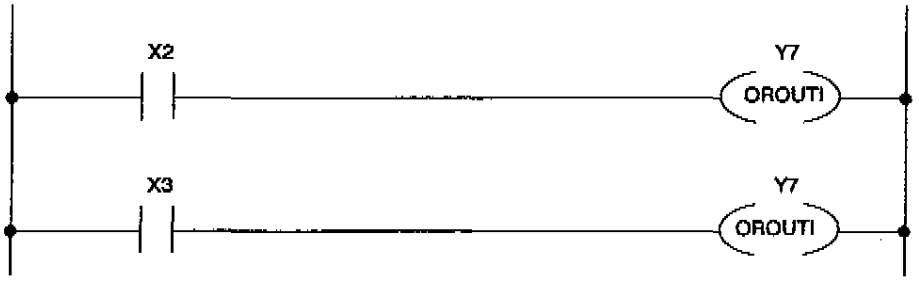
STR | X(IN) | 2 | ENT
OUT | SHIFT | I | SHIFT | Y(OUT) | 7 | ENT

Valid Data Types: Y

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OR OUTI

OR OUT Immediate (OR OUTI) ends a line of logic. The on/off state of the physical output point is updated immediately, not at the end of the scan. If the same point is used as an immediate output more than once in a program, the outputs are considered to be OR'ed together, so that an inactive occurrence of an output later in the program scan does not override an active occurrence.



Key Sequence

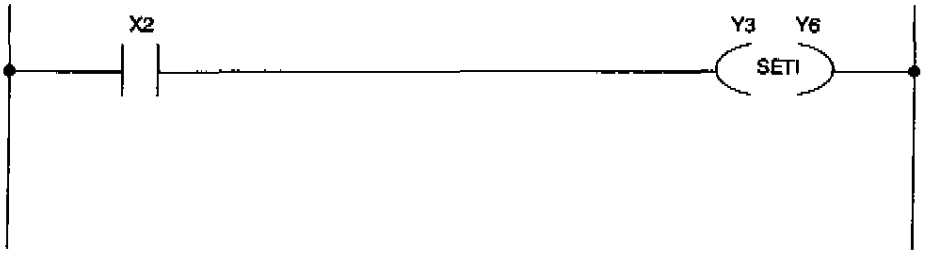


Valid Data Types: Y

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SETI

Set Output Point Range Immediate (SETI) turns on a range of physical output points immediately, not at the end of the scan. If any of the set points are used as outputs elsewhere in the program, they continue to be controlled by program logic.



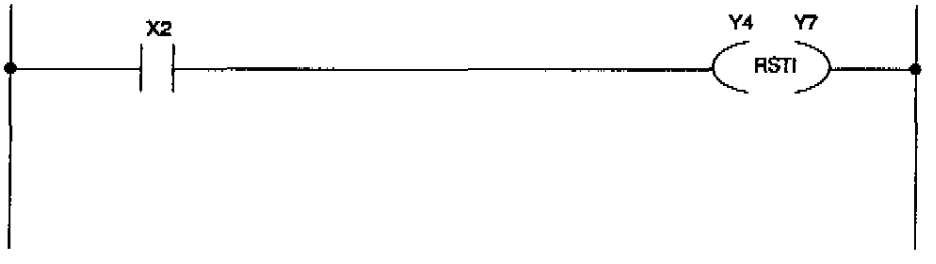
Key Sequence

STR | X(IN) | 2 | ENT
SET | SHIFT | 1 | SHIFT | Y(OUT) | 3 | Y(OUT) | 6 | ENT

Valid Data Types: Y

RSTI

Reset Output Point Range Immediate (RSTI) turns off a range of physical output points immediately, not at the end of the scan. If any of the reset points are used as outputs elsewhere in the program, they continue to be controlled by program logic.



Key Sequence

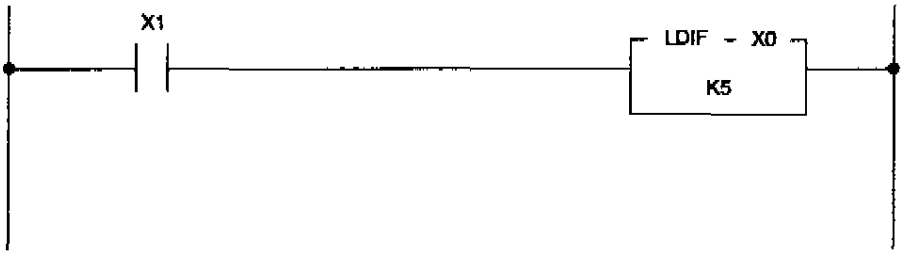
STR | X(IN) | 2 | ENT
RST | SHIFT | 1 | SHIFT | Y(OUT) | 4 | Y(OUT) | 7 | ENT

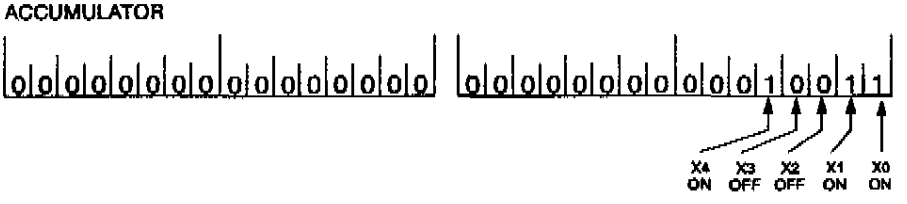
Valid Data Types: Y

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LDIF (TI435 Only)

Load Accumulator Immediate (LDIF) loads up to 32 bits from X input points to the accumulator. The current status of the physical inputs is loaded immediately, not at the end of the scan. The specified point is loaded as the least significant bit, and any upper accumulator bits that are not loaded are set to zero.





Key Sequence

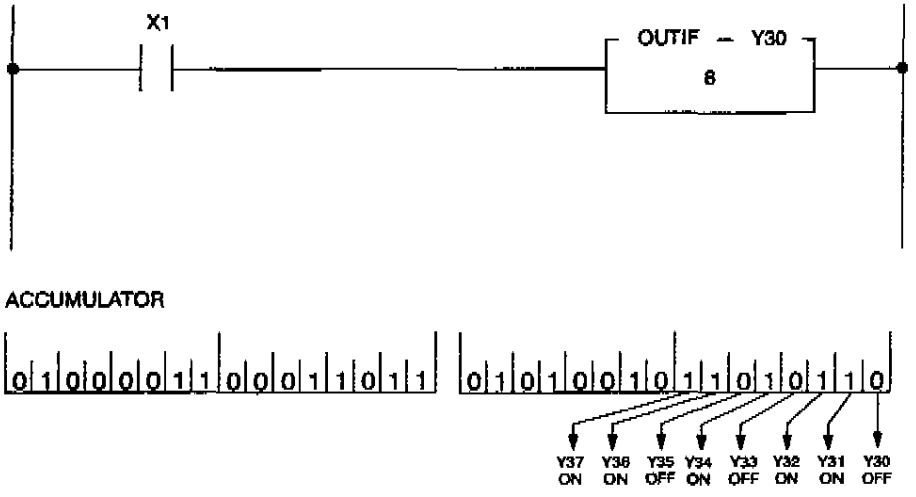


Valid Data Types:	First value	X
	Second value	K (1–32)

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OUTIF
(TI435 Only)

Output Accumulator Immediate (OUTIF) moves up to 32 bits from the accumulator to Y output points. The state of the physical output points is updated immediately, not at the end of the scan. The least significant bit from the accumulator is moved to the specified point.



Key Sequence

STR X(IN) 1 ENT
OUT SHFT 1 F
SHFT Y(OUT) 3 0 K(CONS) 8 ENT

Valid Data Types:

First value	Y
Second value	K (1–32)

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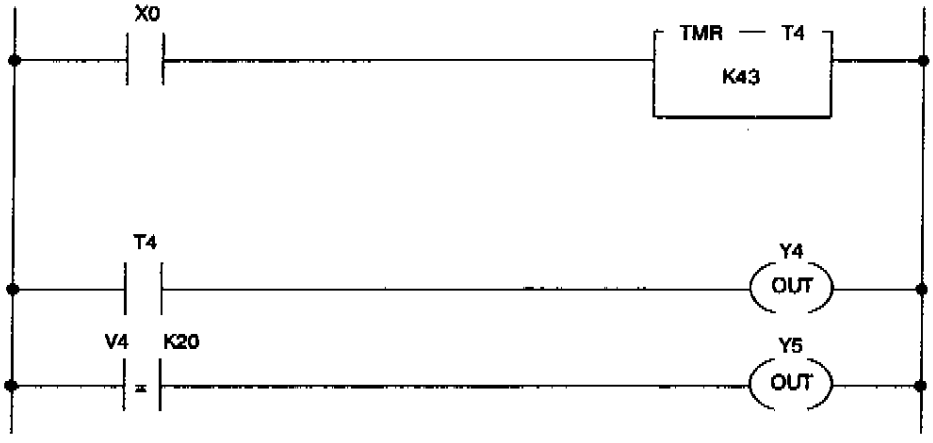
Chapter 12
Timer and Counter Instructions

TMR 12-2
TMRF 12-3
TMRA 12-4
TMRAF 12-5
CNT 12-6
SGCNT 12-7
UDC 12-8

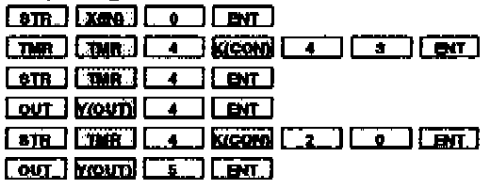
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TMR

Timer (TMR). When the input is on, the TMR increments every 0.1 seconds. When the input is off, the timer resets. The TMR can also be reset with the RST instruction. When the current value is greater than or equal to the preset, the timer contact with the corresponding T-number turns on. You may also specify a different preset with the timer contact. A timer contact with a preset turns on when the timer current value equals that preset, and remains on until the timer is reset. The TMR continues to increment past its preset, up to a maximum of 999.9 seconds. The current value of any TMR is stored in the V-memory location with the same number as the timer, so the current value for TMR T4 is at location V4. Each timer must have a unique number between 0 and 177 (octal). In the example, Y4 turns on 4.3 seconds after X0 is closed. Y5 turns on 2.0 seconds after X0 is closed.



Key Sequence



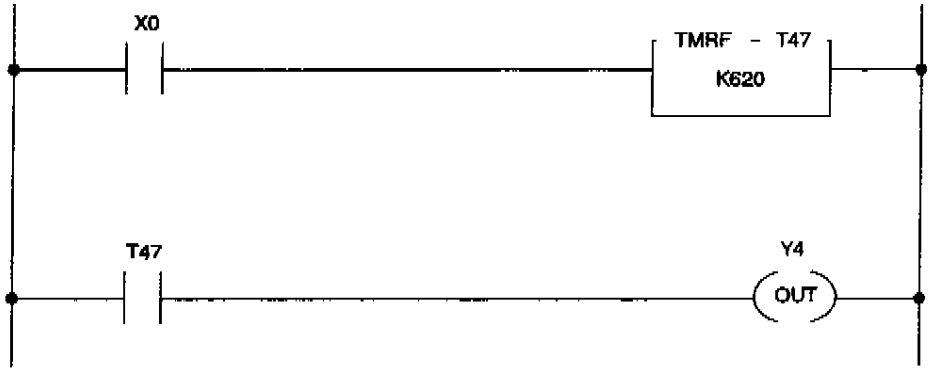
Valid Data Types:

First value	T
Second value	V, and K (1-9999)

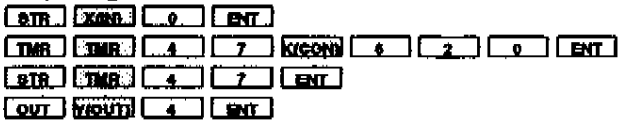
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TMRF

Fast Timer (TMRF). When the input is on, the TMRF increments every 0.01 seconds. When the input is off, the timer resets. The TMRF can also be reset with the RST instruction. When the current value is greater than or equal to the preset, the timer contact with the corresponding T-number turns on. The TMRF continues to increment past its preset, up to a maximum of 99.99 seconds. The current value of any TMRF is stored in the V-memory location with the same number as the timer, so the current value for TMRF T47 is at location V47. Each timer must have a unique number between 0 and 177 (octal). In the example, Y4 turns on 6.2 seconds after X0 is closed.



Key Sequence



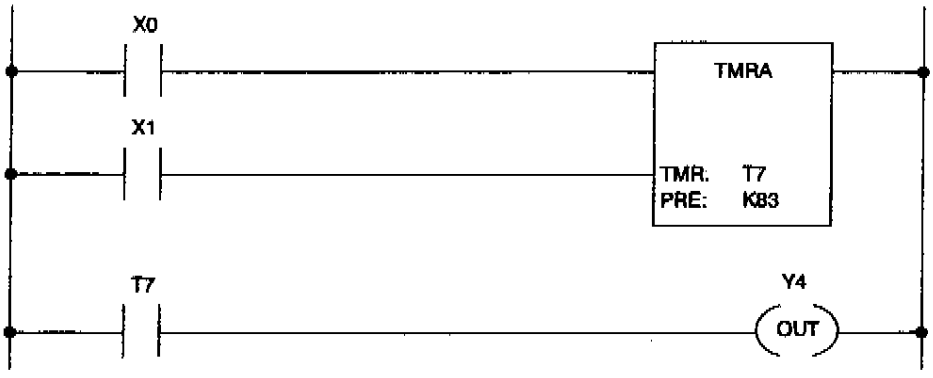
Valid Data Types:

First value	T
Second value	V and K (1-9999)

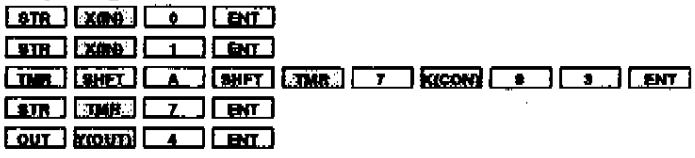
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TMRA

Accumulating Timer (TMRA). When the upper contact is on, the TMRA increments every 0.1 seconds. When the upper contact is off, the timer holds its current value. When the contact turns on again, timing resumes from the current value. When the lower contact is on, the timer is reset to zero. When the current value is greater than or equal to the preset, the timer contact with the corresponding T-number turns on. The TMRA continues to increment past its preset, up to a maximum of 9999999.9 seconds. The current value of any TMRA is stored in two V-memory locations, starting with the one that has the same number as the timer. TMRA T30 stores its current value at V30 and V31. This means that there cannot be a timer number T31, since its corresponding V-memory location is already in use. Each timer must have a unique number between 0 and 177 (octal). In the example, Y4 turns on after X0 has been closed for a total of 8.3 seconds.



Key Sequence

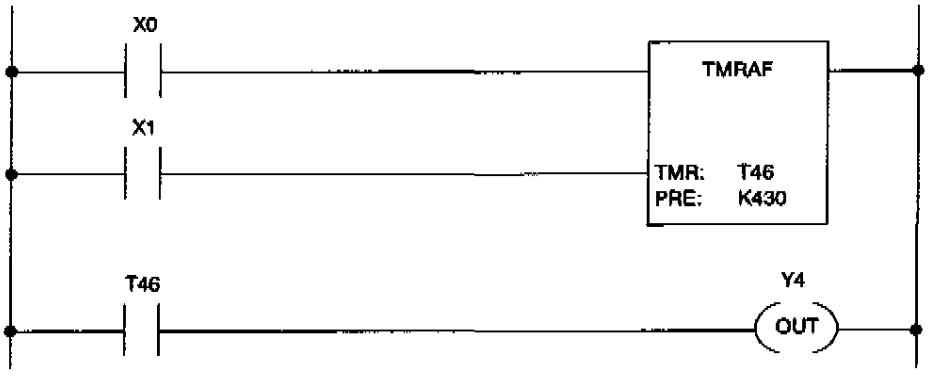


Valid Data Types:	First value	T
	Second value	V and K (1-99999999)

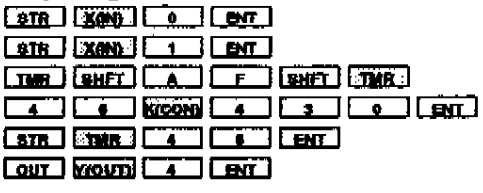
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TMRAF

Fast Accumulating Timer (TMRAF). When the upper contact is on, the TMRAF increments every 0.01 seconds. When the upper contact is off, the timer holds its current value. When the contact turns on again, timing resumes from the current value. When the lower contact is on, the timer is reset to zero. When the current value is greater than or equal to the preset, the timer contact with the corresponding T-number turns on. The TMRAF continues to increment past its preset, up to a maximum of 999999.99 seconds. The current value of any TMRAF is stored in two V-memory locations, starting with the one that has the same number as the timer. TMRAF T46 stores its current value at V46 and V47. This means that there cannot be a timer number T47, since its corresponding V-memory location is already in use. Each timer must have a unique number between 0 and 177 (octal). In the example, Y4 turns on after X0 has been closed for a total of 4.3 seconds.



Key Sequence



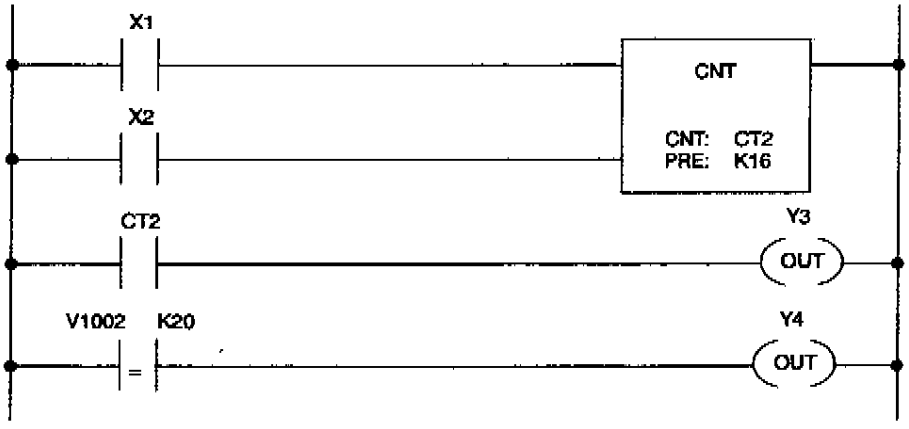
Valid Data Types:

First value	T
Second value	V and K (1-99999999)

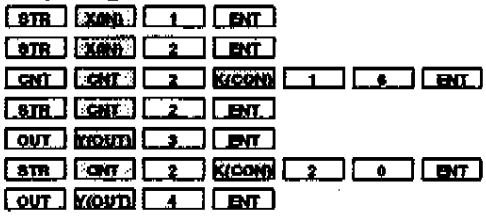
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CNT

The Counter (CNT) increments with each off-to-on transition of its upper contact. The contact with the same CT-number as the counter is on when the current count is greater than or equal to the preset. You may also specify a different preset with the counter contact. A counter contact with a preset turns on when the counter current value equals that preset, and remains on until the counter is reset. The current count continues to increment past the preset to a maximum of 9999. The current count is stored in a V-memory location equal to the counter number plus 1000, so counter CT2 stores its current count in V1002. The CNT retains its current count until its lower contact is turned on; this resets it to zero. In the example, Y3 comes on after X1 has been toggled 16 times. Y4 comes on after X1 has been toggled a total of 20 times. Turning on X2 resets the counter.



Key Sequence

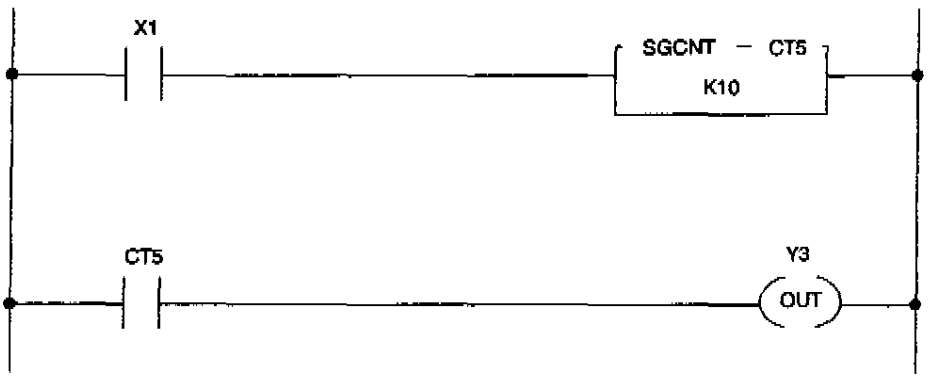


Valid Data Types:	First value	CT
	Second value	V and K (1-9999)

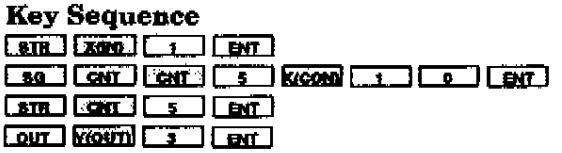
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SGCNT

The Stage Counter (SGCNT) increments with each off-to-on transition of its input. The contact with the same CT-number as the counter is on when the current count is greater than or equal to the preset. The current count continues to increment past the preset to a maximum of 9999. The current count is stored in a V-memory location equal to the counter number plus 1000, so counter CT7 stores its current count in V1007. The SGCNT retains its current count until reset with an RST instruction. In the example, Y3 comes on after X1 has been toggled 10 times.



Key Sequence

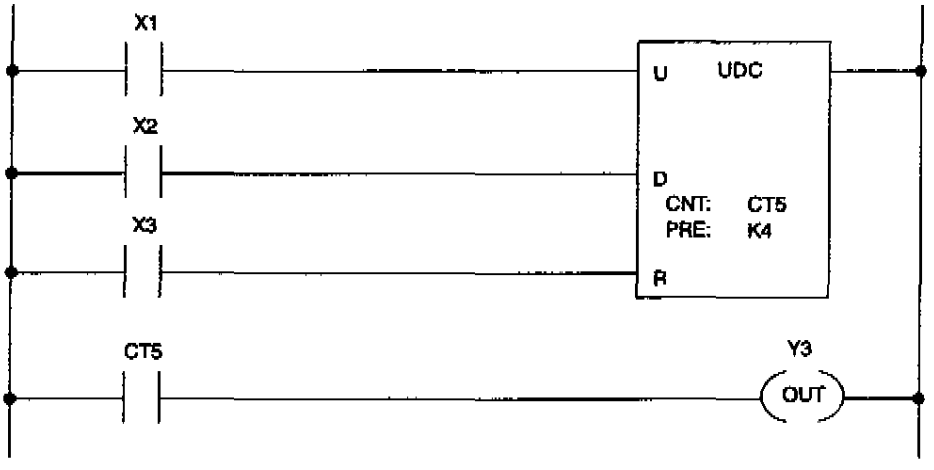


Valid Data Types:	First value	CT
	Second value	V and K (1-9999)

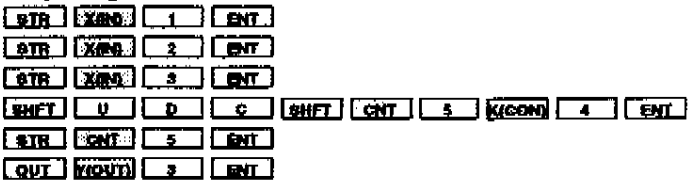
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UDC

The Up/Down Counter (UDC) increments with each off-to-on transition of its U contact, and decrements with each off-to-on transition of its D contact. The contact with the same CT-number as the counter is on when the current count is greater than or equal to the preset. The current count continues to increment past the preset to a maximum of 99999999. The count decrements to a minimum of 0. The current count is stored in two V-memory locations starting with the one equal to the counter number plus 1000. UDC CT5 stores its current count in V1005 and V1006. This means that there cannot be a counter CT6, since its corresponding V-memory location has been used. The UDC retains its current count until the R contact is turned on; this resets it to zero. In the example, Y3 turns on after X1 has been toggled 4 times, and back off after X2 is toggled.



Key Sequence



Valid Data Types:

First value	CT
Second value	V and K (1-99999999)

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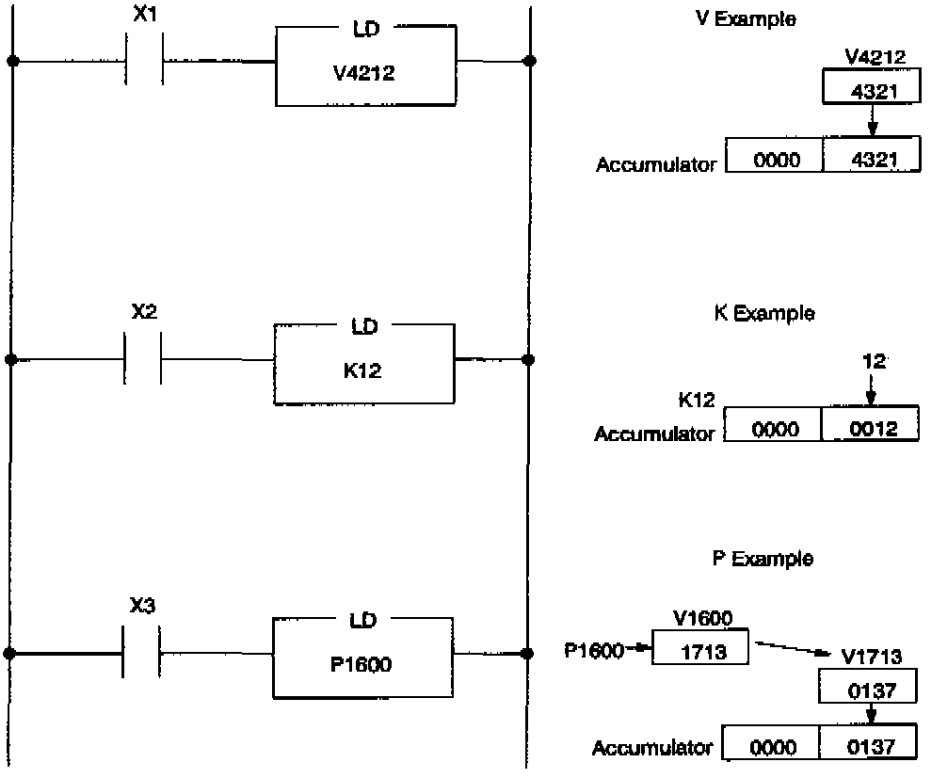
Chapter 13
Accumulator Data Manipulation Instructions

LD 13-2
LDD 13-3
LDX 13-4
LDA 13-5
OUT 13-6
OUTD 13-7
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AND 13-9
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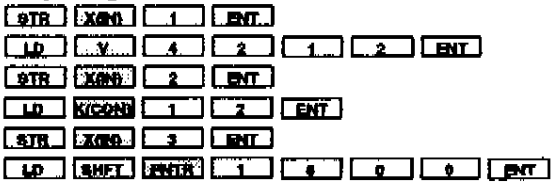
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LD

Load Accumulator with Word (LD) places a 16-bit value into the 32-bit accumulator. The upper 16-bits of the accumulator are zeroed. If LD is used with a V data type, the value from that V-memory location is loaded. If it is used with a K data type, the constant value is loaded directly. If used with a P data type, the value from the V-memory location is loaded by the value pointing to that address.



Key Sequence

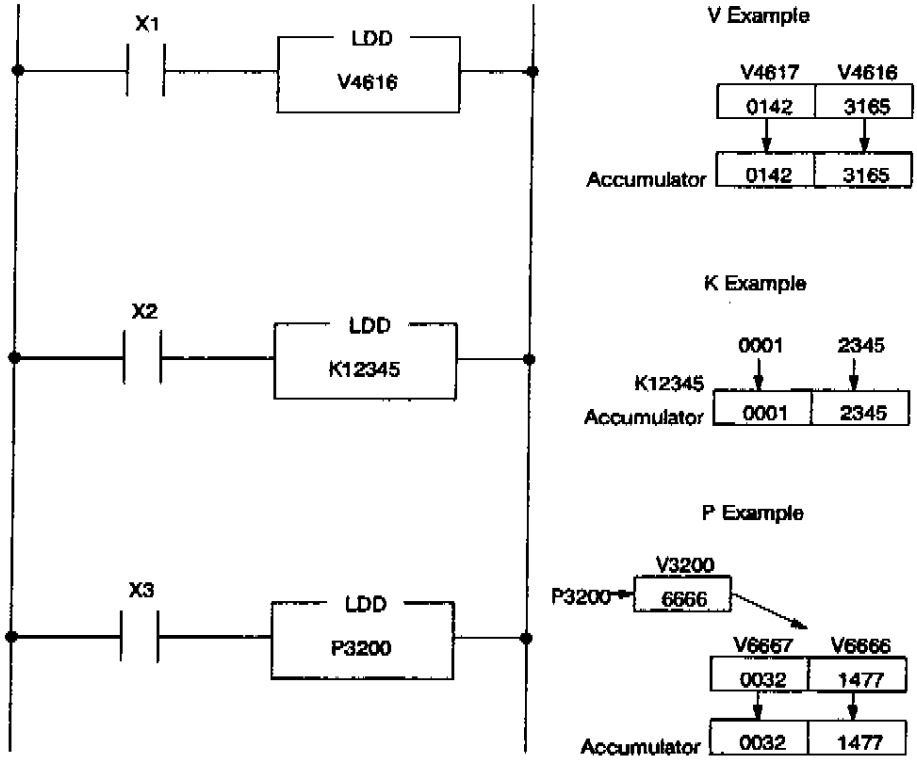


Valid Data Types: V, P, and K

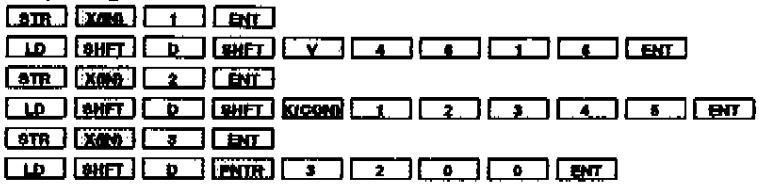
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LDD

Load Accumulator with Double Word (LDD) places a 32-bit value into the 32-bit accumulator. If LDD is used with a V data type, the value from that V-memory location and the one following it are loaded. If it is used with a K data type, the constant value is loaded directly. If used with a P data type, the values from two V-memory locations are loaded. The P value points to the address of the first of the two locations.



Key Sequence

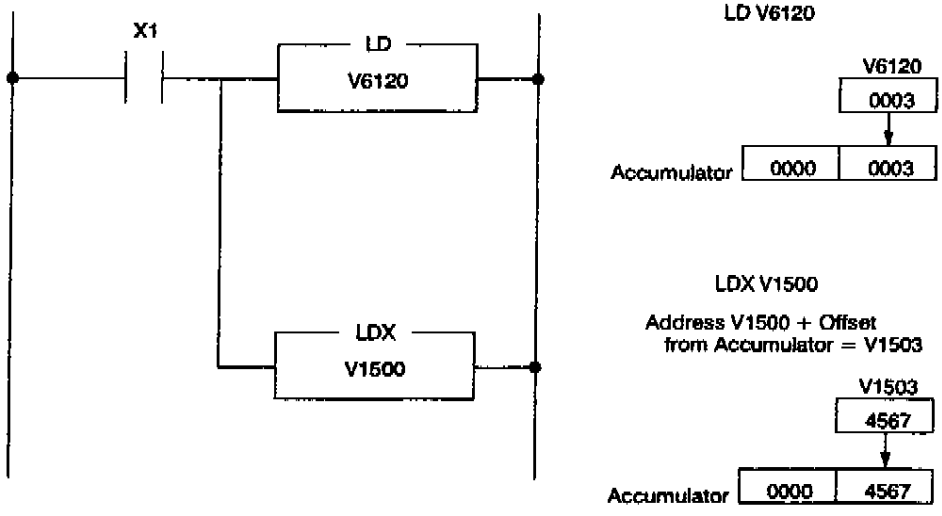


Valid Data Types: V, P, and K

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LDX

Load Accumulator Indexed (LDX) places a 16-bit value into the 32-bit accumulator. The upper 16-bits are zeroed. The contents of the accumulator are used as an offset from the V-memory location supplied by the LDX instruction to calculate the address value that is loaded back to the accumulator. In the example, the LD V6120 instruction is used to load the offset into the accumulator before executing the LDX V1500.



Key Sequence



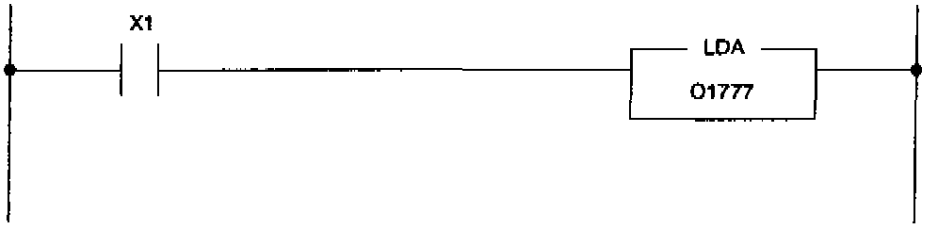
Valid Data Types: V

NOTE: The offset is read as a hexadecimal number and then converted to an octal offset.

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LDA

Load Accumulator with Address (LDA) loads the accumulator with an octal constant to be used for addressing V-memory.



Key Sequence

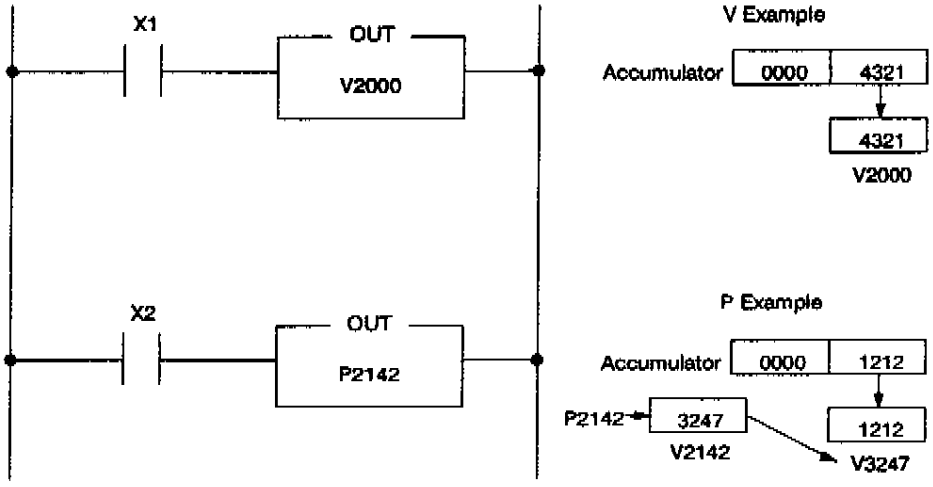
STR | X/IN | 1 | ENT
LD | SHIFT | A | OCT | 1 | 7 | 7 | 7 | ENT

Valid Data Types: O (0 – 77777)

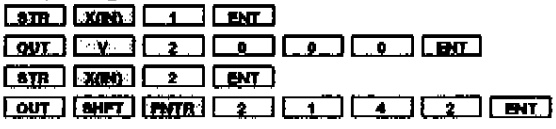
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OUT

Output Accumulator Right Most Word (OUT) stores a 16-bit value from the accumulator into V-memory. When OUT is used with a V data type, the value is placed in that V-memory location. When used with a P data type, the value is placed in the V-memory location pointed to by the P value.



Key Sequence

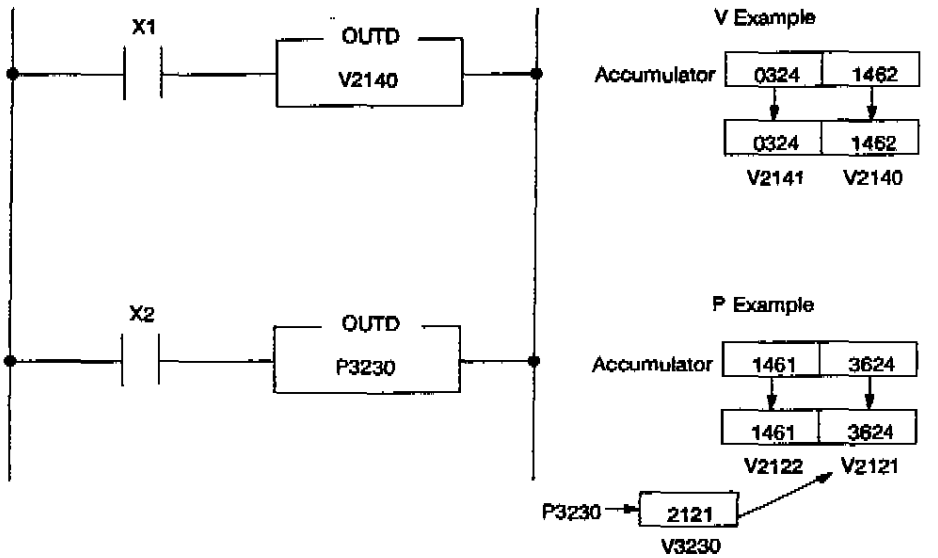


Valid Data Types: V (0-41027) and P

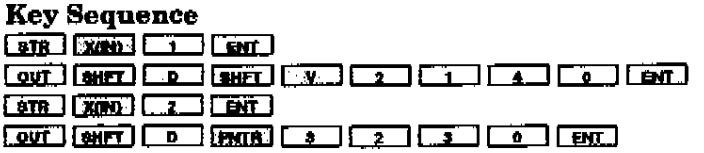
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OUTD

Output Accumulator Double Word (OUTD) stores a 32-bit value from the accumulator into two consecutive V-memory locations. When OUTD is used with a V data type, the value is placed in that memory location and in the next one. When used with a P data type, the value is placed in two V-memory locations, starting with the one pointed to by the P value.



Key Sequence

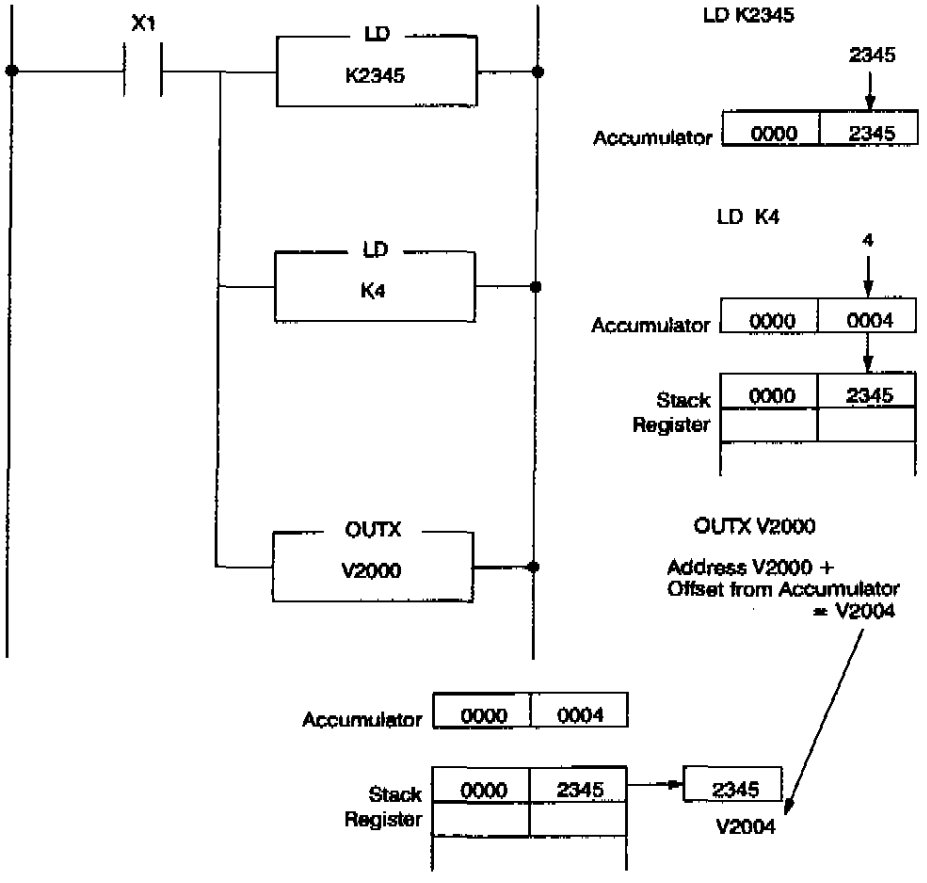


Valid Data Types: V and P

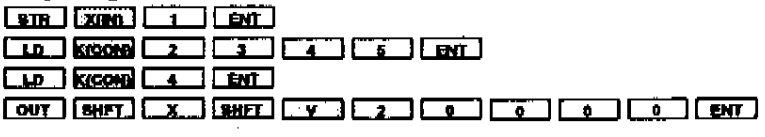
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OUTX

Output Accumulator Indexed (OUTX) stores a 16-bit value from the first stack register at a V-memory address formed by adding an offset value from the accumulator to the address used with the OUTX instruction. In the example, LD K2345 loads a 16-bit value into the accumulator. LD K4 loads an offset of 4 into the accumulator and pushes the previous contents into the first stack register.



Key Sequence



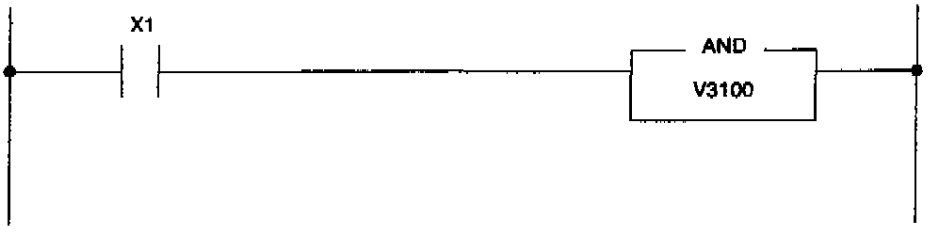
Valid Data Types: V

NOTE: The offset is read as a hexadecimal number and then converted to an octal offset.

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AND

AND Accumulator with Word (AND) performs a logical AND between the accumulator and a four-digit V-memory value. The result is stored in the accumulator. Flags SP63 and 70 are set according to the result.



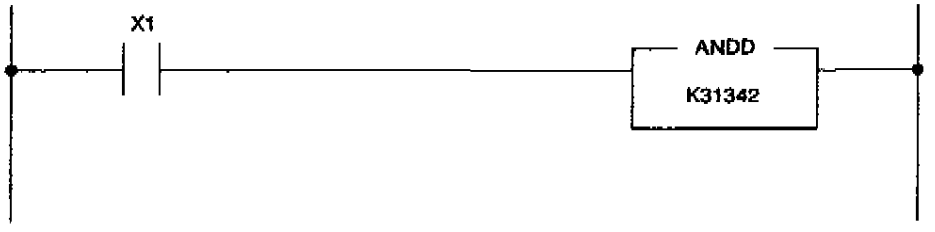
Key Sequence



Valid Data Types: V

ANDD

AND Accumulator with Double Word (ANDD) performs a logical AND between the accumulator and an eight-digit V-memory, or constant value, or the contents of two consecutive V locations. The specified V location contains the least significant two bytes. The result is stored in the accumulator. Flags SP63 and 70 are set according to the result.



Key Sequence



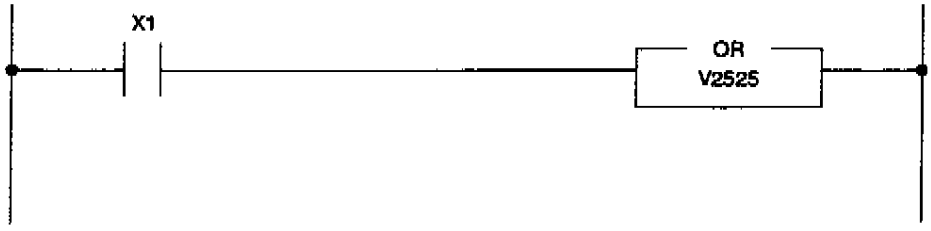
Valid Data Types:

TI425	K
TI435	V and K

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OR

OR Accumulator with Word (OR) performs a logical OR between the accumulator and a four-digit V-memory value. The result is stored in the accumulator.



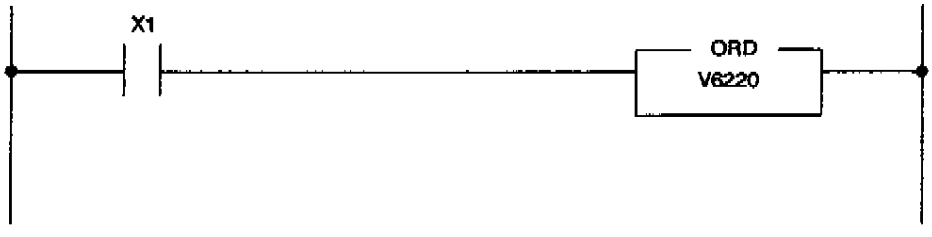
Key Sequence



Valid Data Types: V

ORD

OR Accumulator with Double Word (ORD) performs a logical OR between the accumulator and an eight-digit V-memory or constant value or the contents of two consecutive V locations. The specified V location contains the least significant two bytes. The result is stored in the accumulator.



Key Sequence



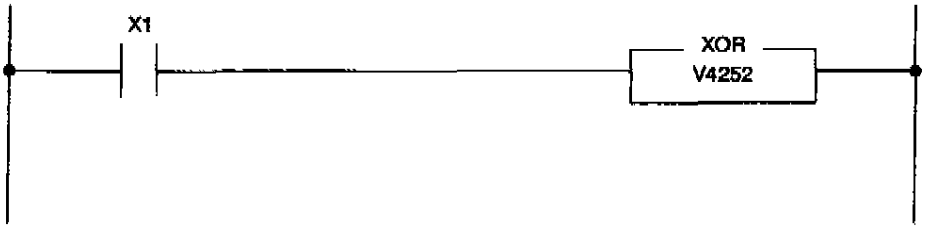
Valid Data Types:

TI425	K
TI435	V and K

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XOR

Exclusive OR Accumulator with Word (XOR) performs a logical exclusive OR between the accumulator and a four-digit V-memory value. The result is stored in the accumulator.



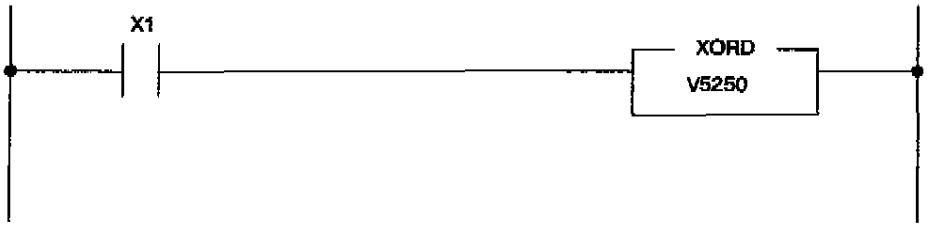
Key Sequence

STR | X(IN) | 1 | ENT
SHIFT | X | SHIFT | OR | V | 4 | 2 | 5 | 2 | ENT

Valid Data Types: V

XORD

Exclusive OR Accumulator with Double Word (XORD) performs a logical exclusive OR between the accumulator and an eight-digit V-memory, or constant value, or the contents of two consecutive V locations. The specified V location contains the least significant two bytes. The result is stored in the accumulator.



Key Sequence

STR | X(IN) | 1 | ENT
SHIFT | X | SHIFT | OR | SHIFT | 0 | SHIFT | V | 5 | 2 | 5 | 0 | ENT

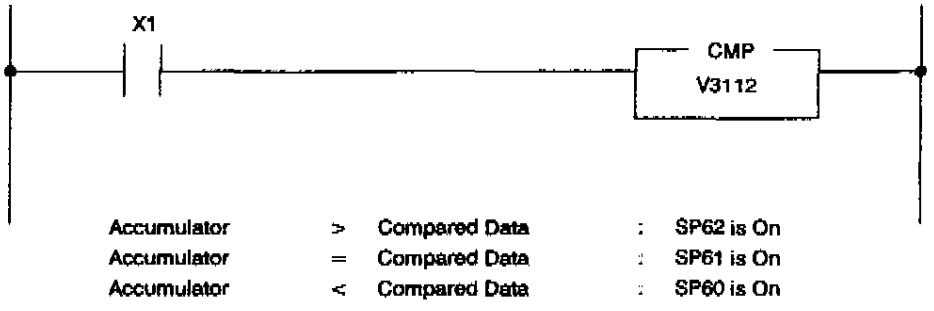
Valid Data Types:

TI425	K
TI435	V and K

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CMP

Compare Accumulator with Word (CMP) compares a four-digit V-memory value with the accumulator. Flags SP60, 61 and 62 are set according to the result.



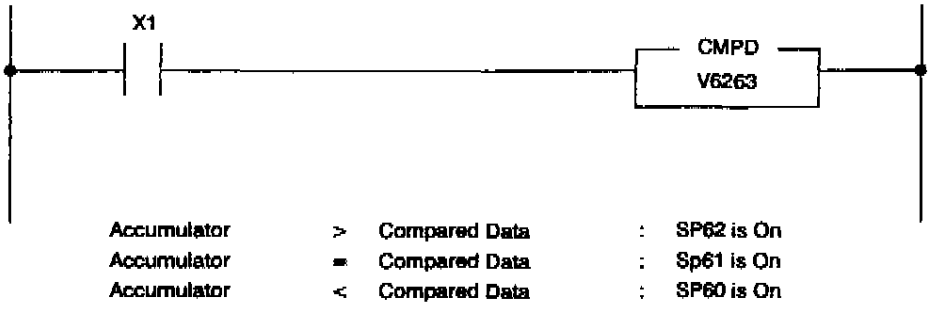
Key Sequence



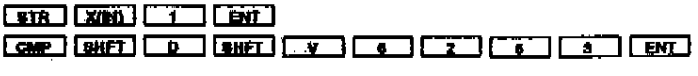
Valid Data Types: V

CMPD

Compare Accumulator with Double Word (CMPD) compares an eight-digit V constant value, or the contents of two consecutive V locations, with the accumulator. The specified V location contains the least significant two bytes. Flags SP60, 61 and 62 are set according to the result.



Key Sequence



Valid Data Types:

TI425	K
TI435	V and K

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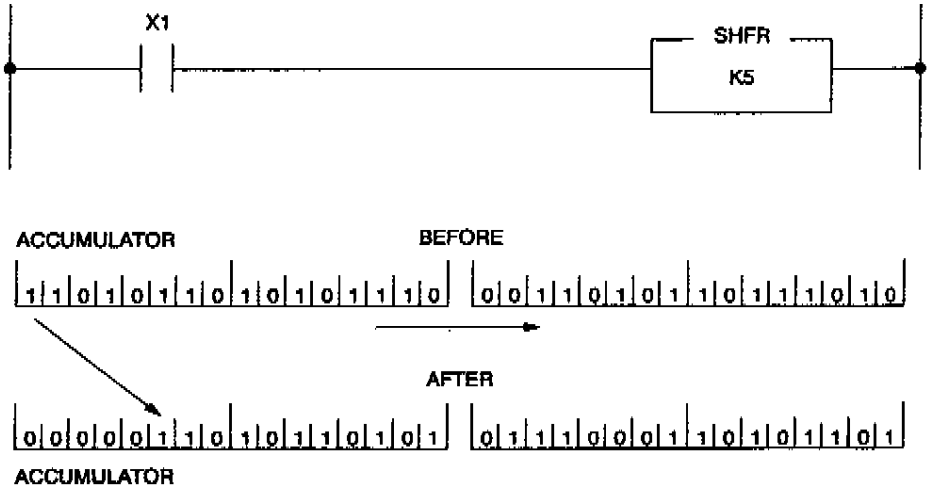
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SHFR

Shift Accumulator Right (SHFR) shifts the value in the accumulator to the right by the number of bit positions specified by a V-memory location or a constant value. Vacant bits on the left are zero filled. The shift can be up to 32 positions. A 32-bit shift sets the accumulator to zero.



Key Sequence

STR | K/CON | 1 | ENT
SHIFT | S | H | F | R | SHIFT | K/CON | 5 | ENT

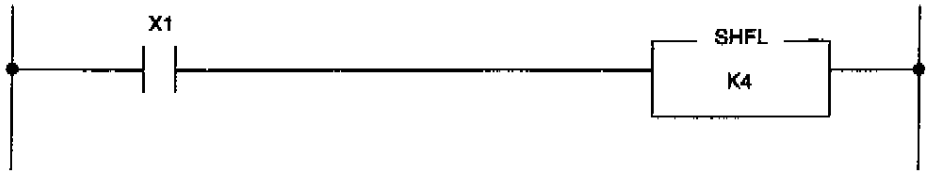
Valid Data Types: V and K

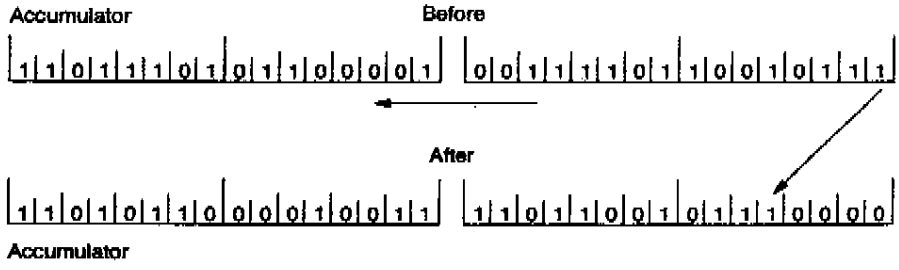
NOTE: The shift value must be a hexadecimal number in the range of 1–F.

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SHFL

Shift Accumulator Left (SHFL) shifts the value in the accumulator to the left by the number of bit positions specified by a V-memory location or a constant value. Vacant bits on the right are zero filled. The shift can be up to 32 positions. A 32-bit shift sets the accumulator to zero.





Key Sequence

STR | X/Ctrl | 1 | ENT

SHFT | 9 | H | F | L | SHFT | X/CONT | 4 | ENT

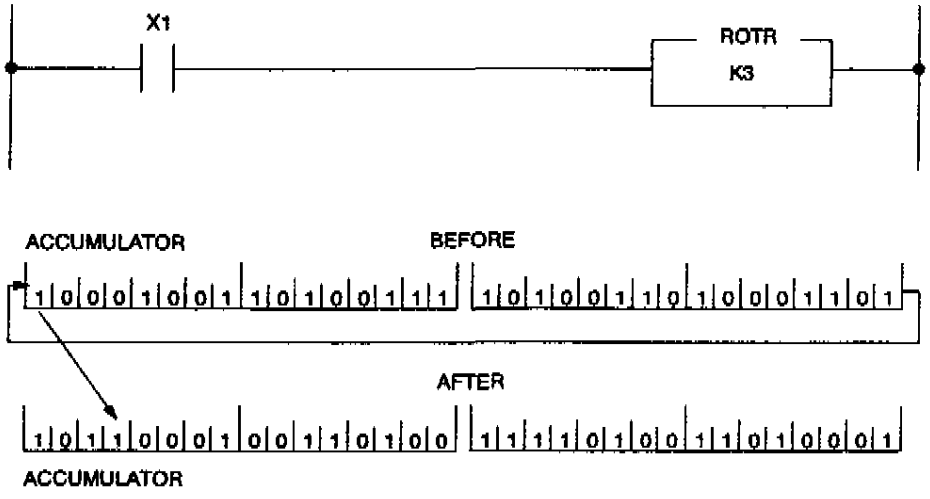
Valid Data Types: V and K

NOTE: The shift value must be a hexadecimal number in the range 1–F.

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ROTR

Rotate Accumulator Right (ROTR) rotates the value in the accumulator to the right by the number of bit positions specified by a V-memory location or a constant value. As a bit is pushed out the right end of the accumulator, it is loaded back into the left end to fill the vacancy. The rotation can be up to 32 positions.



Key Sequence

STR | X/INS | 1 | ENT
SHIFT | R | O | T | R | SHIFT | K/CONT | 3 | ENT

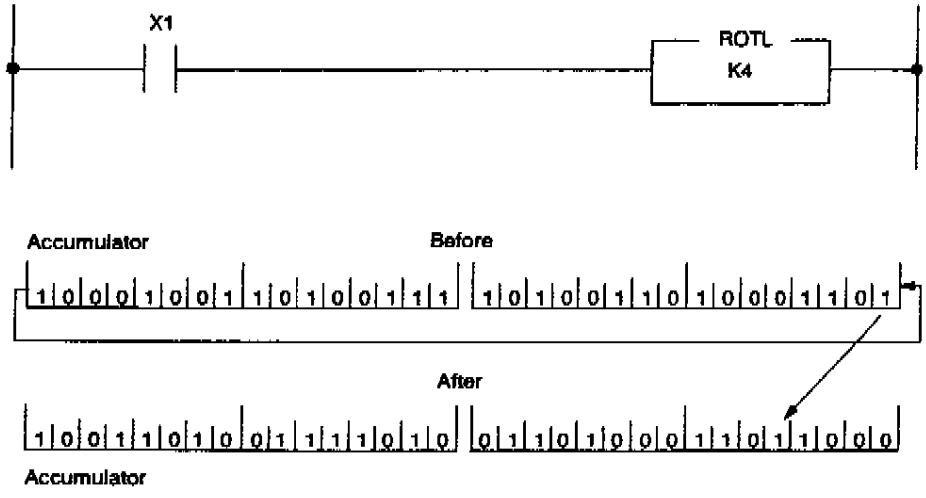
Valid Data Types: V and K

NOTE: The rotate value must be a hexadecimal number in the range of 1–F.

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ROTL

Rotate Accumulator Left (ROTL) rotates the value in the accumulator to the left by the number of bit positions specified by a V-memory location or a constant value. As a bit is pushed out the left end of the accumulator, it is loaded back into the right end to fill the vacancy. The rotation can be up to 32 positions.



Key Sequence



Valid Data Types: V and K

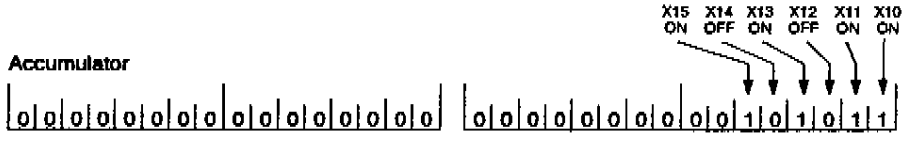
NOTE: The rotate value must be a hexadecimal number in the range of 1–F.

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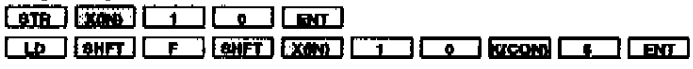
LDF (TI435 Only)

Load Accumulator from Image Register Range (LDF) loads up to thirty-two bits from the specified bit image register to the accumulator. The specified point is loaded as the least significant bit, and any upper accumulator bits that are not loaded are set to zero.





Key Sequence



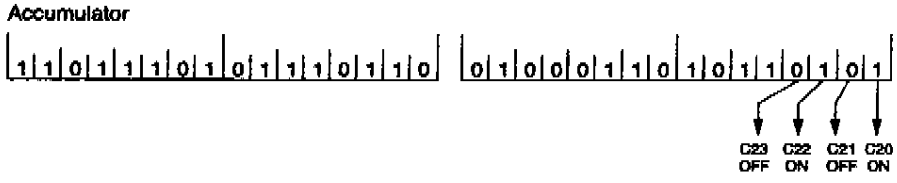
Valid Data Types:	First value	X, Y, C, S, T, CT, SP, and GX
	Second value	K (1–32)

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OUTF (TI435 Only)

Output Accumulator to Image Register Range (OUTF) moves up to 32 bits from the accumulator to the specified bit image register. The least significant bit from the accumulator is moved to the specified point.





Key Sequence

STR | X(IN) | 1 | ENT
OUT | SHIFT | F | SHIFT | C(CR) | 2 | 0 | K(CON) | 4 | ENT

Valid Data Types:

First value	X,Y, C, GX
Second value	K (1–32)

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ADDF (TI435 Only)

Add to Accumulator (ADDF) adds the value formed by the specified image register bits to the eight-digit BCD value in the accumulator. The specified point is the least significant bit. The result is stored in the accumulator. Special relays SP63, SP64, and SP70 are set according to the result.



Key Sequence

STR | X/#N | 1 | ENT

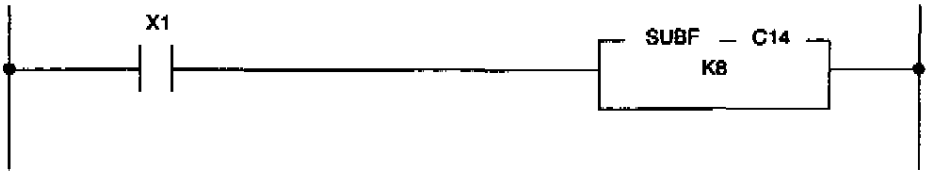
ADD | SHIFT | F | SHIFT | X/#N | 1 | 0 | K/CONT | 4 | ENT

Valid Data Types:

First value	X, Y, C, S, T, CT, SP, and GX
Second value	K (1–32)

SUBF (TI435 (Only)

Subtract from Accumulator (SUBF) subtracts the value formed by the specified image register bits from the eight-digit BCD value in the accumulator. The specified point is the least significant bit. The result is stored in the accumulator. Special relays SP63, SP64, SP65, and SP70 are set according to the result.



Key Sequence

STR | X/#N | 1 | ENT

SUB | SHIFT | F | SHIFT | G/CR | 1 | 4 | K/CONT | 8 | ENT

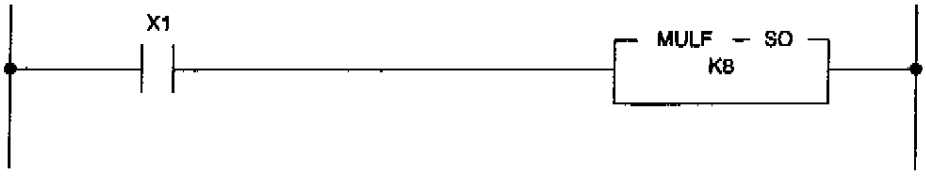
Valid Data Types:

First value	X, Y, C, S, T, CT, SP, and GX
Second value	K (1–32)

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MULF (TI435 Only)

Multiply Accumulator by Image Register Range (MULF) multiplies the four-digit BCD value in the accumulator by the value formed by the specified image register bits. The specified point is the least significant bit. The result is stored in the accumulator. Special relays SP63 and SP70 are set according to the result.



Key Sequence

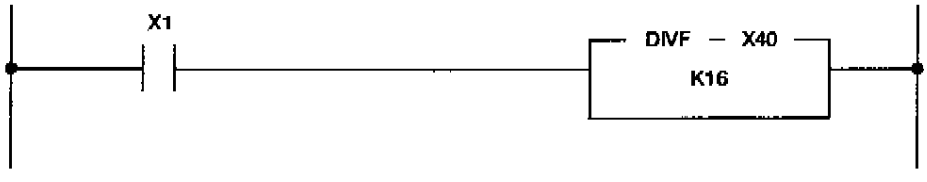
STR | X(IN) | 1 | ENT
MUL | SHFT | F | SHFT | X(SG) | 0 | K(CON) | 8 | ENT

Valid Data Types:

First value	X, Y, C, S, T, CT, SP, and GX
Second value	K (1–16)

DIVF (TI435 Only)

Divide Accumulator by Image Register Range (DIVF) divides the eight-digit BCD value in the accumulator by the value formed by the specified image register bits. The specified point is the least significant bit. The result is stored in the accumulator. Special relays SP53, SP63 and SP70 are set according to the result.



Key Sequence

STR | X(IN) | 1 | ENT
DIV | SHFT | F | SHFT | X(IN) | 4 | 0 | K(CON) | 1 | 6 | ENT

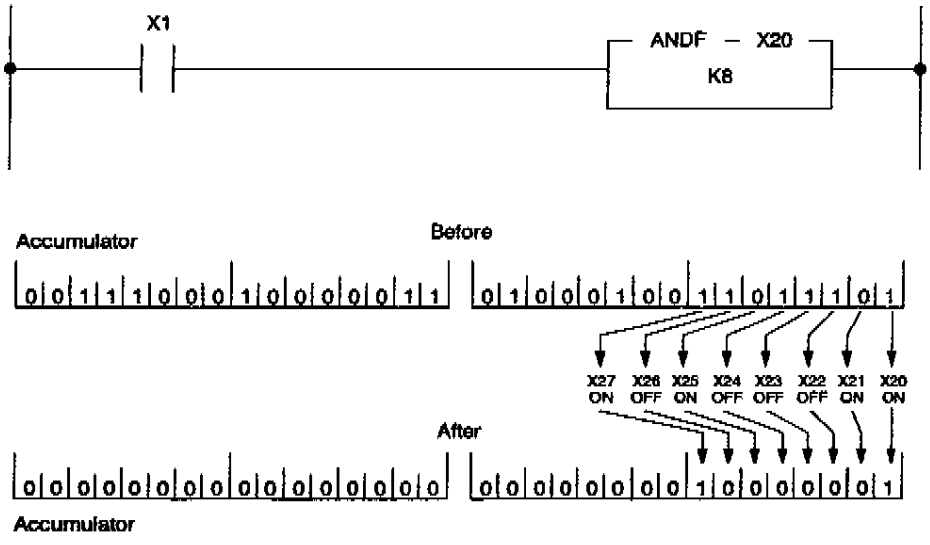
Valid Data Types:

First value	X, Y, C, S, T, CT, SP, and GX
Second value	K (1–16)

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ANDF (TI435 Only)

AND Accumulator with Image Register Range (ANDF) ANDs the contents of the accumulator with the indicated number of bits from the specified image register. The specified point is the least significant bit. The result is stored in the accumulator. Special relays SP63 and SP70 are set accordingly.



Key Sequence

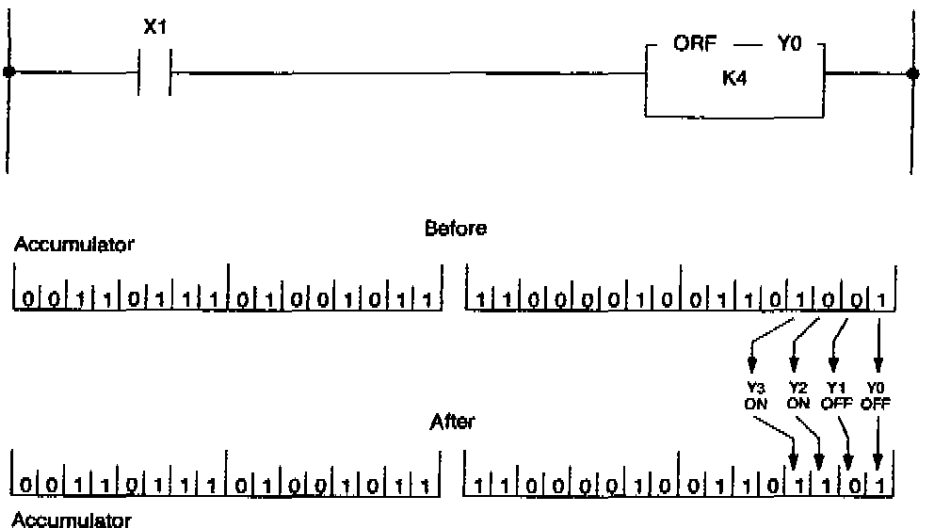


Valid Data Types:	First value	X, Y, C, S, T, CT, SP, and GX
	Second value	K (1–32)

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ORF (TI435 Only)

OR Accumulator with Image Register Range (ORF) ORs the contents of the accumulator with the indicated number of bits from the specified image register. The specified point is the least significant bit. The result is stored in the accumulator.



Key Sequence

STR | X/IMD | 1 | ENT

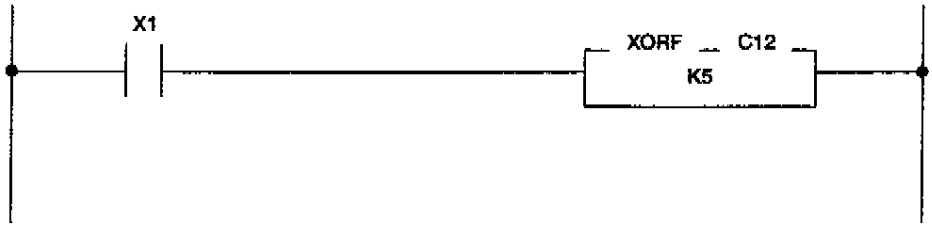
OR | SHFT | F | SHFT | Y/OUT | 0 | K/CONT | 4 | ENT

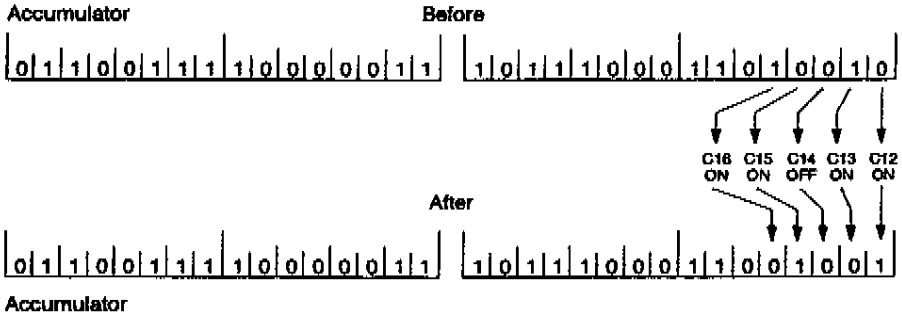
Valid Data Types:	First value	X, Y, C, S, T, CT, SP, and GX
	Second value	K (1–32)

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XORF (TI435 Only)

Exclusive OR Accumulator with Image Register Range (XORF) ORs the contents of the accumulator exclusively with the indicated number of bits from the specified image register. The specified point is the least significant bit. The result is stored in the accumulator.





Key Sequence



Valid Data Types:	First value	X, Y, C, S, T, CT, SP, and GX
	Second value	K (1–32)

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CMPF (TI435 Only)

Compare Accumulator with Image Register Range (CMPF) compares the contents of the accumulator with the indicated number of bits from the specified image register. The specified point is the least significant bit. The result is stored in the accumulator.



Accumulator	<	Image Register	:	SP60 is On
Accumulator	=	Image Register	:	SP61 is On
Accumulator	>	Image Register	:	SP62 is On

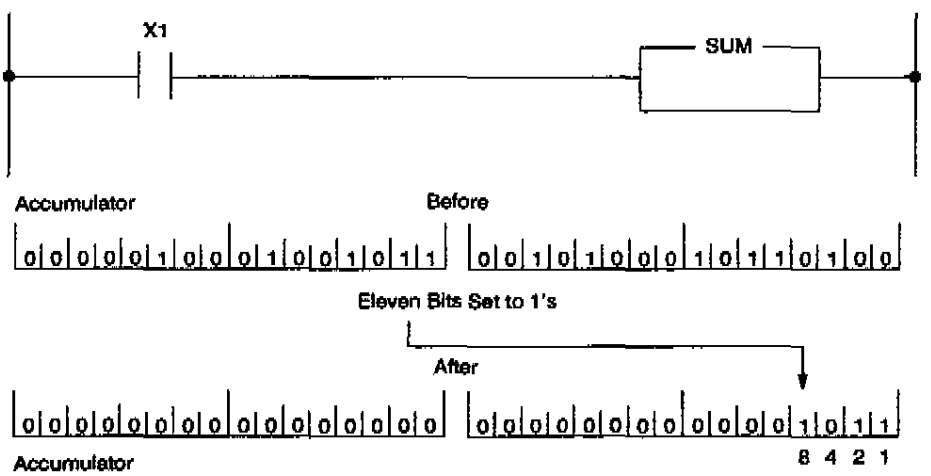
Key Sequence

STR | X(IN) | 1 | ENT
CMP | SHFT | F | SHFT | G(CR) | 4 | 0 | K(COM) | 3 | 2 | ENT

Valid Data Types: First value X, Y, C, S, T, CT, SP, and GX
Second value K (1–32)

SUM

Count One Bits in Accumulator (SUM) counts the number of bits set to ones in the 32-bit accumulator. The count is stored in the accumulator as a hexadecimal number.



Key Sequence

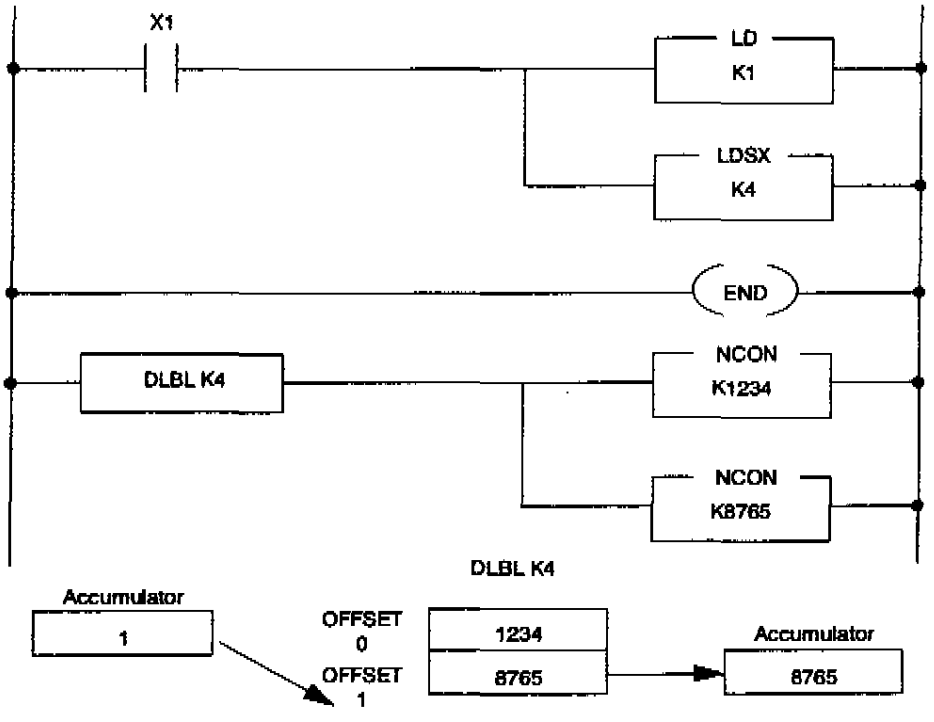
STR | X(IN) | 1 | ENT
SHFT | S | U | M | ENT

Valid Data Types: none

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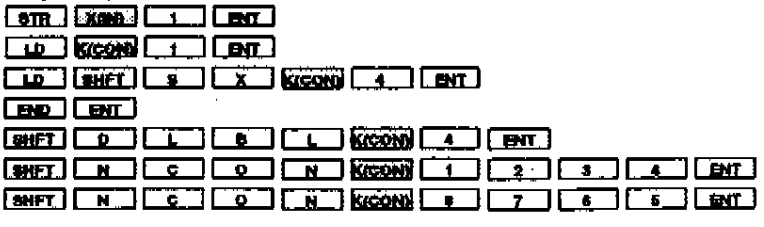
LDSX (TI435 Only)

Load Accumulator Indexed with Data Constants (LDSX) loads the accumulator with data from an ACON or NCON located at an offset from the specified data label. The desired offset must be loaded into the accumulator before the LDSX instruction is executed. In the example, LD K1 sets an offset of 1 into DLBL K4, specified by LDSX K4.



NOTE: The offset value must be a hexadecimal number.

Key Sequence



Valid Data Types: K (1–FFFF)

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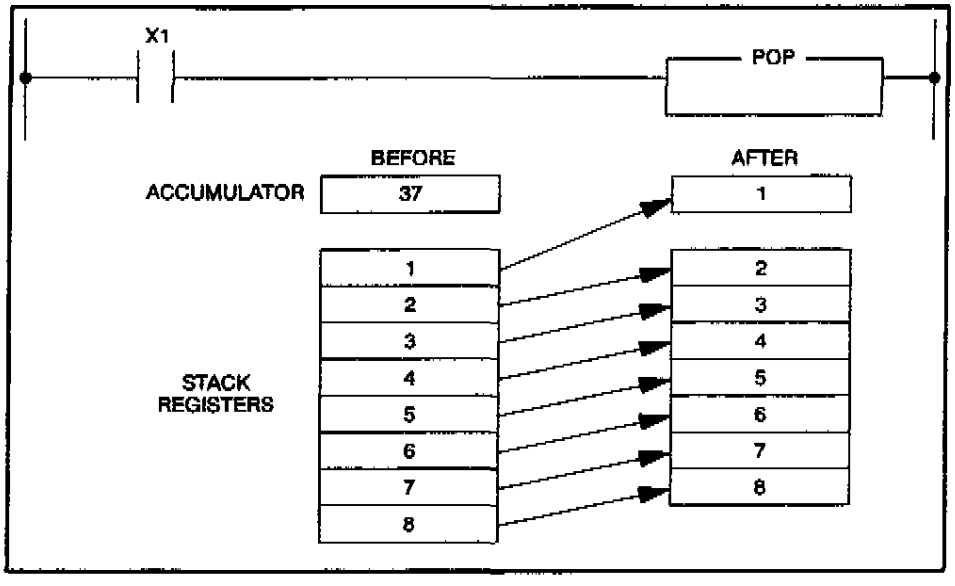
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POP

Load Accumulator from Top-of-Stack (POP) moves the value of each of the eight stack registers up one level. The value in the first register is popped into the accumulator, and any previous value in the accumulator is lost.



Key Sequence

STR | X000 | 1 | ENT
SHIFT | P | 0 | P | ENT

Valid Data Types: none

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ADDS

Add Top-of-Stack to Accumulator (ADDS) adds the value in the first stack register to the value in the accumulator. The result is stored in the accumulator. Flags SP63, SP66, SP67 and SP70 are set according to the result.



Key Sequence

STR	X(n)	1	ENT
ADD	SHIFT	8	ENT

Valid Data Types: none

SUBS

Subtract Top-of-Stack from Accumulator (SUBS) subtracts the value in the first stack register from the value in the accumulator. The result is stored in the accumulator. Flags SP63, SP64, SP65, and SP70 are set according to the result.



Key Sequence

STR	X(n)	1	ENT
SUB	SHIFT	8	ENT

Valid Data Types: none

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MULS

Multiply Accumulator by Top-of-Stack (MULS) multiplies a four-digit value in the accumulator by a four-digit value in the first stack register. The result is stored in the accumulator. Flags SP63 and SP70 are set according to the result.



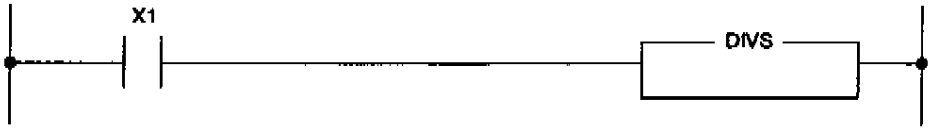
Key Sequence

STR	X(IN)	1	ENT
MUL	SHFT	S	ENT

Valid Data Types: none

DIVS

Divide Accumulator by Top-of-Stack (DIVS) divides the eight-digit value in the accumulator by a four-digit value in the first stack register. The result is stored in the accumulator and the remainder is stored in the first stack register. Flags SP53, SP63 and SP70 are set according to the result.



Key Sequence

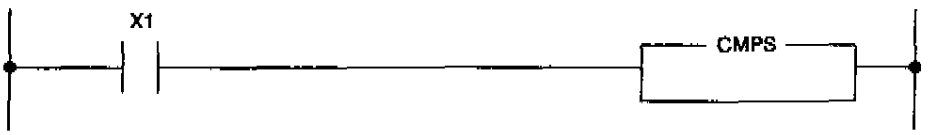
STR	X(IN)	1	ENT
DIV	SHFT	S	ENT

Valid Data Types: none

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CMPS

Compare Accumulator with Top-of-Stack (CMPS) compares the 32-bit value in the accumulator to the 32-bit value in the first stack register. Neither value is changed.



Accumulator	<	Stack Register	:	SP60 is On
Accumulator	=	Stack Register	:	SP61 is On
Accumulator	>	Stack Register	:	SP62 is On

Key Sequence

STR | XIO | 1 | ENT
CMP | SHIFT | 8 | ENT

Valid Data Types: none

INV

One's Complement Accumulator (INV) inverts each bit in the 32-bit accumulator and stores it back in the accumulator.



Key Sequence

STR | XIO | 1 | ENT
SHIFT | I | N | V | ENT

Valid Data Types: none

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BCDCPL

Ten's Complement Accumulator (BCDCPL) takes the 10's complement of the BCD value in the accumulator. The result is stored in the accumulator. The mathematical formula for this operation is:

```
  1 0000 0000
- 8-digit accumulator value
= 10's complement value
```



Key Sequence

STR | XIO | 1 | ENT
BCD | SHFT | C | P | L | ENT

Valid Data Types: none

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Stack Instructions

Overview

TI405 stack instructions use the accumulator stack. TI435 CPU firmware version 2.1 adds the following new stack instructions:

ADDBS	ADD Binary top-of-Stack to accumulator
SUBBS	SUBtract Binary top-of-Stack from accumulator
MULBS	MULtiply Binary accumulator by top-of-Stack
DIVBS	DIVide Binary accumulator by top-of-Stack
ANDS	AND accumulator with top-of-Stack
ORS	OR accumulator with top-of-Stack
XORS	eXclusive OR accumulator with top-of-Stack

Special Relays

Many special (SP) relays or flags exist in the TI405 CPUs. These are internal discrete points that are set and reset by the CPU depending on certain operating conditions.

The seven new stack instructions now available on the TI435 affect the SP flags shown in Table 15-1.

Table 15-1 Flags Affected by New Stack Instructions

Instruction	Flags Affected
ADDBS	SP63, SP66, SP67, SP70
SUBBS	SP63, SP64, SP65, SP70
MULBS	SP63, SP70
DIVBS	SP53, SP63, SP70
ANDS	SP63, SP70
ORS	SP63, SP70
XORS	SP63, SP70

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You can use these special (SP) relays as input contacts in your program to check for specific conditions. The following conditions are reported by the SPs listed in Table 15-1:

SP53 Arithmetic Error – on when the operand value is outside the allowable range; off otherwise. For example, this flag turns on when division by zero is attempted.

SP63 Zero – on when all 32 bits of the accumulator are zero; off otherwise.

SP64 Half borrow – on when 16-bit subtraction results in a borrow because the lower 16 bits of the operand (stack register 1 in this case) are greater than the lower 16 bits of the accumulator; off otherwise.

SP65 Borrow – on when 32-bit subtraction results in a borrow because the 32 bits of the operand (stack register 1 in this case) are greater than the 32 bits of the accumulator; off otherwise.

SP66 Half carry – on when 16-bit addition results in a carry because the sum is greater than can be displayed in 16 bits; off otherwise.

SP67 Carry – on when 32-bit addition results in a carry because the sum is greater than can be displayed in 32 bits; off otherwise.

SP70 Sign – on when the most significant bit of the 32-bit accumulator is on; off otherwise.

The state of each SP listed above can be altered by each instruction that affects that SP. Thus, the state of each SP may change several times during a single program scan. If you use these SPs in your program, be sure to place them immediately following the appropriate instruction to be sure the correct check is performed.

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For example, the program of Figure 15-1 checks a divide instruction to be sure the operand value is within range.

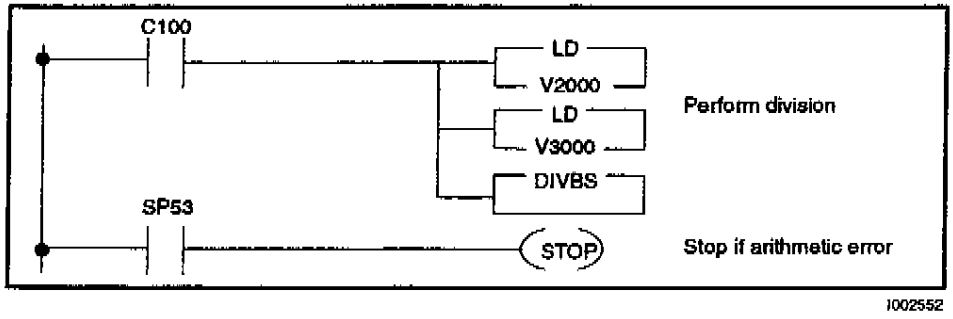


Figure 15-1 SP Example

ADDBS (TI435 only)

ADD Binary Top-of-Stack to Accumulator (ADDBS) adds the value in the first stack register to the value in the accumulator. The result is stored in the accumulator. The contents of the first stack register are popped away. Flags SP63, SP66, SP67, and SP70 are set according to the result. ADDBS is a 32-bit operation. See Figure 15-2.

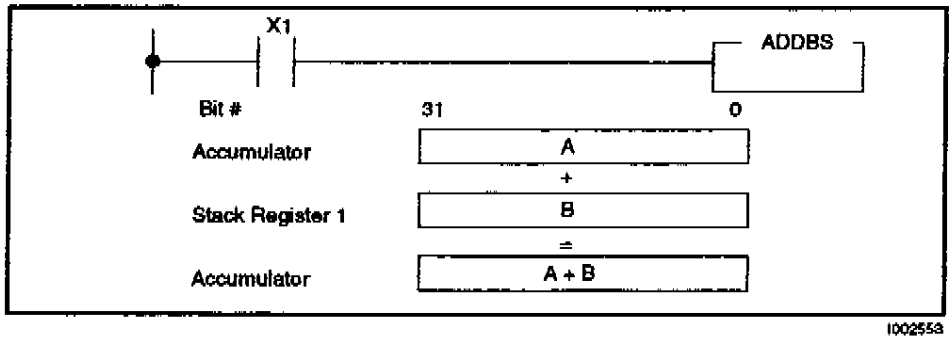


Figure 15-2 ADD Binary Top-of-Stack to Accumulator (ADDBS)

MIU Key Sequence:

STR	X(IN)	1	ENT
ADD	SHIFT	B	B	ENT

Valid Data Types: none

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SUBBS (TI435 only)

SUBtract Binary Top-of-Stack from Accumulator (SUBBS) subtracts the value in the first stack register from the value in the accumulator. The result is stored in the accumulator. The contents of the first stack register are popped away. Flags SP63, SP64, SP65, and SP70 are set according to the result. SUBBS is a 32-bit operation. See Figure 15-3.

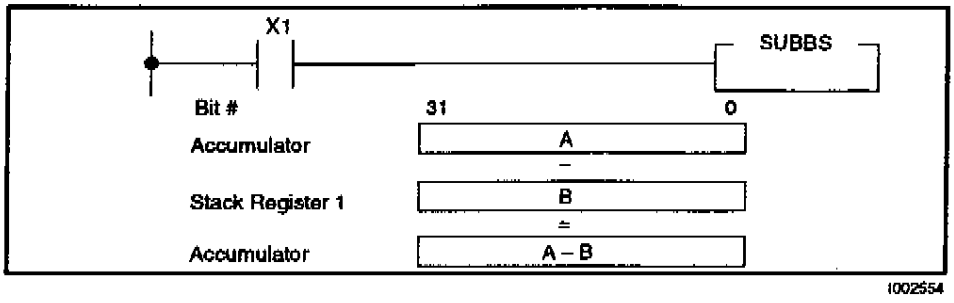


Figure 15-3 SUBtract Binary Top-of-Stack from Accumulator (SUBBS)

MIU Key Sequence:

STR | X (AND) | 1 | ENT
SUB | SHIFT | B | S | ENT

Valid Data Types: none

MULBS (TI435 only)

Multiply Binary Accumulator by Top-of-Stack (MULBS) multiplies a 16-bit (4-digit) value in the accumulator by a 16-bit (4-digit) value in the first stack register. The 32-bit result is stored in the accumulator. The contents of the first stack register are popped away. Flags SP63 and SP70 are set according to the result. See Figure 15-4.

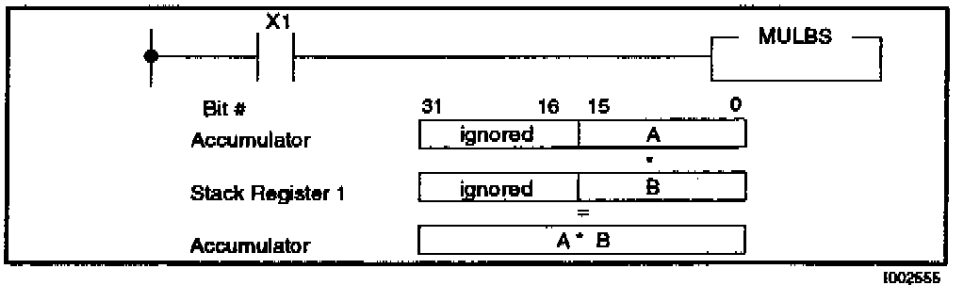


Figure 15-4 Multiply Binary Accumulator by Top-of-Stack (MULBS)

MIU Key Sequence:

STR | X (AND) | 1 | ENT
MUL | SHIFT | B | S | ENT

Valid Data Types: none

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DIVBS (TI435 only)

Divide Binary Accumulator by Top-of-Stack (DIVBS) divides the 32-bit (8-digit) value in the accumulator by a 16-bit (4-digit) value in the first stack register. The 32-bit result is stored in the accumulator, and the remainder is stored in the first stack register. Flags SP53, SP63, and SP70 are set according to the result. See Figure 15-5.

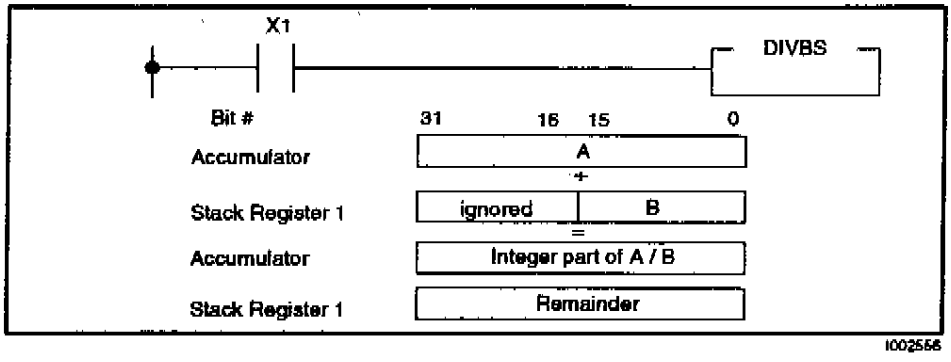


Figure 15-5 Divide Binary Accumulator by Top-of-Stack (DIVBS)

MIU Key Sequence:

STR | X(##) | 1 | ENT
DIV | SHIFT | B | 0 | ENT

Valid Data Types: none

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ANDS (TI435 only)

AND Accumulator with Top-of-Stack (ANDS) performs a logical AND between the contents of the accumulator and the contents of the first stack register. The result is stored in the accumulator. The contents of the first stack register are popped away. Flags SP63 and SP70 are set according to the result. ANDS is a 32-bit operation. See Figure 15-6.

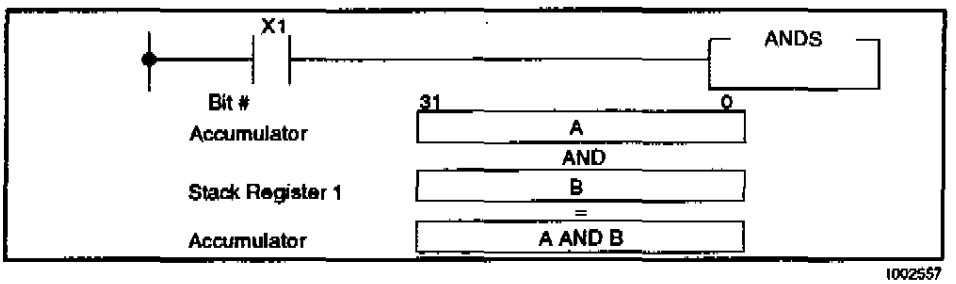


Figure 15-6 AND Accumulator with Top-of-Stack (ANDS)

MIU Key Sequence:

STR | X(IN) | 1 | ENT
AND | SHIFT | 9 | ENT

Valid Data Types: none

ORS (TI435 only)

OR Accumulator with Top-of-Stack (ORS) performs a logical OR between the contents of the accumulator and the contents of the first stack register. The result is stored in the accumulator. The contents of the first stack register are popped away. Flags SP63 and SP70 are set according to the result. ORS is a 32-bit operation. See Figure 15-7.

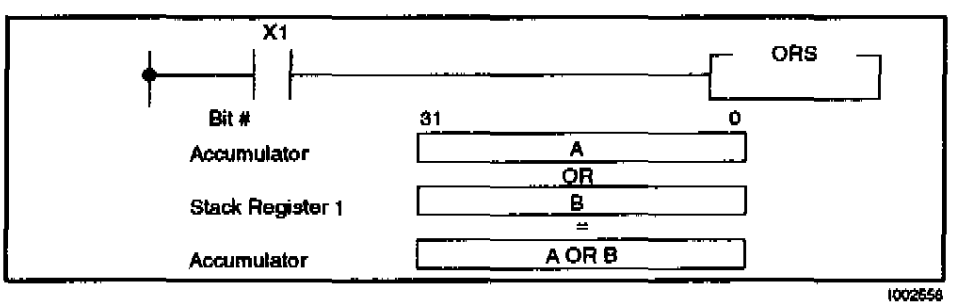


Figure 15-7 OR Accumulator with Top-of-Stack (ORS)

MIU Key Sequence:

STR | X(IN) | 1 | ENT
OR | SHIFT | 9 | ENT

Valid Data Types: none

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XORS (TI435 only)

Exclusive OR Accumulator with Top-of-Stack (XORS) performs a logical exclusive OR between the contents of the accumulator and the contents of the first stack register. The result is stored in the accumulator. The contents of the first stack register are popped away. Flags SP63 and SP70 are set according to the result. XORS is a 32-bit operation. See Figure 15-8.

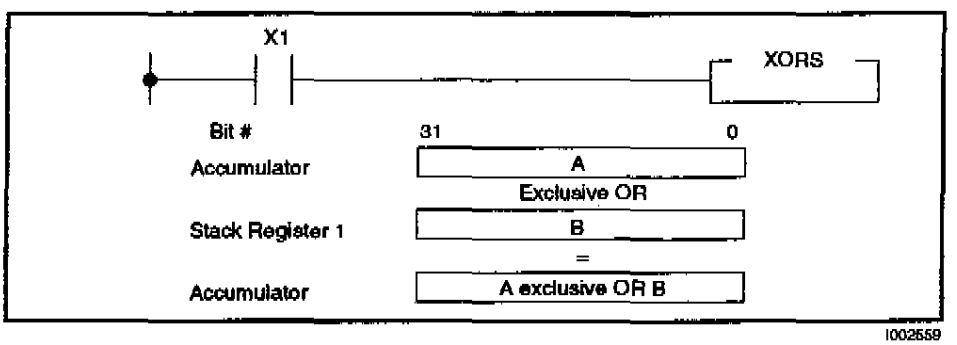


Figure 15-8 Exclusive OR Accumulator with Top-of-Stack (XORS)

MIU Key Sequence:

STR | X (AND) | 1 | ENT

SHFT | X | 9 | R | 9 | ENT

Valid Data Types: none

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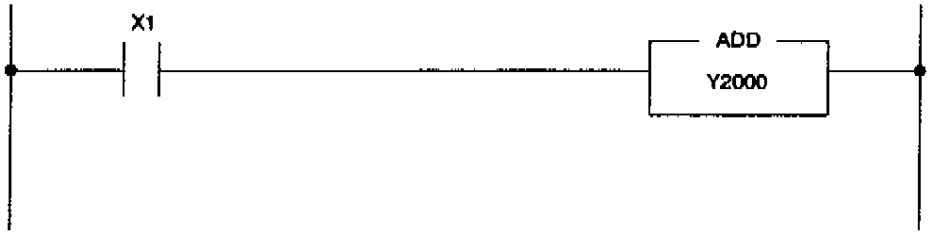
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BCD Instructions

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ADD

Add BCD (ADD) adds a four-digit value from a V-memory location to the value in the accumulator and stores the results in the accumulator. Flags SP63, SP66, SP67, SP70, and SP75 are set according to the result.



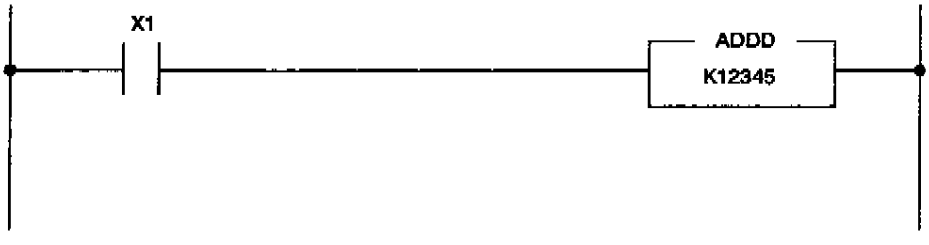
Key Sequence



Valid Data Types: V

ADDD

Add BCD Eight-digit Value (ADDD) adds an eight-digit constant value, or the value from two consecutive V-memory locations, to the accumulator. It stores the results in the accumulator. If a V data type is used, the lower four digits of the number come from the specified V location and the upper four digits from the next higher V location. Flags SP63, SP66, SP67, SP70, and SP75 are set according to the result.



Key Sequence

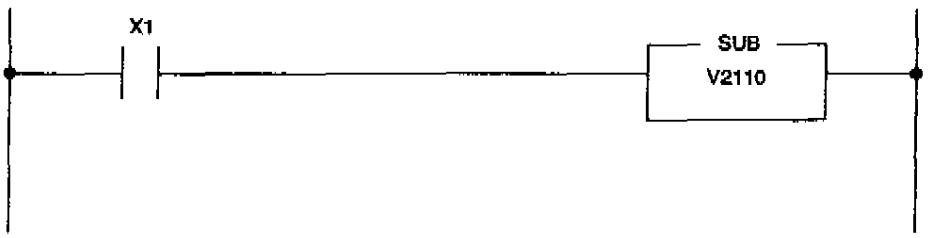


Valid Data Types: V and K

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SUB

Subtract BCD (SUB) subtracts a four-digit value in a V-memory location from the value in the accumulator. It stores the result in the accumulator. Flags SP63, SP64, SP65, SP70, and SP75 are set according to the final result.



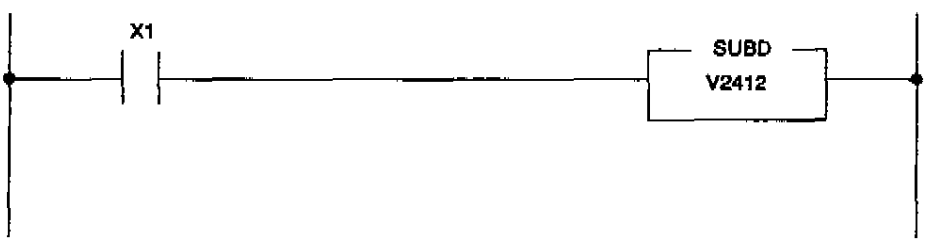
Key Sequence



Valid Data Types: V

SUBD

Subtract BCD Eight-digit Value (SUBD) subtracts an eight-digit constant value, or the value from two consecutive V-memory locations, from the accumulator. If a V data type is used, the lower four digits of the number come from the specified V location, and the upper four digits from the next higher V location. Flags SP63, SP64, SP65, SP70, and SP75 are set according to the result.



Key Sequence



Valid Data Types: V and K

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MUL

Multiply BCD (MUL) multiplies the value in the accumulator by a four-digit value from a V-memory location, or a four-digit constant. It stores the result in the accumulator. Flags SP63, SP70, and SP75 are set according to the result.



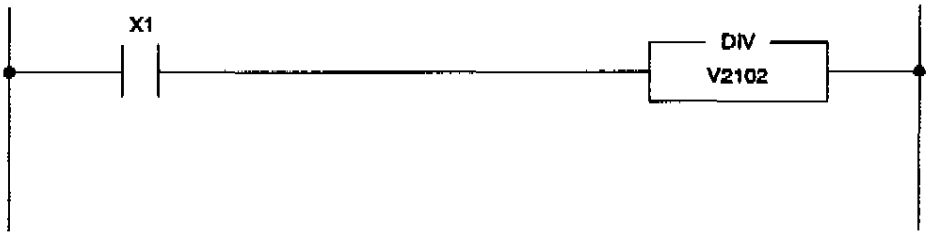
Key Sequence



Valid Data Types: V and K

DIV

Divide BCD (DIV) divides the value in the accumulator by a four-digit value from a V-memory location, or by a four-digit constant. It stores the result in the accumulator. Flags SP53, SP63, SP70, and SP75 are set according to the result.



Key Sequence

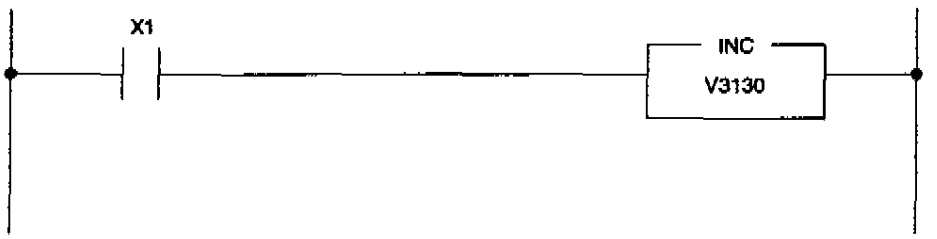


Valid Data Types: V and K

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INC

Increment BCD (INC) adds 1 to the binary coded decimal value in the specified V-memory location. Flag SP63 is set if the location is incremented to zero. Flag SP75 is set if the value is not a BCD number.



Key Sequence



Valid Data Types: V

DEC

Decrement BCD (DEC) subtracts 1 from the binary coded decimal value in the specified V-memory location. Flag SP63 is set if the location is decremented to zero. Flag SP75 is set if the value is not a BCD number.



Key Sequence



Valid Data Types: V

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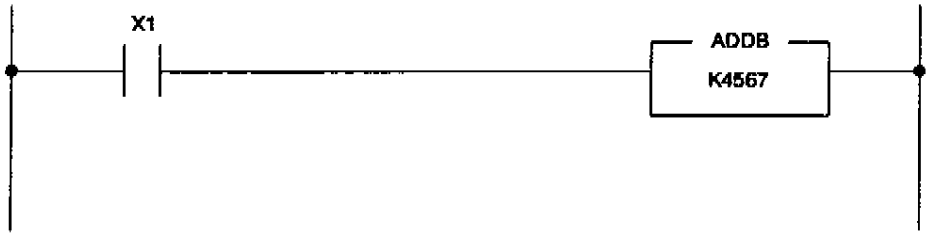
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Binary Instructions

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MULB 17-4
DIVB 17-4
INCB 17-5
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ADDB

ADD Binary Word (ADDB) adds a 16-bit binary value from a V-memory location, or a 16-bit constant, to the value in the accumulator. The result is stored in the accumulator. Flags SP63, SP66, SP67, SP70 and SP73 are set according to the result.



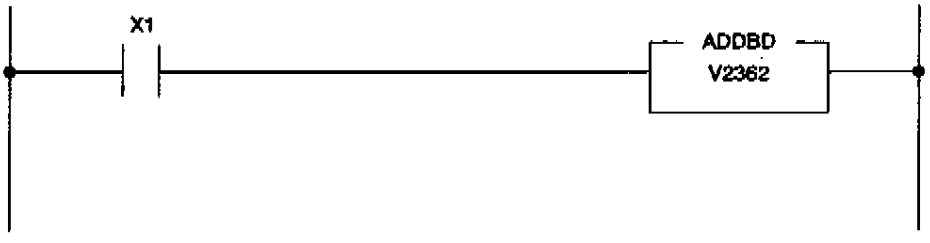
Key Sequence

STR | X/CNO | 1 | ENT
ADD | SHIFT | B | SHIFT | K/CONS | 4 | 5 | 6 | 7 | ENT

Valid Data Types: V and K

ADDBD (TI435 Only)

ADD Binary Double Word (ADDBD) adds a 32-bit binary constant value, or the value from two consecutive V-memory locations, to the accumulator. The result is stored in the accumulator. If a V data type is used, the lower 16-bits come from the specified V location, and the upper 16-bits from the next higher V location. Flags SP63, SP66, SP67, SP70 and SP73 are set according to the result.



Key Sequence

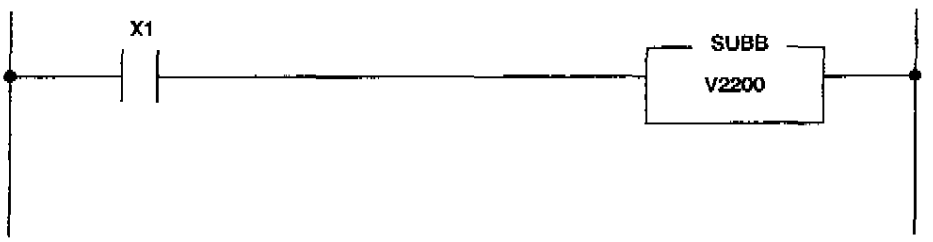
STR | X/CNO | 1 | ENT
ADD | SHIFT | B | D | SHIFT | V | 2 | 3 | 6 | 2 | ENT

Valid Data Types: V and K

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SUBB

Subtract Binary Word (SUBB) subtracts a 16-bit binary constant value, or a 16-bit value from a V-memory location, from the value in the accumulator. The result is stored in the accumulator. Flags SP63, SP64, SP65, and SP70 are set according to the final result.



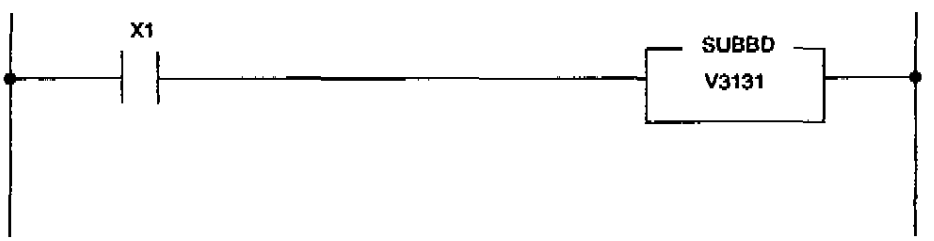
Key Sequence



Valid Data Types: V and K

SUBBD (TI435 Only)

Subtract Binary Double Word (SUBBD) subtracts a 32-bit binary constant value, or the binary value from two consecutive V-memory locations, from the accumulator. If a V data type is used, the lower 16-bits come from the specified V location, and the upper 16-bits from the next higher V location. Flags SP63, SP64, SP65, and SP70 are set according to the result.



Key Sequence

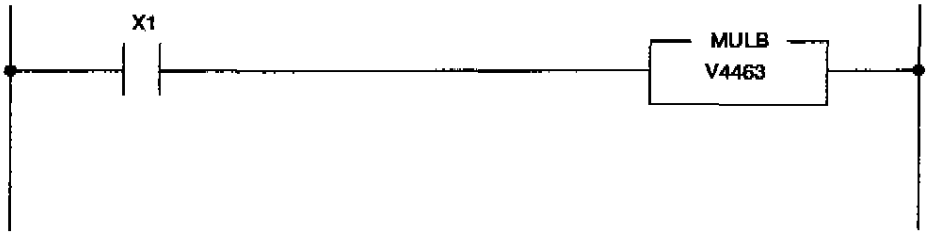


Valid Data Types: V and K

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MULB

Multiply Binary Word (MULB) multiplies the value in the accumulator by a 16-bit binary value from a V-memory location, or a 16-bit constant. The result is stored in the accumulator. Flags SP63 and SP70 are set according to the result.



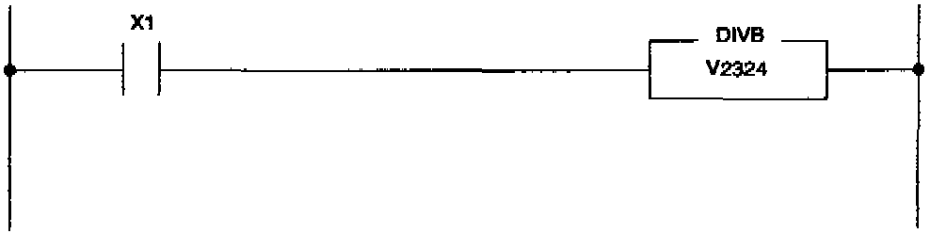
Key Sequence



Valid Data Types: V and K

DIVB

Divide Binary Word (DIVB) divides the value in the accumulator by a 16-bit binary value from a V-memory location, or by a 16-bit binary constant. The result is stored in the accumulator. Flags SP53, SP63, and SP70 are set according to the result.



Key Sequence



Valid Data Types: V and K

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INCB

Increment Binary (INCB) adds 1 to the binary value in the specified V-memory location. Flag SP63 is set if the location is incremented to zero.



Key Sequence



Valid Data Types: V

DECB

Decrement Binary (DECB) subtracts 1 from the binary value in the specified V-memory location. Flag SP63 is set if the location is decremented to zero.



Key Sequence



Valid Data Types: V

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Chapter 18

Encoding and Decoding Instructions

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ATH 18-6
HTA (TI435 Only) 18-8

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BIN

Convert BCD to Binary (BIN) converts the contents of the accumulator to a binary value from an eight digit, binary-coded, decimal value. Flag SP75 is set if the value is not a BCD number.



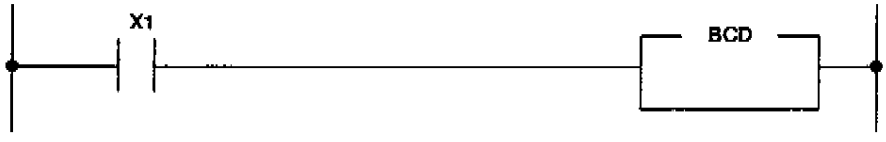
Key Sequence

STR | X(00) | 1 | ENT
BIN | ENT

Valid Data Types: none

BCD

Convert Binary to BCD (BCD) converts the binary value in the accumulator into an eight digit, binary-coded, decimal value. Flags SP63 and SP70 are set according to the result.



Key Sequence

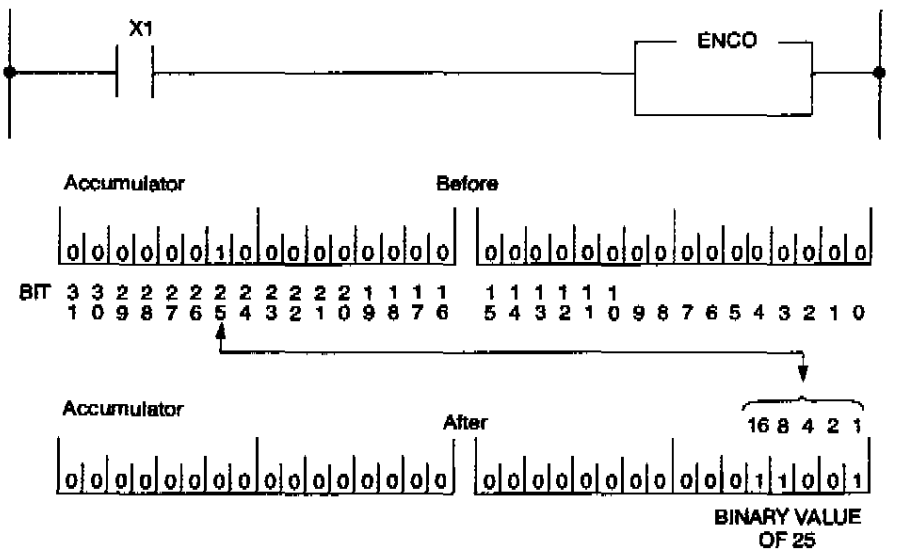
STR | X(00) | 1 | ENT
BCD | ENT

Valid Data Types: none

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ENCO

Encode (ENCO) returns to the accumulator a five-bit binary number indicating the bit position of the bit that was set to a one. If the original contents of the accumulator is either 0000 0001, or 0000 0000, a value of 0 is returned. If more than one bit is on, SP53 is set and the position of the rightmost on bit is returned.



Key Sequence



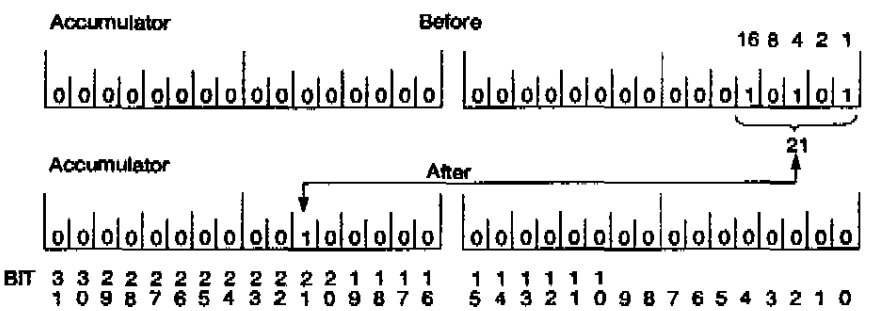
Valid Data Types: none

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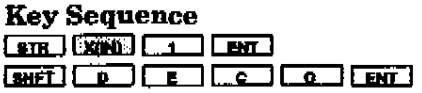
DECO

Decode (DECO) takes a five-bit binary number (0–31) from the accumulator and sets the corresponding bit position to a one. If the original number in the accumulator is larger than 31, the number is divided by 32 until it is less than 32, then the remainder is encoded.





Key Sequence

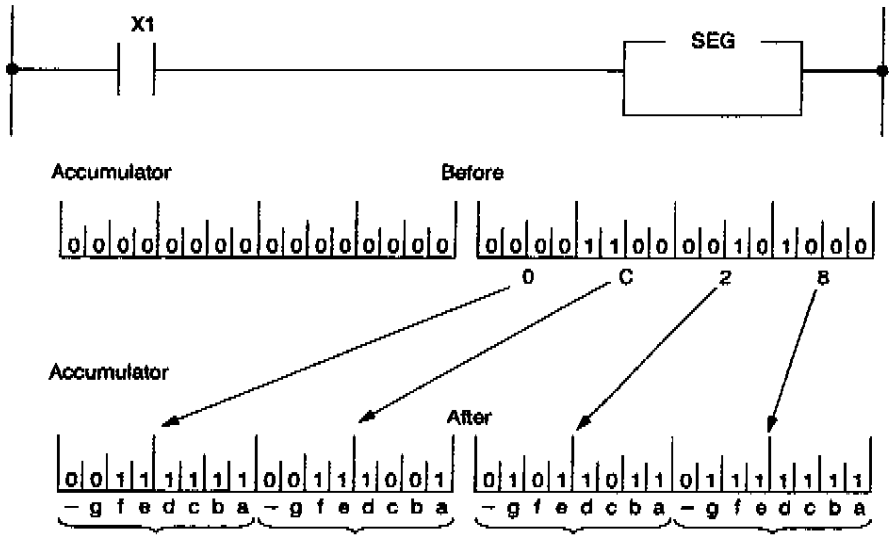


Valid Data Types: none

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SEG

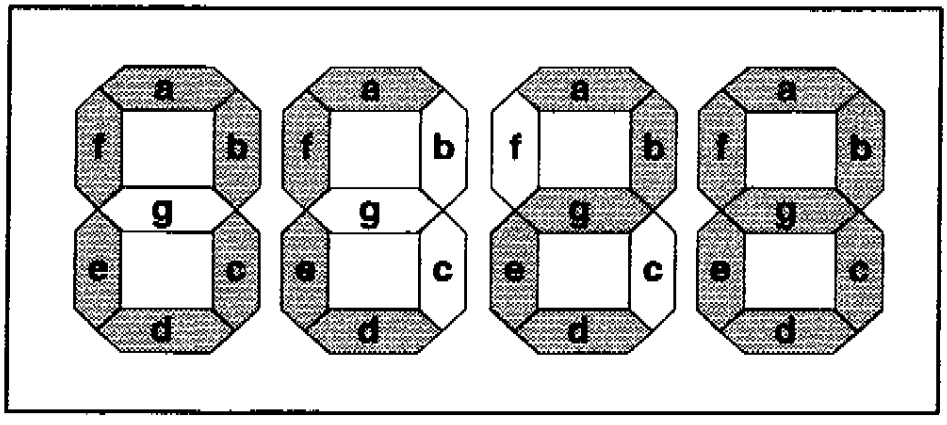
Convert to Seven-segment Display (SEG) converts a four-digit hexadecimal number in the accumulator into the 32-bit pattern required to produce those numbers on seven segment displays.



Key Sequence

STR	X(IN)	1	ENT	
SHIFT	S	E	G	ENT

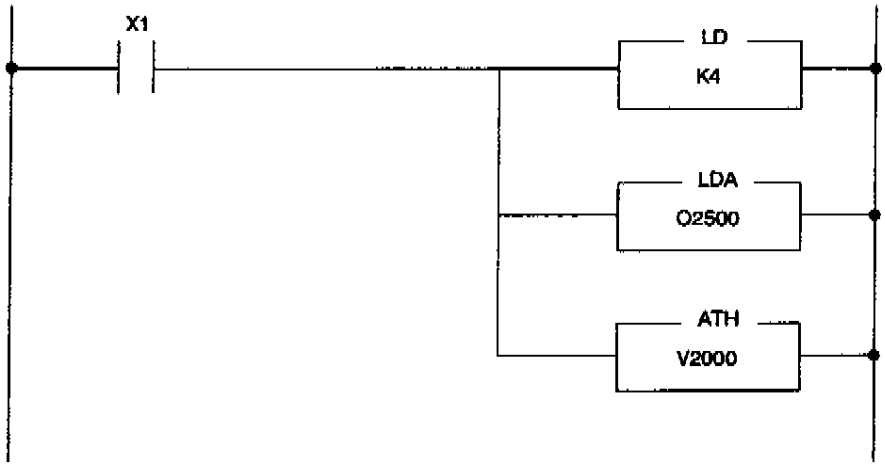
Valid Data Types: none



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ATH

Convert ASCII to Hexadecimal (ATH) converts a table of ASCII values to hexadecimal numbers. The number of V-memory locations occupied by the ASCII table must be in the first stack register, and the V-memory starting address of the ASCII table must be in the accumulator. The V-memory address used with the ATH instruction is the starting address of the hex table. Since eight bits of memory are required to store each ASCII character and only four bits are needed for each hex number, the hex table is half as long as the ASCII table. In the example, LD K4 sets the length of the ASCII table, and LDA O2500 indicates that the ASCII table starts at location V2500.



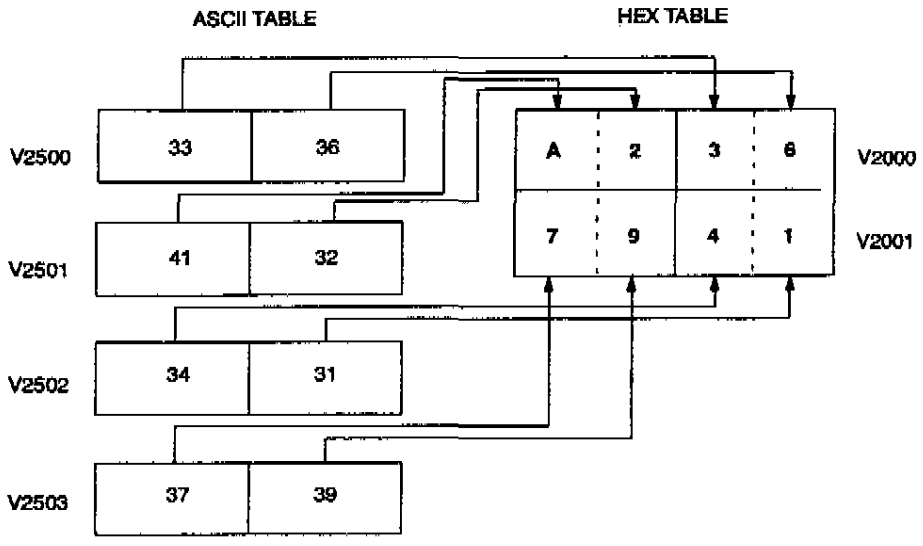
Key Sequence



Valid Data Types: V

NOTE: The ASCII table length must be a hexadecimal number.

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The ATH instruction will correctly convert only the ASCII values listed in Table 18-1.

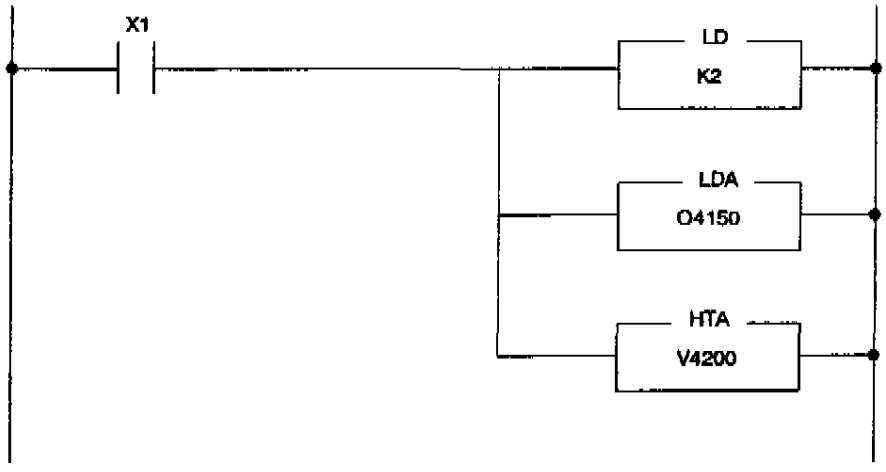
Table 18-1 Valid ASCII Values for ATH Conversion

ASCII Character	ASCII Hex Value	Converted Hex Digit
0	30	0
1	31	1
2	32	2
3	33	3
4	34	4
5	35	5
6	36	6
7	37	7
8	38	8
9	39	9
A	41	A
B	42	B
C	43	C
D	44	D
E	45	E
F	46	F

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HTA (TI435 Only)

Convert Hexadecimal to ASCII (HTA) converts a table of hexadecimal numbers to ASCII values. The number of V-memory locations occupied by the hex table must be in the first stack register, and the V-memory starting address of the hex table must be in the accumulator. The V-memory address used with the HTA instruction is the starting address of the ASCII table. Since only four bits of memory are required to store a hex number, but eight bits are required to store each ASCII character, the ASCII table is twice as long as the hex table. In the example, LD K2 sets the length of the hex table as two V-memory locations, and LDA O4150 indicates that the hex table starts at location V4150.



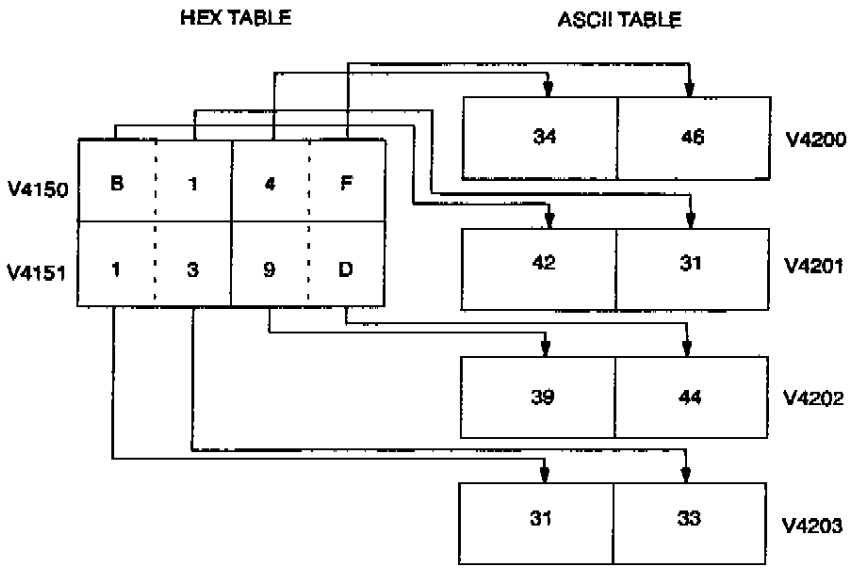
Key Sequence



Valid Data Types: V

NOTE: The table length must be a hexadecimal number.

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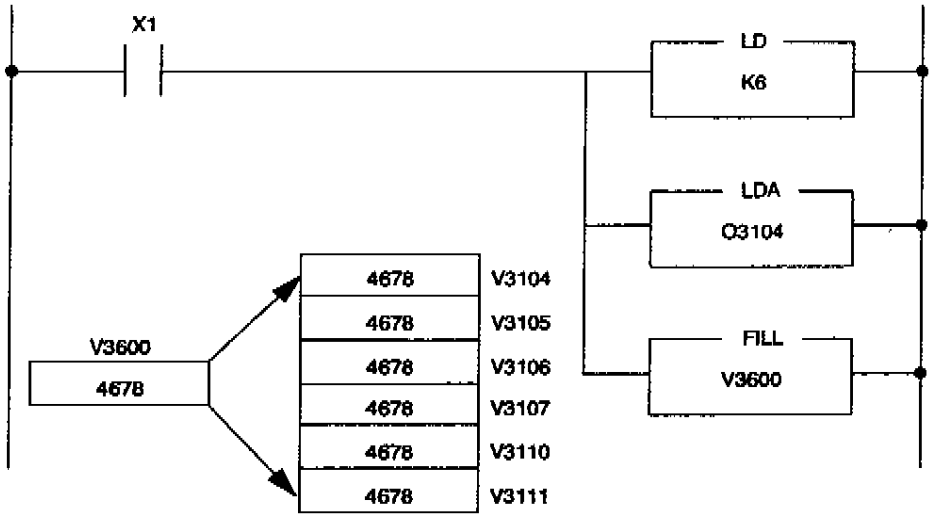
Chapter 19
Table Instructions

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FILL

Fill V-memory Table (FILL) fills a range of V-memory locations with a value. The first stack register must contain the number of consecutive V-memory locations to be filled. The accumulator must contain the V-memory address of the beginning of the range to be filled. If the fill instruction is used with a K data type, the range is filled with that constant. If used with a V data type, the range is filled with the contents of that V location. In the example, the LD K6 specifies a range length of 6. The LDA O3104 specifies that the range starts at V3104.



Key Sequence



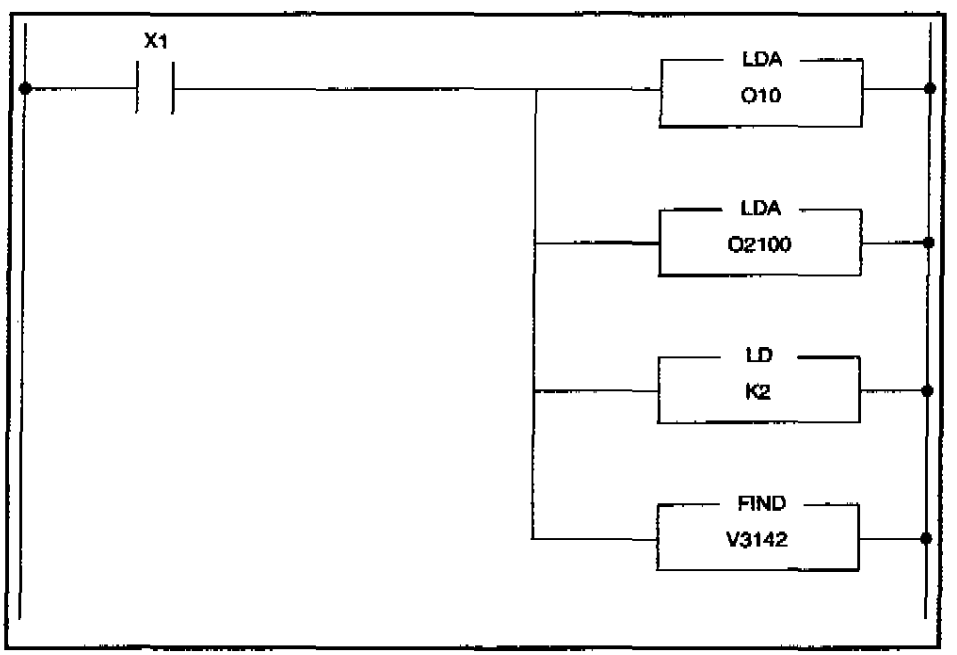
Valid Data Types: V and K

NOTE: The number of locations to be filled value must be a hexadecimal number.

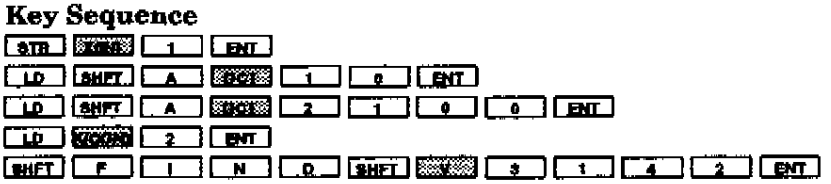
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FIND (TI435 Only)

Find Value (FIND) searches for a value in a block of V-memory. The second stack register must contain the length in octal of the block to be searched. The first stack register must contain the starting V-memory address of the block. The accumulator must contain the offset into the block from which the search is started. The offset to the first memory location that matches the find data is returned in the accumulator. If the FIND instruction is used with a K data type, that constant is used as the search value. If used with a V data type, the contents of that V-memory location is used as the search value. In the example, LDA O10 sets the length of the block as 10 (octal). LDA O2100 indicates that the search block starts at V2100. LD K2 specifies an offset of 2, so the actual search starts at memory location V2102. The value to search for is found in V3142. Flag SP53 is set if the value is not found.



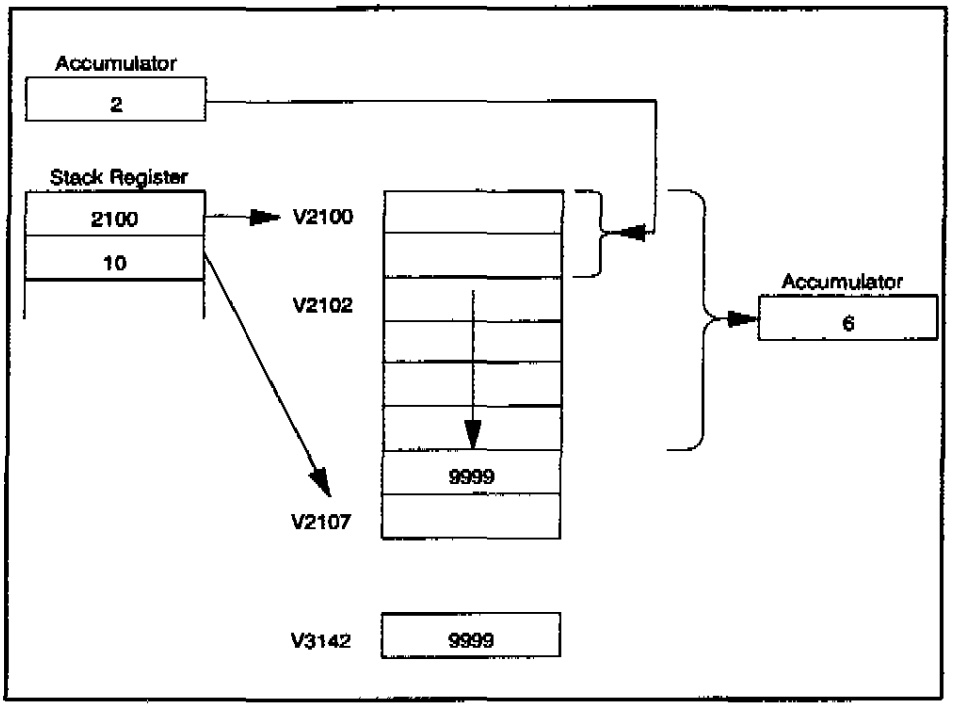
Key Sequence



Valid Data Types: V and K

NOTE: The offset for the start search must be a hexadecimal number.

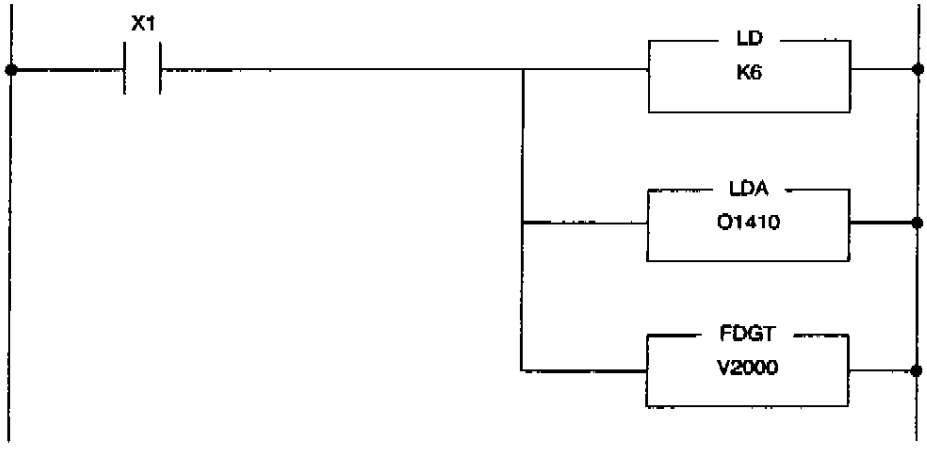
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FDGT (TI435 Only)

Find Greater Than (FDGT) searches a block of V-memory for the first value greater than the search value. The first stack register must contain the length of the block to be searched. The accumulator must contain the starting V-memory address of the block. The offset to the first memory location whose value equals or exceeds the search value is returned in the accumulator. If the FDGT is used with a K data type, that constant is used as the search value. If used with a V data type, the contents of that V-memory location is used as the search value. In the example, LD K6 sets the length of the block as 6 V-memory locations. LDA O1410 indicates that the search block starts at V1410. The search value is found in V2000.



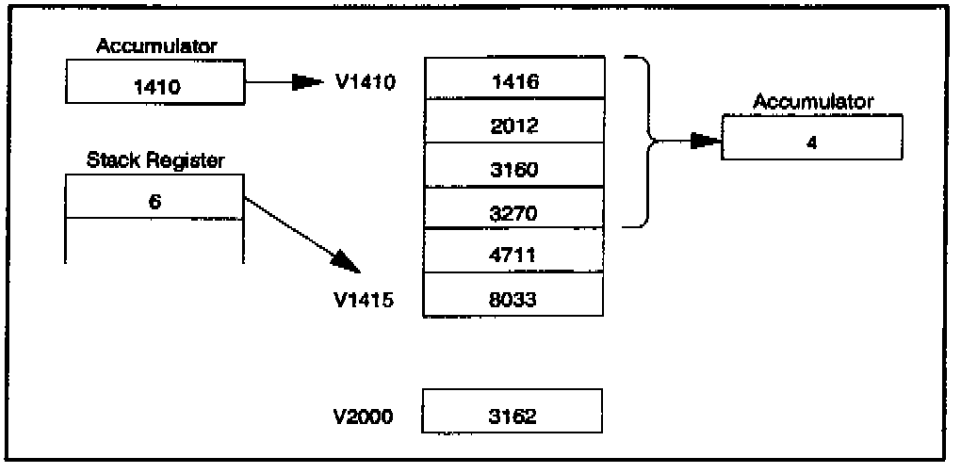
Key Sequence



Valid Data Types: V and K

NOTE: The block length parameter must be a hexadecimal number.

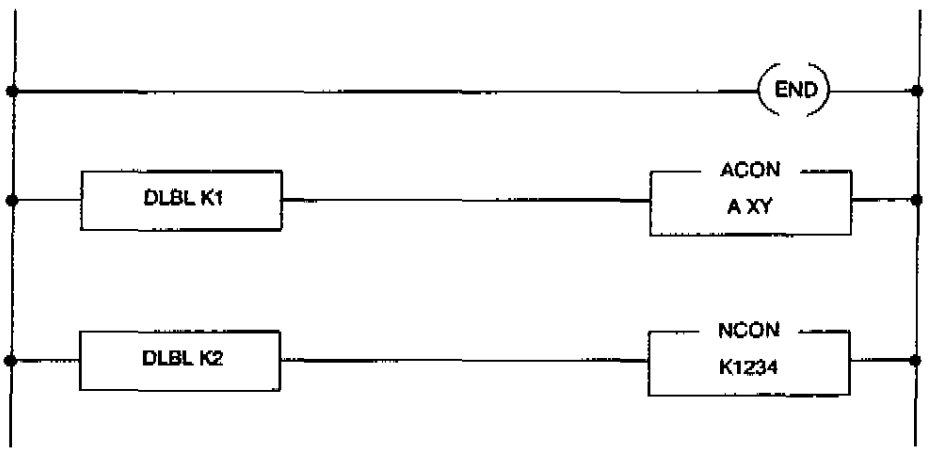
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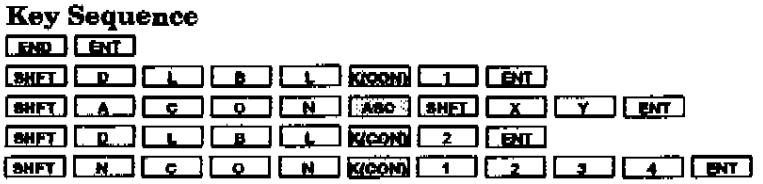
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DLBL (TI435 Only)

Data Label (DLBL) instructions are located after the end instruction and mark the start of either an ASCII or numeric data table. Up to 64 DLBL instructions may be used.



Key Sequence



Valid Data Types: K (1--FFFF)

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NCON (TI435 Only)

Numeric Constant (NCON) is a numeric constant used with the DLBL instruction to store tables of numeric data. Up to four digits can be stored with each NCON instruction. Multiple NCON instructions may be used with one DLBL.

Valid Data Types: K (0–FFFF)

ACON (TI435 Only)

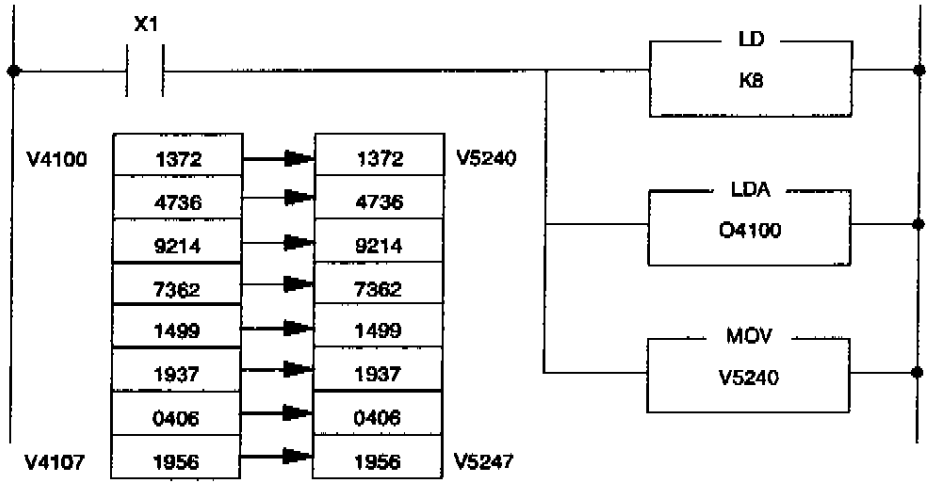
ASCII Constant (ACON) is an ASCII constant used with the DLBL instruction to store tables of ASCII data. Either one or two characters can be stored with each ACON instruction. If only one character is stored, a blank space is inserted in front of that character. Multiple ACON instructions may be used with one DLBL.

Valid Data Types: A (A–Z, 0–9)

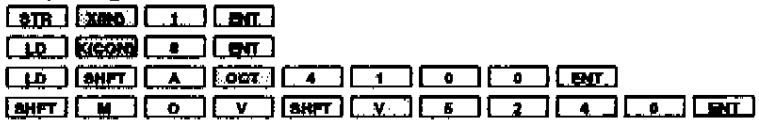
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MOV (TI435 Only)

Move Table (MOV) moves a table of 16-bit words. The first stack register specifies the table length. The accumulator holds the table source address. The MOV instruction provides the destination address. The example moves eight words starting at V4100 to a table starting at V5240.



Key Sequence



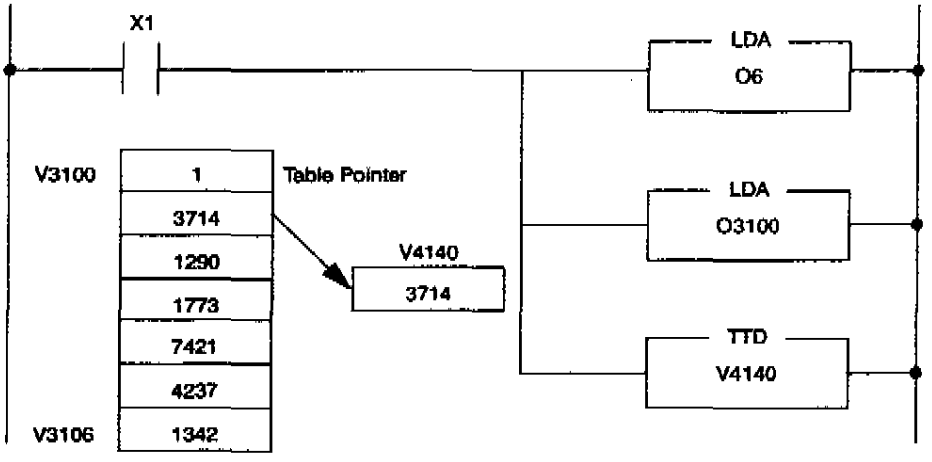
Valid Data Types: V

NOTE: The table length parameter must be a hexadecimal number.

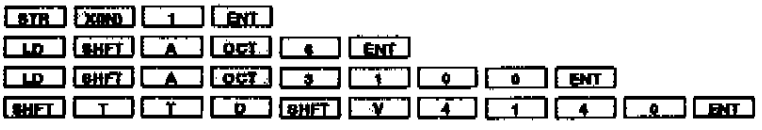
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TTD (TI435 Only)

Table to Destination (TTD) moves a value from a table to a V-memory location, and increments the table pointer. A move and increment occur during each scan for as long as the associated input is on. When the pointer reaches the end of the table, it resets to the first position. The first stack register holds the table length. The accumulator specifies the starting address of the table. The TTD instruction provides the destination address. The first location of the table is used to store the table pointer, that is the offset into the table of the next entry to be moved. The example sets a table with six data words. The table pointer is located at address V3100. The data words are each moved in turn to V4140. When the table pointer equals the table size, flag SP56 is set.



Key Sequence

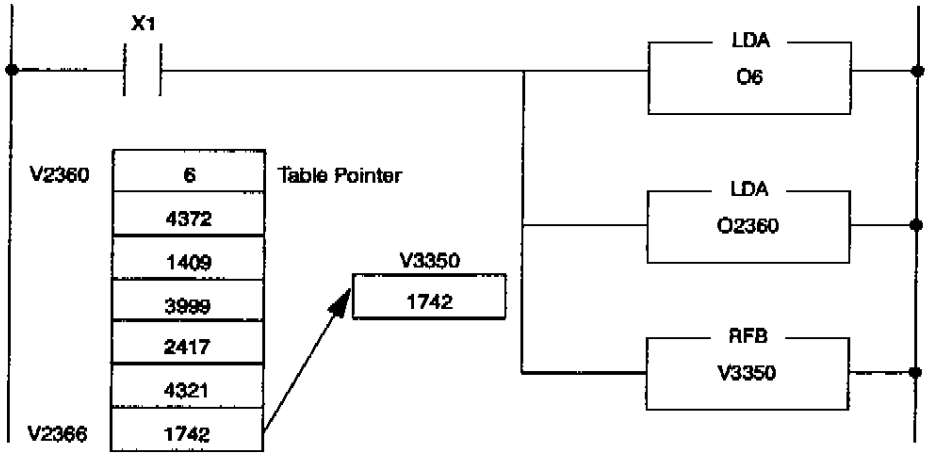


Valid Data Types: V

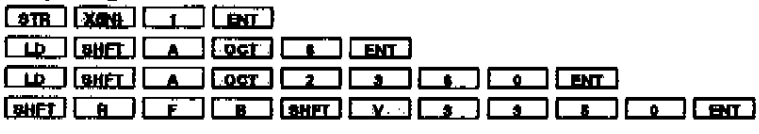
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RFB (TI435 Only)

Remove from Bottom (RFB) moves a value from a table to a V-memory location, and decrements the table pointer. A move and decrement occur during each scan for as long as the associated input is on. Operation stops when the table pointer decrements to zero. The first stack register holds the table length. The accumulator specifies the starting address of the table. The first location of the table is used to store the table pointer, that is the offset into the table of the next entry to be moved. The example sets a table with six data words. The table pointer is located at address V2360. The data words are each moved in turn to V3350. Flag SP56 is set when the table pointer is zero.



Key Sequence

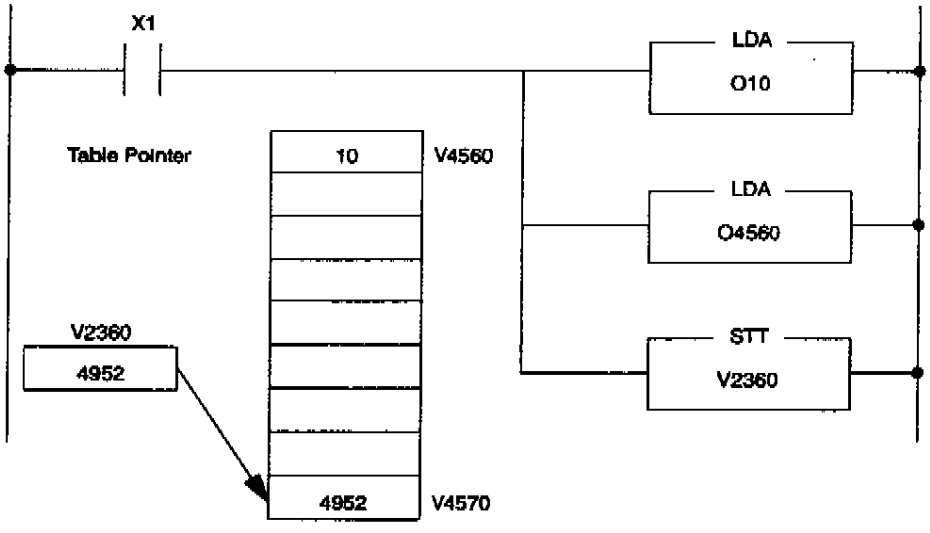


Valid Data Types: V

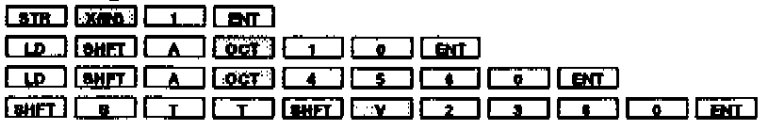
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STT (TI435 Only)

Source to Table (STT) moves a value from a V-memory location to a table and increments the table pointer. A move and increment occur during each scan for as long as the associated input is on. When the pointer reaches the end of the table, it resets to the first position. The first stack register holds the table length. The accumulator specifies the starting address of the table. The STT instruction provides the source address. The first location of the table is used to store the table pointer, that is the offset into the table of the next entry to be written to. The example sets a table with eight data locations. The table pointer is located at address V4560. The data words are moved from location V2360. When the table pointer equals the table size, flag SP56 is set.



Key Sequence

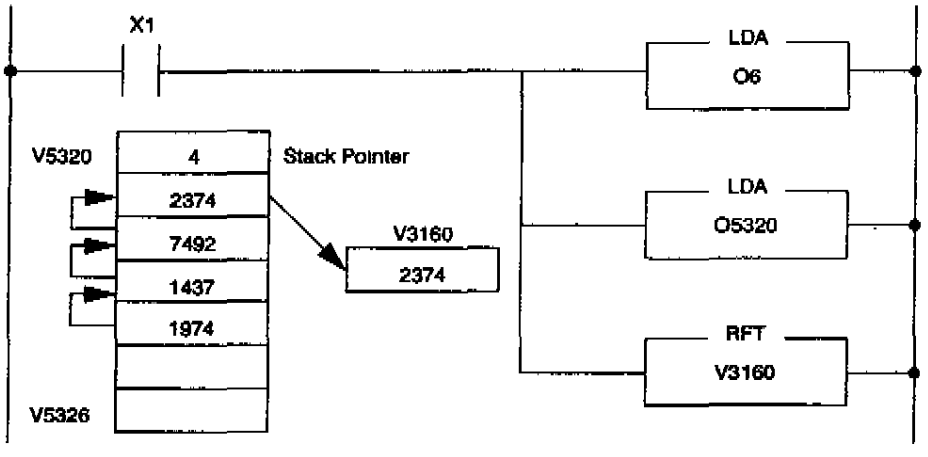


Valid Data Types: V and K

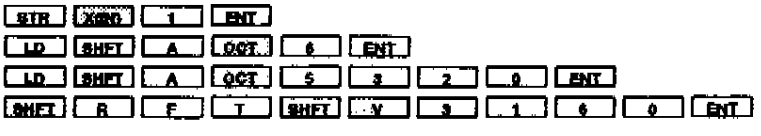
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RFT (TI435 Only)

Remove from Table (RFT) pops a value from a user-defined stack, and stores it in a V-memory location. The first stack register specifies the maximum length of the stack. The accumulator specifies the stack starting address, that is occupied by the stack pointer. The stack pointer contains the current number of values on the stack. If the stack length is zero, operation stops. The example sets up a stack with space for six values. The stack pointer is located at V5320. Values popped from the stack are written to location V3160. When a value is removed from the top of the stack, all other values in the stack move up to the next memory location toward the top of the stack. Flag SP56 is set when the table pointer is zero.



Key Sequence

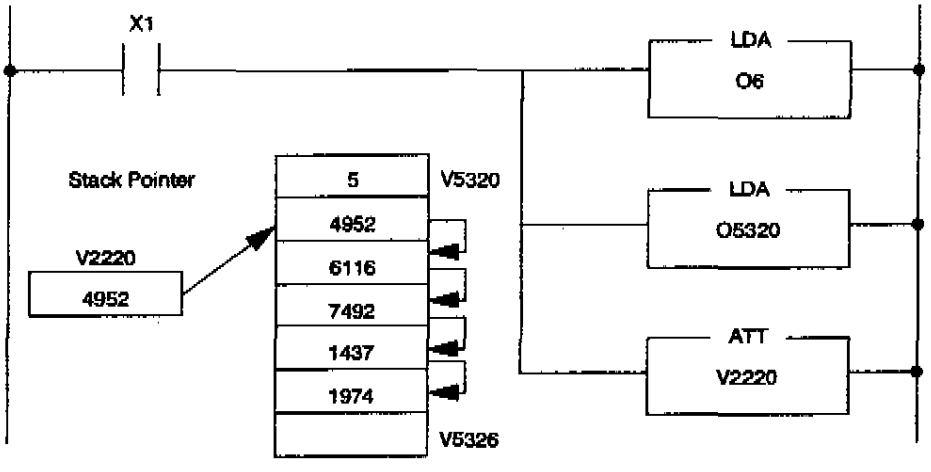


Valid Data Types: V

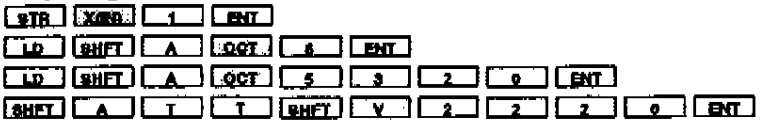
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ATT (TI435 Only)

Add to Top (ATT) pushes a value onto a user-defined stack from a V-memory location. The first stack register specifies the maximum length of the stack. The accumulator specifies the stack starting address, that is occupied by the stack pointer. The stack pointer contains the current number of values on the stack. If the stack length reaches the maximum length, operation stops. The example sets up a stack with space for six values. The stack pointer is located at V5320. Values pushed onto the stack are read from V2220. When a value is added to the top of the stack, all other values in the stack move down to the next memory location away from the top of the stack. When the table pointer equals the table size, flag SP56 is set.



Key Sequence



Valid Data Types: V and K

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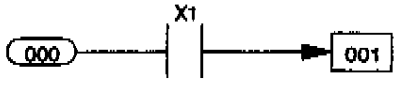
Chapter 20
Stage Instructions

ISG 20-2
SG 20-2
JMP 20-3
NJMP 20-3

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ISG

Initial Stage (ISG) indicates the first segment of a machine stage program made active when the TI405 CPU is switched to RUN mode. In the example, initial Stage S0 is active until X1 is turned on. This allows a transition to Stage S1, that becomes active at the same time initial Stage S0 becomes inactive.



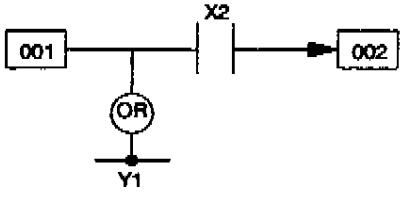
Key Sequence

ISG	S(SG)	0	ENT
STR	X(IN)	1	ENT
JMP	S(SG)	1	ENT

Valid Data Types: S

SG

Stage (SG) indicates any segment of a machine stage program, except the initial stage. Stages are inactive until activated by a JMP or SET from another stage. Stages become inactive when reset with an RST instruction, or a JMP is made from the current stage to another stage. In the example, Stage S1 turns on output Y1 until X2 closes and a jump is made to Stage S2.



Key Sequence

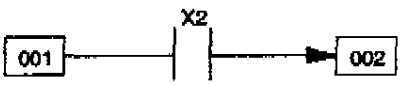
SG	S(SG)	1	ENT	
OR	OUT	Y(OUT)	1	ENT
STR	X(IN)	2	ENT	
JMP	S(SG)	2	ENT	

Valid Data Types: S

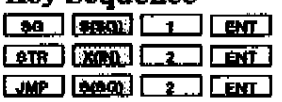
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JMP

Jump to Stage (JMP) makes a transition from one program stage to another when the transition conditions are true. The stage being jumped from is made inactive, and the stage being jumped to is made active. In the example, a jump from Stage S1 to Stage S2 is made when X2 is on.



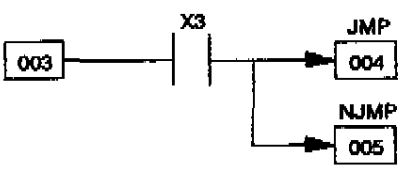
Key Sequence



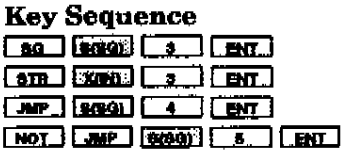
Valid Data Types: S

NJMP

NOT Jump to Stage (NJMP) makes a transition from one stage to another when the transition conditions are false. The stage being jumped from is made inactive, and the stage being jumped to is made active. In the example, a jump is made from Stage S3 to Stage S4 when X3 is on, or a jump is made to Stage S5 when X3 is off.



Key Sequence



Valid Data Types: S

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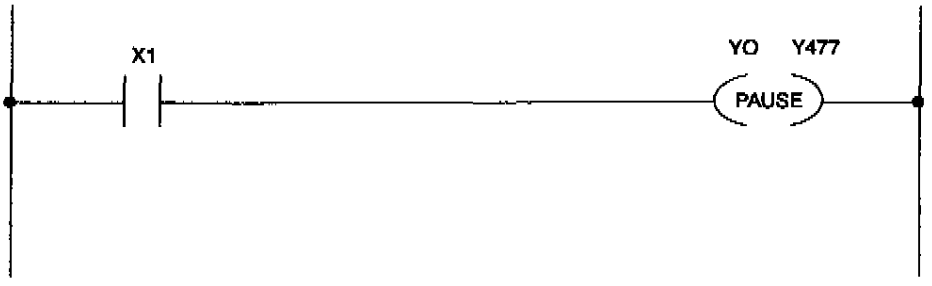
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Program Control Instructions

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PAUSE

PAUSE turns off the specified range of physical output points. Only the actual output module points are turned off; the image register is not affected. In the example, if X1 is turned on, all outputs are disabled.



Key Sequence

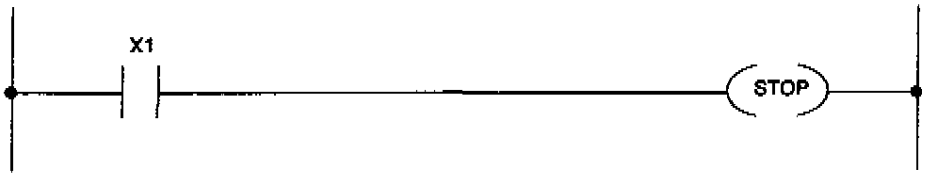


Valid Data Types: Y

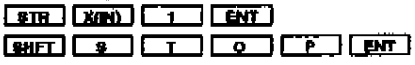
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STOP

The STOP instruction switches the PLC to the program (PGM) mode when its input is on. This turns off all outputs.



Key Sequence

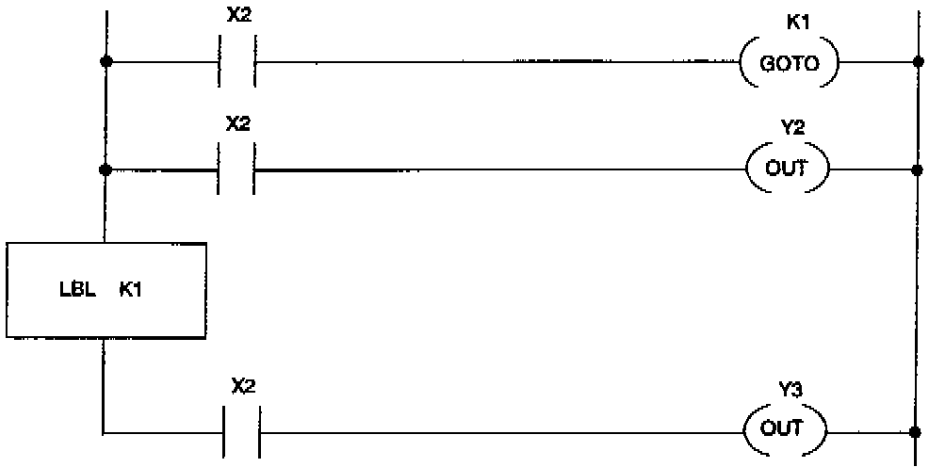


Valid Data Types: none

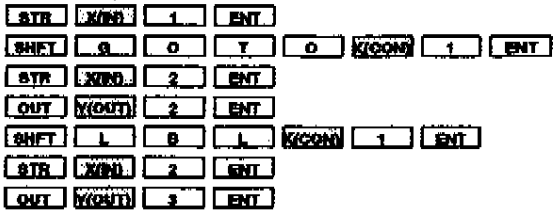
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GOTO/LBL (TI435 Only)

When its input is on, Go To Label (GOTO) causes program execution to skip all instructions until a LBL is found. Program execution resumes with the instruction following the LBL. Up to 128 GOTO instructions may be used in one program, but only 64 LBL instructions may be used. Error E412 results when these limits are exceeded.



Key Sequence



Valid Data Types: K (1–FFFF)

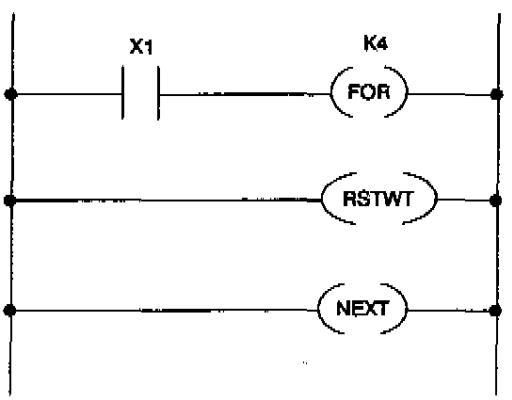
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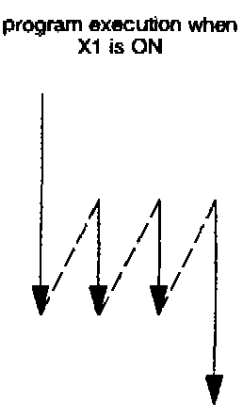
FOR/NEXT (TI435 Only)

When the input to the FOR instruction is on, the instructions between the FOR and the NEXT are executed the number of times specified by the K value used with the FOR. If the input is off, the instructions between the FOR and the NEXT are not executed. If the input is turned off after the FOR/NEXT loop is started, the loop continues to execute for the specified number of times.

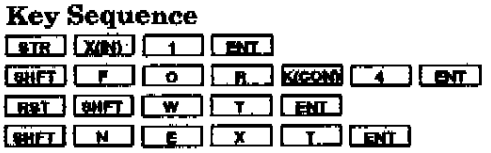
Since the normal program scan is suspended while the FOR/NEXT loop is active, immediate I/O points must be used inside the loop, or no I/O updates are made. It is usually necessary to use a RSTWT instruction inside the loop to reset the watchdog timer, and to prevent a software timeout.

FOR/NEXT loops may not be nested within other FOR/NEXT loops. Up to 64 FOR/NEXT pairs may be used in your program. Error E413 results when this limit is exceeded.





Key Sequence

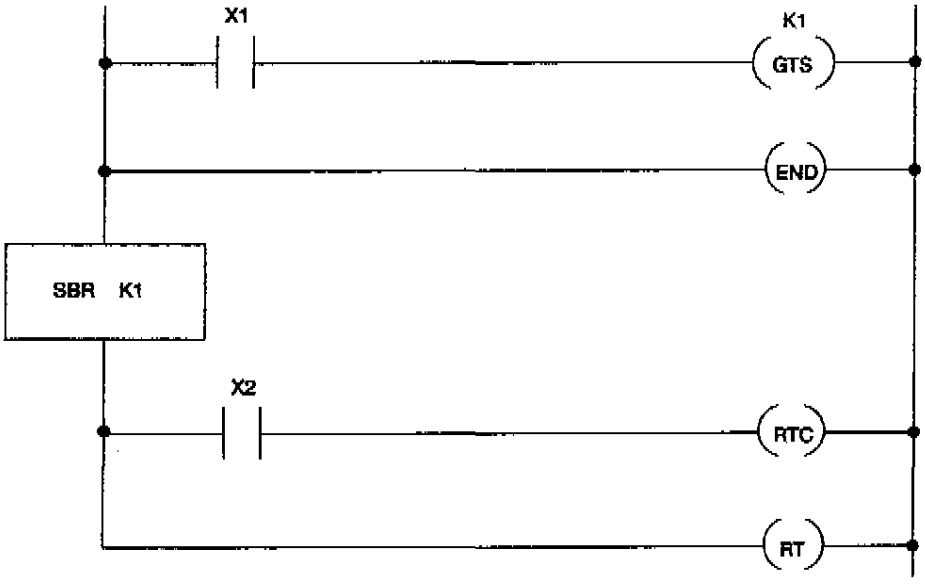


Valid Data Types: K (0–9999) and V

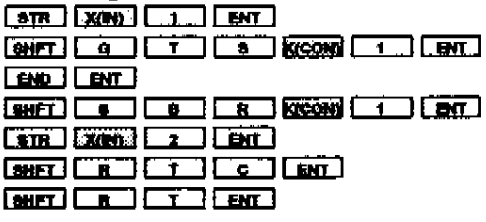
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GTS (TI435 Only)

When the input to Go To Subroutine (GTS) is on, program execution jumps to the subroutine (SBR) with the same identifying number. After the subroutine has executed and returned, program execution resumes with the next instruction after the GTS. Up to 128 GTS instructions may be used with up to 64 SBR instructions. Error E412 results when these limits are exceeded. Nesting of up to 8 levels is supported.



Key Sequence



Valid Data Types: K (1–FFFF)

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SBR (TI435 Only)

The instructions following a Subroutine (SBR) instruction are executed whenever the GTS instruction with the same identifying number is active. The SBR instruction must be located after the end instruction. The last instruction in a subroutine must be an RT.

Valid Data Types: K (1–FFFF)

RTC (TI435 Only)

When the input to the Conditional Subroutine Return (RTC) is on, subroutine execution stops at that point and a return is made to the program that called the subroutine. When the input is off, subroutine execution continues past the RTC.

Valid Data Types: none

RT (TI435 Only)

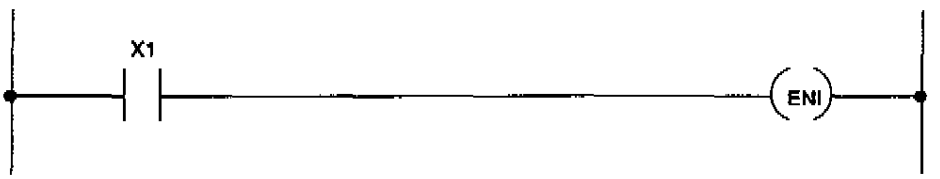
Unconditional Subroutine Return (RT) is always the last instruction in a subroutine. The RT returns program execution to the program that called the subroutine.

Valid Data Types: none

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ENI

After the input to Enable Interrupts (ENI) is turned on, inputs from the interrupt module cause immediate transfer of program execution to the corresponding interrupt routine. Interrupts may be disabled with the DISI instruction.



Key Sequence

STR | X/IN0 | 1 | ENT
SHFT | E | N | I | ENT

Valid Data Types: none

DISI

After the input to Disable Interrupts (DISI) is turned on, inputs from the interrupt module are disabled and interrupt routines are not executed. Interrupts may be enabled with the ENI instruction.



Key Sequence

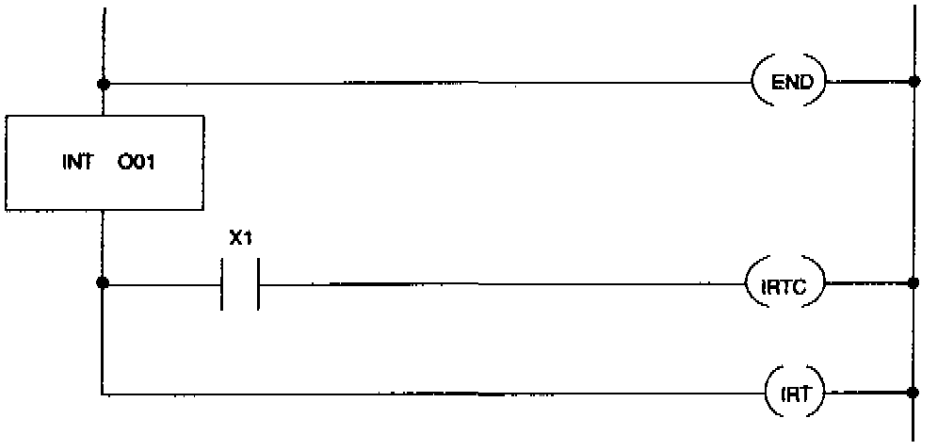
STR | X/IN0 | 1 | ENT
SHIFT | D | I | S | I | ENT

Valid Data Types: none

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INT

When an input is made on the Interrupt (INT) module, and interrupts have been enabled with the ENI instruction, the interrupt routine number that corresponds with the input point is executed immediately. The INT routine must be located after the END statement, and must end with an IRT instruction.



Key Sequence

END ENT
SHIFT I N T OCT 1 ENT
STR X(IN) 1 ENT
SHIFT I R T C ENT
SHIFT I R T ENT

Valid Data Types: O (0–7)

IRTC

When its input is on, and the Conditional Interrupt (IRTC) is reached, execution of the current interrupt routine halts and program execution returns to the main program. When its input is off, interrupt routine execution continues past the IRTC.

IRT

When Interrupt Return (IRT) is reached, execution of the current interrupt routine halts, and program execution returns to the main program. An IRT must be the last instruction in an interrupt routine.

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MLS/MLR

The Master Line Set (MLS) is used in combination with the Master Line Read (MLR) to enable and disable sections of ladder logic by establishing new levels of left power rails. The original left rail is thought of as master line 0. When an MLS K1 instruction is used, it starts a new master line at level 1. Master lines can be used to nest left power rails up to seven levels deep.

Figure 21-1 illustrates how the MLS/MLR instructions operate. Figure 21-2 is the actual RLL program for this example.

In the example, the state of X0 controls all of the outputs between the MLS K1 instruction on the first line, and the MLR K0 instruction on the next to last line. Figure 21-1 shows the apparent operation of this circuit. An MLS is always paired with an MLR that has a K value one less than the MLS. For example, MLS K2 on the second line is paired with MLR K1, and defines the region of the program controlled by X2. The MLR K1 returns control to the master line at level 1: the left rail extending down from the point of the MLS K1 on the first line in Figure 21-1. An MLR K0 always returns control to the original left power rail. Since the line ending in Y16 is below the MLR K0 instruction, the state of Y16 is controlled by X16, and is not affected by any of the Master Line Set instructions.

X0 controls the operation of Y1 through Y15, since it determines whether or not the nested master lines receive any power flow from the original left rail. X2 controls the power flow to master lines 2 and 3, and thus controls the operation of Y3 through Y10. X5 determines whether or not power flow is passed from master line 2 to master line 3 and controls Y6 and Y7. Since master line 3 is nested the deepest in this example, the state of Y7 is dependent on the state of X0 and X2 and X5 and X7. If any of these four X inputs are open, there is a break in power flow between Y7 and master line 0, that is the original left rail and the source of all power flow.

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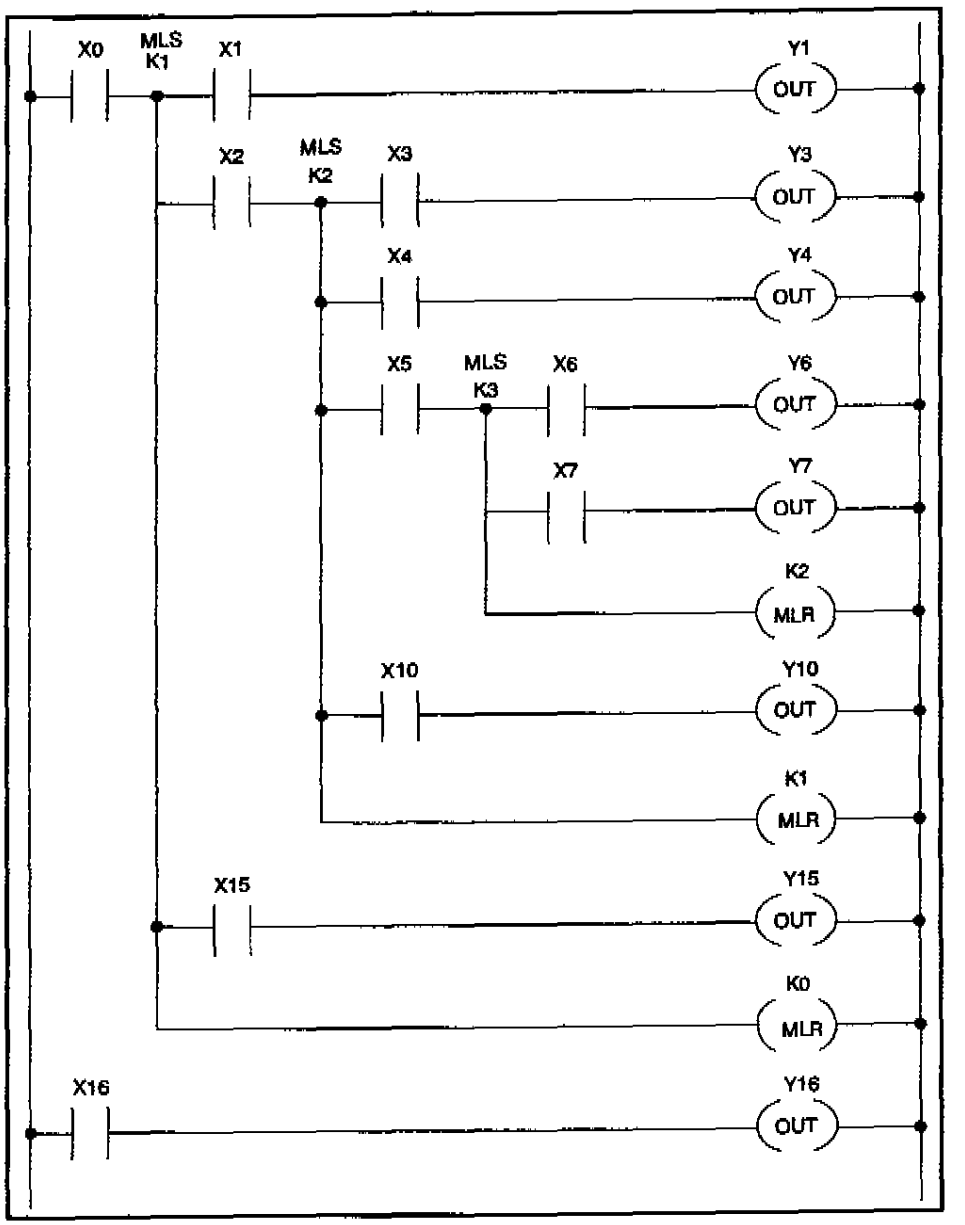
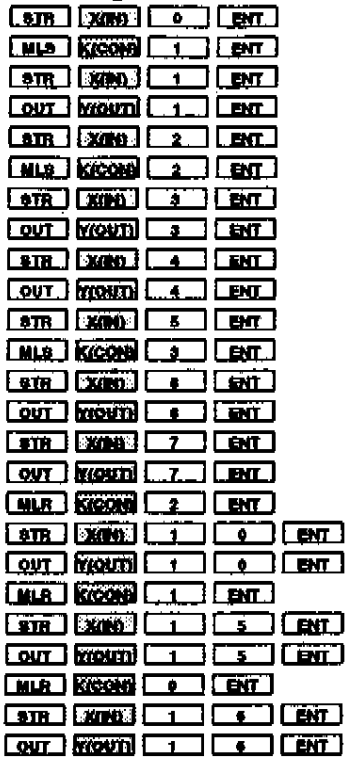


Figure 21-1 Operation of MLS/MLR Instructions

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Key Sequence



Valid Data Types:	**MLS**	**K1-K7**
	MLR	**K0–K7**

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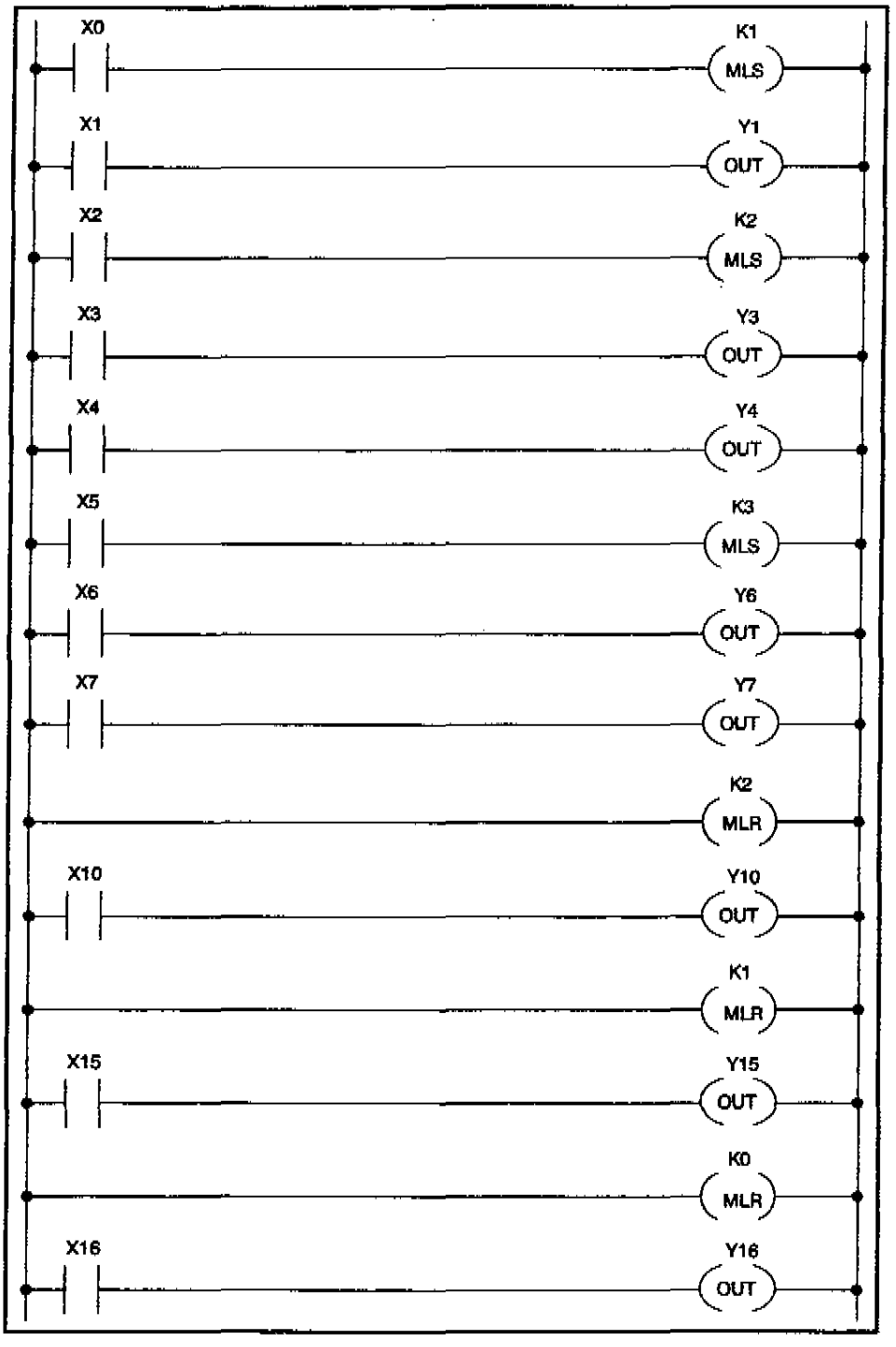


Figure 21-2 MLS/MLR RLL Example

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Chapter 22
Program Support Instructions

SET 22-2
RST 22-2
SR 22-3
PD 22-4
NOP 22-4
END 22-5
LDLBL (TI435 Only) 22-5
MOVMC (TI435 Only) 22-6
RD 22-8
WT 22-9
RX 22-10
WX 22-12
FAULT 22-14
RSTWT 22-15

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SET

Set Image Register Range (SET) turns on a range of points in the image register. If any of the set points are used as outputs elsewhere in the program, they continue to be controlled by program logic.



Key Sequence



Valid Data Types: X, Y, C, S, and GX

RST

Reset Image Register Range (RST) turns off a range of points in the image register. If any of the reset points are used as outputs elsewhere in the program, they continue to be controlled by program logic.



Key Sequence



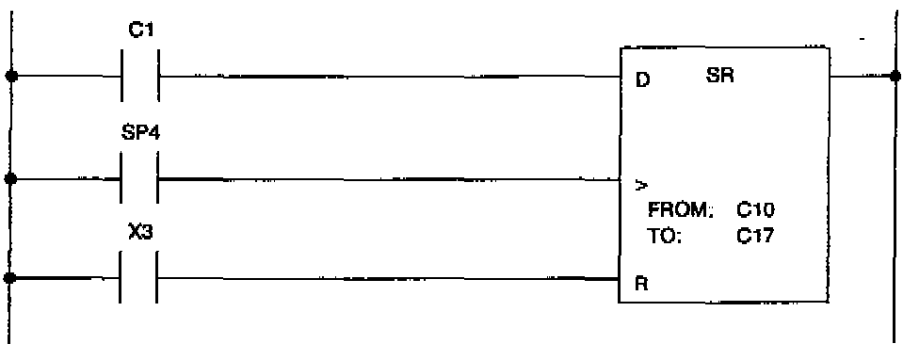
Valid Data Types: X, Y, C, S, T, CT, and GX

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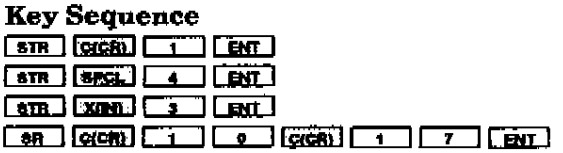
SR

Shift Register (SR). When a low to high transition is seen on the clock input (>), the current on or off states of the contacts in the chain defined by the two C numbers in the SR box are shifted to the next higher contact. The state of the data contact (D) is shifted into the first contact, and the previous state of the last contact is lost. Closing the reset contact (R) turns off all the contacts in the chain.

The first contact in the chain must start on an interval of 8 (0, 10, 20, 30, etc.) and the chain must span a multiple of 8 contacts. This produces ranges such as C0 to C37, C10 to C17, or C30 to C67. Remember that all control relays are numbered in octal, so the numerals 8 and 9 are not used. If your application does not require an even multiple of 8 control relays, the remainder can simply be ignored.



Key Sequence

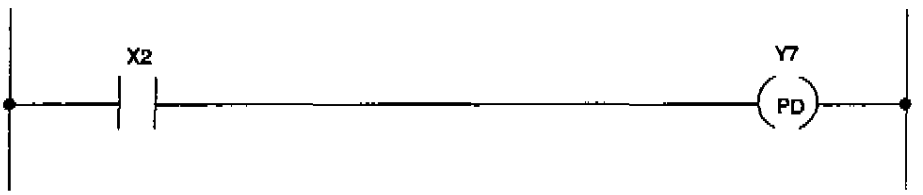


Valid Data Types: C

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PD

Positive Differential (PD) turns on for one scan each time its input makes a low to high transition. This produces a pulse, or one shot.



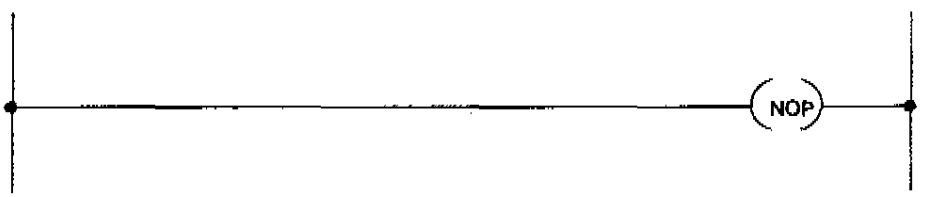
Key Sequence

STR | X/CR | 2 | ENT
SHIFT | P | D | SHIFT | Y/OUT | 7 | ENT

Valid Data Types: X, Y, and C

NOP

No Operation (NOP) represents an empty program location.



Key Sequence

SHIFT | N | O | P | ENT

or

CLR | ENT

Valid Data Types: none

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END

End of Program Scan (END) terminates the program scan. The executable portion of your program must use an END as its last instruction. Omitting the END instruction results in **ERROR E4** NO PROGRAM**. Data constant area, subroutines and interrupt routines are located after the END instruction.



Key Sequence

END ENT

Valid Data Types: none

LDLBL (TI435 Only)

Load Data Label Address (LDLBL) loads a DLBL reference number to the accumulator. This instruction is used with MOVMC to move data from a data label area of program memory to V-memory.

Valid Data Types: K (1–FFFF)

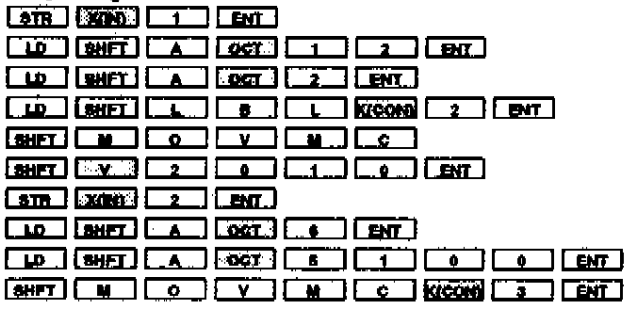
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MOVMC (TI435 Only)

Move Data Label Area to V-memory (MOVMC) is used with LDLBL to transfer data from a DLBL area of program memory to V-memory. It may be used by itself to transfer data from V-memory to a DLBL area of program memory. The second stack register holds the length in words of the memory block to be transferred. The first stack register holds the offset from both the data label in program memory and the beginning of the V-memory block. The accumulator holds the source address and the MOVMC instruction provides the destination address.

The first example shows moving 12 (octal) words of memory from DLBL K2 to a V-memory block beginning at V2010. The data is read starting at an offset of 2 from the data label, and written starting at an offset of 2 into the V-memory block. The second example shows moving 6 words of memory from a table beginning at location V5100 to DLBL K3. The data is read starting at an offset of 14 (octal) into the V-memory table and written starting at an offset of 14 from the data label.

Key Sequence



Valid Data Types: V and K (1–FFFF)

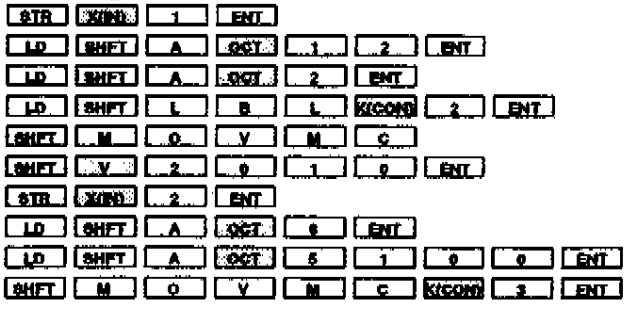
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MOVMC (TI435 Only)

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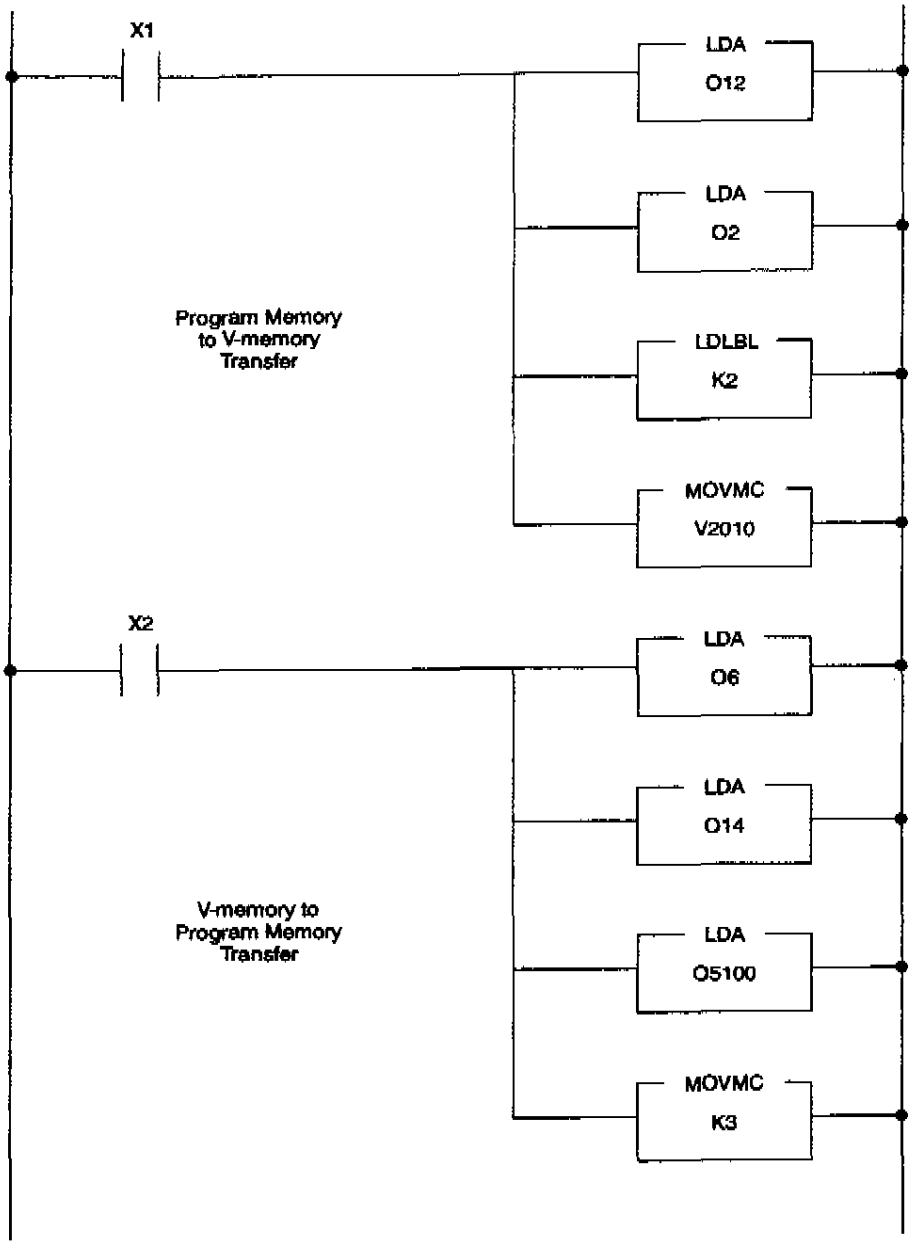
The first example shows moving 12 (octal) words of memory from DLBL K2 to a V-memory block beginning at V2010. The data is read starting at an offset of 2 from the data label, and written starting at an offset of 2 into the V-memory block. The second example shows moving 6 words of memory from a table beginning at location V5100 to DLBL K3. The data is read starting at an offset of 14 (octal) into the V-memory table and written starting at an offset of 14 from the data label.

Key Sequence



Valid Data Types: V and K (1–FFFF)

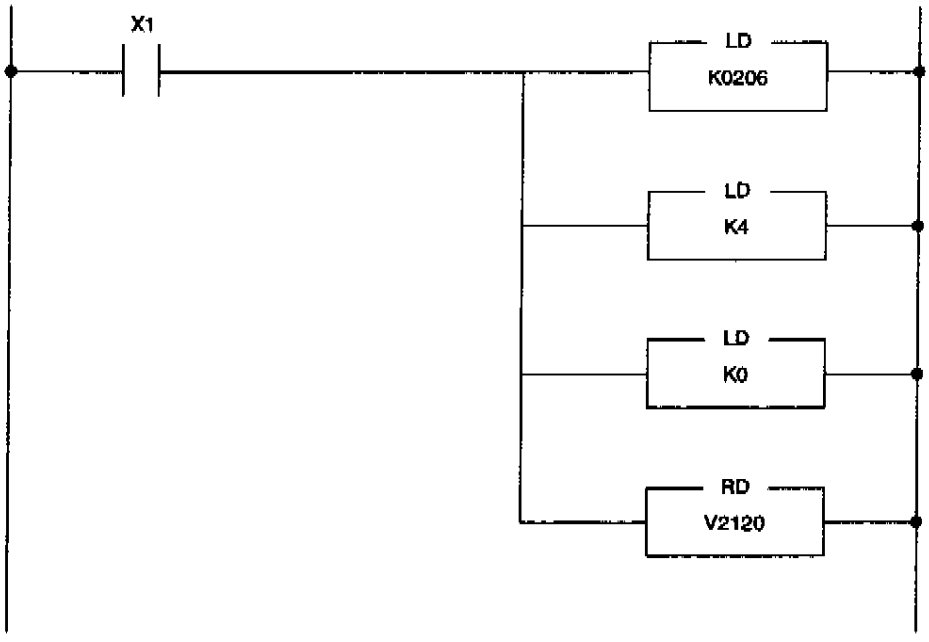
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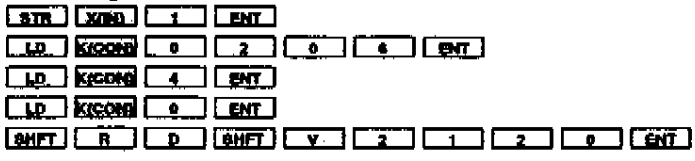
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RD

Read Data From Intelligent I/O (RD) reads a block of data from an intelligent module into V-memory. The first stack register specifies the base (0–3) and slot (0–7) where the module is located. The second stack register specifies the number of bytes to be transferred (1–128). The accumulator specifies the shared RAM address, in BCD, of the intelligent module. The V-memory address used with the RD instruction indicates the first location where the data is to be stored. In the example, LD K0206 specifies that the module is in base 02, slot 06. LD K4 indicates that four bytes of data are transferred. LD K0 indicates that the shared RAM is at address 0. RD V2120 means that the four bytes of data are stored in V-memory locations V2120 and V2121.



Key Sequence



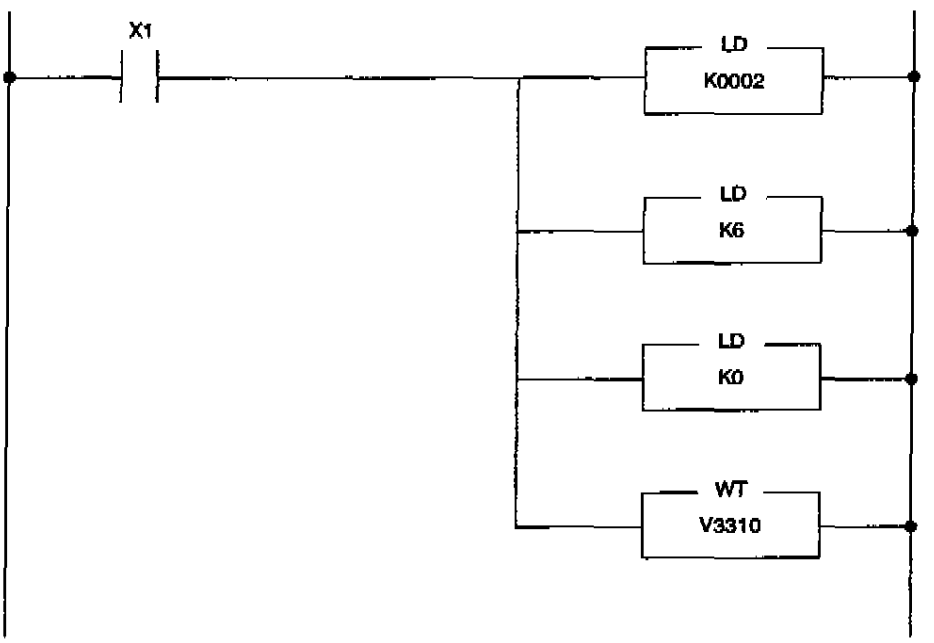
Valid Data Types: V

NOTE: The number of bytes to transfer parameter must be a hex number (1–80).

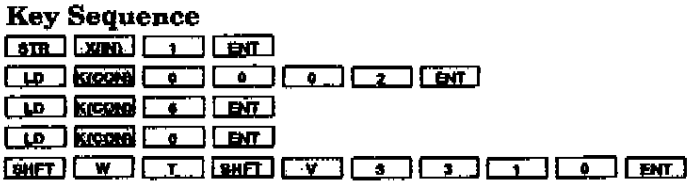
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WT

Write Data To Intelligent I/O (WT) writes a block of data to an intelligent module from V-memory. The first stack register specifies the base (0–3) and slot (0–7) where the module is located. The second stack register specifies the number of bytes to be transferred (1–128). The accumulator specifies the shared RAM address, in BCD, of the intelligent module. The V-memory address used with the WT instruction indicates the first location where the data to be written is to be stored. In the example, LD K0002 specifies that the module is in base 00, slot 02. LD K6 indicates that six bytes of data are transferred to the module. LD K0 indicates that the shared RAM is at address 0. WT V3310 means that the six bytes of data are read starting at memory location V3310, and then written to the module.



Key Sequence



Valid Data Types: V

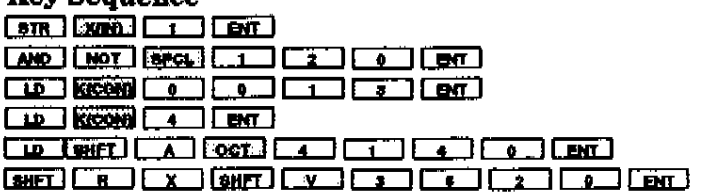
NOTE: The number of bytes to transfer parameter must be a hex number (1–80).

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RX

Read Data From Network (RX) reads data from another PLC through a network communications module. The first stack register holds the slot number (0–7) and the slave station address (in BCD). The second stack register holds the number of bytes to be transferred. The accumulator holds the address of the first V-memory location where incoming data is written. The address used with the RX instruction specifies at what location in the slave PLC the reading of data begins. In the example, special relay SP120 is used to prevent this instruction from executing if the communications module in slot 00 is busy. LD K0013 indicates that the module in slot 00 is used to communicate with slave station 13. LD K4 specifies that four bytes are read. LDA O4140 specifies that incoming data is written to memory starting at address V 4140. RX V3620 means to start reading at memory location V3620 in the slave PLC.

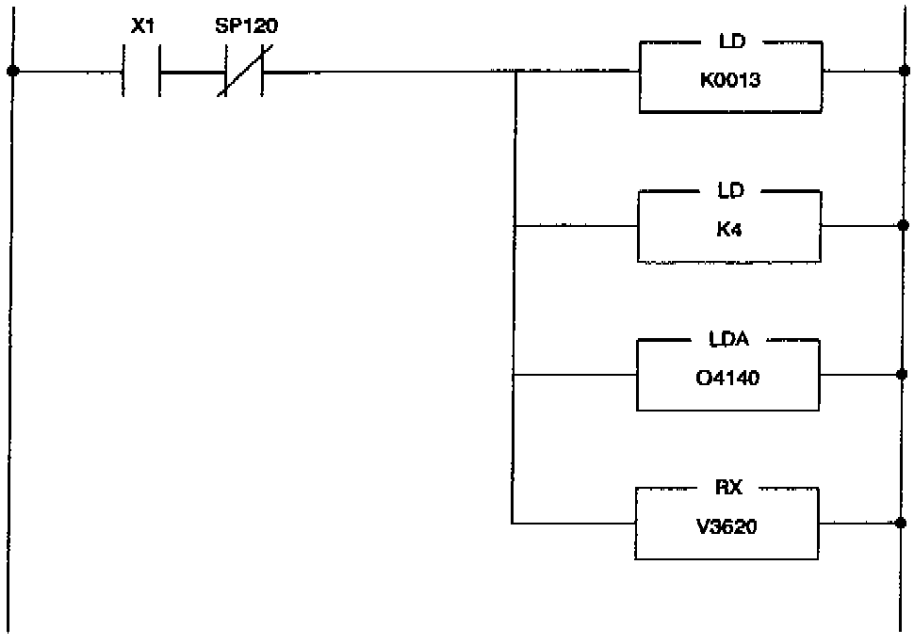
Key Sequence

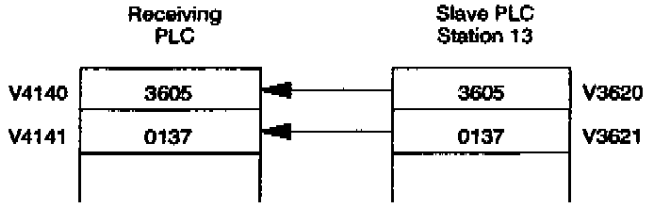


Valid Data Types: X, Y, C, T, CT, GX, V, SP, and S

NOTE: The number of bytes to transfer parameter must be a hex number (1–80).

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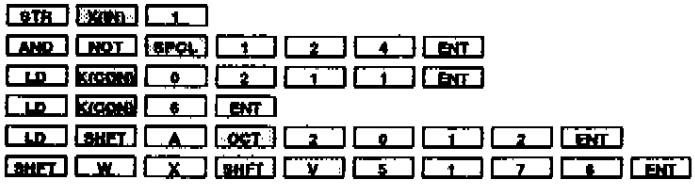


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WX

Write Data To Network (WX) writes data to another PLC through a network communications module. The first stack register holds the slot number (0–7) and the slave station address (in BCD). The second stack register holds the number of bytes to be transferred. The accumulator holds the address of the first V-memory location where the outgoing data is stored. The address used with the WX instruction specifies at what location in the slave PLC the writing of data begins. In the example, SP124 is used to prevent this instruction from executing when the communications module in slot 02 is busy. LD K0211 indicates that the module in slot 02 is used to communicate with slave station 11. LD K6 specifies that six bytes are written. LDA O2012 specifies that outgoing data is read from memory starting at address V 2012. WX V5176 means to start writing at memory location V5176 in the slave PLC.

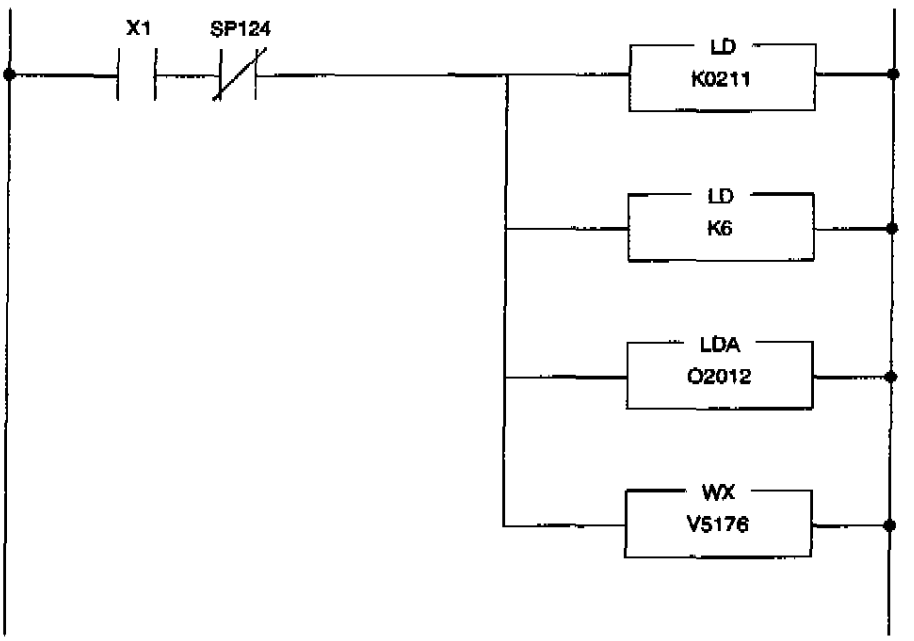
Key Sequence

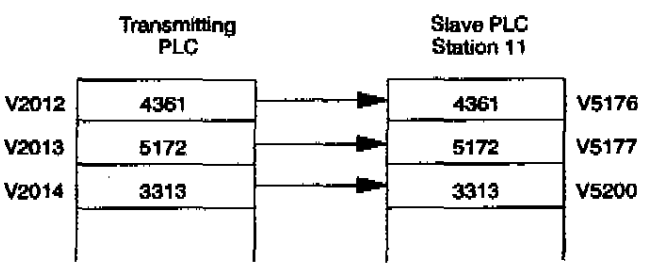


Valid Data Types: X, Y, C, T, CT, GX, V, SP, and $

NOTE: The number of bytes to transfer parameter must be a hex number (1–80).

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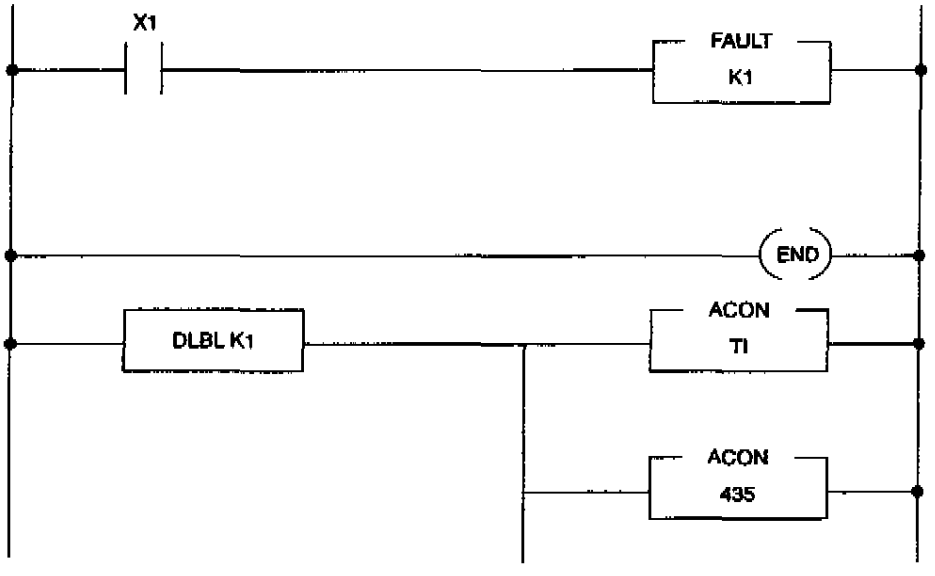




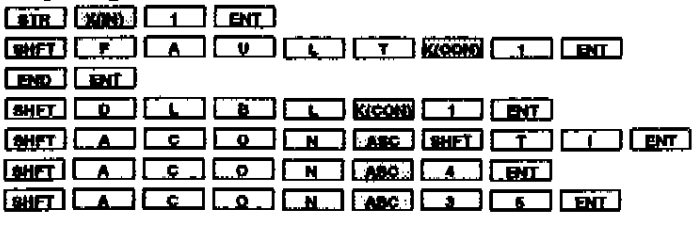
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FAULT

Display Fault Message (FAULT) displays a V-memory value or ASCII message on the MIU. If a V data type is used with the fault instruction, the four-digit value from that memory location is displayed. If a K data type is used with the TI435, the ASCII message (of up to 23 characters, stored with the corresponding DLBL) is displayed. If a K data type is used with the TI425, the specified constant value is displayed. In the example, whenever X1 makes an off-to-on transition, TI435 is displayed on the MIU. An error code is also stored at address V7751. If a V data type was used, the four-digit code from that location is stored at V7751. If a K data type was used, the K value is stored at V7751.



Key Sequence

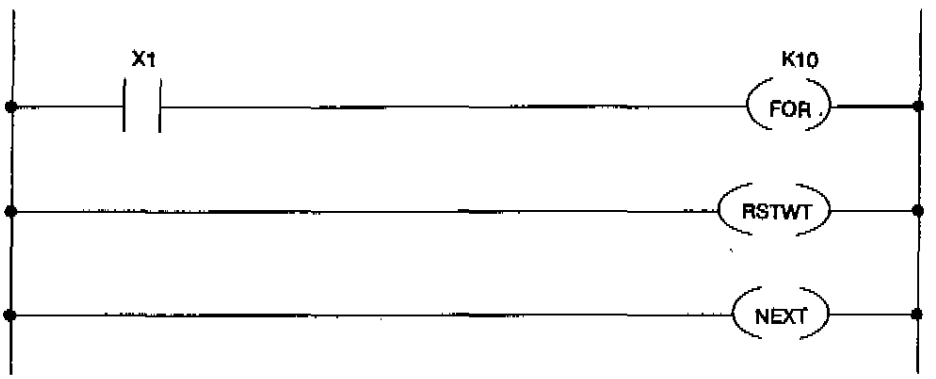


Valid Data Types:	TI425	V and K (0–FFFF)
	TI435	V and K (1–FFFF)

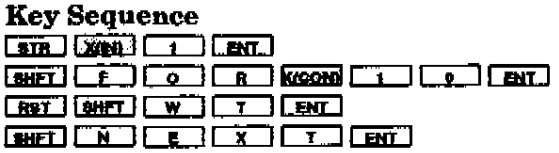
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RSTWT

Reset Watchdog Timer (RSTWT) must be used if a portion of the program, such as a FOR-NEXT loop, causes an extension of the scan time. If not, an E003 S/W TIMEOUT may occur.



Key Sequence



Valid Data Types: none

NOTE: The RSTWT instruction must follow the FOR instruction.

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Appendix A

Number Systems and Codes

A.1 Number Systems A-2

Decimal Numbers A-2
Binary Numbers A-2
Binary Coded Decimal Numbers A-3
Octal Numbers A-4
Hexadecimal Numbers A-5

A.2 ASCII Code A-6

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A.1 Number Systems

The TI405 instruction set uses four positional numbering systems for specifying numeric operands and constants. The Decimal and Binary Coded Decimal (BCD) number systems are used in numeric constants. The Octal numbering system is used to specify V-memory addresses and sequence numbers for stages, timers, counters, and other data types. The Hexadecimal number system is used for boolean and logical arithmetic operations, and for numeric constants.

Decimal Numbers

Our usual numbering system is decimal. This number system is based on raising the digits to the power of ten associated with the digit's position. For example, the number 592 is the representation for the sum of the following.

$$\begin{array}{lll} 2 \times 10^0 = & 2 \times 1 = & 2 \\ 9 \times 10^1 = & 9 \times 10 = & 90 \\ 5 \times 10^2 = & 5 \times 100 = & \underline{500} \\ & & 592 \end{array}$$

In the decimal number system, there are ten possible values for each digit, ranging from 0 to 9.

Binary Numbers

The binary number system has two possible values; 0 or 1. The position of the binary digits also represent raising the value to the corresponding power of two. However, since the value cannot be more than one, the result is the power of two for that position. For example, the binary number 1101 is the representation for the following.

$$\begin{array}{lll} 1 \times 2^0 = & 1 \times 1 = & 1 \\ 0 \times 2^1 = & 0 \times 2 = & 0 \\ 1 \times 2^2 = & 1 \times 4 = & 4 \\ 1 \times 2^3 = & 1 \times 8 = & \underline{8} \\ & & 13 \end{array}$$

Each binary digit position is referred to as a bit. The TI405 instruction set has instructions to perform arithmetic and logical operations on 16-bit and 32-bit binary values.

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Binary Coded Decimal Numbers

Binary Coded Decimal (BCD) numbers were developed to be easily recognized by humans, but in a form that CPUs could easily process. BCD is often used to enter data from a thumbwheel switch into the CPU as shown in Figure A-1. The BCD values are listed in Table A-1.

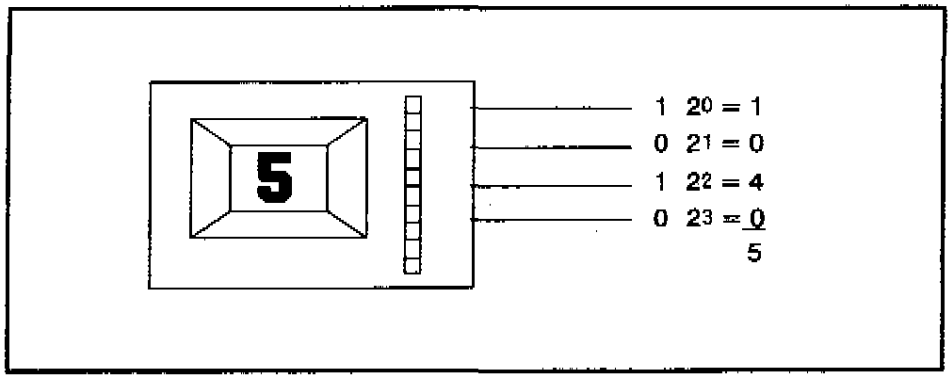


Figure A-1 BCD Output from a Thumbwheel Switch

Thumbwheel switches are often in groups of four digits that represent sixteen BCD bits, the size of the CPU word. See Table A-1 for a list of binary coded decimal values. Although a BCD digit is in binary form to the CPU, only the values from 0000 (0) to 1001 (9) are valid BCD numbers. The TI405 instruction set contains several instructions for performing arithmetic and logical operations on BCD values. Please refer to Chapter 8 for more details.

Table A-1 Binary Coded Decimal Values

Decimal	BCD	Decimal	BCD
0	0000	5	0101
1	0001	6	0110
2	0010	7	0111
3	0011	8	1000
4	0100	9	1001

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Octal Numbers

In the Octal number system, each digit can have eight possible values, from 0 to 7. Each digit position value is multiplied by a corresponding power of eight. For example, the octal number 127 is the representation of the sum of the following.

$$\begin{array}{lll} 7 \times 8^0 = & 7 \times 1 = & 7 \\ 2 \times 8^1 = & 2 \times 8 = & 16 \\ 1 \times 8^2 = & 1 \times 64 = & \underline{64} \\ & & 87 \end{array}$$

Table A-2 lists octal equivalents for the decimal numbers 0–19. The TI405 system uses the octal number system for the addresses of data types. For example, Timer 10 is the eighth timer and Stage 11 is the ninth stage.

Table A-2 Decimal/Octal Equivalents

Decimal	Octal	Decimal	Octal
0	0	10	12
1	1	11	13
2	2	12	14
3	3	13	15
4	4	14	16
5	5	15	17
6	6	16	20
7	7	17	21
8	10	18	22
9	11	19	23

Binary numbers are readily converted to octal numbers by grouping three binary digits as shown in Figure A-2.

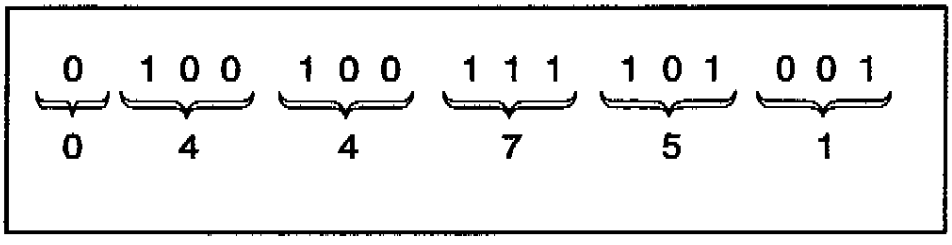


Figure A-2 Converting Binary to Octal

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Hexadecimal Numbers

In the hexadecimal number system, each digit can have sixteen possible values, from 0 to F. Each digit position value is multiplied by a corresponding power of sixteen. For example, the hexadecimal number 127 is the representation of the sum of the following. Table A-3 lists hexadecimal equivalents for the decimal numbers 0–15.

$$
\begin{aligned}
7 \times 16^0 &= 7 \times 1 = 7 \\
2 \times 16^1 &= 2 \times 16 = 32 \\
1 \times 16^2 &= 1 \times 256 = 256 \\
&\qquad\qquad\quad 295
\end{aligned}
$$

Table A-3 Decimal/Hexadecimal Equivalents

Decimal	Hexadecimal
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	A
11	B
12	C
13	D
14	E
15	F

Binary numbers are readily converted to hexadecimal numbers by grouping four binary digits as shown in Figure A-3. Hexadecimal numbers are easier for humans to work with than binary numbers.

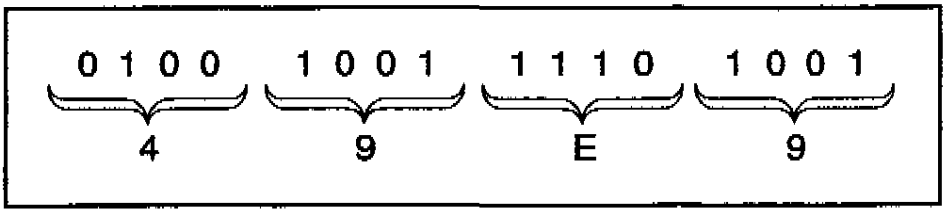


Figure A-3 Converting Binary to Hexadecimal

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A.2 ASCII Code

You can store ASCII code values in your ladder logic programs with the ACON instruction. Table A-4 lists the ASCII character codes. The ASCII control codes, listed in Table A-5, can be used to send protocol signals to the receiving device.

Table A-4 ASCII Character Codes

ASCII	Hex	ASCII	Hex	ASCII	Hex
space	20	@	40	`	60
!	21	A	41	a	61
"	22	B	42	b	62
#	23	C	43	c	63
$	24	D	44	d	64
%	25	E	45	e	65
&	26	F	46	f	66
'	27	G	47	g	67
(	28	H	48	h	68
)	29	I	49	i	69
*	2A	J	4A	j	6A
+	2B	K	4B	k	6B
,	2C	L	4C	l	6C
-	2D	M	4D	m	6D
.	2E	N	4E	n	6E
/	2F	O	4F	o	6F
0	30	P	50	p	70
1	31	Q	51	q	71
2	32	R	52	r	72
3	33	S	53	s	73
4	34	T	54	t	74
5	35	U	55	u	75
6	36	V	56	v	76
7	37	W	57	w	77
8	38	X	58	x	78
9	39	Y	59	y	79
:	3A	Z	5A	z	7A
;	3B	[	5B	{	7B
<	3C	\	5C	|	7C
=	3D	]	5D	}	7D
>	3E	^	5E	~	7E
?	3F	_	5F		

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To use the upper-case alphabetic characters, press [ASC] followed by the A–Z keys. To use any of the other ASCII values like punctuation characters, lower-case alphabetic characters, or the control codes, you must use the hexadecimal value. For example, to store the message "#2 Failure**" that is 2332204661696C7572652A2A in hexadecimal, enter the following key sequences.

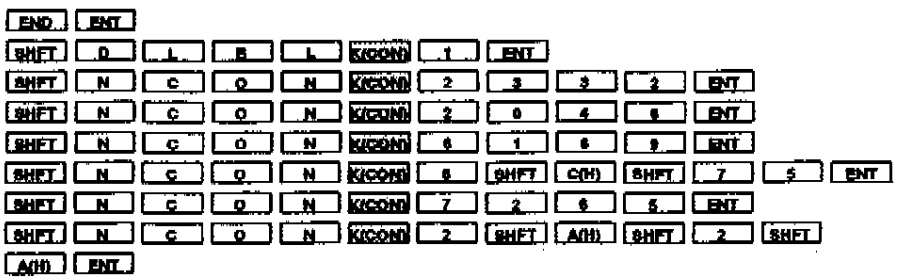


Table A-5 ASCII Control Codes

ASCII	Hex	ASCII	Hex	ASCII	Hex
NUL	00	VT	0B	SYN	16
SOH	01	FF	0C	ETB	17
STX	02	CR	0D	CAN	18
ETX	03	SO	0E	EM	19
EOT	04	SI	0F	SUB	1A
ENQ	05	DLE	10	ESC	1B
ACK	06	DC1	11	FS	1C
BEL	07	DC2	12	GS	1D
BS	08	DC3	13	RS	1E
HT	09	DC4	14	US	1F
LF	0A	NAK	15	DEL	7F

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Appendix B

Instruction Set Summary

B.1 Instruction Set Index B-2

B.2 Instruction Operands B-3

Discrete Operands B-3
Word Operands B-3

B.3 Instruction Summary B-4

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B.1 Instructions Set Index

Instruction	Page	Instruction	Page	Instruction	Page
ACON*	19–8	INCB	17–5	POP	15–2
ADD	16–2	INT	21–9	RD	22–8
ADDB	17–2	INV	15–5	RFB*	19–11
ADDBD*	17–2	IRT	21–9	RFT*	19–13
ADDD	16–2	IRTC	21–9	ROTL	14–5
ADDF*	14–8	ISG	20–3	ROTR	14–4
ADDS	15–3	JMP	20–4	RST	22–2
AND	9–3, 10–6, 13–9	LBL*	21–4	RSTI	11–7
AND STR	9–5	LD	13–2	RSTWT	22–15
ANDD	13–9	LDA	13–5	RT*	21–7
ANDE	10–3	LDD	13–3	RTC*	21–7
ANDF*	14–10	LDF*	14–6	RX	22–10
ANDI	11–4	LDIF*	11–8	SBR*	21–7
ANDN	9–4, 10–7	LDLBL*	22–5	SEG	18–5
ANDNE	10–4	LDSX*	14–14	SET	22–2
ANDNI	11–5	LDX	13–4	SETI	11–7
ATH*	18–6	MLR	21–10	SG	20–2
ATT*	19–14	MLS	21–10	SGCNT	12–7
BCD	18–2	MOV*	19–9	SHFL	14–3
BCDCPL	15–6	MOVMC*	22–6	SHFR	14–2
BIN	18–2	MUL	16–4	SR	22–3
CMP	13–12	MULB	17–4	STOP	21–3
CMPD	13–12	MULF*	14–9	STR	9–2, 10–5
CMPF*	14–13	MULS	15–4	STRE	10–2
CMPS	15–5	NCON*	19–8	STRI	11–2
CNT	12–6	NEXT*	21–5	STRN	9–2, 10–6
DEC	16–5	NJMP	20–3	STRNE	10–3
DECB	17–5	NOP	22–4	STRNI	11–2
DECO	18–4	OR	9–3, 10–5, 13–10	STT*	19–12
DISI	21–8	OR OUT	9–8	SUB	16–3
DIV	16–4	OR OUTI	11–6	SUBB	17–3
DIVB	17–4	OR STR	9–6	SUBBD*	17–3
DIVF*	14–9	ORD	13–10	SUBD	16–3
DIVS	15–4	ORE	10–2	SUBF*	14–8
DLBL*	19–7	ORF*	14–11	SUBS	15–3
ENCO	18–3	ORI	11–3	SUM	14–13
END	22–5	ORN	9–4, 10–7	TMR	12–2
ENI	21–8	ORNE	10–4	TMRA	12–4
FAULT	22–14	ORNI	11–4	TMRAF	12–5
FDGT*	19–5	OUT	9–7, 13–6	TMRF	12–3
FILL	19–2	OUTD	13–7	TTD*	19–10
FIND*	19–3	OUTF*	14–7	UDC	12–8
FOR*	21–5	OUTI	11–5	WT	22–9
GOTO*	21–4	OUTIF*	11–9	WX	22–12
GTS*	21–6	OUTX	13–8	XOR	13–11
HTA*	18–8	PAUSE	21–2	XORD	13–11
INC	16–5	PD	22–4	XORF*	14–12

NOTE: Instructions indicated with * are TI435 only.

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Discrete Operands

The TI405 instruction set uses eight discrete operand types as listed in Table B-1. Each of the types represent a relay ladder logic contact that can either be on or off.

Table B-1 Discrete Operand Types

Symbol	Description
X	Input
Y	Output
C	Control Relay
S	Stage
SP	Special Relay
GX	Remote I/O
T	Timer
CT	Counter

Word Operands

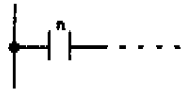
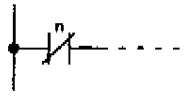
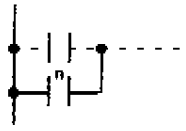
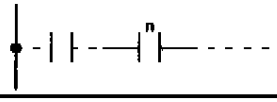
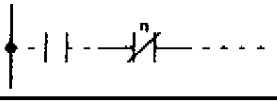
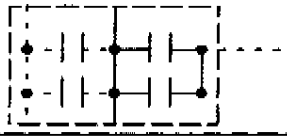
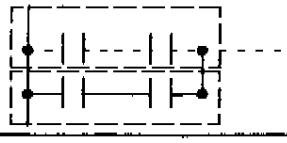
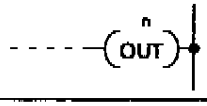
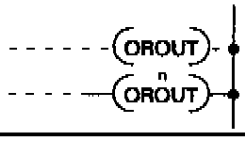
The TI405 instruction set uses six word operand types as listed in Table B-2. Each 16-bit word represents a corresponding value or code in the associated number base or ASCII code system.

Table B-2 Word Operand Types

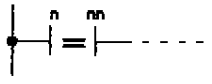
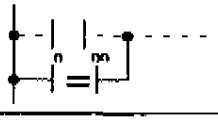
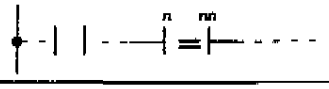
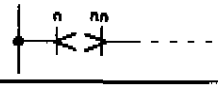
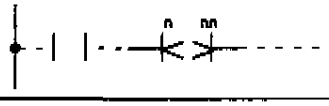
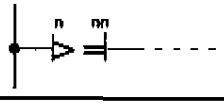
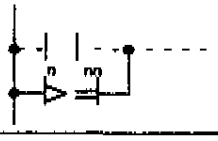
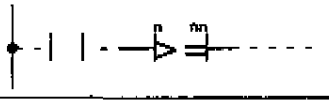
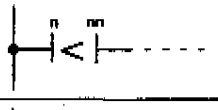
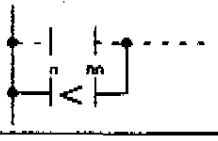
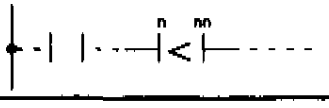
Symbol	Description
$	Program Memory Address (Octal)
V	Variable Memory Address (Octal)
P	Pointer (Octal)
K	Constant (Decimal or Hexadecimal)
O	Octal Constant
A	ASCII Codes

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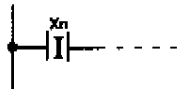
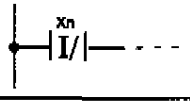
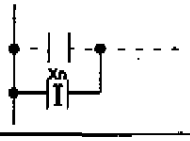
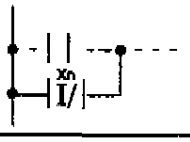
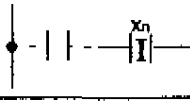
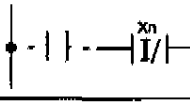
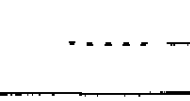
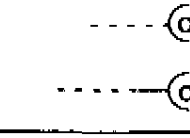
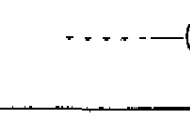
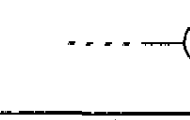
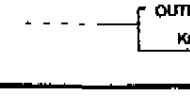
B.3 Instruction Summary

High Speed Boolean Functions		
Instruction	**Symbol**	**Short Description**
STR n=X, Y, C, S, T, CT, SP, GX		Store
STRN n=X, Y, C, S, T, CT, SP, GX		Store not
OR n=X, Y, C, S, T, CT, SP, GX		Or
ORN n=X, Y, C, S, T, CT, SP, GX		Or not
AND n=X, Y, C, S, T, CT, SP, GX		And
ANDN n=X, Y, C, S, T, CT, SP, GX		And not
AND STR		And store
OR STR		Or store
OUT n=X, Y, C, GX		Out
OR OUT n=X, Y, C, GX		Out (OR type)

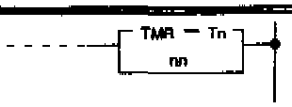
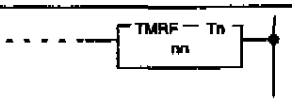
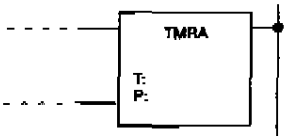
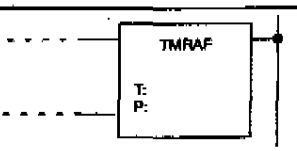
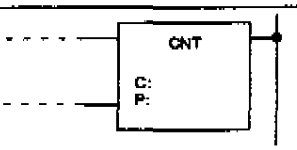
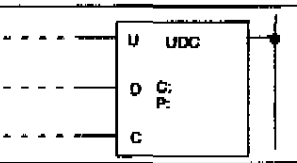
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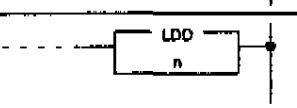
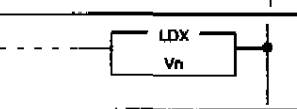
Comparative Boolean Functions		
Instruction	**Symbol**	**Short Description**
STRE n=V nn=V, K		Store if equal
ORE n=V nn=V, K		Or if equal
ANDE n=V nn=V, K		And if equal
STRNE n=V nn=V, K		Store if not equal
ORNE n=V nn=V, K		Or if not equal
ANDNE n=V nn=V, K		And if not equal
STR n=T, CT, V nn=V, K		Store if greater or equal (2 parameters)
OR n=T, CT, V nn=V, K		Or if greater or equal (2 parameters)
AND n=T, CT, V nn=V, K		And contact if greater or equal (2 parameters)
STRN n=T, CT, V nn=V, K		Store if contact if less than (2 parameters)
ORN n=T, CT, V nn=V, K		Or if less than (2 parameters)
ANDN n=T, CT, V nn=V, K		And contact if less than (2 parameters)

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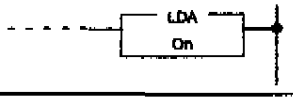
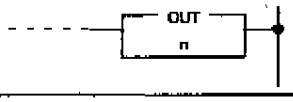
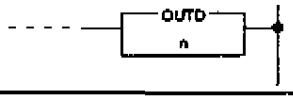
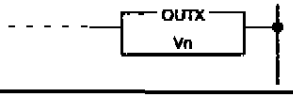
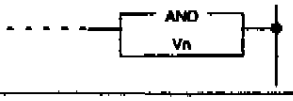
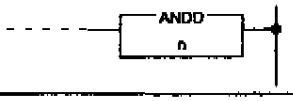
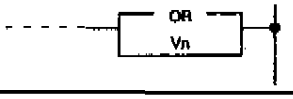
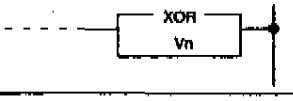
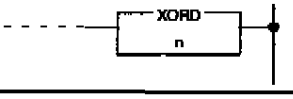
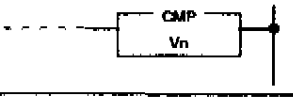
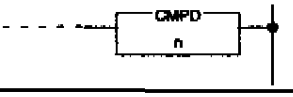
Immediate Functions		
Instruction	**Symbol**	**Short Description**
STRI		Store immediately
STRNI		Store not immediately
ORI		Or immediately
ORNI		Or not immediately
ANDI		And immediately
ANDNI		And not immediately
OUTI		Out immediately
OR OUTI		Out (OR type) immediately
SETI		Set range of bits
RSTI		Reset range of bits
LDIF		Load bits from modules to accumulator (TI435 Only)
OUTIF		Output bits from accumulator to modules (TI435 Only)

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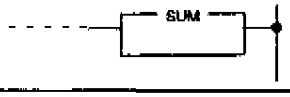
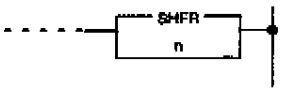
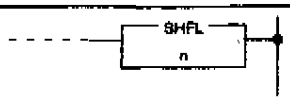
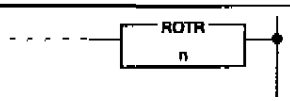
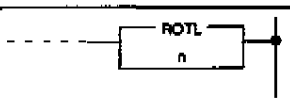
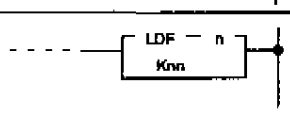
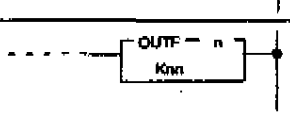
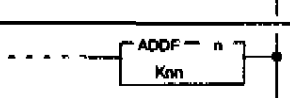
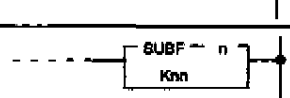
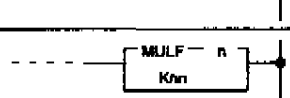
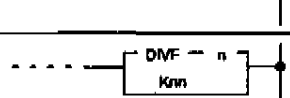
Timers/Counters		
Instruction	**Symbol**	**Short Description**
TMR		.1 sec timer
TMRF		.01 sec timer
TMRA		.1 sec timer with reset
TMRAF		.01 sec timer with reset
CNT		Counter with reset line
SGCNT		Counter reset with RST
UDC		Up/down counter

Accumulator Data Manipulation		
Instruction	**Symbol**	**Short Description**
LD n=V, P, K		Load word to accumulator
LDD		Index load word
LDX		Load octal address word

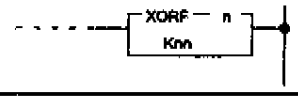
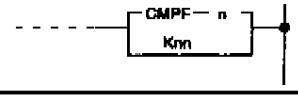
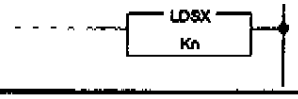
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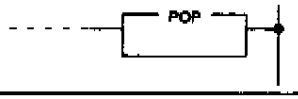
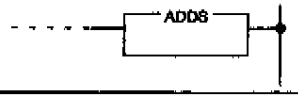
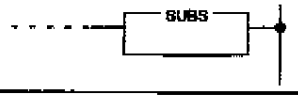
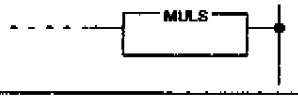
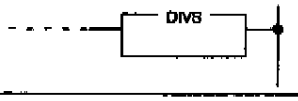
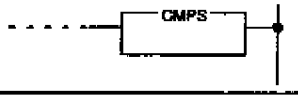
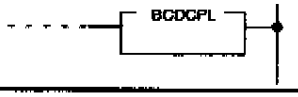
Accumulator Data Manipulation (continued)		
Instruction	**Symbol**	**Short Description**
LDA		Load octal address word
OUT		Output lower word to V-memory
OUTD		Output double word to V-memory locations
OUTX		Indexed Output to V-memory
AND		AND single word with accumulator
ANDD		AND double word with accumulator
OR		OR single word with accumulator
ORD		OR double word with accumulator
XOR		XOR single word with accumulator
XORD		XOR double word with accumulator
CMP		Compare single word with accumulator
CMPD		Compare double word with accumulator

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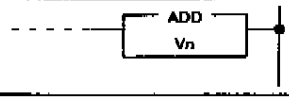
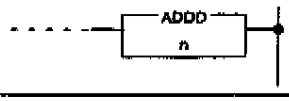
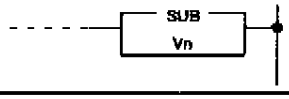
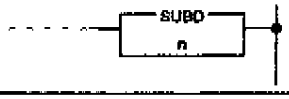
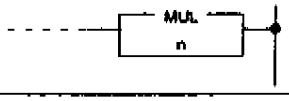
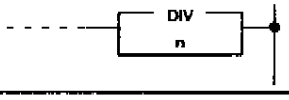
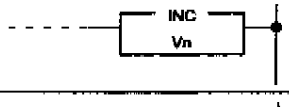
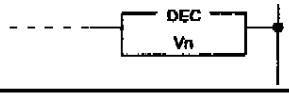
Bit Manipulation		
Instruction	**Symbol**	**Short Description**
SUM		Count number of ones in accumulator
SHFR		Shift accumulator right
SHFL		Shift accumulator left
ROTR		Rotate accumulator right
ROTL		Rotate accumulator left
LDF		Load bits to accumulator (TI435 only)
OUTF		Output bits from accumulator (TI435 only)
ADDF		Add value of specified number of bits to accumulator (TI435 only)
SUBF		Subtract value of specified number of bits (TI435 only)
MULF		Multiply value of specified number of bits by accumulator (TI435 only)
DIVF		Divide accumulator by value of specified number of bits (TI435 only)
ANDF		AND value of specified number of bits with accumulator (TI435 only)
ORF		OR value of specified number of bits with accumulator (TI435 only)

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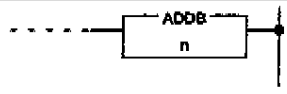
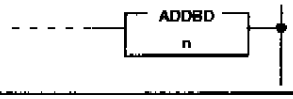
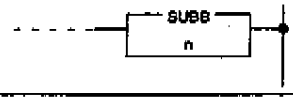
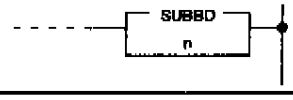
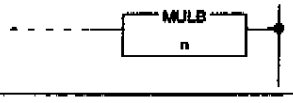
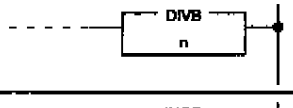
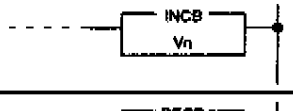
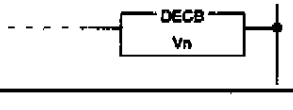
Bit Manipulation (continued)		
Instruction	**Symbol**	**Short Description**
XORF		XOR value of specified number of bits with accumulator (TI435 only)
CMPF		Compare value of specified number of bits with accumulator (TI435 only)
LDSX		Load accumulator with data offset from DLBL (TI435 only)

Accumulator Stack Instructions		
Instruction	**Symbol**	**Short Description**
POP		Pop accumulator stack
ADDS		Add top of stack to accumulator
SUBS		Subtract top of stack from accumulator
MULS		Multiply top of stack with accumulator
DIVS		Divide top of stack with accumulator
CMPS		Compare top of stack with accumulator
INV		One's complement of accumulator
BCDCPL		10's complement of accumulator

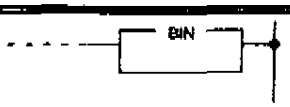
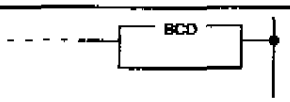
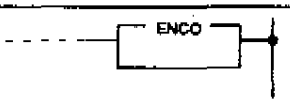
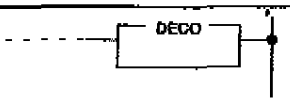
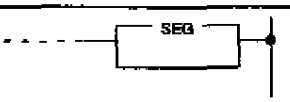
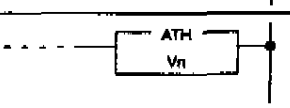
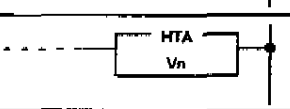
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BCD Operations		
Instruction	**Symbol**	**Short Description**
ADD		BCD 4 digit addition
ADDD		BCD 8 digit addition
SUB		BCD 4 digit subtraction
SUBD		BCD 8 digit subtraction
MUL		BCD 4 digit multiplication
DIV		BCD 4 digit division
INC		BCD increment V-memory
DEC		BCD decrement V-memory

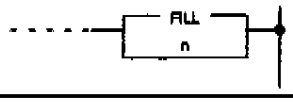
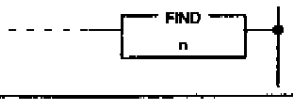
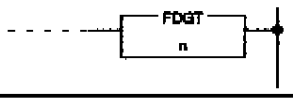
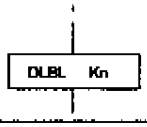
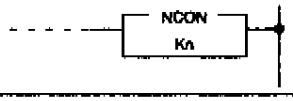
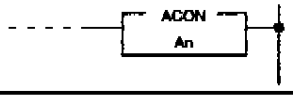
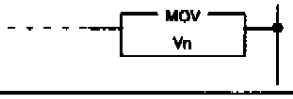
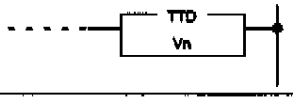
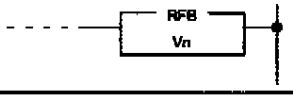
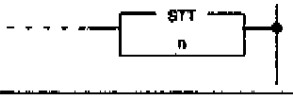
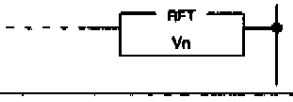
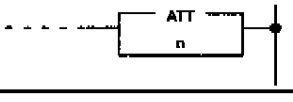
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Binary Operations		
Instruction	**Symbol**	**Short Description**
ADDB		Binary word addition
ADDBD		Binary double word addition
SUBB		Binary word subtraction
SUBBD		Binary double word subtraction
MULB		Binary multiplication
DIVB		Binary division
INCB		Binary increment V-memory
DECB		Binary decrement V-memory

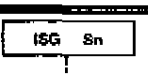
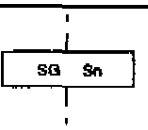
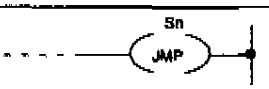
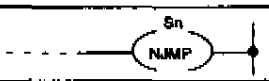
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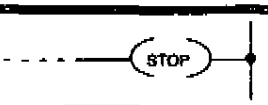
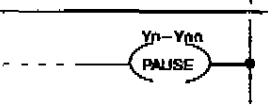
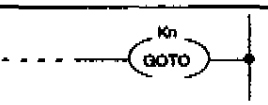
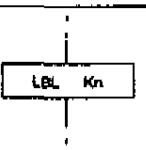
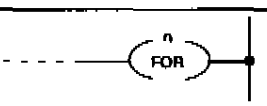
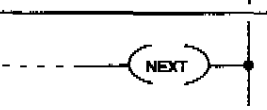
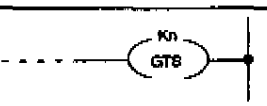
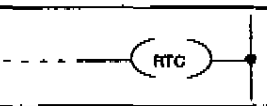
Encoding and Decoding		
Instruction	**Symbol**	**Short Description**
BIN		BCD to binary
BCD		Binary to BCD
ENCO		Encodes position of the first 1 bit in the accumulator
DECO		Decode the encoded code into accumulator
SEG		Accumulator to 7 segment display
ATH		ASCII to hex (TI435 only)
HTA		Hex to ASCII (TI435 only)

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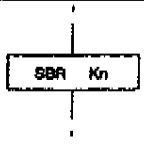
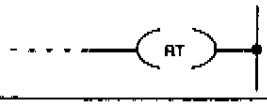
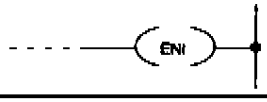
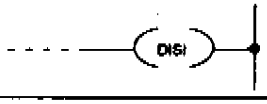
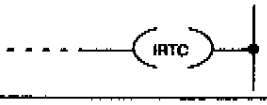
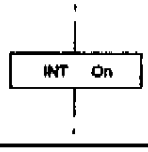
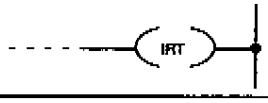
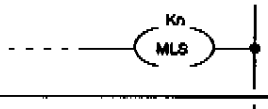
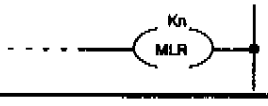
Table Functions		
Instruction	**Symbol**	**Short Description**
FILL		Fill table with value
FIND		Find value in table (TI435 only)
FDGT		Find greater than or equal (TI435 only)
DLBL		Data label reference (TI435 only)
NCON		Hexadecimal table (TI435 only)
ACON		ASCII table (TI435 only)
MOV		Move table (TI435 only)
TTD		Move from table, increment pointer (TI435 only)
RFB		Move from table, decrement pointer (TI435 only)
STT		Source to table, increment pointer (TI435 only)
RFT		Remove (pop) from top of data stack, move to V
ATT		Add (push) to top of data stack a V value

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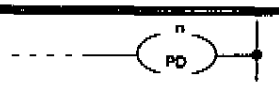
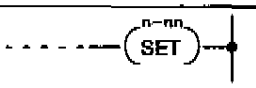
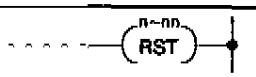
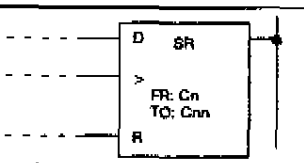
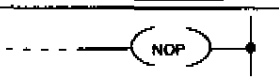
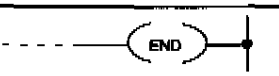
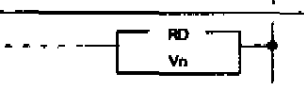
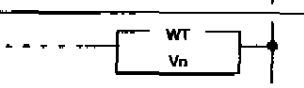
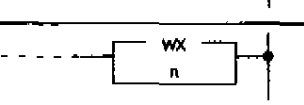
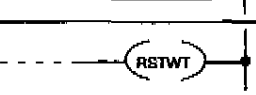
Stage		
Instruction	**Symbol**	**Short Description**
ISG		Initial stage
SG		Stage
JMP		Jump
NJMP		Not jump

Program Control		
Instruction	**Symbol**	**Short Description**
STOP		Change PLC to program mode
PAUSE		Disable range of outputs
GOTO		Go to instruction following LBL (TI435 only)
LBL		Label of GOTO instructions (TI435 only)
FOR		Run loop X times (TI435 only)
NEXT		Signifies end of For/Next loop (TI435 only)
GTS		Go to subroutine (TI435 only)
RTC		Conditional subroutine return (TI435 only)

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Program Control (continued)		
Instruction	**Symbol**	**Short Description**
SBR		Subroutine label (TI435 only)
RT		Unconditional subroutine return (TI435 only)
ENI		Enable interrupt
DISI		Disable interrupt
IRTC		Conditional interrupt return
INT		Interrupt routine label
IRT		Unconditional interrupt return
MLS		Master line set
MLR		Master line read

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Program Support		
Instruction	**Symbol**	**Short Description**
PD n=X, Y, C		Positive differential (one shot)
SET n, nn=X, Y, C, S, GX		Set range (latch)
RST n, nn=X, Y, C, S, T, CT, GX		Resets range (unlatch)
SR		Control relay shift register
NOP		No operation
END		End program
LDLBL		Load table label used with MOVMC (TI435 only)
MOVMC		Transfer V-memory to/from memory cartridge
RD		Read block from intelligent module
WT		Write block to intelligent module
RX n=X, Y, C, T, CT, GX, V, SP, $		Receive communication
WX n=X, Y, C, T, CT, GX, V, SP, $		Transmit communication
FAULT n=V, K		Show message on display
RSTWT		Reset watchdog timer

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Appendix C
Error Messages

No Error Code
No Message

When you press a key, the MIU display reflects your entry. If there is no message displayed in the MIU and the PWR LED is lit, it is probably caused by electrical noise or a CPU hardware failure. To correct this situation, cycle the system power. If this problem continues, replace the CPU.

E001
Fatal Error

The probable cause of a fatal error is CPU hardware failure. SP51 is on when this error is detected, and the specific error code is stored at address V7755. To clear the error, you should cycle the system power. If the problem persists, replace the CPU.

E003
S/W Timeout

When the program scan time exceeds the software watchdog timer setting, an S/W Timeout error message appears in the MIU display. SP51 is on when this error is detected. The specific error code is stored at address V7755. To clear the error, first check the program. Pay special attention to FOR/NEXT loops and subroutines. Add RSTWT instructions as necessary. You can also increase the watchdog timer setting by using AUX 55.

E004
Bad Instruction
(TI435 only)

This message indicates that memory was changed by electrical noise or by hardware failure. SP44 is on when this error is detected. The specific error code is stored at address V7755. To clear the error, cycle the system power and use AUX 21 to check your program's syntax. Correct the program where necessary. If that does not work, clear the memory and reload your program. If the problem persists, replace the CPU.

E041
CPU Battery Low

If the CPU battery voltage falls below 3 volts, an error message appears in the MIU display. SP43 is on when this error is detected. The specific error code is stored at address V7757. To clear the error message in the display, press CLR. Replace the battery within one week.

E043
CPU MC Battery Low
(TI435 only)

If the memory cartridge battery voltage should fall below 3 volts, this message appears. SP43 is on when this error is detected. The specific error code is stored at address V7757. To clear the error, press CLR. To avoid memory loss, copy the contents of the memory cartridge before replacing the battery.

E099
L Mem Exceeded

When the compiled program exceeds the size of CPU memory, this message is displayed. SP52 is on when this error is detected. The specific error code is stored at address V7755. To clear the error, reduce the length of your program.

E101
No CPU MC
(TI435 only)

This message is displayed when the memory cartridge has failed or is missing from the TI435 CPU. SP44 is on when this error is detected. The specific error code is stored at address V7755. With the power off, install a functioning memory cartridge in the CPU.

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E104 **Write Failed**	This message may be displayed when the memory cartridge being used is write-protected, or when the memory cartridge has failed. To clear the error, first set the jumper inside the memory cartridge to the unprotected position. If that is not successful, replace the memory cartridge.
E151 **Bad Command**	If a parity error is detected in the program memory, this error message is displayed. SP44 is on when this error is detected. The specific error code is stored at address V7755. To clear the error, first correct the corrupted program location. If that is unsuccessful, clear the memory and reload the program. If those actions do not clear the error, replace the memory cartridge.
E155 **RAM Memory Failure** (TI435 only)	This message is displayed to indicate the occurrence of a RAM checksum error. SP44 is on when this error is detected. The specific error code is stored at address V7755. This error may be caused by a low battery, electrical noise or a CPU memory failure. Check the CPU battery and reload your program. If the problem persists, replace the CPU.
E2** **Diag Error AUX 42**	An I/O module error is the probable cause of this error. SP54 is on when this error is detected. Use AUX 42 to determine the specific error.
E201 **Terminal Block Off**	When the terminal strip on an I/O module is loose or missing, this error message is displayed. SP45 is on when this error is detected. The specific error code is stored at address V7756. With the power off, install a terminal strip on the indicated module.
E202 **Missing I/O Module**	If an I/O module is out of place in the base, the MIU display indicates that it is missing. SP45 is on when this error is detected. The specific error code is stored at address V7756. With the power off, install the I/O modules in the correct positions.
E203 **Blown Fuse**	This message indicates the presence of a blown fuse in the output module. SP45 is on when this error is detected. The specific error code is stored at address V7756. With the power off, replace the output module.
E206 **User P/S Failure**	When the output module user power supply voltage is too low, this message appears. SP45 is on when this error is detected. The specific error code is stored at address V7756. To clear the error, adjust or replace the user power supply.
E250 **I/O Chain**	This message is probably caused by a failed base or connecting cable. SP45 is on when this error is detected. The specific error code is stored at address V7755. Check your connections, and, if necessary, replace failed hardware.

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E252 **New I/O CFG**	If the I/O arrangement differs from the configuration stored in the system memory, this error message appears. SP45 is on when this error is detected. The specific error code is stored at address V7755. To clear the error, correct the arrangement of the I/O modules, or use AUX 45 to record the new configuration.
E261 **I/O ADDR Conflict** (TI435 only)	This message appears when overlapping I/O addresses have been manually assigned. SP45 is on when this error is detected. The specific error code is stored at address V7755. Use AUX 46 to correct the I/O configuration.
E262 **I/O Out of Range**	If an out-of-range I/O address is detected in the program, this error message is displayed. SP45 is on when this error is detected. The specific error code is stored at address V7755. To clear the error, correct the I/O address in the program.
E263 **Out of Range** (TI435 only)	When an invalid I/O address is manually configured, this error message appears. SP45 is on when this error is detected. The specific error code is stored at address V7755. Correct the I/O configuration with AUX 46.
E264 **Dup I/O Ref** (TI435 only)	If you use AUX 46 to define the same I/O point twice, this error message is displayed. To clear the error, press CLR, then enter an unassigned I/O point number.
E311 **Comm Error 1**	This message appears when a process code error is detected during MIU communication. SP46 is on when this error is detected. The specific error code is stored at address V7756. To clear the error, first press CLR and retry communication. If that does not work, check the network wiring. If the problem persists, replace the CPU.
E312 **Comm Error 2**	This message appears when a data error is detected during MIU communication. SP46 is on when this error is detected. The specific error code is stored at address V7756. To clear the error, first press CLR and retry communication. If that does not work, replace the MIU. If the problem persists, replace the CPU.
E313 **Comm Error 3**	This message appears when an address error is detected during MIU communication. SP46 is on when this error is detected. The specific error code is stored at address V7756. To clear the error, first press CLR and retry communication. If that does not work, replace the MIU. If the problem persists, replace the CPU.
E316 **Comm Error 6**	This message appears when a mode error is detected during MIU communication. SP46 is on when this error is detected. The specific error code is stored at address V7756. To clear the error, first press CLR and retry communication. If that does not work, replace the MIU. If the problem persists, replace the CPU.

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E320 **Time Out**	If the CPU does not respond to the MIU within a given time, this error message appears. To clear the error, first cycle the system power. If the error message persists, replace the CPU, and, if it still persists, replace the MIU.
E321 **Comm Error**	This error message is displayed to indicate that the CPU did not respond to an MIU request with either an ACK or a NAK. To clear the error, first try cycling the system power. If the problem persists, replace the CPU, and finally, if necessary, the MIU.
E360 **Time Out**	If the device connected to the MIU peripheral port does not respond within the timeout period, this message is displayed. To clear the error, cycle the system power. If the message persists, check the attached device and the cable between it and the MIU.
E4** **No Program**	When a syntax error is detected in the program, this message appears in the display. SP52 is on when this error is detected. The specific error code is stored at address V7755. Use AUX 21 to run a detailed syntax check and to display the specific problem.
E401 **Missing End**	This message appears because your program has no END instruction. SP52 is on when this error is detected. The specific error code is stored at address V7755. Enter an [END] instruction at the end of the main program.
E402 **Missing LBL** (TI435 only)	This error message appears if you use a GOTO instruction without a corresponding label, a GTS instruction without an SBR instruction, or an MOVMC or LDLBL instruction without a DLBL instruction. SP52 is on when this error is detected. The specific error code is stored at address V7755. To clear the error, pair all instructions that require labels with their appropriate matches.
E403 **Missing RET** (TI435 only)	This error message indicates a subroutine within the program that does not end with the required RET instruction. SP52 is on when this error is detected. The specific error code is stored at address V7755. To clear the error, add a RET instruction to the subroutine that needs one.
E404 **Missing FOR** (TI435 only)	Using a NEXT instruction without a corresponding FOR instruction causes this error message to appear. SP52 is on when this error is detected. The specific error code is stored at address V7755. To clear the error, match all FOR/NEXT instruction pairs in your program.
E405 **Missing NEXT** (TI435 only)	Using a FOR instruction without a corresponding NEXT instruction causes this error message to appear. SP52 is on when this error is detected. The specific error code is stored at address V7755. To clear the error, match all FOR/NEXT instruction pairs in your program.

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E406 **Missing IRT**	If there is an interrupt routine in the program that does not end with an IRT instruction, this error message appears. SP52 is on when this error is detected. The specific error code is stored at address V7755. To clear the error, add an IRT instruction to the interrupt routine.
E412 **SBR/LBL>64** (TI435 only)	When the number of SBR, LBL, or DLBL instructions in the program exceeds 64, this message is displayed. It also appears if more than 128 GTS or GOTO instructions are programmed. SP52 is on when this error is detected. The specific error code is stored at address V7755. Reprogram so that there are no more than 64 subroutines.
E413 **FOR/NEXT>64** (TI435 only)	When the number of FOR/NEXT instruction pairs in the program exceeds 64, this message is displayed. SP52 is on when this error is detected. The specific error code is stored at address V7755. Reprogram so that there are no more than 64 FOR/NEXT loops.
E421 **DUP SG REF**	If you use the same number with both an ISG and an SG instruction, this error message appears. SP52 is on when this error is detected. The specific error code is stored at address V7755. To clear the error, reprogram either stage with a different number.
E422 **DUP SBR/LBL** (TI435 only)	If you use the same number with more than one SBR, INT, or LBL instruction, this error message appears. SP52 is on when this error is detected. The specific error code is stored at address V7755. To clear the error, reprogram so that unique reference numbers are used with each subroutine, interrupt routine, or label.
E423 **Nested Loops** (TI435 only)	When two or more FOR instructions are programmed without a NEXT, this message is displayed. SP52 is on when this error is detected. The specific error code is stored at address V7755. To clear the error, reprogram so that FOR/NEXT loops are not nested.
E431 **SG Address**	If a stage is programmed inside a subroutine or interrupt routine, this error message is displayed. SP52 is on when this error is detected. The specific error code is stored at address V7755. To clear the error, delete the stage inside the subroutine or interrupt routine.
E432 **Illegal Jump** (TI435 only)	If the LBL that corresponds to a GOTO instruction is placed after a program's END instruction, an error message is displayed. SP52 is on when this error is detected. The specific error code is stored at address V7755. To clear the error, reprogram the label into the main program.
E433 **SBR Address** (TI435 only)	If you program a subroutine into the main program, this error message appears. SP52 is on when this error is detected. The specific error code is stored at address V7755. To clear the error, relocate the subroutine so that it follows the END instruction.

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E434 **RTC Address** (TI435 only)	This message appears when an RTC instruction is placed in the main program or in an interrupt routine. SP52 is on when this error is detected. The specific error code is stored at address V7755. To clear the error, delete the RTC instruction.
E435 **RT Address** (TI435 only)	This message appears when an RT instruction is placed in the main program or in an interrupt routine. SP52 is on when this error is detected. The specific error code is stored at address V7755. To clear the error, delete the RT instruction.
E436 **INT Address**	This message appears when an INT instruction is programmed into the main program. SP52 is on when this error is detected. The specific error code is stored at address V7755. To clear the error, relocate the interrupt routine so that it follows the END instruction.
E437 **IRTC Address**	This message appears when an IRTC instruction is placed in the main program or in a subroutine. SP52 is on when this error is detected. The specific error code is stored at address V7755. To clear the error, delete the IRTC instruction.
E438 **IRT Address**	This message appears when an IRT instruction is placed in the main program or in a subroutine. SP52 is on when this error is detected. The specific error code is stored at address V7755. To clear the error, delete the IRT instruction.
E440 **Data Address** (TI435 only)	Only ACON or NCON instructions may follow a DLBL. If a non-data instruction is placed in a DLBL, an error message appears. SP52 is on when this error is detected. The specific error code is stored at address V7755. To clear the error, delete the instruction.
E441 **ACON/NCON** (TI435 only)	An error message is displayed if an instruction other than an ACON or NCON is programmed in a DLBL. SP52 is on when this error is detected. The specific error code is stored at address V7755. Delete the instruction to clear the error.
E451 **Bad MLS/MLR**	MLS instructions must be numbered in consecutive, ascending order. An error message appears if an MLS instruction is numbered out of order. To clear the error, number MLS instructions in order.
E452 **X as Coil**	This error message is displayed when an X I/O address is used as an output. To clear the error, reprogram using a Y, C, or GX as the output.
E453 **Missing T/C**	When a timer or counter contact is used with no corresponding timer or counter, this message is displayed. Program timers and counters with the same reference numbers as their contacts.

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E454 **Bad TMRA**	If one of the contacts is missing from a TMRA instruction, this error message appears. Program two contacts before the TMRA instruction.
E455 **Bad CNT**	If one of the contacts is missing from a CNT or UDC instruction, this error message appears. Program two contacts before the CNT instruction or three contacts before the UDC instruction.
E456 **Bad SR**	If one of the contacts is missing from a shift register instruction, this error message appears. Program three contacts before the SR instruction.
E461 **Stack Ovflow**	This error message indicates that more than nine levels of logic have been stored on the stack. Check the use of ANDSTR and ORSTR instructions.
E462 **Stack Unflow**	This error message indicates that an unmatched number of logic levels have been stored on the stack. Match the number of ANDSTR and ORSTR instructions with the number of STR instructions.
E463 **Logic Error**	If an STR instruction is not used at the start of a ladder logic rung, this error message is displayed. Reprogram the rung to begin with a STR instruction.
E464 **Missing CKT**	This error message indicates that a rung of ladder logic is not terminated properly. Add one of the terminating instructions to the rung.
E471 **Dup Coil Ref**	If two or more OUT instructions use the same I/O address, an error message is displayed. To clear the error, use a different I/O address. (This error can be ignored if the duplication was intentional.)
E472 **Dup TMR Ref**	If two or more timers use the same reference number, an error message is displayed. To clear the error, reprogram using unique timer numbers.
E473 **Dup CNT Ref**	If two or more counters use the same reference number, an error message is displayed. To clear the error, reprogram using unique counter numbers.
E501 **Bad Entry**	This message appears if an invalid combination of keystrokes was input before [ENT] was pressed. To correct, press [CLR] and input a correct sequence.
E502 **Bad Address**	This message appears if you enter an out-of-range address. To clear the error, press [CLR] and enter a correct address.
E503 **Bad Command**	This message appears if you enter a non-existent instruction. To clear the error, press [CLR] and enter a valid instruction.

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Error Messages (continued)

E504 **Bad Ref/Val**	This message appears if you enter an invalid number for use with the selected instruction. To clear the error, press CLR and enter a valid number.
E505 **Invalid Inst**	This message appears if you enter an invalid programming instruction. To clear the error, press CLR and enter a valid instruction.
E506 **Invalid Oper**	This message appears if you attempt an operation that is invalid for the MIU. To clear the error, press CLR and enter a valid operation.
E520 **Bad OP-RUN**	An error message appears if the attempted operation is not allowed in run mode. Press CLR and change to the appropriate mode.
E521 **Bad OP-TRUN**	An error message appears if the attempted operation is not allowed in test-run mode. Press CLR and change to the appropriate mode.
E523 **Bad OP-TPGM**	An error message appears if the attempted operation is not allowed in test-program mode. Press CLR and change to the appropriate mode.
E524 **Bad OP-PGM**	An error message appears if the attempted operation is not allowed in program mode. Press CLR and change to the appropriate mode.
E525 **Keyswitch**	The keyswitch must be in the term position before you attempt an MIU operation or an error message appears. Before retrying, press CLR and move the keyswitch to the term position.
E526 **Off-line**	When this message appears in the display, the MIU is set for off-line operation. To select on-line operation, use AUX 64.
E540 **CPU Locked** (TI435 only)	This message indicates that the CPU has been locked against program access. Use AUX 82 to unlock the CPU with your password.
E541 **Wrong Pword** (TI435 only)	If an incorrect password is used with AUX 82 in an attempt to unlock the CPU, an error message is displayed. Press CLR to enter the correct password.
E542 **Pword Reset** (TI435 only)	If an invalid password is detected on power up, the password is reset to 00000000 and an error message is displayed. Press CLR to clear the error. Use AUX 81 to enter a new password, if desired.
E601 **Memory Full**	If you attempt to program an instruction that requires more memory than is available, an error message appears. To clear the error, decrease the size of your program.

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E602 **Inst Missing**	If you attempt a search function without specifying an instruction type, an error message is displayed. To clear the error, enter an instruction type for the search.
E603 **Data Missing** (TI435 only)	If you attempt a search function using AUX 33 on the MIU without specifying an I/O or memory type, this error message is displayed. To clear the error, enter an I/O or memory type for the search with the instruction.
E604 **Ref Missing**	If you attempt a search function using AUX 33 on the MIU without specifying a numeric value, an error message is displayed. To clear the error, enter a numeric value with the I/O or memory type for the search with the instruction.
E610 **Bad I/O Type**	If the program references an I/O module as an incorrect type, an error message is displayed. To clear the error, reprogram to reference the correct module type.
E620 **Out of Mem**	An error message appears if you attempt to transfer more memory data between the MIU and the CPU than the receiving cartridge can hold. Match the transfer size to the memory cartridge size.
E621 **MC Not Blank**	An error message appears if you attempt to write to a memory cartridge that already contains data. Use another memory cartridge or check that the data on the present cartridge is not needed and use AUX 75 to erase a RAM or EEPROM cartridge.
E622 **No MIU MC**	This message appears when a data transfer to the MIU is attempted with no memory cartridge in the MIU. Retry the transfer after you insert a memory cartridge into the MIU.
E623 **System MC**	The memory cartridge installed in the MIU contains system information only, so the requested operation cannot be performed. To clear the error, insert the correct memory cartridge for the desired operation.
E624 **V Mem Only**	The memory cartridge installed in the MIU contains V-memory information only, so the requested operation cannot be performed. To clear the error, insert the correct memory cartridge for the desired operation.
E625 **Prog Only**	The memory cartridge installed in the MIU contains program information only, so the requested operation cannot be performed. To clear the error, insert the correct memory cartridge for the desired operation.

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E626 **PROM MC**	If you attempt to transfer data from a tape to a UVPROM memory cartridge, this error message appears. To clear the error, press [CLR] and make the transfer to a CMOS RAM cartridge in the MIU. Either insert the cartridge itself into the CPU, or transfer the data to CPU memory, insert the UVPROM cartridge into the MIU, and upload the data.
E627 **Bad Write**	This error message indicates that the CMOS or EEPROM memory cartridge is write-protected. Move the write-protect jumper inside the memory cartridge as shown in Chapter 5.
E640 **Miscompare**	If a difference is found when comparing the original data to the memory cartridge after a transfer, this error code appears in the MIU display. Clear the memory cartridge and perform the data transfer again.
E641 **Volume Level**	This message indicates that the volume level of the cassette recorder is set improperly. Press [CLR] and try the tape transfer again.
E642 **Chksum Error**	If an error is detected while data is being transferred into the MIUs memory cartridge, this message appears. Press [CLR] and try the transfer again. If the error persists, replace the memory cartridge or the MIU.
E650 **MIU Sys Error**	This message appears if an invalid internal instruction is detected in the MIU. Press [CLR] and try the operation again. If the error persists, replace the MIU.
E651 **MIU ROM Error**	This message indicates a checksum error from the MIU system ROM. Press [CLR] and try the operation again. If the error persists, replace the MIU.
E652 **MIU RAM Error**	This message indicates an MIU system RAM error. Press [CLR] and try the operation again. If the error persists, replace the MIU.
E653 **MC Batt Low**	When the battery inside the CMOS RAM memory cartridge is low, this message appears. Press [CLR] and replace the memory cartridge battery. (The contents of the cartridge are lost when the battery is changed.)

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Glossary

The following is a list of commonly used PLC terms and their definitions.

AC Input Interface — An input circuit that conditions various AC signals from connected devices, to logic levels that are required by the CPU. This interface may or may not be a module type. Typical voltages for AC inputs include 24 VAC, 115 VAC, and 230 VAC.

AC Output Interface — An output circuit that switches the user-supplied control voltage required to control connected AC devices. This interface may or may not be a module type. Typical voltages for AC outputs include 24 VAC, 115 VAC, and 230 VAC.

Accumulator — Memory location where the CPU stores the intermediate results of an arithmetic or logical operation.

Ambient Temperature — The temperature of the air surrounding a module or system.

Analog — An expression of values that can vary continuously between specified limits.

Analog Device — Apparatus that measures continuous information (e.g., voltage-current). The measured analog signal has an infinite number of possible values. The only limitation on resolution is the accuracy of the measuring device.

Analog Input Interface — An input circuit that employs an analog-to-digital converter to convert an analog value, measured by an analog measuring device, to a digital value that can be used by the CPU.

Analog Output Interface — An output circuit that employs a digital-to-analog converter to convert a digital value, sent from the CPU, to an analog value that controls a connected analog device.

Analog Signal — A signal that varies continuously and smoothly over a given range, rather than switching between fixed levels as with discrete signals.

AND — A Boolean operation that yields a logic 1 output if all inputs are 1, and a logic 0 if any input is 0.

Address — A location in the PLC's memory.

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ASCII	American Standards Code for Information Interchange. It is a seven-bit code with an optional parity bit used to represent alphanumerics, punctuation marks, and control code characters.
Battery Backup	A battery or set of batteries that provides power to CPU memory only in case of a system power outage.
Battery Low	A condition that exists when the backup battery voltage drops low enough to require battery replacement. Generally, an indicator or status bit signals this condition.
BCD	See Binary Coded Decimal.
Binary	A numbering system using only the digits 0 and 1. Also called base 2.
Binary Coded Decimal	A binary number system in which each decimal digit from 0 to 9 is represented by four binary digits (bits). The four positions have a weighted value of 1, 2, 4, and 8 respectively starting with the least significant bit. A thumbwheel switch is a BCD device, and when connected to a programmable controller, each decade requires four wires. Decimal 9 = 1001 BCD.
Bit	1. Binary Digit; the smallest unit of information in the Binary Numbering System, represented by the numbers 0 and 1. 2. The smallest division of a PLC word.
Boolean Algebra	Math and/or logical relationships of binary numbers.
Byte	A sequence of eight binary digits (bits) usually operated as a unit.
Character	One symbol of a set of elementary symbols, such as a letter of the alphabet or a decimal number. Characters may be expressed in many binary codes. For example, an ASCII character is usually a group of 7 bits.
Chip	A small piece of semiconductor material on which microscopic electronic components are photo-etched to form one or more circuits. After connection leads and a case are added to the chip, it is called an Integrated Circuit.
Circuit Card	A printed circuit board containing electronic components.
CMOS	Abbreviation for Complementary Metal Oxide Semiconductor. An integrated circuit family characterized by low power consumption and high noise immunity.

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Contact	1. One of the conduction parts of a relay, switch, or connector that is engaged or disengaged to open or close the associated electrical circuits. 2. In reference to software, the juncture point that provides a complete path when closed.
Contact Symbology	A set of symbols used to express the control program using conventional relay symbols (e.g., –| |– normally open contact, –|/|– normally closed contact, and -( )-coil).
Current Loop	A two wire communication link in which the presence of a 20 milliamp current level indicates a binary 1 (mark), and its absence indicates no data, a binary 0 (space).
Current Sink	A device that receives current.
Current Source	A device that supplies current.
Decimal Number System	A number system that uses ten numeral digits (decimal digits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9). Each digit position has a place value of 1, 10, 100, 1000, and so on, beginning with the least significant (right-most) digit. Also called base 10.
Counter	In relay-panel hardware, an electromechanical device that can be wired and preset to control other devices according to the total cycles of one ON and OFF function. In a PLC, a counter is internal to the PLC; i.e., it is controlled by a user-programmed instruction. A counter instruction has greater capability than any hardware counter. Therefore, PLC applications do not require hardware counters.
CPU	Central Processing Unit. This is the physical unit that contains the PLC's intelligence, usually a microprocessor device.
Debugging	Process of detecting, locating, and correcting mistakes in hardware (system wiring) or software (program).
Diagnostic Program	A test program to help isolate hardware malfunctions in the programmable controller and application equipment.
Discrete Digital Signal	This value can either be a 1 or a 0, depending on the field device connected to it.
Documentation	An orderly collection of recorded hardware and software data such as tables, listing, diagrams, etc., to provide reference information for PLC application operation and maintenance.

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Downtime	The time when a system is not available for production due to required maintenance.
Edit	To deliberately modify the user program in the PLC memory.
EPROM	Erasable (user) Programmable Read-Only Memory. A memory chip that can be reprogrammed several times.
EEPROM	Electrically Erasable Programmable Read-Only Memory. An EEPROM can be cleared with an electrical signal. After being cleared, it can be reprogrammed.
Execution	The performance of a specific operation by processing one instruction, a series of instructions, or a complete program.
Execution Time	The total time required for the execution of one specific instruction.
Field Devices	Input devices, such as pushbutton switches, relay contacts, etc., that provide information to the PLC, and output devices, such as motor starters, solenoids, lamps, etc., that perform PLC tasks.
Hardware	The mechanical, electrical, and electronic devices that compose a programmable controller and its application.
Hexadecimal Number System	A number system that uses the numerals 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, and the letters A, B, C, D, E, F to represent numbers and codes. Also called base 16.
Image Register	An area in memory where the on or off state of each input and output is stored for use by the program between I/O updates.
Initial Stage	The segment of a machine stage program where execution starts when the CPU is switched to run mode.
Initial Devices	Any connected equipment that supplies information to the central processing unit such as control devices (e.g., switches, buttons, sensors), or peripheral devices (e.g., CRT, manual programmer). Each type of input device has a unique interface to the CPU.
Instruction	A command or order that causes a PLC to perform one certain prescribed operation.
Instruction Set	The set of general-purpose instructions available with a given controller. In general, different machines have different instruction sets.

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Interfacing	Interconnecting a PLC with its application devices and data terminals through various modules and cables. Interface modules convert PLC logic levels into external signal levels, and vice versa.
I/O	Abbreviation for Input/Output.
I/O Address	A unique number assigned to each input and output. The address number is used when programming, monitoring, or modifying a specific input or output.
I/O Module	That part of the PLC where field devices are connected. It isolates the CPU from electrical noise. It is a plug-in type assembly that contains more than one input or output circuit. A module usually contains two or more identical circuits. Normally 2, 4, 8, 16, or 32 circuits.
I/O Optical Isolation	Isolation that is achieved by a light-emitting diode transferring light energy to the base of a transistor.
I/O Scan	The time required for the PLC to monitor all inputs and control all outputs. The I/O scan repeats continuously.
I/O Scan Time	The time required for the PLC to monitor inputs and control outputs.
I/O Update	The continuous process of revising each and every bit in the I/O tables, based on the latest results from reading the inputs and processing the outputs according to the control program.
I/O Update Time	The time required to update all local and remote I/O. Also called I/O scan.
Jump	A transition to another stage in the program. A jump deactivates the current stage and activates the stage being jumped to.
K	1. An abbreviation for kilo. In computer language, it usually relates to 1024 words of memory. 2. A symbol denoting constant data in TI405 programming.
Ladder Diagram	An industry standard for representing control logic relay systems.
Language	A set of symbols and rules for representing and communicating information (data) among people, or between people and machines.
Latching Relay	A relay with two separate coils, one of which must be energized to change the state of the relay. It remains in either state without power.
Least Significant Bit (LSB)	The bit that represents the smallest value in a nibble, byte, or word.

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Least Significant Digit (LSD)	The digit that represents the smallest value in a byte or word.
LED	Abbreviation for light-emitting diode. A semiconductor diode, the junction of which emits light when passing a current in the forward direction. LEDs are used as diagnostic indicators on various controller hardware components.
Limit Switch	An electrical switch actuated by some part and/or motion of a machine or equipment.
Location	A storage position in memory.
Logic	A means of solving complex problems through the repeated use of simple functions that define basic concepts. Three basic logic functions are AND, OR, and NOT.
Logic Diagram	A drawing that represents the logic functions AND, OR, NOT, etc.
Machine Stage Program	A machine control program that combines relay ladder logic and the sequential function programming elements called stage.
Memory	A grouping of circuit elements that have data storage and retrieval capability.
Microprocessor	An electronic computer processor section implemented in relatively few IC chips (typically LSI) that contains arithmetic, logic, register, control, and memory functions.
Millisecond (ms)	One thousandth of a second: 10^{-3} or 0.001 second.
Module	A plug-in electronic subassembly.
Most Significant Bit (MSB)	The bit that represents the greatest value in a nibble, byte, or word.
Most Significant Digit (MSD)	The digit that represents the greatest value in a byte or word.
NEMA Standards	Consensus standards for electrical equipment approved by the members of the National Electrical Manufacturers Association (NEMA).
NEMA Type 5	A category of industrial enclosures intended for indoor use to provide a degree of protection against dust, falling dirt, and dripping non-corrosive liquids. They do not provide protection against conditions such as internal condensation.

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Network	A grouping of PLC instructions that controls one or more outputs. This is represented as one section of a logic ladder diagram. Also referred to as a rung.
Noise	Random, unwanted electrical signals, normally caused by radio waves or electrical or magnetic fields generated by one conductor and picked up by another.
Noise Immunity	The ability to function in the presence of noise.
Noise Spike	A noise disturbance of relatively short duration.
Nonretentive	Logic status of contact is cleared to zero when power is cycled off/on.
Nonretentive Output	An output that is continuously controlled by a program rung. Whenever the rung changes state (true or false), the output turns on or off. Contrasted with a retentive output that remains in its last state (on or off) depending on which of its two rungs, latch or unlatch, was last true.
Normally-closed Contact	1. A relay contact-pair that is closed when the coil of the relay is not activated, and opens when the coil is activated. 2. A ladder program symbol that allows logic continuity (flow) if the referenced input is logic 0 when evaluated.
Normally-open Contact	1. A relay contact-pair that is open when the coil of the relay is not activated, and closes when the coil is activated. 2. A ladder program symbol that allows logic continuity (flow) if the referenced input is logic 1 when evaluated.
Nonvolatile Memory	A storage device that does not lose its information while its power supply is turned off.
NOT	Inverts the logical status of selected input, output, or control relay.
Octal Number System	A number system that uses eight numeral digits (octal digits 0, 1, 2, 3, 4, 5, 6, 7). Also called base 8.
One's Complement	A binary value formed when each 0 in the original value is replaced with a 1 and each original 1 is replaced with a 0.
OR	Permits user to enter contacts in parallel.
Output	Information transferred from PLC through output modules to control output devices.

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Output Devices	Any connected equipment that receives information or instructions from the CPU, such as control devices (e.g., motors, solenoids, alarms, etc.) Each type of output device has a unique interface to the CPU.
PLC	Abbreviation for Programmable Logic Controller.
Peripheral Equipment	Units that may communicate with the programmable controller, but are not part of the programmable controller; e.g., teletype, cassette recorder, CRT terminal, tape reader, etc.
Positive Logic	The use of binary logic in such a way that 1 represents a positive logic level (e.g., 1 = +5 V, 0 = 0 V). This is the conventional use of binary logic.
Pressure Switch	A switch that is activated at a specified pressure.
Printed Circuit	A board on which a predetermined pattern of printed connections has been formed.
Processor	A unit in the programmable controller that scans all the inputs and outputs in a predetermined order. It is also known as the CPU. The CPU monitors the status of the inputs and outputs in response to the user-programmed instructions in memory and it energizes or de-energizes outputs as a result of the logical comparisons made through these instructions. In the form of an integrated circuit, it may be called a microprocessor.
Program	A sequence of instructions to be executed by the PLC CPU to control a machine or process.
Program Scan	The time required for the PLC CPU to execute all instructions in the program once. The program scan repeats continuously. The program monitors inputs and controls outputs through the Input and Output Image Registers.
Programmable Controller	Also known as Programmable Logic Controller or PLC. A solid-state control system that has a user programmable memory for storage of instructions to implement specific functions such as: I/O control logic, timing, and counting. A PLC consists of a CPU, input/output interface, memory, and programming device that typically uses relay-equivalent symbols. A PLC is purposely designed as an industrial control system that can perform functions equivalent to a relay panel or a wired solid-state logic control system.
Programmer	A device for entry, examination, and alteration of program and storage areas in the PLC's memory.
PROM	Abbreviation for Programmable Read-Only Memory. A digital storage device that can be written into only once but continually read.

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RAM	A Random Access Memory in an addressable Large Scale Integration (LSI) device used to store information in microscopic flip-flops or capacitors. Each may be set to an ON or OFF state, representing logical 1 or 0. This type of memory is volatile; memory is lost while power is off unless battery backup is used.
Read	To sense the presence of information in some type of storage, that includes RAM memory, magnetic tape, punched tape, etc.
Relay	An electrically operated device that mechanically switches electrical circuits.
Relay Logic	A representation of the program or other logic in a form normally used for relays.
Retentive	Logical status of contact is retained when power is cycled off/on.
ROM	A Read-Only Memory is a digital storage device specified for a single function. Data is loaded permanently into the ROM when it is manufactured. This data is available whenever the ROM address lines are scanned.
RS-232-C	An EIA standard, originally introduced by the Bell System, for the transmission of data over a twisted-wire pair, less than 50 feet in length. It defines pin assignments, signal levels, etc., for receiving and transmitting devices. Other RS-standards cover the transmission of data over distances in excess of 50 feet.
RS-422	An EIA standard for the electrical characteristics of balanced voltage digital interface. Maximum distance is 4000 feet.
Rung	A grouping of PLC instructions that controls one or more outputs. This is represented as one section of a logic ladder diagram. Also referred to as a network.
Scan Time	The time necessary to completely execute the entire PLC program one time.
Self-diagnostic	The hardware and instructions within a controller that allows it to continuously monitor its own status and indicate any fault that might occur within it.
Sequential Function Chart	A flow diagram that illustrates the individual steps needed to complete one cycle of a machine's operation.
Software	The user program that controls the operation of a programmable controller.

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Solid-state Devices (Semiconductors)	Electronic components that control electron flow through solid materials such as crystals; e.g., transistors, diodes, integrated circuits.
Stage	A program segment that executes only when made active by another stage.
Stage Action	Operations that are performed while the stage is active.
Stage Number	A unique number that identifies each stage and allows it to be referenced by other stages in the program.
Startup	The time between equipment installation and the full operation of the system.
State	The logic 0 or 1 condition in PLC memory or at a circuit's input or output.
Storage	Synonymous with Memory.
System	A collection of units combined to work as a larger integrated unit having the capabilities of all the separate units.
Thumbwheel Switch	A rotating switch used to input numeric information into a controller.
Timer	In relay-panel hardware, an electromechanical device that can be wired and preset to control the operating interval of other devices. In a PLC, a timer is internal to the CPU, that is to say it is controlled by a user-programmed instruction. A timer instruction has greater capability than any hardware timer. Therefore, PLC applications do not require hardware timers.
Transition Condition	When this condition is met, a jump to another stage in the program occurs.
Truth Table	A table that describes a logic function by listing all possible combinations of inputs and by indicating the outputs for each combination.
Two's Complement	A binary value formed by adding 1 to the one's complement of the original value.
UV Erasable PROM (UVPROM)	An ultraviolet erasable PROM is a programmable read-only memory that can be cleared by exposure to intense ultraviolet light. After being cleared, it may be reprogrammed.
Volatile Memory	A storage device that loses its information if power is removed from it.
Word	A grouping or a number of bits in a sequence that is treated as a unit and is stored in one memory location.

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Word Length	The number of bits in a word. In a PLC, these are generally only data bits. One PLC word equals 16 data bits.
Write	The process of loading information into memory.

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