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Signatec FAST PRODUCTS For an Impatient World

Product Information Sheet

PDA12A

125 MHz WAVEFORM DIGITIZER



FEATURES

- Bandwidth from DC-50 MHz
- 512k or 2Meg Sample memory on board
- Memory expandable to 500 Megasamples
- 250 megabytes/sec data transfer rate over Signatec Auxiliary Bus (SAB)
- Two channel simultaneous sampling at 62.5MHz
- 12 bit resolution
- PCI compatible board

APPLICATIONS

- Radar
- Mass Spectroscopy
- Mass Spectrometry - Time of Flight
- Communications
- Ultrasound
  Medical Diagnostics / Non Destructive Testing
- Laser Doppler Velocimetry
- High Speed Waveform Capture

The PDA12A is a PCI compatible board which offers high resolution waveform capture at higher speeds than have previously been possible. With 12 bits of resolution and a signal bandwidth from DC to 50 MHz, the PDA12A is useful for a wide range of applications which require capturing signal information with a wide dynamic range at multi-megahertz frequencies. The PDA12A is available with 512k or 2M of 12 bit sample memory.

Two signal channels are implemented on the PDA12A allowing two signals to be sampled simultaneously at rates up to 62.5 megasamples per channel. The clocks can also be offset by 180 degrees so that the data from the two channels may be interleaved to obtain a single channel running at 125 megasamples per second. Each channel has either 256k or 1M 12 bit samples. The single channel mode allows the total amount of memory to be available on one channel, or to interleave the data from two converters to yield an effective sampling rate of twice the individual converters.

The PDA12A is equipped with multiple acquisition and trigger modes. For single event acquisitions the PDA12A is equipped with a single shot mode allowing pretrigger, normal or delayed trigger storage. For multi-trigger acquisitions segmented or gated triggering is possible. The PDA12A is equipped with an on board counter providing trigger event time stamping in the segmented mode. Delayed and pretrigger features may also be used when acquiring segmented data.

Multiple PDA12A boards can be connected in a Master/ Slave configuration via a 20 conductor ribbon cable at the top of the board. This allows for data sampling to be synchronized between one Master and up to three Slave PDA12A boards.

The PDA12A incorporates the Signatec Auxiliary Bus (SAB) with data transfer rates up to 250 megabytes per second to other peripherals for storage or processing. The SAB allows for high speed data transfers to large memory boards (such as MEM500) or fast processor boards (such as SP20 or PMP8).

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HARDWARE DESCRIPTION

Mechanization

The functional block diagram for the PDA12A is shown below. Two separate signal channels are implemented. The input signal coupling is DIP switch selected for AC or DC coupling and applied to four scaling amplifiers that determine the four input voltage ranges. The output from one of the four amplifiers is selected via the multiplexer. An offset voltage is summed with the signal to shift the level of the signal to the ADC. The offset range is sufficient to shift the signal at the ADC by ± 1/2 of full scale. For example, if the 3 volt range is selected, the input signal must not exceed 3 volts peak to peak in a -3 to +3 volt window.

The filter is a 3 pole Bessel filter with a cutoff frequency of 54 MHz. Due to the frequency response of other components in the signal path the actual system bandwidth is typically 50 MHz as measured using the ADC output data.

In the single channel mode, when sampling at the maximum rate, the analog signal from channel 1 is connected to the input of both ADCs and the clocks are operated 180 degrees out of phase. This results in interleaved data that yields an effective digitizer rate of 125 MHz. In single channel mode with a sampling rate less than maximum, only one ADC is used and the RAM interface directs the samples from the channel 1 ADC to both banks of RAM, allowing the entire memory to be used for one channel. For two channel operation the analog signal from each input is connected to separate ADCs which are clocked simultaneously.

The PDA12A is equipped with two low jitter internal clock sources of 125 and 100 MHz as well as an external clock input. For slower sampling frequencies an on-board divider is provided to skip data samples stored in memory to yield a division from 2 to 128 in factors of 2. The external clock connector can be used for an output clock which is synchronous with the digitizer clock.

Operating Modes

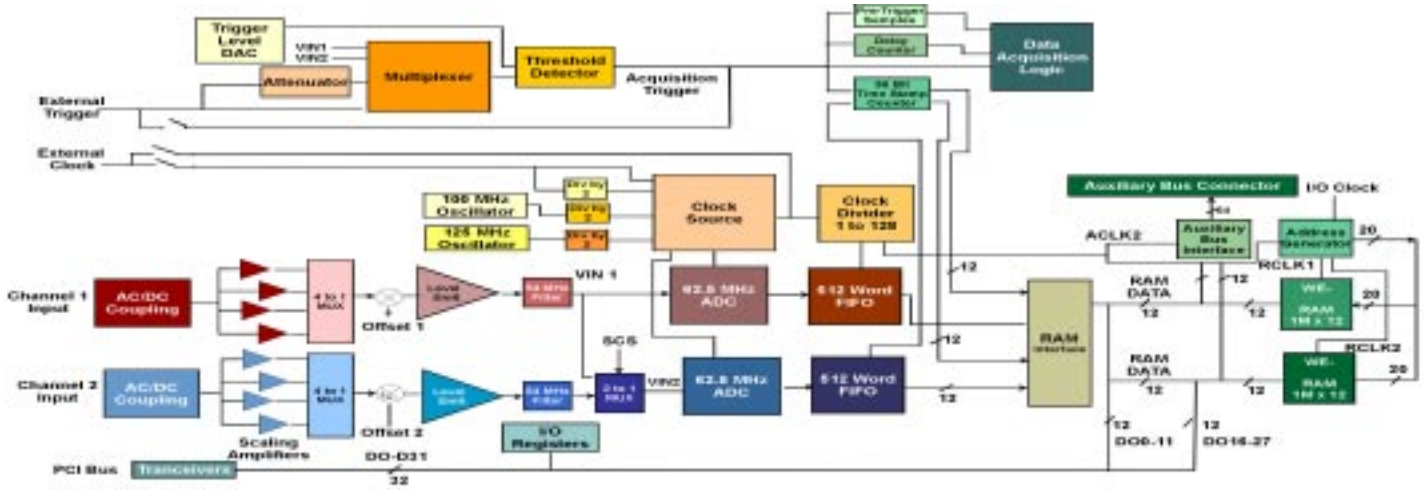
The PDA12A has 8 operating modes as follows: Off, Standby, Acquisition #1 (normal), Acquisition #2 (to SAB), Acquisition #3 (to PCI), Data Transfer #1 (to PCI bus), Data Transfer #2 (to SAB), RAM write.

The Off mode powers down most of the circuitry on the PDA12A board to reduce power consumption when the board is not in use. Acquisition mode #1 stores data samples in the on-board signal memory to be transferred later to the PC. In Acquisition mode #2 data output is directly to the SAB. Acquisition mode #3 acquires data directly to the PCI bus to be stored in system memory. In this acquisition mode the maximum sampling rate is limited by the ability to store the data samples in system memory.

Two triggering modes and four trigger methods are provided on the PDA12A. The trigger modes are single shot and segmented modes. In the single shot mode, following the detection of a trigger signal, all of the active memory is filled. In the segmented mode a separate trigger signal is required to successively fill each memory segment until all of the active memory is filled. The trigger method determines the relationship of the stored data samples to a trigger event. The trigger methods provided are pretrigger, delayed trigger, gated trigger, and time stamping. Pretrigger acquisitions allow a specified number of samples which occur prior to the trigger event to be stored in either trigger mode. Delayed trigger acquisitions allow a software programmable number of samples to be disregarded after the trigger event and before data storage begins in either trigger mode. Gated triggering allows data storage to start and stop directly under the control of the trigger level in the single shot mode. Time stamping allows the value of the on-board 36 bit counter to be stored on each trigger event when using the segmented mode. The trigger source selection can be channel 1, channel 2 or external.

PCI Interface

The PDA12A is a 32 bit 5 Volt PCI board that is “Plug and Play” compatible. Each PDA12A installed in a system can be uniquely identified by the board serial number that can be read from the board through the PCI bus. The control and monitoring registers of the PDA12A are accessed from the PCI bus with 32 bit I/O transfers. The PDA12A is capable of becoming a PCI Bus Master allowing data to be transferred using 32 bit burst direct memory access (DMA) transfers. The PDA12A is capable of transferring one 32 bit word on each PCI bus clock cycle, theoretically making it possible to transfer data at the maximum rate of the PCI bus. The actual transfer rate realized in a system will be less than this and is dependent upon the host system. Signal data can also be transferred using 16 bit memory transfers using standard software functions.



PDA12A Simplified Block Diagram

SOFTWARE, SYSTEM, AND PERFORMANCE DETAILS

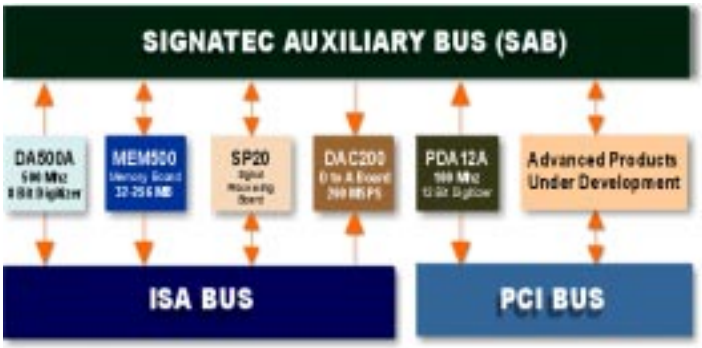
Software

A library of C language functions and a device driver for Windows95 and WindowsNT 3.51/4.0 is supplied with the PDA12A, making it easy to create custom applications without writing extensive code. A DOS and a Windows based application example program are also supplied. These programs can be used to provide a quick and easy method of checking the PDA12A board operation and features. All source code is supplied so users may compile the code using any C language compiler.

System Capabilities

Signatec offers a range of products incorporating the SAB. These boards act as the modular building blocks for constructing high performance systems that mechanize a wide variety of applications. Figure 3 shows the present product groups that are available.

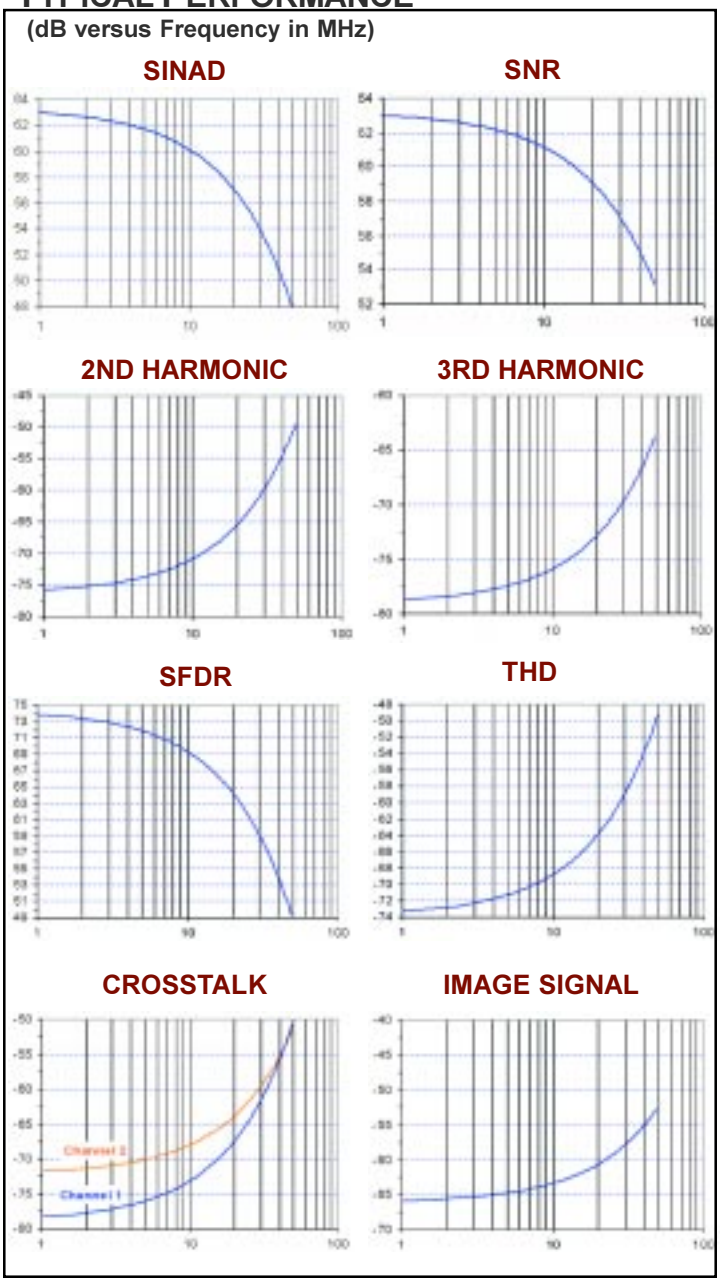
DSP Products can perform as a SAB Bus Controller that manages board operations and data flow on the bus. This allows an integrated acquisition system to accomplish multiple acquisition, transfer, and processing cycles without PC intervention, thereby maximizing system performance.



SAB and Supporting Products

TYPICAL PERFORMANCE

(dB versus Frequency in MHz)



DEFINITION OF TERMS

SINAD - Signal to Noise and Distortion: The ratio of the fundamental sinusoidal signal power to the total noise and distortion component power.

SNR - Signal to Noise Ratio: The ratio of the fundamental sinusoidal signal power to the noise power.

SECOND HARMONIC DISTORTION - The ratio of the power at twice the fundamental frequency to the power of the fundamental sinusoid.

THIRD HARMONIC DISTORTION - The ratio of the power at three times the fundamental frequency to the power of the fundamental sinusoid.

SFDR - Spurious Free Dynamic Range: The ratio of the fundamental sinusoidal power to the power of the next highest spurious signal. Normally the highest spurious signal is the second or third harmonic.

THD - Total Harmonic Distortion: The ratio of the total power of the second and third harmonics to the fundamental sinusoidal power.

CROSSTALK - With a signal applied to one of the channels, this is the ratio of the signal captured on the undriven channel to the signal on the driven channel. The graph indicates the undriven channel.

IMAGE SIGNAL - An unwanted spurious signal occurs at the Nyquist frequency minus the signal frequency when multiple data converters are interleaved as a result of any mismatch between the converters. On the PDA12 this applies for 125 MHz and 100 MHz acquisitions only. The amplitude plot is the ratio of the spurious power level to the signal power level.

Test Method

A digitally synthesized signal source is used and performance is tested at 1.004, 5.04, 12.05, 24.7, and 49.1 MHz. Bandpass filters are used to insure a clean signal source. Signal amplitude is 95% of full scale and the digitizer clock setting is 50 MHz. Measurements are made using a 4096 point FFT with a Blackman-Harris window. The first 10 bins to represent the DC term, 43 bins centered around the peak for the fundamental signal power, 9 bins centered at two and three times the fundamental for the second and third harmonic. All other bins are considered noise.

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PDA12A ELECTRICAL SPECIFICATIONS AND ORDERING INFORMATION

SPECIFICATIONS

Input Signals

Channel 1 Analog Input
Channel 2 Analog Input
External Trigger (in/out)[1]
External Clock (in/out)[1]
Connectors : SMA (4)

Analog Inputs

full scale voltage : 100 mV p-p to 3.0 V p-p
impedance : 50 ohms
bandwidth : DC to 50 MHz
coupling : AC or DC[1]

Frequency Response

gain flatness, dc - 10 Mhz : ± 0.1 dB
-3 dB bandwidth : 50 MHz

Voltage Ranges

full scale value (peak-peak) : 100mV, 300mV, 1.0V, 3.0V
selection : digital, 2 bits

DC Offset Voltage

8 bit DAC each channel, full scale

External Trigger[2]

impedance[3] : 2k ohms
trigger level[3] : ± 1.5 Volts, ± 0.5 Volts[4]
adjustment method[3] : 8 Bit DAC
coupling[3] : DC

External Clock[5]

impedance[3] : 50/2k ohms[1], 100 ohm ECL[1]
signal[3] : sine wave or square wave
coupling[3] : AC
amplitude[3] : 500mV p-p to 5V p-p
frequency[3] : 10 to 62.5 MHz or 20 to 125 MHz[6]
output clock[7] : Channel 1 ADC clock (TTL)
output clock frequency : 62.5 MHz or 50 MHz[8]

Trigger Modes

Single Shot : single trigger fills active memory
Segmented : trigger needed for each memory segment

Trigger Methods

Pretrigger : samples prior to trigger are stored; 0 to 512 samples in steps of 8
Delayed trigger : delay from trigger to data storage; 0 to 65536 digitizer clock cycles
Gated Trigger : samples stored only when trigger above/below threshold depending on trigger slope.
Time Stamp : 36 bit counter value stored in first 4 bytes of data RAM on trigger.
: counter clock is ADC #1 clock divided by 1,2,4, or 8.

Special Channel Mode

Clock Divider = 0 : Interleaved acquisition at two times clock source (effective rate=125 or 100 MHz)
Clock Divider > 0 : Ch. 1 data fills RAM for both channels

Digitizer

resolution : 12 bits
clock oscillator : 62.5 or 50 MHz
clock divider : 1 to 128
aperture jitter : 1pS RMS
full scale input voltage : 1V p-p

Memory

size : 512k or 2M samples
start address settings[9] : 0 to memory size in steps of 2
end address settings[9] : 0 to memory size in steps of 16
addressing[10] : via Memory Mapping or DMA
memory address (PC) : Plug and Play selected

I/0 Addressing

PCI controller address : 64 bytes, Plug and Play selected address
control/status registers : 32 bytes, Plug and Play selected address

Signatec Auxiliary Bus (SAB)

Data Transfer Modes : 64 bit two channel
: 32 bit two channel
: 32 bit channel 1
: 32 bit channel 2
data transfer rate : 250 Megabytes/sec,125Mega Samples/sec
data direction : output only

Interrupts

source : Acquisition complete
: End of DMA transfer
Interrupt (IRQ) used : Plug and Play selected

Power Requirements

+12V : 100 mA max.
-12V : 20.0 mA max.
+5V : 3.2 Amps max. (Normal Operation)
: 0.4 Amps max. (Off Mode)

Absolute Maximum Ratings

Ambient Temperature : 0 to 50°C
Input Signal Voltage : ±4 volts

ORDERING INFORMATION

PDA12A Board

512 sample memory Part number: PDA12A-512k
2 Meg sample memory Part number: PDA12A-2M

SAB Cables

Refer to the "SAB Cable Assembly Ordering Guide" to select and order the appropriate cable assemblies.

Master-Slave Cables

The PDA12A is configured to operate as a Master or a Slave via jumpers on the board which can be changed by the user. In order to operate in a Master/Slave configuration a 20 pin ribbon cable is required to connect multiple boards. This cable is ordered using the basic part number PDA12 MS-X where X is the total number of boards connected together. Master/Slave boards must occupy adjacent slots. The maximum number of boards to be connected is one master and three slaves. The part number for this connector is : PDA12MS-4.

Documentation & Accessories

The PDA12A is supplied with a comprehensive operators manual which thoroughly describes the operation of both the hardware and the software. Also supplied are two four foot coaxial cables with BNC to SMA connectors. Extra cables may be purchased from Signatec. Supplied software disks contain a DOS function library for Borland C, Windows 95/NT function libraries for Borland and Microsoft Visual C/C++, example programs, and all source code to libraries and examples.

Customer Support

Customer Support and Software Updates can be obtained from Signatec's Web Page www.signatec.com, e-mail address techsupport@signatec.com or by calling Signatec at (909) 734-3001.

Product Warranty

This product carries a full 3 year warranty. During the warranty period, Signatec will repair or replace any defective product at no cost to the customer. This warranty does not cover customer misuse or physical damage not reported within 15 days of the time of shipment by Signatec.

Notes:

1. Selected via DIP switch.
2. External Trigger Connector is selected as an input trigger or an output trigger synchronous with the start of data storage using a DIP switch.
3. Applies only when used as input.
4. Selected by software controlled High/Low level trigger.
5. External Clock connector is selected as a clock input or an output clock which is synchronous the digitizer clock using a DIP switch.
6. Clock source selection includes option for additional divide by 2 for the external clock for use in single channel mode. Without divider range is 10-62.5 MHz, with divider range is 20-125 MHz. This divider is independent of the clock divider setting.
7. Applies only to External Clock as output.
8. Clock frequency equal to specified clock source.
9. Active memory for acquisition is end address minus start address.
10. Memory is mapped into a 8k byte window of PC memory which can be read with standard 'C' memory manipulation functions. The memory can also be transferred using high speed 32 bit PCI burst DMA transfers.

Signatec reserves the right to make changes in this specification at any time without notice. The information furnished herein is believed to be accurate, however no responsibility is assumed for its use. Data Sheet Revision Date: 08/31/98.

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