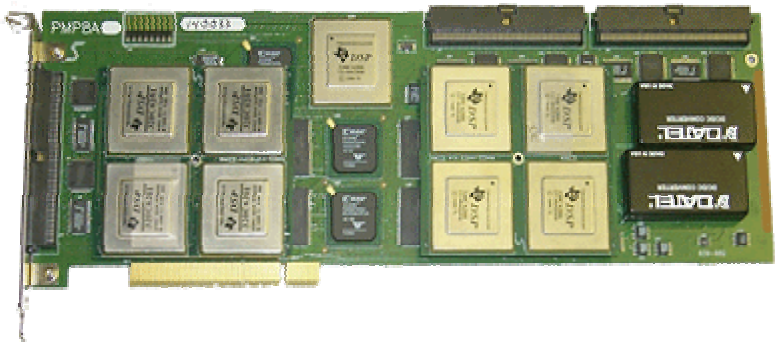
Signatec FAST PRODUCTS For an Impatient World

Product Information Sheet

PMP8A

High Throughput Digital Signal Processor



With Fixed Point or Floating Point Processors !!

OVERVIEW

Performance
- Up to 14.4 GIPS or 7.7 GFLOPS Peak Processing Power
- Continuous Input Data Processing up to 500 MB/s

Applications
- Real Time Processing
- Fast Database Searches
- Image Analysis
- Digital Video
- All High-Data-Throughput Applications

Features
- Absolutely the Highest Performance DSP Board
- Parallel Processing with up to 9 TI DSPs
- C6201 (Fixed Point), or C6701 (Floating Point)
- Unique Program Execution Processor for Dynamic Thread Allocation
- Advanced Parallel DSP Software Simplifies Coding
- Application Specific Customizable Hardware
- Boundary Scan Self-Test Pinpoints Problems
- 870MB/s External I/O via 3 Interfaces
- 1600MB/s Internal I/O via Switching Network
- 32-bit PCI Local Bus Full-Length Board

The PMP8A is a parallel processing DSP board that features incredible processing power and ultra-high data throughput capability. This is facilitated by the internal mechanization of the PMP8A, which utilizes multiple high-speed buses combined with cross-point port switching to connect “anything to anything” at full parallel bus bandwidth. Due to the throughput and processing power of the PMP8A, many processes that were previously performed “off line” can now be performed in REAL TIME.

The unique PMP8A architecture incorporates a “master” DSP called the Program Execution Processor (PEP) and options of four or eight "slave" DSPs. These are mounted four to a daughter card called a "Quad DSP Array" or QDA. QDAs are available as either floating point or fixed point units that incorporate either the TMS320C6701 or C6201 digital signal processors.

Both the C6701 and C6201 processors employ Very Long Instruction Word (VLIW) technology and have been optimized for a C programming environment. In the PMP8A mechanization, all slave DSPs execute program *threads* which are allocated dynamically. Dynamic allocation maximizes DSP utilization.

There are three data interfaces on the PMP8A. The Signatec Auxiliary Bus (SAB) can sustain a transfer rate of 500 megabytes per second. Signatec offers a range of products with SAB interfaces for data acquisition, data storage, and signal generation.

The Signatec External Bus (SEB) interface is a 32-bit implementation of the SAB. Using a bracket-mounted connector, this interface is used to connect to devices external to the host computer or to interconnect up to 8 PMP8A boards. The host PCI bus is the third interface and can sustain a transfer rate in excess of 100 MB/s. Data transfer over the three interfaces can occur simultaneously.

The PMP8A Software Development System makes parallel processor programming easier than ever before. The PMP8A Software Integrator seamlessly connects development tools from Signatec, Texas Instruments, and Microsoft into a user- friendly environment running under Windows NT/2000 or Windows95/98. A preprocessor splits and translates the user’s simple C source code program into code to be run on the PEP and DSPs. Other unique features of the system include whole board profiling and whole board debugging.

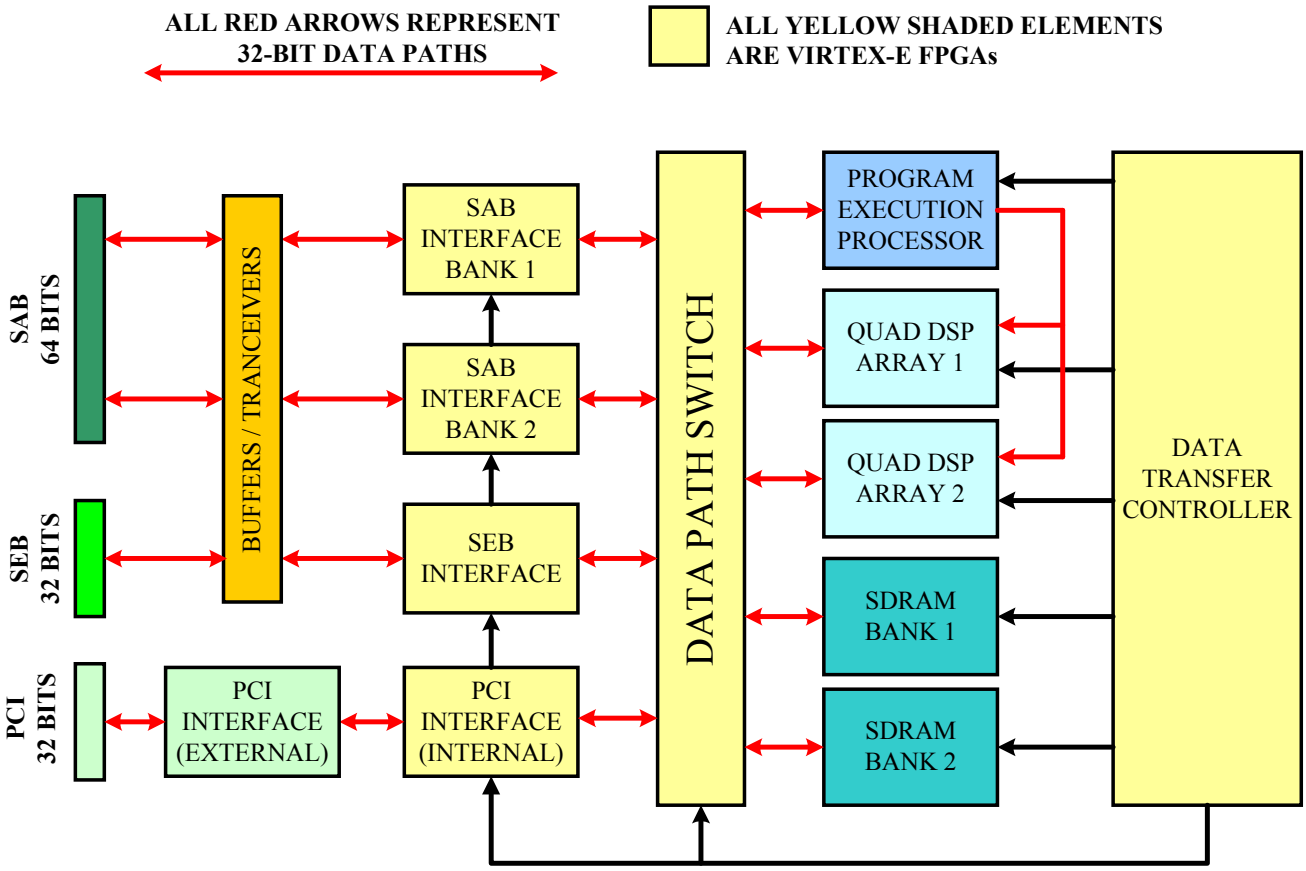
Two important new features have been added to the PMP8A: customizable hardware and Boundary Scan testability. These features are described in detail in the next section.

HARDWARE DESCRIPTION

OVERVIEW

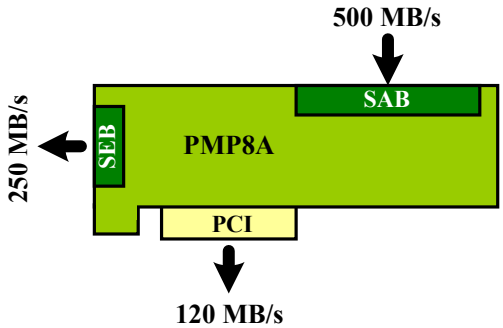
The PMP8A is a parallel processing board designed to provide both maximum data flow and maximum processing power. The data flow is provided by three high-speed buses and multiple internal data paths. The processing power is supplied by eight Digital Signal Processors referred to as the processing core and arranged as two Quad DSP Arrays. A ninth DSP called the Program Execution Processor, or PEP, manages all data flow via the Data Transfer Controller (DTC) and dynamically directs the execution of program *threads* on the core processors. PMP8A Versions are available with one or two QDAs and also with none (PEP only).

PMP8A Data Flow Block Diagram



THE INTERFACES

Each of the three external interfaces employs deep FIFOs so that the internal operation of the board may be largely asynchronous with respect to external bus activity. This is important in maximizing the operational efficiency of the PMP8A. Shown below is a typical high-throughput mechanization whereby data flows in from the SAB and out over the PCI and/or the SEB.



A High Data Flow Mechanization

Signatec Auxiliary Bus (SAB) Interface

The PMP8A implements SAB version 3. This bus is designed to connect up to eight boards via two 100-conductor high-density ribbon cables along the top of the boards. Data widths of 32 and 64 bits are supported with a maximum sustained transfer rate of 500 Mbytes/s. Packetized Data Transfers are supported. See the SAB Data Sheet and SAB Specification for details.

The PMP8A can operate as a SAB controller to direct the operation of other SAB boards, independent of the host PCI bus and operating system. This greatly improves throughput in data acquisition and signal processing systems. Signatec produces a variety of compatible SAB products for data acquisition, data storage, and signal generation.

HARDWARE DESCRIPTION

Signatec External Bus (SEB) Interface

The PMP8A implements the Signatec External Bus. This is a 32-bit implementation of the SAB for external connections. Up to 8 devices may be connected via a 100-conductor high-density ribbon cable. The I/O connector is located on the mounting bracket of the PMP8A. The SEB can transfer data at peak rates up to 250 MB/s. Besides its primary use as a connection to external devices, it can also be used as a high-bandwidth connection between multiple PMP8A boards or as a connection to other PC based boards implementing the SEB specification.

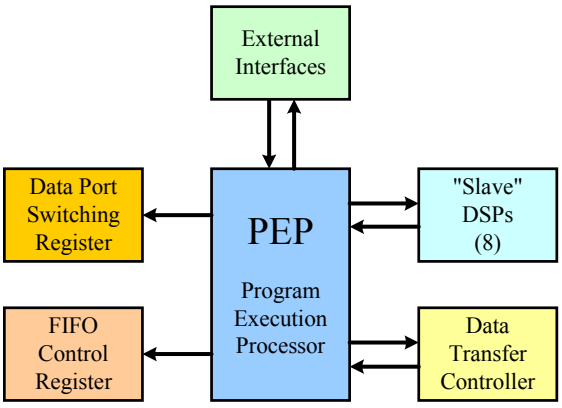
PCI Interface

The PMP8A is a 32-bit peripheral designed and tested per the PCI Local Bus Specification Revision 2.1. It is fully PCI Plug and Play compatible. Systems with a Plug and Play BIOS will automatically reconfigure the PMP8A into available address space. The PCI interface is used both to download code to the DSPs and to transfer data. It has a peak transfer rate of 133 MB/s with a sustained rate of over 100 MB/s.

DATA PROCESSING ELEMENTS

Program Execution Processor (PEP)

The PEP mechanization makes it possible for the PMP8A to combine power with simplicity. The PEP is a C6201 DSP. Although fully capable of executing program code, its main objective is to dynamically allocate the program *threads* (C functions) to the array DSPs and to manage data transfer via the Data Path Switch and Data Transfer Controller.



PEP Control

The PEP controls the execution of a program by writing control words to the FIFO Control Register and the Data Path Switch Register to configure those devices for an impending data transfer. The transfer is initiated by writing a control word to the Data Transfer Controller.

Control words written to the "slave" DSPs indicate the function to be executed and supply necessary parameters. Interrupts received from the DTC and DSPs indicate the end of a transfer and the end of a function execution respectively. The functional hardware blocks are comprised of highly complex circuitry. However, the PEP's control of this circuitry has been made simple and intuitive.

Quad DSP Arrays (QDA)

QDAs are installed as daughter card assemblies. The four DSPs on each QDA module share a common local data bus with connectivity to the port switch as shown in the PMP8A block diagram. With floating point QDAs, all processors (including the PEP) operate with a 160 MHz clock and the data transfer rate between devices is 320 MB/s. With fixed point QDAs all processors operate with a 200 MHz clock and the data transfer rate is 400 MB/s.

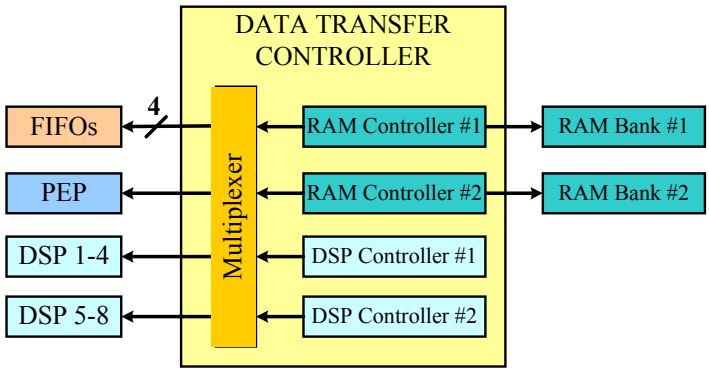
SDRAM

The PMP8A contains two banks of synchronous DRAM, each containing 32 megabytes, and each having its own controller. In 64-bit SAB transfers from a single source, the upper 32 bits are typically transferred to RAM initially and then transferred to the appropriate DSP.

DATA TRANSFER ELEMENTS

Data Transfer Controller (DTC)

There are three types of devices involved in the internal data flow: the interface FIFOs, SDRAM, and the DSPs. The Data Transfer Controller provides the control signals for implementing data transfers between these devices. The following types of transfers are supported: RAM ↔ FIFO, RAM ↔ DSP, DSP ↔ FIFO, and DSP ↔ DSP.



DTC Mechanization

The DTC contains 2 RAM Controllers and 2 NR (not-RAM) Controllers. RAM Controller #1 is used for any transfer involving RAM Bank #1, RAM Controller #2 is similarly used with RAM Bank#2, and either NR Controller can be used for DSP ↔ DSP, DSP ↔ FIFO, or FIFO ↔ FIFO transfers.

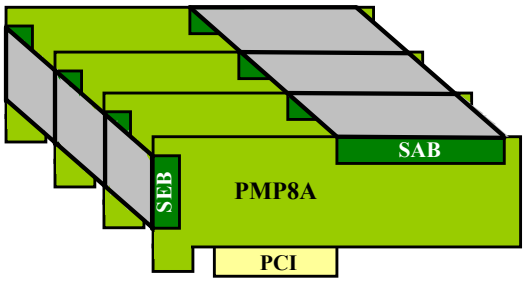
Data Path Cross Point Switching (DPSW)

The DPSW has nine 32-bit ports that connect to the primary data elements as shown in the PMP8A block diagram. Any element can be connected to any other element and up to 4 simultaneous connections are possible, each transferring data at the maximum rate which is 400 MB/s for fixed point QDAs or 320 MB/s for floating point.

PERFORMANCE ISSUES

Expanding to Multiple Boards

The processing power of a system is expanded with multiple boards connected via the SAB and SEB. Typically, input data would flow in via the SAB and the SEB would be used to synchronize the operations of the boards to act as a single virtual unit. This is accomplished through PEP to PEP communication between boards.



Interconnected PMP8A Boards

Frame Transfers

Data transfers within the PMP8A typically occur as 1k-word data frames. The use of frames maximizes the utilization of the internal bus bandwidth and provides a method for quickly responding to devices in need of immediate service. An Almost Full flag in a bus interface indicates that insufficient space is available to write a full frame of data into the FIFO. Similarly, an Almost Empty flag indicates when there is less than one full frame of data to be read.

Concurrent DMA

The DMA transfer capability of the C6x DSPs allows data transfer to be concurrent with the internal DSP processing. The PEP operating system takes advantage of this capability by transferring the next input data set to a DSP while it is still processing its present data set.

Boundary Scan

Boundary Scan Technology allows thousands of component pins on the board to be either injected with test signals or to have the signals available at those points read out. Test signals are supplied via a serial scan chain that is driven from the PCI bus or a parallel port connection. This provides a self-test capability that not only detects a malfunction but also reports its probable cause. If a failure were to occur, this feature will reduce the product down-time, thus increasing its *availability*.

SOFTWARE DESCRIPTION

OVERVIEW

Writing software to operate parallel processors has traditionally been a complex undertaking. The PMP8A Software Development System is designed to make it as simple as possible to create an executable application. The PMP8A Software Integrator provides unique development and optimization environments with innovative tools for creating and debugging an application.

Despite the high-performance nature of the PMP8A hardware configuration, it surprisingly lends itself to a software mechanization that is unique, easy-to-use, and efficient, especially for a parallel processing system.

The PMP8A operation consists of 8 (or 4) DSPs that process program *threads* as directed and a master DSP designated as the Program Execution Processor (PEP). The primary tasks for the PEP are to dynamically distribute the *threads* and to manage all data flow.

The PEP executes *main,* which consists of processor function calls (program threads) and data transfer functions. The PEP may also execute some processing functions, although this is typically kept to a minimum and usually consists of those functions relating to the assimilation of data from the multiple processors. (In the single processor configuration of the PMP8A the PEP obviously will perform all processing.)

We use the term *thread* to be consistent with generally accepted usage. In the PMP8A world, a *thread* is a C function. In some applications, this function will be the entire computational process to be applied to a data set.

SOFTWARE INTEGRATOR

The PMP8A Software Integrator ties together a number of software components from Signatec, Texas Instruments, and Microsoft. It provides a true Windows interface for the TI Tools and supplies a quick link to the text editing and compiler/linker facilities of the Microsoft C environment. The Integrator consists of a Development Environment, a Debugging Environment, and an Optimization Environment.

SOFTWARE DESCRIPTION

DEVELOPMENT ENVIRONMENT

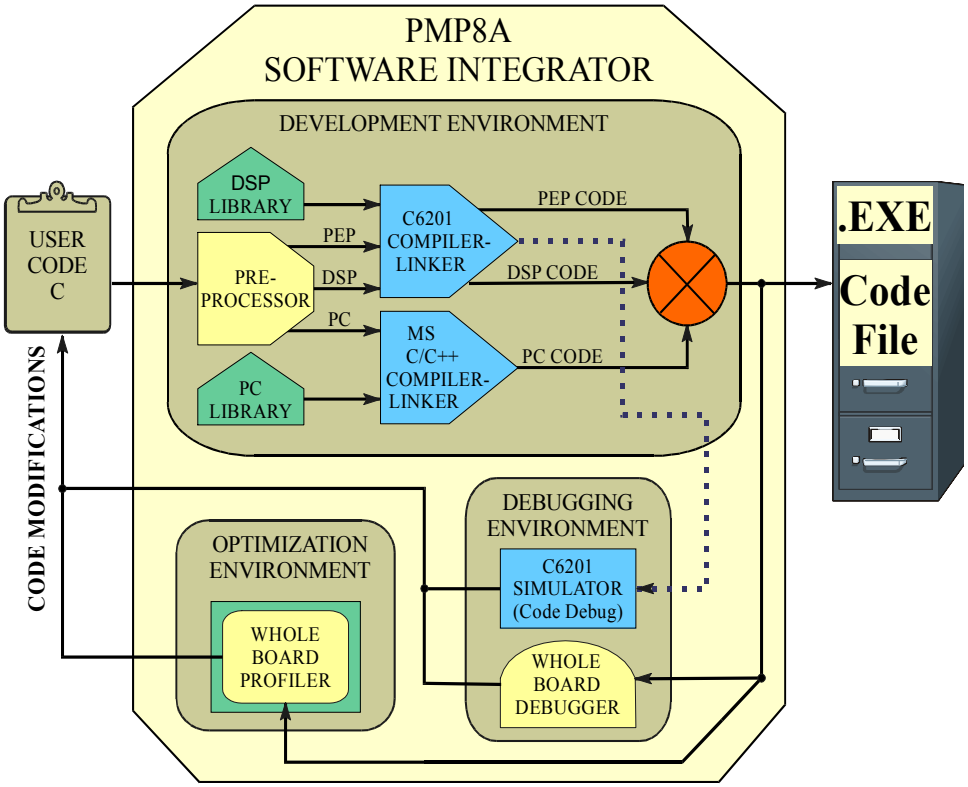
User programs are written in C and contain source code for both the PMP8A and for the PC. The PMP8A code looks very similar to any other C program that runs on a single processor. It consists mostly of data transfer function calls (from the DSP Library) and processing function calls to the DSPs.

The Preprocessor

The Preprocessor is a key element of the development environment. It splits and translates user source code into 2 types: PEP code and DSP code. The PEP and DSP source code is compiled by the C6201/C6701 compiler contained in Code Composer Studio and linked to the DSP library to create the executable code for the PEP and the DSPs.

The Preprocessor performs extensive code translation of the user code to convert it into a form where executable functions are allocated to available core DSPs in a manageable fashion. Directives may also be placed into the source code to provide control over the code generation.

Software Integrator Functionality



DEBUGGING ENVIRONMENT

Simulator and Code Level Debugging

Once a function compiles without error, the TI Simulator within Code Composer Studio is used for debugging to ensure it produces the desired results. All standard code-debugging features are available. Execution cycle counts provide valuable code partitioning information.

Whole Board Debugging

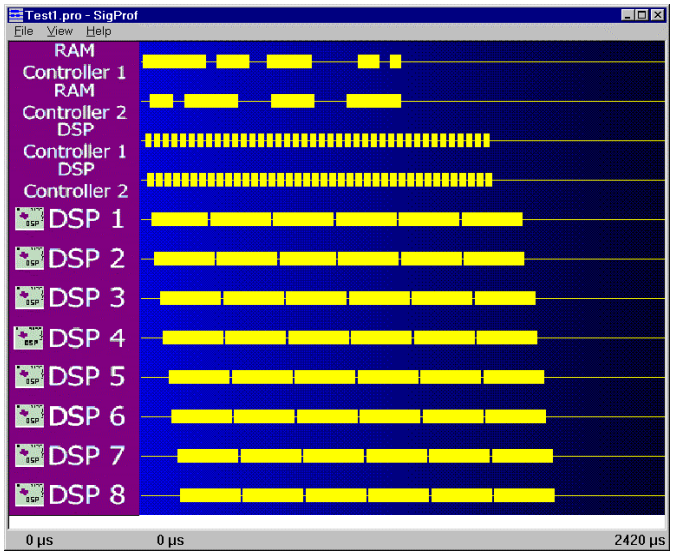
Whole board debugging is primarily used to inspect data and register information at the natural board-level breakpoints. These natural breakpoints occur at the end of every data transfer and at the end of every processed *thread.* At each breakpoint all processing activity may be interrupted. This can be useful in establishing the execution relationship between processors and to inspect data flow into and out of processes.

OPTIMIZATION ENVIRONMENT

Whole Board Profiler

The Whole Board Profiler provides a visual representation of processor and bus activity as a time line. We call it "whole board" to distinguish it from other profilers that provide information only on the internal operation of a single processor. Profile information can be displayed any time the processing is stopped or paused. Time is displayed horizontally and the time window can be scrolled.

Because of the PMP8A's unique mechanization, the PEP is able to gather profiling information at all times without degrading the execution performance of the program. When running a program from the Integrator, it is therefore possible to pause at any time and view the profiling data.



Whole Board Profiler

The Profiler provides utilization information on the 4 data controllers and the 8 core DSPs. The solid bars show when data is being transferred over the four connection paths or when data is being processed by a particular DSP. The space between bars represents inactivity. This information is used to determine execution bottlenecks, possible causes, and potential solutions.

SOFTWARE DESCRIPTION

THE COMPLETE DEVELOPMENT CYCLE

1. Write code for processing functions.
2. Compile code with Code Composer Studio C6000 compiler via the Integrator.
3. Use TI Simulator in Code Composer Studio to debug functions to attain desired performance.
4. Write code for *main*.
5. Use Compiler to determine that *main* has no errors.
6. Write, compile, and link the PC program code.
7. "Build" the program. The Preprocessor translates the code for *main* and the called functions. The translated code is compiled and linked. The executable code for the PEP and core DSPs is combined into a single file.
8. Use the Whole Board Debugger to verify the program with real data flow.
9. Use the Whole Board Profiler to determine how effectively board resources are utilized.

SOFTWARE DEVELOPMENT SYSTEM CONTENTS

The PMP8A Software supports code development and board operation under Windows NT/2000 or Windows 95/98. Most applications require some level of interaction between code executing on the PMP8A and code executing on the PC. All PC software supplied by Signatec for the PMP8A is written in Microsoft Visual C/C++. All DSP software is written for and compiled with Texas Instruments' Code Composer Studio for the TMS320C6201/6701 DSP.

The complete software system contains the following items:

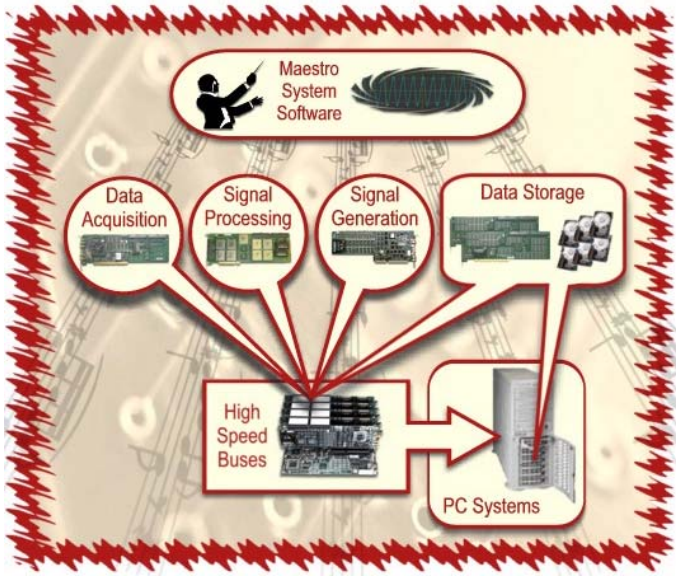
1. Signatec Support
   - Software Integrator
   - DSP Function Library with Source Code
   - PC Function Library with Source Code
   - Windows Device Drivers for 95/98 and NT/2000
2. TI Code Composer Studio with Compiler, Linker, Debugger
3. Microsoft Visual C/C++ (for PC Code)
4. Linux Drivers & Software

Signatec's PMP8A Software is provided free of charge. TI software is sold separately (see our price list). Signatec does not supply Microsoft software.

MISCELLANEOUS INFORMATION

THE SIGNATEC SYSTEM SOLUTION

Signatec is the only company providing leading edge products for signal and data analysis in four key product areas: Data Acquisition, Signal Processing, Signal Generation, and Data Storage. Additionally, all products incorporate the Signatec Auxiliary Bus (SAB) providing data transfers up to 500 MB/s.



Signal Processing products (including the PMP8A) can act as a SAB controller. As such, they can control the operation of all boards on the bus without using the host bus. This bypasses host operating system latencies and host bus bottlenecks.

Signatec can supply multi-card systems in an industrial PC platform with up to 20 full-length slots and plenty of power and airflow for cooling.

DETAILED PMP8A DISCUSSION

For a more detailed discussion of some of the unique features of the PMP8A, the article "A Discussion of the Advanced DSP Technologies Employed in the PMP8 Parallel DSP" is available on the Signatec Web Site or can be supplied upon request.

SPECIFICATIONS AND ORDERING INFORMATION

SPECIFICATIONS

General

Board Type:	Full length, +5v, 32-bit PCI Local Bus
DSP type:	Texas Instruments TMS32C6201
Clock Speed:	200 MHz (supports C6201 QDAs) 160 MHz (supports C6701 QDAs)
DSP Memory: [1]	64k bytes Program RAM, 64k bytes Data RAM

TMS320C6201 DSP

Type:	32-Bit Fixed Point
Architecture:	Very Long Instruction Word (VLIW)
Performance:	1.6 GIPS Peak (@200 MHz)

TMS320C6701 DSP

Type:	32-Bit Floating Point
Architecture:	Very Long Instruction Word (VLIW)
Performance:	0.96 GFLOPS Peak (@160 MHz)

MEMORY

All Models:	Two banks of 8Meg x 32 SDRAM

PCI Interface

PCI Local Bus Specification:	Revision 2.1
Memory Addressing:	Plug-n-Play selectable
I/O Addressing:	Plug-n-Play selectable
FIFO Depth:	4k x 32bit words
Data Width:	32, 16 Bits
Data Transfer Rate:	100-125 Mbytes/s
Host Interrupt:	Via PCI Interface
PCI Master:	PMP8A Initiated DMA Transfers
PCI Target:	Supported

Signatec Auxiliary Bus Interface [2]

Bus Specification:	SAB, version 3
Transfer Method:	Clock & Data via FIFO
FIFO Depth:	8k words
Data Width:	32/64 bits
Data Transfer Rates (MB/s):	500@64 bits, 250@32 bits

Signatec External Bus Interface [3]

Transfer Method:	Clock & Data via FIFO
FIFO Depth:	8k words
Data Width:	32 bits
Data Transfer Rate:	250 Mbytes/s peak

Power Requirements [4]

+5V (from PCI Local Bus):	2.8 Amps maximum
+12V:	3.0 mAmps maximum
+3.3V:	1.3 Amps maximum

Absolute Maximum Ratings

Ambient Temperature:	0 to 50° C

Notes:

1. Internal to each DSP
2. A complete specification for the SAB is available via Signatec web site: www.signatec.com or phone direct for a hard copy.
3. A complete specification for the SEB is available via Signatec web site: www.signatec.com or phone direct for a hard copy.
4. For PMP8A-2

ORDERING INFORMATION

PMP8A	(PEP only, supports C6201 QDA modules only)
PMP8A-1	(PEP plus one C6201 QDA module)
PMP8A-2	(PEP plus two C6201 QDA modules)
PMP8A-F	(PEP only, supports C6701 QDA modules only)
PMP8A-1F	(PEP plus one C6701 QDA module)
PMP8A-2F	(PEP plus two C6701 QDA modules)

SAB Cables

Refer to the "SAB Cable Assembly Ordering Guide" to specify the appropriate cable assemblies.

SEB Cables

Refer to the "SAB Cable Assembly Ordering Guide" to specify the appropriate cable assemblies.

Code Composer Studio

Refer to the TI website for more information.

Documentation & Accessories

The PMP8A is supplied with a comprehensive Operators Manual that thoroughly describes the operation of both the hardware and the software, as well as appropriate software disks.

Customer Support

Sales and product information can be obtained by calling Signatec at (909) 734-3001. Technical Support can be obtained from the Signatec web site at: www.signatec.com

Product Warranty

This product carries a full three-year warranty. If the product is found to be defective during the warranty period, Signatec will repair or replace it at no cost to the customer. This warranty does not cover customer misuse, abuse, or modification of the product or physical damage not reported within 15 days of the time of shipment by Signatec.

Data Sheet Revision Date: 09-23-2003. Check Signatec Web Site for latest revision and possible application notes.