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Find the *Silicon Control PMC650-1* at our website: *Click HERE*

PCI650 PMC650 CPCI650 Bus Analyzers

Analyzer

Exerciser

Stimulus

Anomaly

Performance

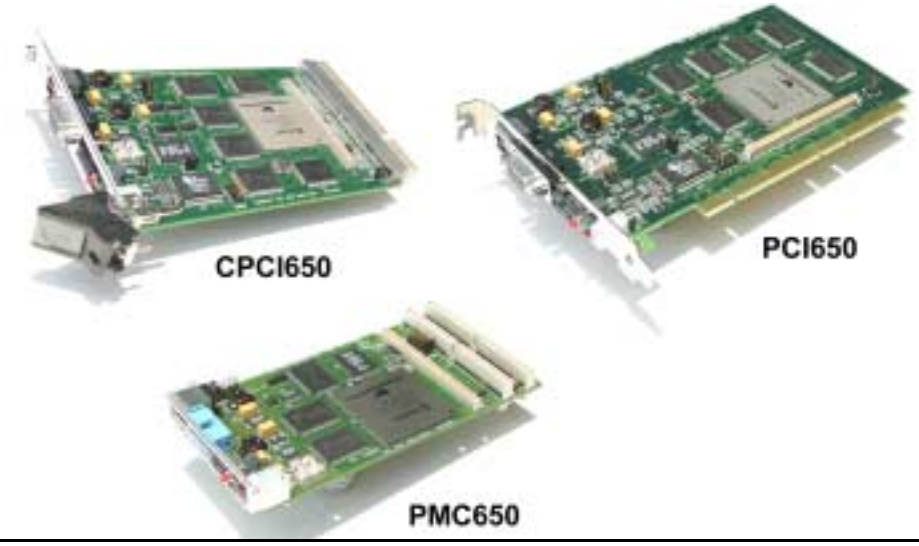
Windows SW

API Interface

USB

RS232

Ext. Power



6 5 0 System Analyzer / Exerciser

Silicon Control Inc. introduces the ultimate analyzer and exerciser for PCI, PMC and Compact PCI systems. The 650 family of analyzers represent our 3rd generation PCI analyzer combining high performance hardware with a sophisticated and intuitive software interface. The result is a powerful diagnostic tool for bus analysis - all on a single plug-in card.

The PCI650 analyzer provides a multitude of functions to help you analyze your system.

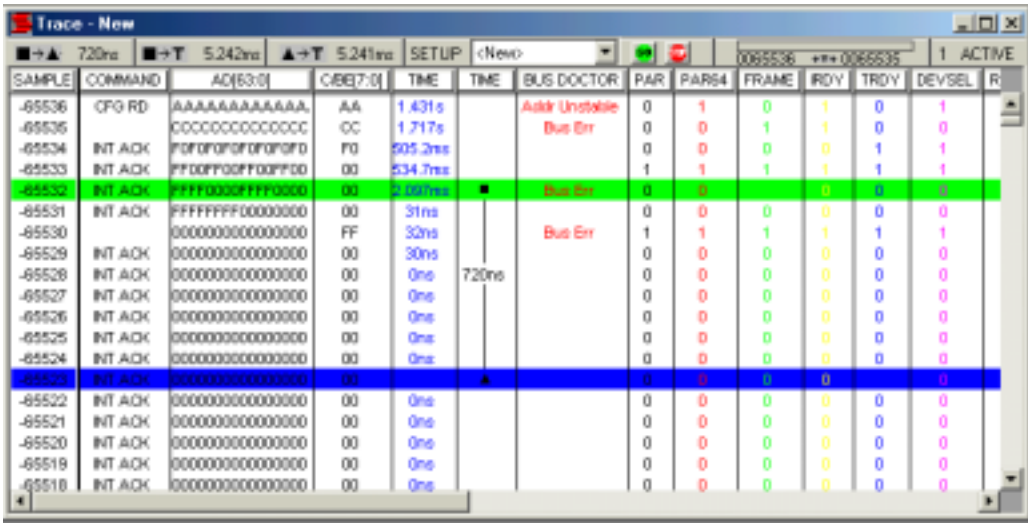
- Capturing bus activity using sequential triggers and filters
- Exciser to perform memory, I\O and configuration cycles
- Stimulus generation for hardware simulation
- Anomaly detection of protocol and timing violations
- Performance analysis of utilization, transfer rates, latency, statistics

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PCI650 State Analysis

State analysis captures bus activity and presents each transaction in an easy to read configur-able display



State Display

The state display presents each PCI signal in column form. Signals can be moved, inserted, deleted and color and radix defined. Grouped signals such as address can be collapsed and expanded and their range specified.

Decoded Signals
These predefined signals interpret information on the bus to assist in understanding activity. They are treated like any other signal in the state display.

Defined Signals
These signals or group of signals are defined by the user who assigns a name to a given bus pattern.

Sampling

The PCI650 has 3 basic sampling modes to capture bus activity for state analysis;
CLOCK—every system clock
SYNC—address and data only
TRANSFER—complete cycles

Triggering

Triggers define when the analyzer captures bus activity. Once a trigger is encountered activity can be observed before and after the trigger event. The position of the trigger can be moved within the trace buffer controlling how much data is before or after the trigger event. Triggers can be simple or complex.

Simple trigger
Any PCI signal or combination of signals.

Logically Combined Triggers
Any logical combination of simple triggers using operators such as AND, OR, NOT, Exclusive OR.

Sequential Triggers
This type of trigger is formed by a number of bus events occurring in a specified order. To accomplish this levels are defined. Each active level controls the analyzers operation based on bus events. Jumps to other levels provide complex sequences.

Filtering

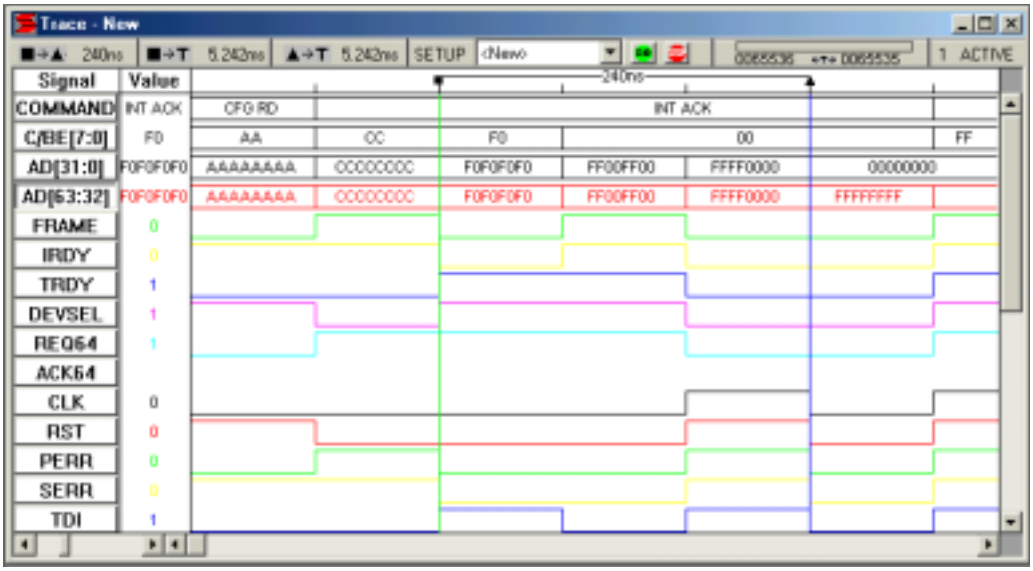
Trace filtering defines which events are captured and stored in the analyzers trace buffer. This filtering of data provides only events which are of interest to you.

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PCI650 Timing Analysis

The timing display shows the relation-ship of bus signals and time measure-ments



Timing Display

The timing display represents trace data as waveforms for timing analysis. A numeric value is provided on top of each waveform. As in the state display, signals can be moved, inserted, deleted and color and radix defined. Grouped signals such as address can be collapsed and expanded and their range specified. A zoom is provided to get a better look at waveform relationships.

Sampling

The PCI650 has a precision oscillator used to sample the bus at periodic intervals for timing analysis. The sample rate is selected by the user.

Time Measurements

Cursors can be placed on the timing and state display to measure time between the trigger and a cursor and the time between 2 cursors. Times are shown at the top of the display and in the trace window.

Status Indicators

At the top of the display a status indicator shows the number of samples captured before and after the trigger and the current state of the analyzer.

Capture Control

GO and STOP icons control when tracing starts and halts.

Setup Wizard



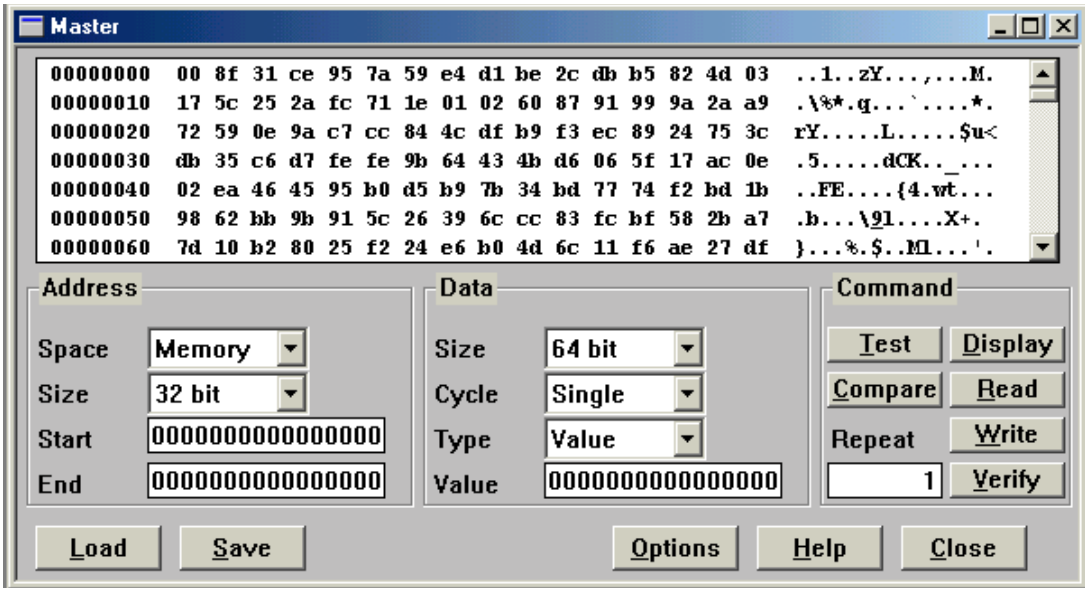
To assist in setting up the analyzer for state and timing analysis a Setup Wizard automatically programs the analyzer based on what the user wants to look at. Once a setup is defined it can be saved and later loaded.

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PCI650 Exerciser

The user can initiate memory, I/O and configuration cycles as well as scan configuration space and stimulate the bus



Exerciser

The exerciser performs 3 main functions:

1. Initiator
2. Stimulus Generator
3. Configuration Scan

Initiator

The initiator performs PCI reads and writes to memory, I/O and configuration space. The user has complete control over many aspects of the transfer including:

- Address Space
- Address Width
- Data Width
- Single or Burst
- Write Data Value

The data from a read or write can be obtained from a file or the user. When data is read to the display it is shown in both hex and ASCII. Special tests can be performed including reading and writing test patterns, comparing and verifying data and repeating cycles.

Stimulus

The PCI650 has the ability to generate signal patterns on the PCI bus. These features provide hardware simulation and test system response to events.

Stimulus is driven onto the bus under control of a 16 level sequencer. At each level any combination of bus signals can be specified along with an activation time and wait time synchronized to the system clock. These levels can then be linked together to form complex stimuli. Initiation of this stimulus can be controlled manually or in response to a bus event.

Configuration Scan

An automatic scan of configuration space identifies the boards in a system and displays the configuration information.

A search is performed of all configuration registers and the results are displayed and decoded for easy identification.

The values of the configuration registers are displayed in one window and the decoded meaning in another window.

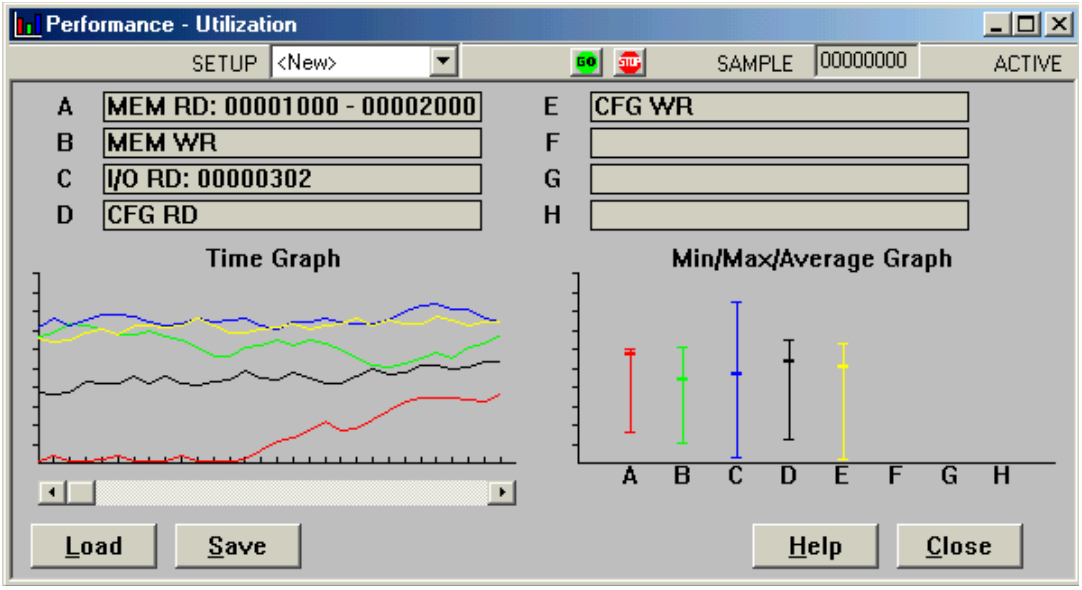
Vendor names, type of board, version numbers, etc. are displayed for easy interpretation.

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PCI650 Performance

Time graphs and histo-grams give you an over-view of sys-tem perform-ance, bottle-necks and problem areas



There are 5 types of performance measurements that are made in real time with dedicated hard-ware:

- Bus Utilization
- Transfer Rate
- Latency
- Burst Distribution
- Statistics

Bus Utilization

This measurement identifies the resources that are using the bus. These can include address usage, command type and overall idle and busy times.

Transfer Rate

The transfer rate measurement measures in MB/s the speed of data transfers. These measure-ments can be specified for spe-cific address ranges and cycles.

Latency

The efficiency of data transfers in a system depend upon the laten-cies involved. Measurements are taken of master, target, address, data and arbitration to provide a look at latencies that slow a bus down.

Burst Distribution

The amount of data transferred during each cycle is measured and displayed in 8 ranges. The ranges include single byte transfers and up.

Statistics

Statistics can be obtained for any bus signal or group of signals. For example the number of memory reads, memory writes, writes to an address or address range can be counted.

Performance Display

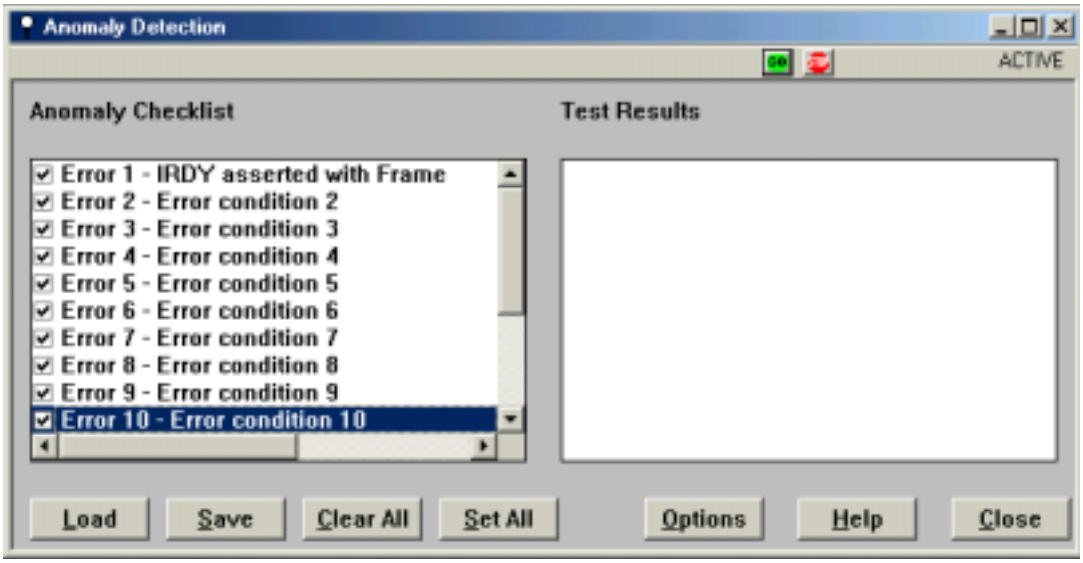
The performance display consists of a moving time graph and an average/min/max bar or pie chart. The time graph shows the current measurement and is updated at fixed time intervals specified by the user. The bar chart averages this moving data and tracks the min and max values. A scroll bar under the time graph lets you re-view the previous data.

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PCI650 Anomaly Detection

Protocol and timing violations are automatically detected and displayed



Automatic Anomaly Detection

The PCI650 continuously monitors and detects over 100 protocol and timing violations. Dedicated hardware checks setup and hold times, unstable signals and glitches on lines. Protocol checking screens for illegal signal assertions referenced to the PCI specification.

Anomaly Display

The anomaly display is divided into 2 windows;

1. Anomaly Checklist
2. Test Results

Anomaly Checklist
The anomaly checklist window allows selection of specific tests. Set All and Clear All buttons are provided to select all the tests and clear all the tests. The checklist can be saved and later loaded.

Test Result Window
After starting the anomaly test the result window displays all violations detected. The user can scroll through these results as well as save them to a file.

State/Timing Display

During state and timing analysis violations are stored in the trace buffer as selected in the checklist. A description of the violation can be selected for display in the state and timing windows.

To include this information in a state or timing display simply select the Bus Wizard decoded signal. The Bus Wizard displays a short description of the error. Highlighting the error displays a complete description of the anomaly.

Trigger and Filter Setup

Any anomaly can be selected as a trigger or filter when tracing bus activity. When used as a trigger this provides a view of activity that lead up to the error. Selecting anomalies for a filter allows the user to trace only errors detected by the anomaly checker.

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PCI650 Other Features

Configuration Scan

The configuration scan automatically detects devices on the bus and displays configuration information in 2 windows:

1. Block configuration data displays the configuration information in binary form.
2. Decoded Configuration interprets the information and displays Vendor name, class description, revision codes, etc.

To select another device Back and Next buttons start a new scan of the configuration space before and after the current device.

Configuration information can be saved, printed and loaded back for display.

External Trigger Inputs

Eight external inputs are provided for monitoring signals external to the PCI connector. These signals can be selected for display in the state and timing windows and used in trigger and trace setups.

A trigger cable is included which plugs into a trigger connector on the front panel. This connector also provides a ground signal.

External Trigger Output

One trigger output is provided to facilitate the triggering of other test equipment. When a trigger is encountered this output is driven active. The polarity and duration of the trigger output is specified by the user. This signal is available on the same front panel trigger connector along with the trigger inputs.

Communication Interfaces

The PCI650 communicates with a PC or terminal through an RS232 or USB interface. The RS232 interface operates at speeds up to 115K baud and the USB interface at 12Mbits/sec. All setup and display results are sent over these interfaces. USB (type B) and RS232 (DB9) connectors are located on the front panel.

External Power

The PCI650 can be powered by an external power supply. This feature can be useful when monitoring a system power up sequence. A power connector is located on the front panel. This connector supplies power to the analyzer and is fuse protected. A power cable is included with the analyzer.

Expansion Connector

A 200 pin expansion connector is located on the analyzer for optional plug on accessories. These include board test adapters and a 500 Mhz high speed timing module.

Reset Options

A pushbutton reset switch and reset jumpers select options for resetting the board and system.

LED Indicators

A green LED illuminates after the analyzer has passed it's self test and a red LED is under user control.

Reprogramability

New firmware updates can be downloaded into flash memory on the analyzer. Updates are available on our Web site.

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PCI650 Specifications

General Specifications

PCI Compliance:	PCI 2.2 Compliant
Bus Size:	64 or 32 bit
Bus Signal Levels:	5V or 3.3V

Trace Specifications

Trace Memory:

PCI650-1	64K by 144 bits
PCI650-2	128K by 144 bits
PCI650-3	256K by 144 bits
PCI650-4	512K by 144 bits

Sampling Rate:	66 Mhz
Sampling Modes:	System Clock System Clock w/ Address/Data System Clock w/ Transfers On board precision Oscillator (15ns to 15us)
Sampled Signals:	AD[63:0], C/BE[7:0], FRAME, DEVSEL, TRDY, IRDY, PAR, REQ, GNT, RST, LOCK, CLK, INTA, INTB, INTC, INTD, PAR64, PERR, SERR, REQ64, ACK64, TDO, TDI, TCK, TMS, TRST, SDONE, SBO, EXT[7:0]
External Inputs:	8 Front Panel Trace/Trigger
External Outputs:	1 Programmable Trigger Output
Triggers:	8 Trigger Conditions each specifying 100 PCI signals, 8 external triggers and anomaly errors
Trigger Types:	Single Condition Logical Combination 16 Level Sequencer
Trigger Positions:	0%, 25%, 50%, 75%, 100%
Occurrence Counters:	16 hardware counters 20 bits
Event Counters:	16 hardware counters 20 bits
Time Tag:	15 ns to 60 sec.

Exerciser Specifications

Initiator Bandwidth:	264 MB/s rate
Initiator Bus Width:	64 or 32 bit
Initiator Transfers:	Memory, I/O, Configuration

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PCI650 Specifications

Front Panel Interfaces

RS232 Port:	DB9 connector, 110 to 115K Baud (cable included)
USB Port:	Series B connector, 12 MB/s (cable included)
Indicators:	GO LED, User LED
Pushbutton:	Reset Analyzer or System
External Power:	2 Conductor front panel (cable included)
Trigger:	10 pin socket (8 in, 1 out, 1 ground) (cable included)
Fuses:	Main power and External power

Power Requirements

Operating—5V at 3 amps max
Standby—5V at 1 Amp max
Generated on-board– 3.3V and 2.5V

Dimensions:

PCI650—PCI Short Card
PMC650– Single slot PMC card
CPCI650– 3U Compact PCI card

Ordering Information:

PCI Analyzers

PCI650-1	PCI Bus Analyzer/Exerciser 64K Trace Buffer
PCI650-2	PCI Bus Analyzer/Exerciser 128K Trace Buffer
PCI650-3	PCI Bus Analyzer/Exerciser 256K Trace Buffer
PCI650-4	PCI Bus Analyzer/Exerciser 512K Trace Buffer

Compact PCI Analyzers

CPCI650-1	CPCI Bus Analyzer/Exerciser 64K Trace Buffer
CPCI650-2	CPCI Bus Analyzer/Exerciser 128K Trace Buffer
CPCI650-3	CPCI Bus Analyzer/Exerciser 256K Trace Buffer
CPCI650-4	CPCI Bus Analyzer/Exerciser 512K Trace Buffer

PMC Analyzers

PMC650-1	PMC Bus Analyzer/Exerciser 64K Trace Buffer
PMC650-2	PMC Bus Analyzer/Exerciser 128K Trace Buffer
PMC650-3	PMC Bus Analyzer/Exerciser 256K Trace Buffer
PMC650-4	PMC Bus Analyzer/Exerciser 512K Trace Buffer

All analyzers include Windows software, cables and manuals.

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