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Find the *Silicon Control VME850A-2* at our website: *Click HERE*

VME850 - Advanced VME64x Bus Analyzer / Exerciser

VME 850

VME64 / VME64x Analyzer/Exerciser

- Single 6U VME board
- Supports SCT, BLT, MBLT, 2eVME, 2eSST protocols
- Optional Analysis/Stimulus of User Defined P2 and P0 signals
- Choice of 96 or 160 pin P1/P2 connectors

Analyze Bus Activity

- State Analysis up to 100 Mhz
- Timing Analysis up to 400 Mhz
- Complex Triggering and Filtering
- Time Stamping
- Performance Analysis of Bus Utilization, Transfer Rates, Statistics

Exercise Bus Activity

- Master Transfers
- Stimulus Generation
- Fault Injection and Timing Modification
- CR/CSR Scan and Decode
- Backplane Short Test

Slave Memory

- Windowed VME bus memory

Protocol and Timing Violation Checker

- Detects over 100 timing and protocol violations
- Displayed and Used as Trigger in State/Timing Analysis

P2 Analysis of User Defined Signals

- 160 pin connector - row a,c,d,z
- Optional plug-in module

P0 Analysis of User Defined Signals

- 95 pin connector – row a,b,c,d,e
- Optional plug-in module

Communication

- USB
- RS232

Other Features

- External Power Connection
- External Trigger Inputs and Output
- Extensive Self Test
- Front Panel Reset and LED Indicators

Software User Interface Packages

- AnalyzeIt! PC GUI Software
- API Library provides User Program Control



VME / VME64x Bus Analyzer

The VME850 Analyzer / Exerciser supports the latest VME bus specifications and protocols. From standard VME transfers to 2eSST protocol. In addition to the VME bus, user defined signals on the P0 and P2 connectors are also analyzed and exercised with optional plug-in modules.

State and timing analysis feature large high speed trace buffers and sophisticated triggering. Transaction and waveform displays provide a clear view of captured bus activity.

Measurements of system performance include Bus Utilization, Transfer Rates and Statistics. As data is acquired the Min, Max and Average values are updated and displayed in graphical form.

Exerciser functions include reading, writing, testing and comparing memory. Stimulus generation provides the ability to simulate hardware, inject faults and modify timing as well as drive any bus signal directly. A built-in backplane test checks for shorts and the ability to drive every signal.

Anomaly detection of protocol and timing violations automatically screen for violations to the bus specification. Anomalies are included in the state display and trigger specifications.

Our AnalyzeIt software package provides an easy to use and intuitive GUI interface that operates under Windows 9x, ME, NT,XP and 2000. For custom application our API software enables users to control the analyzer directly through C library calls. For non-Windows users, a built in terminal interface is available.

Silicon Control introduces the ultimate analyzer and exerciser for VME and VME64x systems. This 4th generation VME analyzer combines high performance hardware with a sophisticated and intuitive software interface. The result is a powerful diagnostic tool for bus analysis all on a single plug-in card.

If you need to debug, integrate or test any VME system or component, the VME850 quickly and accurately pinpoints problems, identifies performance issues and tests for compliance. For more information or training contact our outstanding technical support, application and sales engineers.

SILICON CONTROL INC. *THE LEADERS IN BUS ANALYSIS*

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VME 850 SPECIFICATIONS

State/Waveform/Performance Analysis

- Trace Buffer Sizes
  - 128K, 256K, 512K, 1M, 2M samples
  - 144 bits wide
- Trace Sampling Speeds
  - 100 Mhz max synchronous
  - 400 Mhz max asynchronous
- Protocols Sampled
  - SCT, BLT, MBLT, 2eVME, 2eSST
- Signals Sampled
  - P1/P2 (112 signals)
    - A[31:0], D[31:0], DS[1:0]*, AM [5:0], AS*, WRITE*, LWORD*
    - IRQ[7:1]*, IACK*, IACKI/O*, BR [3:0]*, BG[3:0]*
    - BBSY*, BCLR*, BERR*, DTACK*, RETRY*, RESP*
    - SYSRESET*, SYSFAIL*, ACFAIL*, SYSCLK
    - GA[4:0]*, GAP*, MPR, MCLK, MSD, MMD, MCTL
  - P2 user defined (110 signals)
    - Rows A, C, D and Z
  - P0 user defined (95 signals)
    - Rows A, B, C, D, E
- Other Information Sampled
  - Time Tag (range 2.5 ns to 60 sec)
  - Trigger Level
  - External Front Panel Inputs (x8)
- Trigger Conditions
  - 8 bus events
  - Address and Data Ranges
  - 8 External Front Panel Inputs
- Trigger Types
  - Single Event
  - Logical Event Combination (AND, OR, XOR, NOT)
  - 8 Level Sequencer
- Trigger Occurrence Counting
  - 8 – 16 bit hardware counters
- Trigger Positions
  - 0%, 25%, 50%, 75%, 100%
- Filter Conditions
  - 8 bus events
  - Address and Data Ranges
  - 8 External Front Panel Inputs
- Performance Analysis Measurements
  - Bus Utilization
  - Transfer Rates
  - Statistics
- Performance Event Counters
  - 8 - 20 bit hardware counters

Exerciser Specifications

- Master
  - Protocols Supported
    - SCT, BLT, MBLT, 2eVME, 2eSST
  - Addressing Modes
    - A16, A24, A32, A40, A64
  - Data Widths
    - 8, 16, 32, 64 bit data
  - Master Commands
    - Read – reads data from slave
    - Write – writes data to slave
    - Test – verifies memory with test patterns
    - Compare – reads data and compares with stored data
  - User Parameters
    - Address Modifiers
    - Bus Request Level
    - Protocol
- Stimulus
  - Pattern Generation on P1/P2 and P0
  - 15 Stimulus Conditions
    - Specify active, inactive or not driven on any signal
    - Drive all VME signals
    - Drive all P2 user defined signals
    - Drive all P0 user defined signals
  - 15 Level Stimulus Sequencer
    - Control of stimulus conditions
    - Based on bus events
    - Specify duration and next condition
- CR/CSR Scan and Decode
  - Scans CR/CSR space for devices
  - Identifies and decodes data
- Backplane Short Test
  - Checks for ability to drive signals
  - Checks for shorts between signals

Slave Memory

- Memory Sizes
  - 1MB, 2MB, 4MB, 8MB, 16M
- Protocols Supported
  - SCT, BLT, MBLT, 2eVME, 2eSST
- Addressing Modes
  - A16, A24, A32, A40, A64
- Data Widths
  - 8, 16, 32, 64 bit data
- Windowed 64K Address Space
- Controlled Response
  - Retry
  - Suspend
  - Error

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VME 850 SPECIFICATIONS

Anomaly Detection

- Detects Unstable Signals
- Checks Out of Sequence Signals
- Saved in Trace Buffer
- Specified in Event Triggers

Front Panel Interfaces

- RS232 Port
  - DB9 connector
  - 110 to 115K Baud
  - Cable included
- USB Port
  - Series B connector
  - 12 MB/s
  - Cable included
- Indicators
  - GO LED
  - User LED
- Pushbutton
  - Reset Analyzer
  - Reset System
- External Power
  - 2 Conductor front panel
  - Cable included
- Trigger
  - 10 pin socket
  - 8 in, 1 out, 1 ground
  - Cable included
- Fuses
  - Main power
  - External power

Optional Modules

- P0 User Defined Signal Analyzer/Exerciser
- P2 User Defined Signal Analyzer/Exerciser

Self Test

- Coverage 95%
- Bus Transceiver Test

Environmental

- Operating Temperature 0 to 55 deg C
- Storage Temperature –40 to 85 deg C
- Humidity Up to 95% Non-Condensing

Power Requirements

- Operating—5V at 3 Amps max
- Standby—5V at 1 Amp max

Dimensions

- VME 6U Eurocard

Ordering Information

VME Analyzers

VME850-1	128K Trace Buffer 1MB Slave Memory
VME850-2	256K Trace Buffer 2MB Slave Memory
VME850-3	512K Trace Buffer 4MB Slave Memory
VME850-4	1M Trace Buffer 8MB Slave Memory
VME850-5	2M Trace Buffer 16MB Slave Memory

P0 Analyzer/Exerciser Module

VME850P0-1	128K Trace Memory
VME850P0-2	256K Trace Memory
VME850P0-3	512K Trace Memory
VME850P0-4	1M Trace Memory
VME850P0-5	2M Trace Memory

P2 Analyzer/Exerciser Module

VME850P2-1	128K Trace Memory
VME850P2-2	256K Trace Memory
VME850P2-3	512K Trace Memory
VME850P2-4	1M Trace Memory
VME850P2-5	2M Trace Memory

* Suffix “A” designates the loading of a P0 connector. (Example: VME850A-3 is a VME Bus Analyzer with a 512K trace buffer and a P0 connector)

Included with every VME850

VME850 Analyzer, AnalyzeIt PC software, API software, USB driver software, terminal interface, USB cable, RS232 cable, trigger cable, documentation, quick start guide and carrying case.

Represented By:

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