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ZT 8901

Single Board V53 Computer

A highly integrated, single board STD 32® computer for embedded applications requiring advanced 80286 performance, abundant on-board memory, and industrial I/O.

The ZT 8901 Single Board V53 Computer is intended for embedded applications where performance, size, and reliability are high priorities. It operates at 16 MHz with a high-speed on-board bus, yet is completely compatible with STD 32® and STD Bus designs.

The ZT 8901 also supports multiple bus-master operation, allowing multiple processors to operate in a single STD 32 backplane.

In addition to its STD 32 capabilities, the ZT 8901 features ample on-board memory and I/O, making it an effective stand-alone single board computer.

The NEC V53 microprocessor on the ZT 8901 is code-compatible with the 80286 microprocessor (real mode), while providing better performance and many additional features.

The ZT 8901 is supported by STD ROM for embedded applications, STD DOS for DOS-based systems, and the STAR BIOS for multiprocessing DOS-based applications in an STD 32 STAR SYSTEM™.

The ZT 89CT01 version is available for extended temperature operation (-40° to +85° C) at 12.5 MHz.

- STD 32- and STD-compatible
- 16 MHz V53 processor
- 80286 code-compatible for real mode operation
- 16 Mbyte memory address range
- Up to 1 Mbyte static RAM, optional battery
- Up to 1 Mbyte PROM/512 Kbyte flash PROM
- 64 Kbyte I/O address range
- STD 32 multiple bus-master operation
- One RS-232 serial port (8251)
- Two RS-232/422-485 serial ports (16552), one with DMA
- One interrupt controller (8259)
- Three 16-bit counter/timers (8254)
- Three DMA channels (8237 or 71071)
- 8-bit or 16-bit SBX with DMA
- 48 parallel I/O lines (Opto 22-compatible)
- Real-time clock, optional battery
- AC/DC power-fail detection
- Single-stage watchdog timer
- Push-button reset
- Dynamic 8- and 16-bit bus sizing
- Low power CMOS with sleep mode
- Software-programmable LED
- ZT 89CT01 for extended temperature operation

Note: CT denotes CMOS, TTL backplane-compatible, and extended temperature operation of -40° to +85° C. (Users should make adjustments for temperature rise in enclosures.)

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Functional Considerations

STD Bus Interface

The ZT 8901 supports both STD 32 and STD Bus backplane architectures. In an STD backplane, all data transfers between the ZT 8901 and the bus are reduced to 8 bits. In an STD 32 backplane, dynamic bus sizing signals determine the width of the data transfer between the ZT 8901 and other boards.

The bus address, data, and control signals are held static during local operations for reduced power consumption. External masters, such as fixed and floppy disk controllers, are supported through the bus request/bus acknowledge protocol.

Multiple Bus-Master Operation

The ZT 8901 can be jumper-configured for STD 32 multimaster operation. With the addition of the ZT 89CT39 Slot X Arbiter Card, as many as seven ZT 8901 boards can be used in a single STD 32 system. This architecture permits any of the ZT 8901 boards to access STD Bus memory and I/O using a fixed or rotating priority scheme.

In operation, a ZT 8901 gains permission for a system access from the arbiter. The ZT 8901 then completes the system transfer and either releases control of the system resources (bus release mode) or holds control of the system resources until requested to release by the arbiter (bus hold mode). A locking mechanism is supported to guarantee uninterrupted system access. Also, each ZT 8901 is capable of interrupting any other ZT 8901 using frontplane or backplane interrupt paths.

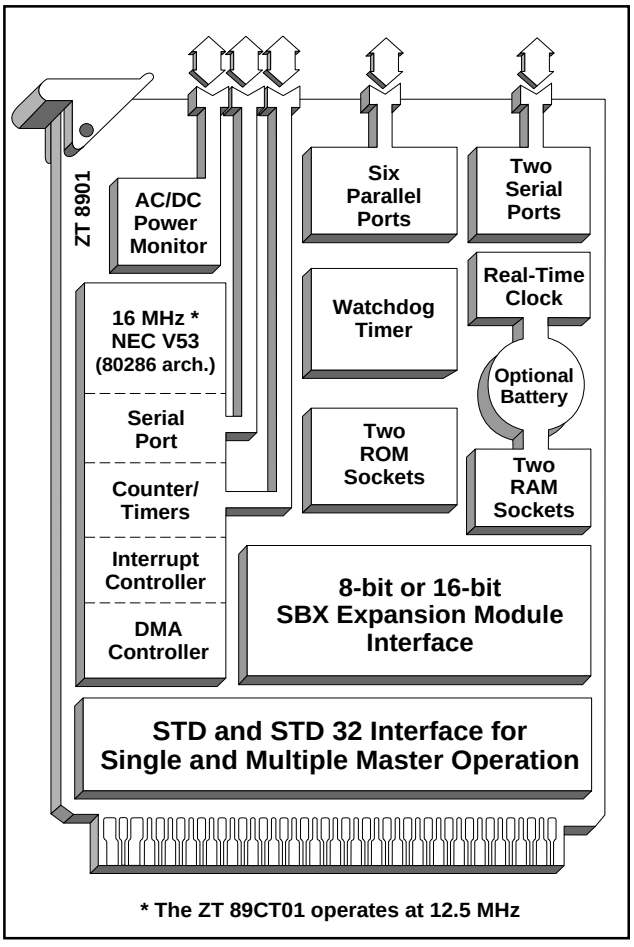


Figure 1. The ZT 8901 Functional Block Diagram

NEC V53 Processor

The NEC V53 is a highly integrated, 16-bit CMOS microprocessor. The V53 includes several standard peripherals in addition to a CPU with an architecture similar to the 80286. Design of the processor has been optimized to execute instructions up to 20% faster than an 80286 operating at the same clock frequency.

The primary difference between the V53 CPU and the 80286 is in the method used to address memory between the 1 Mbyte and 16 Mbyte address range. The V53 uses an extended addressing method to software bank select 16 Kbyte memory blocks from the 16 Mbyte physical address range to the 1 Mbyte logical address range. It does not support the protected address mode available on the 80286.

Memory Addressing

The ZT 8901 supports a 16 Mbyte memory addressing range. This address space is divided between memory local to the ZT 8901 and space available for STD Bus memory expansion. Local memory operations use a 16-bit data path to transfer data at a rate of 16 Mbytes per second.

In an STD system, all backplane memory operations are implemented with 8-bit data transfers. In an STD 32 system, dynamic bus sizing is used to support both 8-bit and 16-bit data transfers for backplane memory.

Four 32-pin memory sockets are organized into two pairs to support the 16-bit nature of the V53. One socket pair accepts RAM devices (32 Kbyte, 128 Kbyte, and 512 Kbyte) with a standard 0.6-inch (15.2mm) DIP footprint. The RAM devices support battery backup with the addition of the optional battery. The other socket pair accepts EPROM and flash memory devices (from 128 Kbyte to 512 Kbyte) with a standard PLCC footprint.

An extractor tool (the ZT 98034) is required to remove the PLCC devices from the sockets. A programming adapter (the ZT 98035) may also be required to program the PLCC devices with a PROM programmer having a 32-pin, 0.6-inch (15.2mm) DIP socket.

I/O Addressing

The ZT 8901 supports a 64 Kbyte I/O address range. This address space is divided between I/O local to the ZT 8901 and space available for STD Bus I/O expansion.

In an STD system, all backplane I/O operations are implemented with 8-bit data transfers. In an STD 32 system, dynamic bus sizing is used to support both 8-bit and 16-bit data transfers for backplane I/O. The STD Bus IOEXP signal is driven low for backplane I/O operations in the address range from FC00 through FFFFh. This prevents boards that decode IOEXP and fewer than 16 bits of address from being redundantly mapped. All devices local to the ZT 8901, except the SBX expansion module, operate with 8-bit data transfers.The SBX expansion module is jumper-selectable for either 8-bit or 16-bit data transfers.

Serial I/O

Three asynchronous serial I/O ports are available, each with a programmable baud-rate generator. The V53 provides one serial channel (8251 architecture for asynchronous operation) configured for RS-232 DTE operation with a maximum transfer rate of 640K baud. This serial channel supports transmit data (TxD), receive data (RxD), and ground through a 3-pin frontplane connector. An optional cable is available to connect the V53 serial channel to a male 25-pin, D-shell connector.

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The other two serial channels (16450 architecture) are equivalent to the serial I/O used in IBM personal computers. These channels support all handshaking and modem control signals and are jumper-selectable for RS-232 or RS-422/485 operation, as well as DCE or DTE. Other features include transfer rates up to 115.2K baud, loopback diagnostics, maskable interrupt generation, software-selectable 16-byte FIFO for both transmit and receive buffers, and software-selectable DMA-driven data transfers.

Optional cables are available to connect these serial channels to a male or female 25-pin D-shell connector.

Parallel I/O

Six 8-bit parallel ports provide a total of 48 buffered parallel I/O lines. Each I/O line is programmable for input or output with readback operation. The outputs sink 12mA and do not glitch during power-up or power-down, features that are especially useful for industrial applications. All signals may be latched for event sense capability. The I/O signals and fused power are accessible through a 56-pin frontplane connector. An interface adapter is available to connect the parallel I/O to two 8-, 16-, or 24-position I/O module mounting racks, such as those offered by Ziatech and Opto 22.

Interrupts

The interrupt controller (8259 architecture) supports eight maskable inputs and cascade operation for up to 43 interrupts. Features include level- and edge-triggered sensing, fixed and rotating priorities, and the ability to mask individual inputs. There are 15 possible interrupt sources selected through jumper configuration. The interrupt sources include counter/timers, serial I/O, SBX expansion module, real-time clock, STD Bus, and a frontplane connector.

Counter/Timers

Three independent, 16-bit counter/timers (8254 architecture) act as timers or event counters.There are six programmable counter/timer modes: interrupt on end-of-count, frequency divider, square wave generator, software-triggered, hardware-triggered, and retriggerable one-shot. Two of the counter/timers can generate maskable interrupts. The third is available through the frontplane to be used by the application.

Watchdog Timer

The watchdog timer monitors system operation. If jumper-enabled, the watchdog timer must be strobed at a periodic rate by the application software. Failure to strobe the watchdog timer results in a system reset.

Real-Time Clock

The real-time clock (National Semiconductor 8572A) performs timekeeping functions and includes 44 bytes of RAM. With the optional battery installed, these features continue to operate when power is removed. Timekeeping features include resolution down to 0.01 seconds, 12- or 24-hour operation, leap year adjustment, rollover status, time comparison and periodic interrupts, and automatic time logging in the event of a power failure.

DMA Controller

The DMA controller is programmable for either 8237 (8-bit) or 71071 (16-bit) operating modes. Regardless of the mode selected, there are three DMA channels for high-speed data transfer between local memory and local I/O. DMA channel 0 is dedicated to transfers between the SBX expansion module and local memory. DMA channel 1 is dedicated to transfers from the COM2 serial channel receive buffer to local memory. DMA channel 2 is dedicated to transfers from local memory to the COM2 serial channel transmit buffer.

Features of the DMA channels include single-byte transfers, block transfers, fixed or rotating channel priorities, and (71071 only) 2.3 Mbytes per second transfer rates for 8-bit I/O and 4.6 Mbytes per second transfer rates for 16-bit I/O.

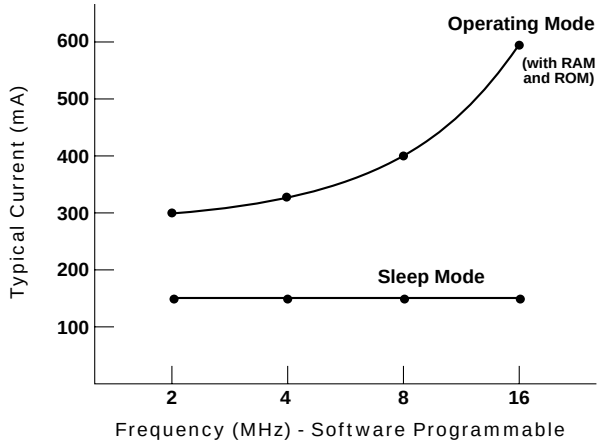
SBX Expansion Module Socket

The SBX expansion module socket provides an alternative for hundreds of off-the-shelf I/O modules. Ziatech sells the following SBX modules:

zSBX 20 GPIB Controller Interface
zSBX CT31 48-point Digital I/O Interface
zSBX CT32 Centronics and Serial Interface
RBX* 311 Analog Input card
RBX* 388 Analog I/O Card
RBX* 398 High Speed Analog I/O Card
*Denotes manufacture by Robotrol Corporation

Extended Temperature Operation

The ZT 89CT01 is designed with low-power and extended temperature CMOS technology for a typical power consumption of less than 600 mA with 256 Kbytes of ROM, and 256 Kbytes of RAM installed. The ZT 8901 also supports a software programmable operating frequency and sleep modes for even lower power consumption. The figure below is a graph of typical power consumption versus programmed frequency for both operating and sleep modes.



AC Power-Fail Protection

With the addition of an optional AC transformer, the ZT 8901 monitors AC power to permit an orderly shutdown during a power failure. When AC power falls below an acceptable operating range, a non-maskable interrupt is generated to notify the V53 processor of the impending power failure. The application software can then save critical data before the processor is reset.

Software

Ziatech offers two software development systems for ZT 8901 applications: STD ROM and STD DOS. STD ROM allows users to develop ROM-based (non-DOS) STD applications on an IBM or compatible PC. The PC, which is connected to the STD system through a serial link, runs Paradigm's DEBUG/RT. This allows high-level languages such as C and Assembly to be used for system development.

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The second development system, STD DOS, is the popular DOS operating system residing in flash memory on the ZT 8901. Applications can be developed much faster with STD DOS by programmers familiar with DOS. STD DOS provides support for many peripherals such as disks and video. It is supported by a large number of development tools such as editors, compilers, assemblers, and debuggers.

When enhanced by the STAR BIOS, the ZT 8901 can work in the same backplane with other processors, each running DOS and sharing disks and video to provide real-time DOS-based control systems *(see the STD 32 STAR SYSTEM™ data sheet).*

Specifications

- Compatible with STD 32, STD-80, and IEEE 959-1988 SBX specifications

Electrical

DC Operating Characteristics:

Power Req.	***Min.***	***Typ.***	***Max.***
Supply Voltage, V_{CC}	4.75V	5.0V	5.25V
Supply Current, V_{CC}=5.0V ***ZT 8901*** ***ZT 89CT01***	 – –	 .45A .35A	 .85A .75A
Aux Voltage, V_{aux+}	11.4V	12.0V	12.6V
Aux Current, V_{aux+}=12.0V	–	0.01A	0.02A
Aux Voltage, V_{aux-}	-12.6V	-12.0V	-11.4V
Aux Current, V_{aux-}=-12.0V	–	0.01A	0.02A

Mechanical

- Measures 4.5" (11.4cm) by 6.5" (16.5cm)
- Height measured from component surface:
  Without the following items = 0.38" (9.7mm)
  Including battery = 0.43" (10.9mm)
  Including SBX expansion module = 1.15" (29.2mm)
- Weight = 5.5 oz. (155.9g)
- Connectors

P1:	114-pin STD Bus card edge connector on 0.0625" (15.9mm) spacing
J1:	2-pin latching AC input
J2:	3-pin latching V53 serial I/O
J3:	16-pin latching counter/timer and interrupts
J4:	14-pin latching COM2 serial I/O
J5:	14-pin latching COM1 serial I/O
J6:	56-pin parallel I/O
J7:	44-pin latching SBX expansion module

STD 32 Compliance Levels

See the STD 32 Brochure in the Data Book appendix for STD 32 Compliance Level definitions.

- Permanent Master: SA16, SA8 - I, ICA, IXL, IXP, MB, MD
- Temporary Master: SA16, SA8 - {MD} I, ICA, IXL, IXP
- Memory Slave: SA8

Note: SA8 is equivalent to STD-80 Series Rev. 2.3 (5 and 8 MHz)

Environmental	
Operating Temperature ***(ZT 8901)***	0° to 65° Celsius
Operating Temperature ***(ZT 89CT01)***	-40° to +85° Celsius
Storage Temperature	-40° to +85° Celsius
Non-Condensing Relative Humidity	less than 95% at 40° Celsius

Reliability

- MTBF: 20 years
- MTTR: five minutes (based on board replacement)

Ordering Information

ZT 8901	Single Board V53 Computer
ZT 89CT01	Single Board V53 Computer, extended temperature
ZT M8901	Single Board V53 Computer manual

Must choose one option from each category:

Flash options

P0	No flash EPROM, 180ns
P1	256 Kbytes flash EPROM, 180ns
P2	512 Kbytes flash EPROM, 180ns

RAM options

R0	No RAM
R1	256 Kbytes static RAM, 100ns
R2	256 Kbytes static RAM, 55ns
R3	1 Mbyte static RAM, 120ns
R4	1 Mbyte static RAM, 55ns (Option R4 cannot be battery backed)

Software options

S0	No software installed on board
S1	DOS and BIOS installed (Requires Options P1R1B or greater)

Battery option

B	1 amp-hour lithium battery (ext. temp.)

Development Toolkits

Either STD DOS or STD ROM is required with initial system purchase. Manuals for hardware are free with the purchase of a STD DOS or STD ROM development system.

ZT 94007 STD DOS Development Toolkit. Includes host development disk containing VSC, PROM-PREP, FLASH, and other utilities. STD Device Driver Package (STD DDP) with support for STD 32 I/O cards peripherals, ZT 7502/00 BIOS diagnostic card, full Microsoft MS-DOS, two serial cables, and a PLCC extractor tool. (Requires options P1R3S1B.)

ZT 94008 STD ROM Development Toolkit. STD ROM development system for PROM-based target systems. Includes Virtual Terminal Interface (VTI) installed on PROM, Paradigm LOCATE and Startup modules, STD DDP, Paradigm DEBUG/RT, two serial cables, and a PLCC extractor tools.

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