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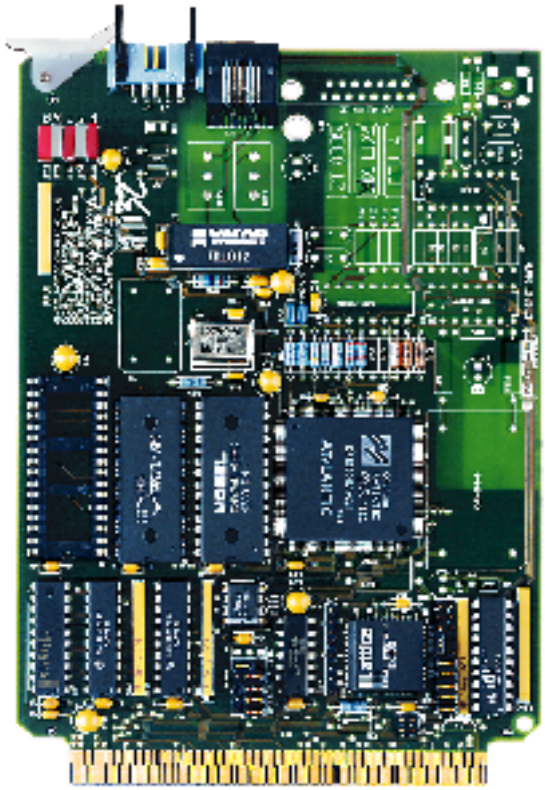
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ZT 8995



STD Bus Ethernet Interface

Hardware User Manual

ZIATECH CORPORATION

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MANUAL ORGANIZATION

This manual describes the operation and use of the ZT 8995 STD Ethernet Interface Board. Each chapter is briefly outlined below to help you find the best place to start.

Chapter 1, "Introduction," offers an overview of the ZT 8995. It includes a product definition, a list of product features, a functional block diagram, and a brief description of each block. The ZT 97115 software drivers, setup, and diagnostic programs are also described. If you wish to evaluate the ZT 8995 to determine if it fits your needs, this chapter is especially useful to you.

Chapter 2, "Getting Started," summarizes the information you need to get your ZT 8995 up and running. Refer to the following sections for further explanation of the material covered in "Getting Started."

Chapter 3, "Theory Of Operation," presents a detailed description of ZT 8995 system level operation. The topics discussed in this chapter include commonly asked questions, the STD bus interface, the Ethernet interface, and diagnostic LEDs present on the board.

Appendix A, "Jumper Configurations," illustrates jumper options that tailor the board's operation to your specific application.

Appendix B, "Network Components and Cabling," provides an overview of Ethernet components and cabling, contrasting Thin Ethernet, Thick Ethernet, Twisted-Pair Ethernet, and fiber optic cabling.

Appendix C, "Network Interconnection," describes the electrical and mechanical requirements to interconnect an Ethernet network.

Appendix D, "Specifications," contains the electrical, mechanical, and environmental specifications for the ZT 8995.

Appendix E, "Customer Support," includes a product revision history, technical assistance, and the necessary information should you need to return your ZT 8995 for repair.

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1. INTRODUCTION

This chapter introduces some key features of the ZT 8995. It includes a product definition, a list of product features, a functional block diagram, and a description of each block. The ZT 97115 software setup and driver package for the ZT 8995 is also covered. Carefully review this chapter to gain a basic understanding of the capabilities of the ZT 8995. Unpacking information, as well as installation and setup instructions, are in Chapter 2, "Getting Started."

ABOUT THE ZT 8995 INTERFACE

The following sections include a product definition for the ZT 8995 and a list of product features.

Product Definition

The ZT 8995 is an Ethernet Interface for the STD 32 bus and for the STD bus. It supports 10Base-T as well as Thin Ethernet (Cheapernet, 10BASE2) and Thick Ethernet (10BASE5) cabling options. For cable configurations, review Appendix B, "Network Components and Cabling". Additional ZT 8995 support includes extensive software drivers for several popular network operating systems, a setup program, and complete diagnostics.

The ZT 8995 conforms to the IEEE 802.3 and Ethernet standards for a 10 Mbps Carrier Sense Multiple Access/Collision Detection (CSMA/CD) local area network. Local area networks using twisted-pair, coax, and fiber optic media can be supported. Refer to Appendix B, "Network Components and Cabling", for more information.

The ZT 8995 comes with a ROM socket and software drivers. Check the ZT 97115 disks for a complete list of supported drivers.

Software packages are also available for TCP/IP support. Department of Defense TCP/IP software from FTP Software allows remote log-in, file transfer, terminal emulation, electronic mail, and many other functions. TCP/IP is widely used and is supported by over 150 vendors, allowing dissimilar computers and operating systems to communicate.

Boot ROM capability for Novell NetWare V2.0A, V2.1 and later is supported by National Semiconductor's boot ROM. When the boot ROM is installed on the ZT 8995, the disk operating system is loaded from the network server. This diskless installation is ideal for systems in harsh industrial environments where driver installation would normally require rotating media.

The ZT 8995 is compatible with all Ziatech STD 32 and STD systems. A versatile setup program allows you to configure the board for the desired I/O address, packet RAM address, PROM socket address, and interrupt selection.

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In addition to these features, the ZT 8995 incorporates low-power CMOS devices for operation in 0º to +70º Celsius environments. CMOS devices that are TTL-compatible ensure system compatibility with other CMOS or TTL STD bus boards.

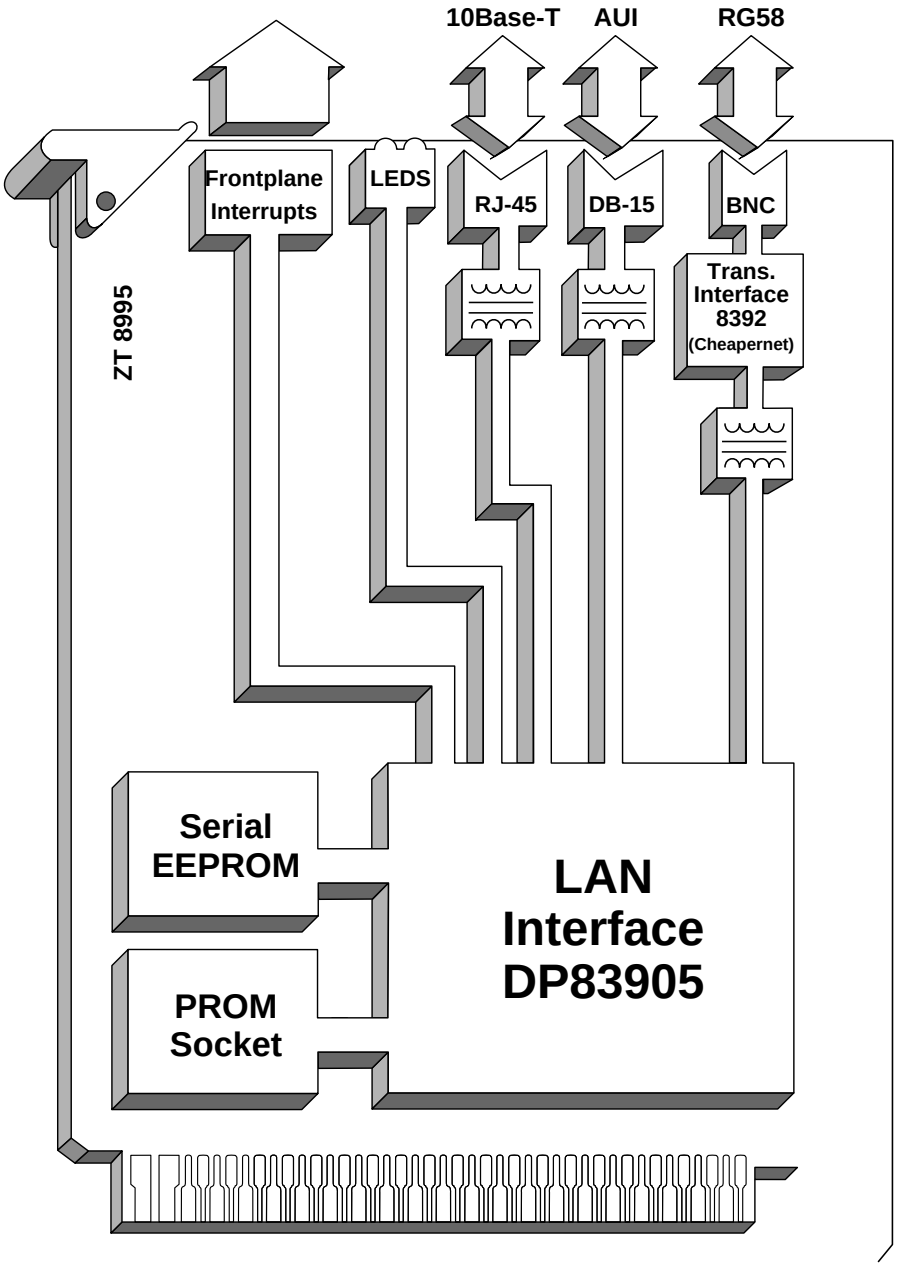
Features

- Novell NE2000-compatible chipset
- STD 32- and STD-compatible
- Exact STD form factor (no porches or connector extensions)
- True 16-bit I/O addressing
- 20- or 24-bit memory addressing
- Includes drivers for Novell's NetWare® environment
- Supports both IEEE 802.3 10BASE2 (Thin Ethernet) and 10BASE5 (Thick Ethernet), as well as 10Base-T Ethernet interfaces, depending on the option ordered
- Dual port RAM capability
- Transmit, Receive, and activity LEDs
- EEPROM stores system configurations
- Low-power CMOS design
- +5 V only operation
- AUI support with locking DB15 connector

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FUNCTIONAL BLOCKS

A description of each functional block follows the below figure "Functional Block Diagram."



Functional Block Diagram

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LAN Interface (DP83905)

The National Semiconductor DP83905 AT/LANTIC provides the interface between the STD bus and the on-board Local Area Network (LAN) bus The DP83905 also provides the network interface portion of the LAN bus.

The LAN Bus

The LAN bus consists of the packet RAM and Network Interface. LAN Interface configuration values are programmed into an external EEPROM when the device is set up. These values are automatically loaded into on-board registers when the board is powered up.

Depending on the configuration, the DP83905, with some external help, decodes both memory and I/O addresses when accessing the on-board PROM socket, RAM, or Network Interface.

The Network Interface

The Network Interface provided by the DP83905 implements all Media Access Control (MAC) layer functions for transmission and reception of Ethernet packets, in accordance with both the IEEE 802.3 standard and pre-IEEE 802.3 standards.

It also contains an internal First In First Out (FIFO) buffer and arbitration logic to control access to the packet RAM. The DP83905 includes:

- Support for physical, multicast, and broadcast address filtering
- Provision for three levels of loopback
- Implementation of buffer management

The DP83905 provides complete IEEE 802.3 protocol and electronics with the only exception being the packet RAM.

Serial Interface (DP83905)

The National Semiconductor DP83905 also provides Manchester encoding, decoding, and collision detection for the Serial Interface. The 83905 includes the following:

- 10 Mbps encoding and decoding
- Loopback capability for diagnostics
- Isolation from Ethernet cable

The DP83905 interfaces the ZT 8995 to the Ethernet cable via an external Attachment Unit Interface (AUI) drop cable, the on-board Transceiver Interface (8392), or twisted-pair cabling.

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Transceiver Interface (DP8392)

The National Semiconductor (or equivalent) DP8392 Transceiver Interface is used as a coaxial cable driver/receiver for Thin Ethernet (Cheapernet) applications. The Thin Ethernet cable can be connected directly to the ZT 8995 without using an external drop (AUI) cable because the connector is isolated from the Serial Interface (8391) by an isolation transformers and a DC to DC converter.

Packet RAM Buffer

The packet RAM buffer is 16 Kbytes in length and can be used by either the STD bus processor or the Network Interface Controller (DP83905). This memory may be placed on any 8-Kbyte memory address boundary. Compatibility with any memory move instruction to the Network Interface results in a very efficient dual-ported packet buffer.

User PROM Socket

The ZT 8995 includes a PROM socket that can accommodate 32-, 64-. 128-, or 256-Kbyte parts where only the top 32Kbyte block is accessible. The PROM can be mapped into any 8, 16, 32, or 64Kbyte boundary beginning at one of eight software selectable locations between 0C000h and 0D000h. The PROM can be accessed without interfering with Ethernet packets being sent or received. You can use the setup program AUTOSET8.EXE to configure the PROM socket address.

Interrupt Capability

Interrupts are supported by the ZT 8995. Interrupts are software selectable for backplane signals INTRQ*, INTRQ1*, INTRQ2* (CNTL), INTRQ3*, INTRQ4* and NMIRQ*. Frontplane interrupts can also be selected through software control across FP3*, FP5*, FP6* and FP7*. Since IRQx is slot specific, it is always driven out onto the backplane.

Diagnostic LEDs

The ZT 8995 has separate transmit, receive, and diagnostic LEDs. These LEDs provide visual indication of network activity. Transmit activity is indicated by a red LED. Receive activity is indicated by a green LED. A green LED is used to indicate a LINK and red LEDs are used to indicate POLARITY problems as well as COLLISIONs.

ZT 97115 SOFTWARE DISK

The ZT 97115 software disk included with each ZT 8995 is supplied under license with National Semiconductor. A variety of software drivers, a setup programs, and extensive diagnostic programs are included. You can use any or all of the software drivers without any additional cost or licensing.

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ZT 97115 Product Definition

Each ZT 97115 includes:

- Software drivers for several popular network operating systems
- A setup program
- Complete diagnostics

These features are described in the following topics.

Software Drivers

The disk includes software drivers for use with several network operating systems. You must integrate these drivers into your network operating system. A complete list of supported software drivers is available on the ZT 97115 disk. Keep in mind that the ZT 8995 is NE2000 compatible and can be used with most drivers that are already provided with your network software.

Setup Program

The ZT 97115 includes a setup program to initialize the ZT 8995. The setup program is used to initialize the following:

- Base I/O address
- Interrupt line
- Operating mode (I/O or Memory Mapped)
- Media Selection (UTP, Thin or Thick Ethernet)

The board is shipped software "disabled". This prevents a possible conflict with your existing system I/O map and interrupt structure. To set your default values, a DOS based configuration program called INFOSET.EXE must be used. Refer to the topic "Using The Setup Program" in Chapter 2 for details.

Diagnostic Programs

The ZT 97115 software disk contains a diagnostic program named AUTOSET8.EXE used to verify the correct configuration (via setup) and operation of a ZT 8995 Ethernet board before installing the network software. Software is also included to test the ZT 8995 and to initiate and respond to network messages while logging network statistics. Diagnostics can be run in iterative or continuous modes initiated from within the diagnostic itself or from the DOS command line. See below:

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AUTOSET8.EXE

This program will re-configure the ZT 8995 to your specific system requirements. Including: the operating mode (memory or I/O mapped), the memory or I/O space, special operating parameters such as signal timing, as well as the desired interrupt. This program can also be used to diagnose board operation.

Note: This program should be used to configure the board for memory operation. INFOSET.EXE can also set memory mode, but does not include the ability to configure the memory map. If you plan to operate the ZT 8995 in shared memory mode, set it for I/O operation first, using INFOSET.EXE, and then use AUTOSET8.EXE to tailor the ZT 8995 configuration for your system.

DEFAULT.EXE

Writing 19h to the configuration register temporarily disables the ZT 8995 by locking out I/O access to the Ethernet chip. DEFAULT.EXE re-enables the ZT 8995.

INSPECT.EXE

This is a DOS-based, "windows-like" program similar to AUTOSET8.EXE in that it includes some diagnostics capabilities. However, it cannot be used to configure the board.

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2. GETTING STARTED

This chapter summarizes the information you need to get your ZT 8995 up and running. You should read this chapter before you attempt to use the board.

Many of the topics in "Getting Started" are covered in greater detail in subsequent chapters. You will find a number of cross references for topics containing further information.

UNPACKING

Please check the shipping carton for damage. If the shipping carton and contents are damaged, notify the carrier and Ziatech for an insurance settlement. Retain the shipping carton and packing material for inspection by the carrier. Save the anti-static packing material for storing or returning the ZT 8995.

Do not return any product to Ziatech without a Return Material Authorization (RMA) number. The topic "Returning for Service" in Appendix E explains the procedure for obtaining an RMA number from Ziatech.



WARNING: Like all equipment utilizing CMOS devices, the ZT 8995 must be protected from static discharge. Never remove any of the socketed parts except at a static-free workstation.

SYSTEM REQUIREMENTS

The ZT 8995 is designed for use in an STD bus application. Therefore, the board is mechanically and electrically compatible with the STD 32 series and STD standards.

Twisted Pair operation: the board requires +5 VDC ±5% at 350 mA maximum, 140 mA typical.

Thin Ethernet operation: the board requires +5 VDC ±5% at 705 mA maximum, 495 mA typical.

Thick Ethernet operation: the board requires +5 VDC ±5% at 330 mA maximum and 120 mA typical.

AUI adapters: normally require +12 VDC ±5% at 220 mA maximum, 165 mA typical. Consult the specific AUI adapter data sheet.

Ambient temperature range: must be maintained between 0º and +70º Celsius for operation.

Relative humidity: must be less than 95% at 40º Celsius, non-condensing.

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Refer to Appendix D, "Specifications," for additional specifications.

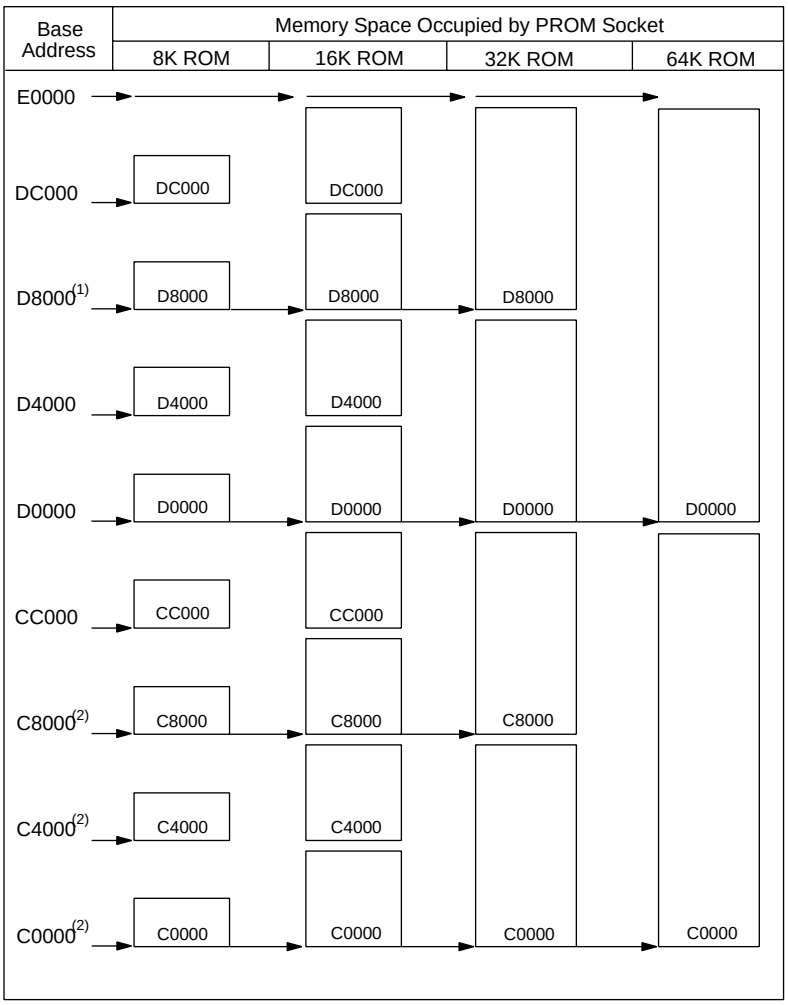
Vertical mounting is recommended in convective cooling systems not equipped with a fan. However, most systems require a fan for reliable operation. Horizontal mounting is not recommended unless forced air cooling of at least 30 cubic ft/min. is provided.

If a standard STD bus card cage is not used, refer to the figure "Board Dimensions" in Appendix D for board dimensions. Be sure to allow enough clearance for good convective or forced cooling.

Memory Requirements

The ZT 8995 may be assigned memory space within a range of addresses located above the system memory (typically 640K). The ZT 8995 may require as much as 48 Kbytes of memory space for its 16 Kbyte RAM buffer and optional 64-Kbyte PROM. The figure "PROM Base Address Map" following illustrates the various address maps available to the PROM socket.

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(1) D8000 is the recommended base address for the optional ROM.
(2) Use care when choosing memory space for C0000 to C8000.
Other boards or functions (for example, EGA) may use this memory space.

PROM Base Address Map

PROCESSOR COMPATIBILITY

The ZT 8995 is designed for STD 32 and STD systems. It can be used with any STD bus microprocessor that meets the STD 32 bus read and write timing specifications.

DEFAULT CONFIGURATION

For most systems, the ZT 8995 does not require jumper changes in order to operate. However, after your initial installation, if a different I/O address or memory configuration is needed, you might need to change the jumpers and/or run the setup program.

The Figure "Factory Default Jumper Configuration" in Appendix A shows the ZT 8995 factory default configuration. The list below shows the ZT 8995 default settings as shipped from the factory.

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- Software disabled (no I/O or memory locations enabled)
- Jumpered for 24-bit (not 20-bit) memory addressing
- BHE* enabled
- 16-Kbyte buffer RAM
- PROM socket disabled
- Interrupts are software disabled
- 16-bit data width operation enabled
- Thin-net DC/DC converter disabled
- Early ALE* signal operation enabled
- WAITRQ* enabled
- ISP PAL programming disabled

If you reconfigure the ZT 8995 jumpers, we recommend you document your configuration on the blank layout provided in the "Customer Jumper Configuration" figure in Appendix A. This allows you to restore the configuration easily if you change it for any reason.

SOFTWARE CONFIGURATION

The ZT 97115 software disks are included with each ZT 8995 interface. The disks contain programs to set up a board for a different configuration and to test a board. The disks also include various software drivers. Program functions are described in the following sections:

- Using the Setup Program
- Testing a Board
- Installing the Drivers

Note: When installing the ZT 8995 in Windows95 and WindowsNT systems, do not use the "Auto Detect" feature in the "Add New Hardware" program. This may cause your system to lock up and you may have to reboot. Instead, specify a new ethernet card and select the "NE2000 Compatible" option.

Using The Setup Program

The setup program contains the software necessary to select the configuration options for the ZT 8995. It may be found on the ZT 97115 diskette under the SETUP directory.

Use the INFOSET.EXE setup program after installing the ZT 8995 board in an STD-80 or STD 32 system. When the desired options are selected, the configuration for the ZT 8995 is saved in on-board, nonvolatile memory (EEPROM).

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If you have purchased a ZT 8995 for a Ziatech system for the first time, it will be configured as follows:

- Software disabled
- Interrupts disabled
- PROM socket disabled

Use the setup program INFOSET to configure and enable the ZT 8995 operating parameters. Once the board has been configured, the board's operation can be checked using the AUTOSET8 or INSPECT programs (see the "Testing a Board" topic in this chapter).

The setup program INFOSET may be executed from the floppy disk or copied to your hard disk and executed there. Be sure to document any changes made using INFOSET. You will need to configure the network software used with the ZT 8995 to match your board's configuration.

The AUTOSET8 program displays the current setup information that is held in on-board, non-volatile memory. It prompts you for any changes. If necessary, change the configuration as required and save the new setup.

If the ZT 8995 is installed into the card cage and the setup programs indicate an error, try looking for an I/O address conflict. If you have not used INFOSET to configure the I/O address, the board may be software disabled. If you used INFOSET to change the I/O address, the ZT 8995 I/O address may conflict with the I/O address of another board. Resolve the I/O address conflict by temporarily removing the other board until INFOSET or AUTOSET8 can be executed and the I/O address changed.

The INFOSET program sets the ZT 8995's initial operating mode and interrupt, but it does not provide any diagnostics. Execute this program from the DOS command line when you first receive the board. The command line format is listed below:

```
INFOSET <I/O address> <IRQ level> <Mode> <Media Selection>
```

Where:

<I/O address> should be 240h, 280h, 2C0h, 300h, 320h, 340h or 360h

<IRQ level> should be 3, 4, 5, 9, 10, 11, 12 or 15

<Mode> should be I/O or MEM

<Media Selection> should be UTP, THIN or THICK

Examples:

To set the ZT 8995-D1 board to a base I/O address of 300h, using interrupt level IR9 the command line is:

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```
INFOSET 300 9 I/O UTP
```

To set the ZT 8995-D2 board to a base I/O address of 280h, using interrupt level IR5, and thin Ethernet (connector J4) the command line is:

```
INFOSET 280 5 I/O THIN
```

If you plan to use the AUI connector (J3) the command variable "THICK" replaces "THIN" in the command line. See also the jumper description for W10.

Interrupt Scheme

The ZT 8995 supports the selection of one of four backplane interrupts and three frontplane interrupts via software control.

The on-board DP83905 (AT/LANTIC controller chip) must be programmed to use the encoded mode interrupt scheme. To do this, set the INTMODE bit in Configuration Register C HIGH (logic 1). The values in bits 3-5 of Configuration Register A select the desired interrupt.

Note: The INFOSET or AUTOSET8 programs set the proper bits in this register for you when you select your interrupt level.

The ZT 8995 uses an encoded interrupt scheme. A decoder maps the AT/LANTIC's interrupt to one of the STD 32 interrupts, as shown in the "Interrupt Selection" table. This interrupt scheme is Novell NE2000*plus* compatible. The INT3 pin from the AT/LANTIC strobes true when an interrupt is generated by the AT/LANTIC' s internal circuitry. The selected interrupt is output from the decoder (strobed LOW) for the duration of the INT3 strobe.

This means that the interrupt outputs are intended for use in an edge-triggered interrupt environment. They do not function correctly in a machine with level-triggered interrupts; interrupts may be missed.

By definition, the STD 32 bus uses edge-triggered interrupts; however, interrupts can be system selected to be either edge or level triggered.

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Interrupt Selection

Configuration Register A			Backplane	Interrupt
Bit 5 INT2	Bit 4 INT1	Bit 3 INT0	Signal	Level
0	0	0	INTRQ1*	IR3
0	0	1	INTRQ2*	IR4
0	1	0	INTRQ4*	IR5
0	1	1	INTRQ*	IR9
1	0	0	FP3*	IR10
1	0	1	FP5*	IR11
1	1	0	FP7*	IR12
1	1	1	JPR SLCT	IR15

Status LEDs

Five LEDs are located at the top of the board to indicate network status. The LEDs from left to right are: POLARITY (POL), COLLISION (COL), TRANSMIT (XMT), LINK (LNK) and RECEIVE (REC).

- The POL LED is lit when the TPI module detects seven consecutive link pulses or three consecutive receive packets with reversed polarity.
- The COL LED is lit for approximately 50 ms whenever a collision is detected.
- The XMT LED is lit for approximately 50 ms whenever the on-board AT/LANTIC controller transmits data.
- In TPI mode, the LNK LED is lit while link pulses are being received. This indicates that the twisted-pair connection is active.
- The REC LED is lit for approximately 50 ms whenever received data is detected.

Configuration Options

Please refer to National Semiconductor's Local Area Networks data book for detailed information on the DP83905 AT/LANTIC hardware for a more detailed explanation of this section.

The ZT 8995 does not require many jumpers because most of the configuration options for the board can be programmed by software. The serial EEPROM can also be written

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to by the on-board AT/LANTIC, allowing the configuration to be changed and saved. The memory map of the EEPROM is shown in the "EEPROM Contents" table.

The fields in the EEPROM are defined as:

Configuration Register A - Stores the base I/O Address and Interrupt number that the board is currently using. The AT/LANTIC has write access to this location. See the "Configuration Register A" bit description below.

Configuration Register B - Stores the Physical Layer Interface and programmable bus options. The AT/LANTIC has write access to this location. Refer to the "Configuration Register B" bit description below.

Configuration Register C - Stores the Boot PROM address and other hardware-specific configuration options. The AT/LANTIC cannot write to this location. See the "Configuration Register C" bit description below.

42h - This location (08h) must contain 42h (ASCII 'B'). When W17 is installed (low), the software will read this location in the PROM Store register of the AT/LANTIC and determine that the board is in an 8-bit STD slot. The AT/LANTIC cannot write to this location.

57h - This location (07h) must contain 57h (ASCII 'W'). When W17 is removed (high), the software will read this location in the PROM Store register of the AT/LANTIC and determine that the board is in a 16-bit STD 32 slot. The AT/LANTIC cannot write to this location.

CHECKSUM - This location is used only in Shared RAM mode. The checksum is used to verify the Ethernet Address and the board type. The two's compliment addition of the last eight bytes (03h..00h) must equal FFh, otherwise there is an error. The value of the checksum is determined from this. The AT/LANTIC cannot write to this location.

BOARD TYPE - This location is used only in Shared RAM mode. The Board Type indicator tells the network driver what hardware is being used. The AT/LANTIC cannot write to this location. When the board is configured to operate in WD8003EBT compatible Shared RAM mode, the Board Type should be 05h.

ETHERNET ADDRESS - The last six bytes of the EEPROM contain the Ethernet Address issued by the IEEE. These bytes are programmed uniquely prior to fitting the device onto the board because the AT/LANTIC is unable to write to these locations.

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EEPROM Contents

	D15 .. D8	D7 ..D0
0Fh	Not used	Config Reg. C
0Eh	Config Reg. B	Config Reg. A
0Dh	Not used	Not used
0Ch	Not used	Not used
0Bh	Not used	Not used
0Ah	Not used	Not used
09h	Not used	Not used
08h	42h	42h
07h	57h	57h
06h	Not used	Not used
05h	Not used	Not used
04h	Not used	Not used
03h	Checksum	Board Type
02h	E'Net Address 5	E'Net Address 4
01h	E'Net Address 3	E'Net Address 2
00h	E'Net Address 1	E'Net Address 0

Configuration Register A - Stores the base I/O Address and Interrupt number that the board is currently using. The AT/LANTIC has write access to this location. See the "Configuration Register A" bit description below.

Configuration Register B - Stores the Physical Layer Interface and programmable bus options. The AT/LANTIC has write access to this location. Refer to the "Configuration Register B" bit description below.

Configuration Register C - Stores the Boot PROM address and other hardware-specific configuration options. The AT/LANTIC cannot write to this location. See the "Configuration Register C" bit description below.

42h - This location (08h) must contain 42h (ASCII 'B'). When W17 is installed (low), the software will read this location in the PROM Store register of the AT/LANTIC and

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determine that the board is in an 8-bit STD slot. The AT/LANTIC cannot write to this location.

57h - This location (07h) must contain 57h (ASCII 'W'). When W17 is removed (high), the software will read this location in the PROM Store register of the AT/LANTIC and determine that the board is in a 16-bit STD 32 slot. The AT/LANTIC cannot write to this location.

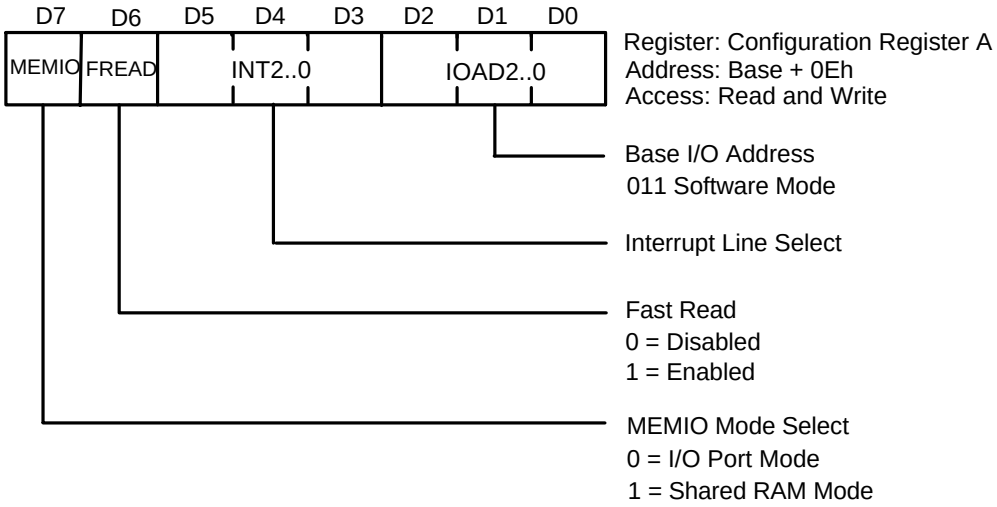
CHECKSUM - This location is used only in Shared RAM mode. The checksum is used to verify the Ethernet Address and the board type. The two's compliment addition of the last eight bytes (03h..00h) must equal FFh, otherwise there is an error. The value of the checksum is determined from this. The AT/LANTIC cannot write to this location.

BOARD TYPE - This location is used only in Shared RAM mode. The Board Type indicator tells the network driver what hardware is being used. The AT/LANTIC cannot write to this location. When the board is configured to operate in WD8003EBT compatible Shared RAM mode, the Board Type should be 05h.

ETHERNET ADDRESS - The last six bytes of the EEPROM contain the Ethernet Address issued by the IEEE. These bytes are programmed uniquely prior to fitting the device onto the board because the AT/LANTIC is unable to write to these locations.

Configuration Register A

Please refer to the AT/LANTIC data sheet for a detailed description of the bits in Configuration Register A. The register contents can be changed only by an I/O read from this location followed immediately by an I/O write to this location. The following descriptions show the bit definitions and their default settings.



IOAD2..0 (D2..0) - The Base I/O Address for the ZT 8995 is programmed by these three bits. When programmed to [0 0 1], the ZT 8995 will power up in software mode and not respond to any I/O Address. However, it will monitor the parallel port (278h) for four consecutive writes. On the fourth write to 278h, bus data will be loaded into

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Configuration Register A, setting the I/O address for the board. This is done so that the board will not conflict with other I/O slaves in the system. The method the AT/LANTIC uses for monitoring the parallel port and activating configuration load is unique; no other device/software is likely to perform four consecutive writes to this location.

INT2..0 (D5..3) - Based on Configuration Register C bit 5, these three bits select the interrupt line that is directly driven or the decode that is used for coded interrupts. The ZT 8995 is shipped programmed to drive coded interrupts, specifically IRQ9, [INT2..0 = 0 1 1], which is driven across backplane signal INTRQ*.

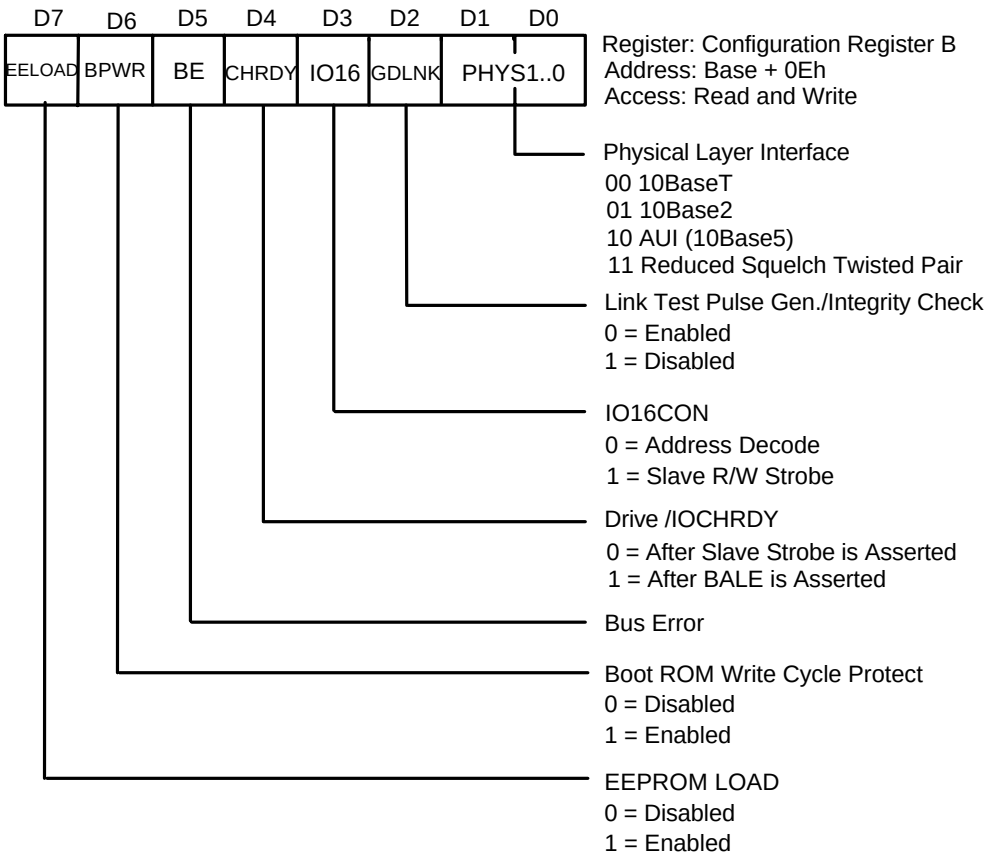
FREAD (D6) - This enables the Fast Read option of the AT/LANTIC's Remote DMA Read operation. The ZT 8995 is shipped with the FREAD function disabled. [FREAD = 0].

MEMIO (D7) - Selects either I/O Port mode or Shared RAM mode. The ZT 8995 comes configured to run in I/O Port mode. [MEMIO = 0].

Configuration Register B

Please refer to National Semiconductor's AT/LANTIC data sheet for a detailed description of the bits in Configuration Register B. The register contents can be changed only by an I/O read from this location followed immediately by an I/O write to this location. The following descriptions show the bit definitions and their default settings.

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PHYS1..0 (D1..0) - The Physical Layer Interface bits select the type of physical layer being used on the board. This could be 10BaseT, 10Base2, AUI (10Base5) or Reduced Squelch Twisted Pair. The ZT 8995 comes configured to use 10BaseT. [PHYS1,0 = 0,0].

GDLNK (D2) - This bit enables link test pulse generation and integrity checking when using twisted pair. It can also be read to indicate status. Link pulse generation and checking is disabled by writing a 1 to this bit. The ZT 8995 is shipped with link testing enabled.

IO16CON (D3) - One of two methods of generating /IO16 is chosen using this bit. In normal operation, /IO16 is driven off of the address decode. /IO16 can be configured to be driven from the slave read or write strobe by this bit. The ZT 8995, as shipped, will generate /IO16 from address decode. [IO16CON = 0].

CHRDY (D4) - The way the AT/LANTIC drives /IOCHRDY can be selected by programming this bit. When low, the AT/LANTIC will drive /IOCHRDY after a slave strobe is asserted. When high, the AT/LANTIC will drive /IOCHRDY on BALE being asserted; this may be required when being used with some chipsets that sample /IOCHRDY early. The ZT 8995, as shipped, will drive /IOCHRDY after slave strobe is asserted.

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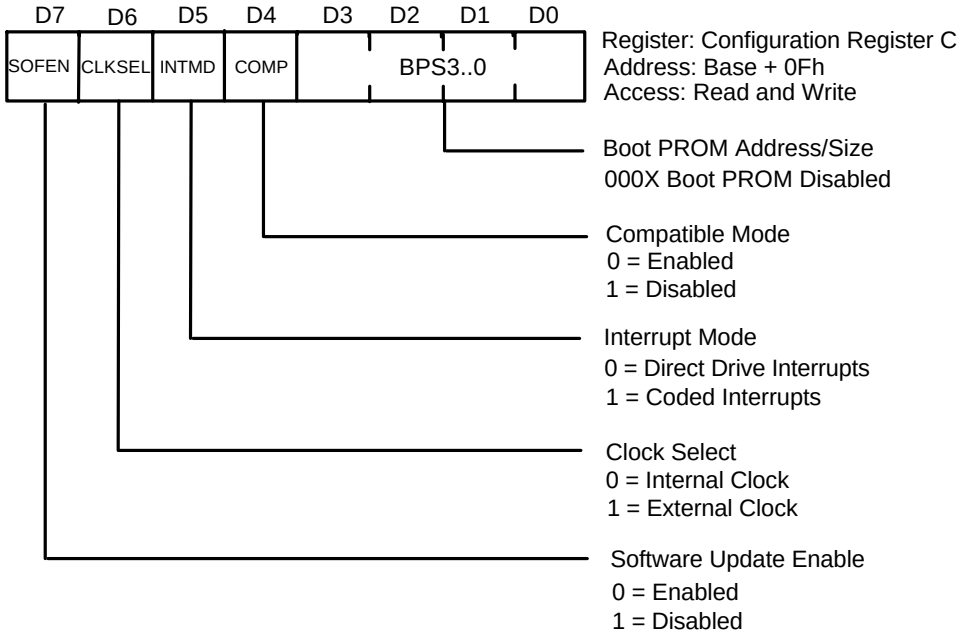
BE (D5) - This bit can be read by software to determine if there was a bus error. A bus error will occur if the AT/LANTIC attempts to insert wait states into a system access and the system terminates the cycle without inserting wait states.

BPWR (D6) - This bit protects Boot PROM write cycles. When high, the AT/LANTIC can generate write cycles to the Boot PROM. This feature is intended for use with writable Boot storage devices. The ZT 8995 does not support this feature, so this is programmed low. Refer to Configuration Register C.

EELOAD (D7) - The EELOAD bit enables/disables the AT/LANTIC from writing the configuration information into the EEPROM. This bit must be set before running the EEPROM load algorithm documented in the AT/LANTIC data sheet.

Configuration Register C

Please refer to the AT/LANTIC data sheet for a detailed description of all the bits in Configuration Register C. The register contents can be changed only by an I/O read from this location followed immediately by an I/O write to this location. The following descriptions show the bit definitions and their default settings.



BPS3..0 (D3..0) - These four bits select the memory address and size of the Boot PROM. If BPS3..0 is equal to [0 0 0 X], the Boot PROM is disabled. The ZT 8995 comes configured to operate with the boot PROM disabled. Refer to the following table, "Boot PROM Address/Size Selection", for valid addresses and sizes.

COMP (D4) - When this bit is programmed high, the AT/LANTIC's memory uses the full 64K bytes of RAM. When low, the memory map is compatible with either the NE2000*plus* or the WD8003EBT (16K bytes of RAM). The ZT 8995 is configured to run in compatible mode with this bit low (Logical 0).

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INTMODE (D5) - This bit selects which interrupt mode the AT/LANTIC controller will use. When low, direct drive interrupts are used. When high, coded interrupts are used. The ZT 8995 must be configured to use coded interrupts (bit is high in this AT/LANTIC register).

CLKSEL (D6) - When low, the NIC core of the AT/LANTIC is clocked by the 20 MHz clock on the X1 input. When high, an external clock other than 20 MHz can be used to clock BSCK. The ZT 8995 must be configured to run on the internal 20 MHz clock.

SOFEN (D7) - This bit enables software to update Configuration Registers A and B. When high, the configuration registers are not accessible by software. The ZT 8995 is configured to allow software such as INFOSET.EXE and AUTOSET8.EXE to update the configuration registers.

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Boot PROM Address/Size Selection

Bit 3	Bit 2	Bit 1	Bit 0	Address	Size (I/O / Shared Memory)
0	0	0	X	X	No Boot PROM
0	0	1	0	0C000h	8K/16K
0	0	1	1	0C400h	8K/16K
0	1	0	0	0C800h	8K/16K
0	1	0	1	0CC00h	8K/16K
0	1	1	0	0D000h	8K/16K
0	1	1	1	0D400h	8K/16K
1	0	0	0	0D800h	8K/16K
1	0	0	1	0DC00h	8K/16K
1	0	1	0	0C000h	32K/32K
1	0	1	1	0C800h	32K/32K
1	1	0	0	0D000h	32K/32K
1	1	0	1	0D800h	32K/32K
1	1	1	0	0C000h	64K/64K
1	1	1	1	0D000h	64K/64K

Shared Memory Mode Operation

The ZT 8995 can be configured for Shared Memory Mode operation. The operating mode and base I/O address of the AT/LANTIC Controller are determined by Configuration Register A. Shared Memory Mode operates under the structure illustrated in the figure "Shared Memory Mode I/O Address Map."

The following topics describe the functionality of the 8/16 detection register and the two Shared Memory Mode Control registers. These registers are available only when Configuration Register A is programmed for Shared Memory Mode operation.

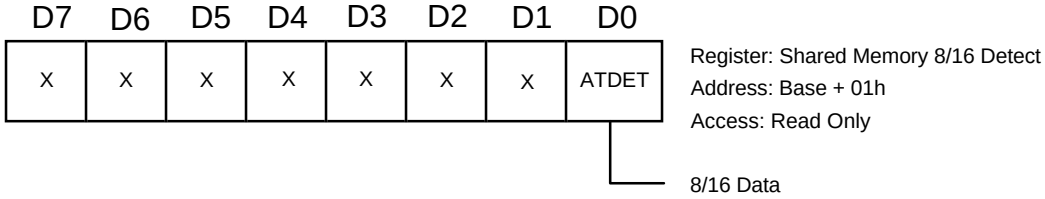
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Base + Addr	D7-0	
00h	Control 1	
01h	AT detect	(Read only)
02h	Unused	
03h	Unused	
04h	Unused	
05h	Control 2	
06h	Unused	
07h	Unused	
08h	Node addr 0	(Read only)
09h	Node addr 1	(Read only)
0Ah	Node addr 2	(Read only)
0Bh	Node addr 3	(Read only)
0Ch	Node addr 4	(Read only)
0Dh	Node addr 5	(Read only)
0Eh	05h	(Read only)
0Fh	Checksum	(Read only)
10h to 1Fh	NIC registers	

ZT8995

Shared Memory Mode I/O Address Map

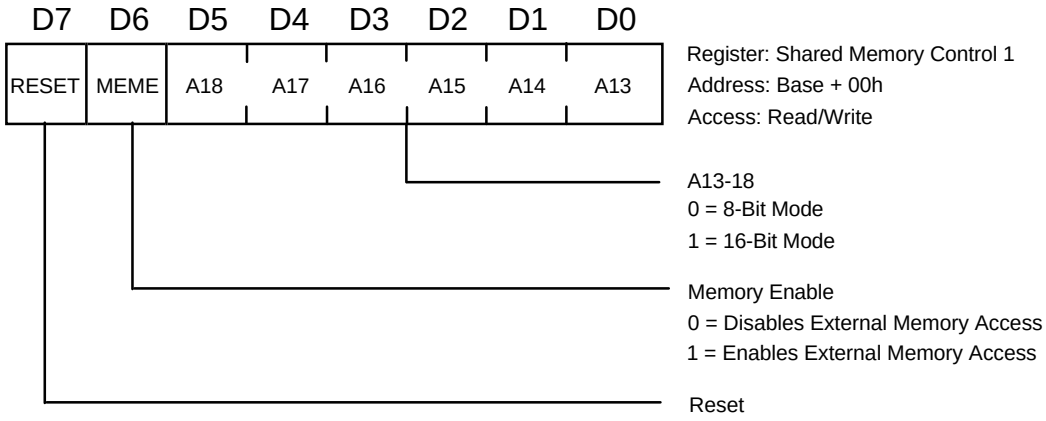
Shared Memory 8/16 Detect Register



8/16 Data (D0) - This bit shows the value of jumper W17 and can be read by software to determine whether the ZT 8995 is operating as an 8- or 16-bit board. When D0 is read as a logical 1 the ZT 8995 is in 16-bit mode. When this bit is read as a logical 0 the ZT 8995 is in 8-bit mode.

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Shared Memory Control Register 1

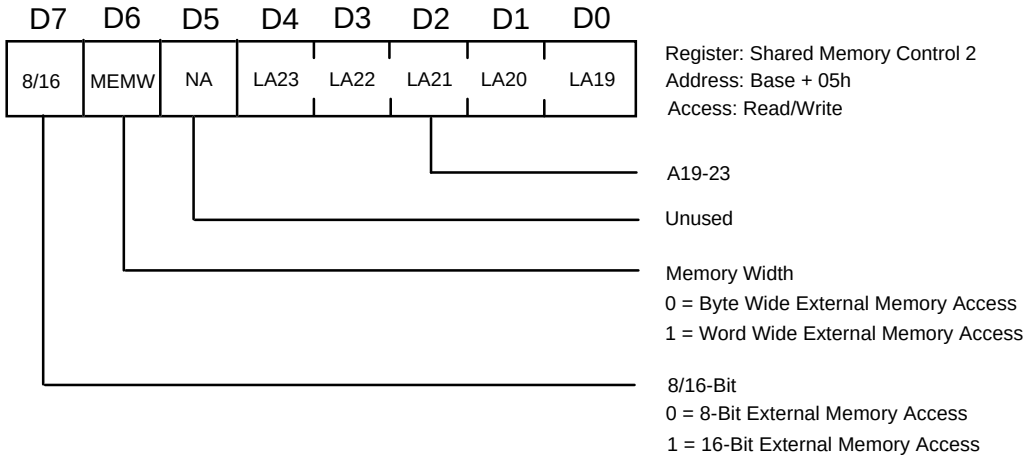


A13 - A18 (D0 - D5) - This is the lower part of the address register used to determine the position of the ZT 8995's memory within the system memory map.

MEME (D6) - Enables external memory accesses when held at logical 1. This bit powers up as logical 0 so you must program the base memory address and set this bit to logical 1 to enable the memory into the system's memory map.

RESET (D7) - Resets the NIC core of the AT/LANTIC controller chip on the ZT 8995.

Shared Memory Control Register 2



A19 - A23 (D0 - D4) - This is the upper part of the address register used to determine the position of the ZT 8995's memory within the system memory map.

D5 - Unused.

MEMW (D6) - This bit sets the width of external memory. When D6 is set to logical 0, external memory is accessed as byte wide, so only 8 Kbytes of memory are available.

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When D6 is set to logical 1, external memory is accessed as word wide and 16 Kbytes are available. When D7 is set to logical 1, this bit must also be set to logical 1.

8/16 (D7) - Set this bit to logical 1 to allow 16-bit system accesses to external memory. Set to logical 0 to allow only 8-bit accesses. Generation of M16 output is allowed when D7 is set to logical 1.

Configuring Multiple Boards

To configure multiple ZT 8995s for use in a single system, you must give each board a unique I/O address as described in "Using The Setup Program". Insert each board into your system and configure it before inserting the next board. This must be done because each board is shipped with the same software disabled mode that monitors access to port 278h. A conflict will occur if more than one board is installed at the same time. To install multiple boards, use the following procedure:

1. Turn off the system.
2. Install one board and turn on the system.
3. Using the INFOSET program, configure the board you just installed.
4. Select any ***available*** I/O base address.
5. Select and alter other configuration options as necessary.
6. Save the configuration, then exit the setup program.

Repeat this procedure until all boards in your system are configured. When the ZT 8995 is installed and configured, you are ready to test the board and cable, install the software drivers, and load the network software. Each of these topics is discussed in the following topics.

Testing a Board

Once the ZT 8995 is installed, use the diagnostic programs AUTOSET8 or INSPECT contained on the floppy disk to check the board installation. Both DOC (Word for Windows) and TXT files provide instructions for using the program. To execute the diagnostic program, change to the \SETUP subdirectory and type the name of the executable program you prefer.

Some of the diagnostic program tests do not operate properly unless the board is attached to the media for which the board is configured (Ethernet Attachment Unit Interface (AUI) or a Thin Ethernet BNC "T" connector that has two terminators connected, or a Twisted Pair cable). Refer to Appendices B and C for information on connecting boards together.

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Because interrupts are used by the diagnostic program, they must be properly selected for the diagnostic program to complete its tests. Once selected, the ZT 8995 interrupt signal must be jumpered to utilize either a backplane signal (factory default is INTRQ*) or a frontplane signal. This signal must be connected to the processor board interrupt request input. The CPU interrupt request input should be the same as the interrupt request (IRQ) selected using the setup program. See the "Interrupt Selection" table and the descriptions for jumpers W11-14 for more information.

The ZT 8995 selection for IR9 drives the interrupt request on the backplane signal INTRQ*, which is compatible with all Ziatech factory default jumpered STD 32 processor boards (INTRQ* is routed to IR9 of their interrupt controllers). See "Interrupts" in Chapter 3 for additional information.

Installing The Drivers

The software driver for each installed ZT 8995 must use the actual parameters you saved with the setup program for that board. The I/O base address, RAM base address, and IRQ channel used by each ZT 8995 must agree with the values for those parameters that are used by the board's software driver. Making modifications to the software driver parameters is described below.

Modifying The Drivers

The method you use to change the software driver parameters depends on your network operating system software. The ZT 97115 diskette has a separate subdirectory for different types of software drivers. Your network software should contain information for installation and use of these drivers.

Loading The Network Software

When the ZT 8995 board and cable are installed and verified, load the network operating system software onto the system. Use the instructions provided with the network software package. If a user-installed EPROM is on the board, you may need to prepare the network software for PROM operation. Refer to the instructions provided with the PROM device and your network software.

TROUBLESHOOTING HINTS

If the ZT 8995 does not appear to be functioning, follow the steps below to verify installation:

1. Verify that the network cable is securely attached to the RJ-45 connector (J2) on the ZT 8995-D1 or to the Thin Ethernet BNC connector (J4) or the Ethernet DB15 AUI network connector (J3) on the ZT 8995-D2. Please review Appendix B and Appendix C for additional cabling information.

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2. Check the cable connection to other computers. In Thin Ethernet systems, check all computers daisy chained to the computer you are troubleshooting. In Ethernet systems, check the drop cable connection (AUI) at the MAU transceiver.

3. Verify that 50 ohm cable terminators are installed as required on Thin Ethernet systems. Terminators must be 50 ohm impedance (within 2%) or errors may occur. Use an ohmmeter to measure the terminators.

4. Make sure the interconnecting cables meet IEEE standard requirements as defined in Appendix C. Use an ohmmeter to measure each cable and cable connector.

5. Verify that there are no memory space conflicts between the ZT 8995 RAM buffer (in shared memory mode) or PROM address (if enabled) and any other functions (such as EGA, VGA, etc.) installed in your computer.

6. Make sure that the ZT 8995 has been configured correctly using the setup program. Verify the board passes the on-board diagnostics with AUTOSET8.

7. Be sure the ZT 8995 interrupt output is connected to the processor board interrupt input corresponding to the IRQ selection made with the setup program.

8. Review the installation documentation for any software copied from the ZT 97115 disk. Were all the necessary files copied? Have the software drivers been modified to reflect the configuration made with the setup program?

9. If more than one ZT 8995 is installed in your computer, make sure each one has a different I/O address, RAM/PROM address, and IRQ selection. Multiple boards must be installed and set up one at a time.

10. Verify with the diagnostic program that the ZT 8995 is working before trying the network operating system software.

11. Verify that the network software is loaded correctly.

12. If a PROM device is installed on the ZT 8995, verify the correct PROM size using the setup program. Verify the PROM type, size, and speed and that all pins are seated properly in the socket.

13. If data transfer problems between two network nodes exist, review the IEEE 802.3 information in Chapter 3.

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FURTHER INFORMATION

You can obtain further information on IEEE 802.3 and debugging techniques from the following sources:

IEEE 802.3	*IEEE 802.3 Local Area Networks Standard* is available from the Institute of Electrical and Electronics Engineers. Inc., 445 Hoes Lane, P. O. Box 1331, Piscataway, NJ 08855-1331, USA. This is a comprehensive standard encompassing several media types and techniques for signal rates. It was released for 10 Mb/s baseband implementation. The Media Access Control (MAC) sublayer of the Data Link Layer and the Physical Layers are described. These layers correspond closely to the lowest layer of the International Standards Organization (ISO) Model for Open System Interconnection (OSI).
Debugging	Several troubleshooting techniques are described in the August, 1989 edition of *LAN Technology* by M&T Publishing Inc., 501 Galveston Drive, Redwood City, CA 94063, USA. The differences between Ethernet and IEEE 802.3 are covered. The CSMA/CD protocol, physical characteristics, and software considerations are also described.
NS Data Sheet	Refer to National Semiconductor's 1993 or later edition of their "Local Area Networks Databook" for detailed information on the DP83905 Network Interface Controller, its registers and programming techniques.

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3. THEORY OF OPERATION

This chapter presents a high-level look at how the ZT 8995 functions. It includes sections covering commonly asked questions, the STD interface, Ethernet interface, and diagnostic LEDs. The "Functional Diagram" figure illustrates the basic functional blocks of the ZT 8995.

FREQUENTLY ASKED QUESTIONS

- **What are the differences between Ethernet and IEEE 802.3?**
  - Ethernet from Xerox specifies 50 ohm coax cabling only. IEEE 802.3 (also called Ethernet) specifies different types of coax, twisted-pair and fiber optic cabling.
  - Transceiver connection signals are slightly different. The AUI transceiver cable must match the DB15 connector found on the interface. Some transceivers provide jumpers for either connection. The ZT 8995 is an IEEE 802.3 compliant interface.
  - The data frame formats are incompatible. Fortunately, most network operating systems and application programs can be configured for Ethernet or IEEE 802.3 data packets. The ZT 8995 hardware is compatible with IEEE 802.3.
- **What cable media is available for Ethernet?**
  - Media types range from thin coax (Thin Ethernet, Cheapernet) to thick coax (Ethernet, IEEE 802.3), twisted-pair wiring, and fiber optic cable. Appendix B describes each interconnection medium in more detail.
  - Media types determine network topology (star, bus). Media types can be mixed. Appendix C illustrates a complex network consisting of various cable media.
- **What are the differences between Ethernet and Thin Ethernet?**
  - Thin Ethernet uses low cost RG58 coax cable. Ethernet uses a more expensive Teflon™ coated, double shielded coax cable. Teflon cable is used in environments in which fire is possible, as ordinary coax cable releases dangerous cyanide gas when it burns.
  - Thin Ethernet allows network spans of 900 meters with segment lengths of 185 meters. Ethernet allows network spans of 2500 meters with segment lengths of 500 meters.
  - Both use 50 ohm cable and termination operating at 10 Mbps.
  - Twisted-pair Ethernet (TPI) also known as 10BaseT uses inexpensive telephone wiring that may already be installed in many applications. An RJ-45 connector

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and 10BaseT transceiver is provided on the ZT 8995-D1. 10BaseT will drive a maximum cable length of 100 m.

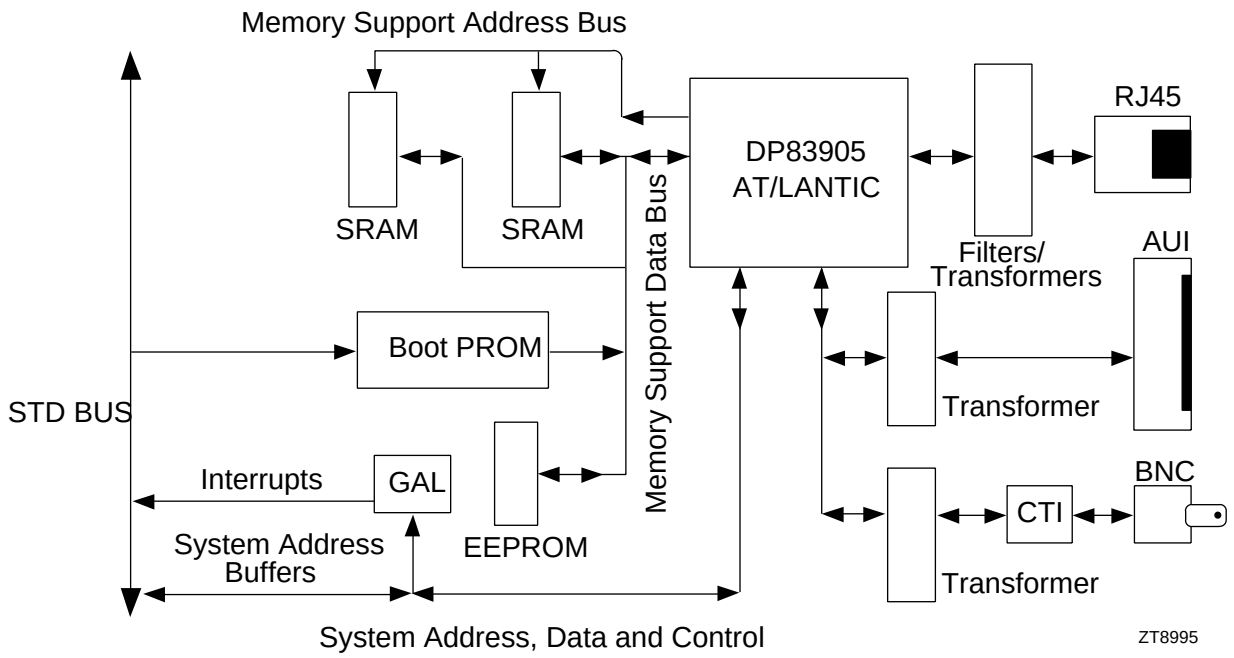
- **Is the ZT 8995 compatible with the WD 8003EB interface?**
  - Yes, the two boards are identical for software operation. The same software driver disk can be used for either board.
  - At the hardware level, the two boards are quite different and the ZT 8995 needs to be configured specifically for WD 8003EB compatibility (shared RAM mode, etc.). Unlike the WD 8003EB board, the ZT 8995 also features isolation of the AUI connector. This feature helps prevent damage to the ZT 8995 from external cable glitches.
  - Both boards utilize the IEEE 802.3 latching DB15 connector to insure compatibility with IEEE 802.3 AUI devices.
- **Is the ZT 8995 really STD bus format?**
  - The ZT 8995 uses no extensions or porches to implement 10BaseT or Thin Ethernet interfaces on a standard STD size board.
  - The ZT 8995 requires only one STD slot at .625" centers. Two slots are required if .500" centers are used.

STD INTERFACE

The ZT 8995 interfaces with the STD bus when the decode logic programmed into the DP83905 Network Interface Chip (NIC) detects an I/O or memory address for the ZT 8995. Refer to the illustration "Functional Diagram" figure. Data is written to or read from the ZT 8995 as required by the command decode and buffer control inside the NIC.

Communications between the STD processor and the ZT 8995 are made via DMA accesses to the NIC (I/O port mode, which is NE2000*plus* compatible) or by the 16K dual-ported (shared memory mode) packet RAM and I/O registers on the ZT 8995. Normal communications between the processor and the adapter consist of remote DMA access to the NIC (I/O mode) or by writing transmit frames to shared memory (shared memory mode) and then initiating a packet. The network interface then performs a DMA transfer of the frame data between the shared packet RAM and the network interface. In the receive direction, the network interface performs a DMA transfer of received frames to the packet RAM, and then interrupts the processor when the completed packet has been received. Alternately, the processor does not have to be interrupted, but can poll the network controller to determine if a packet has been received.

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Functional Diagram

I/O Port Decode

The ZT 8995 requires 32 contiguous I/O address ports. These I/O ports are decoded by the 16-bit I/O decode logic and the LAN interface chip. The LAN interface chip decodes 10 of the 16-bit I/O addresses while the remaining six bits are decoded by the PAL as a "low" or logical 0 for complete 16-bit I/O decode logic without redundancy. IOEXP is ignored and not decoded.

Shared Memory Addressing

When the ZT 8995 is configured for shared memory support (not NE2000*plus* compatible) the Memory addresses are decoded by the DP83905 for selecting either the Ethernet packet RAM or the PROM socket. The ZT 8995 board's packet RAM may be assigned any 16K memory space but should be located within a range of addresses located above the system memory (typically 640K). The ZT 8995 may require as much as 48 Kbytes of memory space for its 16 Kbyte RAM buffer and a user-installed 32 Kbyte PROM. Both the RAM buffer and the PROM device are located in the 24-bit memory range of 000000 to FFE000h. If you require 20-bit memory addressing, use the setup program to configure the lower 20 bits of address and set the upper four bits to 0; then set the upper four bits of the memory address bus to 0 with jumpers W4-7.

EPROM Socket

The ZT 8995 includes a PROM socket that can accommodate 32, 64, 128, or 256 Kbyte parts where only the top 32 Kbyte block is accessible. In shared memory mode (not

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NE2000 compatible) the PROM can be mapped into any 8, 16, 32, or 64 Kbyte boundary beginning at one of eight software selectable locations between 0C000h and 0D000h.

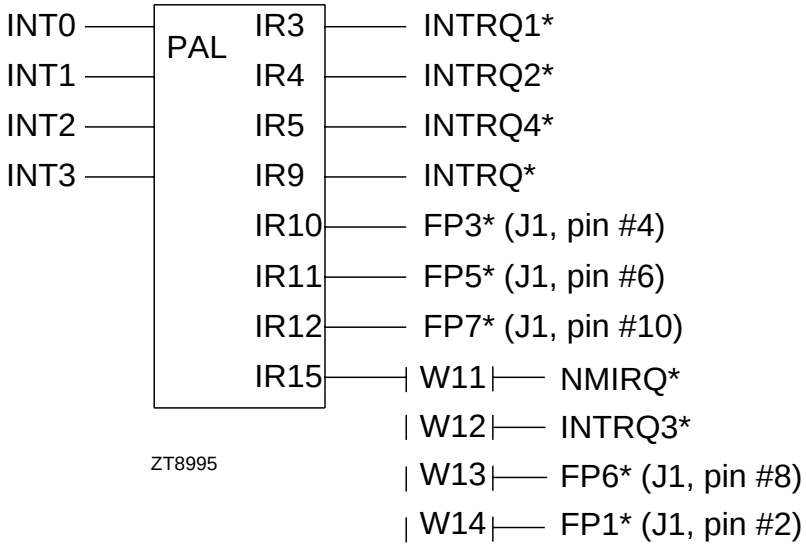
If a PROM device is installed on the ZT 8995, memory space must be allocated to it. A register within the LAN interface chip is used to save the address bits that decode both the PROM socket and the size of the part. Depending on the size of the PROM device installed, the recommended PROM base address options are D0000h or D8000h.

Interrupts

Interrupts are supported by the ZT 8995. Interrupts can be output on backplane signals INTRQ*, INTRQ1*, INTRQ2*, INTRQ3*, INTRQ4*, NMIRQ*, and IRQx. They can also be output on the frontplane connector. The "Interrupt Diagram" figure illustrates the ZT 8995 interrupt structure.

Interrupts are used by the diagnostic program. Interrupts must be properly configured for the diagnostic program to complete all of the on-board tests (a typical selection is IR9 driven across backplane signal INTRQ*). Note: if IRQ15 is selected, the ZT 8995 interrupt signal must be jumpered to utilize INTRQ3*, NMIRQ*, or one of the frontplane signals FP1* or FP6*. This signal must be connected to the processor board interrupt request that matches the interrupt request (IRQ levels) selected using the setup program INFOSET or AUTOSET8. See the "Interrupt Selection" table and the jumper descriptions for W11-14 for more information.

Note: The ZT 8995 selection for IR9 on backplane signal INTRQ* is compatible with all Ziatech factory default jumpered processor boards.



Interrupt Diagram

Note: Frontplane numbers may differ from CPU to CPU in their interrupt routing.

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Backplane Signals

Interrupts can be output on backplane signals INTRQ*, INTRQ1*, INTRQ2* (CNTL), INTRQ3*, INTRQ4*, NMIRQ*, or IRQx. These signals are software selectable, tri-state, logical 0 signals. IRQx is a logical 1 STD 32 slot-specific interrupt signal.

Frontplane Signals

The ZT 8995 frontplane interrupts are tri-state logical 0 signals that are software selectable for FP3*, FP5*, FP7*, and jumper selectable for FP1* or FP6* when the ZT 8995 is configured for interrupt level IR15. These frontplane signals can be routed to the processor board with a frontplane ribbon cable.

Additional information on interrupts can be found in Ziatech's *Application Note #8*, available on Ziatech's web site at http://ziatech.com/graphics/appn8.pdf. Adobe Acrobat Reader must be installed on your computer to access this file. You can download the latest version by clicking "Getting Acrobat Reader" on the Adobe web site at http://www.adobe.com.

Wait States

The ZT 8995 incorporates a wait state generator for STD-80 bus compatibility. The wait state generator inserts one wait state until the ready signal from the network interface chip can be asserted. This is required for STD-80 compatible wait state timing and requires that W19 and W16 be inserted.

If an STD 32 compatible CPU provides the equivalent STD bus timing by inserting one wait state on its own, and can sense wait requests being asserted later in the bus cycle, W16 can be removed. When W16 is removed, wait states are asserted by the WAITRQ* signal only as needed by the network interface chip. Ziatech's ZT 8910 can operate with W16 removed. All other Ziatech CPU boards require that W16 be installed. Removing W19 will disable all wait state requests and should remain installed.

ETHERNET INTERFACE

The National Semiconductor DP83905 Network Interface Controller is compatible with IEEE 802.3. This device is a CMOS VLSI device designed to interface with Carrier Sense Multiple Access/Collision Detection (CSMA/CD) networks, including Twisted-pair Ethernet (10BaseT), Ethernet (10Base5) and Thin Ethernet (10Base2, Cheapernet). All Media Access Control (MAC) layer functions are provided for transmission and reception of data packets.

IEEE 802.3

The term "Ethernet" is also used to describe the publicly available CSMA/CD specification drafted by the IEEE 802.3 committee, although there are some differences

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between Ethernet and IEEE 802.3 standards. Several differences are listed in the "Older Ethernet and IEEE 802.3 Differences" table.

If older Ethernet and IEEE 802.3 hardware/software are improperly mixed on a network, different sections of the network suffer from a chronic inability to communicate with each other, while no apparent hardware faults show up during testing. The ZT 8995 is hardware compatible with the IEEE 802.3 frame format and ideally should not be mixed with the older (pre-certified) ethernet controllers.

The frame format used by the transmission data link layer is typically defined by the network operating system and application software at the network layer or higher. Some software manufacturers include utilities that allow the system to be configured. For example, Novell provides a special utility called ECONFIG that allows the network administrator to configure the interface to either the Ethernet or IEEE 802.3 specification.

If incompatibilities persist, a protocol analyzer may reveal incongruities in the frame formats. Several protocol analysis tools are available for Ethernet and IEEE 802.3 networks. Vendors of complete systems include Network General Corp., Hewlett-Packard Co., and Excelan, Inc.. FTP Software, Inc., which also supplies TCP/IP software, has developed a software-based tool that turns a workstation into an analyzer.

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Older Ethernet and IEEE 802.3 Differences

Feature	Ethernet	IEEE 802.3
Media types	50 ohm coax only	Different types of coax, twisted pair, and fiber optic support
Transceiver connection	Similar but some reserved pins	Similar but more shield pins
Frame formats	Incompatible	Incompatible

Twisted-Pair Ethernet (10BaseT) Connector

Twisted-pair Ethernet (10BaseT) uses smaller and less expensive telephone wiring that may already be installed at most facilities. An RJ-45 connector and 10BaseT transceiver is provided on the ZT 8995. Two unshielded twisted-pairs (22-26 gauge) are used for each cable segment. Cable segments are arranged in a star topology (unlike thin/thick, which are bus topologies) around a multi-port repeater. Twisted-pair Ethernet features:

- Maximum cable segment length of 320 ft. (100 m)
- Maximum number of nodes on a segment is one
- Maximum number of nodes on a network is 1024
- Maximum number of multiport repeats between any two nodes is four

Ethernet (AUI) Connector

Ethernet attaches to the ZT 8995 using a Media Attachment Unit (MAU) and an Attachment Unit Interface (AUI) in the following manner:

- The Ethernet cable connects to the MAU, which is a box containing transformers, an isolating DC/DC converter, and a cable transceiver circuit. Connect the coax cable directly to the MAU in one of the following ways:

  1. Use a "vampire" or "stinger" connector to pierce a hole through the intact coax cable and attach by pinching the cable.

  2. Cut the coax cable and install coax connectors to attach to the MAU.

  The first method is preferred because it causes less reflection in the cable and is easier to install. Please see Appendices B and C for more information.

- The AUI cable connects to the MAU. The AUI is a shielded cable with 15-pin subminiature "D" connectors at each end.

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- The end of the AUI cable opposite the MAU connects to a latching, 15-pin, subminiature "D" connector (J2) the front of the ZT 8995. The slide latch retention system found on J2 meets IEEE 802.3 requirements.

Thin Ethernet (BNC) Connector

As an alternative to the Ethernet AUI connector, Thin Ethernet (Cheapernet) uses smaller and less expensive BNC coax (RG58A/U). It connects to a BNC connector at the front of the ZT 8995 (J1). Normally a BNC "T" connector is attached to the BNC connector so that two RG58 A/U cables may be attached at this point. If the ZT 8995 is the first or last board on the network cable, the unused "T" connector is fitted with a 50 ohm (±2%) termination cap.

The on-board DP8392 coaxial transceiver interface connects the network interface controller to the Thin Ethernet cable. This circuitry replaces the MAU typically used to interface with the Ethernet cable. No external transceiver cable (AUI) is necessary because the DP8392 includes isolation transformers and uses a DC/DC converter.

DIAGNOSTIC LEDS

The ZT 8995 interface has separate transmit and receive diagnostic LEDs. These LEDs provide visual indication of network activity. Transmit activity is indicated by a red LED in the center of the LED block. Receive activity is indicated by the lowest green LED.

The red transmit indicator LED lights when the ZT 8995 sends a packet. Receive indicators (typically green) are illuminated on remaining interfaces while this occurs.

The green receive indicator LED lights when the interface detects any packet present on the cable. Detection is indicated when a packet is transmitted from the ZT 8995 or when other interfaces on the network transmit information. The packet need not be intended for the ZT 8995.

Additional LEDs are used to indicate proper cable link, polarity, and collisions. The LED sequence on the board from top (nearest the ejector) to bottom is as follows:

RED - polarity, illuminates if the twisted pair cable has inverted polarity

GREEN - link indicator, illuminates when a properly connected cable is detected

RED - Transmit, illuminates when the ZT 8995 transmits an information packet

GREEN - Receive, illuminates whenever a packet of information is detected on the network

RED - Collision, illuminates when a transmitted packet collides with another on the network

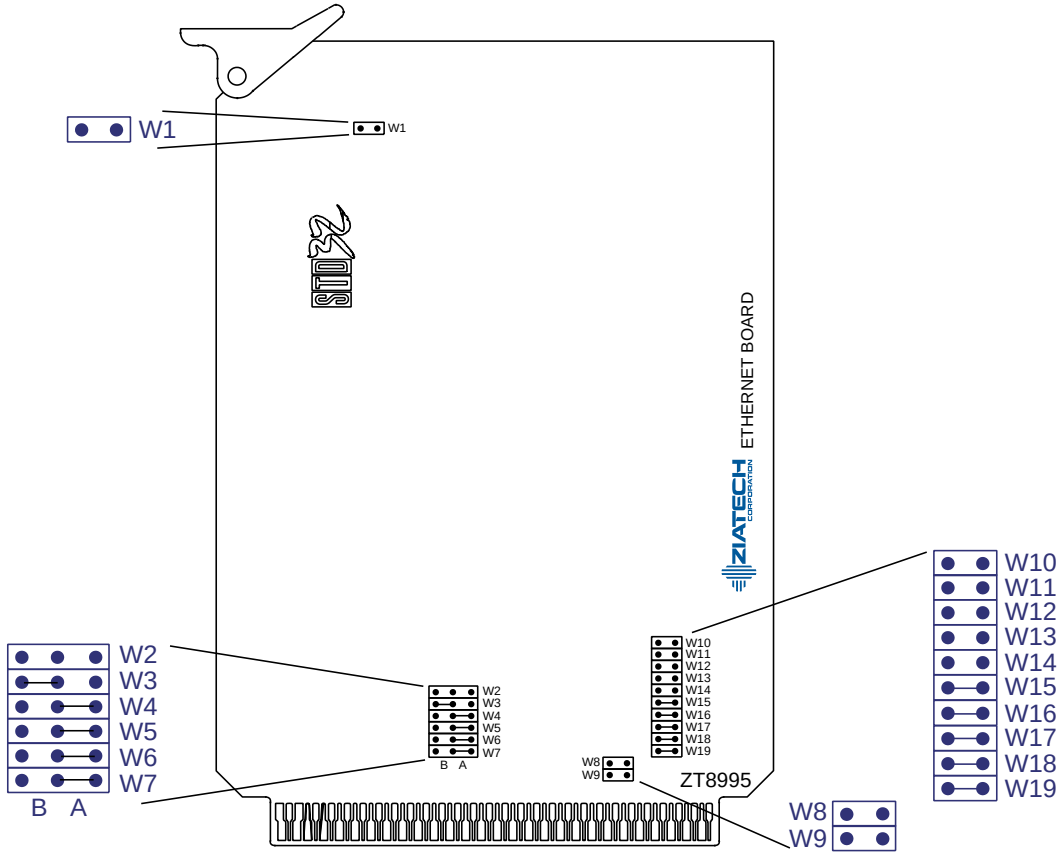
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A. JUMPER CONFIGURATIONS

The ZT 8995's jumpered options tailor the board's operation to specific application requirements.

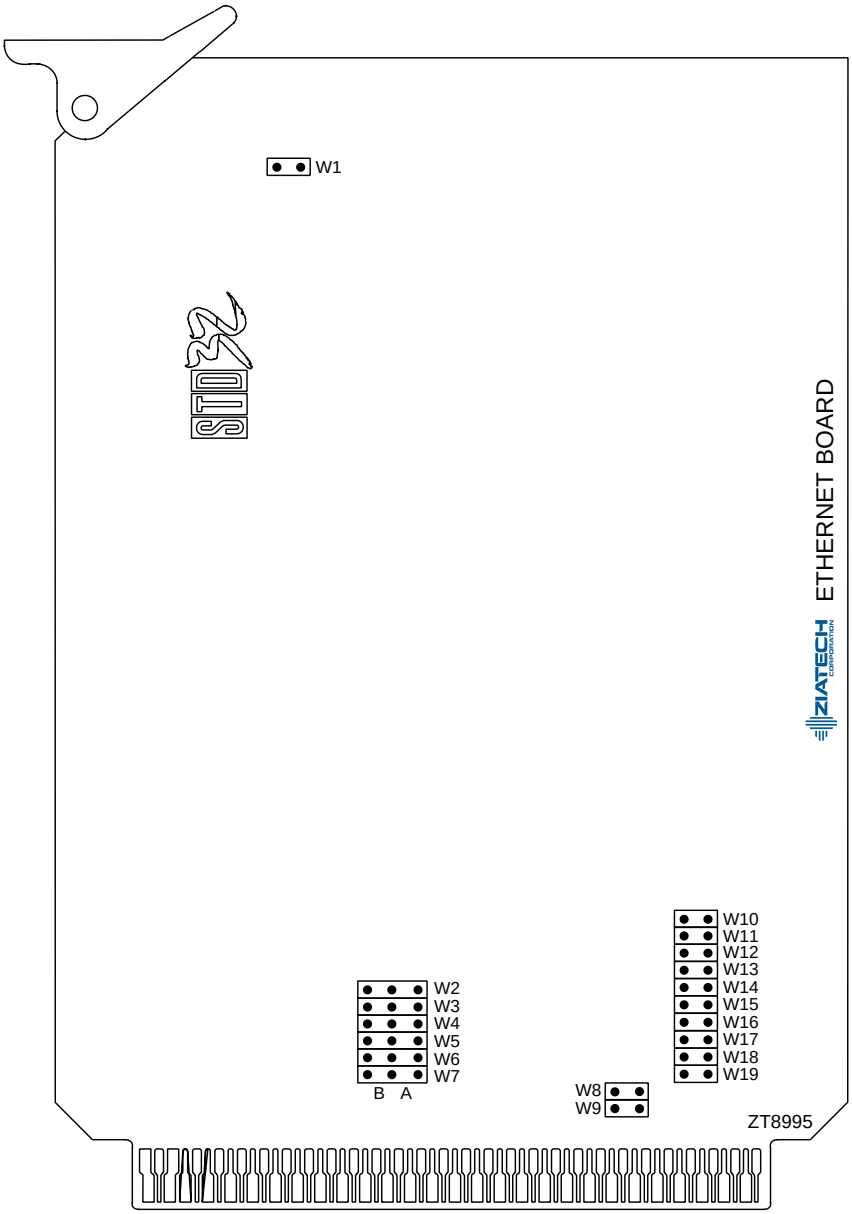
A description of the effects produced by installing or removing each jumper is presented in the "Jumper Descriptions" topic. The "ZT 8995 Jumper Cross Reference" table in that topic lists the jumpers associated with each option.

If your jumper setup differs from the factory default configuration illustrated in the "Factory Default Jumper Configuration" figure, we recommend you document your configuration on the blank jumper layout shown in the "Customer Jumper Configuration" figure. This allows you to quickly restore your custom configuration if the need should arise.



Factory Default Jumper Configuration

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Customer Jumper Configuration

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JUMPER DESCRIPTIONS

The "Jumper Cross Reference" table below lists the jumpers associated with each option. A dagger (†) in a jumper description indicates a factory default configuration.

A description of the effects produced by installing or removing each jumper follows the current topic.

Jumper Cross Reference

Option	Jumper #
24-Bit Address Selection (A20-23)	W4-7
Early ALE* Signal Generation	W15
Shared Memory Block Location	W8,9,15
16-Bit Data Width Selection	W17, W18
ISP PAL Program Enable	W3
Backplane Interrupt Signal Selection	W11,12
Frontplane Interrupt Signal Selection	W13,14
Thin Ethernet Enable	W10
WAITRQ* Enable Selection	W16, W19

W1 (Chassis Ground to Logic Ground)

W1 ties chassis ground to logic ground. This jumper location is not loaded.

Jumper	Function
W1	Ties chassis ground to logic ground

W2 (AT/LANTIC Power-On Configuration)

W2 controls how the AT/LANTIC loads its power-on configuration.

This jumper location is not loaded. The 'A' position is strapped to VCC, forcing the AT/LANTIC chip to load its power-up configuration from the EEPROM.

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W3 (ISP PAL Program Enable)

This jumper is used to three-state the on-board data and address buffers, allowing the PAL at location U15 to be programmed in-circuit. This jumper should be left in the 'B' position for normal operation.

	Jumper	Function
	W3A	In-circuit programming of PAL U15 allowed
†	W3B	In-circuit programming of PAL U15 not allowed

W4-W7 (24-Bit Address Selection)

Jumpers W4-W7 enable the upper four bits of the STD 32 address bus for CPUs that utilize 24-bit addressing (A23-A20). These should remain in the 'A' position for CPU boards that drive all 24 address lines. The 'B' position will tie the upper four address lines to the Ethernet chip to ground.

	Jumpers	Function
†	W4A-W7A In	Enables the upper four STD 32 address lines
	W4A-W7B In	Grounds the upper four Ethernet address lines

† Factory default configuration

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W8,9,15 (Shared Memory Block Location)

These jumpers control the 16K memory address space through which the backplane signal MEM16* is qualified. These jumpers should be used in concert with the configuration softwarewhen the board is programmed for shared memory mode operation. The jumpers should be set as shown below to the same memory space as that selected in the configuration software:

Note: W15 is a dual purpose jumper. See also the description for W15.

	W8	W9	W15	16K Memory Address Base
	In	In	In	0C400h
	In	In	Out	0C000h
	In	Out	In	0CC00h
	In	Out	Out	0C800h
	Out	In	In	0D400h
	Out	In	Out	0D000h
†	Out	Out	In	0DC00h
	Out	Out	Out	0D800h

W10 (Thin Ethernet Enable)

This jumper enables power to the DC/DC unit, enabling Thin Ethernet operation on the ZT 8995-D2. Normal operation leaves this jumper removed to reduce power consumption.

	W10	Function
	In	Enables Thin Ethernet operation
†	Out	Disables Thin Ethernet operation

† Factory default configuration

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W11-W14 (Interrupt Signal Selection)

These jumpers provide additional interrupt control. When a software configuration utility is used to select IR15, the interrupt is routed to these four jumpers. Installing one of the four jumpers determines where IR15 is routed. The factory default leaves these jumpers uninstalled.

Jumper	IR15 Routing
W11	Backplane interrupt NMIRQ*
W12	Backplane interrupt INTRQ3*
W13	Frontplane interrupt FP6 (pin 8 of J1)
W14	Frontplane interrupt FP1 (pin 2 of J1)

W15 (Early ALE* Signal Generation)

W15 controls how ALE is generated for the AT/LANTIC chip. Installing W15 allows an early ALE signal to get addresses on-board to the AT/LANTIC chip. Removing W15 allows normal address generation. Most systems operate equally well with W15 in either position. However, if you experience difficulties or random access problems, install W15. When the board is operated in shared memory mode, see also the jumper description for W8 and W9.

	W15	Function
†	In	Early, on-board ALE generated
	Out	Normal address generation

† Factory default configuration

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W16 (WAITRQ* Enable Selection)

W16 controls how WAITRQ* is generated. Installing W16 allows WAITRQ* to be generated early in the I/O cycle. Removing W16 generates WAITRQ* based only on IOCHRDY from the AT/LANTIC chip. W16 should remain installed.

	W16	Function
†	In	WAITRQ* is generated early in the I/O cycle
	Out	WAITRQ* generated based only on IOCHRDY from the AT/LANTIC chip

W17 (16-Bit Data Width Selection)

W17 controls 8/16-bit operation. Installing the jumper allows 16-bit operation. W17 should only be removed for 8-bit CPU boards. See also jumper W18.

	W17	Function
†	In	Enables 16-bit operation
	Out	Disables 16-bit operation

W18 (16-Bit Data Width Selection)

W18 enables BHE* to the AT/LANTIC chip. W18 should be removed only for 8-bit operation See also jumper W17.

	W18	Function
†	In	Enables BHE* to the AT/LANTIC chip
	Out	Disables BHE* to the AT/LANTIC chip

† Factory default configuration

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W19 (WAITRQ* Enable Selection)

Installing W19 enables the ZT 8995 to drive WAITRQ* onto the backplane. W19 should remain installed.

	W19	Function
†	In	Enables WAITRQ*
	Out	Disables WAITRQ*

† Factory default configuration

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B. NETWORK COMPONENTS AND CABLING

This appendix describes the cabling types and connection methods used for Thin Coax, Thick Coax, and Twisted-Pair Ethernet cabling options. It also includes support for fiber optic cable connection. Use this section in conjunction with Appendix C, "Network Interconnection," which details in table form the allowable interconnection parameters and specifications for these standards. Refer to the "Sample Network Solution Diagram" in Appendix C for a sample network solution diagram.

ETHERNET OPTIONS SUMMARY

The ZT 8995 Ethernet card provides support for several different types of media interfaces to other Ethernet systems. Each type of medium differs in the communication substance or cable used for the transmission and reception of data on the Local Area Network. These media types are:

- Thin coax
- Thick coax
- Twisted-pair
- Fiber optic

They all have different cabling methods and specifications and each has its own advantages.

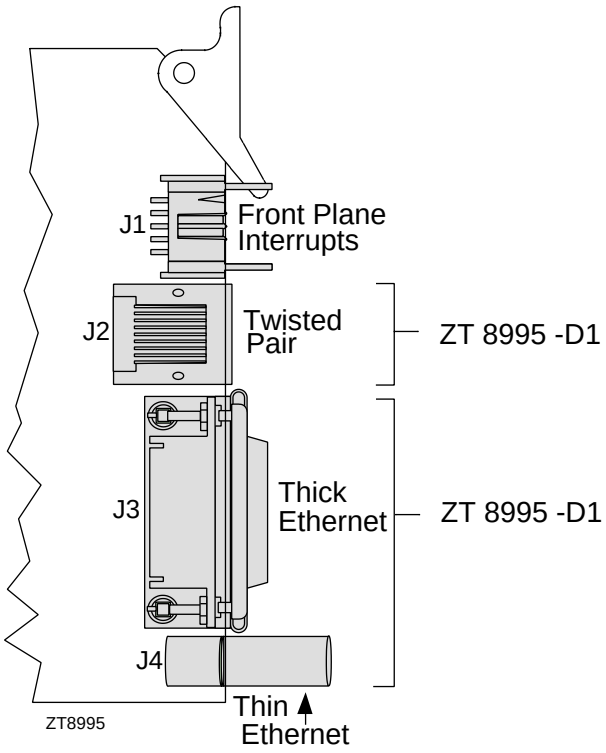
Thin and Thick Ethernet options use a bus topology, while Twisted-Pair Ethernet and fiber optic cabling use a star topology. Due to the increased cabling costs, fiber optic is not generally implemented at the node itself (as are thin, thick and twisted-pair). Instead, fiber optic is commonly supported as a medium for interconnecting segments of the network to avoid noise and cross-talk and to accomplish an overall longer network distance or span.

Call Ziatech's Technical Support for information about where to purchase interconnecting components and products described in this appendix.

Thin Ethernet

Thin Ethernet cabling (10Base2) is the simplest and least expensive approach to Ethernet. It maintains the same data rate as Thick Ethernet but limits distance and number of nodes. Thin Ethernet uses connector J4 on the ZT 8995-D2 frontplane, which is a female BNC type connector. Refer to the figure "Frontplane Connectors". A coaxial transceiver interface on board the ZT 8995-D2 links the driver/receiver with the external thin type coax cable.

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Frontplane Connectors

Thick Ethernet

Thick Ethernet cabling (10Base5) uses an Attachment Unit Interface (AUI) drop cable, also known as a Media Attachment Unit (MAU), to connect the ZT 8995-D2 to an external transceiver. The MAU connects to the Ethernet trunk (or backbone) coaxial cable to provide access to the other Thick Ethernet network components. Thick Ethernet uses the female 15-pin D connector (J3) on the ZT 8995-D2 frontplane for the AUI interface. Refer to the figure "Frontplane Connectors" above.

Twisted-Pair Ethernet

Twisted-Pair Ethernet cabling (10BaseT) uses a star topology, rather than the bus topology used for Thin and Thick Ethernet. A star topology connects all nodes to a central hub (repeater or bridge) rather than tapping the node off the coax bus. Each twisted-pair node receives its signals from the same repeating originator. Therefore, every node has its own data link. The communication rate is equal to that of Thin and Thick Ethernet, which is specified to be 10 Mbps. Twisted-Pair Ethernet allows the use of inexpensive, unshielded, twisted-pair wiring. However, it requires that each node have its own repeater, bridge, or host input.

The ZT 8995-D1 10BaseT connection uses an RJ-45 connector (J2). Refer to the figure "Frontplane Connectors". This connector can be linked directly to the central hub (repeater or bridge) or host using the twisted-pair wiring.

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Fiber-Optic Usage

Fiber optic cable provides immunity to noise, cross-talk, and power surging, and allows for greater cable run lengths. The use of this cable is generally limited to cases in which the distance between two segments is too great for connection to be achieved with media previously described. Fiber optic cable can be used to connect a node to a segment or repeater in a star configuration in a manner similar to that of twisted-pair wiring. Because of its higher cost, however, fiber optic cable is not generally chosen for this purpose unless the application's requirements include noise immunity or connections over large distances.

THIN ETHERNET CABLING

The on-board coaxial transceiver interface (8392) links the driver/receiver to the external coax cable with a female BNC type connector designated J4. Refer to the figure "Frontplane Connectors". The required cable, type RG58 A/U, contains a stranded and tinned copper conductor with 50 ohms of nominal impedance (Belden cable part number 9907 or equivalent).

Note: Coaxial cable type RG58 U is similar in appearance to RG58 A/U but does not comply with the IEEE Thin Ethernet standard.

Each Thin Ethernet cable is actually a point-to-point cable that connects each of the network components together. The cables are fitted with a male BNC connector on both ends.

Contact Ziatech's Technical Support for information regarding where to purchase interconnecting components and products described in this appendix.

ZT 8995-D2 jumper W10 must be installed to operate in a Thin Ethernet configuration.

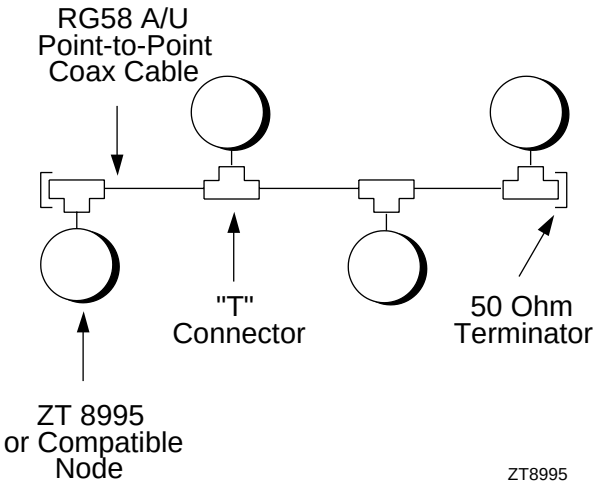
Thin Ethernet "T" Connectors and Terminators

A "T" connector at the ZT 8995-D2 BNC interface provides connection to other Ethernet components or cards on both sides of the T connector. Refer to the following figure, "Thin Ethernet Cable Segment". Each connection between two nodes consists of a point-to-point cable. Therefore, a network segment looks like one length of cable with the network components tapped off the cable.

A 50 ohm (±2%) terminator at each end of the network cabling segment keeps the correct amount of signal reflection on the line during the data communication. The terminators install on the open side of the network component T connectors at the ends of each segment. Proper termination is essential to maintaining a balanced network. The importance of proper termination is underscored in the definition of a network segment: a segment length is defined as the distance from one terminated end of the cable to the other terminated end.

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Each node or component on the network segment connects by a point-to-point cable with a male BNC connector on each end. The male BNC connector on one end of the point-to-point cable screws into one side of the T connector on the ZT 8995-D2. The other male BNC connector screws into the next Ethernet component down the segment line. That component may be another ZT 8995-D2, another compatible Thin Ethernet node, or a repeater.



Thin Ethernet Cable Segment

Standard and Extended Length Segments

The ZT 8995 supports two different types of segment lengths: standard length (SL) segments, which conform to the IEEE specification, and extended length (EL) segments, which are not an IEEE conformity. EL segments can be used only if all of the Ethernet cards and repeaters on the network are capable of operation in the extended length mode. The ZT 8995 can be programmed with AUTOSET8 to use the longer segment length. No jumper changes are required to set the ZT 8995 for SL or EL segment usage. The SL maximum length-per-segment is 185 meters (600 feet), and the EL maximum length-per-segment is 300 meters (1000 feet).

Each SL segment can have a maximum of 30 nodes while EL segments will support up to 100 nodes, less one node for each repeater that may be connected. The minimum distance between nodes is 0.5 meters (20 inches) for either SL or EL segments. See the "Thin Ethernet/Cheapernet" table in Appendix C for additional specifications.

Thin Ethernet Repeaters

A commercially available repeater can connect several network segments together or provide connection to a Thick Ethernet trunk. The repeater retimes and retransmits signals as they pass from one segment of the network to another. Repeaters are available with a single port to connect two segments together, or with multiple ports to

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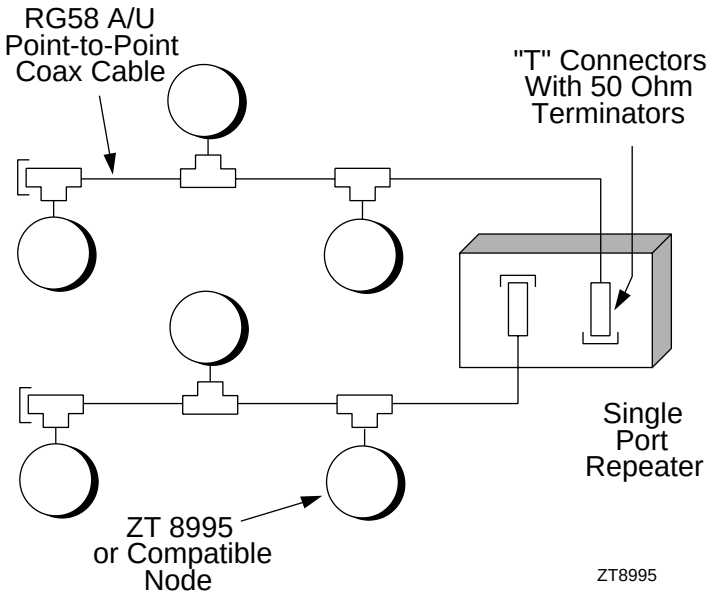
connect several segments together. Even when connecting multiple segments together with repeaters, every segment **must** have a terminator on each end.

Single port repeaters can extend the total length and distance of the entire network span by joining in series a maximum of five SL segments, or three EL segments, with a repeater between each of the segments. That makes a maximum of four repeaters for SL segments, or two repeaters for EL segments. Refer to the following figure, "Repeater to Extend Network Span".

Call Ziatech's Technical Support for information about where to purchase interconnecting components and products described in this appendix.

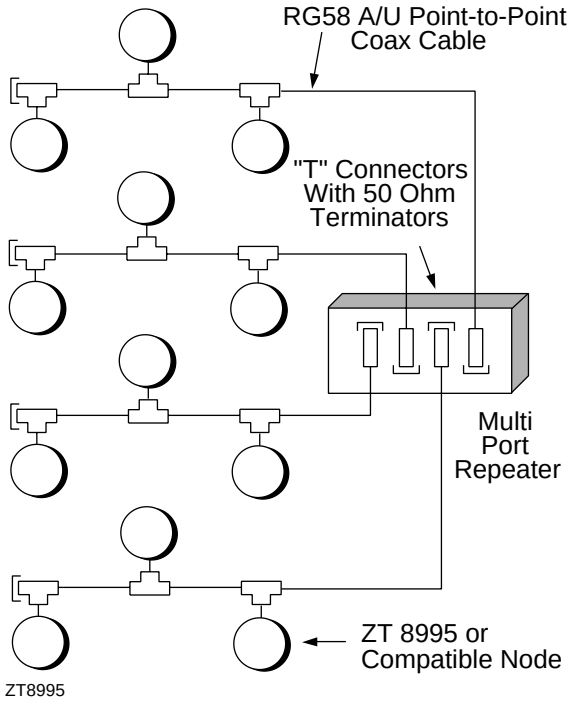
When extending the length of the network span, the five SL segment and three EL segment maximums assume that the maximum length-per-segment is used on each segment. If this is not the case, then the entire network can have more than the maximum of five and three segments respectively, but must not exceed the maximum total network span of 925 meters (3050 feet) for SL segments and 900 meters (2950 feet) for EL segments. The maximum distance between any two nodes on the network can be equal to these maximum network spans.

Multi-port repeaters can expand the number of nodes on the network in a certain locality by increasing the number of segments that have the same signal repeating origination. Refer to the "Repeater to Increase Segment Quantity" figure following. In this configuration, the multi-port repeater does not have to be at the end of each of the segments. Because the repeater is not used to extend the overall network span, the repeater can be inserted anywhere in the segment.



Repeater to Extend Network Span

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Repeater to Increase Segment Quantity

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THICK ETHERNET CABLING

Thick Ethernet communications interface the female 15-pin D connector, designated J3, to an external Attachment Unit Interface (AUI) drop cable. Refer to the figure "Frontplane Connectors". Connector J3 provides a slide latch retention system in accordance with the IEEE 802.3 standard. The other side of the AUI drop cable connects to a Media Attachment Unit (MAU), which is directly tapped off the thick type coaxial cable trunk. Refer to the "Thick Ethernet Cable Segment" figure following. The MAU has a built-in transceiver that links the driver/receiver with the solid conductor thick coaxial trunk cable.

The AUI drop cable is twisted-pair, which typically consists of four individually shielded twisted wire pairs with an overall shield covering these individually shielded pairs. The AUI signal pairs must have a differential characteristic impedance of 78 ohms and can be up to 50 meters (165 feet) in length. The AUI cable must have a male 15-pin D connector on one end, preferably with locking posts (IEEE 802.3 standard), and a female 15-pin D connector on the other end, preferably with a slide latch (also an IEEE 802.3 standard). The male end of the AUI drop cable connects to the female connector (J3) on the ZT 8995-D2. The female end connects to the MAU, which is tapped off the Thick Ethernet cable.

Unlike Thin Ethernet, the Thick Ethernet trunk generally does not use point-to-point cables to connect each of the components on the network segment. Instead, it uses continuous lengths of coaxial cable that have tap-in markings every 2.5 meters (8 feet) to designate the minimum separation between MAU connections. However, some manufacturers can supply a MAU that uses T connectors to splice point-to-point cables.

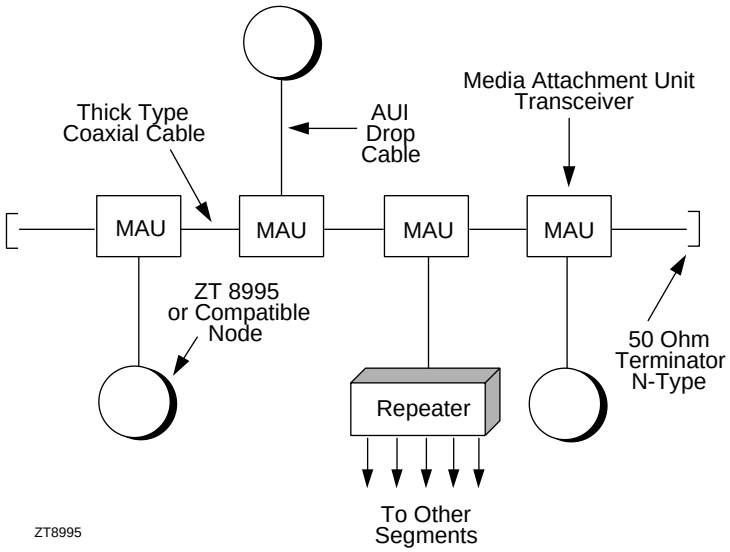
The thick coax is a double-shielded, 0.4 inch diameter cable with a solid and tinned copper conductor, 2.5 meter tap-in markings, 50 ohm nominal impedance, and N-type connectors. Belden cable part number 9901 or equivalent can be used.

Call Ziatech's Technical Support for information regarding where to purchase interconnecting components and products described in this appendix.

Each Thick Ethernet segment can be a maximum of 500 meters (1640 feet) in length, and can support up to 100 nodes, less one for each repeater on the segment.

If the ZT 8995 is used in a Thick Ethernet configuration, jumper W10 must be removed to disable the Thin Ethernet section of the board.

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Thick Ethernet Cable Segment

Thick Ethernet "T" Connectors and Terminators

50 ohm terminators at each end of the Thick Ethernet trunk segment keep the correct amount of signal reflection on line during the data communication.

Call Ziatech's Technical Support for information regarding where to purchase interconnecting components and products described in this appendix.

Proper termination is essential to maintaining a balanced network. The importance of proper termination is underscored in the definition of a network segment: a segment length is defined as the distance from one terminated end of the cable to the other terminated end.

T connectors generally are not used on a Thick Ethernet segment except with certain MAUs that splice into the thick coax with N-type connectors instead of tapping into the cable with non-intrusive taps. The next section describes the MAU.

Thick Ethernet Media Attachment Units

The transceiver MAU is usually a small box with two connectors, one male 15-pin D connector with locking posts (IEEE retention standard) and one coax cable tap connector. The male 15-pin D connects to the female 15-pin D on the AUI drop cable as described in the "Thick Ethernet Cabling" topic. The tap connector typically is either an intrusive tap, which splices with T connectors into point-to-point cables similar to Thin Ethernet, or a non-intrusive tap, which pierces through the insulation and shield of the thick cable trunk to make contact with the solid cable conductor.

Call Ziatech's Technical Support for information regarding where to purchase interconnecting components and products described in this appendix.

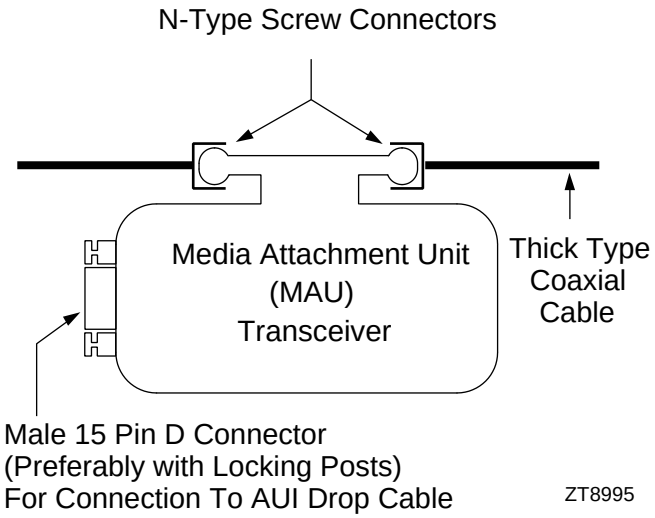
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If an MAU transceiver equipped with a System Quality Error test function is used as a repeater transceiver, you must disable the test. You can, however, enable the test when using the MAU as a transceiver.

Intrusive Tap MAUs

Intrusive cable taps splice into the thick cable trunk by cutting the cable at the desired tap-in marking, located on the cable at 2.5 meter (8 foot) intervals, and installing N-type connectors on both exposed cable ends. Refer to the "Intrusive Tap MAU" figure following. The N connectors then screw into the T connector on the MAU. Intrusive cable taps render the entire segment inoperative during installation due to the necessity of cutting and splicing the cable.

Call Ziatech's Technical Support for information regarding where to purchase interconnecting components and products described in this appendix.

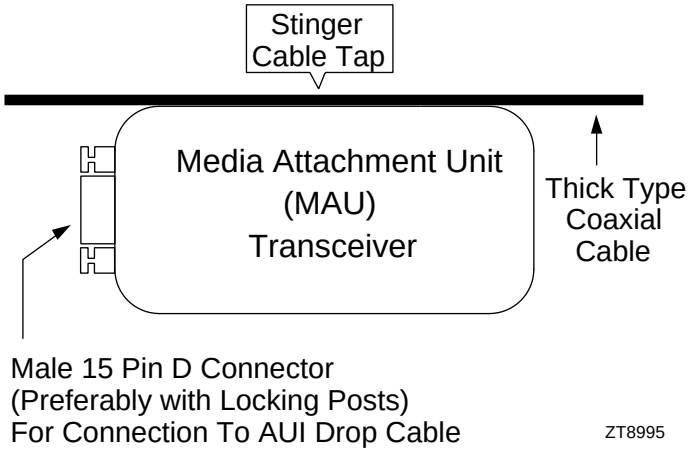


Intrusive Tap MAU

Non-Intrusive Tap MAUs

Non-intrusive cable taps, also known as "vampire" or "stinger" taps, provide easy connection to the thick cable trunk. They make the MAU relocatable without cutting and splicing cables. Refer to the "Non-Intrusive Tap MAU" figure following. They also allow the network segment to remain operative during installation since the thick cable trunk is not cut. Several different types of non-intrusive taps are available. One type installs by piercing a hole in the cable at the desired tap-in marking with a special tool, inserting the tap in the cable, and then attaching the MAU to the tap.

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Non-Intrusive Tap MAU

Thick Ethernet Repeaters

Repeaters in Thick Ethernet segments operate in much the same way as those used in Thin Ethernet segments. However, the use of a repeater connected to a thick cable trunk requires an AUI drop cable and MAU transceiver.

Thick Ethernet supports maximum segment lengths of 500 meters (1640 feet). Signal repeaters can interconnect a maximum of five full length segments to extend the total length and distance of the entire network. The five segment maximum assumes that the maximum length-per-segment is used on each segment. If it is not, then the entire network can have more than the maximum of five segments, but must not exceed the maximum total network span of 2500 meters (8200 feet).

If an MAU transceiver equipped with a System Quality Error test function is used as a repeater transceiver, you must disable the test (a transceiver is used when connecting a repeater to a Thick Ethernet cable trunk). You can, however, enable the test when using the MAU as a ZT 8995-D2 transceiver.

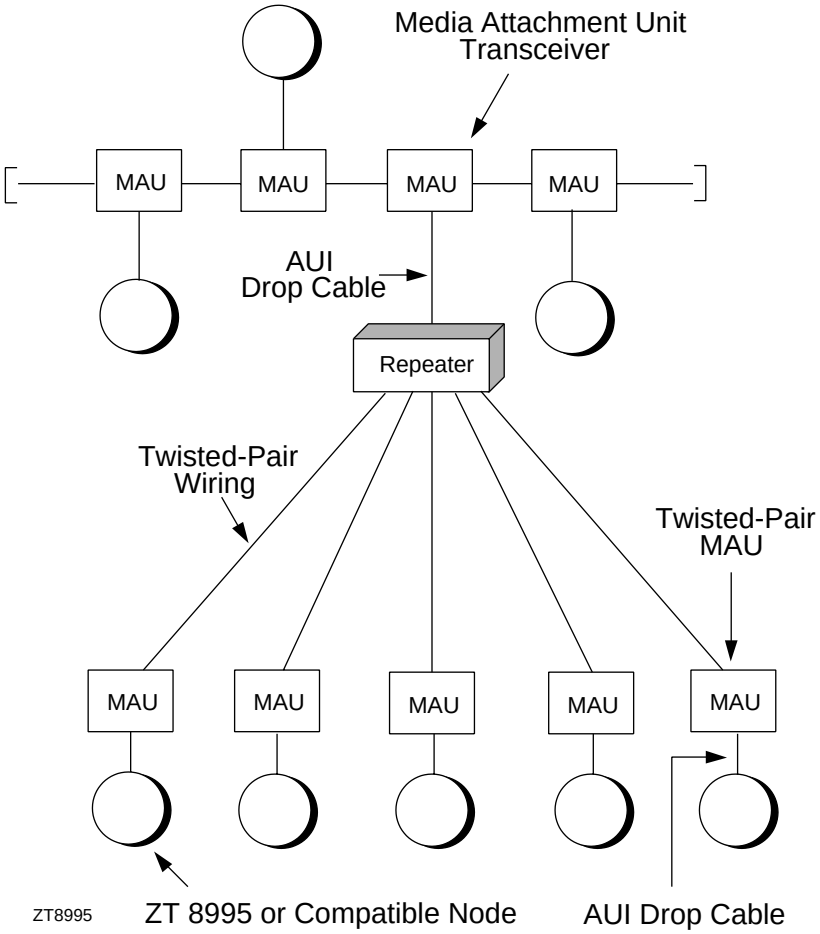
TWISTED-PAIR ETHERNET CABLING

Each Twisted-Pair Ethernet node has its own interface to a central hub. This interface can be a repeater, bridge, or host interface module. Refer to the "Twisted Pair Ethernet Connection" figure. The presence of a unique interface for each node on a central hub constitutes a "star" topology, in contrast to the "bus" topology that has been previously described. Star segments connect to either Thin or Thick Ethernet segments by means of a twisted-pair repeater or bridge. Twisted-Pair Ethernet supports a maximum twisted-pair wiring length of 100 meters (325 feet) per node. A star segment actually consists of a maximum of one node per segment. A node includes the transceiver, whether it is off board or on board. See the "Twisted-Pair Ethernet" table in Appendix C for additional specifications.

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A ZT 8995-D1 uses an RJ-45 connector at location J2 for the interface to twisted-pair media. Twisted-pair provides unique connection to the central hub with inexpensive unshielded or shielded telephone (twisted-pair) wiring. This is the primary advantage to this type of network segment. It is relatively easy to install Twisted-Pair Ethernet nodes in many buildings that already have this twisted-pair telephone wiring.

No jumper changes are required to operate the ZT 8995-D1 in a twisted-pair configuration.



Twisted-Pair Ethernet Connection

Twisted Pair Ethernet Repeaters

Twisted-Pair Ethernet must use multi-port repeaters since a star configuration or segment is the only method supported. Signal repeaters can be used to connect star twisted-pair segments (one node per segment) to either Thin or Thick Ethernet segments. Refer to the "Twisted Pair Ethernet Connection" figure above.

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A maximum length of 100 meters (325 feet) of twisted-pair wiring can run from connector J2 on the ZT 8995-D1 or the twisted-pair media adapter (AUI drop cable) to the repeater.

FIBER OPTIC CABLING

The advantage of fiber optic cable over copper conductor cable is that network users can completely avoid problems such as crosstalk, noise, and power surging. In addition, fiber optic cable can provide much longer cable runs than any of the other media described in this appendix.

There are basically two different ways to use fiber optic cable. The first method is to connect a **segment** to another segment or host interface module that has a separation distance greater than that achievable with copper conductor cable, or when noise immunity is a factor. The second method is to connect a **node** to a segment, repeater, or host interface module that has a similar distance or noise consideration. Refer to the "Fiber Optic Connection" figure. The IEEE standard allows for a maximum run length of 1000 meters (3280 feet) of fiber optic cabling between repeaters or nodes. Some transceivers, repeaters, and host interface modules may support longer cable runs.

Fiber optic cabling uses the Thick Ethernet connector J3 on the ZT 8995. Jumper W10 must be removed to disable the Thin Ethernet section of the ZT 8995.

Implement repeaters and Media Attachment Units (MAUs) in the fiber optic interface when using fiber optic to connect two segments or to connect a node to a segment.

Call Ziatech's Technical Support for information regarding where to purchase interconnecting components and products described in this appendix. The following sections describe these devices.

Fiber Optic Media Attachment Units

Each node or repeater requires a fiber optic transceiver to link the ZT 8995-D2 driver/receiver with the external fiber optic cable. Refer to the "Fiber Optic Connection" figure. The fiber optic Media Attachment Unit (MAU) transceiver's appearance is similar to the Thick Ethernet MAU transceiver except that a fiber optic connector is provided in place of the coax cable tap.

The ZT 8995-D2 connects to the fiber optic MAU through an AUI drop cable as described in the "Thick Ethernet Cabling" topic.

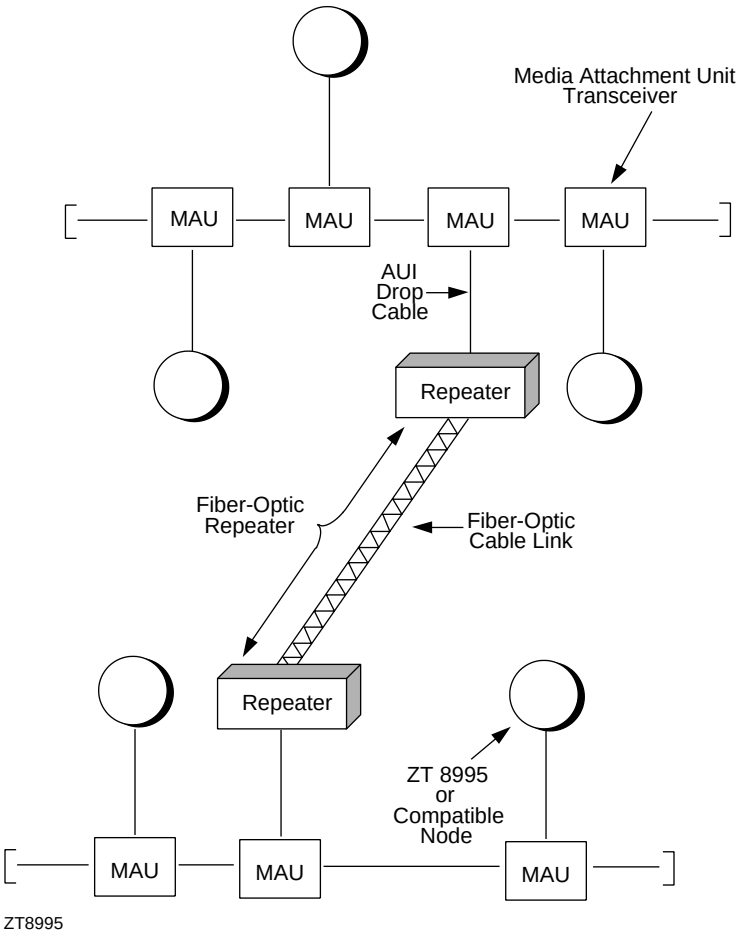
If an MAU transceiver equipped with a System Quality Error test function is used as a repeater transceiver, you must disable the test. You can, however, enable the test when using the MAU as a ZT 8995-D2 transceiver.

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Fiber Optic Repeaters

To join two network segments together, each segment connects to a fiber optic MAU and a single port fiber optic repeater. Refer to the "Fiber Optic Connection" figure following. Each repeater then uses fiber optic cable to interface the two segments. This allows for a greater distance between segments, as well as providing immunity to crosstalk, noise, and power surging.

If you wish to connect a single node to a segment using fiber optic cable, then use a similar configuration except don't use a repeater at the node end of the cable. A fiber optic MAU transceiver is still required, however.



Fiber Optic Connection

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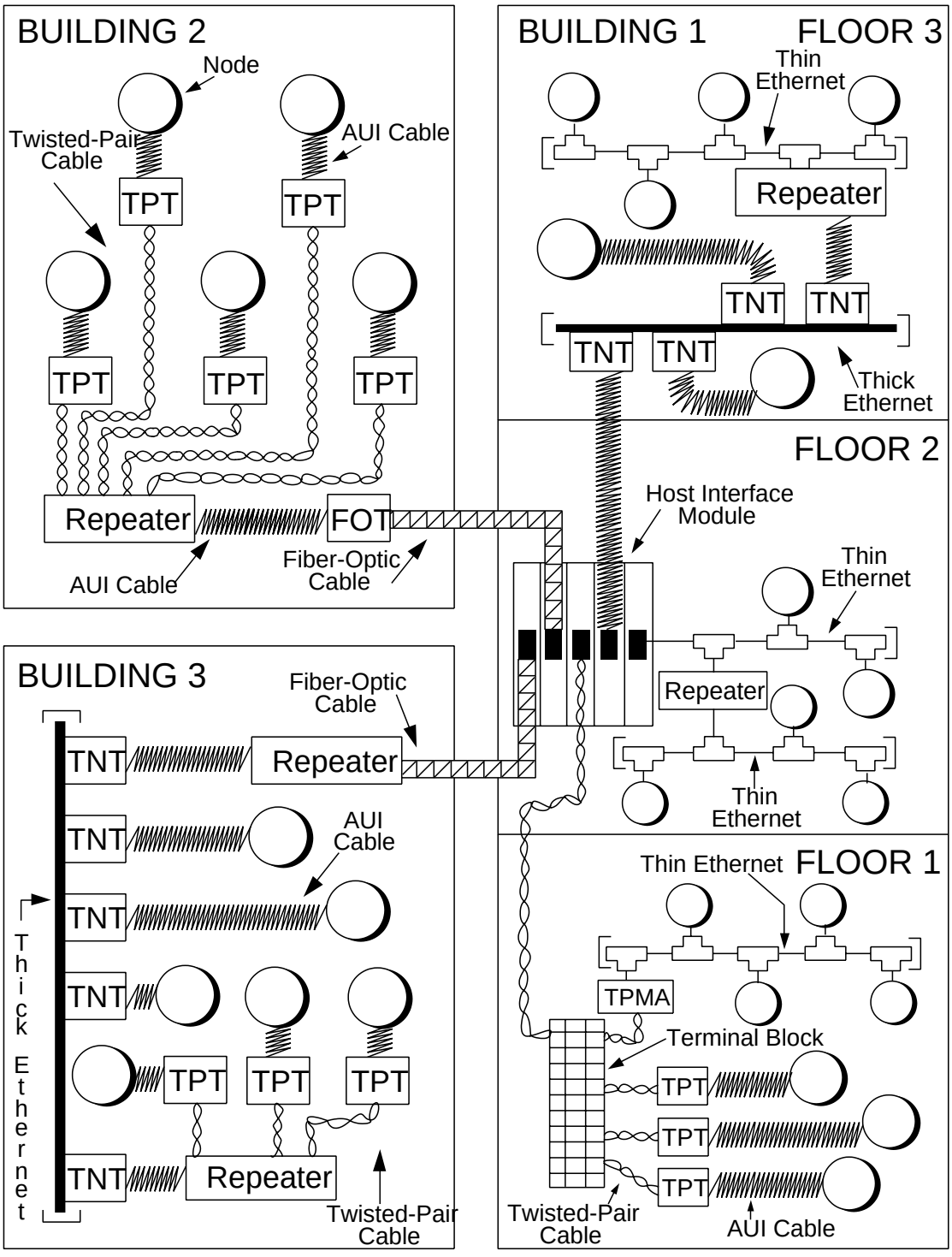
C. NETWORK INTERCONNECTION

This appendix is made up of tables demonstrating the allowable IEEE networking interconnection specifications described in Appendix B. It compares the different forms of media that can be used in the network cabling structure. These media types are thin coax, thick coax, twisted-pair wiring, and fiber optic cable.

Refer to the following figure "Sample Network Solution Diagram" for a diagram of a complete network solution that connects together three buildings, including one with three floors. It is impractical to show all of the possible interconnecting schemes in one figure because so many networking devices are available. The purpose of the figure is to illustrate that there are many different interconnection possibilities available.

There can be large cost differences between interconnection solutions using the different media. Special installation tools may also be required for implementing the chosen method. Time and care should be taken to choose the right medium for your application.

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TNT=Thick Net Transceiver
TPMA=Twisted Pair Media Adapter

ZT8995

TPT = Twisted Pair Transceiver
FOT = Fiber Optic Transceiver

Sample Network Solution Diagram

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NETWORK CHARACTERISTICS

The following tables show the IEEE standards for each of the ZT 8995-compatible network types:

- General Network Characteristics
- Thin Ethernet/Cheapernet
- Thick Ethernet
- Attachment Unit Interface Cable
- Twisted-Pair Ethernet
- Fiber Optic

General Network Characteristics

Data rate	10 Mbps
Maximum number of nodes per network	1024
Communication method	CSMA/CD

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Thin Ethernet/Cheapernet

This table gives the specifications for the non-IEEE standard, Extended Length (EL) segments. Refer to "Standard and Extended Length Segments" in Appendix B for a discussion of Standard Length (SL) and Extended Length (EL) segments. To operate in Extended Length mode, each node on the network must be capable of Extended Length operation.

Characteristic	**Standard Length**†	**Extended Length**‡
Topology	Bus	Bus
Maximum segment length	185 meters (600 feet)	300 meters (1000 feet)
Maximum number of repeaters between any two nodes	4	2
Network span	925 meters (3050 feet)	900 meters (2950 feet)
Maximum nodes per segment	30	100
Minimum spacing between nodes	0.5 meters (20 inches)	0.5 meters (20 inches)
Cable type	RG58 A/U, 50 ohm	RG58 A/U, 50 ohm
Cable connectors	BNC	BNC
Termination	50 ohm	50 ohm

† Defined by IEEE 802.3-10BASE2 standard

‡ Not an IEEE standard

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Thick Ethernet

Characteristic	**Thick Ethernet**†
Topology	Bus
Maximum segment length	500 meters (1640 feet)
Maximum number of repeaters between any two nodes	2
Network span	2500 meters (8200 feet)
Maximum nodes per segment	100
Minimum spacing between nodes	2.5 meters (8 feet) at tap-in markings
Cable type	.4" dia., Solid, 50 ohm, double shield
Cable connectors	N-type
Termination	50 ohm

Attachment Unit Interface Cable

Maximum cable length	50 meters (165 feet)
Cable type	.39" dia., 4 twisted-pairs, shielded
Cable connectors	1 male 15 pin D, 1 female 15 pin D

† Defined by IEEE 802.3-10BASE5 standard

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Twisted-Pair Ethernet

Characteristic	**Twisted-Pair Ethernet**[†]
Topology	Star
Maximum segment length	100 meters (325 feet)
Maximum nodes per segment	1
Cable type	Unshielded twisted-pair
Cable connectors	RJ-45

Fiber Optic

Characteristic	**Fiber Optic**
Topology	Star
Maximum run or segment length	1000 meters (3280 feet)
Maximum nodes per segment	1
Cable type	Duplex fiber optic
Cable connectors	ST or SMA pair

[†] 10BASET

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D. SPECIFICATIONS

This appendix describes the electrical, environmental, and mechanical specifications of the ZT 8995. It also includes illustrations of the board dimensions, connector locations, and the P/E connector pinouts, as well as tables showing the pin assignments for the ZT 8904's five connectors.

ELECTRICAL AND ENVIRONMENTAL SPECIFICATIONS

The following topics list electrical and environmental specifications, including absolute maximum ratings, DC operating characteristics, and STD bus loading characteristics.

Absolute Maximum Ratings

Supply Voltage, VCC:	0 to 7 Volts
Supply Voltage, AUX +V:	0 to 15 Volts
Storage Temperature:	-65º through +150º Celsius
Operating Temperature:	0º through +70º Celsius
Non-Condensing Relative Humidity:	< 95% @ 40º Celsius

DC Operating Characteristics

Twisted-Pair Ethernet (10BaseT) Operation:	+5 VDC ± 5% @ 0.140 A typ., 0.350 A max
Thin Ethernet (10Base2) Operation:	+5 VDC ± 5% @ 0.495 A typ., 0.705 A max
Thick Ethernet (10Base5) Operation:	+5 VDC ±5% @ 0.12 A typ., 0.33 A max +12 VDC ±5% @ 0.17 A typ., 0.22 A max

STD Load Characteristics

The unit load is a convenient method for specifying input and output drive capability of STD bus cards. In STD bus systems, one unit load is equal to one LSTTL load as follows:

- Maximum high level input current: 20 µA.
- Maximum low level input current: -400 µA.

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The STD bus unit load reflects input current requirements at worst case conditions over recommended supply voltage and ambient temperature ranges. An output rated at 60 unit loads can drive 60 STD bus cards having input rated at one unit load.

The "STD Bus Loading, P Connector" table includes load values for STD-80 connections. The "STD Bus Loading, E Connector" table includes load values for STD 32 connections.

Note: The ZT 8995 uses CMOS devices which have high and low input currents of ±10 µA.

STD Bus Loading, P Connector

PIN (CIRCUIT SIDE) / OUTPUT DRIVE / INPUT LOAD / MNEMONIC							PIN (COMPONENT SIDE) / OUTPUT DRIVE / INPUT LOAD / MNEMONIC
+5 VDC			P2	P1			+5 VDC
GND			P4	P3			GND
DCPDN*			P6	P5			VBAT (INTRQ4)
D7/A13 [1]	1	60	P8	P7	60	1	D3/A19 [1]
D6/A22 [1]	1	60	P10	P9	60	1	D2/A18 [1]
D5/A21 [1]	1	60	P12	P11	60	1	D1/A17 [1]
D4/A20 [1]	1	60	P14	P13	60	1	D0/A16 [1]
A15	1		P16	P15		1	A7
A14	1		P18	P17		1	A6
A13	1		P20	P19		1	A5
A12	1		P22	P21		1	A4
A11	1		P24	P23		1	A3
A10	1		P26	P25		1	A2
A9	1		P28	P27		1	A1
A8	1		P30	P29		1	A0
RD*	1		P32	P31		1	WR*
MEMRQ*	1		P34	P33		1	IORQ*
BHE	1		P36	P35			IOEXP
ALE*	1		P38	P37	60		INTRQ1*
STATUS 0*			P40	P39			STATUS 1*
BUSRQ*			P42	P41			BUSAK*
INTRQ*		60	P44	P43		1	INTAK*
NMIRQ*		60	P46	P45	60		WAITRQ*
PBRESET*			P48	P47		1	SYSRESET* [2]
INTRQ2* (CNTRL*)		60	P50	P49		1	CLOCK* [2]
PCI [3]			P52	P51			PCO [3]
AUX GND			P54	P53			AUX GND
AUX-V			P56	P55			AUX+V

ZT8995

Notes:
REQ indicates required connection.
[1] High order address bits multiplied over the data bus.
[2] SYSRESET* and CLOCK* are outputs in permanent master configuration and inputs in temporary master configuration.
[3] PCI is connected to PCO.

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STD Bus Loading, E Connector

PIN (CIRCUIT SIDE) / OUTPUT DRIVE / INPUT LOAD / MNEMONIC							PIN (COMPONENT SIDE) / OUTPUT DRIVE / INPUT LOAD / MNEMONIC
LOCK*			E2	E1			GND
XA23			E4	E3			XA19
XA22			E6	E5			XA18
XA21			E8	E7			XA17
XA20			E10	E9			XA16
RSVD			E12	E11			NOWS*
+5 VDC			E14	E13			+5 VDC
DREQx*			E16	E15			DAKx*
GND			E18	E17			GND
D31			E20	E19			D27
D30			E22	E21			D26
D29			E24	E23			D25
D28			E26	E25			D24
GND			E28	E27			D23
D15	1	60	E30	E29			D22
D14	1	60	E32	E31			D21
D13	1	60	E34	E33			D20
D12	1	60	E36	E35			GND
D11	1	60	E38	E37			D19
D10	1	60	E40	E39			D18
D9	1	60	E42	E41			D17
D8	1	60	E44	E43			D16
MASTER16*			E46	E45			GND
AENx*			E48	E47	60		IRQx
BE3*			E50	E49			BE1*
BE2*			E52	E51			BE0*
GND			E54	E53	60		MEM16*
W-R			E56	E55			M-IO
DMAIOR*			E58	E57			DMAIOW*
EX8*			E60	E59	60		IO16*
START*			E62	E61			CMD*
EX32*			E64	E63			EX16*
T-C			E66	E65			EXRDY
+5 VDC			E68	E67			INTRQ3*
MREQx*			E70	E69			MAKx*
MSBURST*			E72	E71			SLBURST*
XA31*			E74	E73			XA27*
XA30*			E76	E75			XA26*
XA29*			E78	E77			XA25*
XA28*			E80	E79			XA24*

ZT8995TD-02

STD-80 Compatibility

The ZT 8995 is designed for use in an STD 32 backplane environment. While designed to be backward compatible with STD-80 systems, the ZT 8995 is not guaranteed to work in all system topologies.

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MECHANICAL SPECIFICATIONS

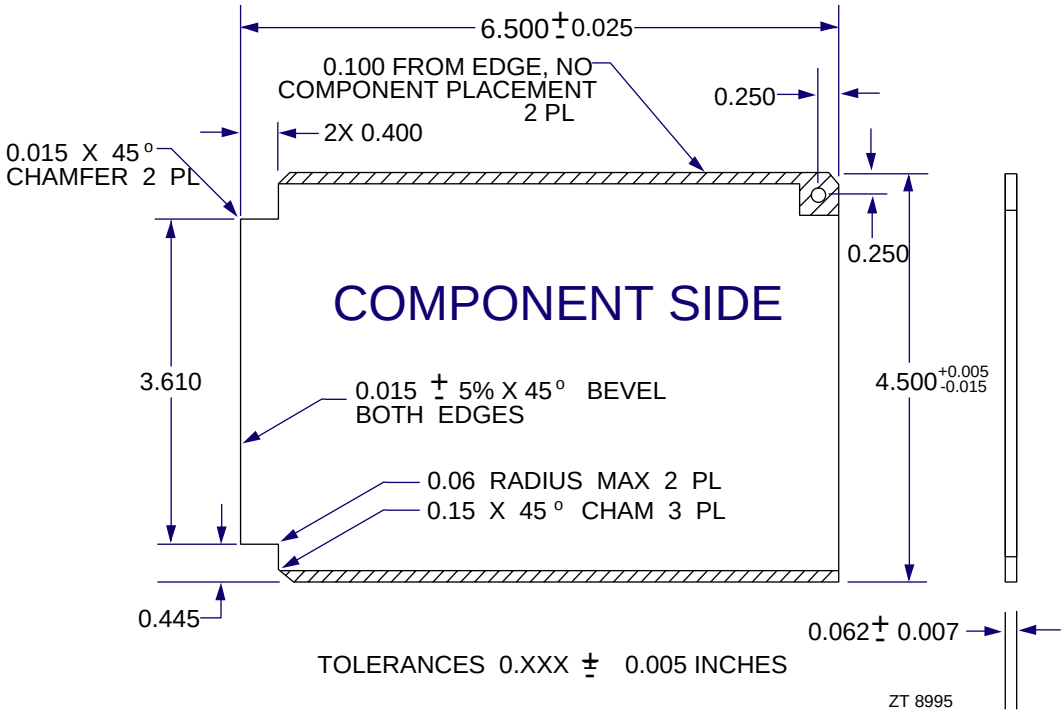
The following topics list mechanical specifications, including card dimensions, card weight, and ZT 8995 connectors.

Card Dimensions and Weight

Width: 113.8 mm (4.5 inches)

Height: 165.1 mm (6.5 inches)

Weight: 4.0 oz. (-D1). 5.1 oz. (-D2)



Board Dimensions

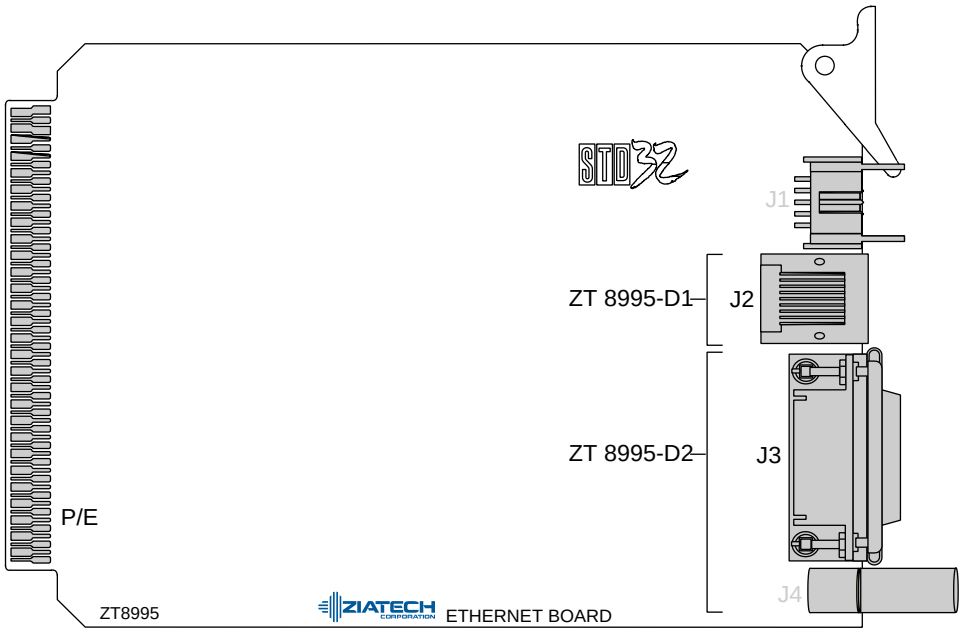
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Connectors

The ZT 8995 has the following connectors:

- One STD 32 card edge connector (P/E)
- One BNC network interface connector (-D2 option)
- One DB-15 network interface connector (-D2 option)
- One RJ-45 network connector for interrupts (-D1 option)
- One header connector for interrupts

The connectors are described below.



Connector Locations

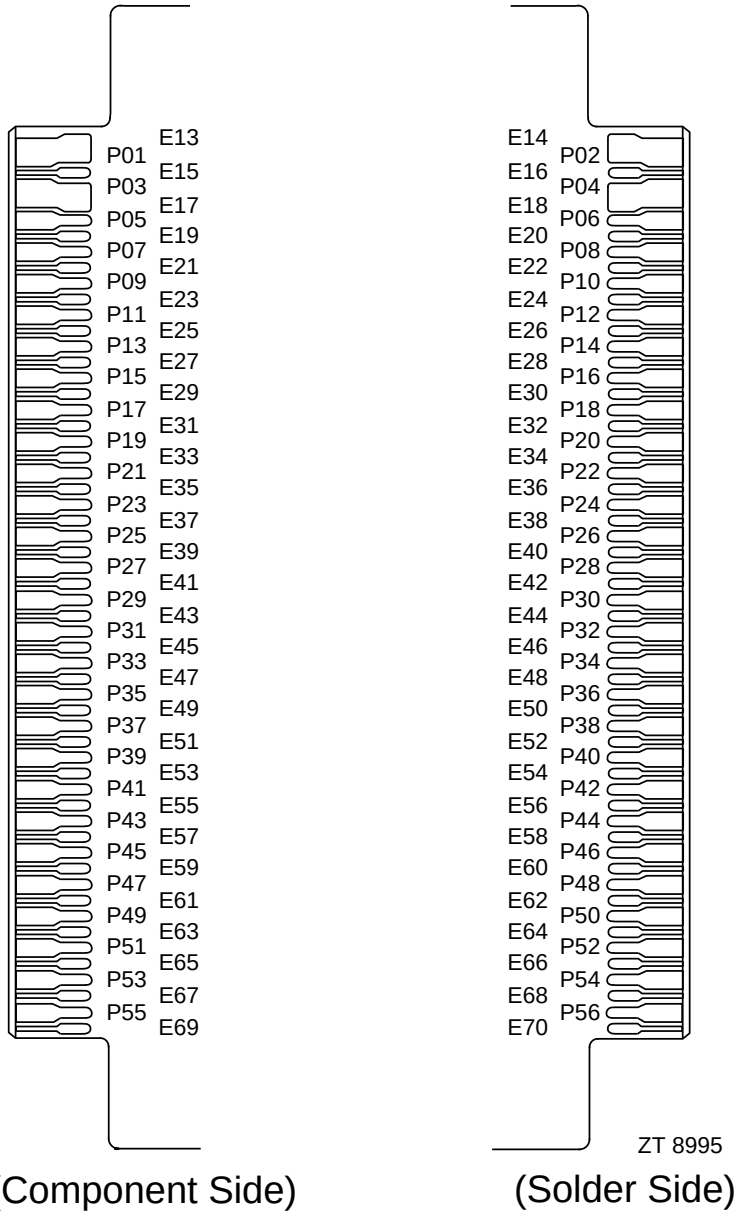
STD 32 P/E Connector

P: The P connector is the interface between the ZT 8995 and the STD-80 bus. This connector is a 56-pin (dual 28-pin) card-edge connector with fingers on 0.125 inch contact spacing. The mating connector is a Viking 3VH28/1CNK5 or equivalent for the solder tail, or a Viking 3VH28/1CND5 or equivalent for a three-level wire wrap. The "P/E Connector Pinout" figure following shows pin assignments for the P connector and the "STD Bus Loading, P Connector" table shows signal assignments.

E: The E connector extends the P connector to interface the ZT 8904 to the STD 32 bus. This connector combines with the P connector to make a 114-pin (dual 57-

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pin) card-edge connector with fingers on 0.0625 inch contact spacing. The mating connector is a Viking S3VT68/5DP12 or equivalent for the solder tail, or a Viking S3VT68/5DE12 or equivalent for the card extender. The "P/E Connector Pinout" figure shows pin assignments for the E connector and the table "STD Bus Loading, E Connector" shows signal assignments.



P/E Connector Pinout

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J1 (Frontplane Interrupts)

Connector J1 is a male 10-pin right angle header connector with a retention latch. This connector provides frontplane access to interrupt signals.

The mating connector is a female 10-pin ribbon cable connector. If a 10-pin connector for interrupts is used, or any connector with less than 10 pins, and it has a polarization key, the keyed notch must be cut from the connector in order to fit into connector J1. The 10-pin part number is 622-1030 from TB Ansley or equivalent. The pin assignment are given in the "J1 Frontplane Interrupts Pinout" table below.

J1 Frontplane Interrupts Pinout

Pin #	Signal Name	Signal Level
2	FP1* Interrupt Output	IR15†
4	FP3* Interrupt Output	IR10
6	FP5* Interrupt Output	IR11
8	FP6* Interrupt Output	IR15†
10	FP7* Interrupt Output	IR12
1-9 Odd	Ground	--

† Depends upon jumper W13 and jumper W14 configuration.

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J2 (Twisted-Pair)

Connector J2 is a female 8-pin right angle header RJ-45 connector. This connector provides access to a network using twisted-pair wiring.

The part number for connector J2 is 555164-1 from AMP or equivalent. The pin assignment are given in the "J2 Twisted-Pair Pinout" table below. The mating connector is a female 8-pin plug and can be purchased from Amp part number 5-641338-2 or Molex part number 90075-0132 or equivalent

J2 Twisted-Pair Pinout

Pin #	Signal Name
1	Transmit + (Tx +)
2	Transmit - (Tx -)
3	Receive + (RX +)
4	No Connection
5	No Connection
6	Receive - (RX -)
7	No Connection
8	No Connection

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J3 (Thick Ethernet)

Connector J3 is a female right angle DB-15 connector with a slide latch for cable retention. The part number is 747845-4 from AMP, Inc.

The mating connector is a male DB-15 connector, preferably with locking posts for retention. This part can also be purchased through AMP, Inc. The pin assignment are given in the below "J3 Thick Ethernet Pinout" table below for IEEE 802.3 operation.

J3 Thick Ethernet Pinout

Pin #	Signal Name
1	Ground
2	Collision Detect + (CD+)
3	Transmit + (Tx +)
4	Ground
5	Receive + (RX +)
6	Ground
7	No Connection
8	Ground
9	Collision Detect - (CD -)
10	Transmit - (TX -)
11	Ground
12	Receive - (RX -)
13	+12 Volts
14	Ground
15	No Connection

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J4 (Thin Ethernet)

Connector J4 is a female right angle miniature coaxial BNC type connector that has an impedance of 50 ohm.

The mating connector is typically a male BNC "T" connector, part number 252640 from AVA Electronics or equivalent.

Note: J4 could make contact with an electrically conductive retaining bar used on some card cages to lock the cards in place. This retaining bar may be tied to logic ground, while J4 is meant to be isolated from logic ground (the shield of J4 is tied to chassis or earth ground). Any unwanted contact can be eliminated in one of the following ways:

1. Remove the bar altogether.

2. Insert some form of insulating material between the retaining bar and the BNC connector.

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E. CUSTOMER SUPPORT

This appendix offers technical and sales assistance information for this product, warranty information, and necessary information for the return of a Ziatech product.

TECHNICAL/SALES ASSISTANCE

If you have a technical question, please call Ziatech's Customer Support Service at the number below, or e-mail our technical support team at tech_support@ziatech.com. Ziatech also maintains an FTP site located at ftp://ziatech.com/Tech_support.

If you have a sales question, please contact your local Ziatech Sales Representative or the Regional Sales Office for your area. Address, telephone and FAX numbers, and additional information are available at Ziatech's website, located at http://www.ziatech.com.

Corporate Headquarters

1050 Southwood Drive

San Luis Obispo, CA 93401 USA

Tel (805) 541-0488

FAX (805) 541-5088

RELIABILITY

Ziatech takes extra care in the design of the product in order to ensure reliability. The product was designed in top-down fashion, using the latest in hardware and software design techniques, so that unwanted side effects and unclean interactions between parts of the system are eliminated. Each product has an identification number. Ziatech maintains a lifetime data base on each board and the components used. Any negative trends in reliability are spotted and Ziatech's suppliers are informed and/or changed.

RETURNING FOR SERVICE

Before returning any of Ziatech's products, you must phone Ziatech at (805) 541-0488 and obtain a Return Material Authorization (RMA) number. Please supply the following information to Ziatech in order to receive an RMA number:

- Your company name and address for invoice
- Your shipping address and phone number
- The product I.D. number
- The name of a technically qualified individual at your company familiar with the mode of failure

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Once you have an RMA number, follow these steps to return your product to Ziatech:

1. Contact Ziatech for pricing if the warranty has expired.
2. Supply a purchase order number for invoicing the repair if the warranty has expired.
3. Pack the board in **anti-static** material and ship in a sturdy cardboard box with enough packing material to adequately cushion it.

Note: Any product returned to Ziatech improperly packed will immediately void the warranty for that particular product!

4. Mark the RMA number clearly on the outside of the box.

ZIATECH WARRANTY

Warranty information for Ziatech products is available at Ziatech's website, located at http://www.ziatech.com.

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