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ZT 89CT39

STD 32 Slot X Arbiter

H A R D W A R E M A N U A L

For ZT 89CT39 Revision D.1
ZT 89CT39X Revision D.2



ZT M89CT39
January 12, 1998
10244300

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WHAT'S IN THIS MANUAL

This manual describes the operation and use of the ZT 89CT39 and ZT 89CT39X STD 32 Slot X Arbiters. All references to the ZT 89CT39 also apply to the ZT 89CT39X except where otherwise specified.

The following outline summarizes the focus of each chapter in this manual.

Chapter 1, "Introduction," is an overview of the ZT 89CT39. It includes a product definition, a listing of product features, answers to commonly asked questions, a functional block diagram, and a description of each block.

Chapter 2, "Getting Started," summarizes the information you need to get your ZT 89CT39 operational. This includes system requirements and a description of the jumper options. Depending upon how you wish to utilize the ZT 89CT39, this information may be all you need to begin using the ZT 89CT39.

Chapter 3, "STD Bus Interface," describes the ZT 89CT39 interface to the STD 32 bus structure in detail. Topics include fixed and rotating priority, bus monopolization, watchdog timer, DMA connector, and status LEDs.

Appendix A, "Specifications," gives the electrical, mechanical, and environmental specifications for the ZT 89CT39, as well as STD 32 and frontplane connector pin assignments.

Appendix B, "Customer Support," offers a product revision history, technical support information, and instructions for returning the ZT 89CT39 if service becomes necessary.

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CHAPTER 1. INTRODUCTION

This chapter provides a brief introduction to the ZT 89CT39 and ZT 89CT39X. It includes a product definition, a listing of product features, a functional block diagram, and a description of each functional block. Unpacking information and installation instructions are in Chapter 2, "Getting Started." All references in this manual to the ZT 89CT39 also apply to the ZT 89CT39X except where otherwise specified.

PRODUCT DEFINITION

Many STD bus applications have grown to be so complex that a single microprocessor is not enough to complete the necessary operations in the required amount of time. One solution is to distribute the operations among multiple microprocessors, each capable of managing STD bus memory and I/O resources. These microprocessor boards are referred to as bus masters.

Multiple bus masters have not been supported by an STD bus specification in the past. However, multiple bus masters are allowed with the *STD 32 Bus Specification*. Bus masters are defined as either temporary or permanent and are identical in operation except the permanent master usually drives CLOCK* and SYSRESET*. The ZT 89CT39X version of the ZT 89CT39 can be configured to drive CLOCK* and SYSRESET* as a master clock and a master reset.

With multiple bus masters sharing STD bus resources, arbitration is needed to ensure that only one bus master is temporarily granted access to the shared resources at a time. The ZT 89CT39 provides arbitration for multiple bus masters (both temporary and permanent) in a single STD 32 backplane. When the ZT 89CT39 is installed into the left-most slot (Slot X), up to seven bus masters then have fixed or rotating priority access to STD bus memory and I/O resources. The ZT 89CT39 also has an optional watchdog feature that prevents any one bus master from monopolizing STD bus resources.

FEATURES OF THE ZT 89CT39

- STD 32 compatible for Slot X operation
- Manages up to seven STD 32 bus masters
- Status LEDs indicate active bus master
- Watchdog timer prevents bus monopolization
- CMOS for low power and extended temperature range
- Five-Year warranty
- Burned in at 55° Celsius and tested to guarantee reliability
- STD 32 compliance:

  Arbiter (M7,D7): EA32, EA16, EA8, SA16, SA8-MX, MD, IXP, IXL

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COMMONLY ASKED QUESTIONS

1. **Does the ZT 89CT39 work in an STD-80 backplane?** No. STD-80 architecture does not define the signals needed to implement a multiple bus master architecture. STD 32 architecture defines Master Request and Master Acknowledge signals for multiple bus master implementations. These signals are routed to a special slot reserved for a bus arbiter, such as the ZT 89CT39.
2. **Why does the ZT 89CT39 operate only in the left-most slot of an STD 32 backplane?** An STD 32 architecture defines several slot-specific signals, including the Master Request and Master Acknowledge signals needed for multiple bus master implementation. These slot-specific signals are routed from up to 15 unique slots to the left-most slot, also known as Slot X. The arbiter must be inserted into Slot X to manage the multiple bus master slot-specific signals.
3. **Can any STD bus processor board operate in a multiple bus master configuration?** No. An STD bus processor board must be designed with multiple bus master operation in mind. This means the processor board must be compatible with the STD 32 architecture and must also include support of the Master Request and Master Acknowledge protocol. The ZT 8903 board is one example of a processor board that meets these requirements. Check the board's STD 32 compliance level for "MD,MX."
4. **Do the bus masters need to be plugged into specific slots?** Yes. The bus masters must be plugged into slots that support the Master Request and Master Acknowledge signals. Refer to the data sheet for the selected STD 32 backplane to determine which slots support slot-specific signals.

   The jumpers on the ZT 89CT39 must be installed to route the slot-specific Master Request and Master Acknowledge signals from each CPU slot to the Arbiter chip. See "Master Signal Selection" later in this chapter.

FUNCTIONAL BLOCKS

The "ZT 89CT39 Functional Block Diagram" figure illustrates the board's major functional blocks. A description of the board's features and functional blocks can be found in the following topics.

STD 32 Slot X Interface

The ZT 89CT39 must be inserted in the left-most slot of an STD 32 backplane. The left-most slot, also referred to as Slot X, supports the slot-specific Master Request and Master Acknowledge signals from up to 15 other slots. It is through these signals that up to seven bus masters gain access to shared STD bus resources. The ZT 89CT39 does not require software programming and as such, does not occupy memory or I/O address space.

Master Signal Selection

The ZT 89CT39 includes a jumper selection block to assign the slot-specific Master Request and Master Acknowledge signals to an input level on the arbiter. There are 15 slot-specific slots and seven arbiter input levels. The most common selections are made with the installation of shorting jumpers; you can make other selections by using wire-wrap techniques. Masters must use one of two request/acknowledge protocols, MREQ/MAK or DREQ/DAK, to access the arbiter. The ZT 89CT39 will accept either protocol without the user having to explicitly know which is being used by a given processor board.

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Arbiter

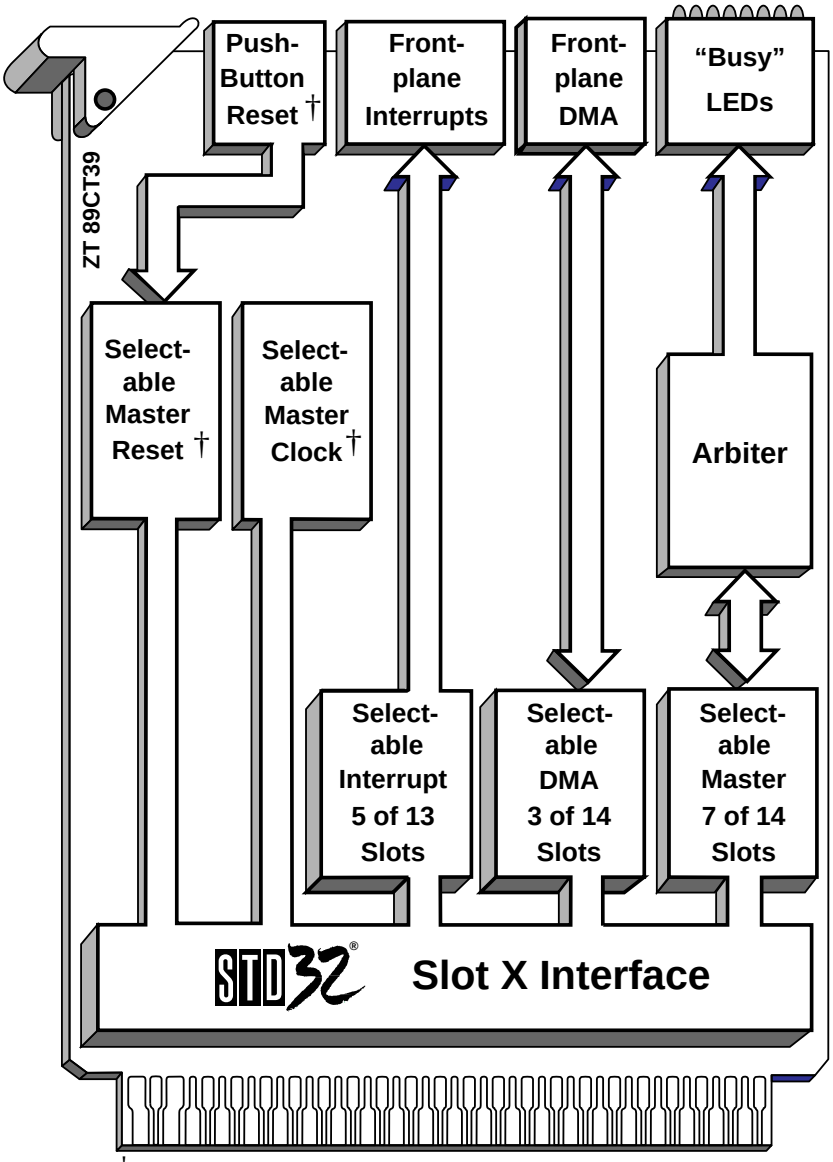
Any board designed for multiple bus master operation supports two handshake signals used to gain access to the shared STD bus resources. These signals are either:

- DMA Request (DREQx*) and DMA Acknowledge (DAKx*)

or:

- Master Request (MREQX*) and Master Acknowledge (MAKX*).

The arbiter monitors DMA/Master Request and generates DMA/Master Acknowledge for up to seven bus masters with a fixed or rotating priority.



† ZT 89CT39X only.

Functional Block Diagram.

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Interrupts

In addition to Master Request and Master Acknowledge, the STD 32 architecture supports a slot-specific interrupt request. The ZT 89CT39 provides a mechanism (frontplane connector J1) to route the slot-specific interrupt requests from the STD 32 backplane to a frontplane cable that is supported by Ziatech bus masters. This is useful when the application requires one bus master to interrupt another bus master.

Status LEDs

Eight light emitting diodes (LEDs) are provided on the ZT 89CT39 to indicate the relative amount of time each bus master is in control of STD bus resources. These LEDs can also be used as diagnostic indicators during system software development. The eighth LED indicates a non-maskable interrupt.

DMA Connector

Three slot-specific DMA Request and Acknowledge lines are brought out to the frontplane (connector J2) for use with CPU boards that support frontplane DMA (but not slot-specific DMA).

Reset Button (ZT 89CT39X Only)

A reset button is provided to generate SYSRESET* when the "DRIVE RESET" jumper is installed.

DC Power Fail Reset (ZT 89CT39X Only)

A power monitor device senses +5 V power and generates SYSRESET* if Vcc drops below 4.625 V. The "DRIVE RESET" jumper also selects this option.

CLOCK (ZT 89CT39X Only)

The CLOCK* signal is driven by the ZT 89CT39X when the "DRIVE CLOCK" jumper is installed.

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CHAPTER 2. GETTING STARTED

This chapter summarizes the information you need to make your ZT 89CT39 operational. You should read this chapter before you attempt to use the board.

UNPACKING

Please check the shipping carton for damage. If the shipping carton and contents are damaged, notify the carrier and Ziatech for an insurance settlement. Retain the shipping carton and packing material for inspection by the carrier. Do not return any product to Ziatech without a Return Material Authorization (RMA) number. Appendix B explains the procedure for obtaining an RMA number from Ziatech.

WHAT'S IN THE BOX?

The items listed below are included in your ZT 89CT39 order.

- ZT 89CT39 STD 32 Slot X Arbiter board in an anti-static bag
- On-Line Help disk for ZT 89CT39
- Optional paper version of the user's manual

Save the anti-static bag for storing or returning the ZT 89CT39.

WARNING!

Like all equipment utilizing MOS devices, the ZT 89CT39 must be protected from static discharge. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the ZT 89CT39 to handle the board.

SYSTEM REQUIREMENTS

The ZT 89CT39 is designed for use only in an STD 32 backplane, not in an STD-80 backplane. The ZT 89CT39 is electrically, mechanically, and functionally compatible with the *STD 32 Bus Specification* (ZT MSTD32).

The ZT 89CT39 requires +5 VDC ±5% at 150 mA maximum. The ambient temperature range must be maintained between -40 and +85° Celsius to guarantee proper operation and to avoid damage. Relative humidity must be less than 95% at 40° Celsius, non-condensing. Refer to "Electrical And Environmental Specifications" in Appendix A for additional specifications.

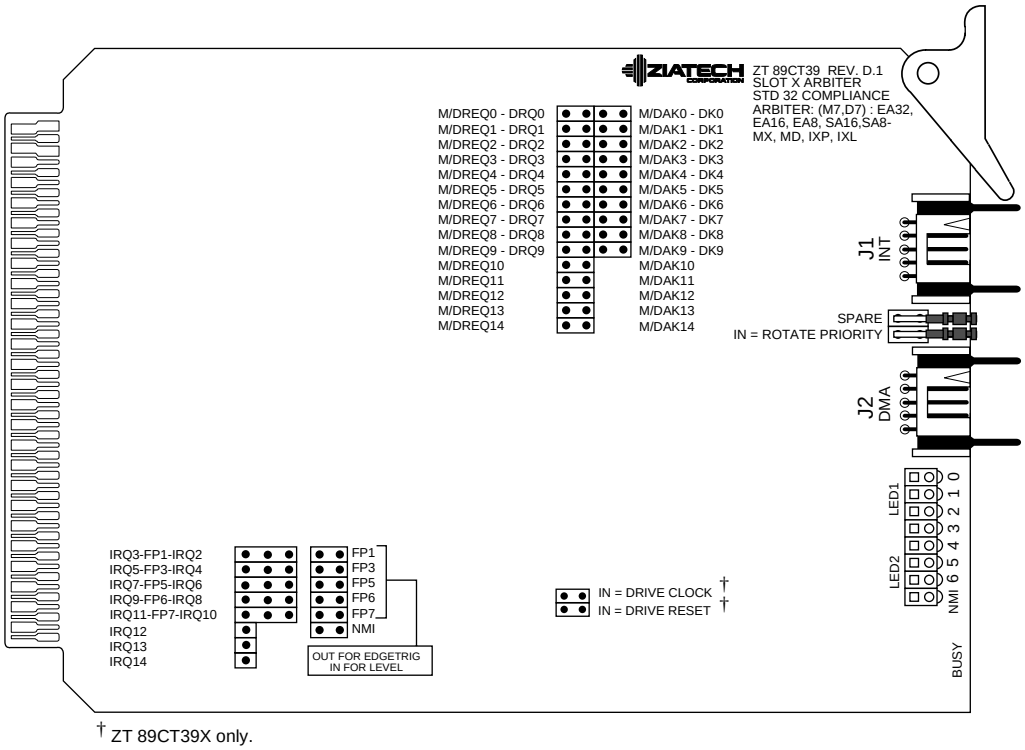
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JUMPER OPTIONS

The ZT 89CT39 includes several jumper options to tailor the board's operation to the requirements of specific applications. The jumpers on the ZT 89CT39 are labeled with signal names. The "ZT 89CT39 Jumper Locations" figure illustrates the jumper locations for your reference. The "Default Jumper Configuration" figure illustrates the factory default jumper configuration.

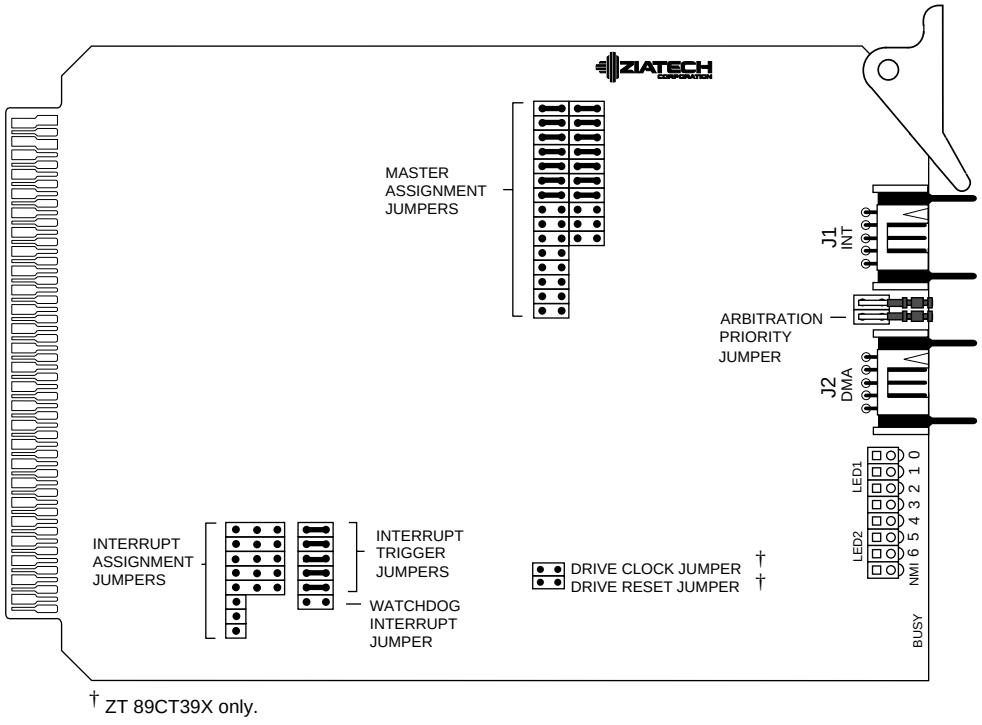
The jumpers can be divided into the following functional groups for discussion.

- Master Assignment
- Interrupt Assignment
- Interrupt Trigger
- Watchdog Interrupt
- Arbitration Priority
- Reset Selection (ZT 89CT39X only)
- Clock Selection (ZT 89CT39X only)



ZT 89CT39 Jumper Locations.

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Default Jumper Configuration.

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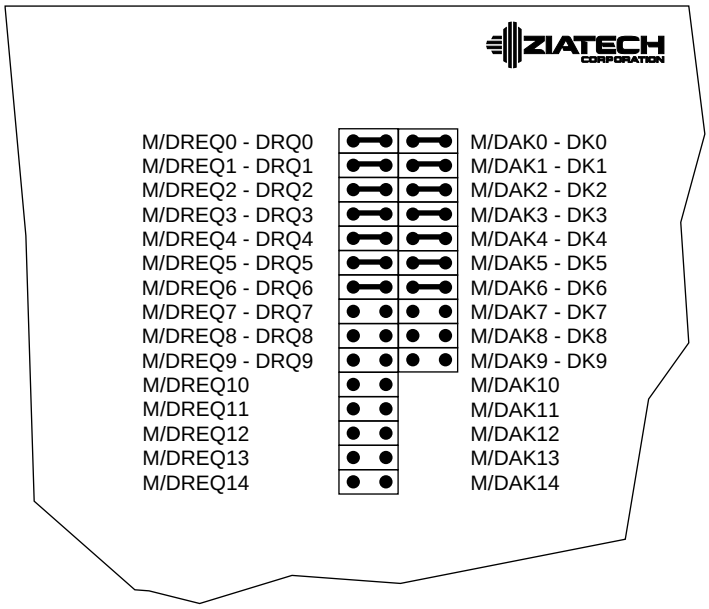
Master Assignment Jumpers

The master assignment jumpers are illustrated below. These jumpers route the slot-specific multiple master, Master Request, and Master Acknowledge signals from the backplane to the arbiter.

The STD 32 architecture includes up to 15 slots that support Master/DMA Request and Master/DMA Acknowledge. The request and acknowledge signals from the backplane (either MREQx* and MAKx* or DREQx* and DAKx*) are connected to jumper posts labeled "M/DREQx" and "M/DAKx", where "x" is a slot number from 0 through 14. The request and acknowledge signals to and from the arbiter are connected to jumper posts labeled "DRQx" and "DKx", where "x" is an arbiter level from 0 through 6.

The most common configuration connects the slot 0 bus master to the level 0 arbiter input, the slot 1 bus master to the level 1 arbiter input, and so on, with up to 7 jumper pairs. Other configurations can be implemented with wire-wrap techniques.

Note: DK0-DK6 must always be jumpered to an M/DAKx pin in order to insure consistent Arbiter operation.



Master Assignment Jumpers.

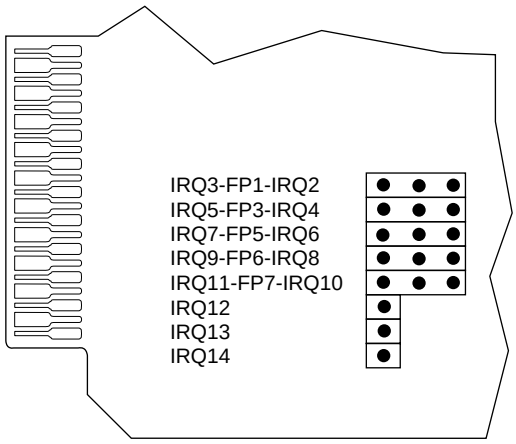
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Interrupt Assignment Jumpers

The interrupt assignment jumpers are illustrated below. These jumpers route the slot-specific interrupt requests from the STD 32 backplane to the J1 frontplane connector.

In addition to the three shared interrupt request signals INTRQ*, INTRQ1*, and INTRQ2*, the STD 32 architecture includes up to 15 slots, each supporting a unique interrupt request. The slot-specific interrupt request signals from the backplane are labeled "IRQx," where "x" is a slot number from 3 through 14. The interrupt request signals to connector J1 are labeled "FPx," where "x" is 1, 3, 5, 6, and 7. The "FPx" designation is defined in the Ziatech frontplane interrupt standard with "x" being the interrupt level to which the request is connected on the programmable interrupt controller. The 10-pin standard defines FP1, 3, 5, 6, and 7 to connect to J1 pins 2, 4, 6, 8, and 10.

The most common configuration connects IRQ3, 5, 7, 9, and 11 to FP1, 3, 5, 6, and 7. Other configurations are available through jumper selection and wire-wrap techniques. Using the IRQ3 to FP1 selection as an example, this means the slot 3 interrupt request is connected to FP1 (J1 pin 2), which connects through a ribbon cable to FP1 on any bus master. FP1 on the bus master normally connects to IR1 on the bus master programmable interrupt controller.



Interrupt Assignment Jumpers.

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Interrupt Trigger Jumpers

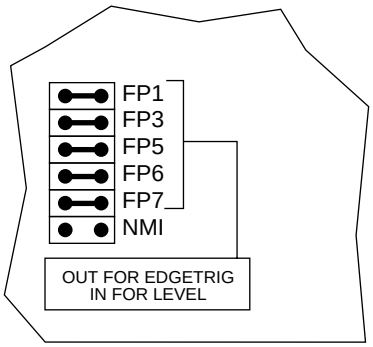
The interrupt trigger jumpers are illustrated below. These jumpers individually configure the FP1, 3, 5, 6, and 7 interrupts for edge-triggered or level-triggered operation. Installing one of these jumpers configures the associated interrupt as level-triggered and removing the jumper configures the interrupt as edge-triggered.

The selection depends on the programmable interrupt controller located on the bus master to which the interrupt is connected. If the interrupt controller is programmed for edge-triggered operation, the associated interrupt should be jumpered for edge-triggered operation. If the interrupt controller is programmed for level-triggered operation, the associated interrupt should be jumpered for level-triggered operation.

Watchdog Interrupt

The watchdog interrupt jumper, grouped with the interrupt trigger jumpers, is labeled "NMI." Installing this jumper enables the generation of the STD bus Non-Maskable Interrupt NMIRQ* in the event that any one bus master monopolizes the bus. Removing the jumper eliminates this watchdog feature. The default configuration removes the jumper.

For a bus master to be in control of STD bus resources, the associated Master Request and Master Acknowledge signals must both be active. The arbiter removes the Master Acknowledge of the bus master currently in control of the STD bus resources within 2 clocks of the assertion of Master Acknowledge. At this time, the watchdog timer starts counting STD bus clock cycles while waiting for the bus master to release STD bus resources and remove Master Request. If 256 clock cycles (32 microseconds) pass before the bus master removes the Master Request, the STD bus Non-Maskable Interrupt is generated.

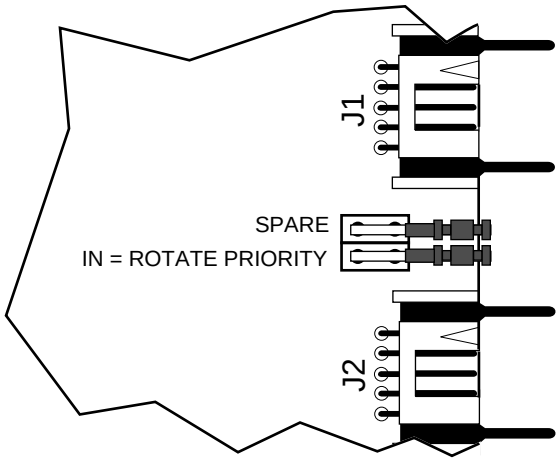


Interrupt Trigger Jumpers.

Arbitration Priority Jumper

The arbitration priority jumper is illustrated below. It selects the arbitration priority to be fixed or rotating. Installing this jumper selects rotating priority; removing this jumper selects fixed priority. Rotating and fixed priority are discussed in more detail in Chapter 3.

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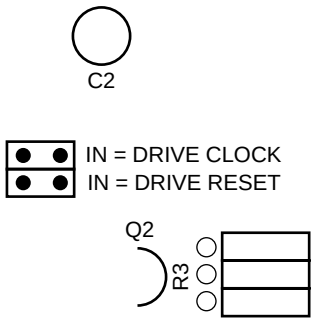
Arbitration Priority Jumper.

Reset Selection (ZT 89CT39X Only)

The Drive Reset jumper, illustrated below, selects both DC power fail reset and push-button reset which drive SYSRESET*. Installing the jumper enables both functions. When the jumper is installed, the permanent master must ***not*** drive SYSRESET*. Consult the manual for your CPU to determine how to disable its SYSRESET*.

Clock Selection (ZT 89CT39X Only)

The Drive Clock jumper, illustrated below, selects the clock source for the STD bus. Installing the jumper selects clock to be driven by the ZT 89CT39X. When the jumper is installed, the permanent master must ***not*** drive CLOCK*. Consult the manual for your CPU to determine how to disable its CLOCK*.



Reset/Clock Selection Jumpers.

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CHAPTER 3. STD BUS INTERFACE

The ZT 89CT39 operates in the left-most slot of an STD 32 backplane. This slot, known as Slot X, provides access to the slot-specific Master Request, Master Acknowledge, and Interrupt Request signals supported by the ZT 89CT39. This chapter defines the operation of the ZT 89CT39 relative to these signals.

FIXED AND ROTATING PRIORITIES

The arbiter supports two methods for servicing requests from more than one bus master: fixed priority and rotating priority. Before we discuss fixed and rotating priorities, it is important to understand how bus masters operate.

Bus masters are generally designed to support both bus hold and bus release operation. In bus hold operation, the bus master gains control of the STD bus resources and does not release them until requested to do so by the arbiter. In bus release operation, the bus master gains control of the STD bus resources, performs the operation, and releases control of the STD bus resources. The advantage of bus hold operation is the bus master does not have to arbitrate for repeated STD bus transfers if no other bus masters are in need of STD bus resources or are present in the system.

Note that the arbiter will request that the current master release the bus 250 ns after the arbiter has granted use of the bus. Depending on the algorithm used by a CPU in bus hold mode operation, this timing could limit the effectiveness of bus hold mode.

Fixed Priority Operation

In a fixed priority architecture, the arbiter input levels have a decreasing priority with level 0 being the highest and level 6 being the lowest. This is illustrated in the "Fixed Priority Operation" figure. The bus masters must be configured for bus release operation. The following example illustrates a fixed priority arbitration sequence.

1. The system is powered on and the level 1 bus master is the first to make a request for STD bus resources.
2. The arbiter grants the level 1 bus master control of the STD bus resources. At this point, all requests from the level 2 through 6 bus masters are ignored because they are of lower priority. These requests are not latched, meaning they must be held active until they are acknowledged.
3. The level 0 bus master generates a request for the STD bus resources.
4. The level 1 bus master completes its STD bus operation and relinquishes bus ownership.
5. The arbiter grants the level 0 bus master control of the STD bus resources. At this point, all other requests are ignored because they are of lower priority. It is not until the level 0 bus master relinquishes bus ownership that any other bus master request is processed. This is the reason the bus masters cannot use bus hold operation mode for fixed priority operation.

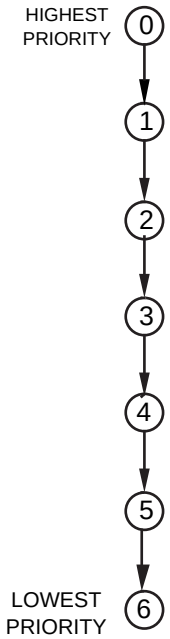
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Rotating Priority Operation

In a rotating priority architecture, the arbiter input levels change in priority as each is serviced. In rotating priority operation, input levels 0 through 6 support a rotating priority. This is illustrated in the "Rotating Priority Operation" figure. The bus masters may be configured for bus hold mode or bus release mode; all input levels are supported.

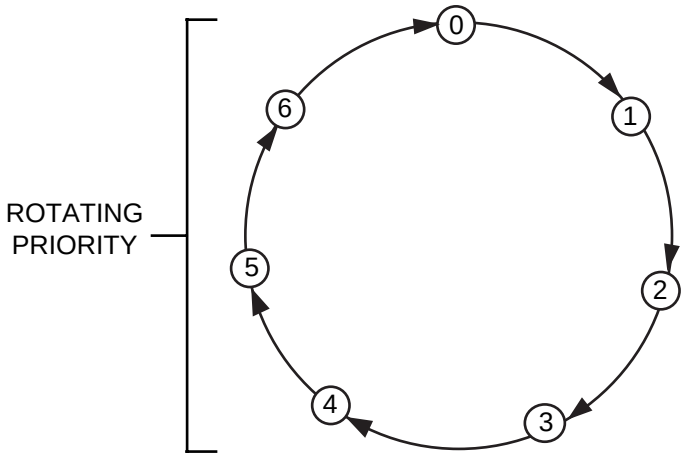
The following example illustrates a rotating priority operation.

1. The system is powered on and the level 1 bus master is the first to make a request.
2. The arbiter grants the level 1 bus master control of the STD bus resources. At this point, requests from levels 2 through 6 and 0 are monitored. These requests are not latched, meaning they must be held active until they are acknowledged.
3. The level 0 bus master generates a request for the STD bus resources.
4. The arbiter requests the level 1 bus master to relinquish control of the STD bus resources if it has not already done so.
5. The level 1 bus master completes STD bus operation and relinquishes bus ownership.
6. The arbiter grants the level 0 bus master control of the STD bus resources. Note that if the level 3 bus master had a request pending at the same time as level 0, the level 3 bus master's request would have been acknowledged first.



Fixed Priority Operation.

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Rotating Priority Operation.

WATCHDOG TIMER

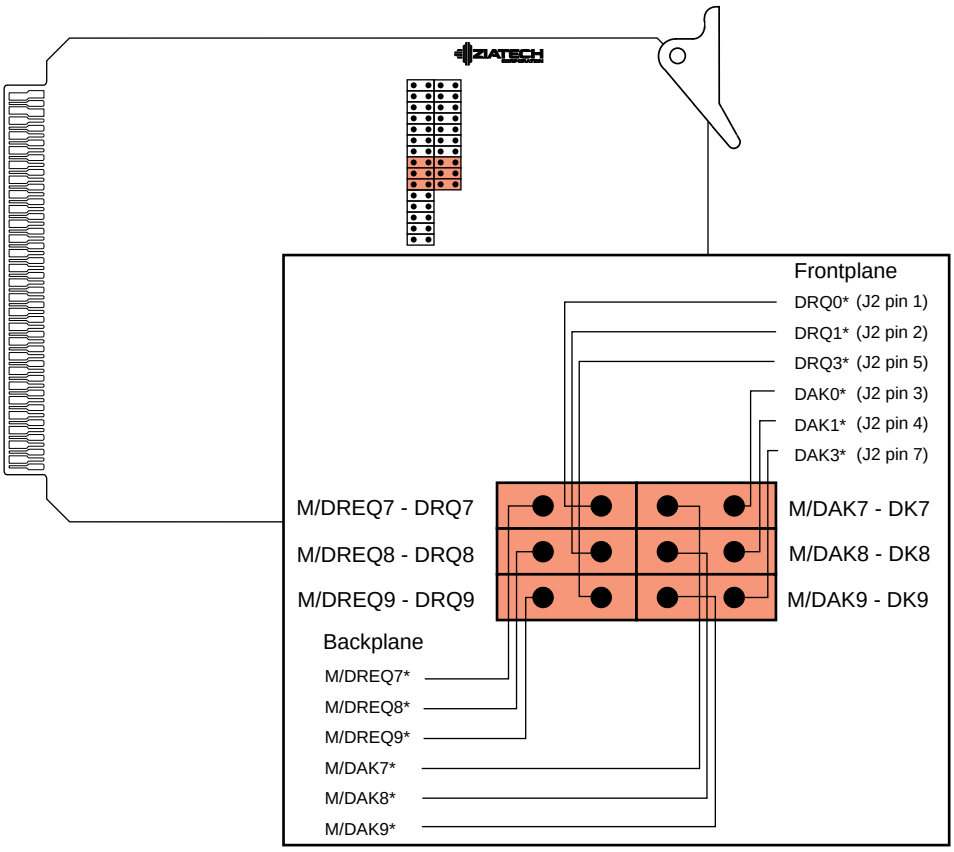
During operation, once a bus master is granted control of STD bus resources, it is not required to release them until requested to do so by the arbiter. The arbiter makes this request within two clock cycles of granting the master's request. When the arbiter makes this request, the watchdog timer begins a timeout period that lasts 256 STD bus clock cycles (32 microseconds). If the current bus master does not release the resources within this time period, the watchdog timer can be jumpered to generate an STD bus Non-Maskable Interrupt Request.

DMA CONNECTOR

The STD 32 specification defines the backplane slot-specific DMA Request and Acknowledge signals. CPUs that do not occupy Slot X (for example, ZT 8901 and ZT 8902) cannot make use of these signals. Connector J2 on the ZT 89CT39 allows routing three DMA Request/Acknowledge pairs to the frontplane for use by CPUs.

Jumper posts M/DREQ7-DRQ7 through M/DREQ9-DRQ9 connect to frontplane DMA Request channels DRQ0*, DRQ1*, and DRQ3* (see the figure below). Jumper posts M/DAK7-DK7 through M/DAK9-DK9 connect to frontplane DMA Acknowledge channels DAK0*, DAK1*, and DAK3*. Installing jumpers connects DRQ0*, DRQ1*, and DRQ3* to M/DREQ7* through M/DREQ9* and DAK0*, DAK1*, and DAK3* to M/DAK7* through M/DAK9*. Other pairs may be chosen by use of wire-wrap techniques.

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Frontplane DMA Jumpers.

STATUS INDICATORS

Eight light emitting diodes (LEDs) on the ZT 89CT39 provide operating status. Seven of the LEDs are labeled BUSY 0 through BUSY 6. The busy LEDs indicate which bus master is currently in control of STD bus resources. The BUSY 0 LED is associated with the level 0 arbiter input, the BUSY 1 LED is associated with the level 1 arbiter input, and so on. Infrequent accesses by a bus master may not be visible on the LED.

The final LED indicates a non-maskable interrupt. The NMI LED is active when the watchdog timer counts to zero. That is, the LED becomes active whenever a lower priority master does not relinquish the bus within 256 STD bus clock cycles (32 microseconds).

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APPENDIX A. SPECIFICATIONS

This appendix contains the electrical, mechanical, and environmental specifications for the ZT 89CT39, as well as STD 32 and frontplane connector pin assignments.

ELECTRICAL AND ENVIRONMENTAL SPECIFICATIONS

The following topics provide the electrical and environmental specifications for the ZT 89CT39, including absolute maximum ratings, DC operating characteristics, and STD bus loading characteristics.

Absolute Maximum Ratings

Supply Voltage, Vcc 0 to 7 V

Storage Temperature -55° to +125° Celsius

Operating Temperature -40° to +85° Celsius

DC Operating Characteristics

Supply Voltage, Vcc: 4.75 to 5.25 V

Supply Current, Vcc: 110 mA typ., 150 mA max

Non-condensing relative humidity < 95% at 40° Celsius

STD Bus Loading Characteristics

Unit load is a convenient method by which to specify input and output drive capability of STD bus boards. Using this method, one unit load is equal to one LSTTL load as follows:

- Current for single input load: 20 µA
- Current for single output drive: -400 µA

The unit load reflects the current requirements at worst case conditions over recommended supply voltage and ambient temperature ranges. An output drive of 60 unit loads drives 60 STD bus boards having input ratings of one unit load. The tables "ZT 89CT39 STD Bus Loading, E Connector, Slot X" and "ZT 89CT39 STD Bus Loading, P Connector, Slot X" include load values for the ZT 89CT39 interface signals.

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ZT 89CT39 STD Bus Loading, E Connector, Slot X

PIN (CIRCUIT SIDE) / OUTPUT DRIVE / INPUT LOAD / MNEMONIC							PIN (COMPONENT SIDE) / OUTPUT DRIVE / INPUT LOAD / MNEMONIC
RSVD [1]			E2	E1		REQ	GND [1]
RSVD [1]			E4	E3			RSVD [1]
RSVD [1]			E6	E5			RSVD [1]
RSVD [1]			E8	E7			RSVD [1]
RSVD [1]			E10	E9			RSVD [1]
RSVD [1]			E12	E11			RSVD [1]
+5VDC	REQ		E14	E13		REQ	+5VDC
DAK0*		15	E16	E15		1	DREQ0*
GND	REQ		E18	E17		REQ	GND
DAK2*		15	E20	E19		1	DREQ2*
DAK4*		15	E22	E21		1	DREQ4*
DAK6*		15	E24	E23		1	DREQ6*
DAK8*		15	E26	E25		1	DREQ8*
GND	REQ		E28	E27			RSVD
DAK11*		15	E30	E29		1	DREQ11*
DAK13*		15	E32	E31		1	DREQ13*
AEN14*			E34	E33			IRQ14
RSVD			E36	E35		REQ	GND
AEN11*			E38	E37			IRQ11
AEN9*			E40	E39			IRQ9
AEN7*			E42	E41			IRQ7
AEN5*			E44	E43			IRQ5
AEN3*			E46	E45		REQ	GND
AEN1*			E48	E47			IRQ2
MAK14*			E50	E49			IRQ0
MAK12*			E52	E51			MREQ13*
GND	REQ		E54	E53			MREQ11*
MAK10*			E56	E55			MREQ10*
MAK8*			E58	E57			MREQ8*
MAK7*			E60	E59			MREQ6*
MAK5*			E62	E61			MREQ5*
MREQ4*			E64	E63			MREQ3*
MAK2*			E66	E65			MAK1*
+5VDC	REQ		E68	E67			MREQ1*
MAK0*			E70	E69			MREQ0*
RSVD [1]			E72	E71			RSVD [1]
RSVD [1]			E74	E73			RSVD [1]
RSVD [1]			E76	E75			RSVD [1]
RSVD [1]			E78	E77			RSVD [1]
RSVD [1]			E80	E79			RSVD [1]

Notes:
[1] Not implemented.

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ZT 89CT39 STD Bus Loading, P Connector, Slot X.

PIN (CIRCUIT SIDE) / OUTPUT DRIVE / INPUT LOAD / MNEMONIC							PIN (COMPONENT SIDE) / OUTPUT DRIVE / INPUT LOAD / MNEMONIC
+5VDC	REQ		P2	P1		REQ	+5VDC
GND	REQ		P4	P3		REQ	GND
DAK1*		15	P6	P5		1	DREQ1*
DAK3*		15	P8	P7		1	DREQ3*
DAK5*		15	P10	P9		1	DREQ5*
DAK7*		15	P12	P11		1	DREQ7*
DAK9*		15	P14	P13		1	DREQ9*
DAK10*		15	P16	P15		1	DREQ10*
DAK12*		15	P18	P17		1	DREQ12*
DAK14*		15	P20	P19		1	DREQ14*
AEN13*			P22	P21			IRQ13
AEN12*			P24	P23			IRQ12
AEN10*			P26	P25			IRQ10
AEN8*			P28	P27			IRQ8
AEN6*			P30	P29			IRQ6
AEN4*			P32	P31			IRQ4
AEN2*			P34	P33			IRQ3
AEN0*			P36	P35			IRQ1
MAK13*			P38	P37			MREQ14*
MAK11*			P40	P39			MREQ12*
BUSRQ*			P42	P41			BUSAK*
MAK9*			P44	P43			MREQ9*
NMIRQ*			P46	P45			MREQ7*
MAK6*			P48	P47			SYSRESET*
MAK4*			P50	P49			CLOCK*
MAK3*			P52	P51			MREQ2*
AUX GND	REQ		P54	P53		REQ	AUX GND
AUX -			P56	P55			AUX +

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MECHANICAL SPECIFICATIONS

The following topics include specifications for ZT 89CT39 card dimensions and weight and for ZT 89CT39 connector descriptions and pinouts.

Card Dimensions and Weight

The ZT 89CT39 meets all mechanical requirements of the STD 32 bus specification. The ZT 89CT39 must be inserted into Slot X of an STD 32 backplane. Mechanical dimensions are shown in the "Card Dimensions" figure and are outlined below.

Board Length: 6.500 ±0.025

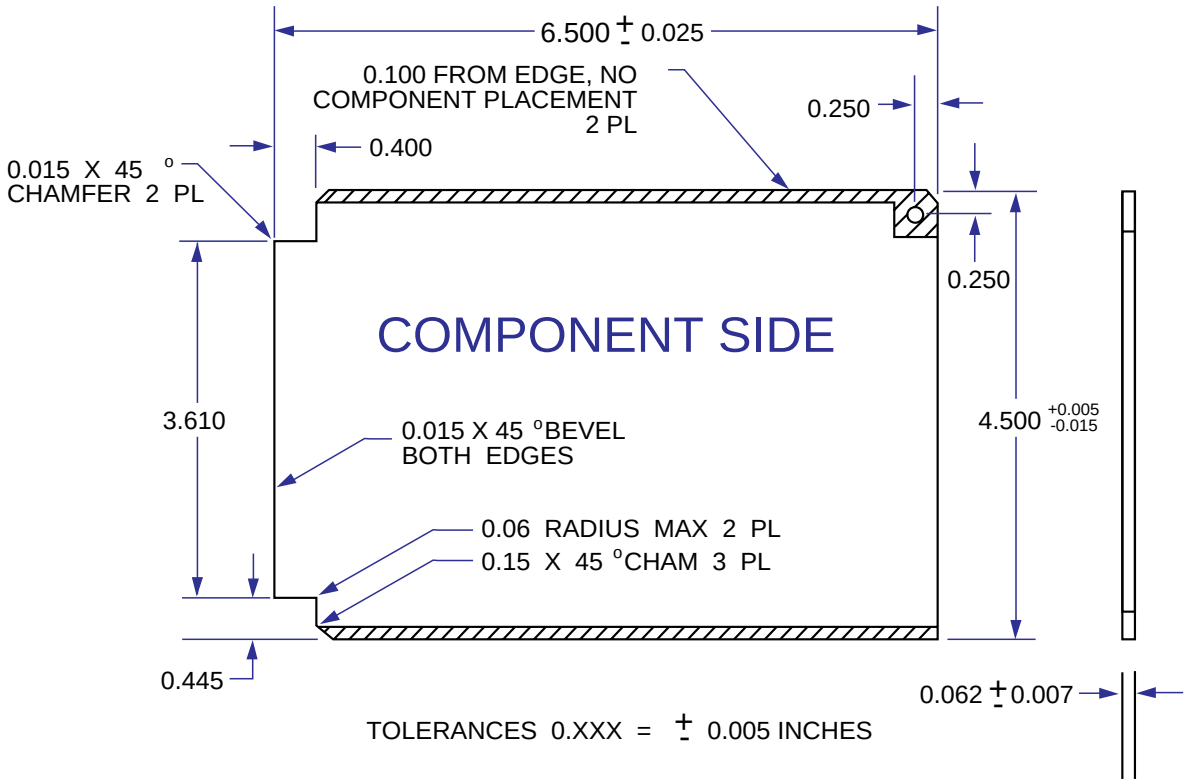
Board Width: 4.500 ±0.015

Board Thickness: 0.062 ±0.005

Board Weight: 2 oz.

Board Height From Top Surface: 0.38" max.

Board Height From Bottom Surface: 0.04" max.



Card Dimensions.

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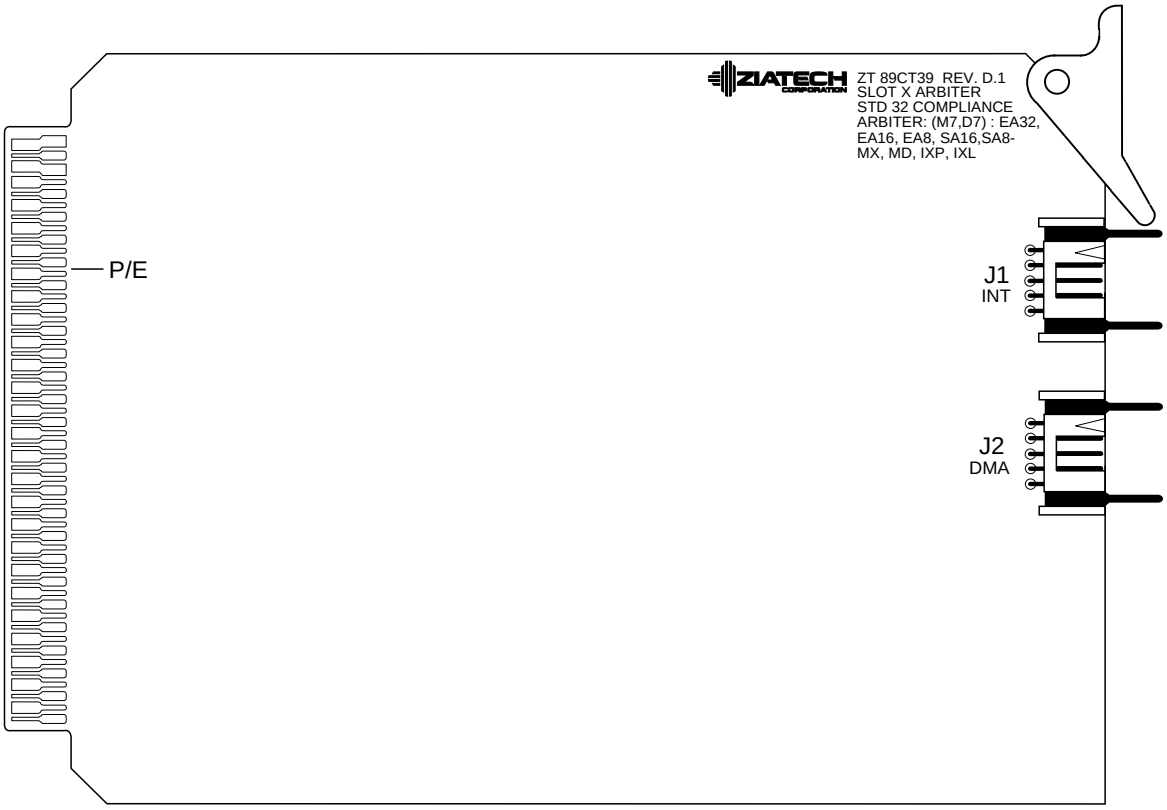
Connector Specifications

The ZT 89CT39 includes connectors to interface to Slot X on the STD 32 backplane and to route the slot-specific interrupt requests over the frontplane. The "Connector Locations" illustration shows the their positions on the board. The following topics provide descriptions and pinouts for these connectors.

P and E: STD-80 and STD 32 bus, respectively

J1: Frontplane interrupts

J2: DMA



Connector Locations.

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P&E: The ZT 89CT39's backplane interface is composed of two sets of finger patterns: 56 "P" fingers carrying the original STD-80 signals, and 80 "E" fingers carrying the additional STD 32 signals. The two sets of fingers are interleaved to create a 136-pin (dual 68-pin) STD 32 interface. Pin-to-pin spacing is 0.0625 inches.

Mating connectors are a Viking S3VT68/5DE12 or equivalent for a three-level wire wrap, or a Viking S3VT68/5DP12 or equivalent for the solder tail.

See any of the following table titles to view pin assignments for the P/E connector:

STD 32 P Connector Pinout, Component Side
STD 32 P Connector Pinout, Solder Side
STD 32 E Connector Pinout, Component Side
STD 32 E Connector Pinout, Solder Side

The "STD 32 P/E Connector Pinout" figure shows the pin locations.

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STD 32 P Connector Pinout

Component Side.

Pin No.	Mnemonic	Description
P1	+5 VDC	Logic Power
P3	GND	Logic Ground
P5	DREQ1*	DMA Request
P7	DREQ3*	DMA Request
P9	DREQ5*	DMA Request
P11	DREQ7*	DMA Request
P13	DREQ9*	DMA Request
P15	DREQ10*	DMA Request
P17	DREQ12*	DMA Request
P19	DREQ14*	DMA Request
P21	IRQ13	Interrupt Request
P23	IRQ12	Interrupt Request
P25	IRQ10	Interrupt Request
P27	IRQ8	Interrupt Request
P29	IRQ6	Interrupt Request
P31	IRQ4	Interrupt Request
P33	IRQ3	Interrupt Request
P35	IRQ1	Interrupt Request
P37	MREQ14*	Master Request
P39	MREQ12	Master Request
P41	BUSAK*	Bus Acknowledge
P43	MREQ9	Master Request
P45	MREQ7	Master Request
P47	SYSRESET*	System Reset
P49	CLOCK*	Clock
P51	MREQ2	Master Request
P53	AUX GND	AUX Ground
P55	AUX+	AUX Positive (+12VDC)

Solder Side.

Pin No.	Mnemonic	Description
P2	+5 VDC	Logic Power
P4	GND	Logic Ground
P6	DAK1*	DMA Acknowledge
P8	DAK3*	DMA Acknowledge
P10	DAK5*	DMA Acknowledge
P12	DAK7*	DMA Acknowledge
P14	DAK9*	DMA Acknowledge
P16	DAK10*	DMA Acknowledge
P18	DAK12*	DMA Acknowledge
P20	DAK14*	DMA Acknowledge
P22	AEN13*	Address Enable
P24	AEN12*	Address Enable
P26	AEN10*	Address Enable
P28	AEN8*	Address Enable
P30	AEN6*	Address Enable
P32	AEN4*	Address Enable
P34	AEN2*	Address Enable
P36	AEN0*	Address Enable
P38	MAK13*	Master Acknowledge
P40	MAK11*	Master Acknowledge
P42	BUSRQ*	Bus Request
P44	MAK9*	Master Acknowledge
P46	NMIRQ*	Non-Maskable Interrupt Req
P48	MAK6*	Master Acknowledge
P50	MAK4*	Master Acknowledge
P52	MAK3*	Master Acknowledge
P54	AUX GND	Auxiliary Ground
P56	AUX-	AUX Negative (-12VDC)

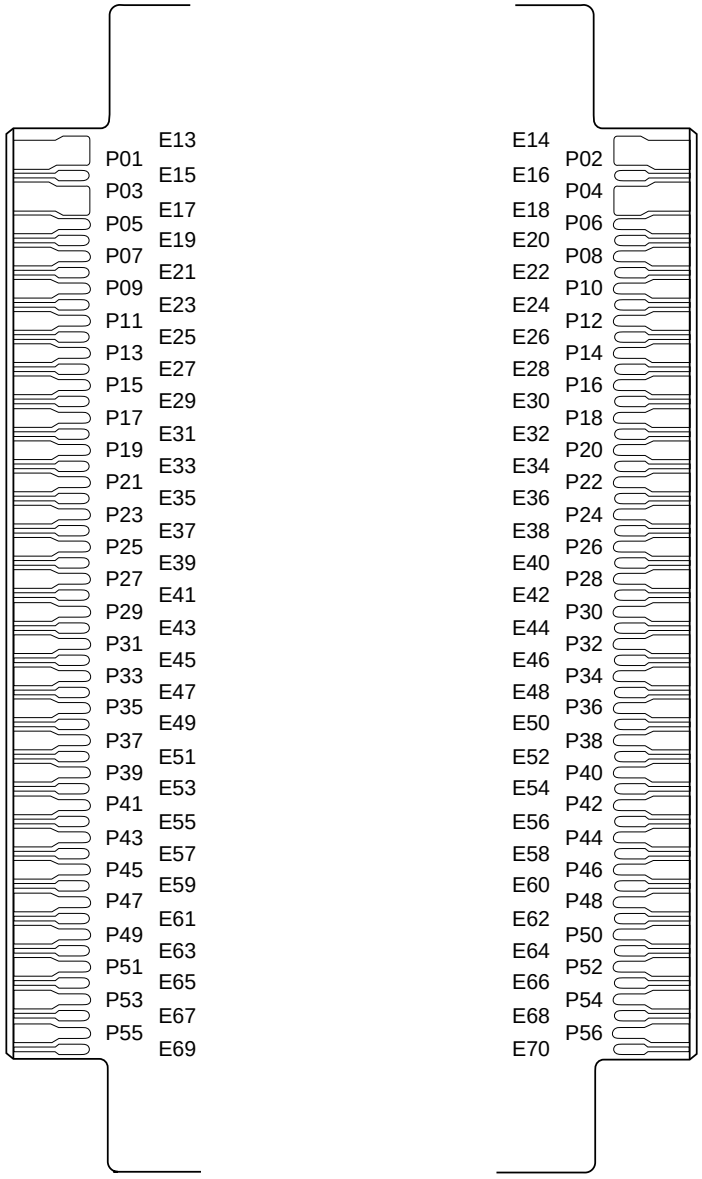
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STD 32 E Connector Pinout

Component Side			Solder Side.		
Pin No.	**Mnemonic**	**Description**	**Pin No.**	**Mnemonic**	**Description**
E1	GND†	Logic Ground	E2	RSVD†	Reserved
E3	RSVD†	Reserved	E4	RSVD†	Reserved
E5	RSVD†	Reserved	E6	RSVD†	Reserved
E7	RSVD†	Reserved	E8	RSVD†	Reserved
E9	RSVD†	Reserved	E10	RSVD†	Reserved
E11	RSVD†	Reserved	E12	RSVD†	Reserved
E13	+5 VDC	Logic Power	E14	+5 VDC	Logic Power
E15	DREQ0*	DMA Request	E16	DAK0*	DMA Acknowledge
E17	GND	Logic Ground	E18	GND	Logic Ground
E19	DREQ2*	DMA Request	E20	DAK2*	DMA Acknowledge
E21	DREQ4*	DMA Request	E22	DAK4*	DMA Acknowledge
E23	DREQ6*	DMA Request	E24	DAK6*	DMA Acknowledge
E25	DREQ8*	DMA Request	E26	DAK8*	DMA Acknowledge
E27	RSVD	Reserved	E28	GND	Logic Ground
E29	DREQ11*	DMA Request	E30	DAK11*	DMA Acknowledge
E31	DREQ13*	DMA Request	E32	DAK13*	DMA Acknowledge
E33	IRQ14	Interrupt Request	E34	AEN14*	Address Enable
E35	GND	Logic Ground	E36	RSVD	Reserved
E37	IRQ11	Interrupt Request	E38	AEN11*	Address Enable
E39	IRQ9	Interrupt Request	E40	AEN9*	Address Enable
E41	IRQ7	Interrupt Request	E42	AEN7*	Address Enable
E43	IRQ5	Interrupt Request	E44	AEN5*	Address Enable
E45	GND	Logic Ground	E46	AEN3*	Address Enable
E47	IRQ2	Interrupt Request	E48	AEN1*	Address Enable
E49	IRQ0	Interrupt Request	E50	MAK14*	Master Acknowledge
E51	MREQ13*	Master Request	E52	MAK12*	Master Acknowledge
E53	MREQ11*	Master Request	E54	GND	Logic Ground
E55	MREQ10*	Master Request	E56	MAK10*	Master Acknowledge
E57	MREQ8*	Master Request	E58	MAK8*	Master Acknowledge
E59	MREQ6*	Master Request	E60	MAK7*	Master Acknowledge
E61	MREQ5*	Master Request	E62	MAK5*	Master Acknowledge
E63	MREQ3*	Master Request	E64	MREQ4*	Master Request
E65	MAK1*	Master Acknowledge	E66	MAK2*	Master Acknowledge
E67	MREQ1*	Master Request	E68	+5 VDC	Logic Power
E69	MREQ0*	Master Request	E70	MAK0*	Master Acknowledge
E71	RSVD†	Reserved	E72	RSVD†	Reserved
E73	RSVD†	Reserved	E74	RSVD†	Reserved
E75	RSVD†	Reserved	E76	RSVD†	Reserved
E77	RSVD†	Reserved	E78	RSVD†	Reserved
E79	RSVD†	Reserved	E80	RSVD†	Reserved

†Not implemented

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STD 32 P/E Connector Pinout.

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J1: J1 is a latching 10-pin (dual 5-pin) male transition connector with 0.1 inch spacing. The slot-specific interrupt request signals are routed to J1 for connection to programmable interrupt controllers on bus masters, as required. The J1 signals are labeled "FPx" where "x" is the interrupt controller input level defined for this signal in the Ziatech standard for frontplane interrupts. The mating connector is a T & B Ansley #622-1001, or equivalent.

J1 Interrupt Pinout.

Pin	Signal	Description
2	FP1*	Frontplane Request 1
4	FP3*	Frontplane Request 3
6	FP5*	Frontplane Request 5
8	FP6*	Frontplane Request 6
10	FP7*	Frontplane Request 7
1-9 Odds	GND	Ground

J2: J2 is a latching 10-pin (dual 5-pin) male transition connector with 0.1 inch spacing. The slot-specific DMA request and acknowledge signals are routed to J2 for connection (via the CPU master's frontplane DMA connector) to a DMA controller. The mating connector is a T & B Ansley #622-1001 or equivalent.

J2 DMA Pinout.

Pin	Signal	Description
1	DRQ0*	Frontplane DMA Request 0 (ZT 8902 Channel 0)
2	DRQ1*	Frontplane DMA Request 1 (ZT 8902 Channel 1)
3	DAK0*	Frontplane DMA Acknowledge 0 (ZT 8902 Channel 0)
4	DAK1*	Frontplane DMA Acknowledge 1 (ZT 8902 Channel 1)
5	DRQ3*	Frontplane DMA Request 3 (ZT 8902 Channel 3)
6	N/C	No Connect
7	DAK3*	Frontplane DMA Acknowledge 3 (ZT 8902 Channel 3)
8	N/C	No Connect
9	GND	Ground
10	N/C	No Connect

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APPENDIX B. CUSTOMER SUPPORT

This appendix offers a product revision history, technical assistance for the ZT 89CT39, the Ziatech 5 + 5 warranty, and the necessary information should you need to return your ZT 89CT39 for repair.

REVISION HISTORY

Revision 0

The ZT 89CT39 was initially released on 10/15/90.

Revision A

Revision A supported the use of the ZT 8910 as a permanent master (using BUSRQ*/BUSAK*) with up to six other bus masters.

Revision B

This version is backward compatible with Revision A only if ZT 8910 use is not required. It is then a superset, compatible with Revision 0 and Revision A.

Revision B added a 10-pin DMA connector to route slot-specific DMA channels to the frontplane.

Revision C

This version is backward compatible with Revision B.

Revision C changed the arbitration algorithm to one that always removes master acknowledge within two clock cycles of granting it. This simplification works with all currently existing CPU boards in the STD 32 marketplace. It corrects an infrequent failure mechanism found when using ZT 8902s.

Revision C provides rotating priority arbitration for up to 7 masters without the need for a jumper (required by Rev. B) by utilizing one large rotating wheel of up to 7 masters.

This revision also extends the NMI timeout from 64 clocks to 256 clocks to account for the time floppy disks take to complete a FIFO transfer.

Revision D.1

This version is backward compatible with Revision C.

Revision D.1 created two products, the ZT 89CT39 and the ZT 89CT39X.

ZT 89CT39 Revision D.1 added the ability to accept either MREQx*/MAKx* or DREQx*/DAKx* pairs of request/acknowledge signals. This is invisible to the user. Revision D.1 supports 8, 16, and 32 bit EA transfers for permanent and temporary masters. 8 and 16 bit SA transfers are still supported. This revision also added diode termination networks to all incoming Slot X signals and added resistive series terminations to all outgoing Slot X signals.

ZT 89CT39X Revision D.1 adds the following features to the ZT 89CT39. SYSRESET* and CLOCK* are jumper selectable to be driven by the ZT 89CT39X. The SYSRESET* signal can be asserted by pressing the push-button reset switch and will automatically be asserted when Vcc drops below 4.625 V. The CLOCK* signal can be used in place of a Permanent Master clock to provide the 8 MHz backplane clock.

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TECHNICAL/SALES ASSISTANCE

If you have a technical question, please call Ziatech's Customer Support Service at one of the numbers below, or e-mail our technical support team at tech_support@ziatech.com.

If you have a sales question, please contact your local Ziatech Sales Representative or the Regional Sales Office for your area.

Additional information is available at Ziatech's website, located at *http://www.ziatech.com*.

Corporate Headquarters

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San Luis Obispo, CA 93401 USA

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Austin, TX 78752 USA

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FAX (512) 458-3178

Eastern Regional Office

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Exton, PA 19341 USA

Tel (610) 524-9070

FAX (610) 524-9072

European Office

P.O Box 110

5690 AC SON

The Netherlands

Tel 31-(0)499-477666

FAX 31-(0)499-474463

RELIABILITY

Ziatech has taken extra care in the design of the ZT 89CT39 to assure reliability. Four major ways in which reliability is achieved are:

1. The product is designed with the latest hardware and software techniques. All interconnections undergo extensive timing and parametric analysis over the entire specified operating range.
2. The components on the ZT 89CT39 are high-reliability parts.
3. Ziatech quality assurance tests include inspection at several stages of manufacturing and temperature cycling under power to eliminate infant mortality.
4. Each ZT 89CT39 is marked with an identification number used to track the product. Any negative reliability trends are identified and corrected immediately.

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RETURNING FOR SERVICE

Before returning any of Ziatech's products, you must phone Ziatech at (805) 541-0488 and obtain a Return Material Authorization (RMA) number. We require the following information to expedite shipment of your board to you:

1. Your company name and address for invoice
2. Shipping address and phone number
3. Product identification number
4. If possible, the name of a technically qualified individual at your company familiar with the mode of product failure

If the unit is out of warranty, service is available at a predesignated service charge. Contact Ziatech for pricing and please supply a purchase order number for invoicing the repair.

Pack the ZT 89CT39 in *anti-static* material and ship in a sturdy cardboard box with enough packing material to adequately cushion it. **Any product returned to Ziatech improperly packed will immediately void the warranty for that particular product!** Mark the RMA number clearly on the outside of the box before returning.

ZIATECH 5+5 WARRANTY

Ziatech provides a five year limited warranty to its customers with a special extended warranty option. Ziatech also has an explicit policy regarding the use of Ziatech products in life support systems. These topics are covered in the following sections.

Five-Year Limited Warranty

Products manufactured by Ziatech Corporation are covered from the date of purchase by a five-year warranty against defects in materials, workmanship, and published specifications applicable to the date of manufacture. During the warranty period, Ziatech will repair or replace, solely at its option, defective units provided they are returned at customer expense to an authorized Ziatech repair facility. Products which have been subjected to misuse, abuse, neglect, alteration, or unauthorized repair, determined at the sole discretion of Ziatech, whether by accident or otherwise, are excluded from warranty. The warranty on fans and disk drives is limited to two years and the warranty on flat panel displays is limited to nine months from date of purchase. Other products and accessories not manufactured by Ziatech are limited to the warranty provided by the original manufacturer. Consumable items (fuses, batteries, etc.) and software are not covered by this warranty.

Ziatech Corporation warrants that for a period of ninety (90) days from the date of purchase; the media on which software is furnished will be free of defects in materials and workmanship under normal use; and the software contains the features described in the Ziatech price list. Otherwise, the software is provided "AS IS". This limited warranty extends only to Customer as the original licensee. Customer's exclusive remedy and Ziatech's entire liability under this limited warranty will be, at Ziatech's option, to repair or replace the software, or refund the license fee paid therefore.

Ziatech may offer, where applicable and available, replacement products; otherwise, repairs requiring components, assemblies, and other purchased materials may be limited by market availability.

Ziatech assumes no liability resulting from changes to government regulations affecting use of materials, equipment, safety, and methods of repair. Ziatech may, at its discretion, offer replacement products.

THE ABOVE WARRANTY IS IN LIEU OF ANY OTHER WARRANTY, WHETHER EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING, BUT NOT LIMITED TO, ANY WARRANTY FOR

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FITNESS OF PURPOSE, MERCHANTABILITY, OR FREEDOM FROM INFRINGEMENT OR THE LIKE, AND ANY WARRANTY OTHERWISE ARISING OUT OF ANY PROPOSAL, SPECIFICATIONS, OR SAMPLE.

Ziatech neither assumes nor authorizes any person to assume for it any other liability. The liability of Ziatech under this warranty agreement is limited to a refund of the purchase price. In no event shall Ziatech be liable for loss of profits, use, incidental, consequential, or other damage, under this agreement.

Special Extended Warranty Option

In addition to the standard five-year warranty, Ziatech offers, for a nominal fee, an extended period of warranty up to five extra years. This extended warranty period provides similar coverage and conditions as stated above in the five-year limited warranty agreement.

Life Support Policy

Ziatech products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Ziatech Corporation. As used herein:

1. Life support devices or systems are devices or systems which support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be expected to cause the failure of the life support device or system, affect its safety, or limit its effectiveness.

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