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SONY

# CX20201A-1/-2/-3
# CX20202A-1/-2/-3

## 10/9/8-bit 160MSPS D/A Converter

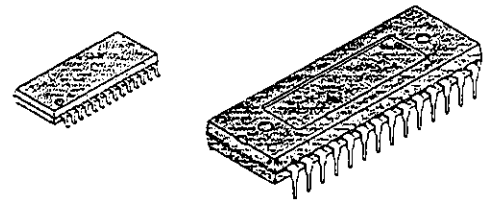
### Descriptions

A series of D/A converters CX20201A/CX20202A convert binary data into an analog signal at rates higher than 160 MHz. The devices include input data registers and have a capability of driving 75 ohms load. Three versions with linearity specifications of 10, 9 or 8 bits are available for each model.

These D/A converter ICs can be used in signal processings which require high speed and high resolution D/A conversions such as high quality displays, high definition video systems, digital measurement instruments and radars.

| | |
|---|---|
| CX20201A-1/CX20202A-1 | 10-bit |
| CX20201A-2/CX20202A-2 | 9-bit |
| CX20201A-3/CX20202A-3 | 8-bit |

28pin SOP(Plastic) 28pin DIP(Plastic)



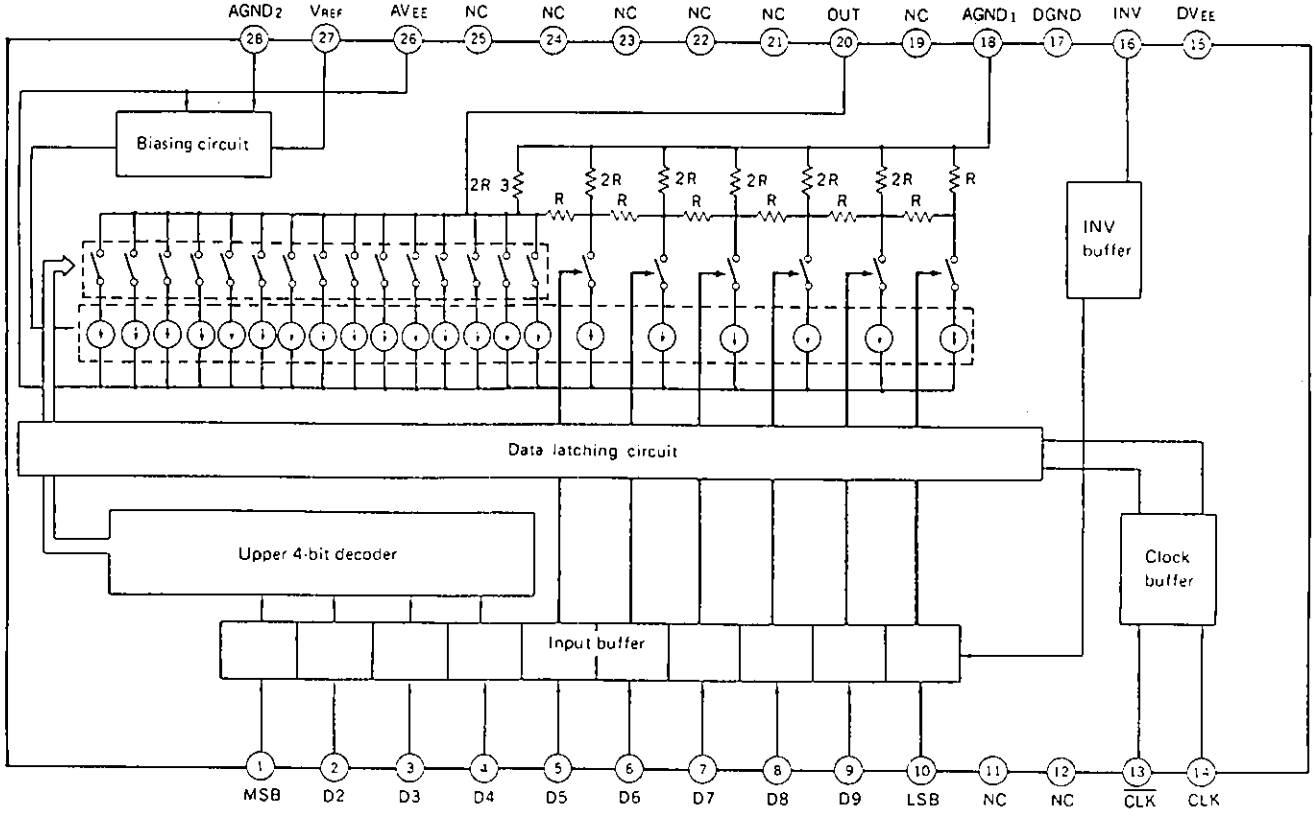
### Features

- High speed 160 MHz
- High accuracy 10 bit (CX20201A-1/CX20202A-1)
- Low glitch energy 15 pVsec
- Low power consumption 420 mW
- Logic invert input
- 75-Ω direct drive capability
- Analog multiplying function

### Structure

Bipolar silicon monolithic IC.

### Block Diagram and Pin Configuration (Top View)






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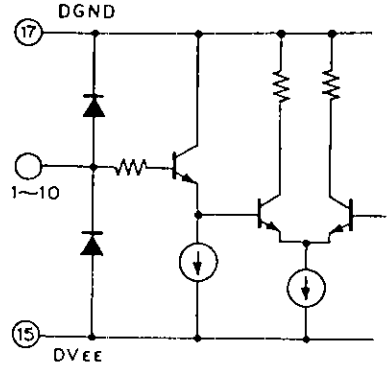
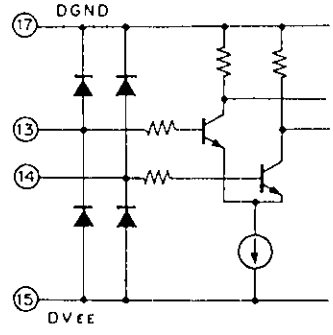
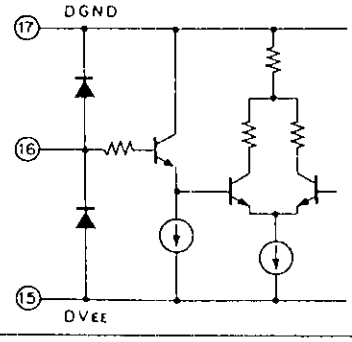
## Absolute Maximum Ratings (Ta = 25°C)

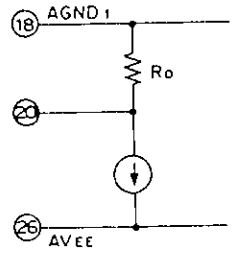
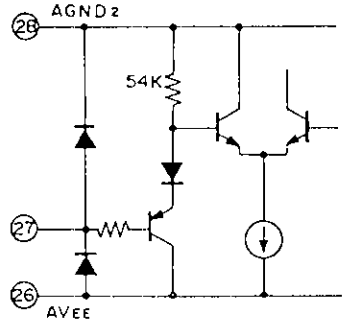
| | | | |
|---|---|---|---|
| • Supply voltage | $V_{EE}$ | −7 | V |
| • Digital input voltage | $V_I$ | +0.3 to $V_{EE}$ | V |
| • Reference input voltage | $V_{REF}$ | +0.3 to $V_{EE}$ | |
| • Analog output current | $I_{OUT}$ | 20 | mA |
| • Operating temperature | $T_{ope}$ | −20 to + 75 | °C |
| • Storage temperature | Tstg | −55 to +150 | °C |
| • Allowable power dissipation | $P_D$ | | |
| CX20201A-1/-2/-3 | | 870 | mW |
| CX20202A-1/-2/-3 | | 1430 | mW |

## Recommended Operating Conditions

| | | | | | |
|---|---|---|---|---|---|
| • Supply voltage | $AV_{EE}$, $DV_{EE}$ | −4.75 | to | −5.45 | V |
| | $AV_{EE}$-$DV_{EE}$ | −0.05 | to | +0.05 | V |
| • Digital input voltage | $V_{IH}$ | −1.0 | to | −0.7 | V |
| | $V_{IL}$ | −1.9 | to | −1.6 | V |
| • Reference input voltage | $V_{REF}$ | $V_{EE}$+0.5 | to | $V_{EE}$+1.4 | V |
| • Load resistance | $R_L$ | above 75 | | | Ω |
| • Output voltage | $V_{O(FS)}$ | 0.8 | to | 1.2 | V |

## Pin Description

| No. | Symbol | Equivalent circuit | Description |
|---|---|---|---|
| 1<br>2<br>3<br>4<br>5<br>6<br>7<br>8<br>9<br>10 | MSB<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7<br>D8<br>D9<br>LSB |  | Input pin for digital data. MSB and LSB are corresponded to the most significant bit and least significant bit, respectively. Pins not used should be left open or connected to DVEE. |
| 11<br>12 | NC | | Non-connection |
| 13<br>14 | $\overline{\text{CLK}}$<br>CLK |  | Pins for clock inputs. |
| 15 | DVEE | | Power supply pin for digital circuit. |
| 16 | INV |  | Code invert input pin which inverts the relationship between the binary code of digital data and D/A output voltage level. |
| 17 | DGND | | Grounding pin for digital circuit. |
| 18 | AGND1 | | Grounding pin directly connected to the R-2R output resistor circuit network in the IC. Grounding for analog circuit system. |
| 19 | NC | | Non-connection |

| No. | Symbol | Equivalent circuit | Description |
|---|---|---|---|
| 20 | OUT |  | D/A analog output. |
| 21<br>22<br>23<br>24<br>25 | NC | | Non-connection |
| 26 | $AV_{EE}$ | | Power supply pin for analog circuit. |
| 27 | $V_{REF}$ |  | Bias pin which controls D/A output range. The output scale is set by the potential difference between $V_{REF}$ and $AV_{EE}$. |
| 28 | $AGND_3$ | | Grounding pin for analog circuit system other than the R-2R output resistor circuit network in the IC |

**Electrical Characteristics (1)** Ta = 25°C, $AV_{EE}$ = $DV_{EE}$ = −5.2V, AGND = DGND = 0V, $R_L$ = ∞, $V_{O(FS)}$ = −1V

CX20201A-1/CX20202A-1

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Resolution | RES | | 10 | | bit |
| Differential linearity error | ELD | −1/2 | | +1/2 | LSB |
| Linearity error | ELI | −0.1 | | +0.1 | % of FS |
| Settling time | $t_S$ | | 5.2 | | ns |

CX20201A-2/CX20202A-2

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Resolution | RES | | 9 | | bit |
| Differential linearity error | ELD | −1/2 | | +1/2 | LSB |
| Linearity error | ELI | −0.1 | | +0.1 | % of FS |
| Settling time | ts | | 4.7 | | ns |

CX20201A-3/CX20202A-3

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Resolution | RES | | 8 | | bit |
| Differential linearity error | ELD | −1/2 | | +1/2 | LSB |
| Linearity error | ELI | −0.2 | | +0.2 | % of FS |
| Settling time | ts | | 4.3 | | ns |

**Electrical Characteristics (2)** Ta = 25°C, AVEE = DVEE = −5.2V, AGND = DGND = 0V, RL = ∞, VO(FS) = −1V

| Item | | Symbol | Measuring condition*1 | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Power supply current | CX20201A | $I_{EE}$ | | −60 | −75 | −90 | mA |
| | CX20202A | | | −65 | −82 | −100 | |
| Data input current (for upper 4 bits) | | $I_{IH(U)}$ | $V_{IH}$ = −0.89V | 0.1 | 1.5 | 6.0 | μA |
| | | $I_{IL(U)}$ | $V_{IL}$ = −1.75V | 0.1 | 1.5 | 6.0 | μA |
| Data input current (for lower 6 bits) | | $I_{IH(L)}$ | $V_{IH}$ = −0.89V | 0.1 | 0.75 | 3.0 | μA |
| | | $I_{IL(L)}$ | $V_{IL}$ = −1.75V | 0 | 0.75 | 3.0 | μA |
| Clock input current | | $I_{CLKH}$ | $V_{IH}$ = −0.89V | 2 | 23 | 70 | μA |
| Invert input current | | $I_{INVH}$ | $V_{IH}$ = −0.89V | 0.1 | 1.5 | 6.0 | μA |
| Reference input current | | $I_{REF}$ | $V_{REF}$ = −4.58V | −3 | −0.4 | −0.1 | μA |
| Output resistance | | $R_O$ | Io = −1mA | 52 | 65 | 78 | Ω |
| Maximum conversion rate | | fc | $R_L$ = 75Ω | 160 | | | MSPS |
| Output voltage full-scale deviation | | $V_{O(FS)}$ | $V_{REF}$ = −4.58V | 0.90 | 1.00 | 1.10 | V |
| Set-up time | | $t_{su}$ | | 5.0 | | | ns |
| Hold time | | $t_{hd}$ | | 1.0 | | | ns |

*1 See Figs. 3 to 5.

## Data for Typical Application

Ta = 25°C, AVEE = DVEE = −5.2V, AGND = DGND = 0V, RL = ∞, VO(FS) = −1V

| Item | Symbol | Measuring condition | Typ. | Unit |
|---|---|---|---|---|
| Output voltage zero offset | EZS | $R_L \geqq 10k\Omega$ | −7 | mV |
| | | $R_L = 75\Omega$ | −7 | |
| Output voltage full-scale temperature coefficient | $T_{C(FS)}$ | $R_L \geqq 10k\Omega$ | −140 | ppm/°CV |
| | | $R_L = 75\Omega$ | −580 | |
| Output voltage zero offset temperature coefficient | $T_{C(ZS)}$ | $R_L \geqq 10k\Omega$ | 16 | μV/°C |
| Glitch energy | GE | Digital ramp | 15 | pVsec |
| Rise time | $t_r$ | $R_L = 75\Omega$ | 1.5 | ns |
| Fall time | $t_f$ | | 1.5 | ns |
| Propagation delay | $t_d$ | | 3.8 | ns |
| Band width for multiplying | $BW_{MUL}$ | $R_L = 75\Omega$, −3dB | 14 | MHz |

## Timing Chart

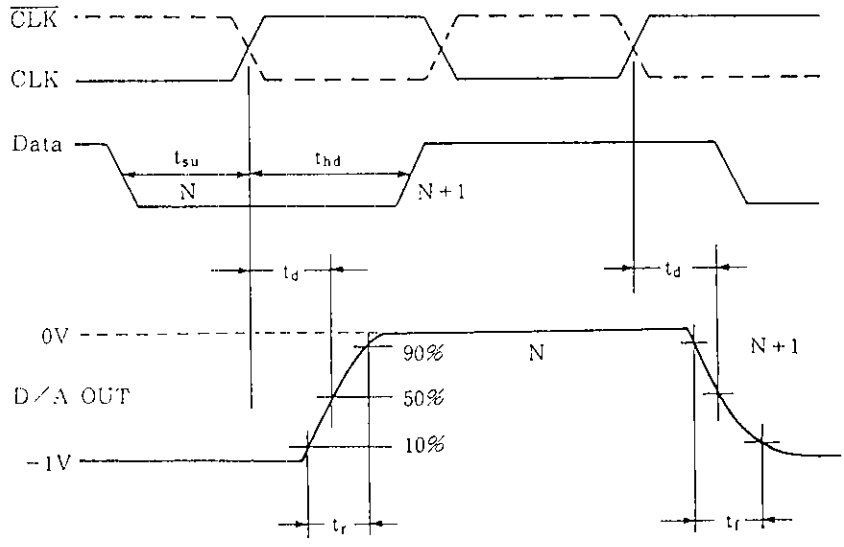



Fig. 1

## Input Coding Table

| Input code | Output code (V) | |
|---|---|---|
| | INV = 1 | INV = 0 |
| 0 0 0 ····· 0 0 | 0 | −1 |
| ⋮ | ⋮ | ⋮ |
| 0 1 1 ····· 1 1 | −0.5 | −0.5 |
| 1 0 0 ····· 0 0 | ⋮ | ⋮ |
| 1 1 1 ····· 1 1 | −1 | 0 |

## Measuring Conditions for Current Consumption, Input Current and Output Resistance (See Fig. 2.)

| Test item | Symbol | Switch condition | | | | | | | | | | | | | | | | | | | | | | Test point |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 | S10 | S11 | S12 | S13 | S14 | S15 | S16 | S17 | S18 | S19 | S20 | S21 | | |
| Current consumption | $I_{EE}$ | b | b | b | b | b | b | b | b | b | b | b | b | b | b | b | a | b | b | b | b | b | | I1 |
| Data input current for upper 4 bits (H level) | $I_{IH(U)}$ | a | b | b | b | b | b | b | b | b | b | a | b | b | b | b | b | b | b | b | b | b | | I2 |
| | | b | a | b | b | | | | | | | | | | | | | | | | | | | |
| | | b | b | a | b | | | | | | | | | | | | | | | | | | | |
| | | b | b | b | a | | | | | | | | | | | | | | | | | | | |
| Data input current for lower 4 bits (L level) | $I_{IL(U)}$ | a | b | b | b | b | b | b | b | b | b | b | b | b | b | b | b | b | b | b | b | b | | I2 |
| | | b | a | b | b | | | | | | | | | | | | | | | | | | | |
| | | b | b | a | b | | | | | | | | | | | | | | | | | | | |
| | | b | b | b | a | | | | | | | | | | | | | | | | | | | |
| Data input current for upper 6 bits (H level) | $I_{IH(L)}$ | b | b | b | b | a | b | b | b | b | b | a | b | b | b | b | b | b | b | b | b | b | | I2 |
| | | | | | | b | a | b | b | b | b | | | | | | | | | | | | | |
| | | | | | | b | b | a | b | b | b | | | | | | | | | | | | | |
| | | | | | | b | b | b | a | b | b | | | | | | | | | | | | | |
| | | | | | | b | b | b | b | a | b | | | | | | | | | | | | | |
| | | | | | | b | b | b | b | b | a | | | | | | | | | | | | | |
| Data input current for lower 6 bits (L level) | $I_{IL(L)}$ | b | b | b | b | a | b | b | b | b | b | b | b | b | b | b | b | b | b | b | b | b | | I2 |
| | | | | | | b | a | b | b | b | b | | | | | | | | | | | | | |
| | | | | | | b | b | a | b | b | b | | | | | | | | | | | | | |
| | | | | | | b | b | b | a | b | b | | | | | | | | | | | | | |
| | | | | | | b | b | b | b | a | b | | | | | | | | | | | | | |
| | | | | | | b | b | b | b | b | a | | | | | | | | | | | | | |
| Clock input current (H level) | $I_{CLKH}$ | b | b | b | b | b | b | b | b | b | b | b | a | b | b | a | b | b | b | b | b | b | | I3 |
| Clock-bar input current (H level) | $I_{\overline{CLK}H}$ | b | b | b | b | b | b | b | b | b | b | b | b | a | a | b | b | b | b | b | b | b | | I4 |
| Invert input current (H level) | $I_{INVH}$ | b | b | b | b | b | b | b | b | b | b | b | b | b | b | b | b | a | a | b | b | b | | I5 |
| Referecnce input current | $I_{REF}$ | b | b | b | b | b | b | b | b | b | b | b | b | b | b | b | b | b | b | b | b | a | | I6 |
| Output resistance | $R_O$ | b | b | b | b | b | b | b | b | b | b | b | b | b | b | b | b | b | b | a | a | b | | V1 |

## Electrical Characteristics Test Circuit

### Test Circuit for Current Consumption, Input Current and Output Resistance

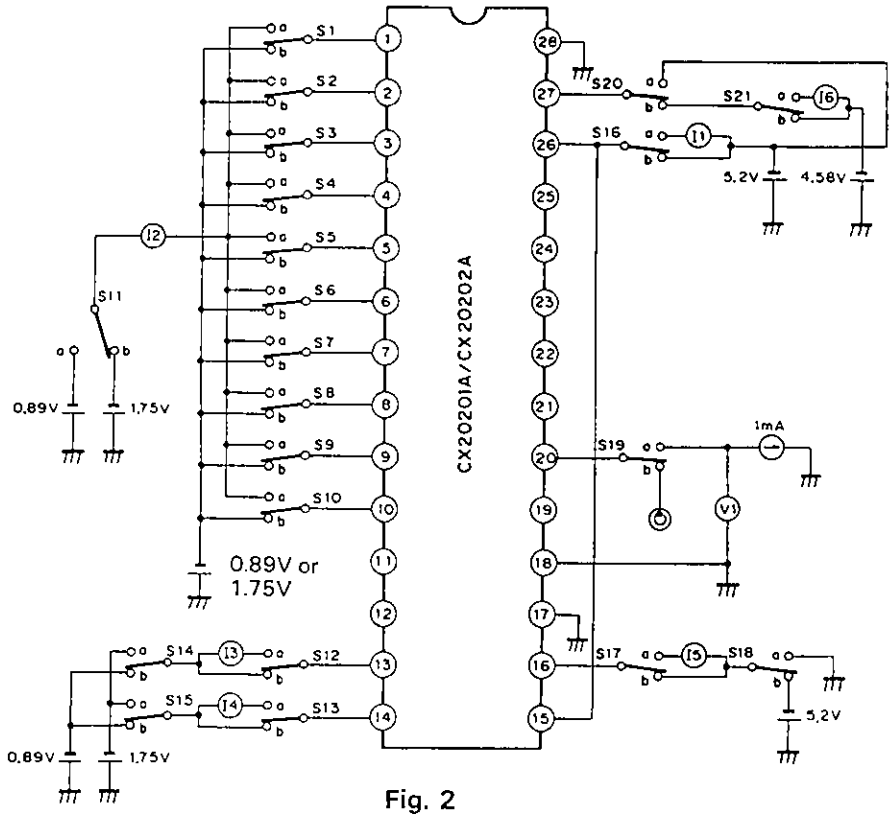
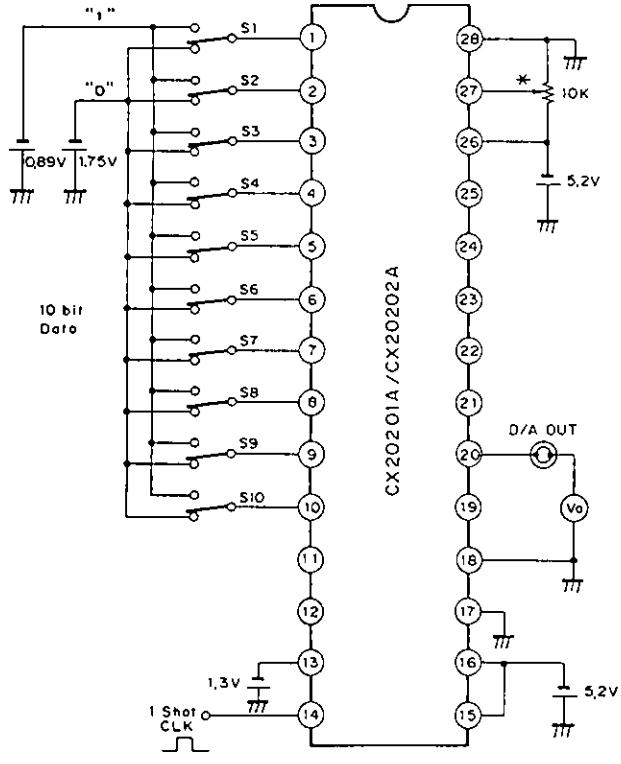



Fig. 2

### Test Circuit for Differential Linearity Error and Linearity Error




* Adjust so that the full scale of DC voltage at Pin 20 becomes 1.023V, that is, to satisfy $V_0 - V_{1023} = 1.023V$.

Fig. 3

Linearity errors are measured as follows.

| S1 | S2 | S3 | ····· | S9 | S10 | D/A out |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | ····· | 0 | 0 | $V_0$ |
| 0 | 0 | 0 | ····· | 0 | 1 | $V_1$ |
| 0 | 0 | 0 | ····· | 1 | 0 | $V_2$ |
| | | | ⋮ | | | ⋮ |
| 1 | 1 | 1 | ····· | 1 | 1 | $V_{1023}$ |

| Linearity error | Differential linearity error |
|---|---|
| $V_0$ | |
| $V_1$ | $V_1 - V_0$ |
| $V_2$ | $V_2 - V_1$ |
| $V_4$ | $V_4 - V_3$ |
| $V_8$ | $V_8 - V_7$ |
| $V_{16}$ | $V_{16} - V_{15}$ |
| $V_{32}$ | $V_{32} - V_{31}$ |
| $V_{64}$ | $V_{64} - V_{63}$ |
| $V_{128}$ | $V_{128} - V_{127}$ |
| $V_{192}$ | $V_{192} - V_{191}$ |
| ⋮ | ⋮ |
| $V_{960}$ | $V_{960} - V_{959}$ |
| $V_{1023}$ | |

Errors at individual measurement points are calculated according to the following definition.

$(V_{1023} - V_0)/1023 = V_{0(FS)}/1023 \equiv 1$ LSB.

Test circuits for
- Maximum conversion rate
- Rise time
- Fall time
- Propagation delay
- Set-up time
- Hold time
- Settling time

DL: delay line (ELMEC VDS1110)
Capacitors are 0.047 μF ceramic chip capacitors unless otherwise specified.

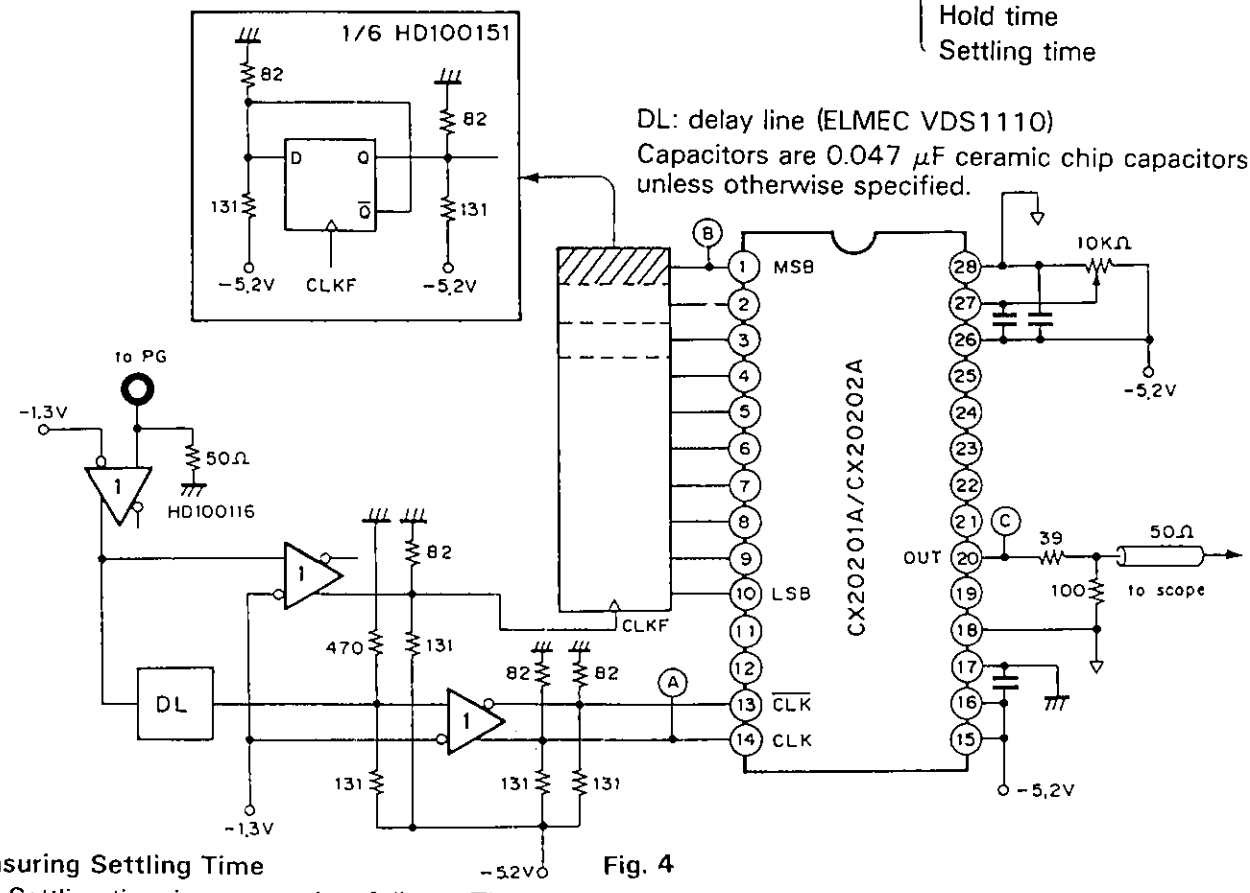



Fig. 4

## Measuring Settling Time

Settling time is measured as follows. The relationship between V and $V_{O(FS)}$ as shown in the D/A output waveform in Fig. 5 is expressed as

$V = V_{O(FS)} (1 - e^{-t/\tau})$.

The settling time for respective accuracy of 10 , 9 and 8-bit is specified as

$V = 0.9995\ V_{O(FS)}$
$V = 0.999\ V_{O(FS)}$
$V = 0.998\ V_{O(FS)}$

which results in the following:

$t_s = 7.60\tau$ for 10-bit,
$t_s = 6.93\tau$ for 9-bit, and
$t_s = 6.24\tau$ for 8-bit

Rise time ($t_r$) and fall time ($t_f$) are defined as the time interval to slew from 10% to 90% of full scale voltage ($V_{O(FS)}$):

$V = 0.1\ V_{O(FS)}$
$V = 0.9\ V_{O(FS)}$

and calculated as $t_r = t_f = 2.20\ \tau$.
The settling time is obtained by combining these expressions:

$t_s = 3.45 t_r$ for 10-bit,
$t_s = 3.15 t_r$ for 9-bit, and
$t_s = 2.84 t_r$ for 8-bit

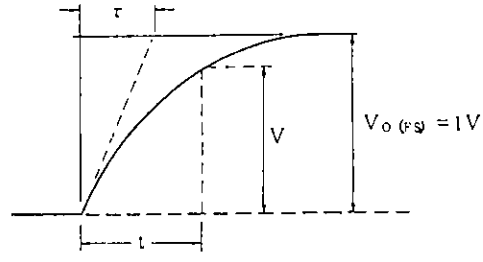



Fig. 5

## Test Circuit for Multiplying Band Width

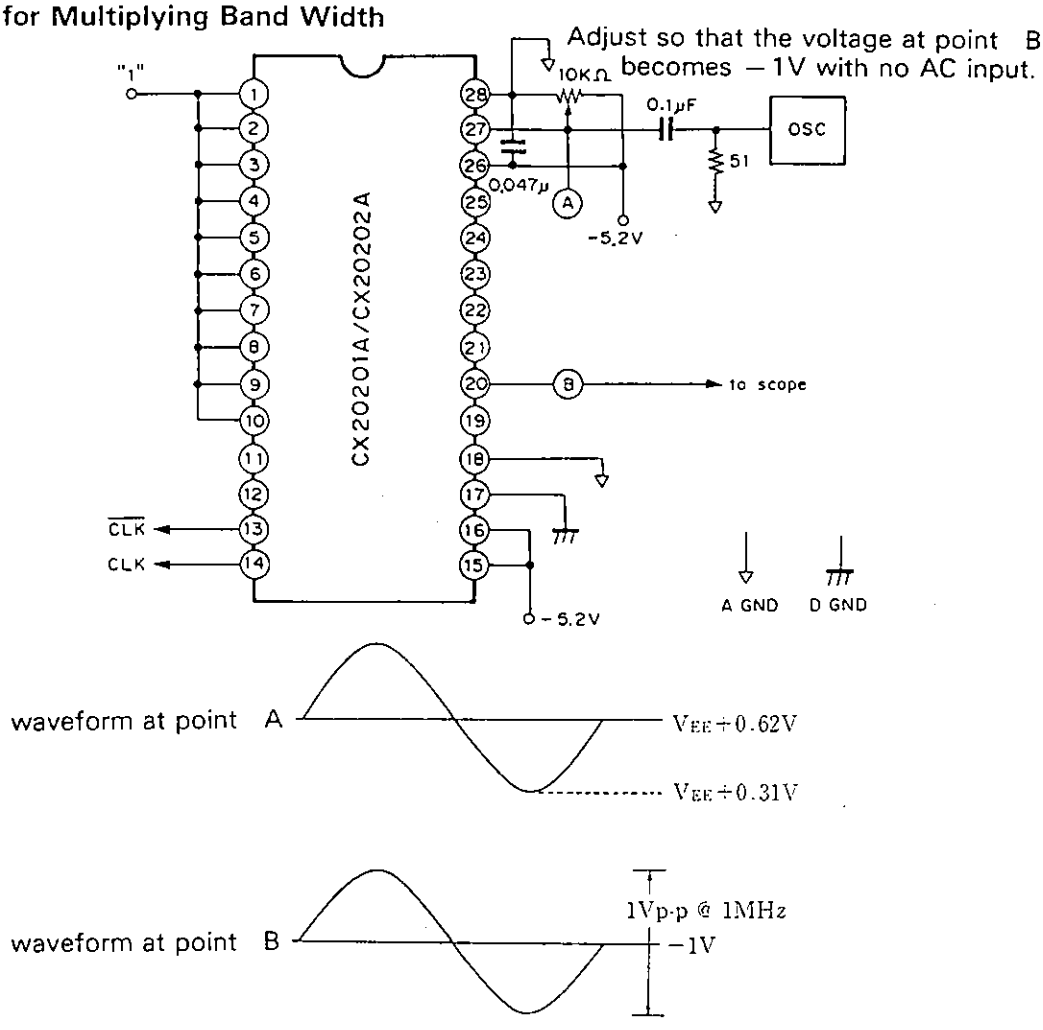



Fig. 6

## Typical Application Circuit

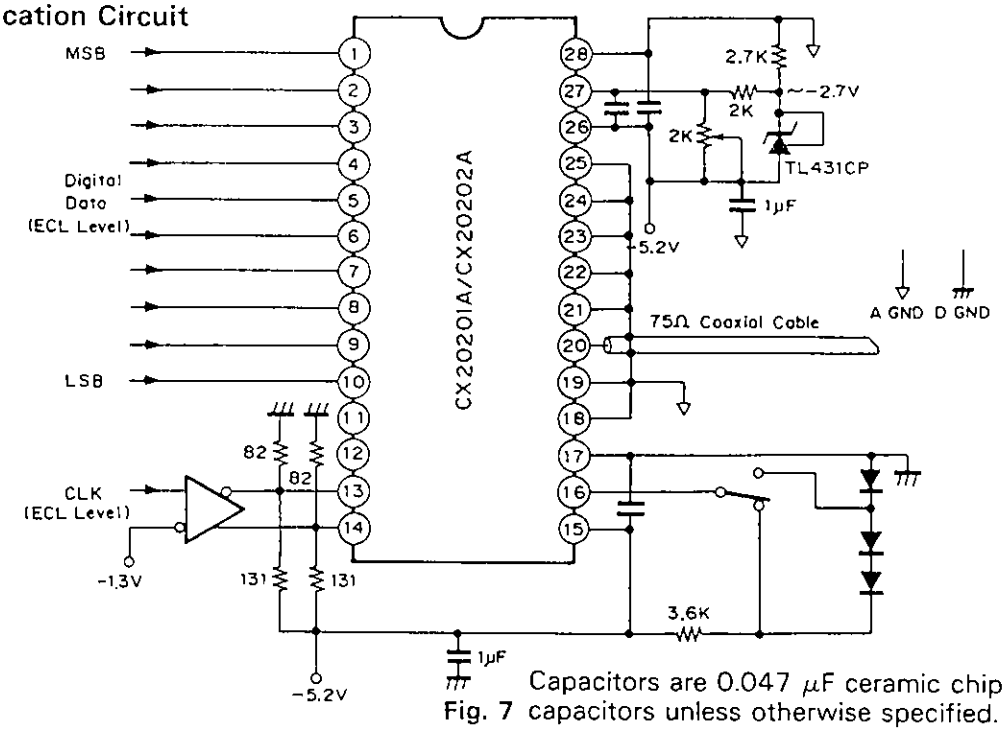



Fig. 7 Capacitors are 0.047 μF ceramic chip capacitors unless otherwise specified.

## Notes on Applications

(1) Setting of full-scale output voltage

The full-scale output voltage ($V_{O(FS)}$) is set by the pin 27 ($V_{REF}$). $V_{O(FS)}$ varies in proportion to the voltage difference between pin 27 and pin 26 ($AV_{EE}$) as shown in Fig. 9.

$V_{O(FS)}$ can be set by simply dividing the supply voltage using resistors as shown in Fig. 8, but in this simple set up the voltage deviation of the supply voltage result in a deviation of $V_{O(FS)}$. This influence can be avoided by using a stabilization circuit as shown in Fig. 7 to allow stable full-scale output.

Pin 27 ($V_{REF}$) should be stabilized against high-frequency noise by sufficient by passing using a capacitor with low lead inductance such as ceramic chip capacitors. The stabilization capacitor should be inserted between pin 27 ($V_{REF}$) and pin 26 ($AV_{EE}$) as $V_{O(FS)}$ is direct proportion to the voltage across these two terminals.

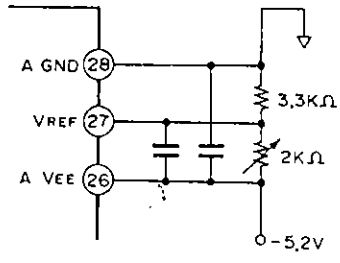



Fig. 8

(2) Noise reduction

An external digital noise should be minimized because the system handles small analog voltage (1 LSB corresponds 1 mV of analog output voltage for 10 bit resolution). Refer to the following notes to minimize the system noise contamination.

- Ground plane and $V_{EE}$ plane on a printed circuit board should be made as wide as possible to reduce parasitic inductance and resistance.
- The patterns AGND and DGND should be separated on the printed circuit board. $AV_{EE}$ and $DV_{EE}$ should be separated too. The connections between analog system and digital system are to be made at the I/O ports of the printed circuit board.
- $AV_{EE}$ and $DV_{EE}$ should be bypassed to respective GND by using a tantalum capacitor of 1 $\mu$F and a ceramic chip capacitor of 47$\mu$F positioned as close as to terminals of the IC.
- Pins not in sure are to be connected to the ground plane.

(3) Load resistance and temperature coefficient

Temperature coefficient of the full-scale output voltage and zero offset voltage depend on the load resistance (value and type). Generally, the larger the load resistance the better the temperature coefficient value. Temperature characteristics at $R_L \geqq 10\ k\Omega$ and $R_L = 75\ \Omega$ are shown in Fig. 10.

(4) Input data and internal latching circuit

CX20201A/CX20202A incorporates a latching circuit as shown in the block diagram. This latching circuit has a two-stage configuration (master-slave type) and fetches input data only at the rising edge of the clock; the output is not affected by the changes in input data at any other timings. This mechanism allows stable operation against any changes in input data at any timings, except for the set-up time immediately before and the hold time immediately after the clock change from L to H.

(5) Driving input data and clock

CX20201A/CX20202A are designed to be operated at very high speed. It is, therefore, necessary to drive it with a high-speed ICs such as an ECL100K for full performance. Also the output port of the data and clock drivers should be terminated with 50-$\Omega$ systems. See Figs. 4 and 7.

$V_{O(FS)}$ Ratio vs. ($V_{REF}$-$V_{EE}$)

Ta = 25°C, $V_{EE}$ = −5.2V

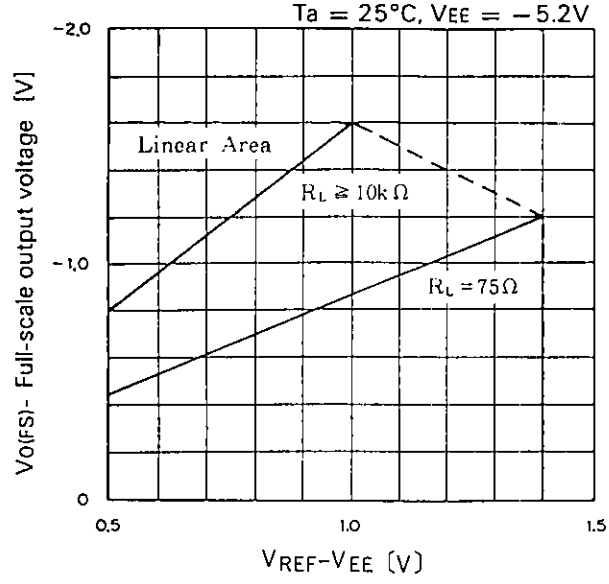



Fig. 9

Full-scale Output Voltage vs. Ambient Temperature

(typ.)

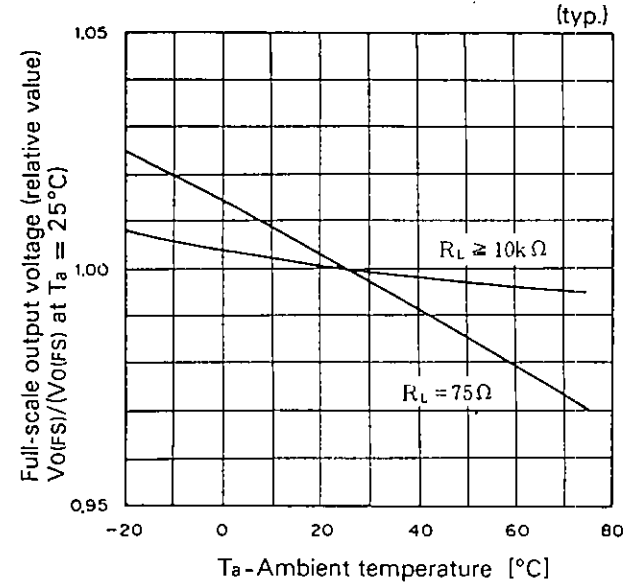



Fig. 10

Outbut Characteristics vs. Multiplying Input Signal Frequency

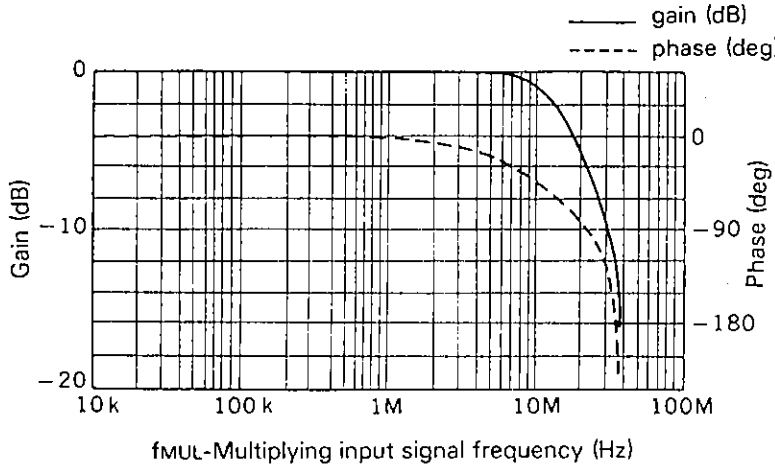



Fig. 11

Glitch Energy vs. Case Temperature (Full Scale−1023mV)

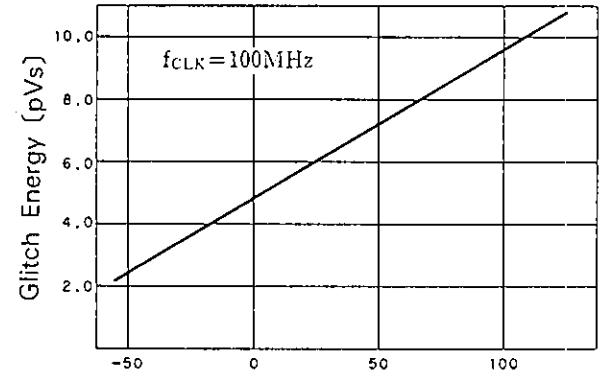
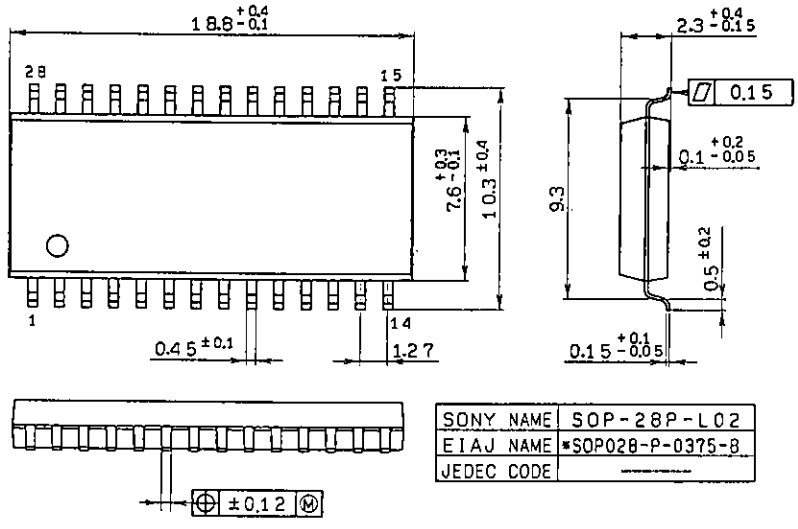


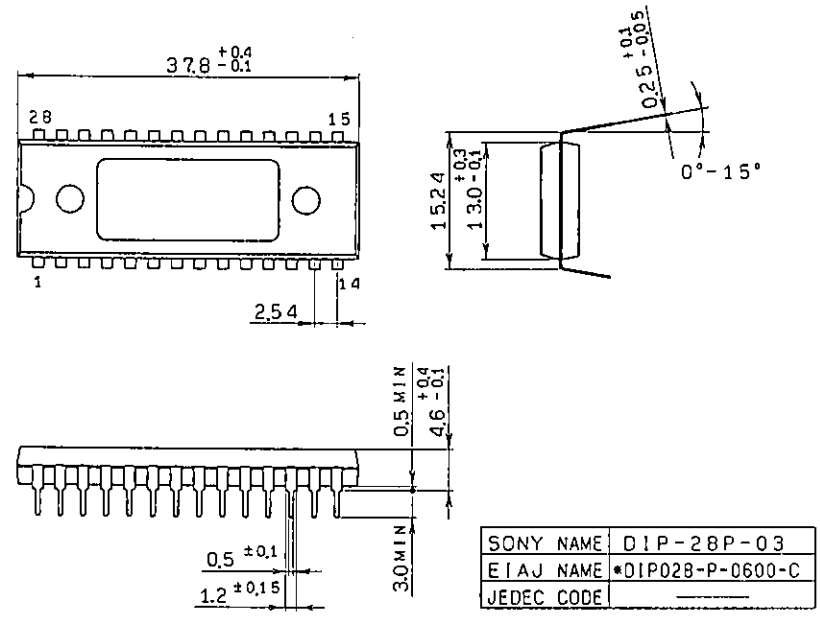

Fig. 12

## Package Outline Unit : mm

CX20201A 28pin SOP(Plastic) 375mil 0.6g




CX20202A 28pin DIP(Plastic) 600mil 4.2g



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