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SONY

CCD B/W VIDEO CAMERA MODULE

XC-77/77CE

JUNCTION BOX
JB-77

STANDARD LENS
VCL-16Y-M

TRIPOD ATTACHMENT
VCT-37

4-PIN M CONNECTOR
PC-XC04

12-PIN F CONNECTOR
PC-XC12

CAMERA CABLE
CCXC-12P02/12P05
CCXC-12P10/12P25



SERVICE MANUAL XCM-77/77CE

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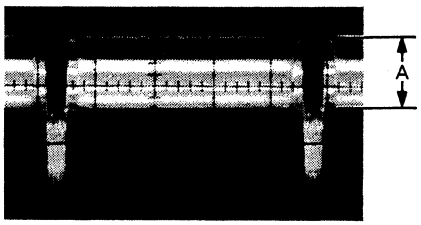
Step 2: Coupling noise elimination adjustment

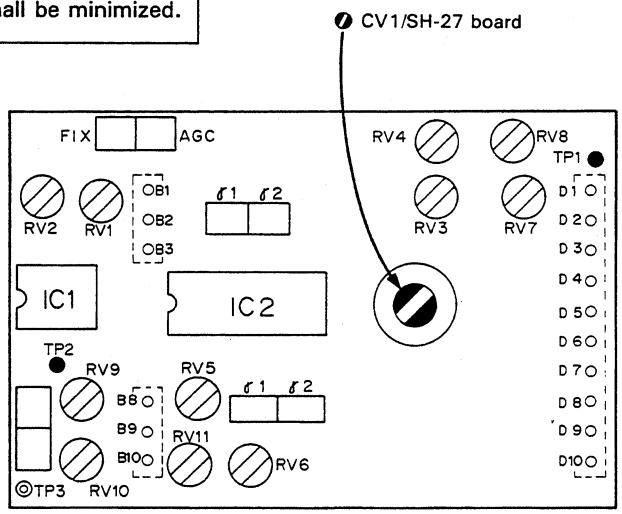
• Setting

Lens iris Measuring instrument	Close it with the lens cap Oscilloscope	Trigger	TP4(HD)/MB-136 board

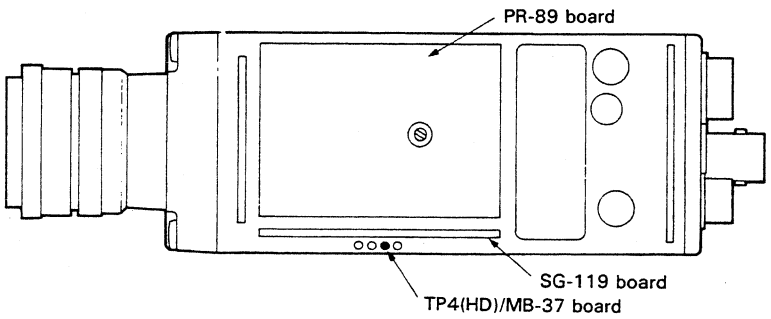
• Adjustment procedure

Test Point/PR-89 board	Adj. Point	Spec.
TP2(GND:TPI)	◐CV1/SH-27 board	A shall be minimized.





PR-89 BOARD (Component Side)



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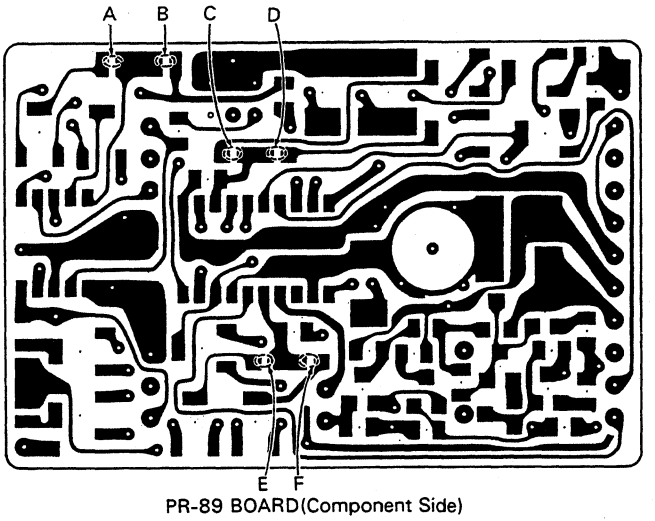
Step 3: SET UP adjustment

• Setting

Lens iris	Close it with the lens cap	Measuring instrument	Waveform monitor (WFM)

• Preparation

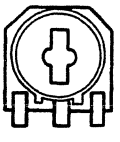
1. Solder parts A, D, and F, and remove the solder from parts B, C, and E.



PR-89 BOARD(Component Side)

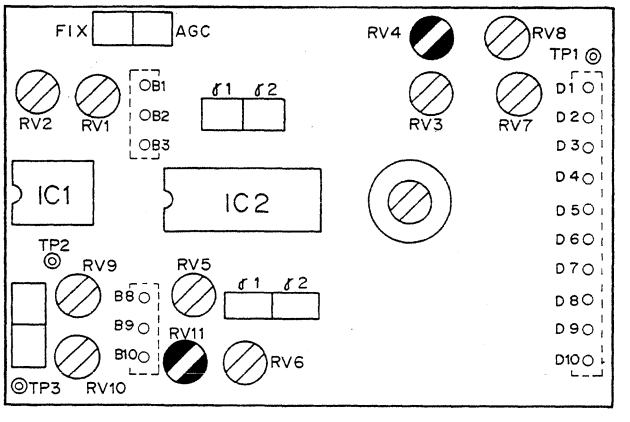
2. Set ◐RV4, ◐RV11/PR-89 on the PR-89 board to the mechanical center.

[Front view]



[Top view]





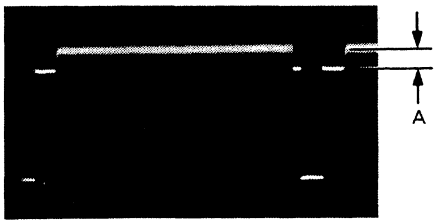
PR-89 BOARD (Component Side)

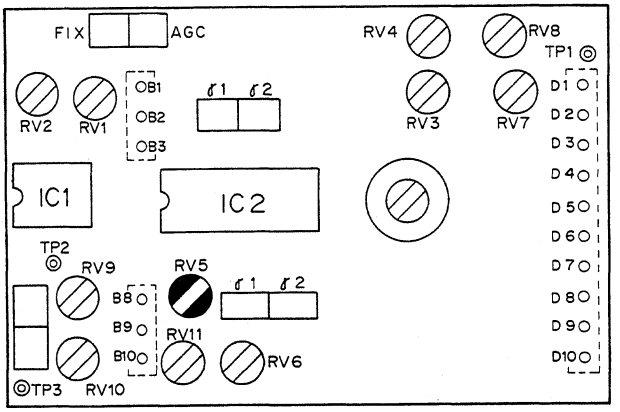
(Continued to next page)

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• Adjustment procedure

Test Point	Adj. Point	Spec.
VIDEO OUT terminal	◐RV5/PR-89 board	A = 8.0 ± 0.5 IRE





PR-89 BOARD (Component Side)

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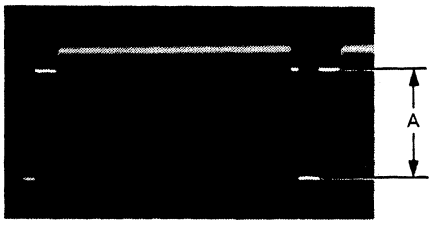
Step 4: SYNC adjustment

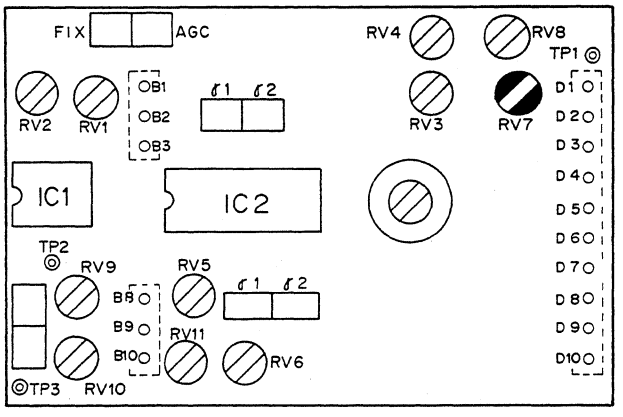
• Setting

Measuring instrument	Waveform monitor (WFM)

• Adjustment procedure

Test Point	Adj. Point	Spec.
VIDEO OUT terminal	◐RV7/PR-89 board	A = 40 ± 10 IRE





PR-89 BOARD (Component Side)

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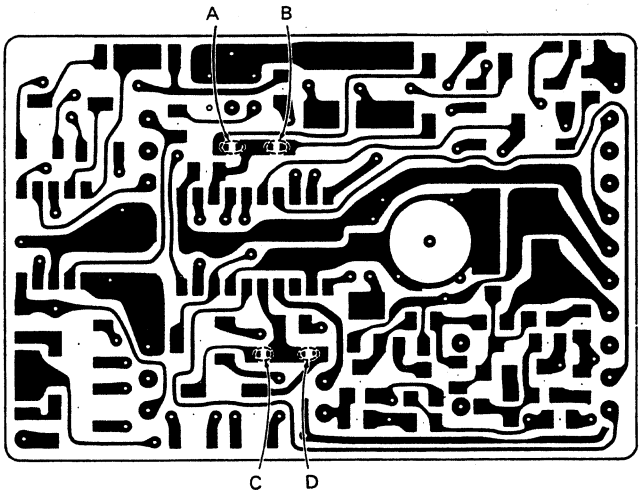
Step 5: GAIN adjustment

• Setting

Object	Grayscale chart	Measuring instrument	Oscilloscope and wave-form monitor

• Preparation

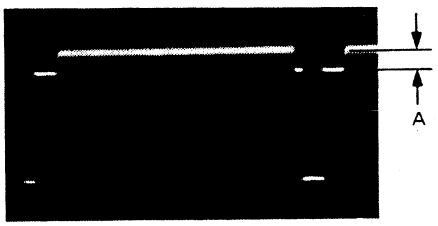
1. Solder parts A and C and remove the solder from parts B and D as shown in the figure.

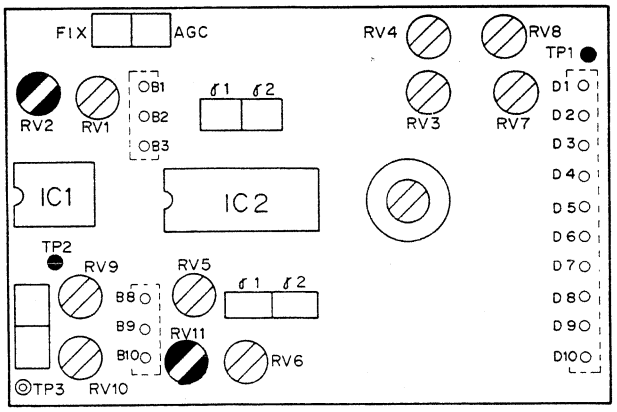


PR-89 BOARD(Component Side)

• Adjustment procedure

1. Lens iris ⇨ Close it with the lens cap
2. Test point: VIDEO OUT terminal
   Adj. Point: ◐RV11/PR89 board
   Spec.: A = 7.0 ± 0.5 IRE

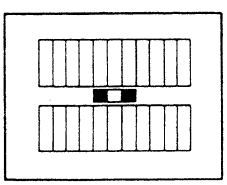




PR-89 BOARD (Component Side)

3. Shoot the grayscale chart, and place the camera so that the chart frame touches the underscanned picture frame on the monitor screen.

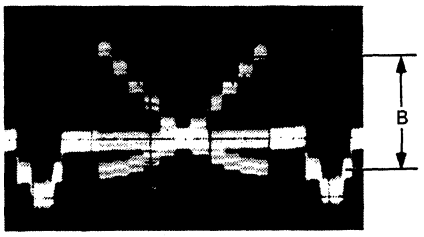
Monitor screen

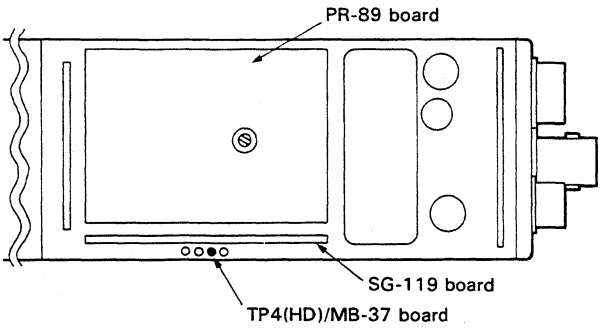


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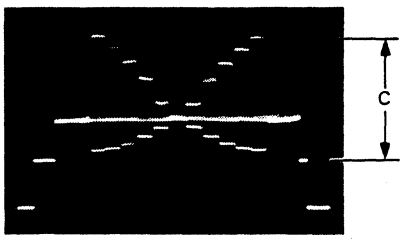
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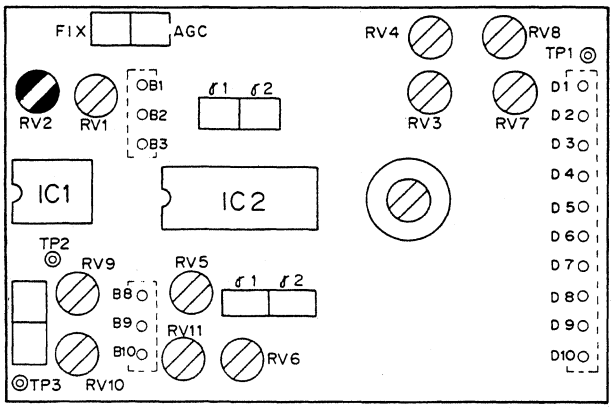
4. Test Point: TP2 (GND:TP1)/PR-89 board
   Trigger: TP4(HD)/MB-136 board
   Adj point: Lens iris
   Spec.: B = 350 ± 10 mV





5. Test/Point: VIDEO OUT terminal
   Adj. Point: RV2/PR-89 board
   Spec.: C = 100 ± 5 IRE





PR-89 BOARD (Component Side)

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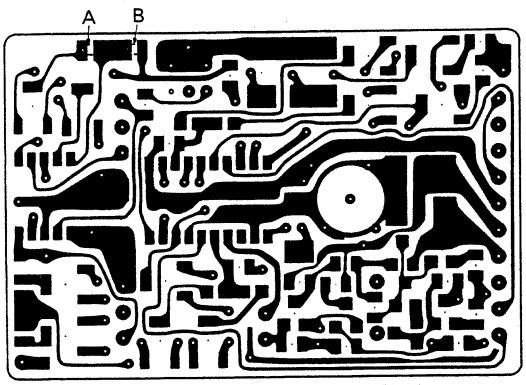
Step 6: AGC adjustment

• Setting

Object	Grayscale chart	Measuring instrument	Oscilloscope and wave-form monitor

• Preparation

Solder part B and remove the solder from part A as shown in the figure.

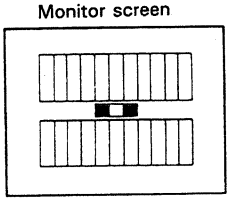


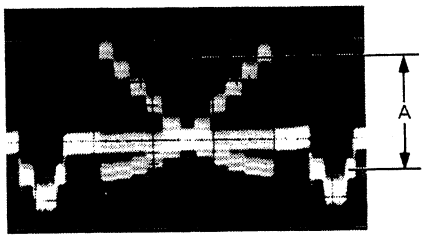
PR-89 BOARD(Component Side)

• Adjustment procedure

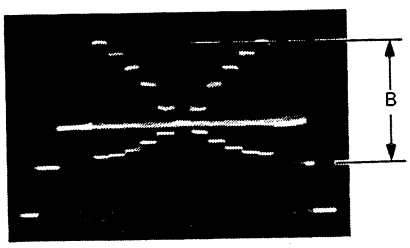
1. Shoot the grayscale chart, and place the camera so that the picture frame of the chart touches the underscanned picture frame on the monitor screen.
2. Test Point: TP2 (GND:TP1)/PR-89 board
   Trigger: TP4(HD)/MB-136 board
   Adj. Point: Lens iris
   Spec.: A = 350 ± 10 mV

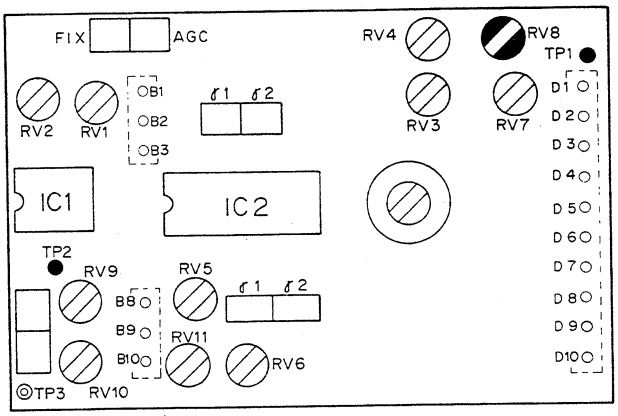
Monitor screen





3. Test Point: VIDEO OUT terminal
   Adj. Point: ◐RV8/PR-89 board
   Spec.: B = 100 ± 5 IRE





PR-89 BOARD (Component Side)

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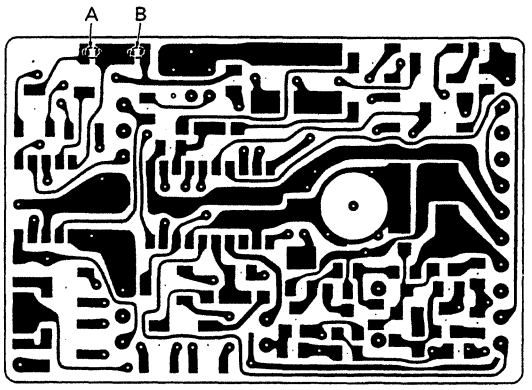
Step 7: White clip adjustment 1

• Setting

Object	Grayscale chart	Measuring instrument	Waveform monitor (WFM)

• Preparation

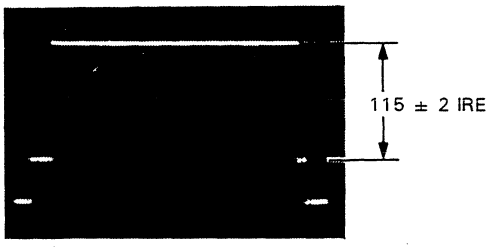
Solder part A and remove the solder from part B as shown in the figure.

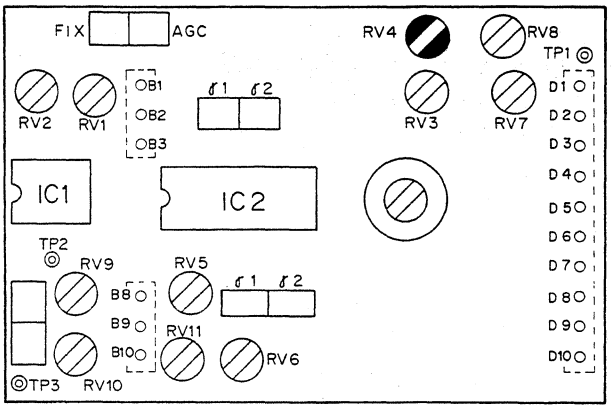


PR-89 BOARD(Component Side)

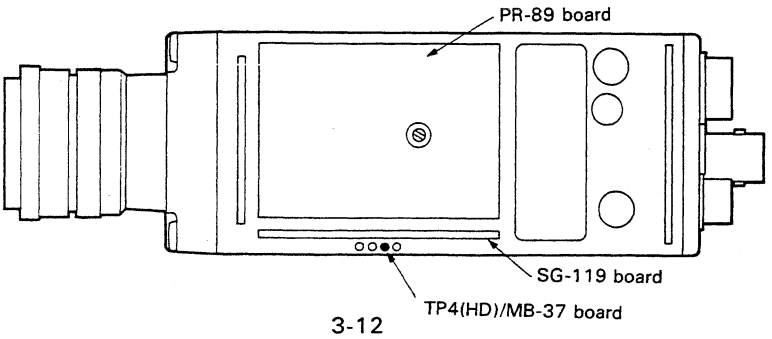
• Adjustment procedure

1. Shoot the grayscale chart, and place the camera so that the picture frame of the camera touches the underscanned picture frame on the monitor screen.
2. Test Point: VIDEO OUT terminal
   Adj. Point: ◐RV4/PR-89 board
   Adjustment: Open the lens iris, and adjust so that the VIDEO OUT waveform clips at 115 ± 2 IRE.





PR-89 BOARD (Component Side)



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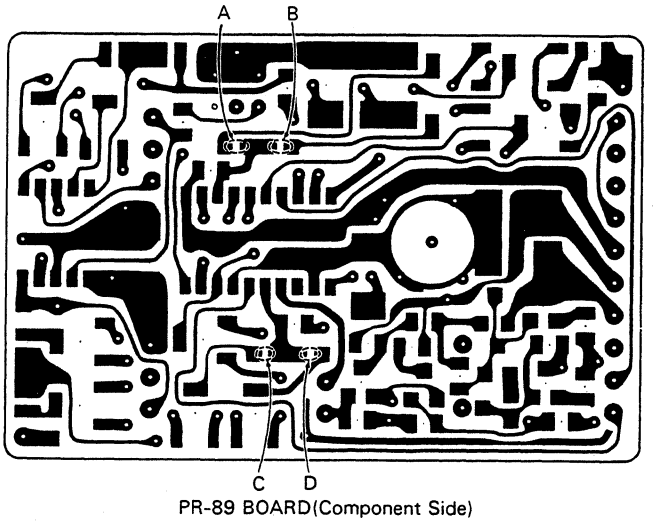
Step 8: Gamma adjustment

• Setting

Object	Grayscale chart	Measuring instrument	Oscilloscope and wave-form monitor

• Preparation

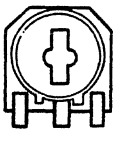
1. Solder parts B and D and remove the solder from parts A and C as shown in the figure.



PR-89 BOARD(Component Side)

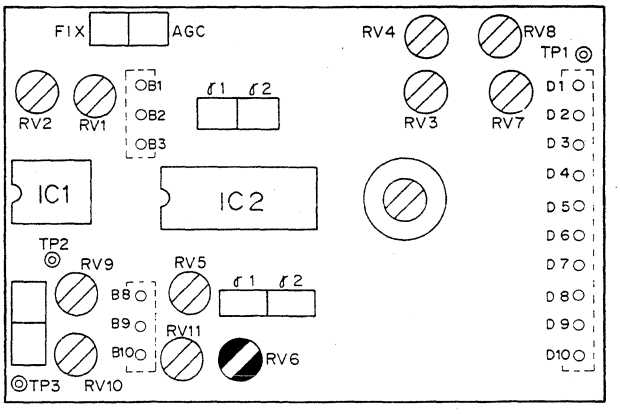
2. Set ◐RV6/PR-89 on the PR-89 board to the mechanical center.

[Front view]



[Top view]





PR-89 BOARD (Component Side)

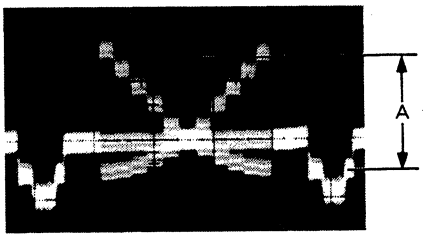
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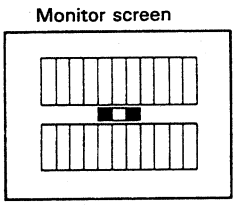
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• Adjustment procedure

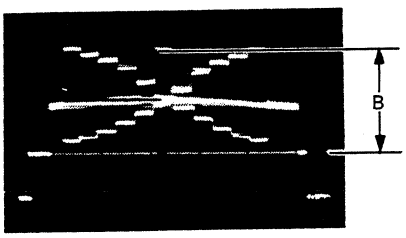
1. Shoot the grayscale chart, and place the camera so that the chart frame touches the underscanned picture frame on the monitor screen.

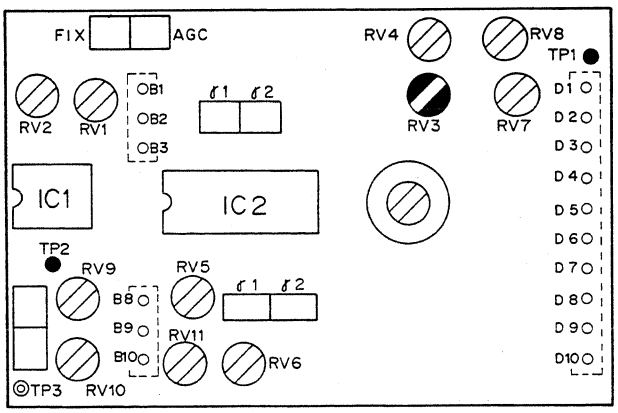
Test Point/PR-89 board	Adj. Point	Spec.
TP2(GND:TPI)	Lens iris	A = 350 ± 10mV





Test Point	Adj. Point	Spec.
VIDEO OUT terminal	◐RV3/PR-89 board	B = 100 ± 5 IRE





PR-89 BOARD (Component Side)

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Step 9: White clip adjustment 2

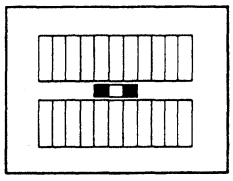
• Setting

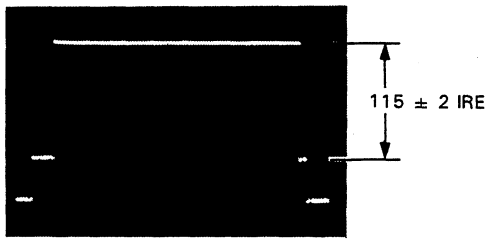
Object	Grayscale chart	Measuring instrument	Waveform monitor (WFM)

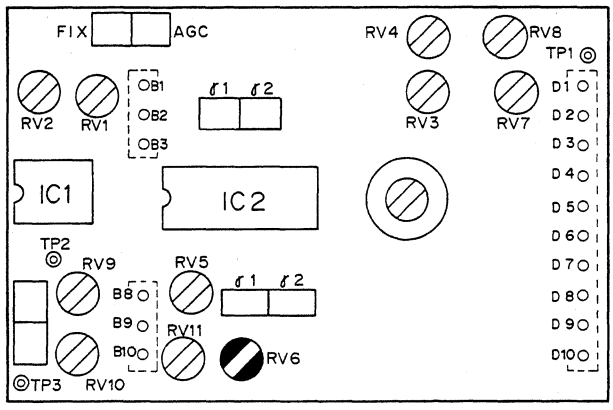
• Adjustment procedure

1. Shoot the grayscale chart, and place the camera so that the chart frame touches the underscanned picture frame on the monitor screen.
2. Test Point: VIDEO OUT terminal
   Adj. Point: ◐ RV6/PR-89 board
   Adjustment: Open the lens iris and adjust so that the VIDEO OUT waveform clips at 115 ± 2 IRE .

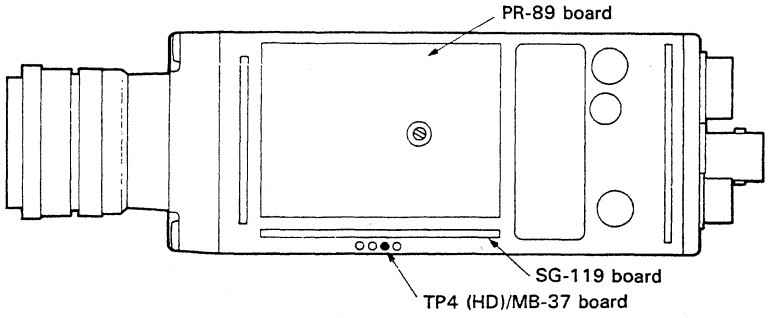
Monitor screen







PR-89 BOARD (Component Side)



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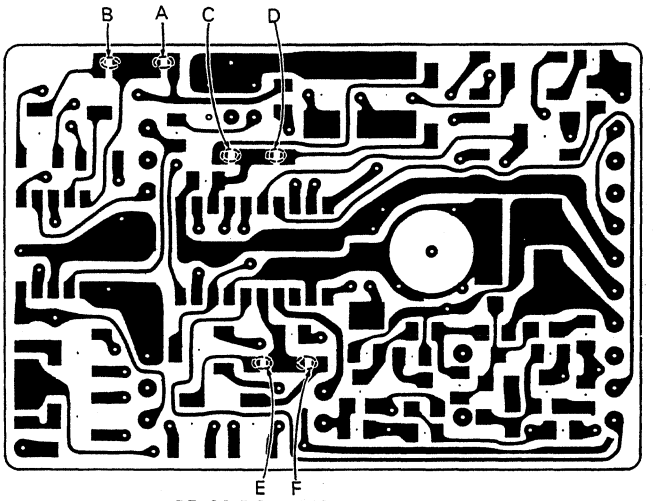
Step 10: GAIN LIMIT adjustment

• Setting

Object	White window chart	Measuring instrument	Oscilloscope and wave-form monitor

• Preparation

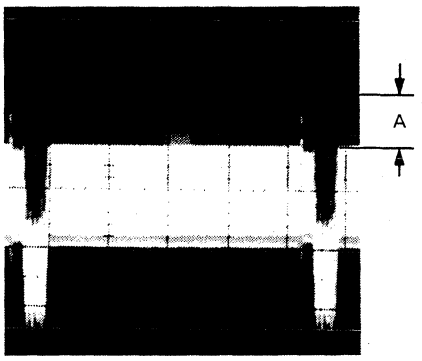
1. Solder parts A, C and E and remove the solder from parts B, D, and F as shown in the figure.



PR-89 BOARD(Component Side)

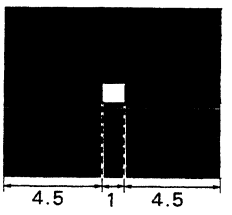
• Adjustment procedure

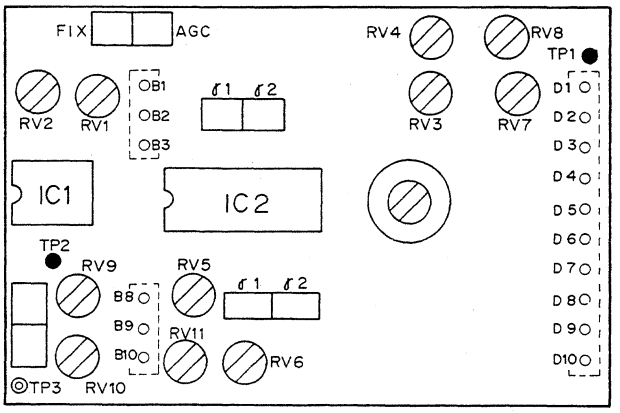
1. Shoot the white window chart as shown in the figure at right.
2. Test Point: TP2 (GND:TP1)/PR-89 board
   Trigger: TP4(HD)/MB-136 board
   Adj. Point: Lens iris
   Spec.: A = 50 ± 10 mV



If the specification cannot be satisfied:
- When the pattern box is PTB-100:
  Adjust the luminance control on the pattern box so that the specification is satisfied.
- When the pattern box is PTB-500:
  Put an ND-4 filter that meets the specification of the lens over the lens, and make readjustment.
- When a 100-W bulb is used:
  Adjust the variable voltage transformer so that the specification is satisfied.

Monitor screen

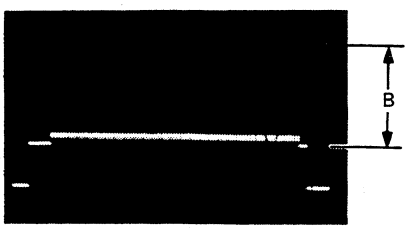


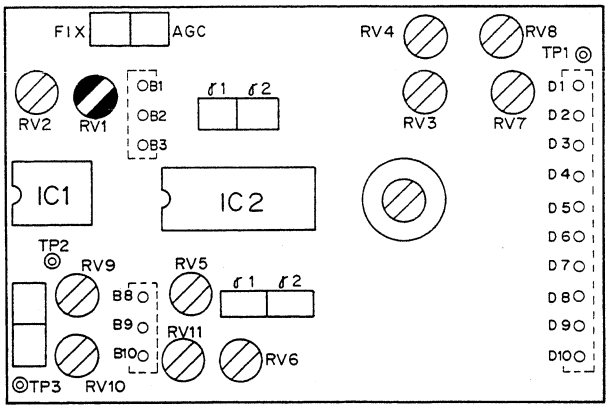


PR-89 BOARD (Component Side)

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3. Test/Point: VIDEO OUT terminal
   Adj. Point: ◐RV1/PR-89 board
   Spec.: B = 100 ± 10 IRE





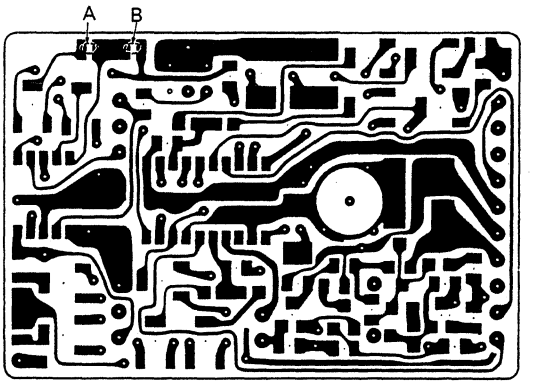
PR-89 BOARD (Component Side)

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Step 11: Setting after adjustment

- Setting

Solder part A and remove the solder from part B as shown in the figure.



PR-89 BOARD(Component Side)

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TABLE OF CONTENTS

1. OPERATION ..... 1-1 (E)

1-1. Features ..... 1-1 (E)
1-2. Composition ..... 1-2 (E)
1-3. Parts location, function and operation ..... 1-3 (E)
1-3-1. XC-77/77CE CCD video camera module ... 1-3 (E)
1-3-2. VCT-37 tripod attachment ..... 1-5 (E)
1-3-3. JB-77 junction box ..... 1-6 (E)
1-4. Connections ..... 1-8 (E)
1-4-1. When junction box is used ..... 1-8 (E)
1-4-2. When junction box is not used ..... 1-9 (E)
1-5. Initialization of the mode ..... 1-10 (E)
1-6. Precautions ..... 1-10 (E)
1-7. Special characteristics of a CCD ..... 1-11 (E)

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2. COMPREHENSIVE SPECIFICATIONS (XC-77)

2-1. SPECIFICATIONS 2-1
2-2. CONNECTOR'S PIN FUNCTION 2-6
2-3. OUTPUT SIGNAL TIMING CHART 2-7
2-4. External Synchronization 2-8
2-4-1. VS/VBS mode 2-8
2-4-2. HD and VD mode 2-8
2-4-3. RESTART mode 2-15
2-5. MODE SETTING 2-16
2-6. THEORY OF OPERATION 2-18

3. ALIGNMENT (XC-77)

3-1. PREPARATION 3-1
Step 1: Jigs and measuring instruments 3-1
Step 2: Connection diagram 3-2
3-2. OVERALL ADJUSTMENT 3-4
Step 1: V SUB (field) adjustment 3-4
Step 2: V SUB (frame) adjustment 3-5
Step 3: Coupling noise elimination adjustment 3-6
Step 4: SET UP adjustment 3-7
Step 5: SYNC adjustment 3-9
Step 6: GAIN adjustment 3-10
Step 7: AGC adjustment 3-12
Step 8: White clip adjustment 1 3-13
Step 9: Gamma adjustment 3-14
Step 10: White clip adjustment 2 3-16
Step 11: GAIN LIMIT adjustment 3-17
Step 12: Setting after adjustment 3-19

2. COMPREHENSIVE SPECIFICATIONS (XC-77CE)

2-1. SPECIFICATIONS 2-1
2-2. CONNECTOR'S PIN FUNCTION 2-6
2-3. OUTPUT SIGNAL TIMING CHART 2-7
2-4. External Synchronization 2-8
2-4-1. VS/VBS mode 2-8
2-4-2. HD and VD mode 2-8
2-4-3. RESTART mode 2-15
2-5. MODE SETTING 2-16
2-6. THEORY OF OPERATION 2-18

3. ALIGNMENT (XC-77CE)

3-1. PREPARATION 3-1
Step 1: Jigs and measuring instruments 3-1
Step 2: Connection diagram 3-2
3-2. OVERALL ADJUSTMENT 3-4
Step 1: V SUB (field) adjustment 3-4
Step 2: Coupling noise elimination adjustment 3-5
Step 3: PEDESTAL adjustment 3-6
Step 4: SYNC adjustment 3-8
Step 5: GAIN adjustment 3-9
Step 6: AGC adjustment 3-11
Step 7: White clip adjustment 1 3-12
Step 8: Gamma adjustment 3-13
Step 9: White clip adjustment 2 3-15
Step 10: GAIN LIMIT adjustment 3-16
Step 11: Setting after adjustment 3-18

A. DIAGRAM

A-1. BLOCK DIAGRAM A-1
A-2. MOUNTING DIAGRAM A-4
A-3. SCHEMATIC DIAGRAM A-7

B. SEMICONDUCTOR

C. SPARE PARTS

C-1. PARTS INFORMATION C-1
C-2. ELECTRICAL PARTS C-2
C-3. EXPLODED VIEW SCREW C-9

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SECTION 1
OPERATION

1-1. FEATURES

The XC-77/77CE is a monochrome video camera module which uses a solid state image sensor — the CCD (Charge Coupled Device).

High quality image
High quality, fine image is made possible by a large number of picture elements, as much as 768x493 for XC-77 and 753x581 for XC-77CE.
The XC-77CE's picture elements are equally arrayed in vertical and horizontal directions, and allow easy addressing. This makes XC-77CE most suitable for image processing systems which require highly accurate addressing.

Adaptability to diversified signal processing
Gain can be internally selected either the AGC (Automatic Gain Control) or Fixed, and the γ (gamma) can be set either to the compensation mode or to the fixed (1) mode.
The accumulation mode of the electrical charge can be internally changed from the frame accumulation to the field accumulation. This enables the non-interlace mode sensitivity to be elevated up to the equivalent level to the sensitivity of the interlace mode by entering signals into the external sync input for the setting of the non-interlace mode.

Three types of external sync signals
Synchronization with other cameras is possible by entering the three types of signals from the external sync signal generator. The capture range is set as wide as ±1% of the horizontal frequency.

HD, VD signals: external synchronization is applied in accordance with the system, either the interlace or non-interlace system, which is automatically identified by the HD, VD signals.

VBS (Video, Burst, Sync) signal: the camera module is synchronized with the VBS signal (BB signal or composite sync signal.) (The sync system, whether by HD/VD signal or VBS signal, is automatically selected depending on the input signal.)

Reset pulse: this is used to set the timing for the read-out of register contents at an arbitrary moment.

Internal sync signal output
Clock signals are constantly output. HD signal and field index signal can be output to the 12P connector by altering the internal wiring.

Solid body
The body consists of aluminum diecast and steel sheet. On the bottom are 2 screw holes (reference holes) which can be used to keep deviation of the optical axis at a minimum.

Compatibility with XC-37 series
XC-77/77CE has common types of VIDEO OUT connector and 12-pin multi-connector pin assignment with the XC-37 series, as well as having identical cross section external dimensions, and can replace the XC-37 series camera module.

Long life and high stability

Precise image geometry

Low lag and little image sticking

High resistance to vibration and mechanical shock

Quick start-up

Shooting in a strong magnetic field

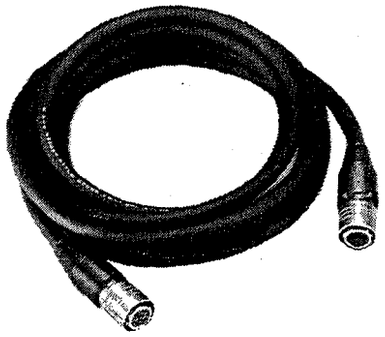
Low power consumption (2.2W)

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1-2. COMPOSITION

The CCD video camera module system consists of the following optional products which can be purchased separately.

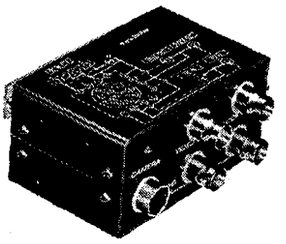
Camera cables
CCXC-12P02 (2m)
CCXC-12P05 (5m)
CCXC-12P10 (10m)
CCXC-12P25 (25m)



XC-77/77CE CCD video camera module



JB-77 junction box



VCL-16Y-M standard lens



PC-XC12 12-pin connector





PC-XC04 4-pin connector

VCT-37 tripod attachment



XC-77/77CE CCD video camera module

VCL-16Y-M standard lens
This is a standard lens of f = 16 mm, F1.4. The iris and focus are adjusted manually.

JB-77 Junction box
This is attached to the camera module using the CCXC-12P02/12P05/12P10/12P25 camera cable and will supply power, transmit video signals, and exchange external sync signals.

PC-XC04 4-pin connector
This is used to attach the lens cord of the auto iris lens to the LENS connector on the XC-77/77CE video camera module.

PC-XC12 12-pin connector
This connector is prepared for system-up, and used to connect to the DC IN/SYNC connector of the camera module.

VCT-37 tripod attachment
To attach the video camera module to a tripod, use this tripod attachment.

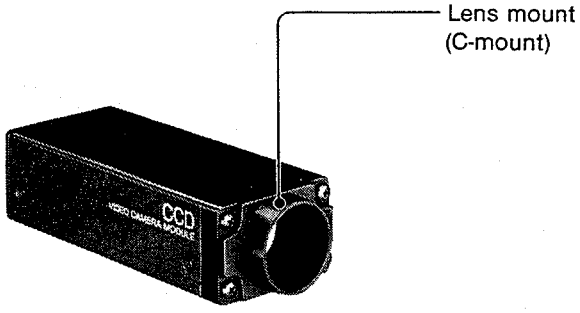
CCXC-12P02 (2m), 12P05 (5m), 12P10 (10m) and 12P25 (25m) camera cables
These cables can be attached to the 12-pin DC IN/SYNC connector on the rear of the camera module to supply power, transmit video signals and exchange sync signals.

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1-3. PARTS LOCATION, FUNCTION AND OPERATION

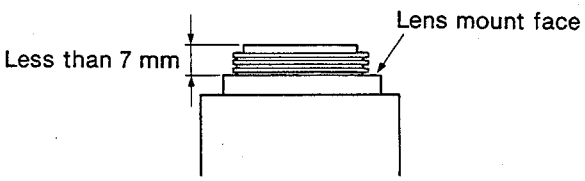
1-3-1. XC-77/77CE CCD VIDEO CAMERA MODULE

Front

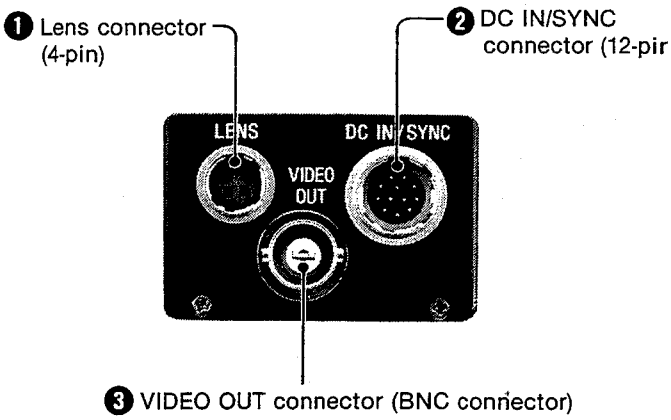


Lens mount (C-mount)
Attach a C-mount lens, such as the VCL-16Y-M standard lens, or a piece of optical equipment.

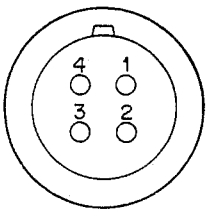
Note
Projection of the lens or other piece of optical equipment must be less than 7 mm from the lens mount.



Rear



❶ LENS connector (4-pin)
When the plug of an auto iris lens is connected to this connector, the iris of the lens can automatically be adjusted.
The pin configuration of this connector is shown in the diagram below.

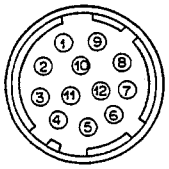


Pin No.	Signal
1	+12 V
2	Ground
3	–
4	Video signal

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❷ DC IN/SYNC (DC power input/sync) connector (12-pin)
Connect a CCXC-12P02, CCXC-12P05, CCXC-12P10 or CCXC-12P25 camera cable to this connector to supply power (12 V DC) from an external power source and output the video signal from the video camera module. When a sync signal generator is connected to supply the sync signal (VBS, VS, BS or HD/VD), the camera module can be operated on external sync signals.

The pin configuration of this connector is shown in the diagram below.



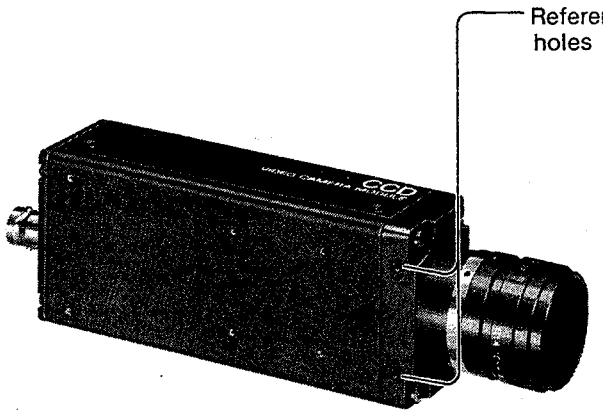
Signal Pin No.	External Sync mode			Camera Sync output
	HD, VD	VBS/VS	RESTART RESET	
1	Ground	Ground	Ground	Ground
2	+12 V	+12 V	+12 V	+12 V
3	Video output (ground)	Video output (ground)	Video output (ground)	Video output (ground)
4	Video output (signal)	Video output (signal)	Video output (signal)	Video output (signal)
5	HD input (ground)	—	HD input (ground)	HD output (ground)
6	HD input (signal)	—	HD input (signal)	HD output* (signal)
7	VD input (signal)	VBS input (signal)	RESET PULSE (signal)	FIELD INDEX* output (signal)
8	—	—	—	CLOCK output (ground)
9	—	—	—	CLOCK output (signal)
10	Ground	Ground)	—	Ground
11	+12 V	+12 V	—	+12 V
12	VD input (ground)	VBS input (ground)	RESET PULSE (ground)	FIELD INDEX output (ground)

*It is necessary to modify connections of the circuits in side the camera in order to output the HD and FIELD INDEX signals.

❸ VIDEO OUT (output) connector (BNC connector)
The video signal from the video camera module is output from this connector. This connector can be used only when a CCXC-12P02 camera cable is connected to the DC IN/SYNC connector and the video output of the 12-pin connector of the CCXC-12P02 cable is not terminated with 75 ohms.

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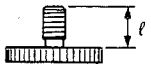
Bottom



Reference holes
These are screw holes cut with high precision to affix the camera module. Affixing the module according to these reference holes keeps deviation of the optical axis at a minimum.
For details on dimensions, refer to the service manual.

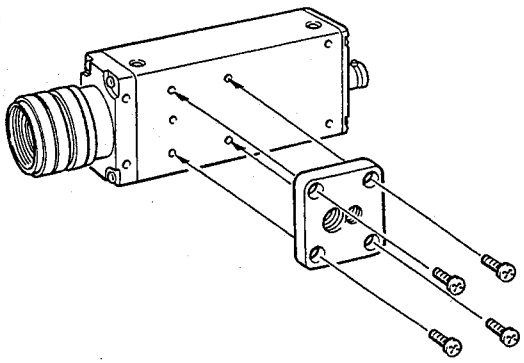
1-3-2. VCT-37 TRIPOD ATTACHMENT

The screws must also be in accordance with the following specifications.
ISO standard: ℓ = 4.5 mm±0.2 mm
ASA standard: ℓ = 0.197 inches



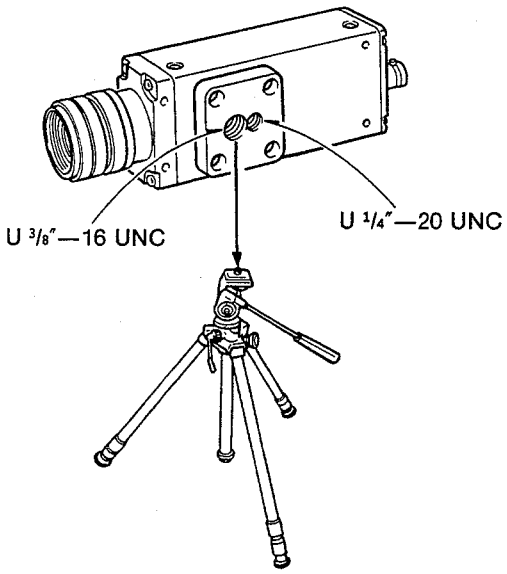
How to attach the tripod attachment to the video camera module.

1



Screws (M2 x 4)

2

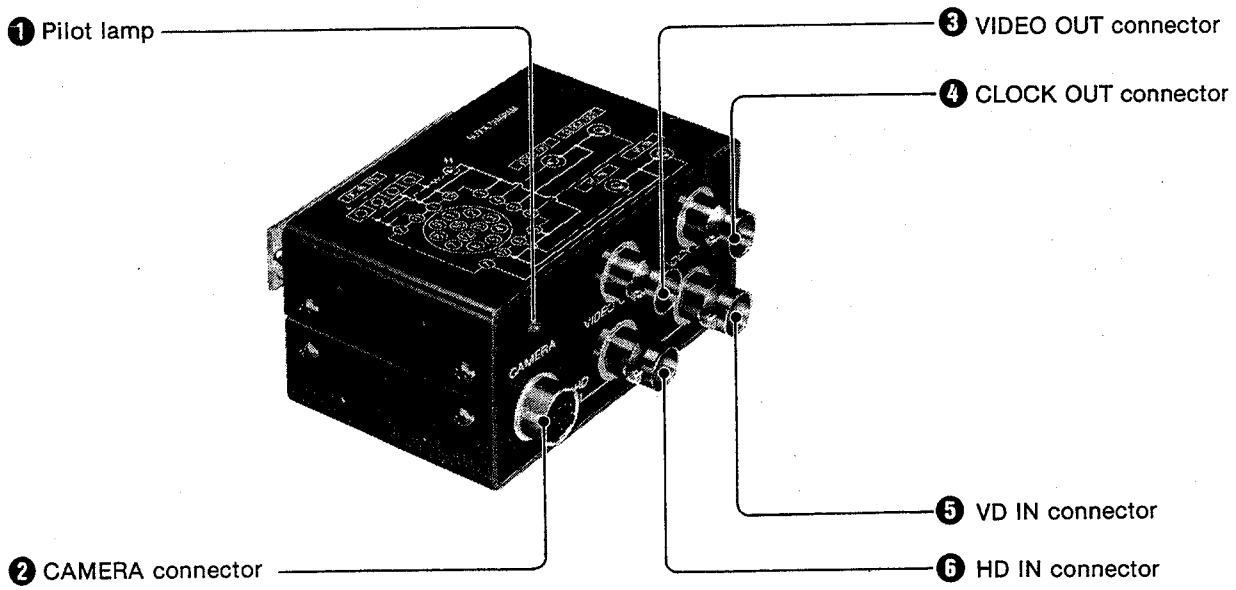


Caution
Use screws which are less than 4 mm (3/16 inches) long to attach the tripod attachment. If the screw being used is too long, the circuit boards inside the video camera module may be damaged.

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1-3-3. JB-77 JUNCTION BOX

Front



1 Pilot Lamp
Lights up when 12 V DC is input.

2 CAMERA connector (12-pin)
Connect a CCXC-12P02/12P05/12P10 or CCXC-12P25 camera cable to this connector to supply power (12 V DC) from an external power source and external sync signals from an external sync system and input the video signal from the video camera module.

3 VIDEO OUT (output) connector (BNC connector)
The video signal from the video camera module is output from this connector when connected to a video monitor or VTR etc.

4 CLOCK OUT (internal sync signal output) connector
Clock signal is output through this connector for the independent use of the camera module.

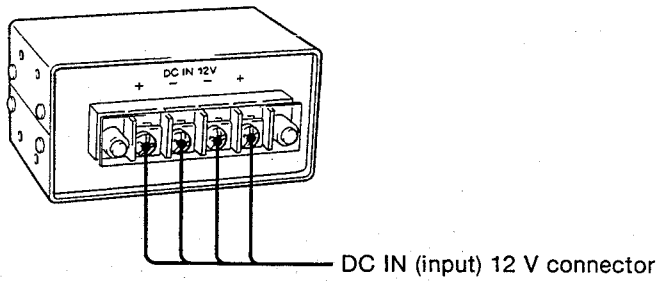
5 VD IN connector (BNC connector)
Connect the sync signal generator to input the VD signal or the VBS signal. This enables the camera module to be operated on external sync signals.
- When receiving VD signals, input HD signals to the HD connector.
- When receiving VBS signals, do not input HD signals to the HD connector.

For the independent use of the camera module, the field index signal (FLD, VD or composite sync signal) can be output by changing the camera's internal wiring.

6 HD IN connector
Connect the sync signal generator to input the HD signal. Combining it with the VD signal input from VD IN connector enables the camera module to be operated on external sync signals.
For the independent use of the camera module, the HD signal can be output by changing the camera's internal wiring.

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Rear

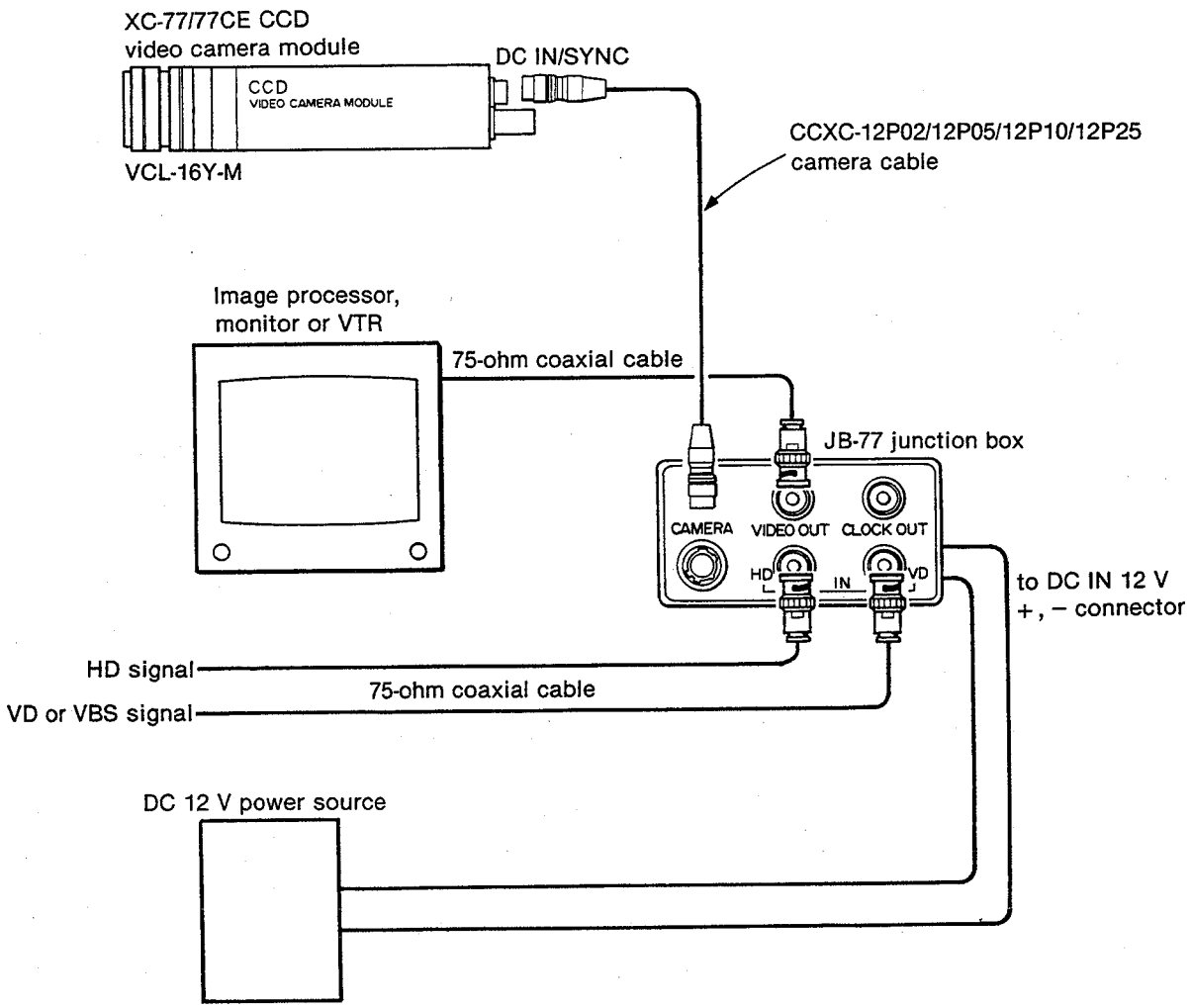


DC IN (input) 12 V connector
DC 12 V power is received through this connector. When connecting a multiple number of cameras, connect other JB-77 to the empty connectors. Power can be supplied to all JB-77 connected from an external power source.

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1-4. CONNECTIONS

1-4-1. WHEN JUNCTION BOX IS USED

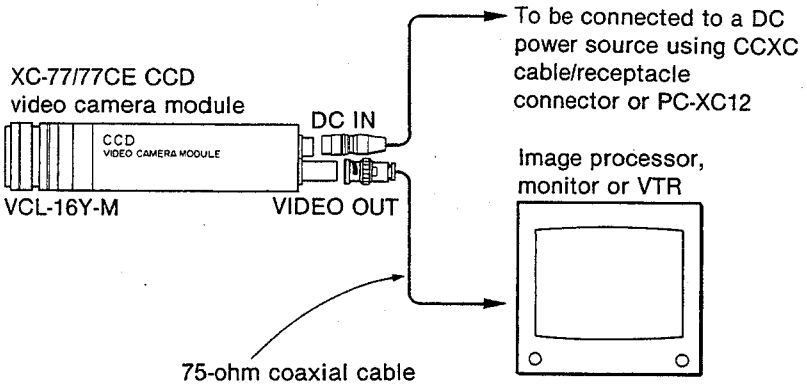


Note

When applying external sync by VBS or VB signal, the image may be affected by VBS signal during gen lock if a long type CCXC cable is used (especially CCXC-12P25). When this occurs use only BS or an S signals.

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1-4-2. WHEN JUNCTION BOX IS NOT USED



Note

- When using the VIDEO OUT connector for video signal output, use the DC IN/SYNC connector for power supply. Connect only the CCXC-12P02 cable to the DC IN/SYNC connector, and do not terminate its video output.
- When a cable longer than 5 m is connected to the DC IN/SYNC connector, video output signals cannot be obtained through the VIDEO OUT connector.

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1-5. INITIALIZATION OF THE MODE

Modes for the following 8 items can be switched. At the time of delivery, each item is set to the upper mode in the list shown below.

Item	Mode	Remarks
AGC	FIX GAIN	Gain fix
	AGC	Automatic gain control
γ	1	No γ compensation
	compensate	γ compensation
EIA/CCIR	EIA	ROM (EIA mode)
	CCIR	ROM (CCIR mode)
FRAME/ FIELD	FRAME	Frame accumulation
	FIELD	Field accumulation
FRAME	NORMAL	Normal scanning
	INVERSION	Inversion of even number field and odd number field
RESTART RESET	OFF	Frame not synchronizing
	ON	Frame synchronizing
EIA/CCIR	EIA	SG (EIA mode)
	CCIR	SG (CCIR mode)

Note
EIA/CCIR mode settings vary depending on the CCD (EIA/CCIR).

1-6. PRECAUTIONS

Power source
Operates on 12 V DC. Use a stable power source, free from ripples or noise.

Foreign objects
Do not spill any liquid, drop any inflammable or metal objects inside. This could result in fire, electrification, malfunction or accident.

Do not wrap in cloth while in operation

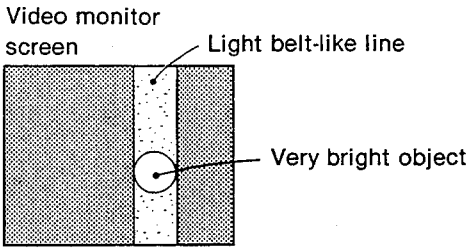
Locations for operation and storage
Avoid operating or storing in the following places.
- An extremely hot or cold location.
  Operating temperature: 0°C to 40°C (32°F to 104°F)
- A location exposed to high humidity or dust.
- A location exposed to rain.
- A location subjected to strong vibrations.
- A location near a TV or radio station which radiates high powered radio frequencies.

Care
Clean the dust on the surface of the lens and optical filter with a blower. Clean the exterior with a soft, dry cloth. If it becomes very dirty, clean with a cloth slightly moistened with a mild detergent solution. Do not use any type of solvent, such as alcohol or benzine, which may damage the finish.

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1-7. SPECIAL CHARACTERISTICS OF A CCD

Smear phenomenon
This phenomenon occurs when shooting a very bright object (such as electronic light, fluorescent lamp, the sun or a strong reflection).

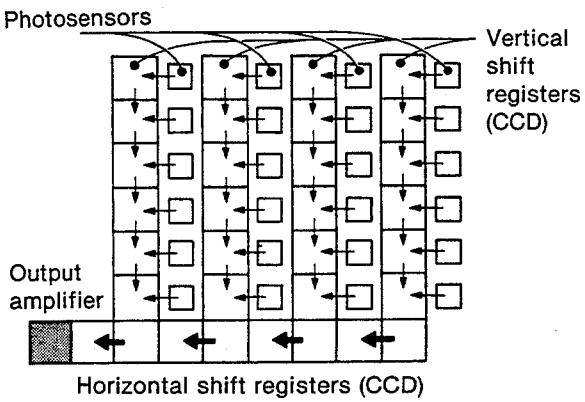


Due to the interline-transfer organization of the CCD image sensors (Refer to "The interline-transfer Organization of the CCD Image Sensors"), this phenomenon is caused by electronic charges generated beneath the photosensors by a light with a long wavelength, such as an infrared light.

False signal
When vertical stripes or straight lines are shot, they may look wavy.

Blemishes
The photosensor elements generate electronic charges which ultimately produce horizontal and vertical rows in the CCD image sensor.
Therefore, any malfunctioning photosensor element will eventually cause a blemish on the monitor screen. Consult the specifications in "Comprehensive Specifications" for details on the blemishes of the XC-77/77CE.

The interline-transfer organization of the CCD image sensors
The XC-77/77CE CCD video camera module adopts an interline-transfer organization in which precisely aligned photosensors and vertical shift registers are arrayed interlinearly and a horizontal shift resister links up with the vertical shift register, as shown. Light variations are sensed by the photosensors, which generate electronic charges proportional to the light intensity. The generated charges are fed into the vertical shift registers all at one. The charges are then transferred from the vertical shift registers to the horizontal shift registers successively and finally reach the output amplifier to be read out successively.



White micro spots
At high temperatures, numerous white spots may appear on the screen when shooting a dark object.

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SECTION 2
COMPREHENSIVE SPECIFICATIONS

2-1. SPECIFICATIONS

<CAMERA MODULE XC-77>

Pickup Device		Interline transfer CCD
Picture elements		768 (H) x 493 (V)
Sensing area		8.8 mm x 6.6 mm (the same as the 2/3-inch camera tube)
Optical black		22 pixels each horizontal line
Vertical drive frequency		15.734 kHz
Horizontal drive frequency		9.545 MHz
Signal system		EIA standard
Structure		Interline transfer
Cell size		17 μm (H) x 13 μm (V)
Chip size		10.0 mm (H) x 9.3 mm (V)
Optical System		
Lens mount		C mount
Frange back length		17.526 mm
Sync System		Internal/External autmatic change
External sync input		VBS, VS, BS (SYNC LEVEL 0.3 Vp-p ± 6 dB)
External sync frequency tolerance		± 1%
Jitter		Within ± 100 n sec
Locking time when power is on.		Within 10 sec
Scanning System		2 : 1 Interface ; 525 lines
Video Output		1.0 Vp-p sync negative, 75 ohms unbalanced.
Horizontal Resolution		380 TV lines
Vertical Effective lines		2 : 1 Interlace ; 485 lines
Sensitivity		400 Luxes with F4 (γ ON/odB)
Minimum Illumination		3 Luxes, F1.4 (without an infrared cut filter)
S/N ratio		50 dB
Power Requirement		DC 12 V
Power Voltage Tolerance		DC 10.5 V ~ 15 V
Power Consumption		2.2 W
Weight		
Camera module		190 g (XC-77)
Tripod attachment		15 g (VCT-37)
Camera cable	(2 m)	130 g (CCXC-12P02)
	(5 m)	295 g (CCXC-12P05)
	(10 m)	560 g (CCXC-12P10)
	(25 m)	1.4 Kg (CCXC-12P25)
Junction box		170 g (JB-77)
Storage Temperature		−30°C ~ +60°C
Operating Temperature		0°C ~ 40°C
Shock resistance		70 G
Storage Humidity		Within 90%
Operating Humidity		Within 70%

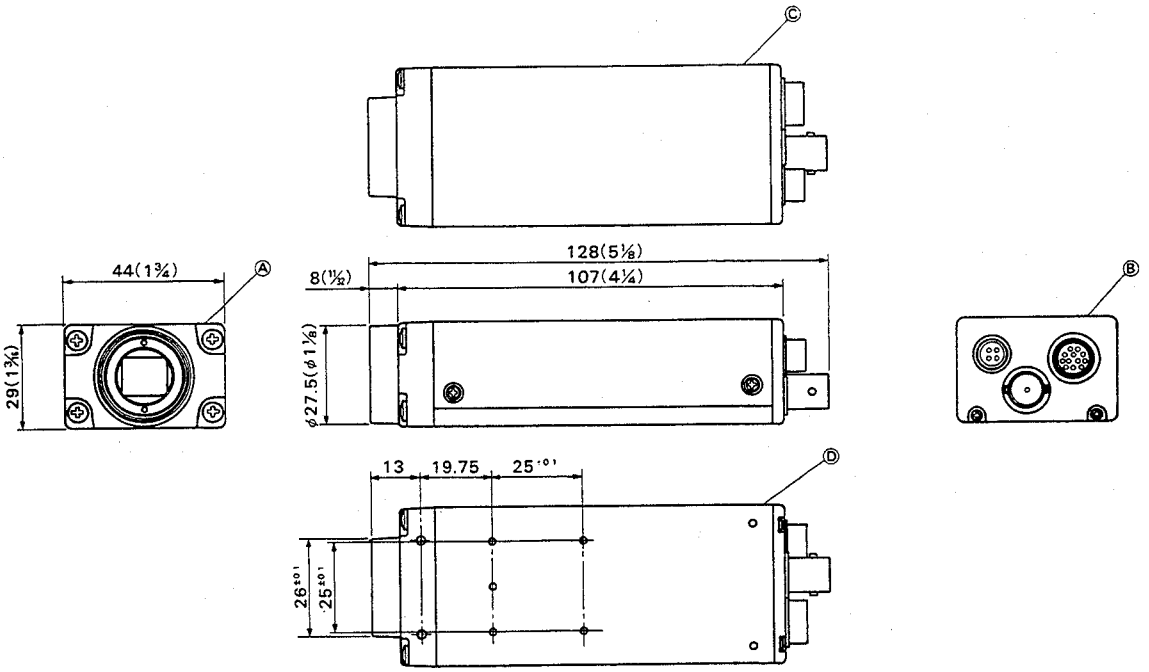
<STANDARD LENS VCL-16Y-M>

Focal Length	16 mm
Maximum Aperture Ratio	1 : 1.4
Iris Control	F1.4 ~ F16
Filter Thread	M 25.5 mm x P 0.5 mm
Mount	C mount
Weight	50 g

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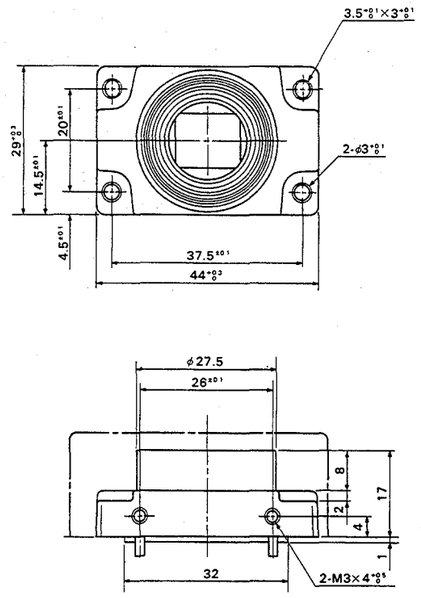
Dimensions:

Camera Module <XC-77>

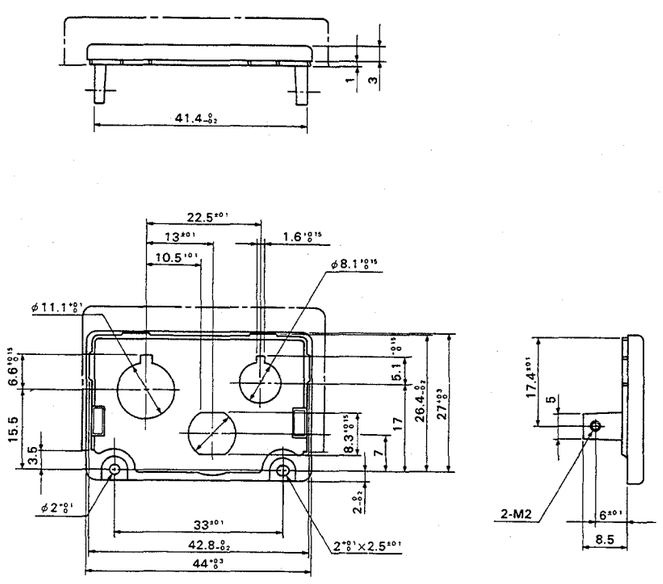


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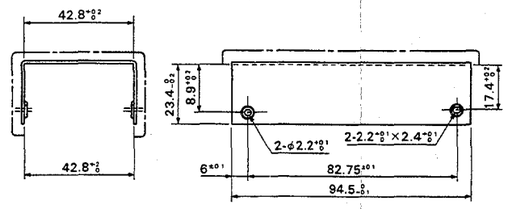
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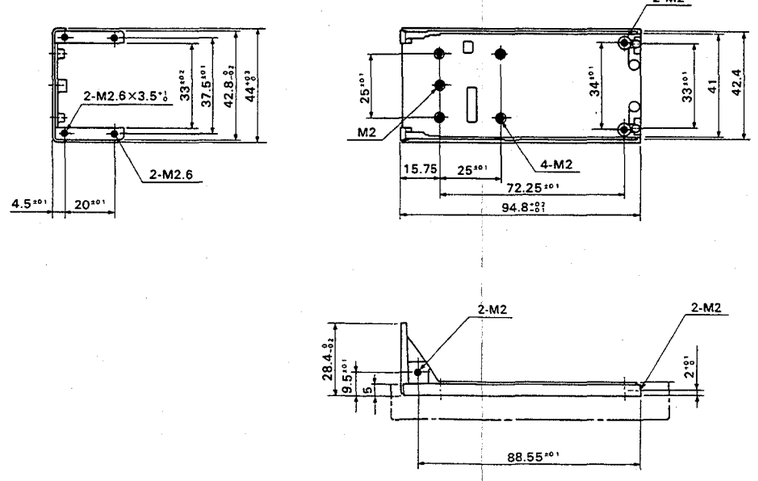
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Ⓒ

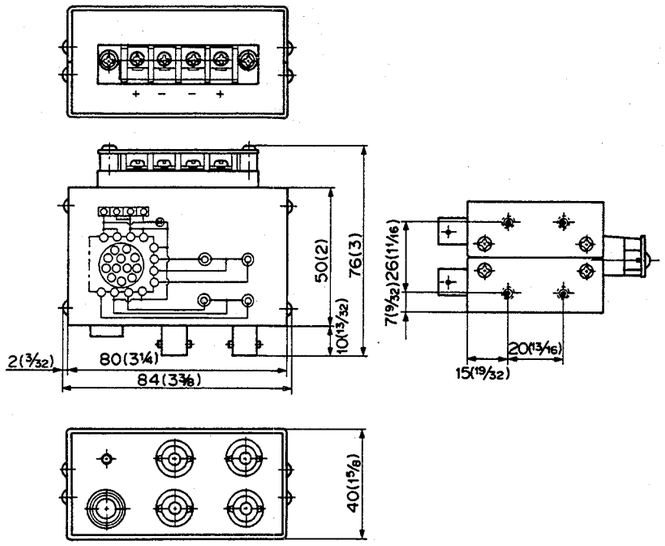


Ⓓ

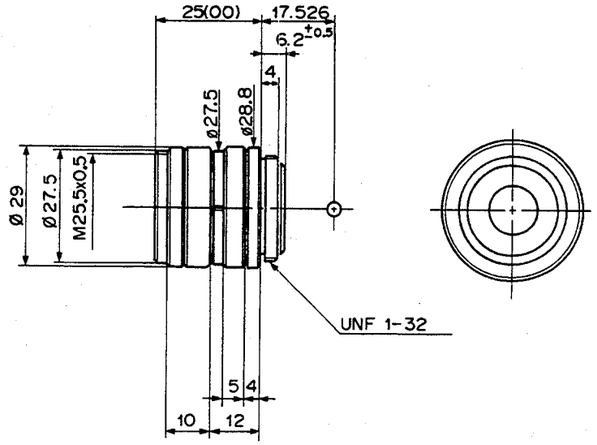


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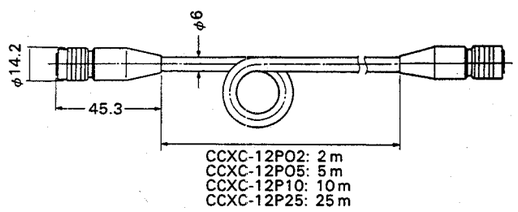
Junction box



Lens

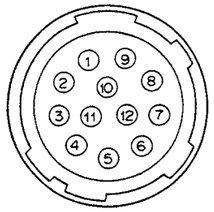


Camera cable



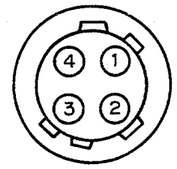
2-2. CONNECTORS' PIN FUNCTION

12-P Multiconnector (External view)



PIN NO.	EXTERNAL SYNC MODE			CAMERA SYNCRONOUS OUTPUT
	HD, VD	VBS/VS	RESTART RESET	
1	GND	GND	GND	GND
2	+12 V	+12 V	+12 V	+12 V
3	VIDEO OUTPUT (GND)	VIDEO OUTPUT (GND)	VIDEO OUTPUT (GND)	VIDEO OUTPUT (GND)
4	VIDEO OUTPUT (SIGNAL)	VIDEO OUTPUT (SIGNAL)	VIDEO OUTPUT (SIGNAL)	VIDEO OUTPUT (SIGNAL)
5	HD INPUT (GND)	——	HD INPUT (GND)	HD INPUT (GND)
6	HD INPUT (SIGNAL)	——	HD INPUT (SIGNAL)	——
7	VD INPUT (SIGNAL)	VBS INPUT (SIGNAL)	RESET PULSE (SIGNAL)	——
8	CLOCK OUTPUT (GND)	CLOCK OUTPUT (GND)	CLOCK OUTPUT (GND)	CLOCK OUTPUT (GND)
9	CLOCK OUTPUT (SIGNAL)	CLOCK OUTPUT (SIGNAL)	CLOCK OUTPUT (SIGNAL)	CLOCK OUTPUT (SIGNAL)
10	GND	GND	GND	GND
11	+12 V	+12 V	+12 V	+12 V
12	VD INPUT (GND)	VBS INPUT (GND)	RESET PULSE (GND)	FIELD INDEX OUTPUT (GND)

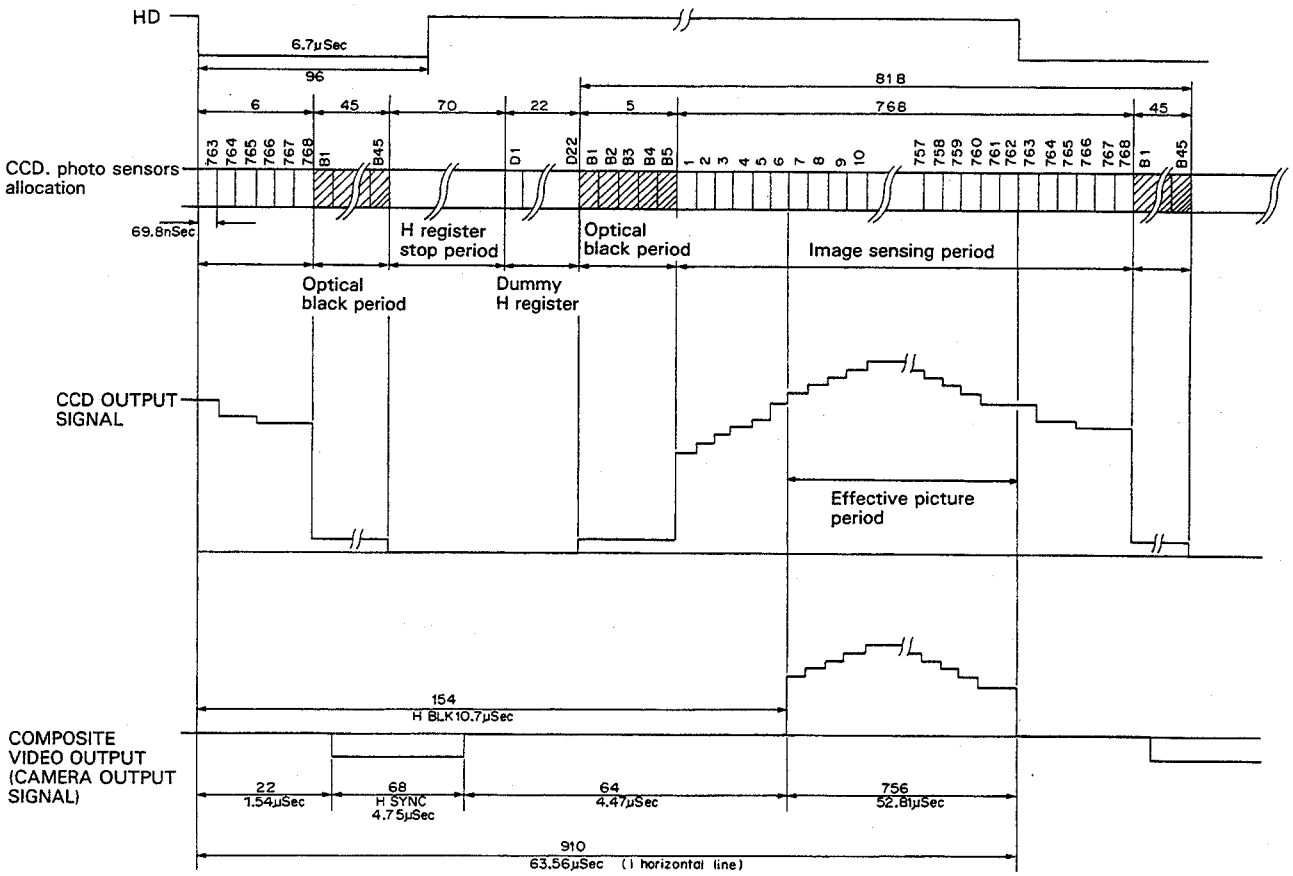
4P Lens Connector (External view)



PIN NO.	SIGNAL	SPECIFICATION
1	+12 V OUT	DC 12 V OUTPUT
2	GND	GND
3	NC	NC
4	VS OUT	VIDEO SIGNAL OUTPUT

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2-3. OUTPUT SIGNAL TIMING CHART



2. COMPREHENSIVE SPECIFICATIONS

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2-4. External Synchronization

There are three external synchronization modes:
1. VS/VBS mode
2. HD and VD mode
3. RESTART RESET mode

2-4-1. VS/VBS mode

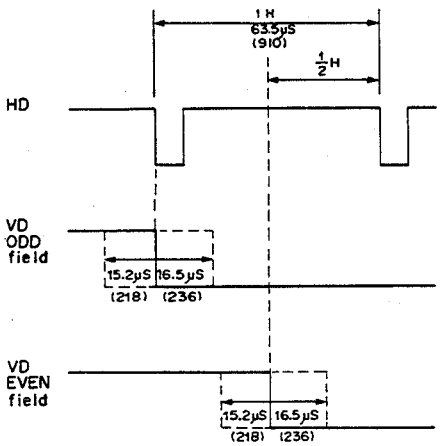
The VS/VBS mode provides external synchronization by supplying a normal composite signal, VS or VBS, to pin 7 of the 12-pin connector.

2-4-2. HD and VD mode

The HD and VD mode provides external synchronization by supplying an HD signal to pin 6 and a VD signal to pin 7 of the 12-pin connector.

- Input conditions of HD and VD signals
- Frequency (period)
  HD: 15.734 kHz ±1% (63.56 μs ±1%)
  VD: 244 to 1023 1/2 H
  * The maximum number of vertical effective lines is 486 in the interlace mode.
    In the non-interlace mode, it is 242 for both the ODD field and the EVEN field.

- Phase



The figure in parentheses ( ) indicates the number of clock pulses

As shown in the illustration above, the ODD field is provided when the phase shift between the trailing edge of the VD signal and the trailing edge of the HD signal is between a lead of 15.2 μs and a lag of 16.5 μs. The EVEN field is provided when the phase shift between the trailing edge of the VD signal and the point 1/2H from the trailing edge of the HD signal is between a lead of 15.2 μs and a lag of 16.5 μs.

- Interlace and noninterlace

Operation can be performed in either interlace or non-interlace mode by changing the input condition of the VD signal. See Figure 1.

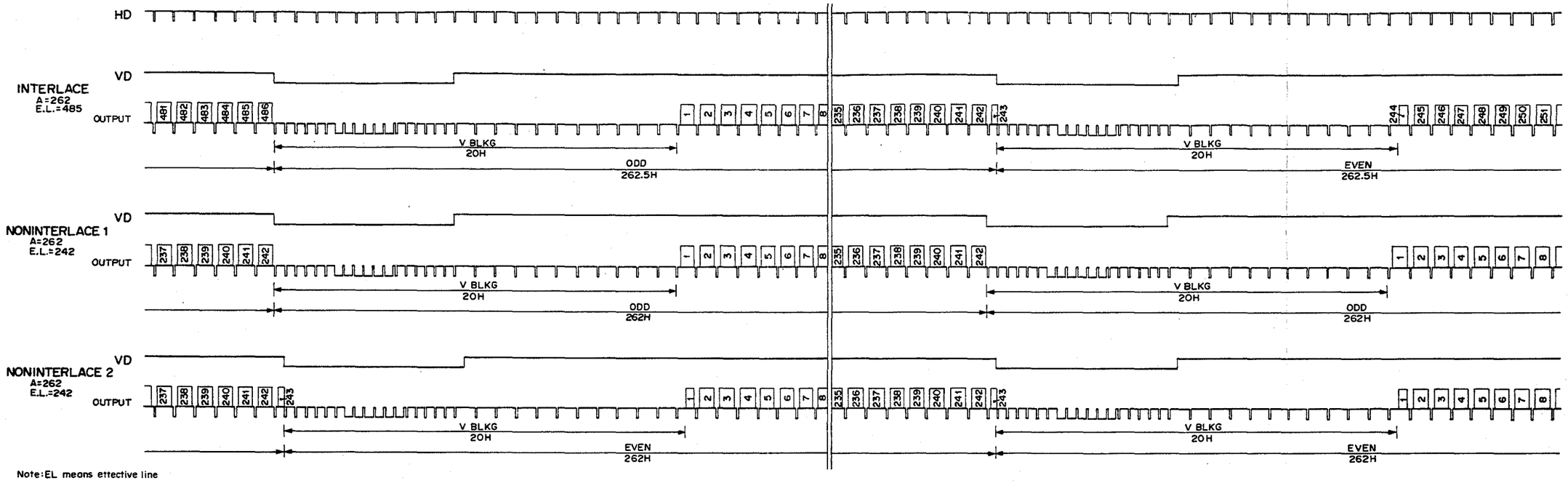
- Interlace

To operate in the interlace mode, set the period of the VD signal to (A + 1/2)H. A is an integer, 244 to 1023. In other words, the phase of the leading edge of the VD signal against the leading edge of the HD signal is changed for each VD signal. The field changes from ODD to EVEN and to ODD, repeatedly during operation in the interlace mode. At this time, the number of scanning lines per frame is 2A + 1.

- Non-interlace

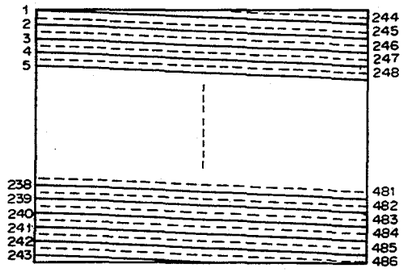
To operate in the non-interlace mode, set the period of the VD signal to A H. A is an integer, 244 to 1023. In other words, the phase of the leading edge of the VD signal against the leading edge of the HD signal is not changed for each VD signal, and the field ODD or EVEN remains unchanged for operation in the non-interlace mode. The number of scanning lines is A; this is half of the number of scanning lines for operation inthe interlace mode. The sensitivity is half of the sensitivity provided in the interlace mode, when the frame is stored.

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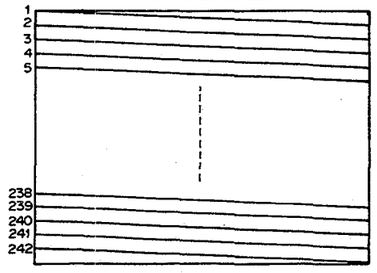


Note:EL means effective line

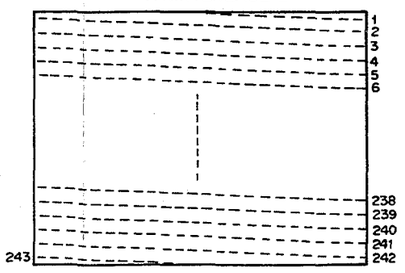
INTERLACE



NONINTERLACE 1

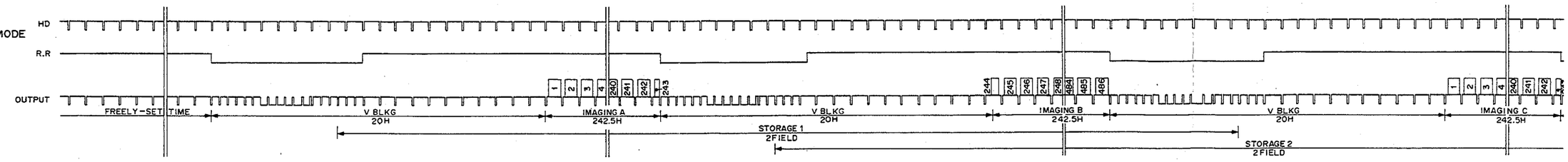


NONINTERLACE 2

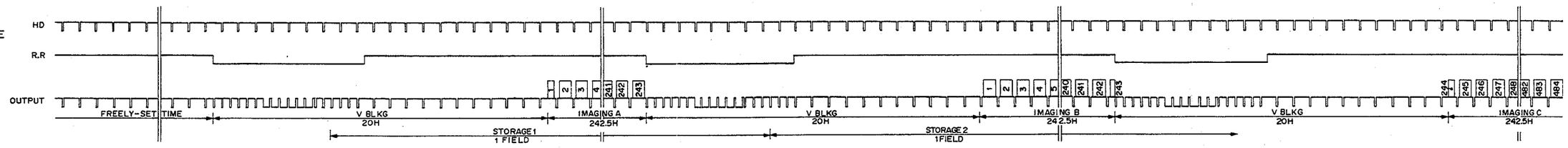


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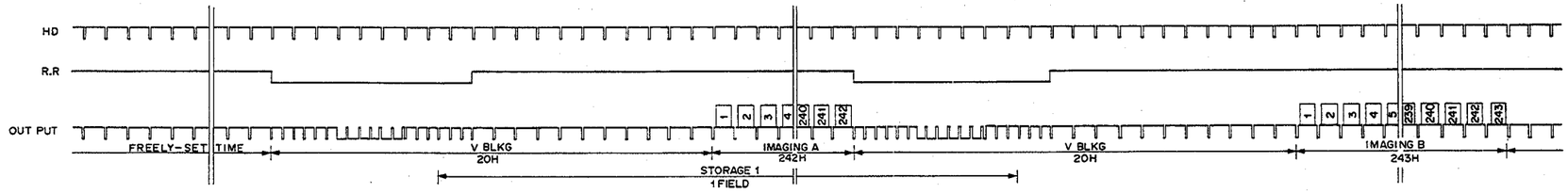
FRAME INTEGRATION MODE
INTERLACE
A=262
E.L.=485



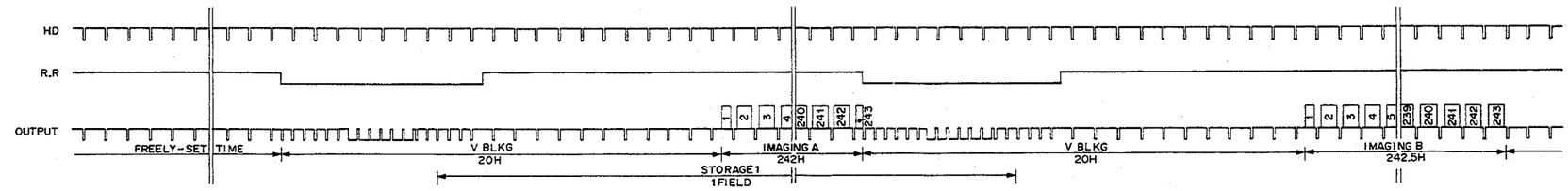
FIELD INTEGRATION MODE
INTERLACE
A=262
E.L.=485



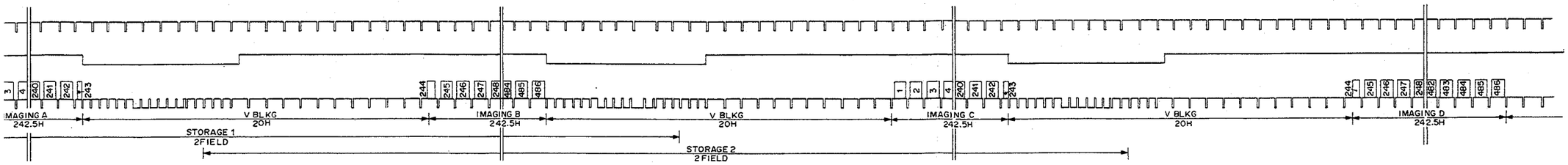
NONINTERLACE 1
A=262
E.L.=243

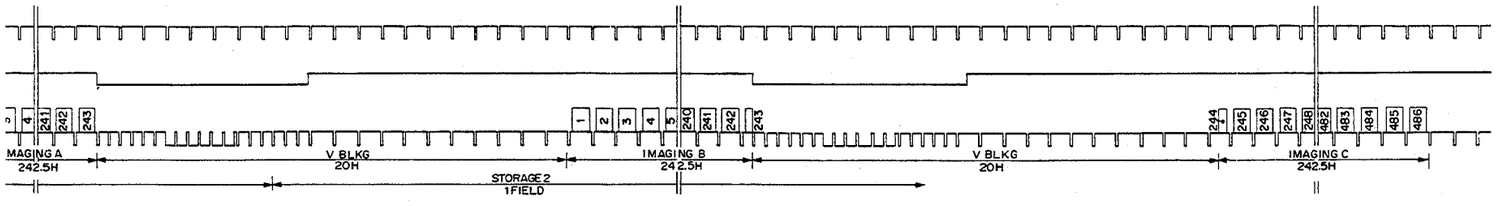


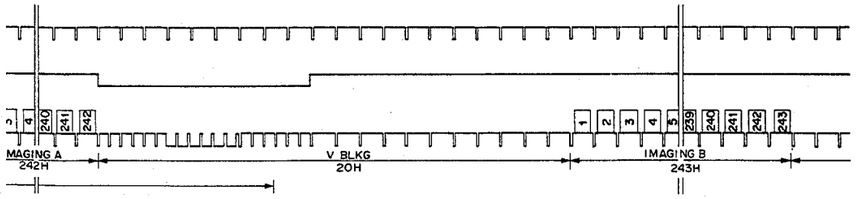
NONINTERLACE2
A=262
E.L.=242

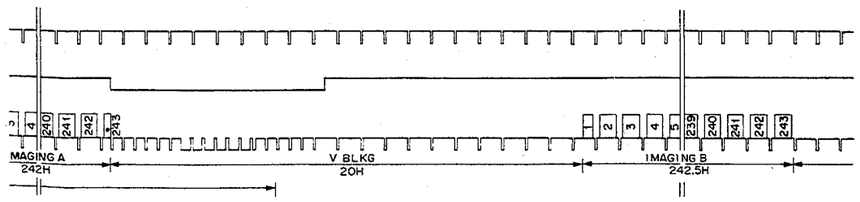


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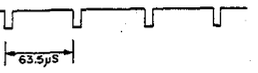
2-4-3. RESTART RESET mode

In the RESTART RESET (RR) mode, information for one screen can be retrieved at any time. It is necessary to internally set the RR mode in the camera to provide the RR mode. See Section 2-5 "Mode Setting". Supply the HD and RR signals to pin 6 and pin 7 of the 12-pin connector to obtain output.

- Input conditions for the HD and RR signals
- Frequency (period)

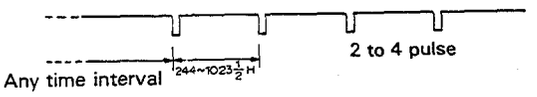
HD signal: 15.734 kHz ±1% (63.56 μs ±1%)

Continuous pulse



VD signal: 244 to 1023 1/2 H

2 to 4 pulses depending on the mode



- Phase

The same phase conditions as for the HD and VD mode are applied to this mode. See Section 2-4-2.

- Explanation of the timing chart

Figure 2 is the timing charts for each operation mode. The details of these timing charts are given below:

- Frame INTEGRATION interlace mode

The RR requires four pulses. Set the period of the RR to A + 1/2H. A is an integer, 244 to 1023. It is 262 in the figure.
Shooting information during STORAGE 1 and STORAGE 2 is output in the intervals of IMAGING C (ODD) and IMAGING D (EVEN). The CCD is reset in the intervals of IMAGING A and IMAGING B. Therefore, signals output during these intervals are meaningless.

- Field INTEGRATION interlace mode

The RR requires three pulses. Set the period of the RR to A + 1/2H. A is an integer, 244 to 1023. It is 262 in the figure.
Shooting information during STORAGE 1 and STORAGE 2 is output in the intervals of IMAGING B (ODD) and IMAGING C (EVEN). The CCD is reset in the interval of IMAGING A; therefore, signals output during this interval are irrelevant.

- Noninterlace mode

The RR requires two pulses regardless of the storage mode. Set the period of the RR to A H. A is an integer, 244 to 1023. It is 262 in the figure.
Shooting information in STORAGE 1 is output in the interval of IMAGING B. The CCD is reset in the interval of IMAGING A; therefore, signals output during this period are irrelevant.

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2-5. Mode Setting

The XC-77 can switch the operation mode, depending on the use.
The modes are set on the PR-89, SG-119, and MB-136 boards.

PR-89 board

Item	Mode	SHORT	OPEN
AGC	AGC	AGC	FIX
	FIX GAIN	FIX	AGC
γ	1	γ1	γ2
	COMPENSATE	γ2	γ1
WHITE CLIP	γ	γ1	γ2
	WHITE CLIP	γ2	γ1

SG-119 board

Item	Mode	M't	OPEN
EIA/CCIR	EIA	R 7	R 6
	CCIR	R 6	R 7
FRAME/FIELD	FRAME	R 1	R 2
	FIELD	R 2	R 1
FIELD	NORMAL	R23	R28
	INVERSION	R28	R23
RESTART RESET	NORMAL	R24	R29
	RESET	R29	R24
EIA/CCIR	EIA	R27	R22
	CCIR	R22	R27

*The value of resistors R1 and R2 is 1 kΩ.
The value of all resistors is 10 kΩ except R1 and R2.

MB-136 board

Item	Mode	M't	OPEN
RESTART RESET	NORMAL	R35	
	RESET		R35

*The value of resistor R35 is 220 kΩ.

- Explanation of all operation modes

- VIDEO GAIN mode (AGC/FIX GAIN)

Set the gain of the video output signal with this mode.
When it is set to AGC, the automatic gain control functions.
When it is set to FIX GAIN, a fixed gain is obtained.
The setting is performed with the AGC trace on the PR-89 board. To set the gain to AGC, connect the AGC end and disconnect the FIX end. To set the gain to FIX GAIN, connect the FIX end. To set the gain to FIX GAIN, connect the FIX end and disconnect the AGC end.
The factory setting is FIX GAIN.

- Gamma compensation mode (1/COMPENSATION)

Set the gamma correction of the video output signal by this mode. When the gamma is set to COMPENSATE, video signals for which gamma correction is performed are output. When it is set to 1, no gamma correction is performed for video signals. This setting provides video signals proportional to the amount of light from the object.
The setting is performed with the gamma and white clip traces on the PR-89 board. To set COMPENSATE, connect the gamma 2 ends of both gamma and white clip traces, and disconnect the gamma 1 ends. To set 1, connect the gamma 1 ends of both gamma and white clip patterns, and disconnect the gamma 2 end.
The factory setting is 1.

- EIA/CCIR mode (EIA/CCIR)

Set the signal system of the video output signal with this mode.
Always set the signal system to EIA.

- Storage mode (FRAME/FIELD)

Set the period in which a signal charge is read from the photosensor in the CCD with this mode.
When it is set to FIELD, a signal charge is read for each field. When it is set to FRAME, a signal charge is read for each frame. Note that if the FRAME mode is set for operation in the non-interlace mode, the sensitivity is half of the sensitivity provided in the interlace mode.
The setting is performed with the FRAME/FIELD trace on the SG-119 board.
To set the period to FIELD, mount then R1 (1 kΩ) on the FRAME/FIELD trace, and demount R2.
To set the period to FRAME, mount then R2 (1 kΩ) on the FRAME/FIELD trace and demount R1.
The factory setting is FRAME.

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• RESTART RESET mode (NORMAL/RESET)

Set the external synchronization mode with this mode. When NORMAL is set, the external synchronization mode is set to the VS/VBS mode or HD and VD mode. When RESET is set, the external synchronization mode is set to the RESTART RESET mode. See Section 2-4 External Synchronization for the details of each external synchronization mode.

The setting is performed with the RESTART RESET trace on the SG-119 board and R35 to be mounted on the MB-136 board.

To set NORMAL, mount R24 (10 kΩ) of RESTART RESET and demount R29. Also mount R35 on the MB-136 board.

To set RESET, mount R29 (10 kΩ) of RESTART RESET and demount R24. Also demount R35 on the MB-136 board.

The factory setting is NORMAL.

• Field inversion mode (NORMAL/INVERSION)

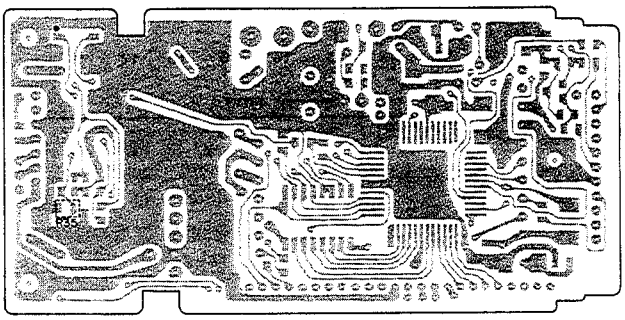
Set the field inversion operation of the video output signal at external synchronization with this mode.

When INVERSION is set, the field of the video output signal is inverted against the external synchronization signal. In other words, when the field of the external synchronization signal is ODD, EVEN is output and when it is EVEN, ODD is output.

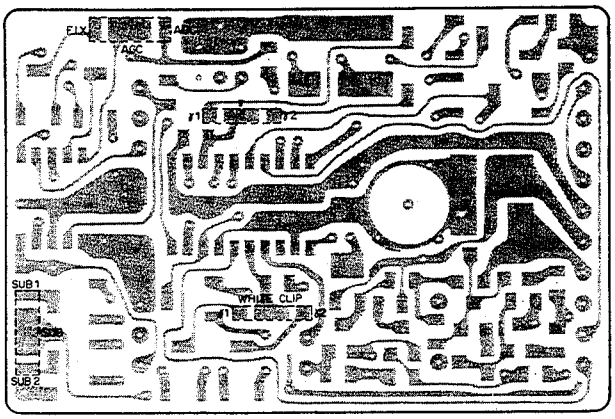
When NORMAL is set, operation is the same as for the normal external synchronization. In other words, when the field of the external synchronization signal is ODD, ODD is output and when it is EVEN, EVEN is output.

The setting is performed with the FIELD trace on the SG-119 board. To set NORMAL, mount R23 (10 kΩ) of FIELD, and demount R28. To set INVERSION, mount R28 (10 kΩ) of FIELD, and demount R23.

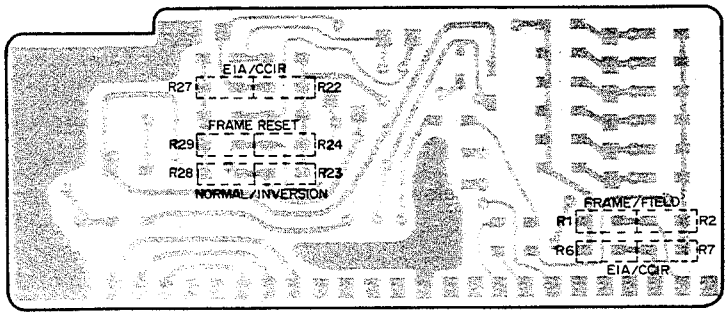
The factory setting is NORMAL.



MB−136 BOARD (Soldering Side)



PR−89 BOARD (Soldering Side)



SG−119 BOARD (Soldering Side)

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2-6. THEORY OF OPERATION

<Operation principle of the CCD>

A CCD (Charge Coupled Device) consists of MOS (Metal-Oxide-Semiconductor) capacitors arranged in a regular array.
It basically performs three functions connected with handling charges.

1. Photoelectric conversion (photosensor)
Incident light generates charges on the MOS capacitors, with the quantity of charge being proportional to the brightness.

2. Accumulation of charges
When a voltage is applied to the electrodes of the MOS capacitors, an electric potential well is formed in the silicon layer. The charge is accumulated in this well.

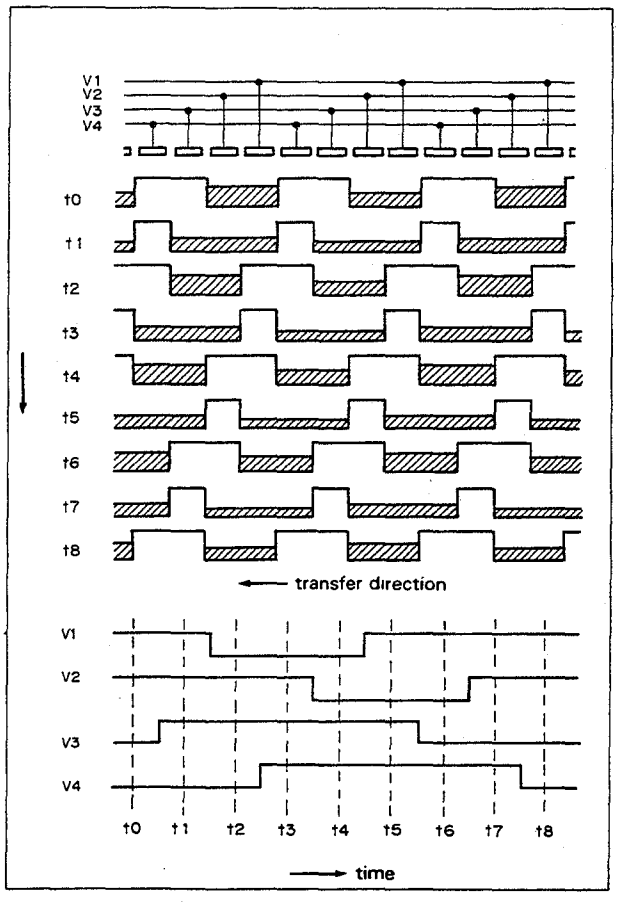
3. Transmission of charge
When a high voltage is applied to the electrodes, a deeper well is formed; when a low voltage is applied, a shallower well is formed, In the CCD, this property is used to transmit the charge. When a high voltage is applied to the electrodes, a deep electric potential well is formed, and charge flows in from neighboring well. When this is repeated over and over among the regularly arranged electrodes, the charge is transferred from ones MOS capacitor to another. This is the principle of CCD charge transmission.

<Mechanism of CCD charge transfer>

1. Vertical transfer
The vertical shift register transfers charges using a four-phase drive mode. Figure 1 shows an example of the changes which can occur in potential wells in successive time intervals.
At t0, the electrode voltages are (V1 = V2) > (V3 = V4), so the potential wells are deeper toward the electrode at the higher voltages V1 and V2. Charges accumulate in these deep wells. At t1, the electrode voltages are (V1 = V2 = V3) > (V4), so the charges accumulate in the wells toward the electrode at V1, V2 and V3. At t2, the electrode voltages are (V2 = V3) > (V4 = V1), so the charges accumulate in the wells toward the electrode at V2 and V3.
Electrode voltage states at t3 and after are shown below.

t3 (V2 = V3 = V4) > (V1)
t4 (V3 = V4) > (V1 = V2)
t5 (V4) > (V1 = V2 = V3)
t6 (V4 = V1) > (V2 = V3)
t7 (V4 = V1 = V2) > (V3)
t8 (V1 = V2) > (V3 = V4) (Initial state)

These operations are repeated to execute the vertical transfer.



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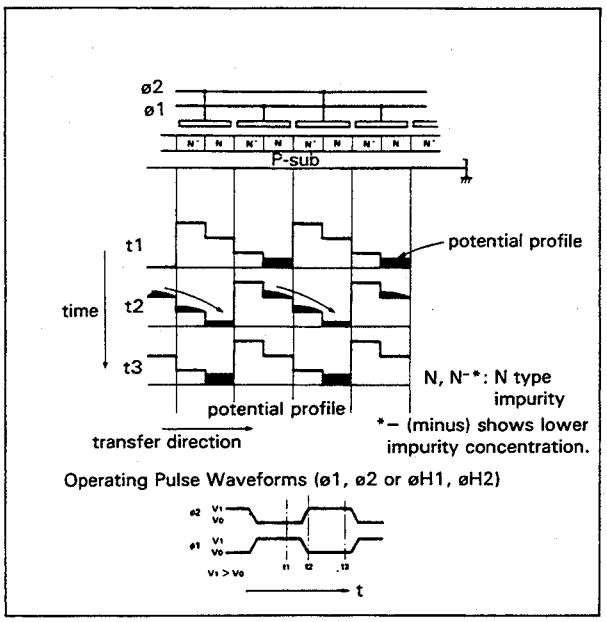
2. Horizontal transfer

The horizontal shift register transfers charges using a two-phase drive mode. Figure 2 shows an example of the changes which can occur in the potential wells in successive time intervals. At t1, the electrode voltages are H1 > H2, so the potential wells are deeper toward the electrode of the higher voltage H1. The charges accumulate in these wells. At t2, the electrode voltages H1 and H2 are inverted, the wells toward the electrode at voltage H2 becomes deeper while the wells toward the electrode at voltage H1 become shallower. So the wells at H2 are deeper than those at H1, the charge flows into the deeper wells toward the electrode at H2. At t3, the electrode voltage have not changed since t2, so the charge flows into the wells at H2 and one transfer of charge is completed. These operations are repeated to execute the horizontal transfer.

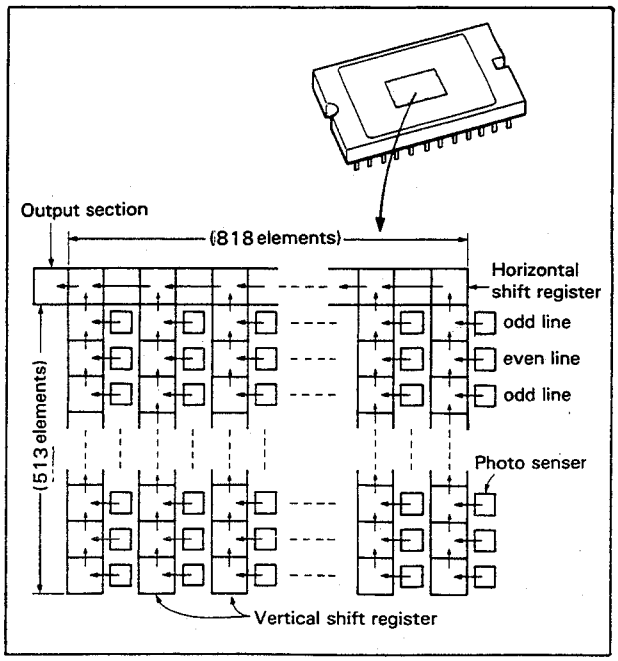
<BI-12 board>

Light which comes through the camera lens strikes the CCD chip surface of IC1 on the BI-12 board. The surface of the CCD contains a number of photosensors.

The array is 818 horizontal photosensors by 513 vertical photosensors, so that there are a total of 419,634. The effective number of them is 768 photosensors by 494 photosensors, so there are total of 382,464. Incident light is converted to a charge (signal charge) at the photosensor in proportion to the brightness of the light. The converted signal charge is read out by a register from the photosensor, and is transferred in sequence and fed to the output section. The register is subdivided into horizontal and vertical shift registers. As shown in Fig. 3, there are 818 vertical rows of registers, while there is only one horizontal row of registers, across the top. Each converted charge is transmitted every field (frequency of VD) to the vertical shift register adjoining to the photosensor. The signal charge is then vertically transferred in sequence at the vertical transfer clock V1, V2, V3 and V4 (frequency of HD) to the horizontal register. The horizontal registers transfer charges horizontally at the horizontal transfer clock H1, H2 (= 910 fh) to the output section. The output section converts the charge to the voltage and outputs it. The signal from IC1 is fed to the SH-27 board via the buffer Q1.



[Fig.1] The interline-transfer organization of the CCD image sensors



[Fig. 2] Two Phase CCD Charge Transfer

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<SH-27 board>
It contains a sample and hold circuit. CCD output signals sent from the BI-12 board are divided into two Both signals are sampled and held by a sampling and holding pulses (SHP, SHD). One signal is sampled and held three times by these pulses; in order of the SHP, SHD and SHP pulses. The other signal is sampled and held two times by the SHD pulse and then SHP pulse. The difference of these two signal removes a noise component of CCD output signal to obtain the video signal, using a differential amplifier consisting of Q16 through Q19. The video signal from the differential amplifier is sent to the PR-89 board.

<PR-89 board>
It contains a video signal processing circuit, which converts the video signal from the SH-27 board into a video signal of EIA standard. The video signal from the SH-27 board is fed to IC1. IC1 contains an auto-iris circuit and a gain control amplifier for AGC. The signal from the gain control amplifier passes through a low-pass filter FL1 and is then fed to IC2. In IC2, various signal processings such as clamping, gamma correction, white clipping, blanking mixing, setup addition, and sync signal mixing are executed. The resultant signal is then passed through an output driver circuit consisting of Q1 through Q8 and sent from this board.

<CN-163 board>
It connects the MB-136 board with each external connector. 12-pin multiconnector (DC IN/SYNC connector), 4-pin connector (LENS connector) and BNC connector (VIDEO OUT connector) are mounted on this board. At 12-pin multiconnector, +12 V power voltage, external synchronizing signals (EXT HD, EXT VD, RESET PULSE, VBS and VS) are input and the video signal (VS) and synchronizing signals (CLOCK, HD, FIELD INDEX) are output. 12-pin multiconnector I/O signals varies according to selection of sync mode(internal sync or external sync mode). Refer to Section 2-2 in details. +12 V power supply and video signal for auto-iris lens are output from 4-pin connector. The video signal (VS) is output from the BNC connector.

<RG-18 board>
It supplies a DC voltage to be applied to CCD driving clock generator and CCD substrate.

<MB-136 board>
It contains an external synchronizing signal detection circuit, 1820 fh oscillator, DC-to-DC converter and CCD driving clock generator. When external synchronizing signals are supplied to this board, the camera automatically selects external sync mode and outputs a video signal synchronized with the external synchronizing signal. For external synchronizing, EXT VD and EXT HD, or EXT SYNC, or EXT HD and RESET PULSE can be used. When EXT HD and EXT VD, or EXT HD and RESET PULSE are supplied, the MB-136 board wave-shapes these signals using Q1, Q2, Q3 and IC7 and outputs them to the SG-119 board. When EXT SYNC of VBS or VS is supplied, this board detects only a sync component using Q2, Q3 and IC7, and wave-shapes it. The resultant SYNC signal is output to the SG-119 board.
1820 fh oscillator is subdivided into two, which are for external and internal synchronizing. In the internal sync mode, the oscillator using a crystal oscillator (X1) operates. In the external sync mode, the voltage controlled oscillator VCO which is an LC oscillator operates. The VCO can vary oscillation frequency within ±1%. A control voltage of VCO are supplied between 0 V and 5 V. When the control voltage is 2.8 V, the oscillation frequency is set to be 28.6363 MHz (= 1820 fh).
The clock signal of 1820 fh is fed to the CCD driving clock generator. The DC-to-DC converter converts the externally-supplied DC (+12 V) into four DC voltages; +15 V, +10 V, +7 V, and +5 V. These voltages are fed to each board.
CCD driving clock generator generates the clock signal necessary to drive the CCD. When the HD and VD signals from the SG-119 board and the clock signal of 1820 fh from the 1820 fh oscillator are fed to IC1.
It outputs the following signals.

CLOCK: The clock signal of 910 fh (half the clock signal of 1820 fh)

H1, H2: Two-phase clock signal
These are used to drive the horizontal shift register and to transfer the signal charges.

V1 to V4: Four-phase clock signal
These are used to drive the vertical shift register and to transfer the signal charges.

PG: Precharge gate control pulse
A precharge gate is the gate of the output section connected to the horizontal register. This gate is controlled by this pulse to convert a transferred signal charge into the voltage.

SHP, SHD: These pulses are used to sample the CCD output signal.

CLP1: This pulse is used to clamp the optical black level of the CCD output signal.

CCD driving clock signals H1, H2, V1 to V4, and PG are output to the CCD after passing through the drive circuit consisting of IC3, IC5 and IC6.

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<SG-119 board>

It contains synchronizing signal generator. When CLOCK of 910 fh from the MB-136 board is fed to the IC1 and IC2, they outputs the following synchronizing signals.

SYNC:	Synchronizing signal
BLKG:	Blanking signal
HD, VD:	Horizontal and vertical synchronizing signal
FLD:	Field index signal
INT/EXT:	Sync mode selection signal Low for internal sync mode, and high for external sync mode.
VCO CONT:	A control voltage of VCO for external synchronizing.

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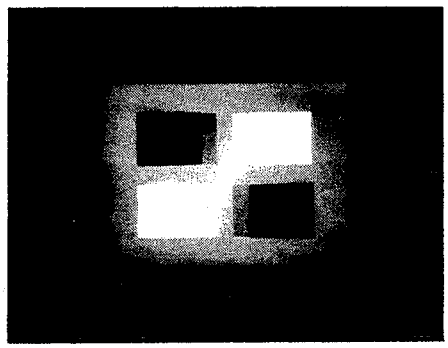
SECTION 3
ALIGNMENT

3-1. PREPARATION

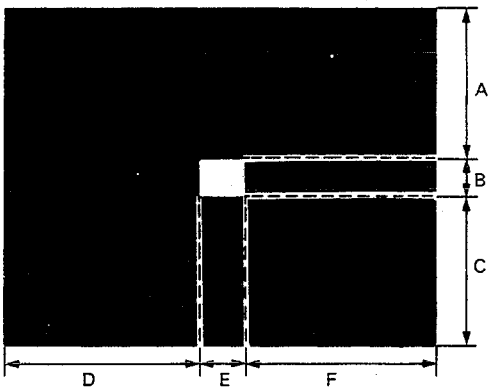
Step 1: Jigs and measuring instruments

- Oscilloscope
- Waveform monitor
- B/W monitor
- Digital voltmeter
- Power supply equipment: Junction box JB-77 (sold on the market), regulated power supply unit
- Tripod attachment: VCT-37 (sold on the market)
- Lens: Standard VCL-16Y-M (sold on the market)
- Pattern box: PTB-500 or PTB-100
  (SONY part No.: J-6029-140-A)

- Grayscale chart
  (SONY part No.: J-6026-130-A)



- White window chart
  Make a hole in black paper as shown in the figure.



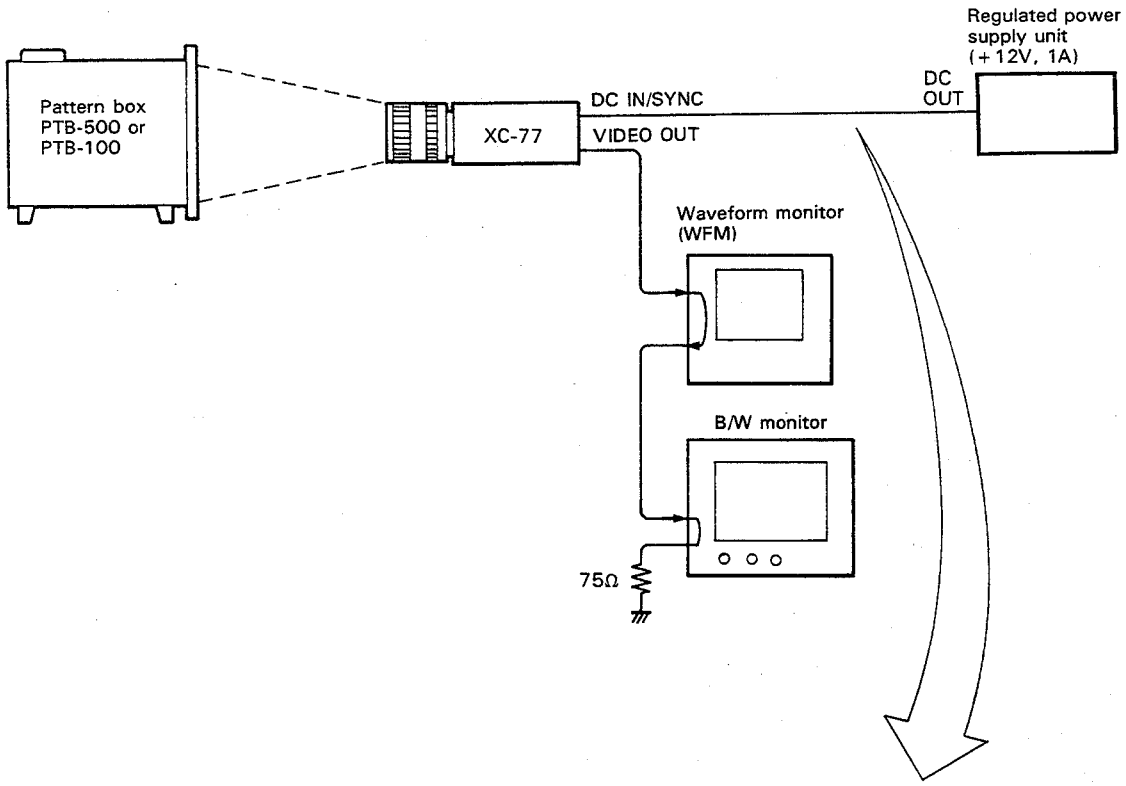
Vertical A:B:C = 4.5:1:4.5
Horizontal D:E:F = 4.5:1:4.5

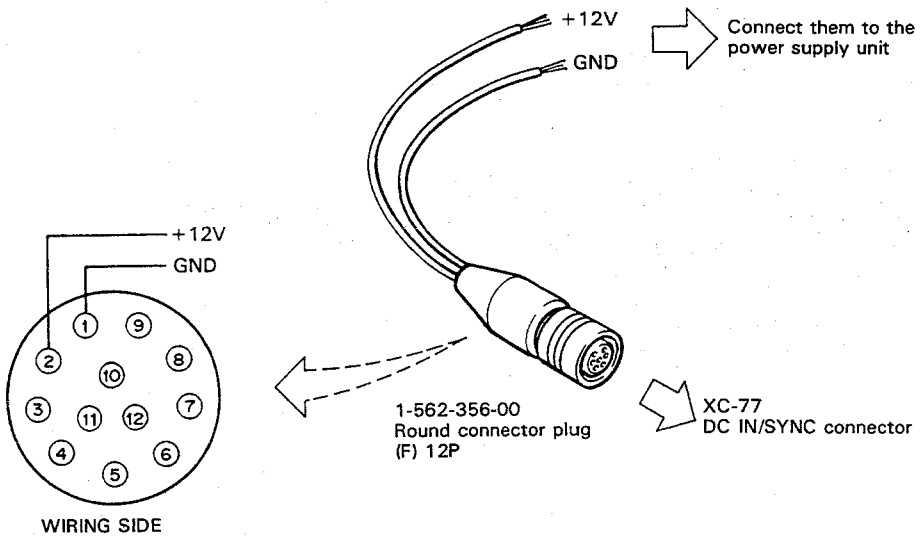
[If the pattern box is unavailable]
- 100-W bulb
- Variable voltage transformer

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Step 2: Connection diagram

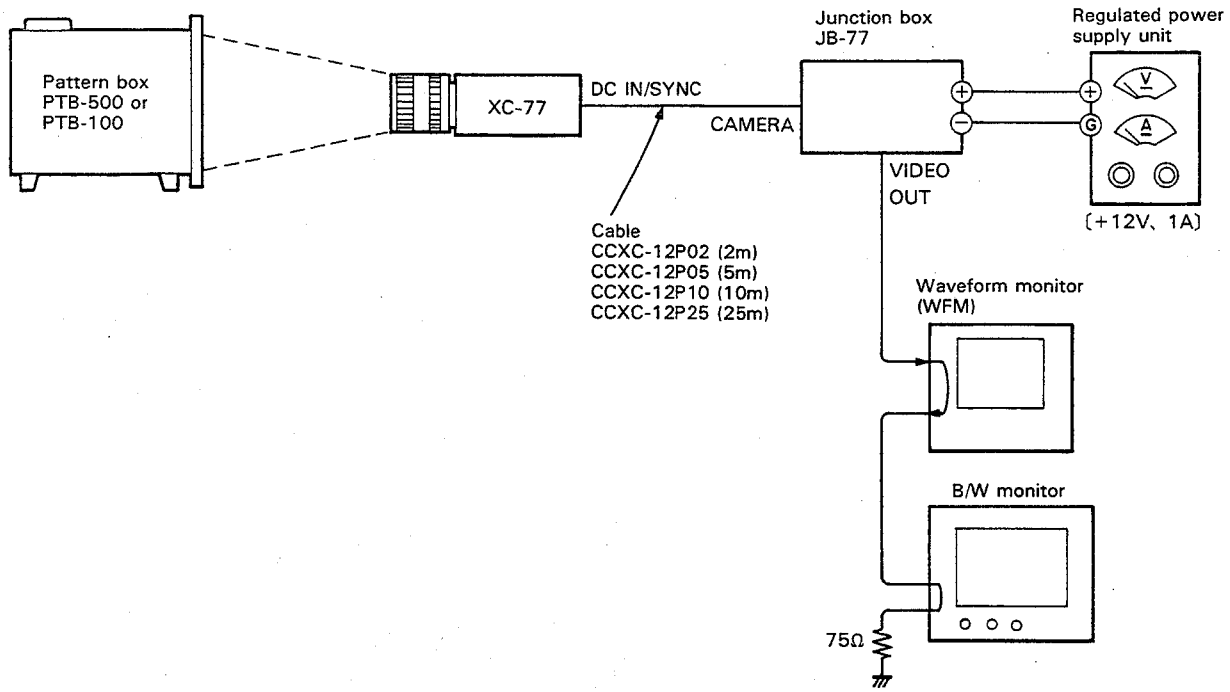
[Connection method 1]



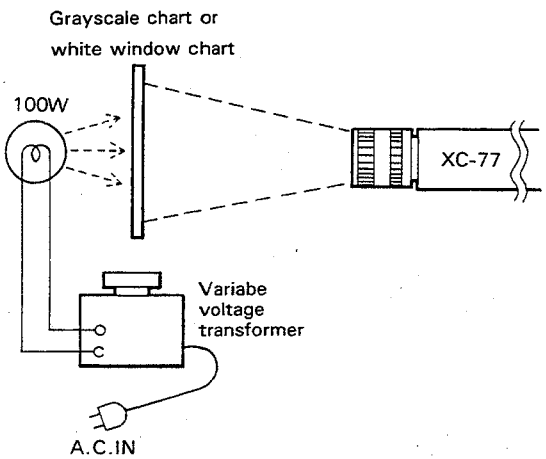


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[Connection method 2]



[If the pattern box is unavailable]
Make adjustment with a simple illuminator as shown below.



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3-2. OVERALL ADJUSTMENT

Step 1: V SUB (field) adjustment

• Caution

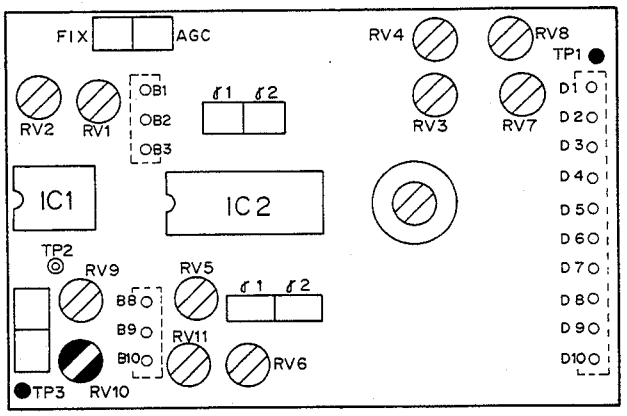
Do not make this adjustment except when the CCD is replaced.

• Setting

Measuring instrument	Digital voltmeter

• Adjustment procedure

1. Test Point; TP3 (GND:TP1)/PR-89 board
   Adj. Point: ◐ RV10/PR-89 board
   Spec.: When using a new CCD, adjust the V SUB voltage so that the specification written in the back of the CCD is satisfied.



PR-89 BOARD (Component Side)

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SECTION 2
COMPREHENSIVE SPECIFICATIONS

2-1. SPECIFICATIONS

<CAMERA MODULE XC-77CE>

Pickup Device		Interline transfer CCD
Picture elements		756 (H) x 581 (V)
Sensing area		8.8 mm x 6.6 mm (the same as the 2/3-inch camera tube)
Optical black		60 pixels each horizontal line
Vertical drive frequency		15.625 kHz
Horizontal drive frequency		14.1875 MHz
Signal system		CCIR standard
Structure		Interline transfer
Cell size		11 μm (H) x 11 μm (V)
Chip size		10.0 mm (H) x 8.2 mm (V)
Optical System		
Lens mount		C mount
Frange back length		17.526 mm
Sync System		Internal/External autmatic change
External sync input		VBS, VS, BS (SYNC LEVEL 0.3 Vp-p ± 6 dB)
External sync frequency tolerance		± 1%
Jitter		Within ± 100 n sec
Locking time when power is on.		Within 10 sec
Scanning System		2 : 1 Interface ; 625 lines
Video Output		1.0 Vp-p sync negative, 75 ohms unbalanced.
Horizontal Resolution		560 TV lines
Vertical Effective lines		2 : 1 Interlace ; 575 lines
Sensitivity		400 Luxes with F4 (γ ON/odB)
Minimum Illumination		3 Luxes, F1.4
S/N ratio		50 dB
Power Requirement		DC 12 V
Power Voltage Tolerance		DC 10.5 V ~ 15 V
Power Consumption		2.2 W
Weight		
Camera module		190 g (XC-77CE)
Tripod attachment		15 g (VCT-13)
Camera cable	(2 m)	130 g (CCXC-12P02)
	(5 m)	295 g (CCXC-12P05)
	(10 m)	560 g (CCXC-12P10)
	(25 m)	1.4 Kg (CCXC-12P25)
4-pin connector		g (PC-XC04)
12-pin connector		g (PC-XC12)
Junction box		170 g (JB-77)
Storage Temperature		−30°C ~ +60°C
Operating Temperature		0°C ~ 40°C
Shock resistance		70 G
Storage Humidity		Within 90%
Operating Humidity		Within 70%

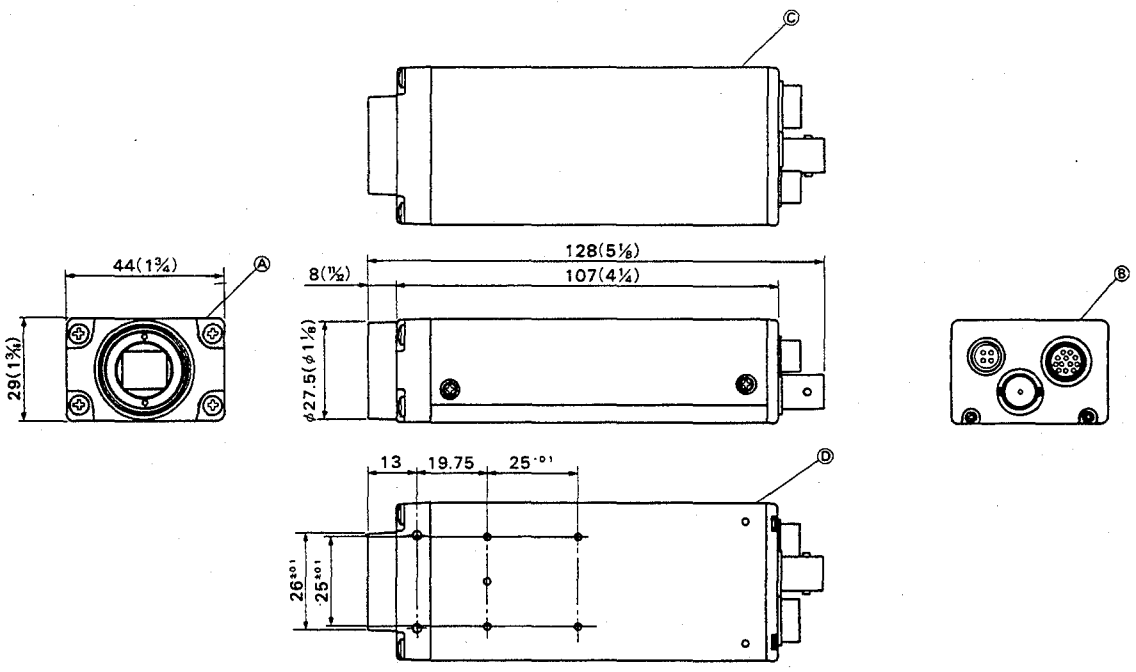
<STANDARD LENS VCL-16Y-M>

Focal Length	16 mm
Maximum Aperture Ratio	1 : 1.4
Iris Control	F1.4 ~ F16
Filter Thread	M 25.5 mm x P 0.5 mm
Mount	C mount
Weight	50 g

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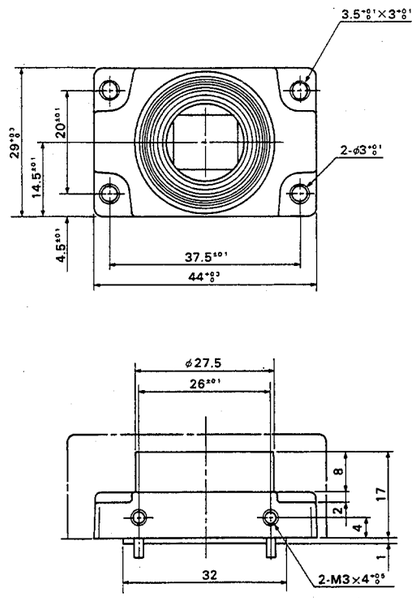
Dimensions:

Camera Module <XC-77CE>

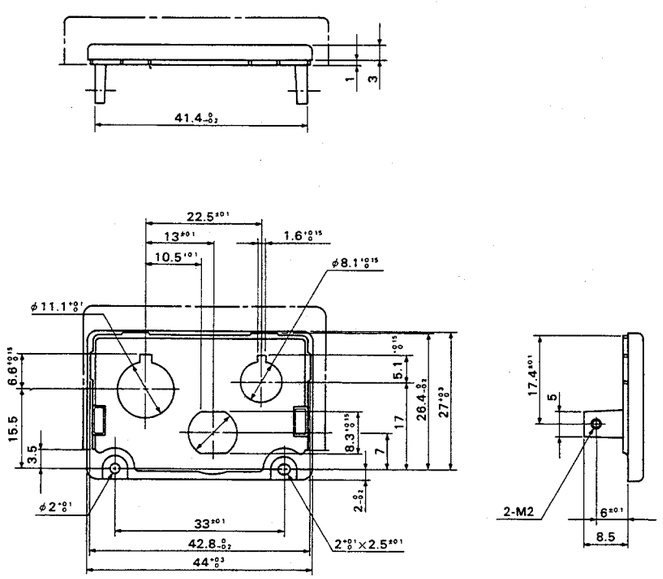


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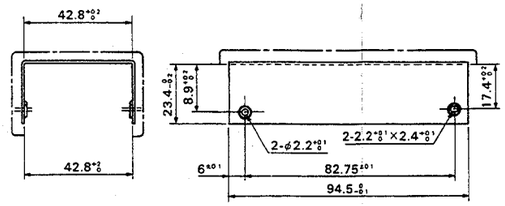
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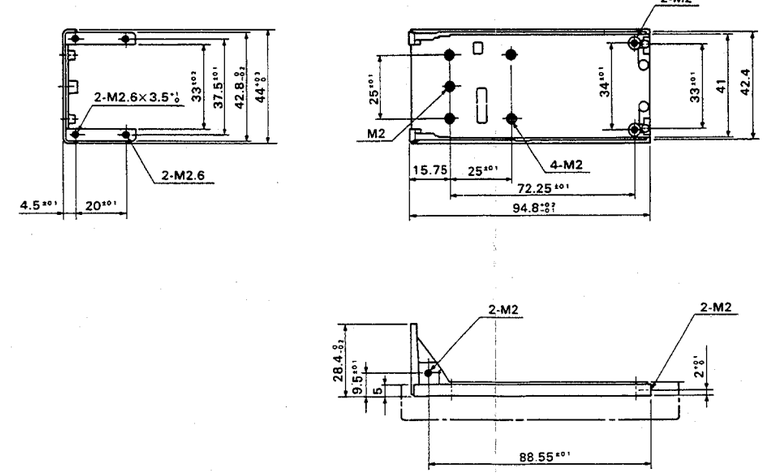
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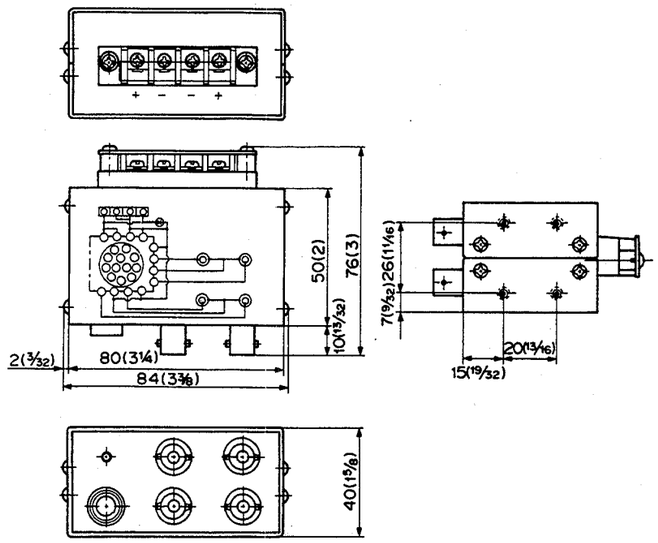


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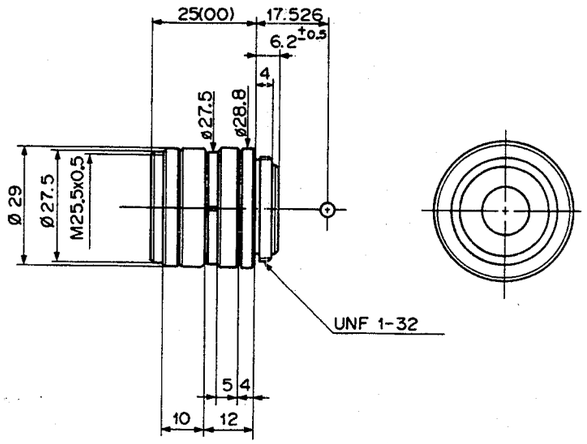


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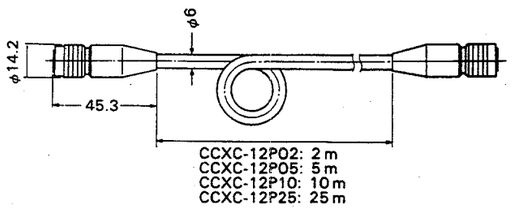
Junction box



Lens

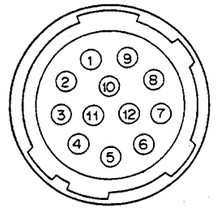


Camera cable



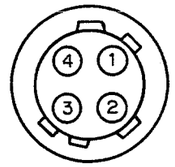
2-2. CONNECTORS' PIN FUNCTION

12-P Multiconnector (External view)



PIN NO.	EXTERNAL SYNC MODE			CAMERA SYNCRONOUS OUTPUT
	HD, VD	VBS/VS	RESTART RESET	
1	GND	GND	GND	GND
2	+12 V	+12 V	+12 V	+12 V
3	VIDEO OUTPUT (GND)	VIDEO OUTPUT (GND)	VIDEO OUTPUT (GND)	VIDEO OUTPUT (GND)
4	VIDEO OUTPUT (SIGNAL)	VIDEO OUTPUT (SIGNAL)	VIDEO OUTPUT (SIGNAL)	VIDEO OUTPUT (SIGNAL)
5	HD INPUT (GND)	—	HD INPUT (GND)	HD INPUT (GND)
6	HD INPUT (SIGNAL)	—	HD INPUT (SIGNAL)	—
7	VD INPUT (SIGNAL)	VBS INPUT (SIGNAL)	RESET PULSE (SIGNAL)	—
8	CLOCK OUTPUT (GND)	CLOCK OUTPUT (GND)	CLOCK OUTPUT (GND)	CLOCK OUTPUT (GND)
9	CLOCK OUTPUT (SIGNAL)	CLOCK OUTPUT (SIGNAL)	CLOCK OUTPUT (SIGNAL)	CLOCK OUTPUT (SIGNAL)
10	GND	GND	GND	GND
11	+12 V	+12 V	+12 V	+12 V
12	VD INPUT (GND)	VBS INPUT (GND)	RESET PULSE (GND)	FIELD INDEX OUTPUT (GND)

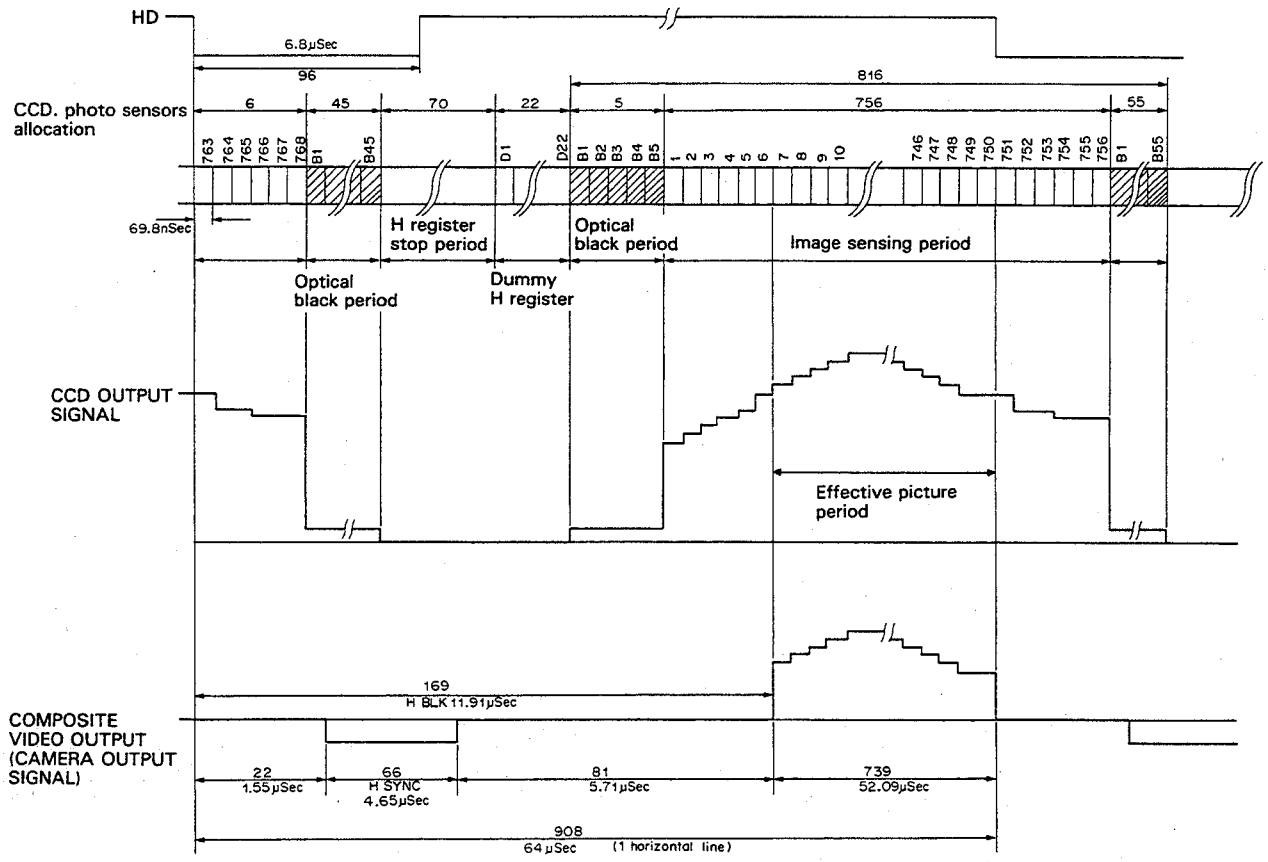
4P Lens Connector (External view)



PIN NO.	SIGNAL	SPECIFICATION
1	+12 V OUT	DC 12 V OUTPUT
2	GND	GND
3	NC	NC
4	VS OUT	VIDEO SIGNAL OUTPUT

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2-3. OUTPUT SIGNAL TIMING CHART



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2-4. External Synchronization

There are three external synchronization modes:
1. VS/VBS mode
2. HD and VD mode
3. RESTART RESET mode

2-4-1. VS/VBS mode

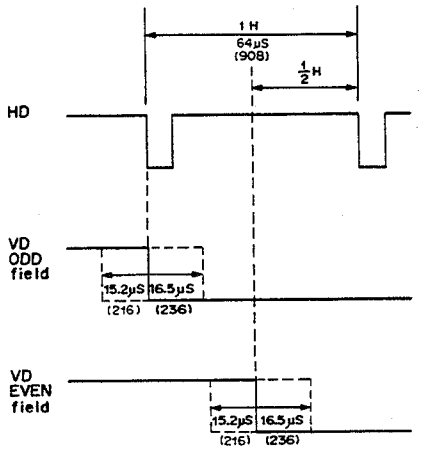
The VS/VBS mode provides external synchronization by supplying a normal composite signal, VS or VBS, to pin 7 of the 12-pin connector.

2-4-2. HD and VD mode

The HD and VD mode provides external synchronization by supplying an HD signal to pin 6 and a VD signal to pin 7 of the 12-pin connector.

- Input conditions of HD and VD signals
- Frequency (period)
  HD: 15.625 kHz ±1% (64 μs ±1%)
  VD: 294 to 1023 1/2 H
  * The maximum number of vertical effective lines is 575 in the interlace mode.
    In the non-interlace mode, it is 287 for both the ODD field and the EVEN field.

- Phase



The figure in parentheses ( ) indicates the number of clock pulses

As shown in the illustration above, the ODD field is provided when the phase shift between the trailing edge of the VD signal and the trailing edge of the HD signal is between a lead of 15.2 μs and a lag of 16.5 μs. The EVEN field is provided when the phase shift between the trailing edge of the VD signal and the point 1/2H from the trailing edge of the HD signal is between a lead of 15.2 μs and a lag of 16.5 μs.

- Interlace and noninterlace

Operation can be performed in either interlace or non-interlace mode by changing the input condition of the VD signal. See Figure 1.

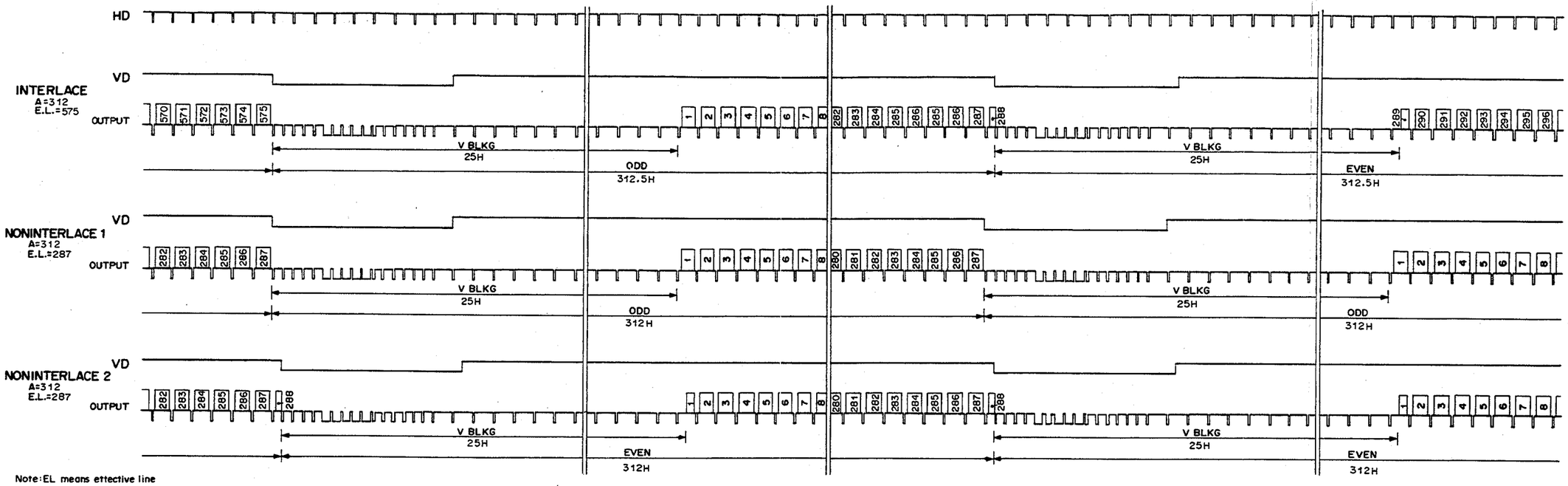
- Interlace

To operate in the interlace mode, set the period of the VD signal to (A + 1/2)H. A is an integer, 294 to 1023. In other words, the phase of the leading edge of the VD signal against the leading edge of the HD signal is changed for each VD signal. The field changes from ODD to EVEN and to ODD, repeatedly during operation in the interlace mode. At this time, the number of scanning lines per frame is 2A + 1.

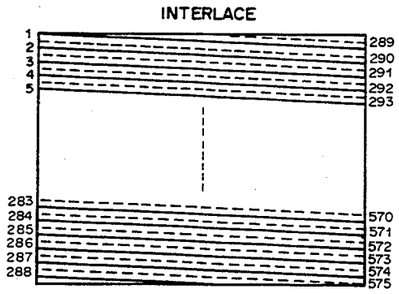
- Non-interlace

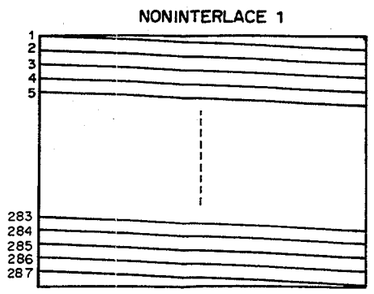
To operate in the non-interlace mode, set the period of the VD signal to A H. A is an integer, 294 to 1023. In other words, the phase of the leading edge of the VD signal against the leading edge of the HD signal is not changed for each VD signal, and the field ODD or EVEN remains unchanged for operation in the non-interlace mode. The number of scanning lines is A; this is half of the number of scanning lines for operation inthe interlace mode. The sensitivity is half of the sensitivity provided in the interlace mode, when the frame is stored.

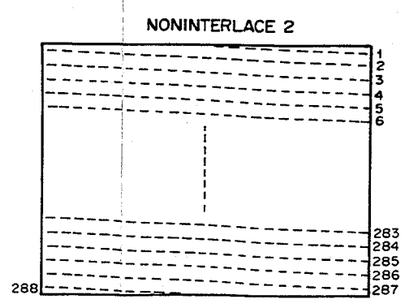
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Note:EL means effective line

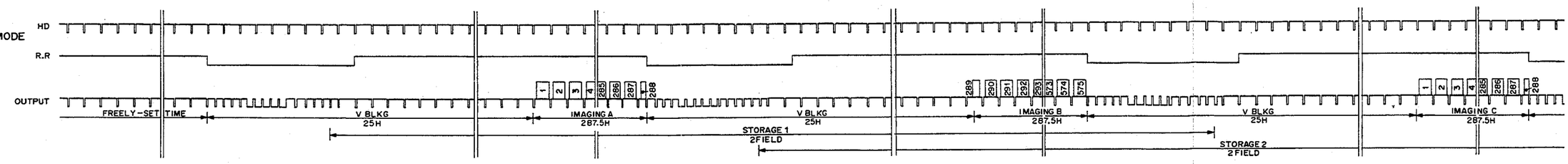




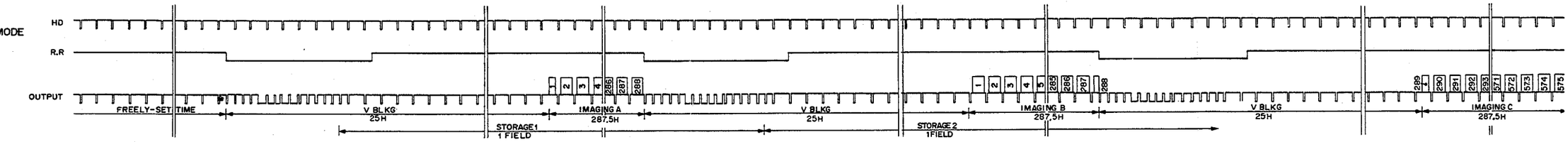


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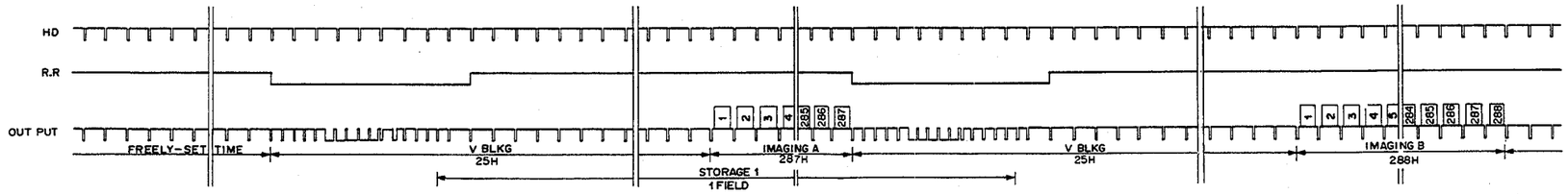
FRAME INTEGRATION MODE
INTERLACE
A=312
E.L=575



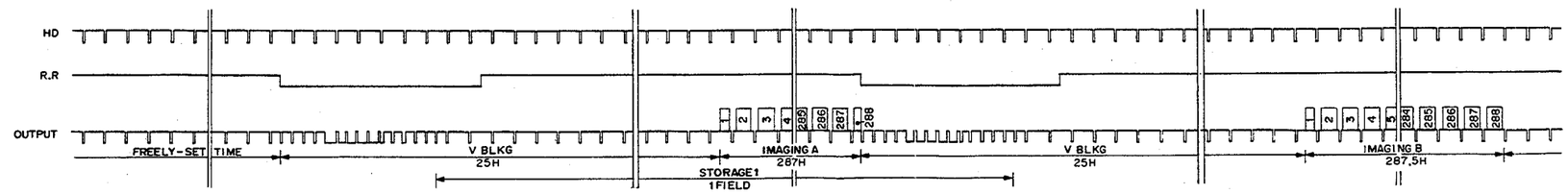
FIELD INTEGRATION MODE
INTERLACE
A=312
E.L=287



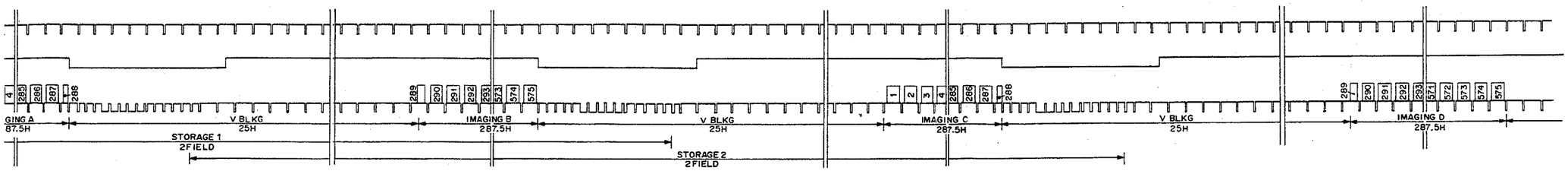
NONINTERLACE 1
A=312
E.L=287

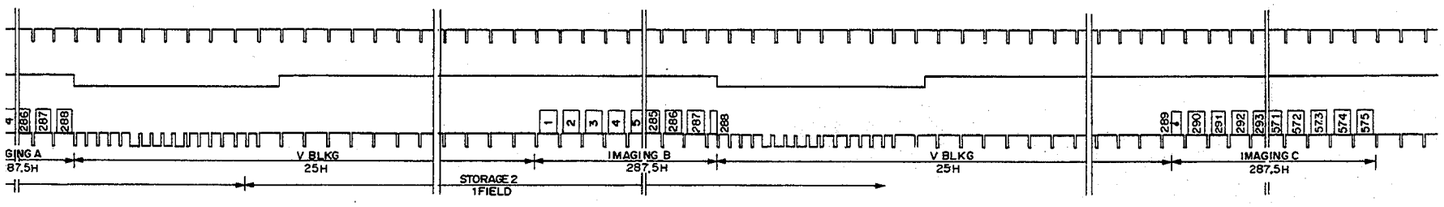


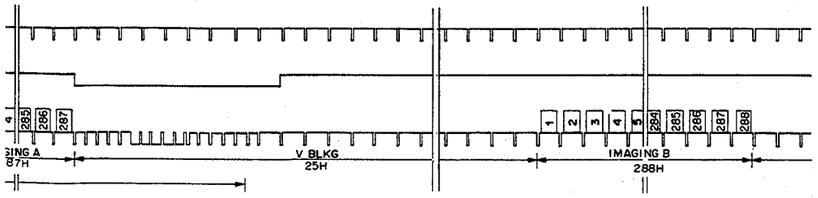
NON INTERLACE2
A=312
E.L=287

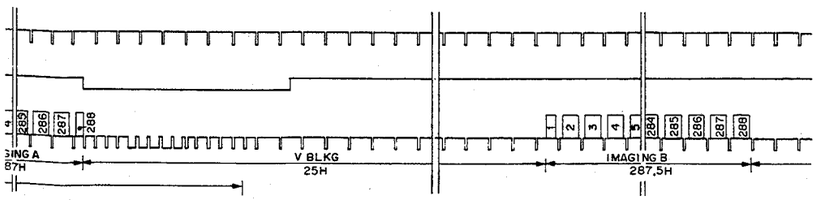


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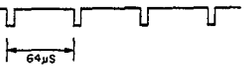
2-4-3. RESTART RESET mode

In the RESTART RESET (RR) mode, information for one screen can be retrieved at any time. It is necessary to internally set the RR mode in the camera to provide the RR mode. See Section 2-5 "Mode Setting". Supply the HD and RR signals to pin 6 and pin 7 of the 12-pin connector to obtain output.

- Input conditions for the HD and RR signals
- Frequency (period)

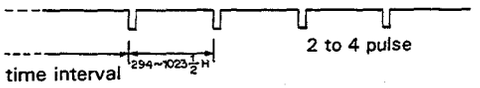
HD signal: 15.625 kHz ±1% (64 μs ±1%)

Continuous pulse



VD signal: 294 to 1023 1/2 H

2 to 4 pulses depending on the mode



- Phase

The same phase conditions as for the HD and VD mode are applied to this mode. See Section 2-4-2.

- Explanation of the timing chart

Figure 2 is the timing charts for each operation mode. The details of these timing charts are given below:

- Frame INTEGRATION interlace mode

The RR requires four pulses. Set the period of the RR to A + 1/2H. A is an integer, 294 to 1023. It is 312 in the figure.
Shooting information during STORAGE 1 and STORAGE 2 is output in the intervals of IMAGING C (ODD) and IMAGING D (EVEN). The CCD is reset in the intervals of IMAGING A and IMAGING B. Therefore, signals output during these intervals are meaningless.

- Field INTEGRATION interlace mode

The RR requires three pulses. Set the period of the RR to A + 1/2H. A is an integer, 294 to 1023. It is 312 in the figure.
Shooting information during STORAGE 1 and STORAGE 2 is output in the intervals of IMAGING B (ODD) and IMAGING C (EVEN). The CCD is reset in the interval of IMAGING A; therefore, signals output during this interval are irrelevant.

- Noninterlace mode

The RR requires two pulses regardless of the storage mode. Set the period of the RR to A H. A is an integer, 294 to 1023. It is 312 in the figure.
Shooting information in STORAGE 1 is output in the interval of IMAGING B. The CCD is reset in the interval of IMAGING A; therefore, signals output during this period are irrelevant.

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2-5. Mode Setting

The XC-77 can switch the operation mode, depending on the use.
The modes are set on the PR-89, SG-119, and MB-136 boards.

PR-89 board

Item	Mode	SHORT	OPEN
AGC	AGC	AGC	FIX
	FIX GAIN	FIX	AGC
γ	1	γ1	γ2
	COMPENSATE	γ2	γ1
WHITE CLIP	γ	γ1	γ2
	WHITE CLIP	γ2	γ1

SG-119 board

Item	Mode	M't	OPEN
EIA/CCIR	EIA	R 7	R 6
	CCIR	R 6	R 7
FRAME/FIELD	FRAME	R 1	R 2
	FIELD	R 2	R 1
FIELD	NORMAL	R23	R28
	INVERSION	R28	R23
RESTART RESET	NORMAL	R24	R29
	RESET	R29	R24
EIA/CCIR	EIA	R27	R22
	CCIR	R22	R27

*The value of resistors R1 and R2 is 1 kΩ.
The value of all resistors is 10 kΩ except R1 and R2.

MB-136 board

Item	Mode	M't	OPEN
RESTART RESET	NORMAL	R35	
	RESET		R35

*The value of resistor R35 is 220 kΩ.

- Explanation of all operation modes

- VIDEO GAIN mode (AGC/FIX GAIN)

Set the gain of the video output signal with this mode.
When it is set to AGC, the automatic gain control functions.
When it is set to FIX GAIN, a fixed gain is obtained.
The setting is performed with the AGC trace on the PR-89 board. To set the gain to AGC, connect the AGC end and disconnect the FIX end. To set the gain to FIX GAIN, connect the FIX end. To set the gain to FIX GAIN, connect the FIX end and disconnect the AGC end.
The factory setting is FIX GAIN.

- Gamma compensation mode (1/COMPENSATION)

Set the gamma correction of the video output signal by this mode. When the gamma is set to COMPENSATE, video signals for which gamma correction is performed are output. When it is set to 1, no gamma correction is performed for video signals. This setting provides video signals proportional to the amount of light from the object.
The setting is performed with the gamma and white clip traces on the PR-89 board. To set COMPENSATE, connect the gamma 2 ends of both gamma and white clip traces, and disconnect the gamma 1 ends. To set 1, connect the gamma 1 ends of both gamma and white clip patterns, and disconnect the gamma 2 end.
The factory setting is 1.

- EIA/CCIR mode (EIA/CCIR)

Set the signal system of the video output signal with this mode.
Always set the signal system to CCIR.

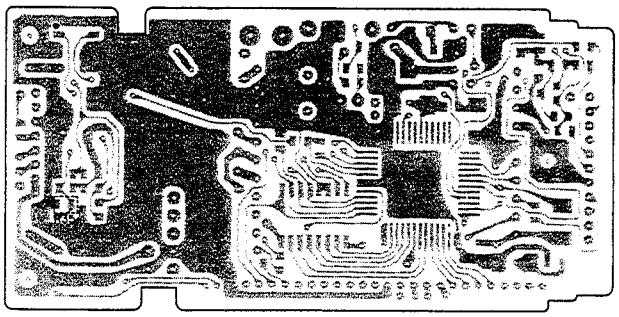
- Storage mode (FRAME/FIELD)

Set the period in which a signal charge is read from the photosensor in the CCD with this mode.
When it is set to FIELD, a signal charge is read for each field. When it is set to FRAME, a signal charge is read for each frame. Note that if the FRAME mode is set for operation in the non-interlace mode, the sensitivity is half of the sensitivity provided in the interlace mode.
The setting is performed with the FRAME/FIELD trace on the SG-119 board.
To set the period to FIELD, mount then R1 (1 kΩ) on the FRAME/FIELD trace, and demount R2.
To set the period to FRAME, mount then R2 (1 kΩ) on the FRAME/FIELD trace and demount R1.
The factory setting is FRAME.

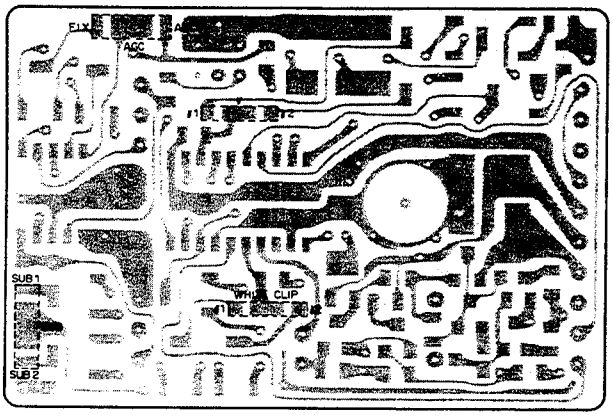
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• RESTART RESET mode (NORMAL/RESET)
Set the external synchronization mode with this mode. When NORMAL is set, the external synchronization mode is set to the VS/VBS mode or HD and VD mode. When RESET is set, the external synchronization mode is set to the RESTART RESET mode. See Section 2-4 External Synchronization for the details of each external synchronization mode.
The setting is performed with the RESTART RESET trace on the SG-119 board and R35 to be mounted on the MB-136 board.
To set NORMAL, mount R24 (10 kΩ) of RESTART RESET and demount R29. Also mount R35 on the MB-136 board.
To set RESET, mount R29 (10 kΩ) of RESTART RESET and demount R24. Also demount R35 on the MB-136 board.
The factory setting is NORMAL.

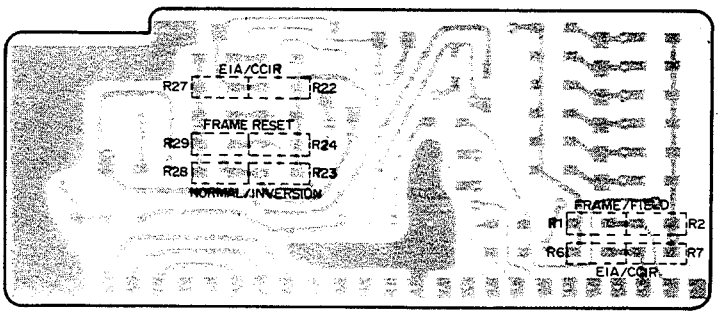
• Field inversion mode (NORMAL/INVERSION)
Set the field inversion operation of the video output signal at external synchronization with this mode.
When INVERSION is set, the field of the video output signal is inverted against the external synchronization signal. In other words, when the field of the external synchronization signal is ODD, EVEN is output and when it is EVEN, ODD is output.
When NORMAL is set, operation is the same as for the normal external synchronization. In other words, when the field of the external synchronization signal is ODD, ODD is output and when it is EVEN, EVEN is output.
The setting is performed with the FIELD trace on the SG-119 board. To set NORMAL, mount R23 (10 kΩ) of FIELD, and demount R28. To set INVERSION, mount R28 (10 kΩ) of FIELD, and demount R23.
The factory setting is NORMAL.



MB-136 BOARD (Soldering Side)



PR-89 BOARD (Soldering Side)



SG-119 BOARD (Soldering Side)

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2-6. THEORY OF OPERATION

<Operation principle of the CCD>

A CCD (Charge Coupled Device) consists of MOS (Metal-Oxide-Semiconductor) capacitors arranged in a regular array.
It basically performs three functions connected with handling charges.

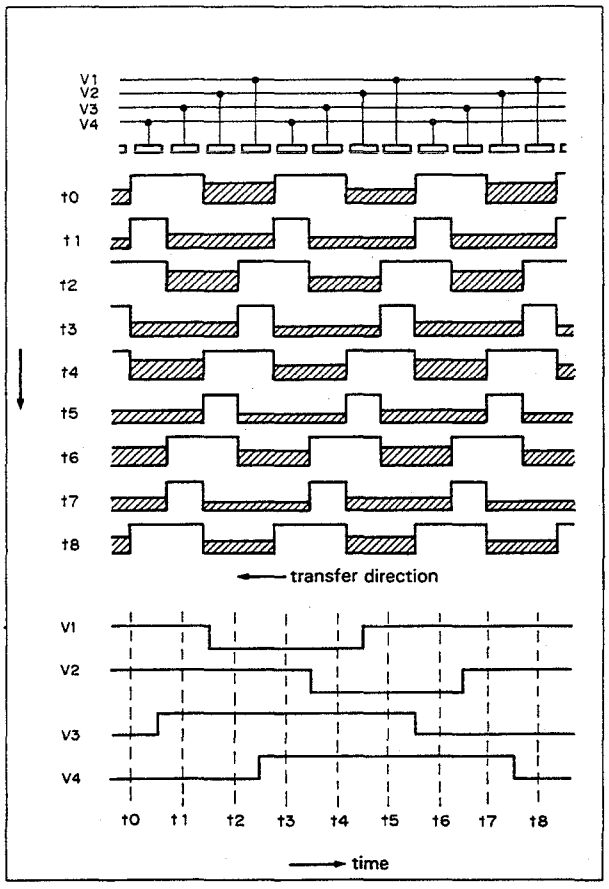
1. Photoelectric conversion (photosensor)
Incident light generates charges on the MOS capacitors, with the quantity of charge being proportional to the brightness.

2. Accumulation of charges
When a voltage is applied to the electrodes of the MOS capacitors, an electric potential well is formed in the silicon layer. The charge is accumulated in this well.

3. Transmission of charge
When a high voltage is applied to the electrodes, a deeper well is formed; when a low voltage is applied, a shallower well is formed, In the CCD, this property is used to transmit the charge. When a high voltage is applied to the electrodes, a deep electric potential well is formed, and charge flows in from neighboring well. When this is repeated over and over among the regularly arranged electrodes, the charge is transferred from ones MOS capacitor to another. This is the principle of CCD charge transmission.

<Mechanism of CCD charge transfer>

1. Vertical transfer
The vertical shift register transfers charges using a four-phase drive mode. Figure 1 shows an example of the changes which can occur in potential wells in successive time intervals.
At to, the electrode voltages are (V1 = V2) > (V3 = V4), so the potential wells are deeper toward the electrode at the higher voltages V1 and V2. Charges accumulate in these deep wells. At t1, the electrode voltages are (V1 = V2 = V3) > (V4), so the charges accumulate in the wells toward the electrode at V1, V2 and V3. At t2, the electrode voltages are (V2 = V3) > (V4 = V1), so the charges accumulate in the wells toward the electrode at V2 and V3.
Electrode voltage states at t3 and after are shown below.
t3 (V2 = V3 = V4) > (V1)
t4 (V3 = V4) > (V1 = V2)
t5 (V4) > (V1 = V2 = V3)
t6 (V4 = V1) > (V2 = V3)
t7 (V4 = V1 = V2) > (V3)
t8 (V1 = V2) > (V3 = V4) (Initial state)
These operations are repeated to execute the vertical transfer.



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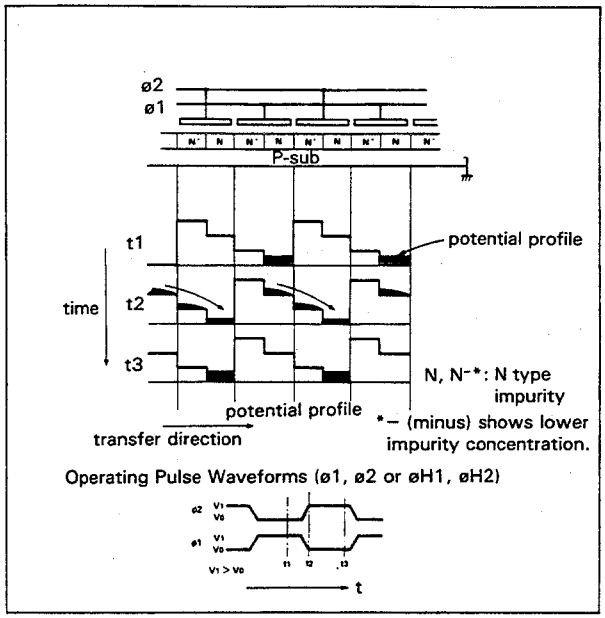
2. Horizontal transfer

The horizontal shift register transfers charges using a two-phase drive mode. Figure 2 shows an example of the changes which can occur in the potential wells in successive time intervals. At t1, the electrode voltages are H1 > H2, so the potential wells are deeper toward the electrode of the higher voltage H1. The charges accumulate in these wells. At t2, the electrode voltages H1 and H2 are inverted, the wells toward the electrode at voltage H2 becomes deeper while the wells toward the electrode at voltage H1 become shallower. So the wells at H2 are deeper than those at H1, the charge flows into the deeper wells toward the electrode at H2. At t3, the electrode voltage have not changed since t2, so the charge flows into the wells at H2 and one transfer of charge is completed. These operations are repeated to execute the horizontal transfer.

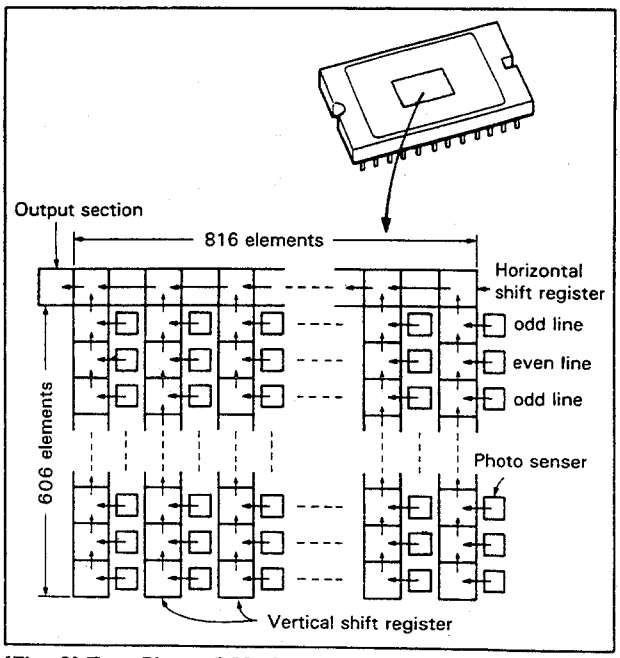
<BI-12 board>

Light which comes through the camera lens strikes the CCD chip surface of IC1 on the BI-12 board. The surface of the CCD contains a number of photosensors.

The array is 816 horizontal photosensors by 606 vertical photosensors, so that there are a total of 494,496. The effective number of them is 756 photosensors by 581 photosensors, so there are total of 439,236. Incident light is converted to a charge (signal charge) at the photosensor in proportion to the brightness of the light. The converted signal charge is read out by a register from the photosensor, and is transferred in sequence and fed to the output section. The register is subdivided into horizontal and vertical shift registers. As shown in Fig. 3, there are 816 vertical rows of registers, while there is only one horizontal row of registers, across the top. Each converted charge is transmitted every field (frequency of VD) to the vertical shift register adjoining to the photosensor. The signal charge is then vertically transferred in sequence at the vertical transfer clock V1, V2, V3 and V4 (frequency of HD) to the horizontal register. The horizontal registers transfer charges horizontally at the horizontal transfer clock H1, H2 (= 908 fh) to the output section. The output section converts the charge to the voltage and outputs it. The signal from IC1 is fed to the SH-27 board via the buffer Q1.



[Fig.1] The interline-transfer organization of the CCD image sensors



[Fig. 2] Two Phase CCD Charge Transfer

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<SH-27 board>
It contains a sample and hold circuit. CCD output signals sent from the BI-12 board are divided into two Both signals are sampled and held by a sampling and holding pulses (SHP, SHD). One signal is sampled and held three times by these pulses; in order of the SHP, SHD and SHP pulses. The other signal is sampled and held two times by the SHD pulse and then SHP pulse. The difference of these two signal removes a noise component of CCD output signal to obtain the video signal, using a differential amplifier consisting of Q16 through Q19. The video signal from the differential amplifier is sent to the PR-89 board.

<PR-89 board>
It contains a video signal processing circuit, which converts the video signal from the SH-27 board into a video signal of CCIR standard. The video signal from the SH-27 board is fed to IC1. IC1 contains an auto-iris circuit and a gain control amplifier for AGC. The signal from the gain control amplifier passes through a low-pass filter FL1 and is then fed to IC2. In IC2, various signal processings such as clamping, gamma correction, white clipping, blanking mixing, setup addition, and sync signal mixing are executed. The resultant signal is then passed through an output driver circuit consisting of Q1 through Q8 and sent from this board.

<CN-163 board>
It connects the MB-136 board with each external connector. 12-pin multiconnector (DC IN/SYNC connector), 4-pin connector (LENS connector) and BNC connector (VIDEO OUT connector) are mounted on this board. At 12-pin multiconnector, +12 V power voltage, external synchronizing signals (EXT HD, EXT VD, RESET PULSE, VBS and VS) are input and the video signal (VS) and synchronizing signals (CLOCK) are output. 12-pin multiconnector I/O signals varies according to selection of sync mode(internal sync or external sync mode). Refer to Section 2-2 in details. +12 V power supply and video signal for auto-iris lens are output from 4-pin connector. The video signal (VS) is output from the BNC connector.

<RG-18 board>
It supplies a DC voltage to be applied to CCD driving clock generator and CCD substrate.

<MB-136 board>
It contains an external synchronizing signal detection circuit, 1816 fh oscillator, DC-to-DC converter and CCD driving clock generator. When external synchronizing signals are supplied to this board, the camera automatically selects external sync mode and outputs a video signal synchronized with the external synchronizing signal. For external synchronizing, EXT VD and EXT HD, or EXT SYNC, or EXT HD and RESET PULSE can be used. When EXT HD and EXT VD, or EXT HD and RESET PULSE are supplied, the MB-136 board wave-shapes these signals using Q1, Q2, Q3 and IC7 and outputs them to the SG-119 board. When EXT SYNC of VBS or VS is supplied, this board detects only a sync component using Q2, Q3 and IC7, and wave-shapes it. The resultant SYNC signal is output to the SG-119 board.
1816 fh oscillator is subdivided into two, which are for external and internal synchronizing. In the internal sync mode, the oscillator using a crystal oscillator (X1) operates. In the external sync mode, the voltage controlled oscillator VCO which is an LC oscillator operates. The VCO can vary oscillation frequency within ±1%. A control voltage of VCO are supplied between 0 V and 5 V. When the control voltage is 2.8 V, the oscillation frequency is set to be 28.375 MHz (= 1816 fh).
The clock signal of 1816 fh is fed to the CCD driving clock generator. The DC-to-DC converter converts the externally-supplied DC (+12 V) into four DC voltages; +15 V, +10 V, +7 V, and +5 V. These voltages are fed to each board.
CCD driving clock generator generates the clock signal necessary to drive the CCD. When the HD and VD signals from the SG-119 board and the clock signal of 1816 fh from the 1816 fh oscillator are fed to IC1.
It outputs the following signals.

CLOCK: The clock signal of 1816 fh (half the clock signal of 1816 fh)

H1, H2: Two-phase clock signal
These are used to drive the horizontal shift register and to transfer the signal charges.

V1 to V4: Four-phase clock signal
These are used to drive the vertical shift register and to transfer the signal charges.

PG: Precharge gate control pulse
A precharge gate is the gate of the output section connected to the horizontal register. This gate is controlled by this pulse to convert a transferred signal charge into the voltage.

SHP, SHD: These pulses are used to sample the CCD output signal.

CLP1: This pulse is used to clamp the optical black level of the CCD output signal.

CCD driving clock signals H1, H2, V1 to V4, and PG are output to the CCD after passing through the drive circuit consisting of IC3, IC5 and IC6.

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<SG-119 board>

It contains synchronizing signal generator. When CLOCK of 908 fh from the MB-136 board is fed to the IC1 and IC2, they outputs the following synchronizing signals.

SYNC: Synchronizing signal
BLKG: Blanking signal
HD, VD: Horizontal and vertical synchronizing signal
FLD: Field index signal
INT/EXT: Sync mode selection signal
Low for internal sync mode, and high for external sync mode.
VCO CONT: A control voltage of VCO for external synchronizing.

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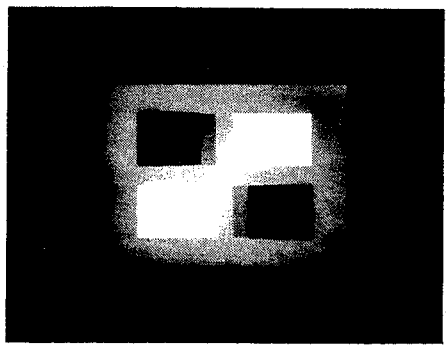
SECTION 3
ALIGNMENT

3-1. PREPARATION

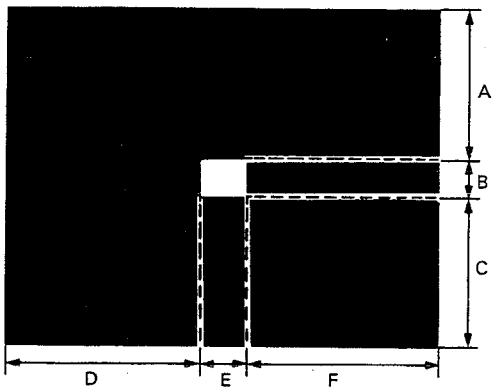
Step 1: Jigs and measuring instruments

- Oscilloscope
- Waveform monitor
- B/W monitor
- Digital voltmeter
- Power supply equipment: Junction box JB-77 (sold on the market), regulated power supply unit
- Tripod attachment: VCT-37 (sold on the market)
- Lens: Standard VCL-16Y-M (sold on the market)
- Pattern box: PTB-500 or PTB-220
  (SONY part No.: J-6029-140-A)

- Grayscale chart
  (SONY part No.: J-6026-130-A)



- White window chart
  Make a hole in black paper as shown in the figure.



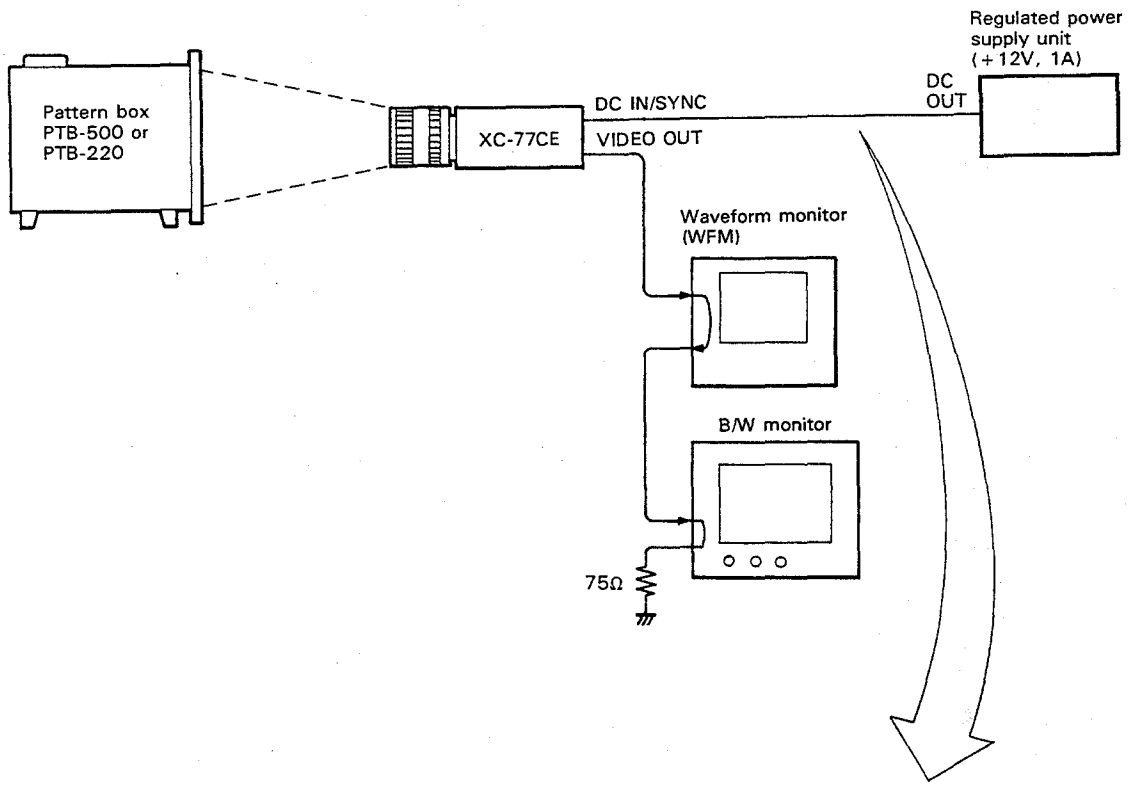
Vertical A:B:C = 4.5:1:4.5
Horizontal D:E:F = 4.5:1:4.5

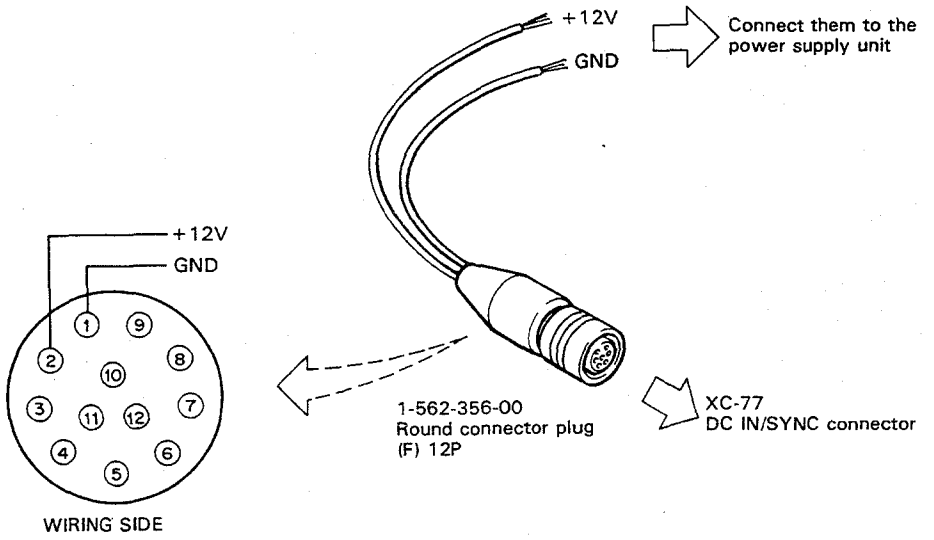
[If the pattern box is unavailable]
- 100-W bulb
- Variable voltage transformer

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Step 2: Connection diagram

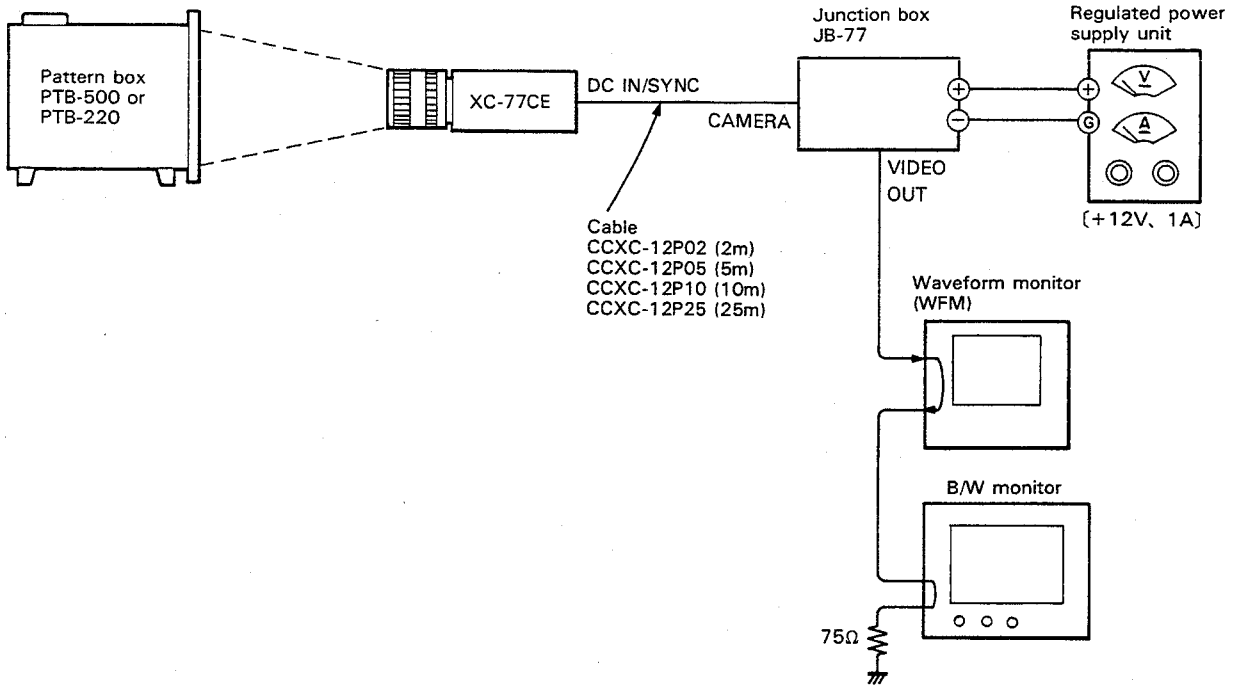
[Connection method 1]



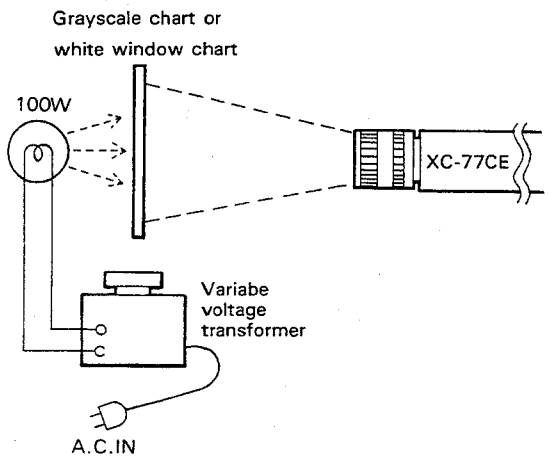


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[Connection method 2]



[If the pattern box is unavailable]
Make adjustment with a simple illuminator as shown below.



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3-2. OVERALL ADJUSTMENT

Step 1: V SUB (field) adjustment

• Caution

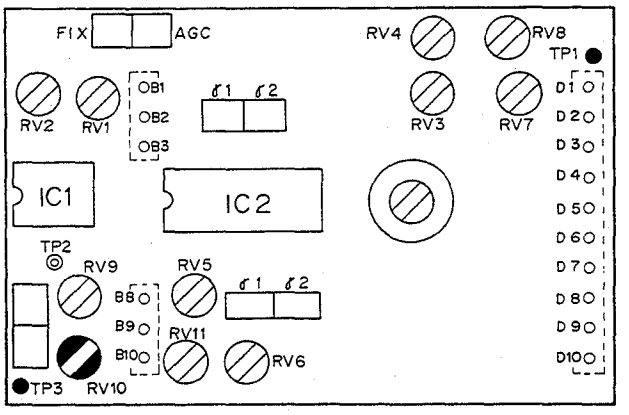
Do not make this adjustment except when the CCD is replaced.

• Setting

Measuring instrument	Digital voltmeter

• Adjustment procedure

1. *Test Point;* TP3 (GND:TP1)/PR-89 board
   Adj. Point: ◐ RV10/PR-89 board
   Spec.: When using a new CCD, adjust the V SUB voltage so that the specification written in the back of the CCD is satisfied.



PR-89 BOARD (Component Side)

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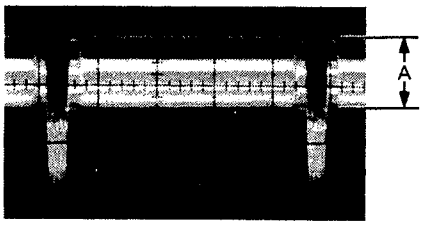
Step 2: Coupling noise elimination adjustment

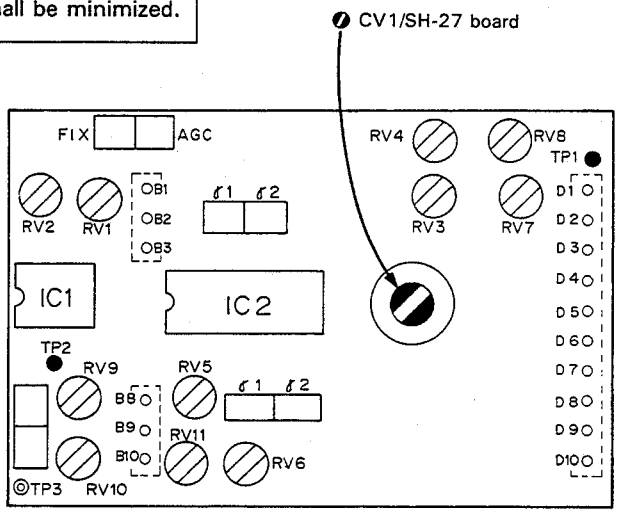
• Setting

Lens iris Measuring instrument	Close it with the lens cap Oscilloscope	Trigger	TP4(HD)/MB-136 board

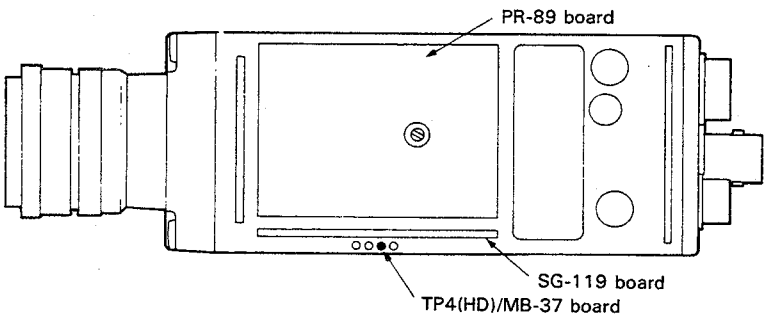
• Adjustment procedure

Test Point/PR-89 board	Adj. Point	Spec.
TP2(GND:TPI)	◐CV1/SH-27 board	A shall be minimized.





PR-89 BOARD (Component Side)



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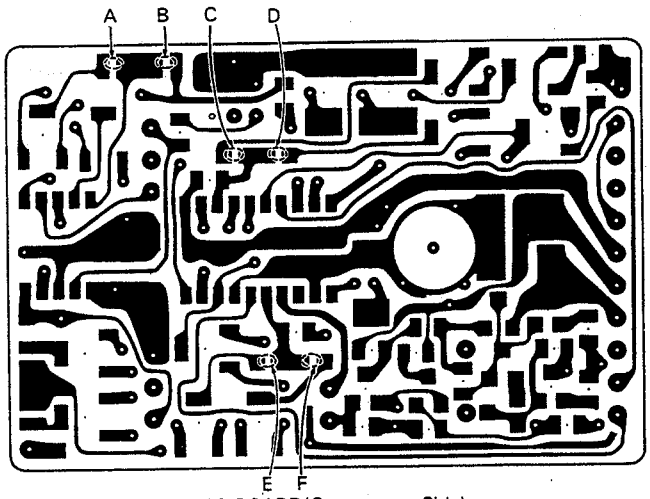
Step 3: PEDESTAL adjustment

• Setting

Lens iris	Close it with the lens cap	Measuring instrument	Waveform monitor (WFM)

• Preparation

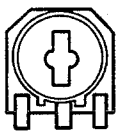
1. Solder parts A, D, and F, and remove the solder from parts B, C, and E.



PR-89 BOARD(Component Side)

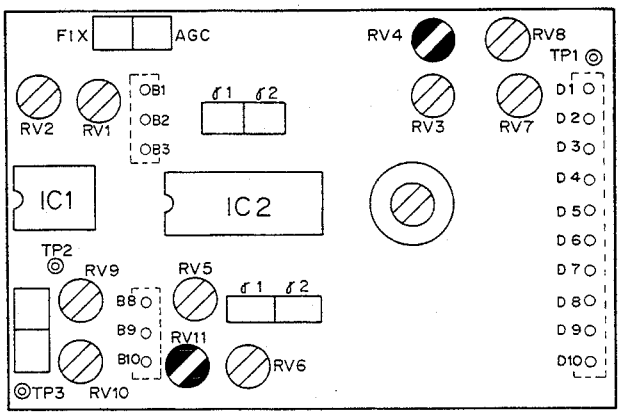
2. Set ◐RV4, ◐RV11/PR-89 on the PR-89 board to the mechanical center.

[Front view]



[Top view]





PR-89 BOARD (Component Side)

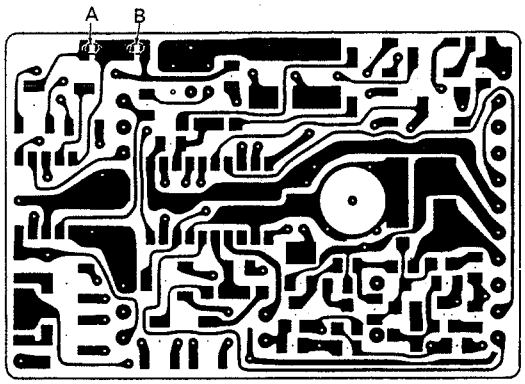
(Continued to next page)

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Step 11: Setting after adjustment

- Setting

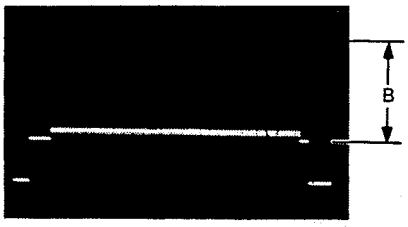
Solder part A and remove the solder from part B as shown in the figure.

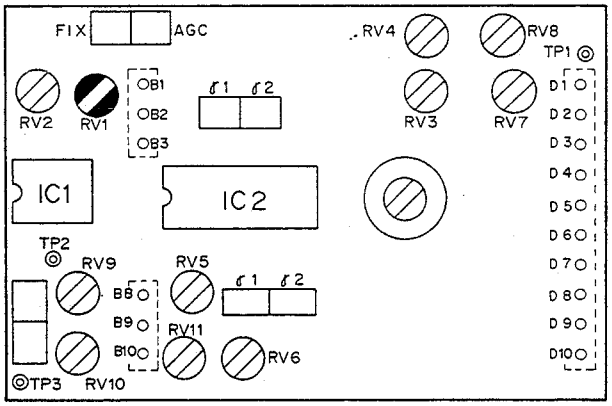


PR-89 BOARD(Component Side)

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3. Test/Point: VIDEO OUT terminal
   Adj. Point: ◐RV1/PR-89 board
   Spec.: B = 700 ± 10 mV





PR-89 BOARD (Component Side)

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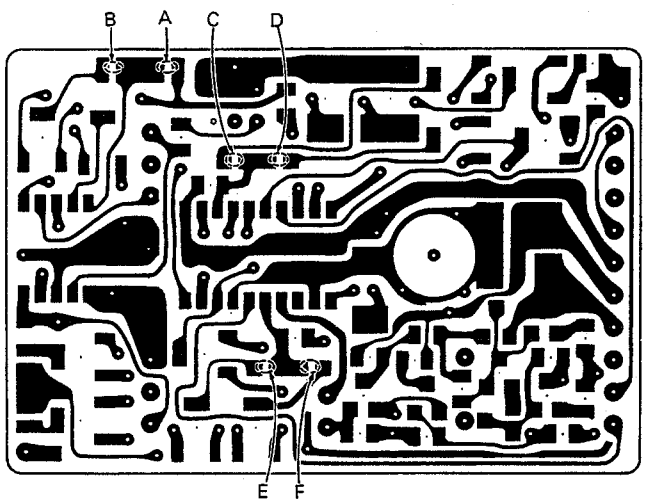
Step 10: GAIN LIMIT adjustment

• Setting

Object	White window chart	Measuring instrument	Oscilloscope and waveform monitor

• Preparation

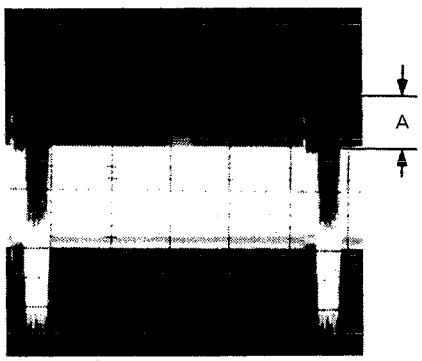
1. Solder parts A, C and E and remove the solder from parts B, D, and F as shown in the figure.



PR-89 BOARD(Component Side)

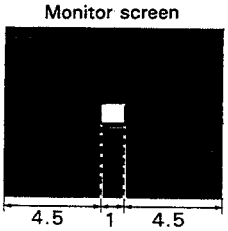
• Adjustment procedure

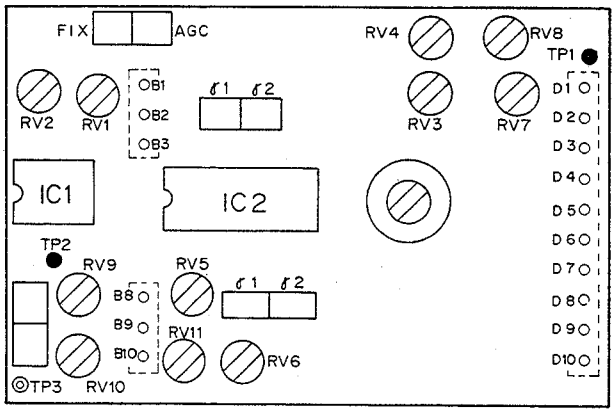
1. Shoot the white window chart as shown in the figure at right.
2. Test Point: TP2 (GND:TP1)/PR-89 board
   Trigger: TP4(HD)/MB-136 board
   Adj. Point: Lens iris
   Spec.: A = 50 ± 10 mV



If the specification cannot be satisfied:
- When the pattern box is PTB-220:
  Adjust the luminance control on the pattern box so that the specification is satisfied.
- When the pattern box is PTB-500:
  Put an ND-4 filter that meets the specification of the lens over the lens, and make readjustment.
- When a 100-W bulb is used:
  Adjust the variable voltage transformer so that the specification is satisfied.

Monitor screen





PR-89 BOARD (Component Side)

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Step 9: White clip adjustment 2

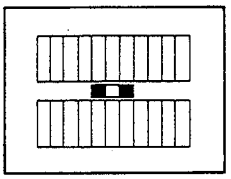
• Setting

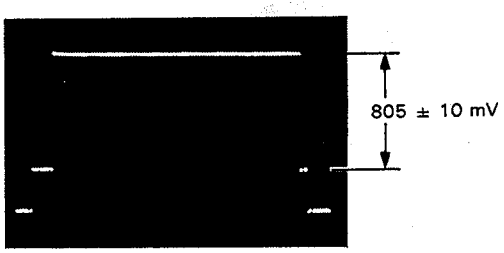
Object	Grayscale chart	Measuring instrument	Waveform monitor (WFM)

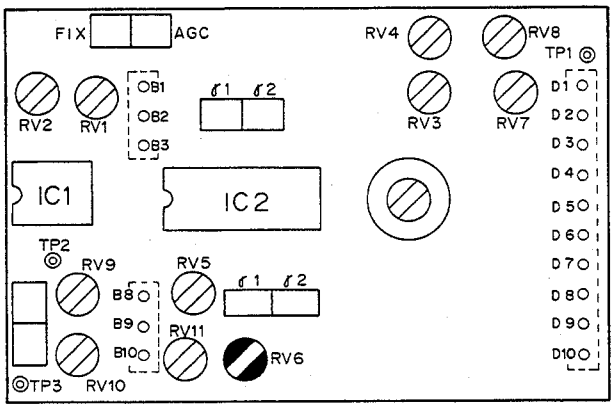
• Adjustment procedure

1. Shoot the grayscale chart, and place the camera so that the chart frame touches the underscanned picture frame on the monitor screen.
2. Test Point: VIDEO OUT terminal
   Adj. Point: ◐ RV6/PR-89 board
   Adjustment: Open the lens iris and adjust so that the VIDEO OUT waveform clips at 805 ± 10 mV.

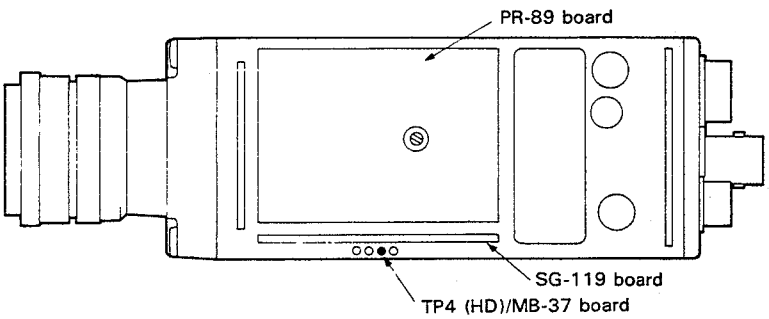
Monitor screen







PR-89 BOARD (Component Side)

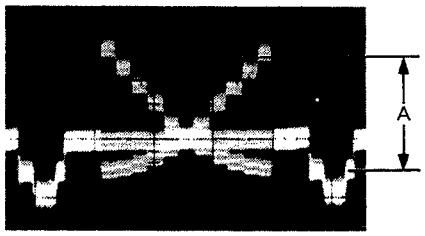


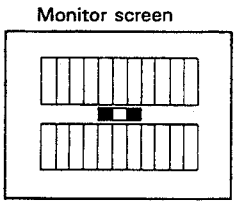
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• Adjustment procedure

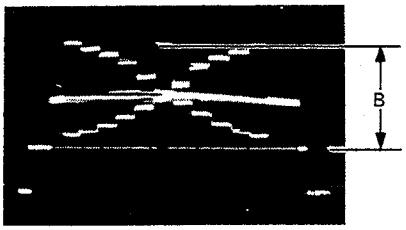
1. Shoot the grayscale chart, and place the camera so that the chart frame touches the underscanned picture frame on the monitor screen.

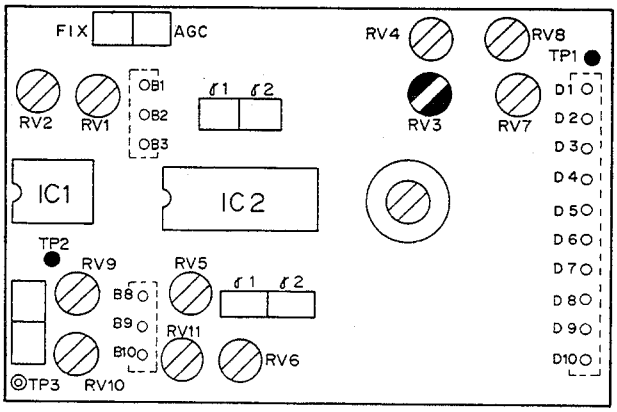
Test Point/PR-89 board	Adj. Point	Spec.
TP2(GND:TPI)	Lens iris	A = 350 ± 10mV





Test Point	Adj. Point	Spec.
VIDEO OUT terminal	◐RV3/PR-89 board	B = 700 ± 10 mV





PR-89 BOARD (Component Side)

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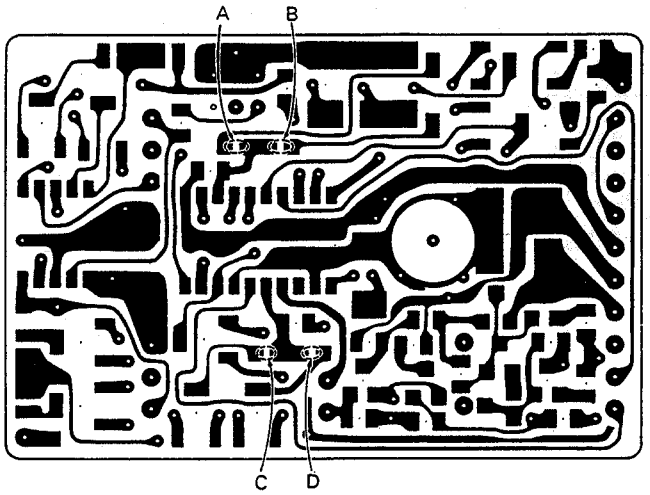
Step 8: Gamma adjustment

• Setting

Object	Grayscale chart	Measuring instrument	Oscilloscope and waveform monitor

• Preparation

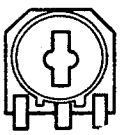
1. Solder parts B and D and remove the solder from parts A and C as shown in the figure.



PR-89 BOARD(Component Side)

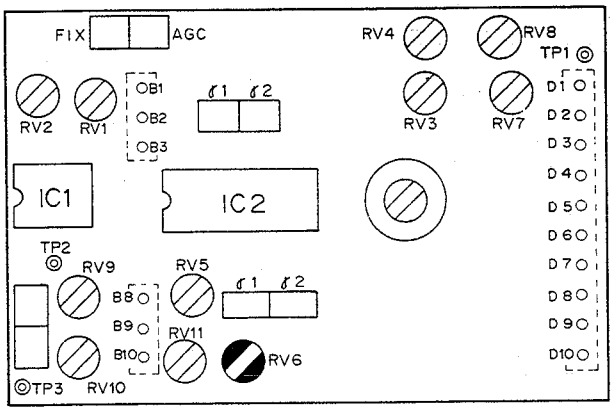
2. Set ⊘RV6/PR-89 on the PR-89 board to the mechanical center.

[Front view]



[Top view]





PR-89 BOARD (Component Side)

(Continued to next page)

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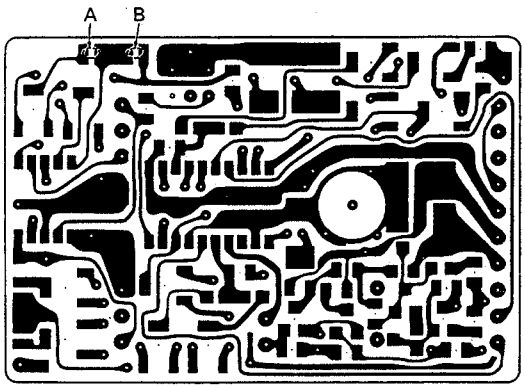
Step 7: White clip adjustment 1

• Setting

Object	Grayscale chart	Measuring instrument	Waveform monitor (WFM)

• Preparation

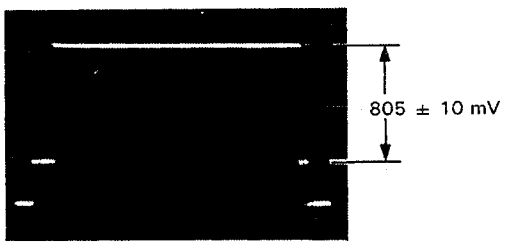
Solder part A and remove the solder from part B as shown in the figure.

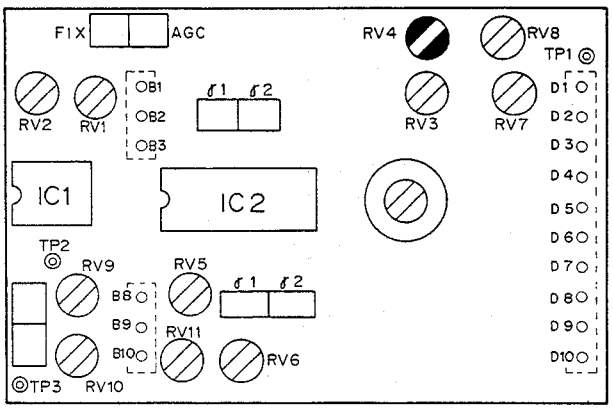


PR-89 BOARD(Component Side)

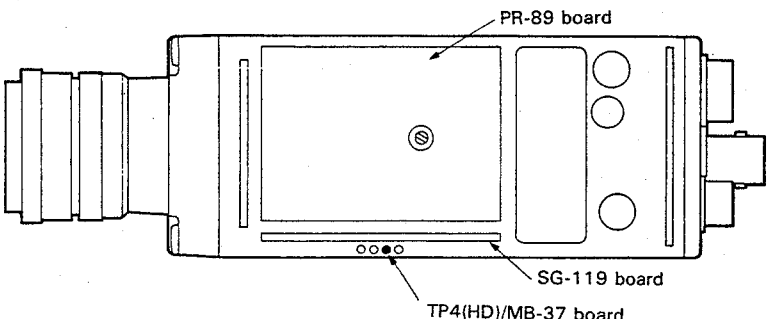
• Adjustment procedure

1. Shoot the grayscale chart, and place the camera so that the picture frame of the camera touches the underscanned picture frame on the monitor screen.
2. Test Point: VIDEO OUT terminal
   Adj. Point: ◐RV4/PR-89 board
   Adjustment: Open the lens iris, and adjust so that the VIDEO OUT waveform clips at 805 ± 10 mV.





PR-89 BOARD (Component Side)



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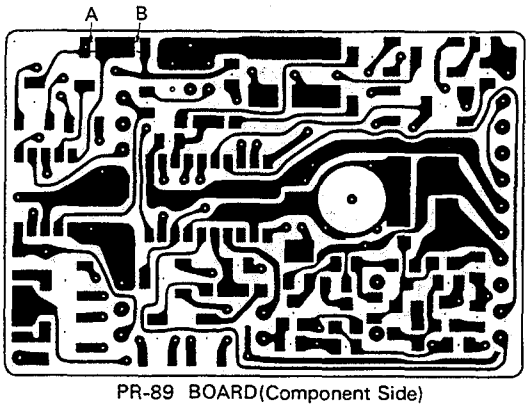
Step 6: AGC adjustment

• Setting

Object	Grayscale chart	Measuring instrument	Oscilloscope and wave-form monitor

• Preparation

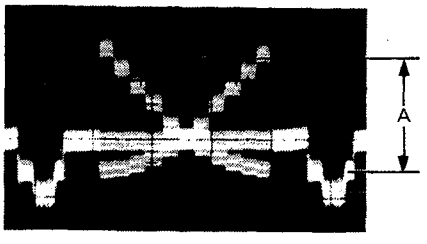
Solder part B and remove the solder from part A as shown in the figure.



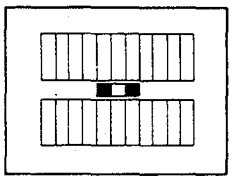
PR-89 BOARD(Component Side)

• Adjustment procedure

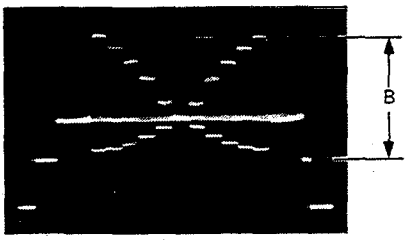
1. Shoot the grayscale chart, and place the camera so that the picture frame of the chart touches the underscanned picture frame on the monitor screen.
2. Test Point: TP2 (GND:TP1)/PR-89 board
   Trigger: TP4(HD)/MB-136 board
   Adj. Point: Lens iris
   Spec.: A = 350 ± 10 mV

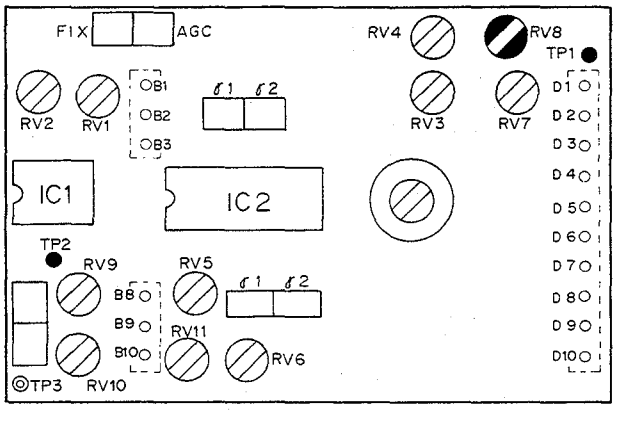


Monitor screen



3. Test Point: VIDEO OUT terminal
   Adj. Point: ◐RV8/PR-89 board
   Spec.: B = 700 ± 10 mV

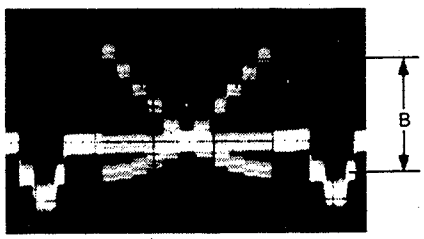


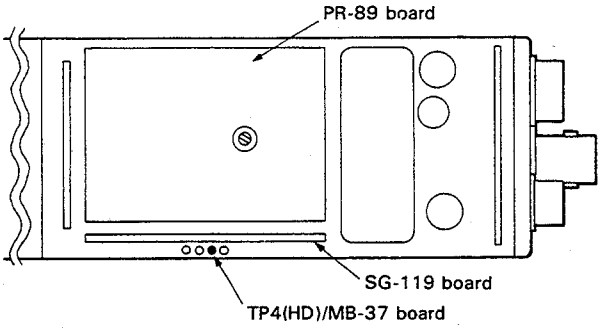


PR-89 BOARD (Component Side)

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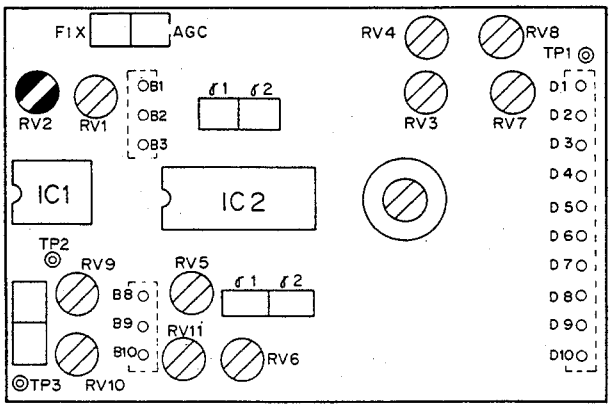
4. Test Point: TP2 (GND:TP1)/PR-89 board
   Trigger: TP4(HD)/MB-136 board
   Adj point: Lens iris
   Spec.: B = 350 ± 10 mV





5. Test/Point: VIDEO OUT terminal
   Adj. Point: RV2/PR-89 board
   Spec.: C = 700 ± 10 mV





PR-89 BOARD (Component Side)

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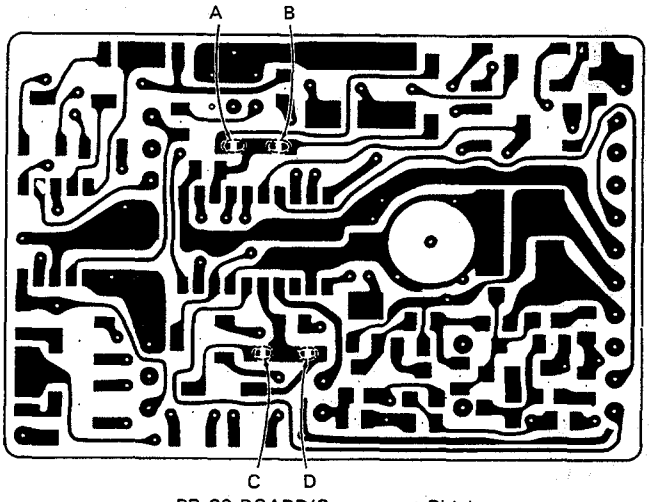
Step 5: GAIN adjustment

• Setting

Object	Grayscale chart	Measuring instrument	Oscilloscope and wave-form monitor

• Preparation

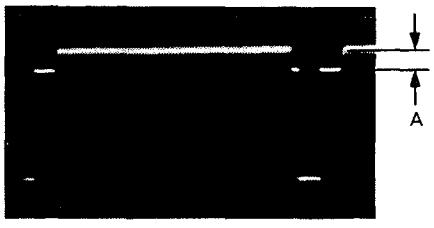
1. Solder parts A and C and remove the solder from parts B and D as shown in the figure.

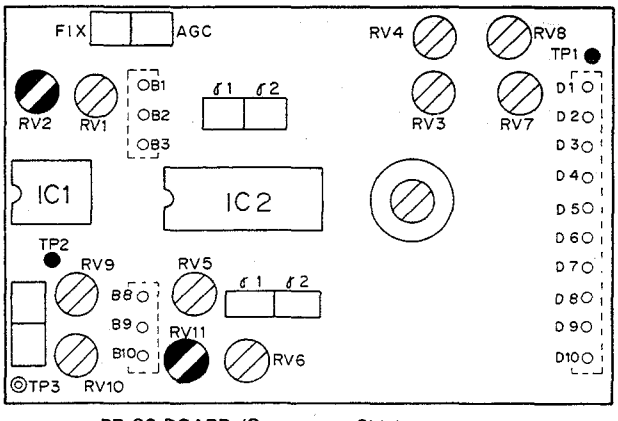


PR-89 BOARD(Component Side)

• Adjustment procedure

1. Lens iris ⇨ Close it with the lens cap
2. Test point: VIDEO OUT terminal
   Adj. Point: ◐RV11/PR89 board
   Spec.: A = 20 ± 5 mV

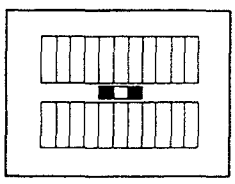




PR-89 BOARD (Component Side)

3. Shoot the grayscale chart, and place the camera so that the chart frame touches the underscanned picture frame on the monitor screen.

Monitor screen



(Continued to next page)

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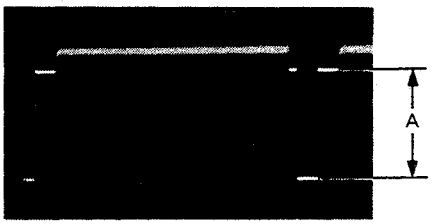
Step 4: SYNC adjustment

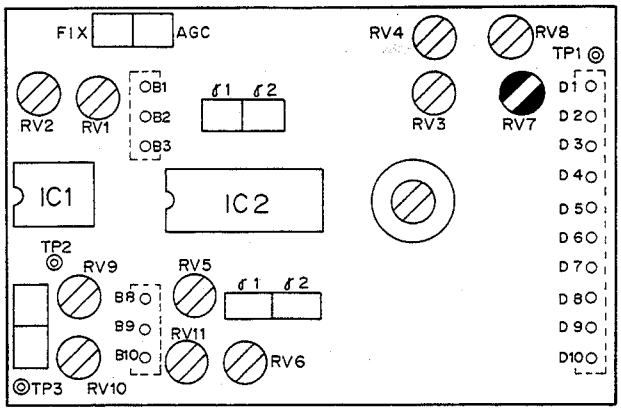
• Setting

Measuring instrument	Waveform monitor (WFM)

• Adjustment procedure

Test Point	Adj. Point	Spec.
VIDEO OUT terminal	◐RV7/PR-89 board	A = 300 ± 10 mV



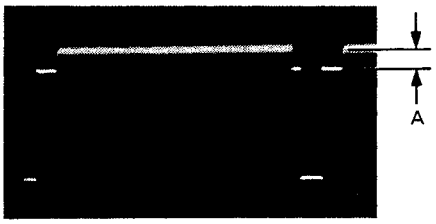


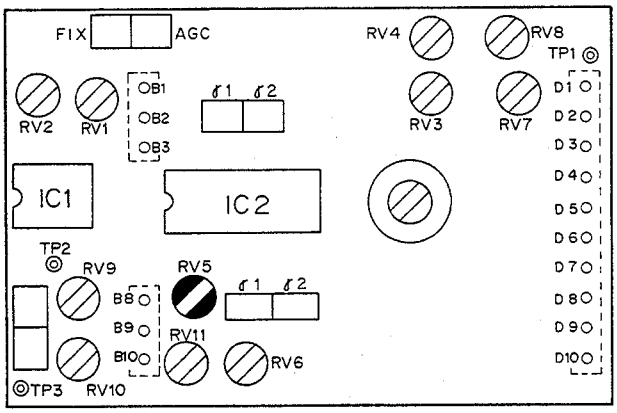
PR-89 BOARD (Component Side)

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• Adjustment procedure

Test Point	Adj. Point	Spec.
VIDEO OUT terminal	◐RV5/PR-89 board	A = 20 ± 5 mV





PR-89 BOARD (Component Side)

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目次

1. 取り扱い操作

1-1. 概要…… 1-1(J)

1-2. 構成…… 1-2(J)

1-3. 各部の名称と使いかた…… 1-3(J)

1-3-1. CCD ビデオカメラモジュール XC-77/77CE… 1-3(J)

1-3-2. 三脚アタッチメント VCT-37…… 1-5(J)

1-3-3. ジャンクションボックス JB-77…… 1-6(J)

1-4. 接続例…… 1-8(J)

1-4-1. ジャンクションボックスを使用する場合…… 1-8(J)

1-4-2. ジャンクションボックスを使用しない場合… 1-9(J)

1-5. モードの初期設定…… 1-10(J)

1-6. 使用上のご注意…… 1-10(J)

1-7. CCD特有の現象…… 1-11(J)

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2. 製品仕様

2-1. 仕様……2-1
2-2. コネクターの入出力信号……2-6
2-3. CCD出力波形タイミングチャート……2-7
2-4. 外部同期について……2-8
2-4-1. VS/VBSモード……2-8
2-4-2. HD.VDモード……2-8
2-4-3. RESTART RESETモード……2-15
2-5. モード設定……2-16
2-6. 動作説明……2-18

3. 調整要項

3-1. 準備……3-1
ステップ1. 使用機械……3-1
ステップ2. 接続図……3-2
3-2. 総合調整……3-4
ステップ1. V SUB(field)調整……3-4
ステップ2. V SUB(frame)調整……3-5
ステップ3. カップリング・ノイズ除去調整……3-6
ステップ4. SET UP調整……3-7
ステップ5. SYNC調整……3-9
ステップ6. GAIN調整……3-10
ステップ7. AGC調整……3-12
ステップ8. ホワイトクリップ調整……3-13
ステップ9. ガンマ調整……3-14
ステップ10. ホワイトクリップ調整2……3-16
ステップ11. GAIN LIMIT調整……3-17
ステップ12. 調整後のセッティング……3-19

A. DIAGRAM

A-1. BLOCK DIAGRAM A-1
A-2. MOUNTING DIAGRAM A-4
A-3. SCHEMATIC DIAGRAM A-7

B. SEMICONDUCTOR

C. SPARE PARTS

C-1. PARTS INFORMATION C-1
C-2. ELECTRICAL PARTS C-2
C-3. EXPLODED VIEW SCREW C-9

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第1章
取り扱い操作

1-1. 概要

XC-77/77CEは，カメラ用の固体撮像素子CCD (Charge Coupled Device) を採用した白黒ビデオカメラモジュールです。

高画質化

768×493 (XC-77)/753×581 (XC-77CE) 画素の画面により，きめ細かな画像を再現します。
また，XC-77CEは画素の縦横の配列が等間隔になっておりアドレスがしやすく，正確なアドレシングが要求される画像処理システムに適しています。

多様な信号処理方式に対応

用途に応じて，GAINはAGC (Automatic Gain Control) と固定GAIN，γは補正と1の選択が内部切り換えにより可能です。
また，内部切り換えで電荷の蓄積モードをフレームからフィールドに切り換えることもできますので，外部同期入力にノンインターレースモードを設定する信号を入力すると，感度が上がり，インターレースモードと同一の感度を得ることも可能です。

3種類の外部同期が可能

外部の同期信号発生器から，次の3種類の信号によってほかのカメラと同期させることができます。なお引き込み周波数範囲は，水平周波数の±1%と広くとってあります。

HD，VD信号：HD，VD信号からインターレース方式かノンインターレース方式かを自動的に識別し，その方式に応じて外部同期をかけます。

VBS (Video, Burst, Sync) 信号：VBS信号 (BB信号，または複合同期信号) によって同期をかけます (HD，VD信号による同期方式とVBSによる同期方式は自動的に入力信号で切り換えられます)。

リセットパルス：レジスタの内容を任意のタイミングで読み出したいとき，所定のリセットパルスによりこのタイミングをコントロールすることができます。

内部同期信号出力

クロック信号は常時出力されていますが，HD信号およびフィールドインデックス信号 (FLD信号，VD信号，複合同期信号のいずれか) は，機内配線を変更することによって12Pコネクターより出力することができます。

堅牢な筐体

アルミダイキャストおよび鉄板で構成されています。筐体固定時に基準となる面にネジ穴が設けてあり，これを利用することにより光軸のずれを最小限にとどめることができます。

XC-37シリーズと交換可能

横断面の外形寸法を始め，VIDEO OUT端子の種類や12ピン・マルチコネクターのピン配置もXC-37シリーズと共通していますので，XC-37シリーズのカメラモジュールのあとに，そのまま設置することができます。

長寿命・高信頼性

画像ひずみが少なく，精度の高い画像

低残像で焼き付きのない，見やすい画像

優れた耐振動・衝撃性

クイックスタート

強磁界でも乱れない画像

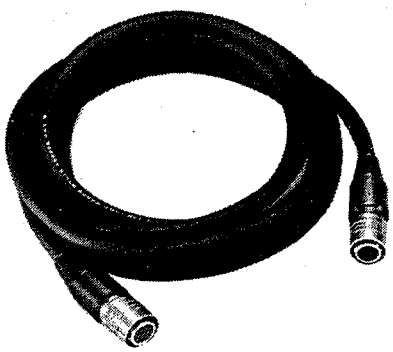
低消費電力 2.2W

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1-2. 構成

CCD ビデオカメラモジュール XC-77/77CE を中心としたシステムの構成は次の通りです。(それぞれが別売りになっています。)

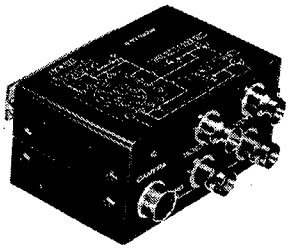
カメラケーブル
CCXC-12P02 (2 m)
CCXC-12P05 (5 m)
CCXC-12P10 (10 m)
CCXC-12P25 (25 m)



CCD ビデオカメラ
モジュール XC-77/77CE



ジャンクションボックス JB-77



標準レンズ
VCL-16Y-M



12 ピンコネクター PC-XC12



4 ピンコネクター PC-XC04

三脚アタッチメント
VCT-37



CCD ビデオカメラモジュール XC-77/77CE

標準レンズ VCL-16Y-M

f=16 mm, F1.4 の標準レンズで，絞りとピント合わせは手動です。

ジャンクションボックス JB-77

カメラケーブル CCXC-12P02/12P05/12P10/12P25 を使ってカメラモジュールと接続し，電源の供給や映像信号の送出および外部同期信号の授受を行います。

4 ピンコネクター PC-XC04

オートアイリスレンズのレンズコードをカメラモジュール XC-77/77CE の LENS 端子に接続するために使用します。

12 ピンコネクター PC-XC12

カメラモジュールの DC IN/SYNC 端子に接続するためのプラグで，システム用に準備されたものです。

三脚アタッチメント VCT-37

三脚を使ってカメラモジュールを固定するとき，このアタッチメントをカメラモジュールの底部に取り付けます。

カメラケーブル CCXC-12P02 (2 m)/12P05 (5 m)/12P10 (10 m)/12P25 (25 m)

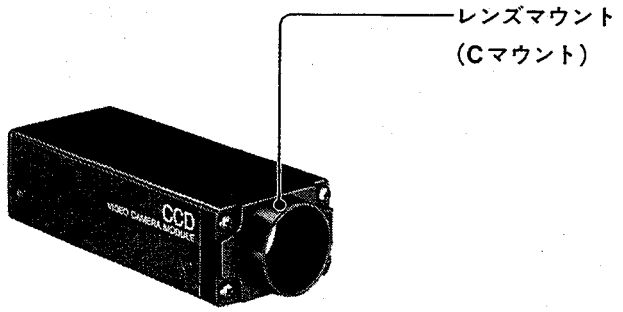
カメラモジュール裏面の DC IN/SYNC 端子に接続し，電源の供給や映像信号の送出および同期信号の授受を行います。

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1-3. 各部の名称と使いかた

1-3-1. CCD ビデオカメラモジュール XC-77/77CE

前面

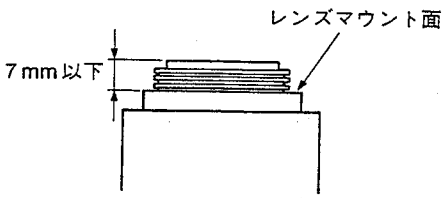


レンズマウント(Cマウント)

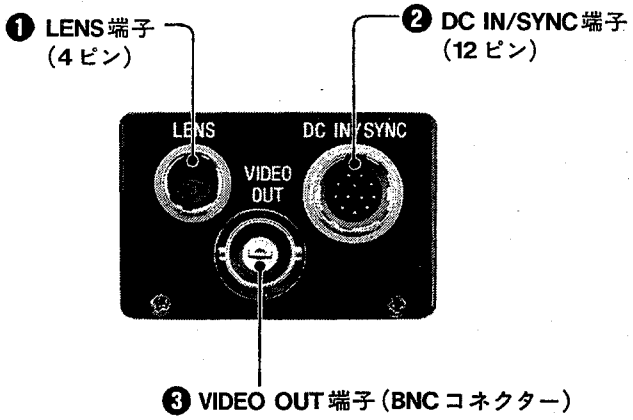
標準レンズVCL-16Y-Mなど，Cマウント式のレンズや光学機器を取り付けます。

ご注意

Cマウント式のレンズは，レンズマウント面からの飛び出し量が7mm以下のものを使用してください。



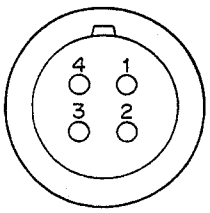
裏面



❶ LENS(レンズ)端子(4ピン)

オートアイリスレンズのプラグを接続すると，レンズの絞りを自動調整することができます。

この端子のピン配置は下図のとおりです。



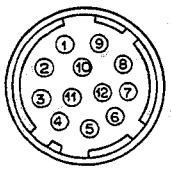
ピン番号	信　号
1	+12V
2	アース
3	——
4	映像信号

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❷ DC IN/SYNC (DC電源入力/同期信号) 端子 (12 ピン)

カメラケーブル CCXC-12P02/12P05/12P10/12P25 を接続し，DC＋12 V の電源の供給を受けるとともにカメラモジュールからの映像信号を出力します。また，同期信号発生器を接続して外部同期信号 (VBS，VS または BS，HD/VD) を入力すると，カメラモジュールを外部同期で動作させることができます。

この端子のピン配置は下図のとおりです。



信号 ピン番号	外部同期モード			CAMERA 同期出力
	HD, VD	VBS/VS	RESTART RESET	
1	アース	アース	アース	アース
2	＋12 V	＋12 V	＋12 V	＋12 V
3	映像出力（アース）	映像出力（アース）	映像出力（アース）	映像出力（アース）
4	映像出力（信号）	映像出力（信号）	映像出力（信号）	映像出力（信号）
5	HD 入力（アース）	—	HD 入力（アース）	HD 出力（アース）
6	HD 入力（信号）	—	HD 入力（信号）	HD 出力（信号)*
7	VD 入力（信号）	VBS 入力（信号）	RESET PULSE（信号）	FIELD INDEX 出力（信号)*
8	—	—	—	CLOCK 出力（アース）
9	—	—	—	CLOCK 出力（信号）
10	アース	アース	—	アース
11	＋12 V	＋12 V	—	＋12 V
12	VD 入力（アース）	VBS 入力（アース）	RESET PULSE（アース）	FIELD INDEX 出力（アース）

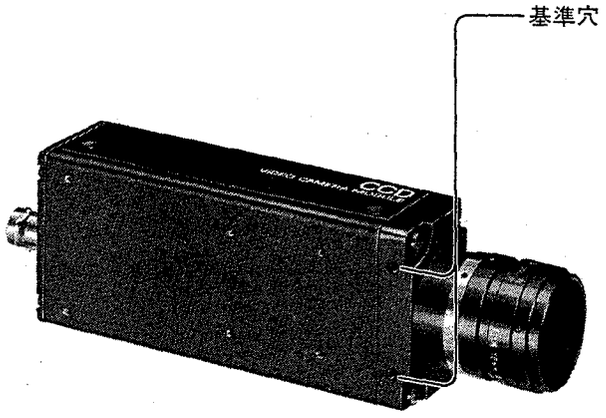
*HD, FIELD INDEX 信号出力を得るにはカメラ内部配線の変更が必要です。

❸ VIDEO OUT (映像出力) 端子 (BNC コネクター)

カメラモジュールからの映像信号を出力します。DC IN/SYNC 端子にカメラケーブル CCXC-12P02 を接続した場合で，CCXC-12P02 の 12 ピンコネクターの映像出力を 75Ω終端しない場合にのみ，この端子を使用できます。

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底面



基準穴

カメラモジュール固定用に高い精度で切られたネジ穴です。ここでモジュールを固定すると，光軸のずれを最小限にとどめることができます。

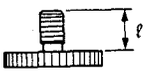
寸法など詳しくは第2章以後をご覧ください。

1-3-2. 三脚アタッチメント VCT-37

三脚の取り付け部のネジは次の規格のものを使用してください。

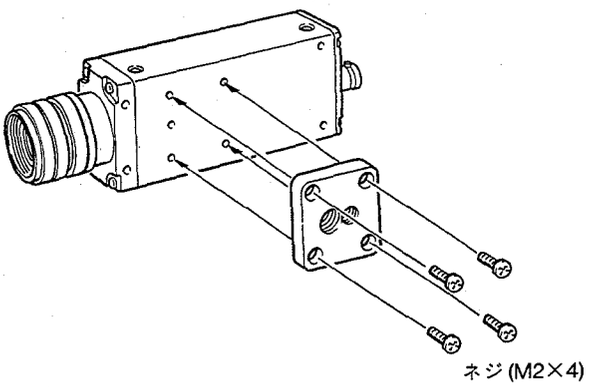
ISO 規格　ℓ＝4.5 mm ±0.2 mm

ASA 規格　ℓ＝0.197 インチ



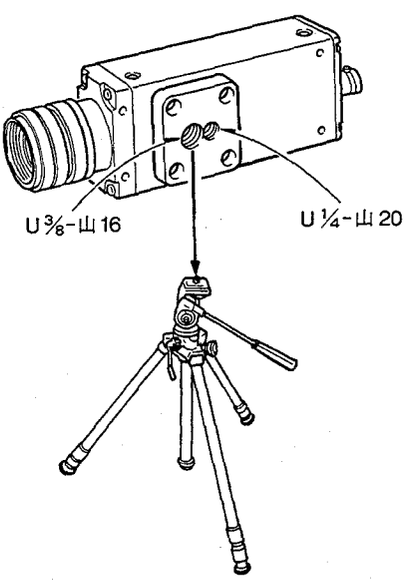
取り付けかた

1



ネジ (M2×4)

2

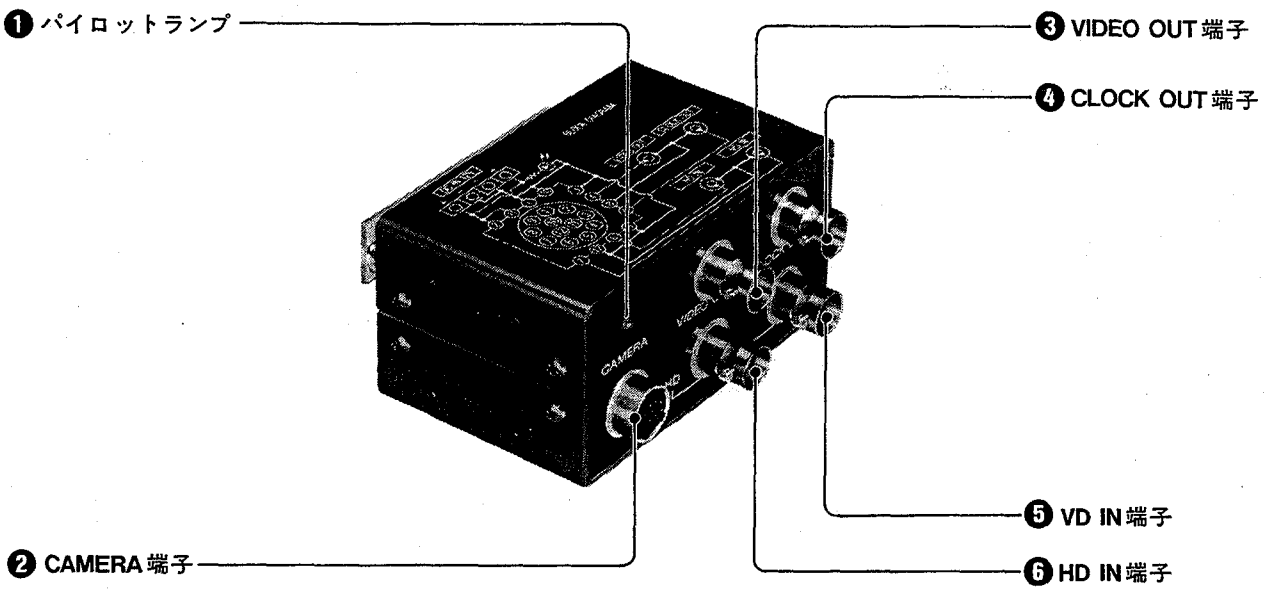


ご注意

三脚アタッチメントを CCD ビデオカメラモジュールに取り付けるときは，長さ 4 mm 以内のネジをご使用ください。ネジが長すぎると，カメラモジュール内の基板に傷をつける恐れがあります。

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1-3-3. ジャンクションボックス JB-77



❶ パイロットランプ

DC 12Vの電源が入ると点灯します。

❷ CAMERA（カメラ）端子（12 ピン）

カメラケーブルCCXC-12P02/12P05/12P10/12P25を接続し，カメラモジュールへDC 12Vの電源の供給と外部同期信号の送出を行うとともに，カメラモジュールから映像信号を入力します。

❸ VIDEO OUT（映像出力）端子（BNC コネクター）

ビデオモニター，VTRなどに接続し，カメラモジュールからの映像信号を出力します。

❹ CLOCK OUT（内部同期信号出力）端子

カメラモジュールを単独で使用する場合，クロック信号を出力します。

❺ VD IN端子（BNC コネクター）

同期信号発生器を接続して，VD信号またはVBS信号を入力します。これにより，カメラモジュールを外部同期で動作させることができます。

- VD入力時はHD端子にHDを入力します。
- VBS入力時はHD端子にHDを入力しません。

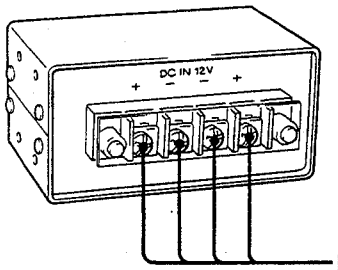
またカメラモジュールを単独で使用する場合，カメラの内部配線を変更することによってフィールドインデックス信号（FLD信号，VD信号，または複合同期信号）を出力します。

❻ HD IN端子

同期信号発生器を接続して，HD信号を入力します。VD IN端子から入力されるVD信号と合わせて，カメラモジュールを外部同期で動作させることができます。
またカメラモジュールを単独で使用する場合，カメラの内部配線を変更することによって，HD信号を出力します。

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裏面



DC IN 12 V (DC 12 V電源入力) 端子

DC IN 12 V (DC 12 V電源入力) 端子

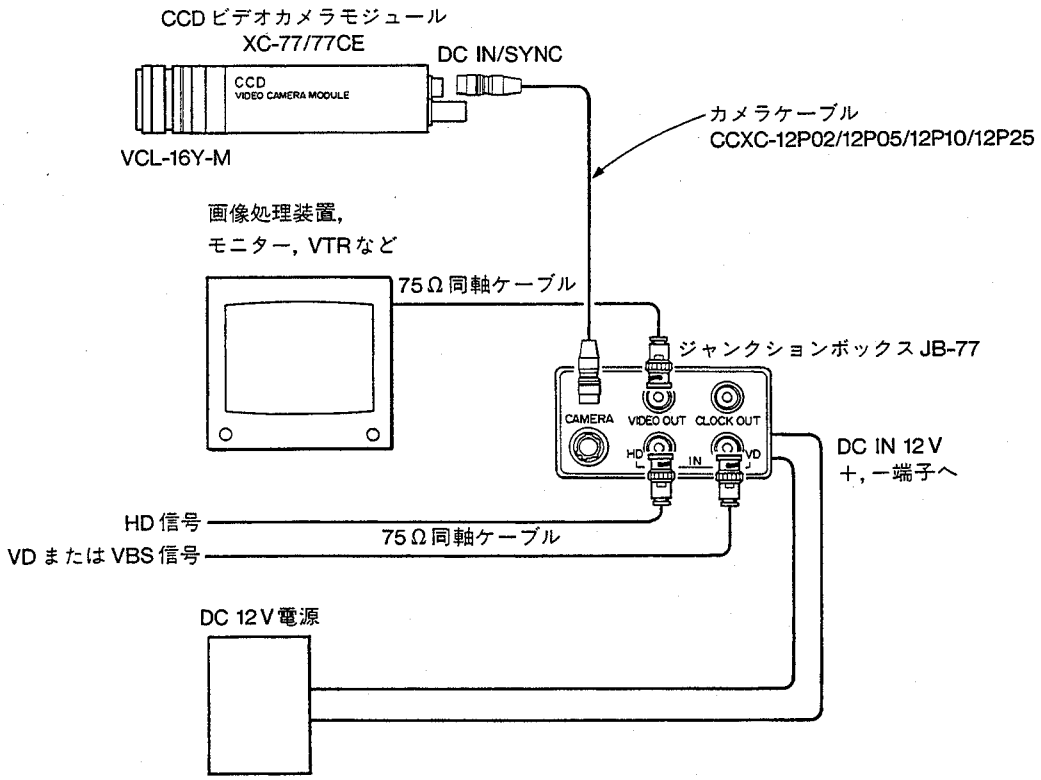
DC 12 Vの電源の供給を受けます。

カメラを複数台接続するときは，あいている方の端子に別のJB-77を接続すると，そのJB-77にも電源を供給することができます。

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1-4. 接続例

1-4-1. ジャンクションボックスを使用する場合

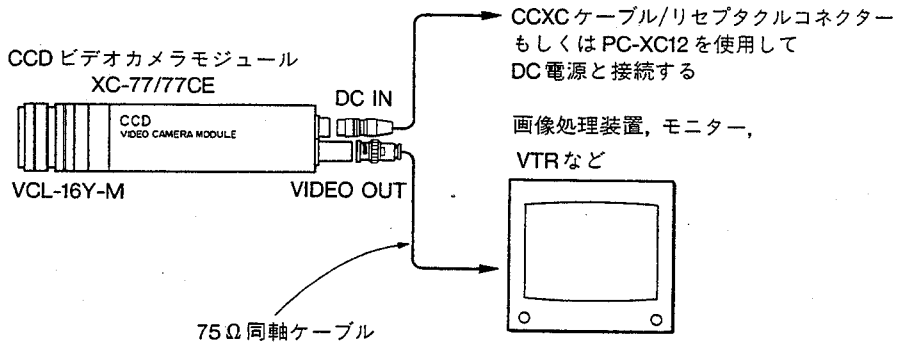


ご注意

CCXC ケーブルを使用して VBS または VS による外部同期をかける場合，カメラケーブル CCXC-12P25 を使用するとゲンロック時の画像に VBS 信号の影響が出る場合があります。その場合には，BS もしくは S のみを使用してください。

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1-4-2. ジャンクションボックスを使用しない場合



ご注意

- 映像出力を VIDEO OUT 端子から取り出すときは，DC IN/SYNC 端子は電源供給用に使い，DC IN/SYNC 端子の接続には CCXC-12P02 ケーブルをご使用ください。このとき 12 ピンコネクターの映像出力を終端しないでください。
- DC IN/SYNC 端子に 5 m 以上のケーブルをつないだ場合は，VIDEO OUT 端子から映像出力を取り出すことはできません。

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1-5. モードの初期設定

本機では，次の8項目についてそれぞれモードの切り換えが可能です。各項目とも上が工場出荷時の初期設定モードです。

項　目	モ ー ド	備　考
AGC	FIX GAIN	利得固定
	AGC	利得自動調整
γ	1	γ補正なし
	compensate	γ補正
EIA/CCIR	EIA	ROM（EIAモード）
	CCIR	ROM（CCIRモード）
FRAME/FIELD	FRAME	フレーム蓄積
	FIELD	フィールド蓄積
FRAME	NORMAL	通常走査
	INVERSION	偶数フィールドと奇数フィールド反転
RESTART RESET	OFF	フレーム同期せず
	ON	フレーム同期
EIA/CCIR	EIA	SG（EIAモード）
	CCIR	SG（CCIRモード）

ご注意

EIA/CCIRのモード設定はCCD素子 (EIA/CCIR) によって異なります。

1-6. 使用上のご注意

電源について

DC 12Vで動作します。リップル，ノイズのない安定した電源をお使いください。

異物について

内部に液体をこぼしたり，燃えやすいものや，金属類を落とさないでください。そのまま使用すると火災や感電，故障，事故の原因となります。

動作中は布などで包まないでください。

使用・保管場所

次のような場所での使用および保管はお避けください。

- 極端に暑い所や寒い所。（使用温度は0°C～40°C）
- 湿気，ほこりの多い所。
- 雨にあたる所。
- 激しい振動のある所。
- 強力な電波を発生するテレビ，ラジオの送信所の近く。

お手入れ

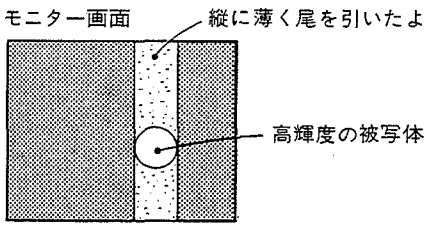
レンズや光学フィルターの表面に付着したごみやほこりは，ブロアーで払ってください。外装の汚れは，乾いた柔らかい布でふきとります。ひどい汚れは，中性洗剤溶液を少し含ませた布でふきとった後，からぶきします。アルコール，ベンジンなどは，変質したり，塗料がはげることがありますので使用しないでください。

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1-7. CCD特有の現象

スミア現象

高輝度の被写体（電灯，蛍光灯，太陽，強い反射光など）を写したときに起こる現象。



この現象は，CCDが右の図のようなインターライン転送方式を採用しているため，フォトセンサーの深いところに入った赤外線などにより誘起された電荷がレジスターに転送されるために起こるものです。

折り返しひずみ

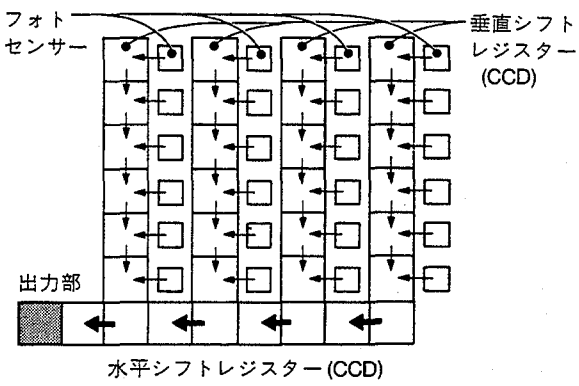
縞模様，線などを写すと，ギザギザに見えることがあります。

傷

CCDはフォトセンサー(素子)が縦横に並んでできており，フォトセンサーのいずれかに欠陥があると，その部分だけ画像が写らず，モニター画面上に傷となって見えます（実用上支障がない程度)。傷の規格については製品仕様書を参照してください。

CCDインターライン転送方式

本機が採用しているインターライン転送方式は，CCD上に結んだ像の明暗に対応した電荷を，順次転送して行くものです。フォトセンサーで検知した被写体の明暗に対応した電荷は，下図のように，まず，それぞれ隣りの垂直シフトレジスターに転送され，垂直シフトレジスターに移った電荷は，垂直方向に順次，水平シフトレジスターへ送られます。水平シフトレジスターに移された電荷は，水平方向に順次転送され，出力部から出力されます。



微小白点

高温時，暗い被写体を写している場合，画面全体に多数の白点が現れることがあります。

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第 2 章
製品仕様

2-1. 仕様

〈カメラモジュール XC-77〉

撮像素子	インターライン方式CCD固体撮像素子
有効画素数	768(H)×493(V)
撮像面積	8.8mm×6.6mm (⅔インチサイズ)
光学黒期間	各水平走査線のうち50画素
垂直駆動周波数	15.734KHz ±1%
水平駆動周波数	14.318MHz
信号方式	EIA方式
転送方式	インターライン転送
セルサイズ	11μm(H)×13μm(V)
チップサイズ	10.0mm(H)×8.2mm(V)
光学系	
レンズマウント	Cマウント
フランジバック	17.526mm
同期方式	内部/外部自動切り替え
外部同期入力	VBS, VS (SYNC LEVEL 0.3Vp-p±6dB)
外部同期許容周波数偏差	±1%
ジッター	±50nsec以内
電源投入時のロック時間	10sec以内
走査方式	525本 2:1インターレース
映像出力	1.0Vp-p同期負, 75Ω不平衡
水平解像度	570TV本
垂直有効ライン数	485本 2:1インターレース
感度	400Lux, F4(ガンマON/0dB)
最低被写体照度	3Lux, F1.4
S/N比	50dB
電源電圧	DC 12V
電圧範囲	DC 10.5V~15V
消費電力	2.2W
重さ	
カメラモジュール	190g(XC-77)
三脚アタッチメント	15g(VCT-37)
カメラケーブル	(2m) 130g (CCXC-12P02)
	(5m) 295g (CCXC-12P05)
	(10m) 560g (CCXC-12P10)
	(25m) 1.4kg (CCXC-12P25)
ジャンクションボックス	170g (JB-77)

保在温度	−30°C~+60°C
性能保証温度	0°C~40°C
耐衝撃	70G
保存湿度	90%以下
動作湿度	70%以下

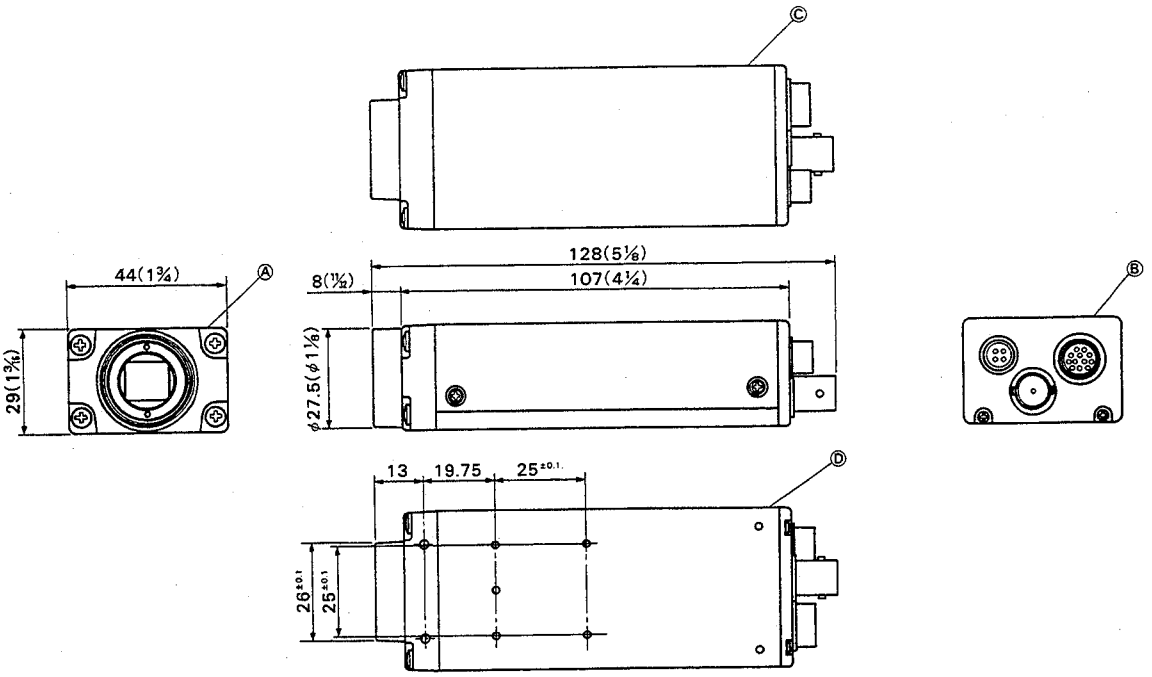
〈標準レンズ VCL-16Y-M〉

焦点距離	16mm
最大口径比	1:1.4
絞り	F1.4~F16
フィルター取り付けねじ	M25.5mm×P0.5mm
マウント	Cマウント
重さ	50g

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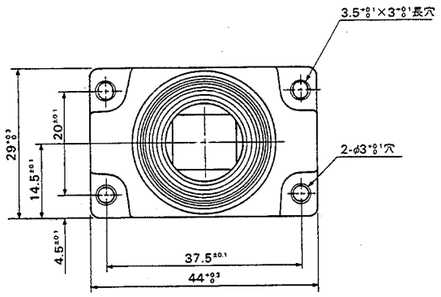
寸法

カメラモジュール〈XC-77〉

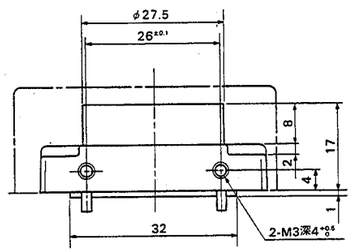


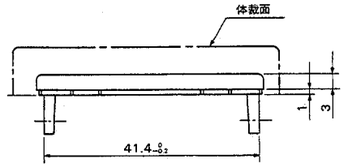
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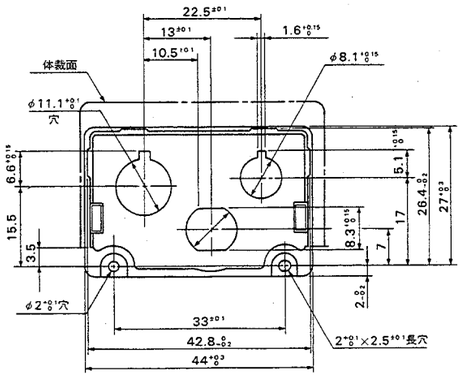
Ⓐ部

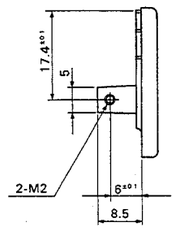


Ⓑ部

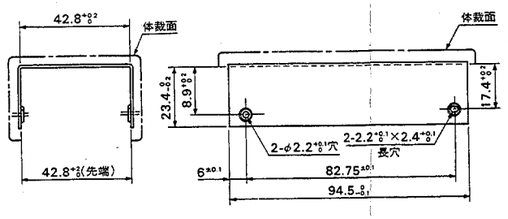




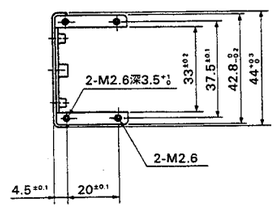


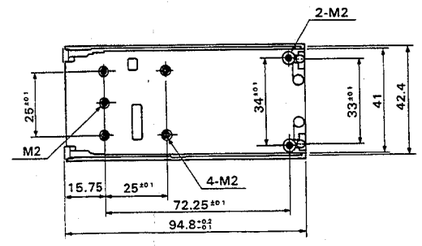


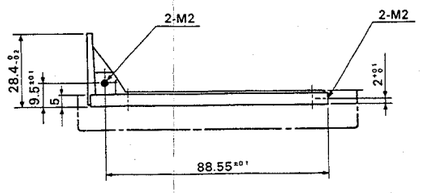
Ⓒ部



Ⓓ部

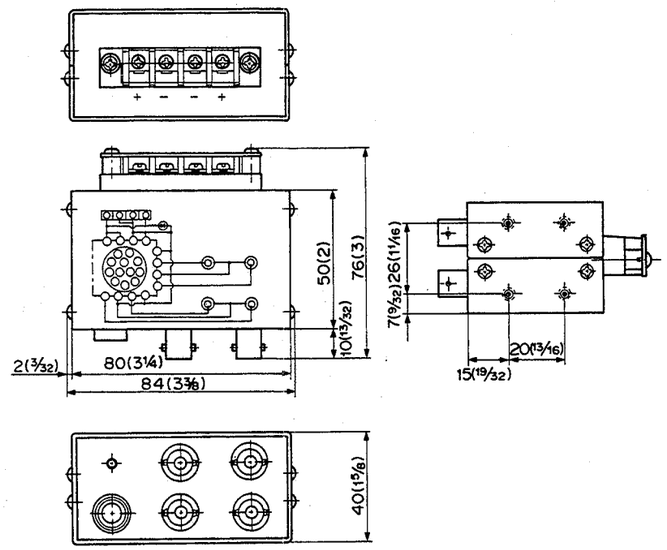




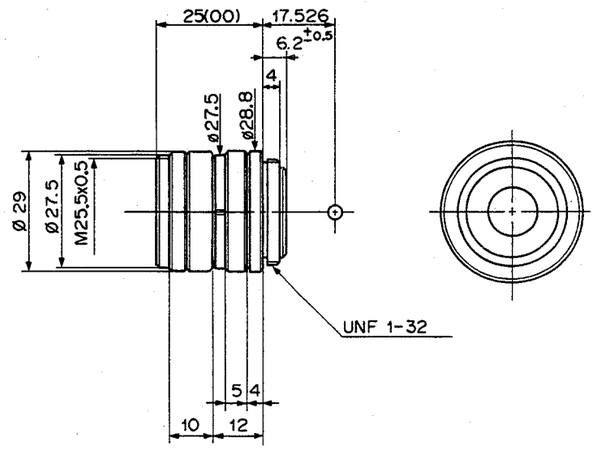


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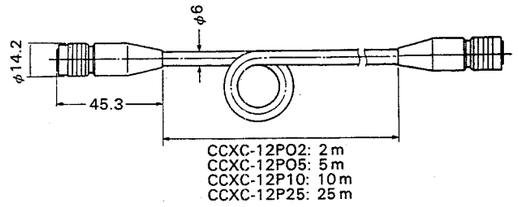
ジャンクションボックス



レンズ

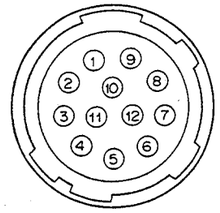


カメラケーブル



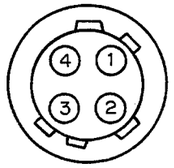
2-2. コネクターの入出力信号

12P マルチコネクター（接続側）



信号 / ピン番号	外部同期モード			CAMERA 同期出力
	HD, VD	VBS/VS	RESTART RESET	
1	アース	アース	アース	アース
2	+12 V	+12 V	+12 V	+12 V
3	映像出力（アース）	映像出力（アース）	映像出力（アース）	映像出力（アース）
4	映像出力（信号）	映像出力（信号）	映像出力（信号）	映像出力（信号）
5	HD 入力（アース）	—	HD 入力（アース）	HD 入力（アース）
6	HD 入力（信号）	—	HD 入力（信号）	—
7	VD 入力（信号）	VBS 入力（信号）	RESET PULSE（信号）	—
8	CLOCK 出力（アース）	CLOCK 出力（アース）	CLOCK 出力（アース）	CLOCK 出力（アース）
9	CLOCK 出力（信号）	CLOCK 出力（信号）	CLOCK 出力（信号）	CLOCK 出力（信号）
10	アース	アース	アース	アース
11	+12 V	+12 V	+12 V	+12 V
12	VD 入力（アース）	VBS 入力（アース）	RESET PULSE（アース）	FIELD INDEX 出力（アース）

4 ピンレンズコネクター（接続側）

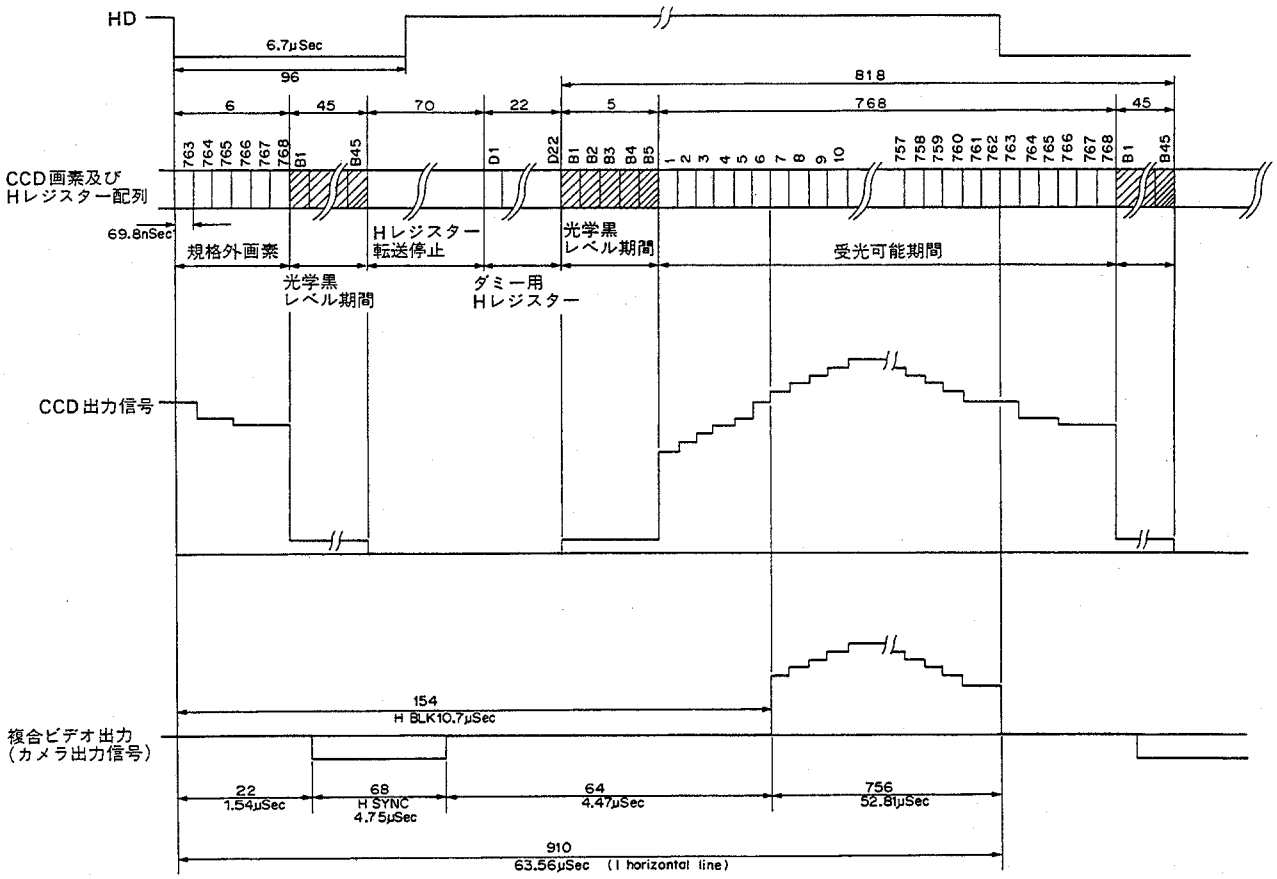


ピン番号	信号名	規格
1	+12V OUT	DC12V出力
2	GND	GND
3	NC	空ピン
4	VS OUT	ビデオ信号 出力

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2-3. CCD出力波形タイミングチャート

タイミングチャート中に記載してある周期はHDの周波数
が15.734KHzのときの値です。



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2-4. 外部同期について

外部同期モードには
1. VS/VBSモード
2. HD.VDモード
3. RESTART RESETモード
の3モードがあります。

2-4-1. VS/VBSモード

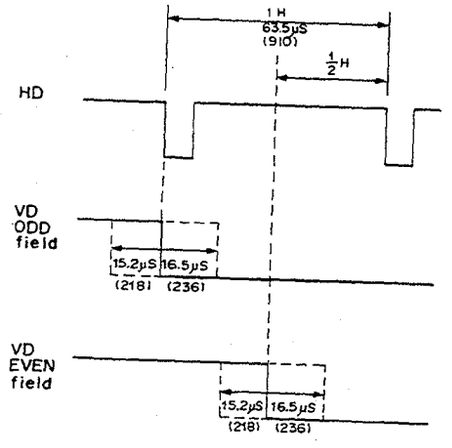
正規のコンポジット信号（VS又はVBS）を12ピンコネクターの7ピンに加えることで，外部同期を掛けるモードです。

2-4-2. HD.VDモード

HD.VDを12ピンコネクターの6ピンと7ピンにそれぞれ加えることで外部同期を掛けるモードです。

●HD.VDの入力条件
・周波数（周期）
HD　15.734KHz ±1%（63.56μS±1%）
VD　244～1023½H
※注意：最大垂直有効ライン数はインターレース時で486ラインです。
ノンインターレース時は，ODDフィールド，EVENフィールドとも242ラインです。

・位相



※（　）内はクロック数

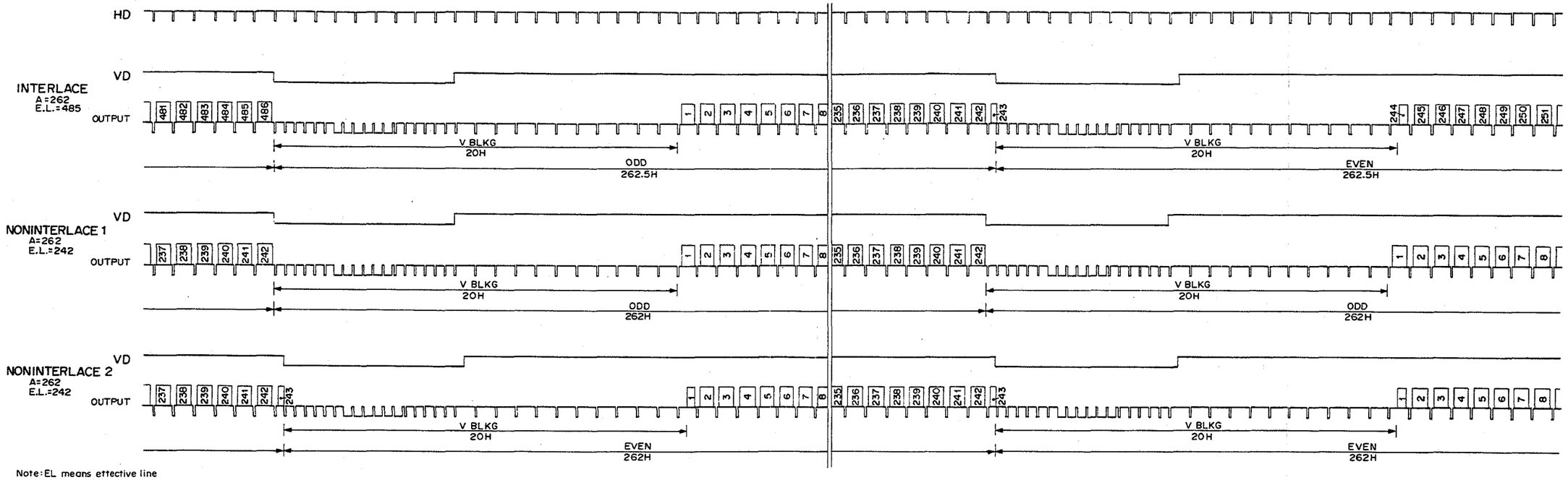
イラスト中でHDの立ち下がりに対してVDの立ち下がりが進相15.2μS～遅相16.5μS以内の時はODDフィールドになります。
また，HDの立ち下がりから½Hの時点に対するVDの立ち下がりが進相15.2μS～遅相16.5μS以内の時はEVENフィールドになります。

●インターレース，ノンインターレース
VDの入力条件を変化させることで，インターレースでもノンインターレースでも動作させることができます。（〔図1〕参照）

・インターレース
インターレースで動作させる時は，VDの周期を(A+½)Hにします。「Aは244～1023までの整数」すなわちHDの立ち下がりに対するVDの立ち下がりの位相が，VD毎に切り換わります。するとフィールドがODD→EVEN→ODD→…と変化し，インターレースで動作します。この時の1フレームの走査線数は2A+1ラインです。

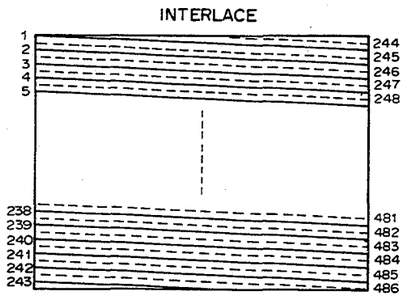
・ノンインターレース
ノンインターレースで動作させる時は，VDの周期をA·Hにします。「Aは244～1023までの整数」すなわちHDの立ち下がりに対するVDの立ち下がりの位相がVD毎に変化せず，フィールドがODD→ODD→ODD→…，又はEVEN→EVEN→EVEN→…と続き，ノンインターレースで動作します。但し，1フレームの走査線数はAラインでインターレース時の半分になります。またフレーム蓄積時には感度もインターレース時の半分になります。

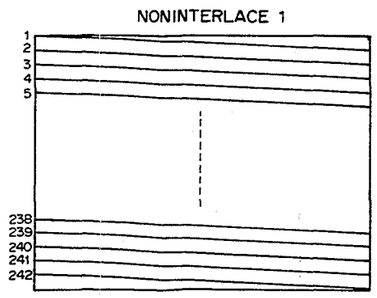
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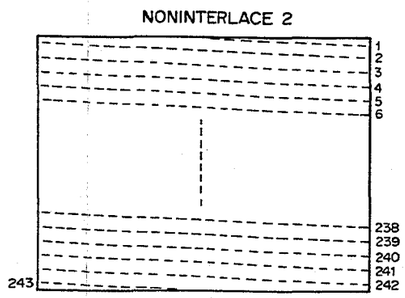


Note:EL means effective line

注意：E.L. は有効ライン数です。



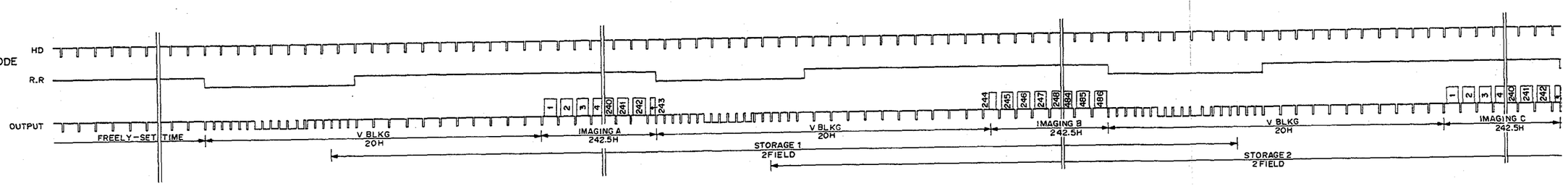




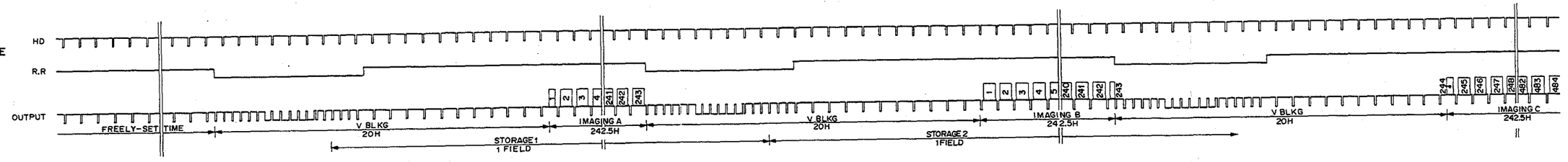
〔図1〕

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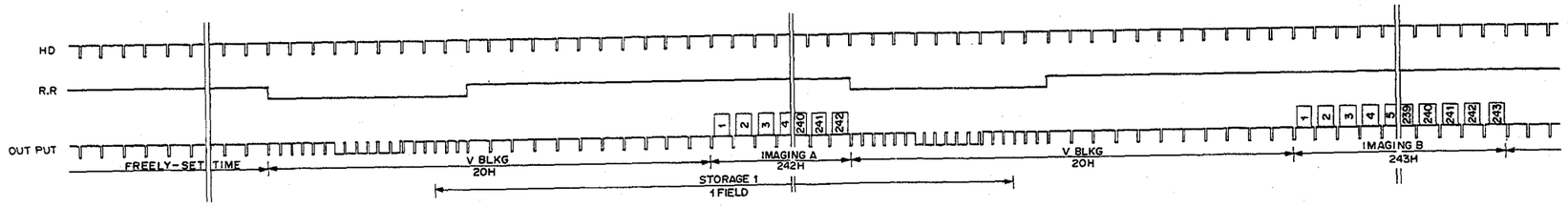
FRAME INTEGRATION MODE
'NTERLACE
A=262
E.L=485



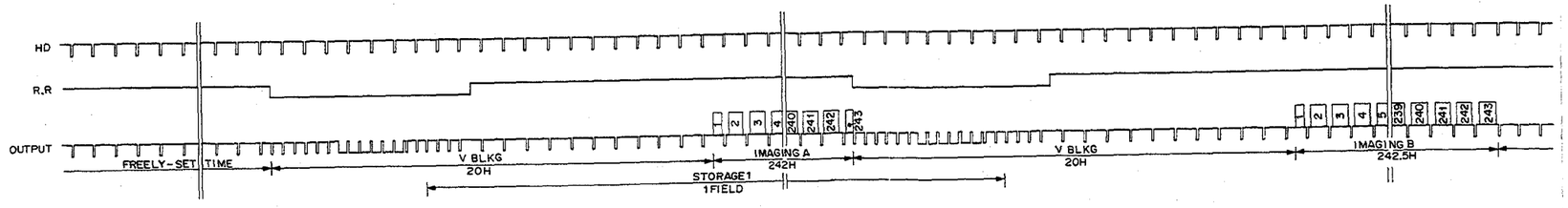
FIELD INTEGRATION MODE
INTERLACE
A=262
E.L=485



NONINTERLACE 1
A=262
E.L=243

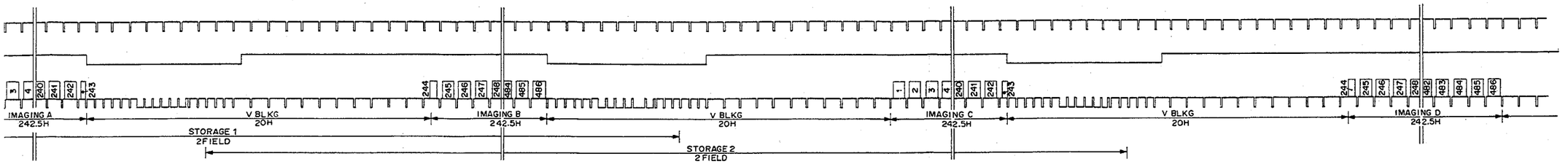


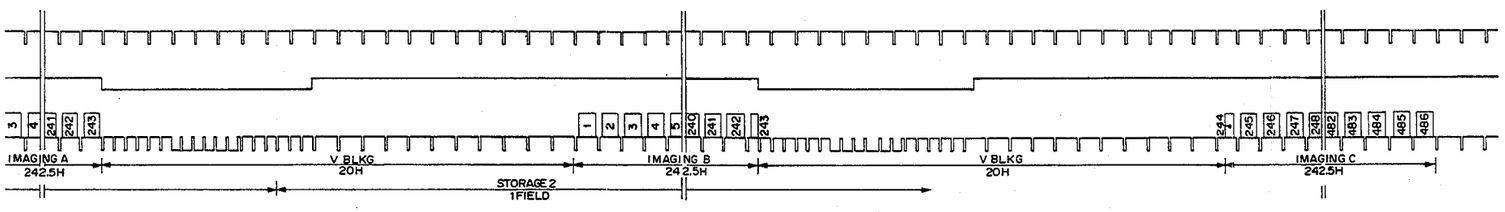
NON INTERLACE2
A=262
E.L=242

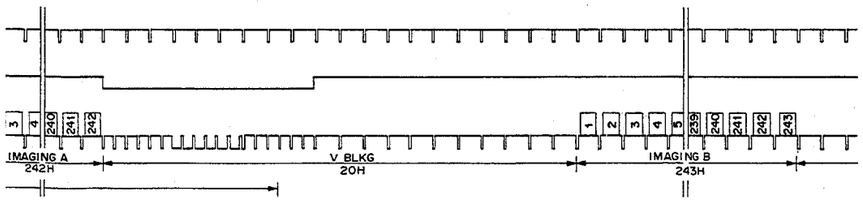


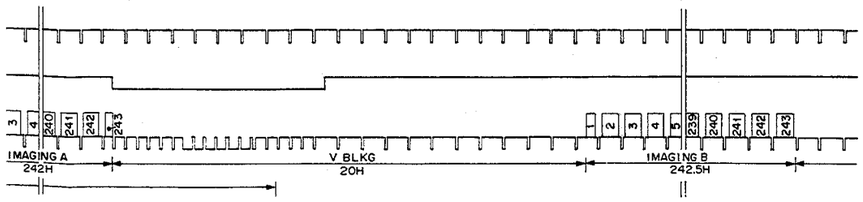
〔図2〕

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〔図2〕

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2-4-3. RESTART RESETモード

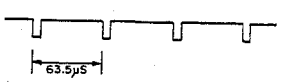
RESTART RESET(R.R)モードを使うと任意の時刻に1画面の情報を取り出すことができます。R.Rモードを使う場合は，カメラ内部でモードを設定する必要があります。2-5.モード設定を参照してモードを設定して下さい。HD. R.Rを12ピンコネクターの6ピンと7ピンにそれぞれ加えることで，出力を得ることができます。

●HD. R.Rの入力条件

・周波数（周期）

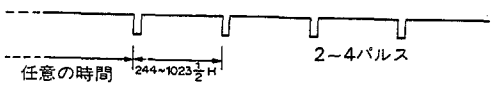
HD　15.734KHz ±1%（63.56μS±1%）

連続パルス



VD　244～1023½H

2～4パルス（モードによって異なります。）



・位相

2-4-2. HD. VDモードの位相条件と同じです。参照して下さい。

●タイミングチャートの説明

〔図2〕は各動作モード別のタイミングチャートです。以下に詳細を説明します。

・フレーム蓄積，インターレースモード

R.Rが4パルス必要です。R.Rの周期を(A+½H)にします。「Aは244～1023までの整数(図はA=262)」

IMAGING C(ODD) と IMAGING D(EVEN) の期間にそれぞれSTORAGE 1, STORAGE 2の間に撮像した情報が出力されます。IMAGING A, IMAGING Bの期間にCCDがリセットされます。よって，この間に出力される信号は意味がありません。

・フィールド蓄積，インターレースモード

R.Rが3パルス必要です。R.Rの周期を(A+½H)にします。「Aは244～1023までの整数(図はA=262)」

IMAGING B(ODD) と IMAGING C(EVEN) の期間にそれぞれSTORAGE 1, STORAGE 2の間に撮像した情報が出力されます。IMAGING Aの期間にCCDがリセットされます。よって，この間に出力される信号は意味がありません。

・ノンインターレースモード

蓄積モードに関係なくR.Rが2パルス必要です。

R.Rの周期をA・Hにします。「Aは244～1023までの整数(図はA=262)」

IMAGING Bの期間にSTORAGE 1の間に撮像した情報が出力されます。IMAGING Aの期間にCCDがリセットされます。よって，この間に出力される信号は意味がありません。

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2-5. モード設定

XC-77は，用途に応じて動作モードを切り換えることが可能です。
モードの設定はPR-89基板とSG-119基板，そしてMB-基板で行います。

PR-89基板

項　　目	モード	SHORT	OPEN
AGC	AGC	AGC	FIX
	FIX GAIN	FIX	AGC
γ	1	γ1	γ2
	COMPENSATE	γ2	γ1
WHITE CLIP	γ	γ1	γ2
	WHITE CLIP	γ2	γ1

SG-119基板

項　　目	モード	M't	OPEN
EIA/CCIR	EIA	R 7	R 6
	CCIR	R 6	R 7
FRAME/FIELD	FRAME	R 1	R 2
	FIELD	R 2	R 1
FIELD	NORMAL	R23	R28
	INVERSION	R28	R23
RESTART RESET	NORMAL	R24	R29
	RESET	R29	R24
EIA/CCIR	EIA	R27	R22
	CCIR	R22	R27

※R1，R2の抵抗値は1KΩです。
それ以外は全て10KΩです。

MB-136基板

項　　目	モード	M't	OPEN
RESTART RESET	NORMAL	R35	
	RESET		R35

※R35の抵抗値は220KΩです。

●各動作モードの説明

・VIDEO GAINモード（AGC/FIX GAIN）
ビデオ出力信号のゲイン（利得）を設定します。
AGCに設定すると，AGC(Automatic Gain Control)機能が働きます。
FIX GAINに設定するとゲインが固定になります。
設定はPR-89基板の「AGC」で行います。AGCに設定する場合はAGC側をショート（短絡）し，FIX側をオープン（開放）します。FIX GAINに設定する場合は，FIX側をショートし，AGC側をオープンします。
工場出荷時は，FIX GAINに設定されています。

・γ補正モード（1/COMPENSATE）
ビデオ出力信号のγ補正を設定します。
γをCOMPENSATEに設定すると，γ補正が行われたビデオ信号を出力します。γを1に設定すると，γ補正を行いません。よって被写体の光量に比例した信号を得ることができます。
設定はPR-89基板の「γ」と「WHITE CLIP」で行います。
COMPENSATEに設定する場合は，「γ」，「WHITE CLIP」共にγ2側をショート（短絡）し，γ1側をオープン（開放）します。1に設定する場合は，「γ」，「WHITE CLIP」共に，γ1側をショートし，γ2側をオープンします。
工場出荷時は，γ＝1に設定されています。

・EIA/CCIRモード（EIA/CCIR）
ビデオ出力信号の信号方式を設定します。
必ず「EIA」に設定します。

・蓄積モード（FRAME/FIELD）
CCDのフォトセンサーから信号電荷を読み出す周期を設定します。
フィールドに設定すると，信号電荷をフィールド毎に読み出します。　フレームに設定すると信号電荷をフレーム毎に読み出します。ノンインターレースで動作させる時に，フレーム蓄積モードに設定されていると，インターレース動作時に比べて感度が半分になります。注意して下さい。
設定はSG-119基板の「FRAME/FIELD」で行います。
フィールドに設定する場合は，「FRAME/FIELD」のR1（1KΩ）をマウントし，R2をオープンします。
フレームに設定する場合は，「FRAME/FIELD」のR2（1KΩ）をマウントし，R1をオープンします。
工場出荷時はフレームに設定されています。

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・RESTART RESETモード（NORMAL/RESET）

外部同期モードを設定します。

NORMALに設定すると，外部同期モードが「VS/VBSモード」又は，「HD. VDモード」になります。

RESETに設定すると外部同期モードが「RESTART RESET モード」になります。

外部同期のそれぞれのモードについての詳細は，2-4. 外部同期についてを参照して下さい。

設定はSG-119基板の「RESTART RESET」と，MB-136基板のR35をマウント，オープンすることで行います。

NORMALに設定する場合は「RESTART RESET」のR24（10KΩ）をマウントし，R29をオープンします。同時にMB-136基板のR35をマウントします。

RESET に設定する場合は，「RESTART RESET」の R29（10KΩ）をマウントし，R24をオープンします。同時にMB-136基板のR35をオープンします。

工場出荷時はNORMALに設定されています。

・フィールド反転モード（NORMAL/INVENSION）

外部同期時にビデオ出力信号のフィールド反転動作を設定します。

INVERSIONに設定すると，ビデオ出力信号のフィールドが外部同期信号に対して反転します。つまり外部同期信号のフィールドが ODD の時は EVEN, EVEN の時は ODDを出力します。

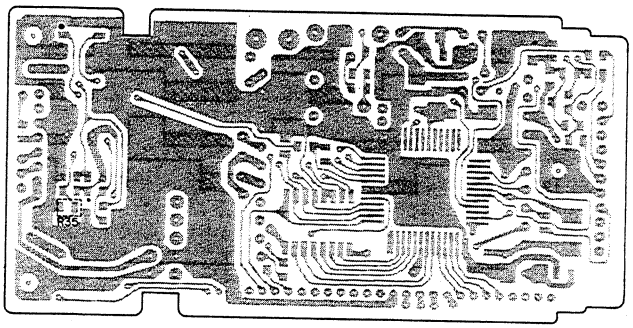
NORMAL に設定すると，通常の外部同期時と同じで外部同期信号のフィールドがODDの時はODD, EVENの時はEVEN を出力します。

設定は，SG-119基板の「FIELD」で行います。

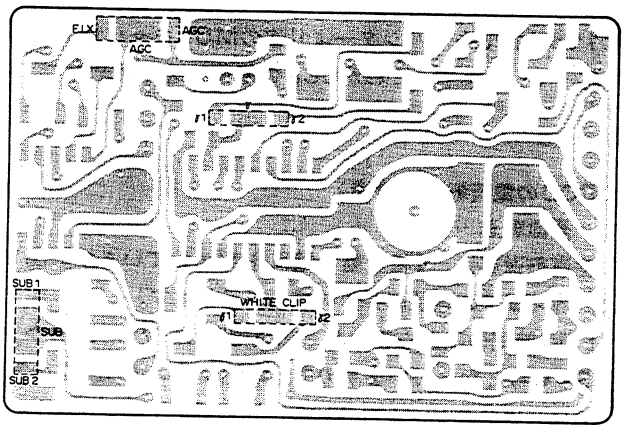
NORMALに設定する場合は，「FIELD」のR23（10KΩ）をマウントし，R28をオープンします。

INVERSIONに設定する場合は，「FIELD」のR28（10KΩ）をマウントし，R23をオープンします。

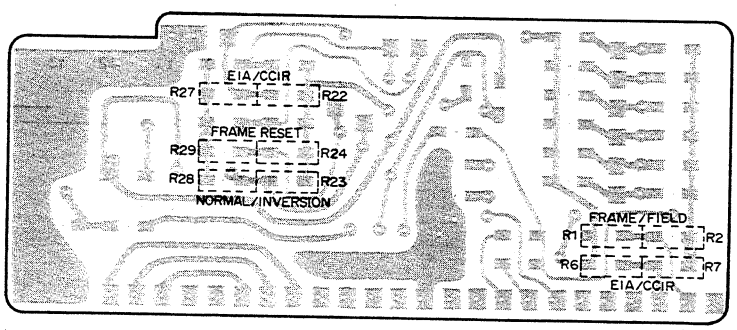
工場出荷時は，NORMALに設定されています。



MB−136 BOARD (Soldering Side)



PR−89 BOARD (Soldering Side)



SG−119 BOARD (Soldering Side)

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2-6. 動作説明

〈CCDの原理〉

CCD（Charge Coupled Device＝電荷結合ディバイス）は、規則正しく配列されたMOS（Metal-Oxide-Semiconductor）キャパシターによって構成されています。MOSキャパシターは電荷を扱うための3つの基本的な機能を持っています。

1. 光電変換（フォトセンサー）

入射光は，MOSキャパシターで電荷を発生させます。このとき発生する電荷量は，光の明暗に比例します。

2. 電荷の蓄積

MOS キャパシターの電極に電圧がかけられると，シリコンの層の中の電位の井戸が作られます。電荷はこの井戸に蓄えられます。

3. 電荷の転送

高い電圧が電極にかけられるとより深い井戸が作られ，また低い電圧では，浅い井戸が作られます。電荷の転送は，この特性を利用して行われます。

電極に高い電圧を加えると，深い電位の井戸ができて，隣の井戸にたまっていた電荷が流れこんできます。

これが規則的に並んだ電極に次々繰り返されると，電荷は1つのMOSキャパシターより次のMOSキャパシターへと移っていきます。これがCCDの電荷転送の原理です。

〈CCDの電荷転送の機構〉

1. 垂直転送

垂直転送部は，4相駆動で電荷を転送しています。図1に，各時間での電位の井戸の様子を示します。

t 0の時間の状態をみると，電極電圧は（V1＝V2）＞（V3＝V4）となっていますので，電圧が高いV1とV2の電極の部分は井戸が深くなり，この深い部分に電荷が蓄えられています。

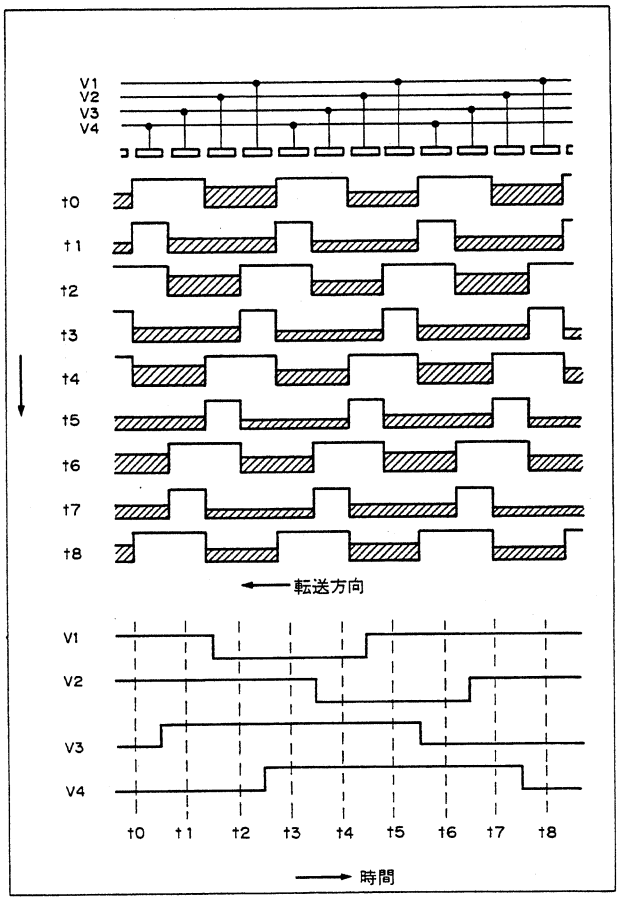
時刻ｔ 1では，電極電圧が（V1＝V2＝V3）＞（V4）となり，V1とV2とV3の井戸に電荷が蓄えられます。

時刻ｔ 2では，電極電圧が（V2＝V3）＞（V4＝V1）となり，V2とV3の井戸に電荷が蓄えられます。

時刻ｔ 3以降の電極電圧の状態を次に示します。

時刻ｔ 3　（V2＝V3＝V4）＞（V1）
時刻ｔ 4　（V3＝V4）＞（V1＝V2）
時刻ｔ 5　（V4）＝（V1＝V2＝V3）
時刻ｔ 6　（V4＝V1）＞（V2＝V3）
時刻ｔ 7　（V4＝V1＝V2）＞（V3）
時刻ｔ 8　（V1＝V2）＞（V3＝V4）〔時刻t0の状態と同じ〕

この動作を次々に繰り返して垂直転送が行われます。



〔図1〕垂直転送

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2. 水平転送

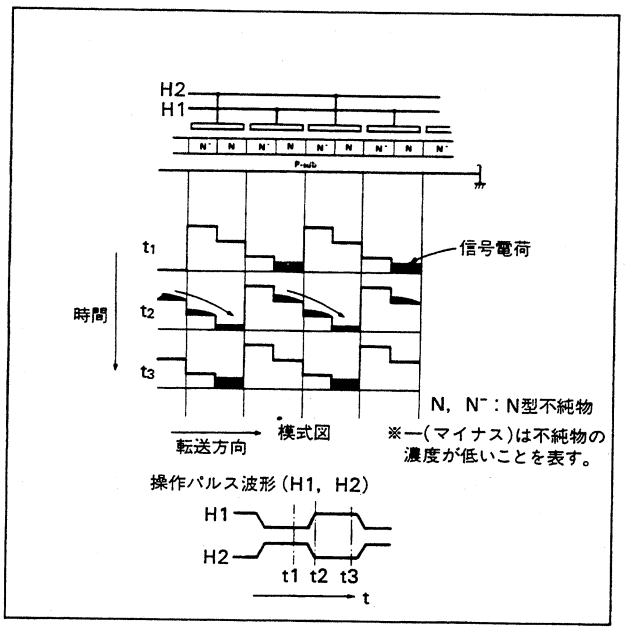
水平転送部は，2相駆動で電荷を転送しています。図2に各時間での電位の井戸の様子を示します。

t 1の時間の状態をみると，電極電圧はH1＞H2となっていますので，電圧が高いH1の電極の部分は井戸が深くなり，この深い井戸の部分に電荷が蓄えられています。

時刻t 2では，H1とH2の電圧が反転しており，H2の井戸は深く，H1の井戸は浅くなり，H2の井戸がH1の井戸よりも深くなるので信号電荷は，深いH2の井戸の方へ流れ込みます。

時刻t 3の状態では，電極電圧は変化していないから，信号電荷は，H2の井戸へ流れ込み1つの電荷転送が完了します。

この動作を次々に繰り返して水平転送が行われます。



〔図2〕水平転送

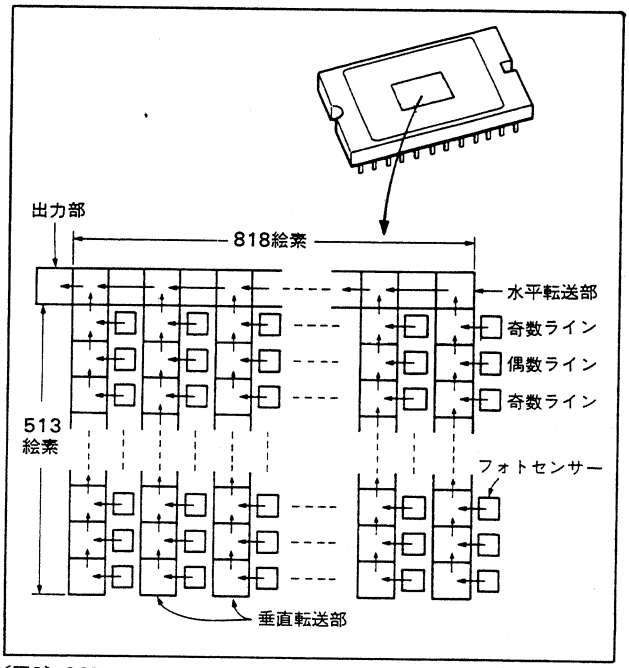
〈BI-12基板〉

カメラレンズを通して来た光は，BI-12基板のIC1（CCD）のチップ面に当たります。

CCDチップの表面には，フォトセンサー（感光素子）が配置されています。フォトセンサーは水平方向に818個，垂直方向に513個，合計419，634個あります。この内の水平方向に768個，垂直方向に498個，合計382,464個が有効画素です。入射光はフォトセンサー部で光の明暗に応じ，電荷に変換されます。

変換された電荷は，フォトセンサーから転送部に読み出され，その後順々に転送され出力部へ導かれます。転送部には，垂直転送部と水平転送部があります。垂直転送部は図3に示すように，画面の垂直方向に818本あります。又，水平転送部は画面(図3の最上部)の水平方向に1本あります。フォトセンサーで変換された電荷は，1FIELD（VDの周波数）毎に各フォトセンサーに隣接した垂直転送部に移されます。各垂直転送部に移された電荷は，垂直転送クロックV1，V2，V3，V4（HDの周波数）で，並列に垂直方向へ転送され，順次，水平転送部に移されます。水平転送部は，水平転送クロックH1，H2（周波数910fh）で，電荷を水平方向へ転送し，出力部に送ります。

出力部は，電荷を電気信号に変換して出力します。ICIを出力する信号はQ1のバッファーを通った後に，SH-27基板へ送られます。



〔図3〕CCDインターライン転送方式

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〈SH-27基板〉

この基板には，サンプルホールド回路があります。

BI－12基板から送られて来るCCDの出力信号は2本に分岐されます。どちらの信号もサンプルホールドパルス（SHP，SHD）により，サンプルホールドされます。一方はSHP，SHD，SHPの順番で3回サンプルホールドされます。他方はSHD，SHPの順番で2回サンプルホールドされます。この2つの信号の差をとることで，ビデオ信号を取り出しています。これは，CCDの出力信号には特有のノイズ成分があり，その主要なノイズ成分を除去するために行われます。

2つの信号の差は，Q16～Q19で構成される差動アンプで得ています。この差動アンプを出力するビデオ信号は，PR-89 基板へ出力されます。

〈PR-89基板〉

この基板には，ビデオ信号処理回路があり，SH-27 基板から送られるビデオ信号をEIA方式のビデオ信号に変換しています。

SH-27 基板から送られるビデオ信号は，IC1 に入力します。IC1 には，オートアイリス回路と AGC 用のゲインコントロールアンプがあります。ゲインコントロールアンプを出力するビデオ信号はFL1(ローパスフィルター)を通った後に，IC2に入力します。この信号にIC2で，クランプ，ガンマ補正，ホワイトクリップ，ブランキングミックス，セットアップ付加，SYNC信号ミックスなどの信号処理が行われ，IC2を出力します。この後，Q1～Q8で構成される出力ドライバー回路を介して，出力しています。

〈CN-167基板〉

この基板はMB-136 基板と各外部コネクターとを接続する基板です。

CN-167 基板には，12ピンマルチコネクター（DC IN/SYNC 端子），4ピンコネクター（LENS 端子），BNCコネクター（VIDEO OUT端子）がマウントされています。

12ピンマルチコネクターは，電源電圧（＋12V），外部同期信号（EXT HD，EXT VD，RESET PULSE，VBS，VS）を入力し，ビデオ信号（VS），同期信号（CLOCK，HD，FIELD INDEX）を出力します。このコネクターの入出力信号は，使用する同期モード（内部同期，外部同期）によって違います。詳しくは，2-2. コネクターの入出力信号をご覧下さい。

4ピンコネクターは，電源電圧（＋12V）とオートアイリスレンズ用のビデオ信号を出力します。

BNCコネクターは，ビデオ信号（VS）を出力します。

〈RG-18基板〉

この基板は，CCD駆動クロック発生器とCCDサブストレート用のDC電圧を供給します。

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〈MB-136基板〉

この基板には，外部同期信号検出回路，1820fh発振回路，DC-DC コンバーター，CCD駆動クロック発生回路があります。

XC-77 は外部同期信号が入力されると自動的に外部同期モードに切り換わり，外部同期信号に同期したビデオ信号を出力するようになります。外部同期モードには，VS/VBS モード，HD.VD モード，FRAME RESET (FR) モードの3つがあります。

詳細は2-4.外部同期についてを参照して下さい。

HD.VD又はHD.FRが入力されるとMB-136基板ではQ1～Q3及びIC7によってこれらの信号を波形整形してSG-119基板に出力します。

VBS又はVSが入力されると，Q2，Q3及びIC7によってSYNC成分だけ取り出し，波形整形を行います。

このSYNC信号はSG-119基板に出力されます。

1820fh発振回路は，内部同期用と外部同期用の2つに分かれています。内部同期時には，水晶振動子（X1）を使用した発振回路が動作し，外部同期時にはVCOであるLC発振回路が動作します。VCOは発振周波数を±1%変化させることができます。VCOが入力するコントロール電圧は0～5Vで，2.8V入力時に28.6363MHz（1820fh）を出力するように設定しています。

発生する1820fhのクロックは，CCD駆動クロック発生回路に出力されます。

DC-DC コンバーターは，外部から供給される電源電圧（+12V）を+15V，+10V，+7V，+5Vに変換して各基板に供給しています。

CCD駆動クロック発生回路では，CCDを駆動するために必要なクロックを発生しています。IC1は，SG-119基板から出力するHDとVD信号及び1820fh回路が出力する1820fhのクロックを入力すると，次の信号を発生します。す。

CLOCK　：910fhのクロック（1820fhの半分の周波数のクロック）

H1・H2　：この2相のクロックによって水平転送部を

V1～V4　：駆動し，電荷を転送します。

V1～V4　：この4相のクロックによって垂直転送部を駆動し，電荷を転送します。

PG　：プリチャージゲートコントロールパルス。プリチャージゲートとは水平転送部と出力部のゲートであり，このゲートをコンロールして，転送されてきた電荷を電気信号（電圧）に変換しています。

SHP・SHD　：CCDの出力信号をサンプリングするためののパルスです。

CLP1　：CCDの出力信号の光学黒レベルをクランプするためのパルスです。

CCD駆動クロック（H1・H2，V1～V4，PG）は，IC3，IC5，IC6のドライブ回路を通った後に，CCDに出力されます。

〈SG-119基板〉

この基板には，各種同期信号発生回路があります。

IC1とIC2は，MB-136基板が出力するCLOCK(910fh)を入力すると下期の同期信号を出力します。

SYNC　：コンポジットシンク信号。

BLKG　：ブランキング信号。

HD・VD　：水平・垂直同期信号。

FLD　：フィールド識別信号。

$\overline{\text{INT}}$/EXT　：同期モード切り換え信号であり，内部同期モードでLowレベル，外部同期モードでHighレベルになります。

VCO CONT　：外部同期時のVCOのコントロール電圧です。

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第3章
調整要項

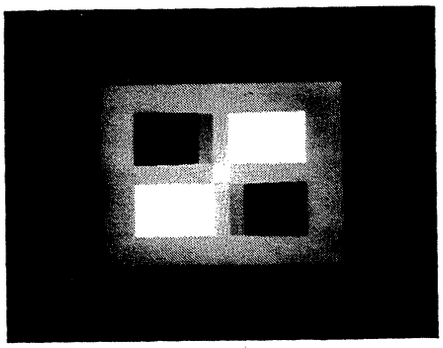
3-1. 準備

ステップ 1. 使用機器

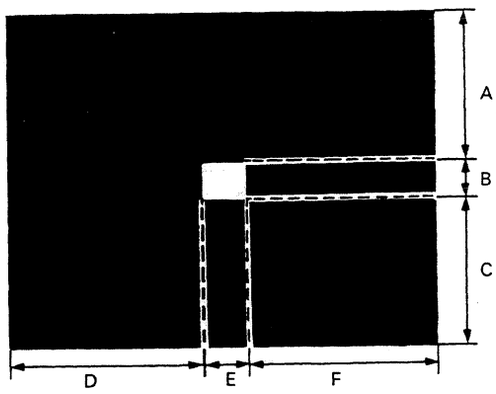
・オシロスコープ
・波形モニター
・白黒モニター
・デジタル電圧計
・電源供給用機器;
ジャンクションボックスJB-77(市販品)及び安定化電源
・三脚アタッチメントVCT-37(市販品)
・レンズ　標準:VCL-16Y-M(市販品)
・パターンボックス PTB-500 又は PTB-100
ソニー部品番号 J-6029-140-A

〔パターンボックスが入手困難な場合〕
・電球 100W
・スライダック

・グレースケールチャート
ソニー部品番号 J-6026-130-A



・ホワイトウインドウチャート
黒い紙に図のような穴をあける。

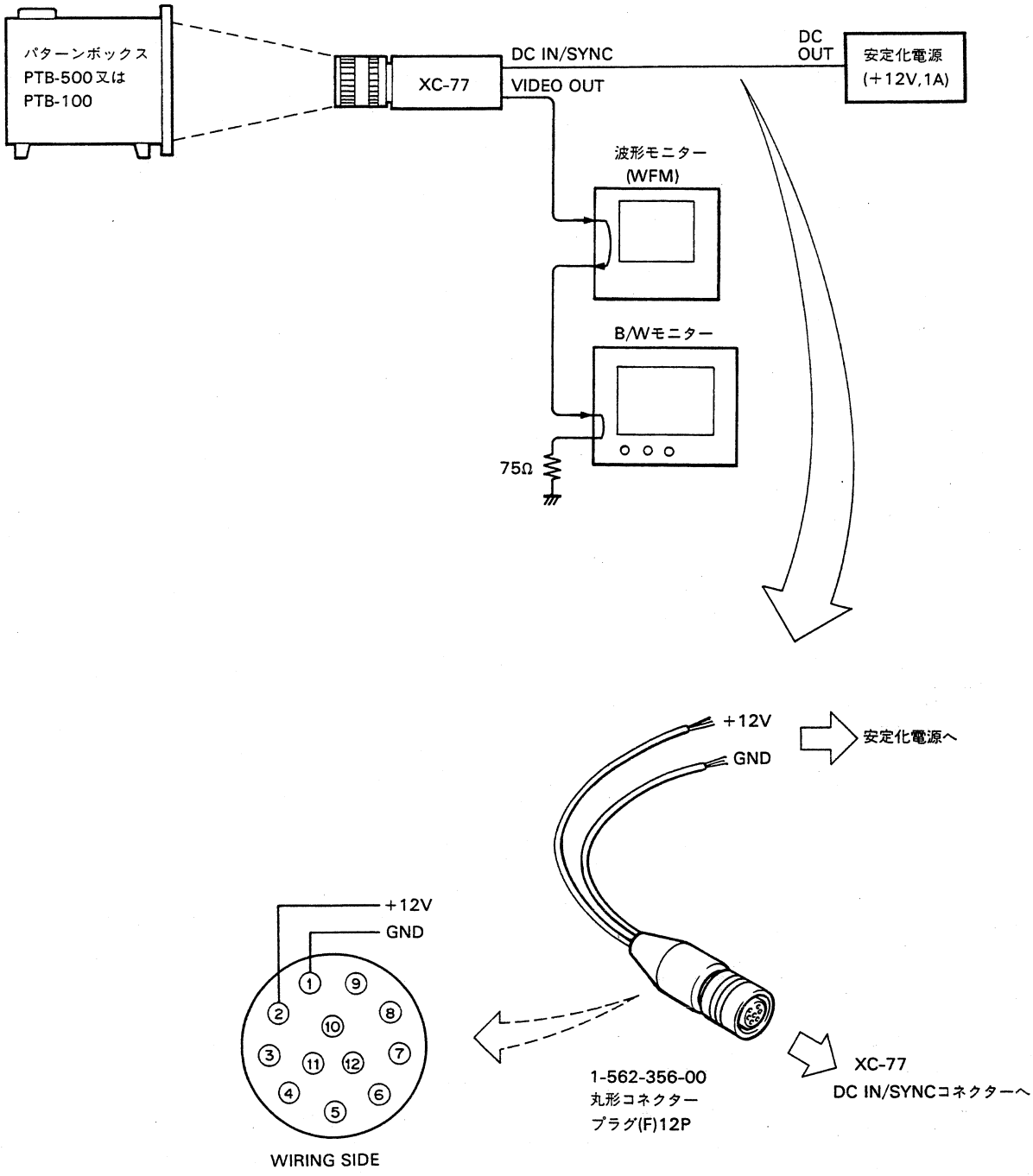


(Vertical A : B : C=4.5 : 1 : 4.5
Horizontal D : E : F=4.5 : 1 : 4.5)

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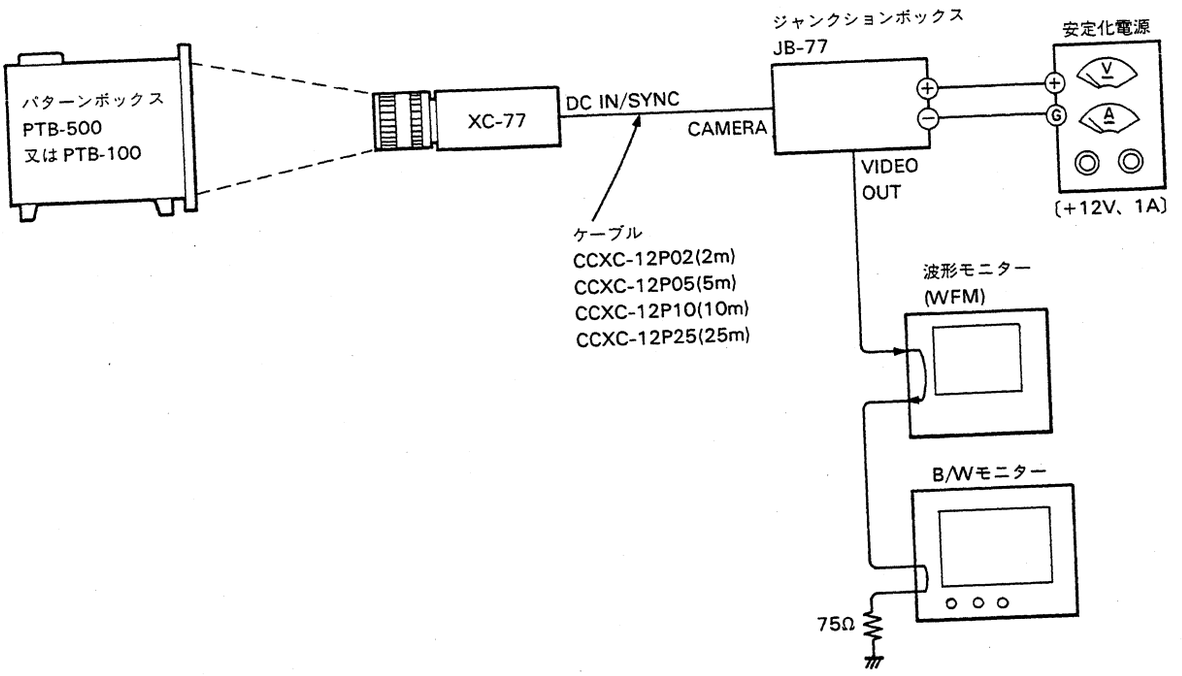
ステップ2.接続図

〔接続方法1〕

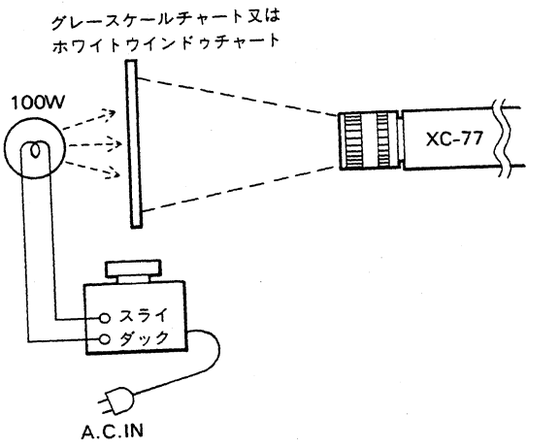


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〔接続方法2〕



〔パターンボックスが入手困難な場合〕
下図のような簡易光源で調整を行って下さい。



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3-2. 総合調整

ステップ 1. V SUB(field)調整

注意事項

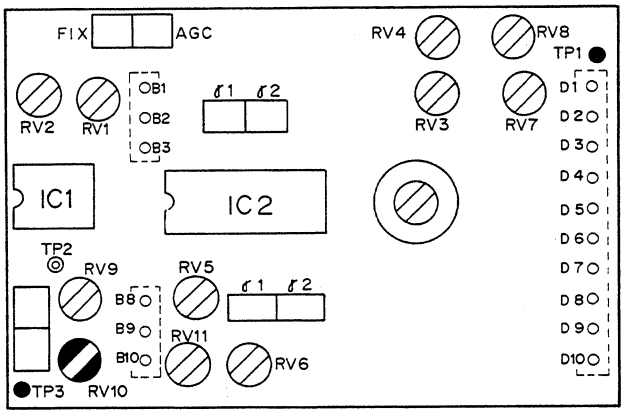
・CCDを交換した場合以外は絶対にこの調整を行わないこと。

・セッティング

測　定　器	デジタル電圧計

調整手順

測定点:TP3(GND:TP1)/PR-89基板
調整箇所:◐RV10/PR-89基板
規　格:新しいCCDを購入した際に、そのCCDの裏にVSUB2の規格電圧が記入されてありますので,その規格に合うように調整して下さい。



PR－89　BOARD　(Component Side)

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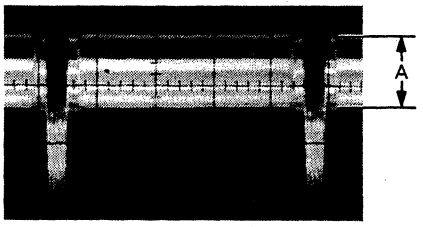
ステップ 2. カップリング・ノイズ除去調整

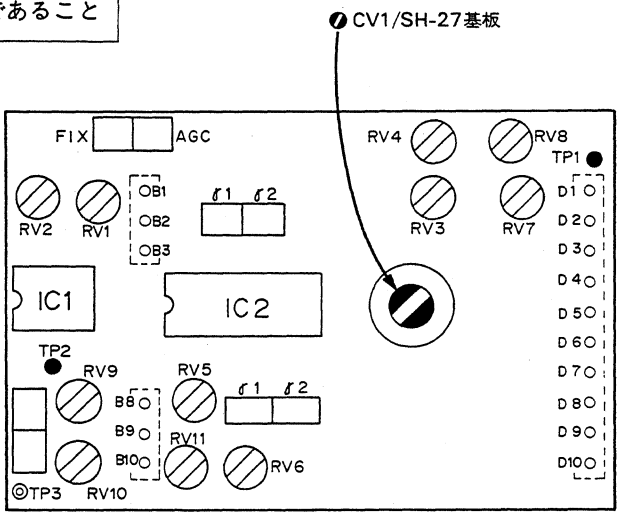
・セッティング

レンズ絞り 測　定　器	レンズキャップにてクローズ オシロスコープ	ト　リ　ガ	TP4(HD)/MB-136基板

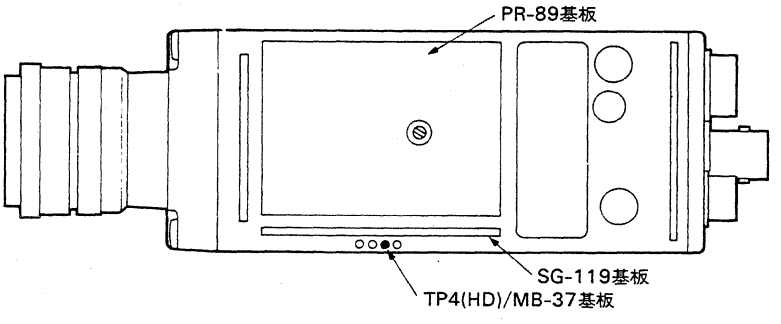
・調整手順

測定点/PR-89基板	調整箇所	規格
TP2(GND:TP1)	◐CV1/SH-27基板	Aが最小であること





PR－89　BOARD　(Component Side)



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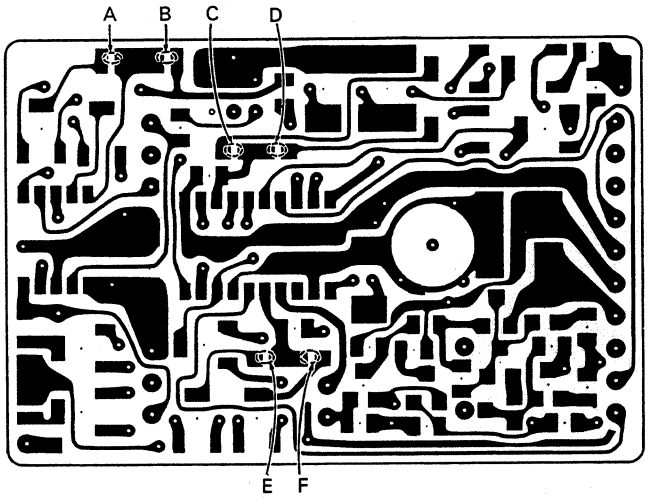
ステップ 3. SET UP調整

・セッティング

レンズ絞り	レンズキャップにてクローズ	測　定　器	波形モニター(WFM)

・準　備

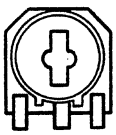
1.下図のように、A部、D部及びF部に半田を付け、B部、C部及びE部の半田をとります。



PR-89 BOARD(Component Side)

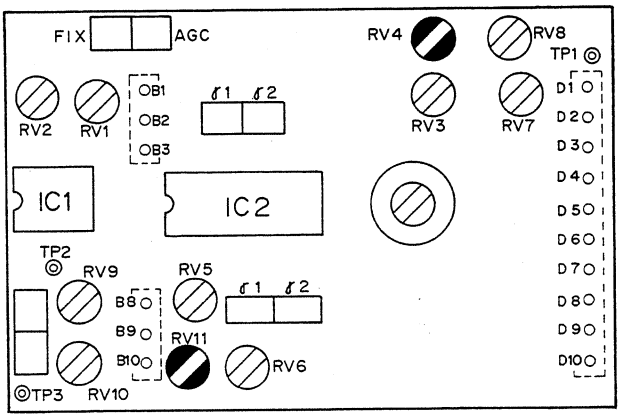
2.◐RV4,◐RV11/PR-89基板をメカニカルセンターにします。

〔真正面〕



〔真上面〕





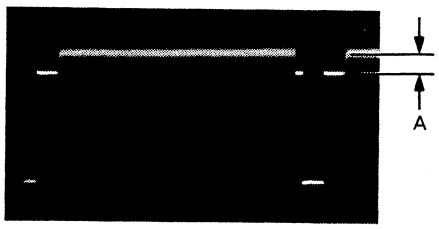
PR－89　BOARD　(Component Side)

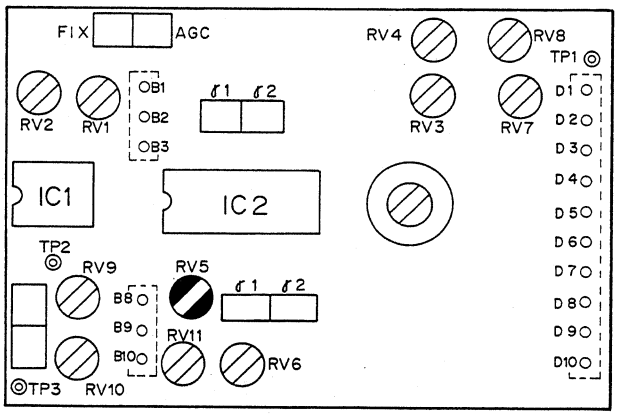
（次ページへ続く）

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・調整手順

測定点	調整箇所	規　格
VIDEO OUT端子	◐RV5/PR-89基板	A＝8.0±0.5 IRE





PR－89　BOARD　(Component Side)

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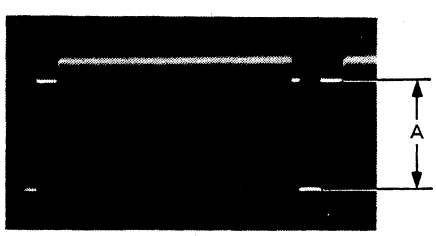
ステップ 4. SYNC調整

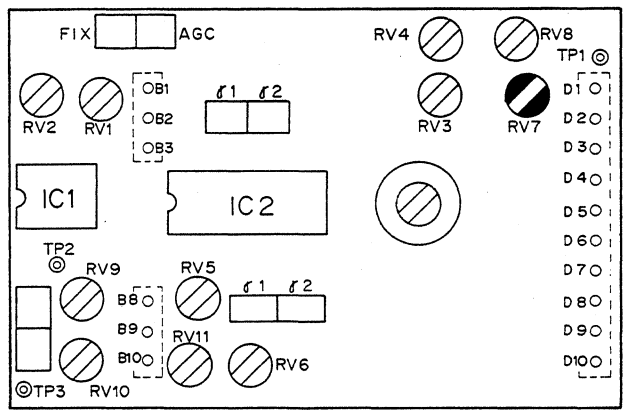
・セッティング

測　定　器	波形モニター(WFM)

・調整手順

測定点	調整箇所	規　格
VIDEO OUT端子	◐RV7/PR-89基板	A=40±10 IRE





PR－89　BOARD　(Component Side)

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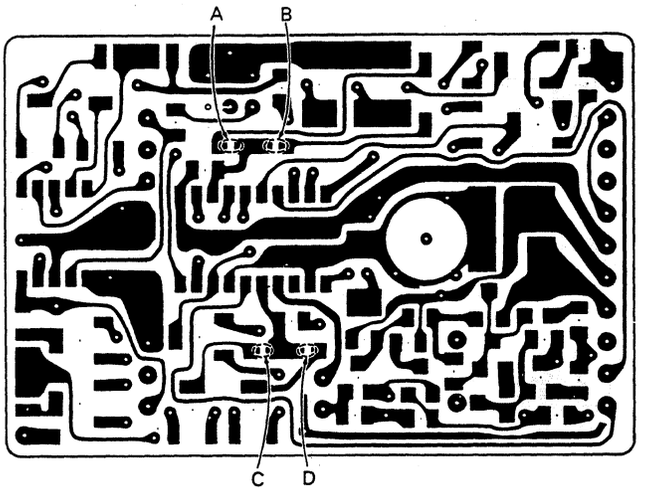
ステップ 5.　GAIN調整

・セッティング

被　写　体	グレースケールチャート	測　定　器	オシロスコープ及び波形モニター

・準備

下図のようにA部、C部に半田を付け、B部、D部の半田をとります。



PR-89 BOARD(Component Side)

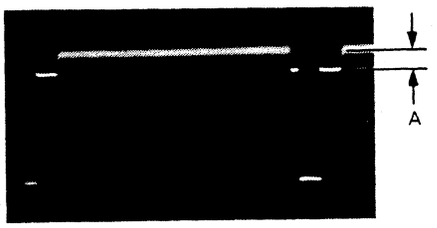
・調整手順

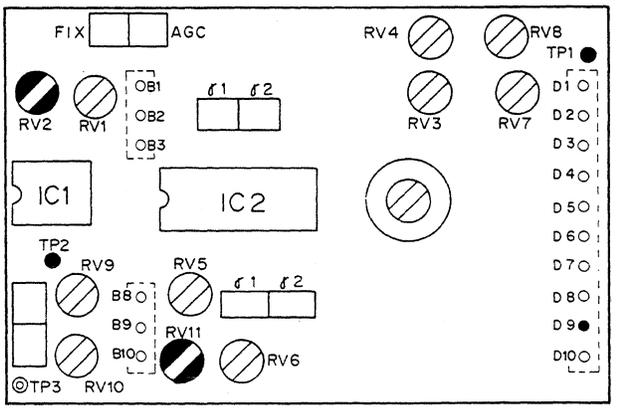
1.レンズ絞り➡レンズキャップにてクローズ

2.測定点：VIDEO OUT 端子

調整箇所：◐RV11/PR-89 基板

規　格：A＝7.0±0.5 IRE

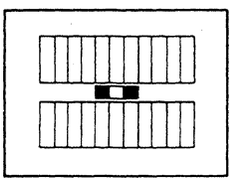




PR－89　BOARD　(Component Side)

3.グレースケールチャートを撮像し、チャートの画枠とモニター画面のアンダースキャン画枠が一致するようにカメラを設置します。

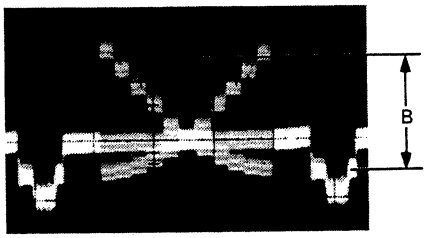
モニター画面

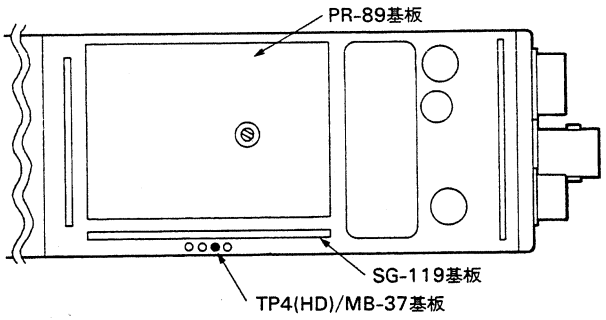


（次ページに続く）

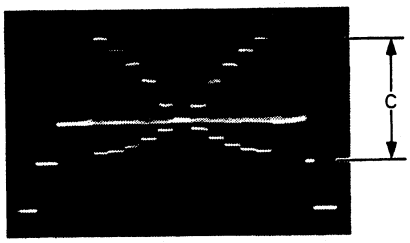
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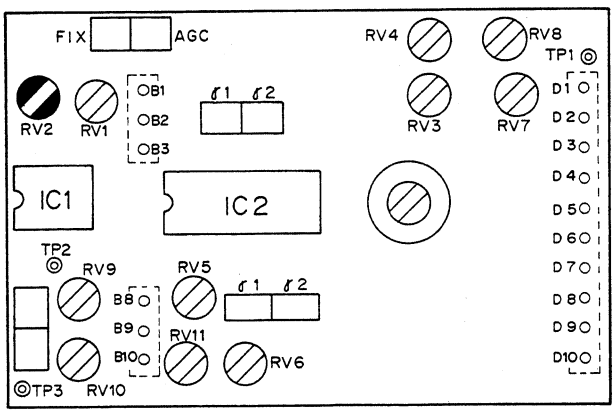
4.測定点：TP2(GND:TP1)/PR-89基板
トリガ：TP4(HD)/MB-136基板
調整箇所：レンズ絞り
規　格：B＝350±10mV





5.測定点：VIDEO OUT端子
調整箇所：◐RV2/PR-89基板
規　格：C＝100±5 IRE





PR－89　BOARD　(Component Side)

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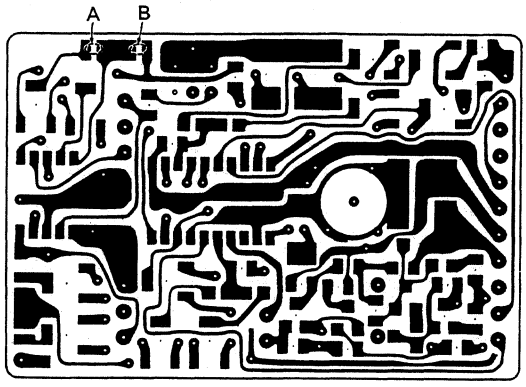
ステップ 6. AGC調整

セッティング

被　写　体	グレースケールチャート	測　定　器	オシロスコープ及び波形モニター

・準備

下図のように、B部に半田をつけ、A部の半田をとります。

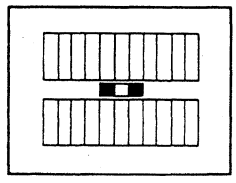


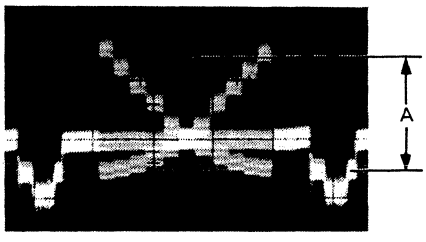
PR-89　BOARD(Component Side)

・調整手順

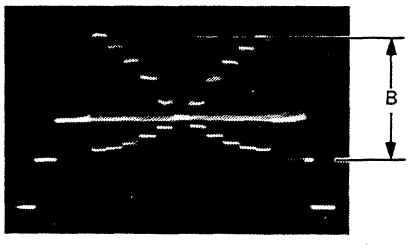
1. グレースケールチャートを撮像し、チャートの画枠とモニター画面のアンダースキャン画枠が一致するようにカメラを設置します。
2. 測定点:TP2(GND:TP1)/PR-89基板
   トリガ:TP4(HD)/MB-136基板
   調整箇所:レンズ絞り
   規　格:A＝350±10mV

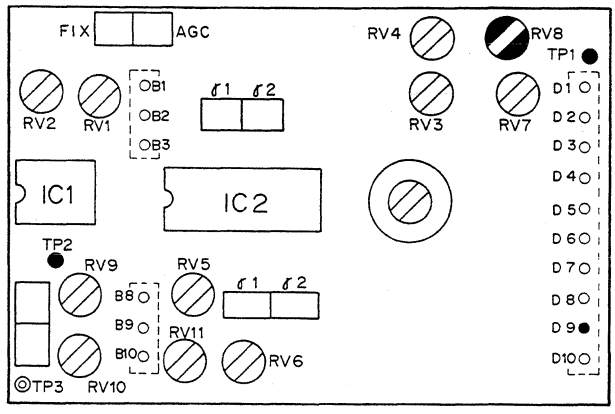
モニター画面





3. 規定点:VIDEO OUT端子
   調整箇所:◐RV8/PR-89基板
   規　格:B＝100±5 IRE





PR－89　BOARD　(Component Side)

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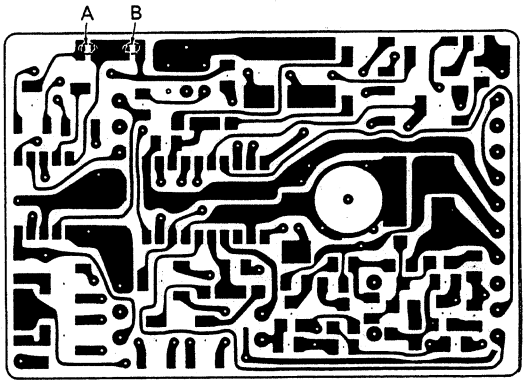
ステップ 7. ホワイトクリップ調整1

・セッティング

被　写　体	グレースケールチャート	測　定　器	波形モニター(WFM)

・準備

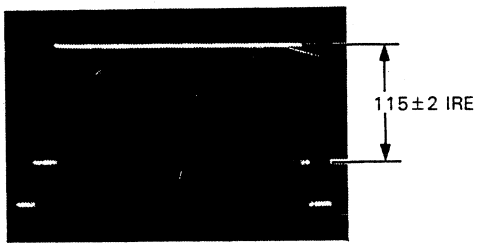
下図のように、A部に半田をつけ、B部の半田をとります。

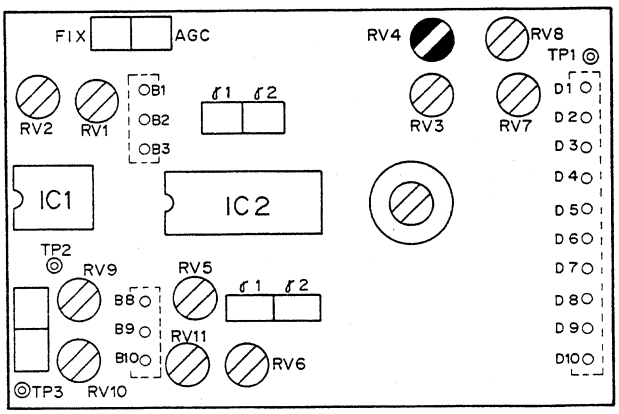


PR-89 BOARD(Component Side)

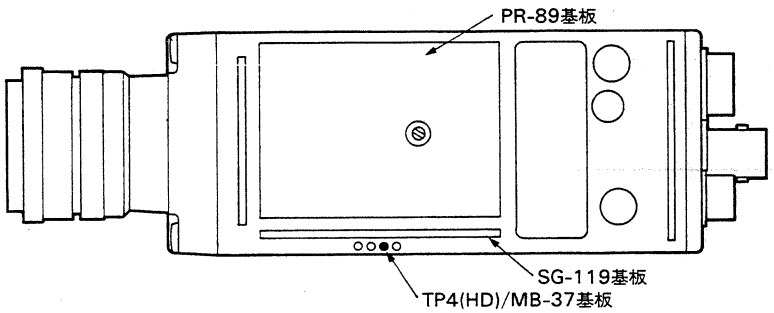
・調整手順

1. グレースケールチャートを撮像し、チャートの画枠とモニター画面のアンダースキャン画枠が一致するようにカメラを設置します。
2. 測定点：VIDEO OUT 端子
   調整箇所：◐RV4/PR-89 基板
   調　整：レンズ絞りを開放し、VIDEO OUTの波形が 115±2 IRE でクリップするように調整します。





PR－89　BOARD　(Component Side)



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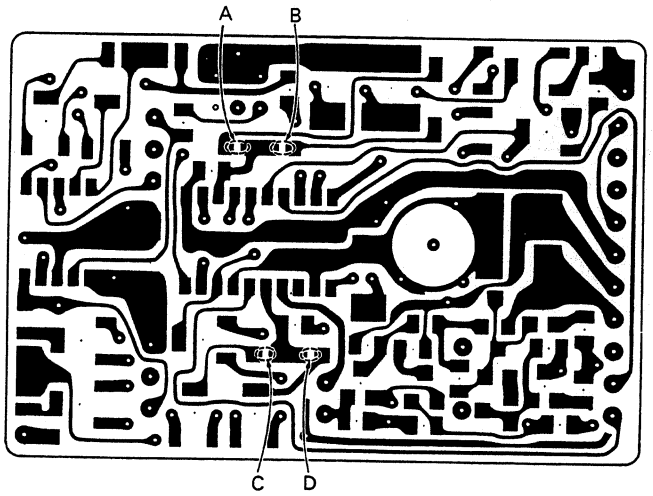
ステップ 8. ガンマ調整

・セッティング

被　写　体	グレースケールチャート	測　定　器	オシロスコープ及び波形モニター

・準備

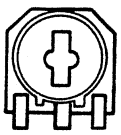
1.下図のように、B部及びD部に半田を付け、A部及びC部の半田をとります。



PR-89 BOARD(Component Side)

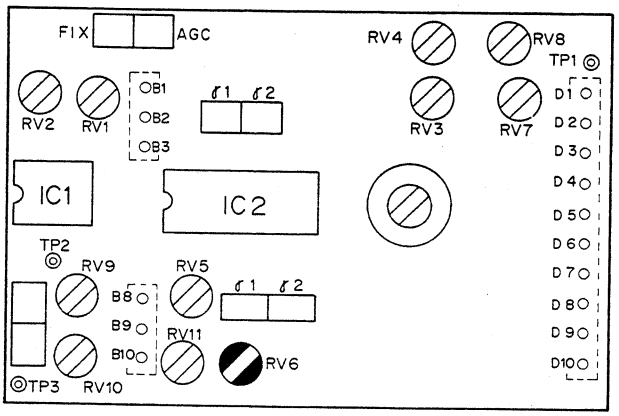
2.◐RV6/PR-89基板をメカニカルセンターにします。

〔真正面〕



〔真上面〕





PR－89　BOARD　(Component Side)

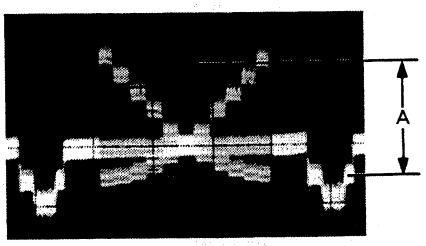
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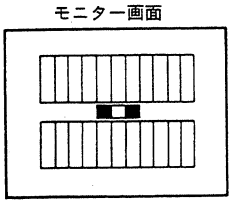
・調整手順

1. グレースケールチャートを撮像し、チャートの画枠とモニター画面のアンダースキャン画枠が一致するようにカメラを設置します。

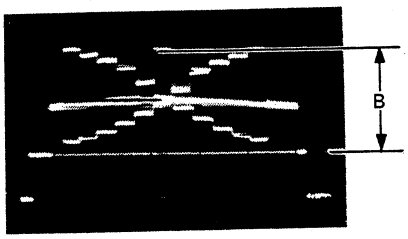
測定点/PR-89基板	調整箇所	規格
TP2(GND:TP1)	レンズ絞り	A＝350±10mV

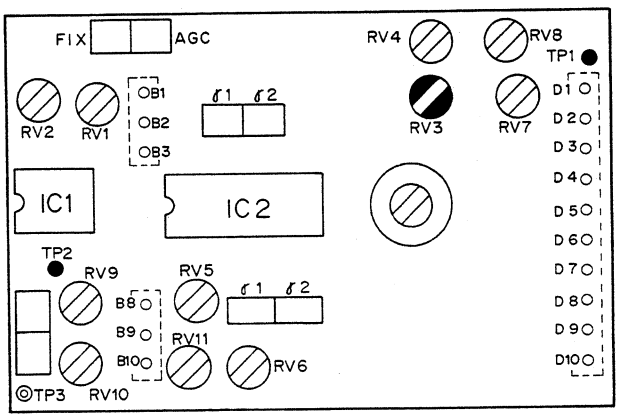


モニター画面



測定点/PR-89基板	調整箇所	規格
VIDEO OUT端子	◐RV3/PR-89基板	B＝100±5 IRE





PR－89 BOARD (Component Side)

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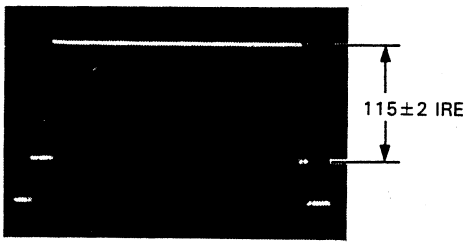
ステップ 9. ホワイトクリップ調整2

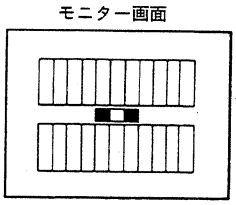
・セッティング

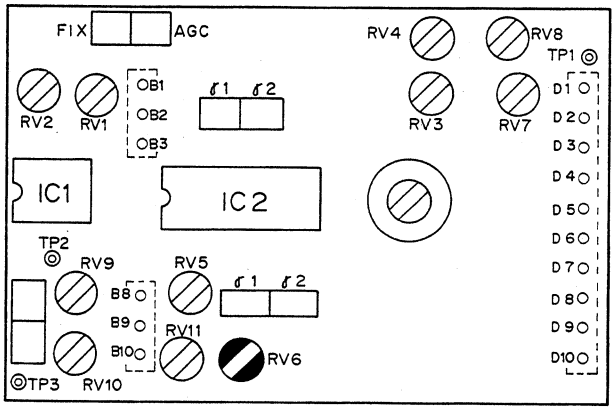
被　写　体	グレースケールチャート	測　定　器	波形モニター(WFM)

・調整手順

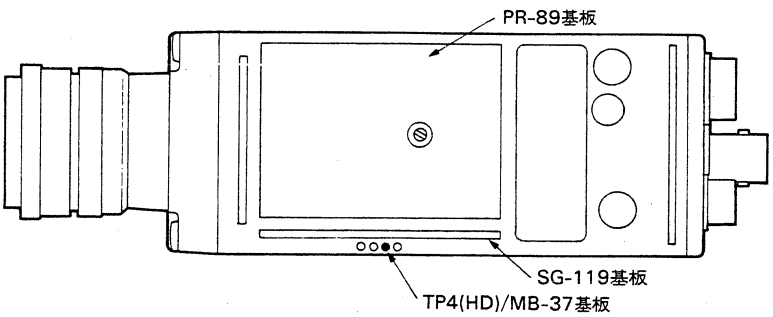
1. グレースケールチャートを撮像し、チャートの画枠とモニター画面のアンダースキャン画枠が一致するようにカメラを設置します。
2. 測定点VIDEO OUT端子
   調整箇所: ◐RV6/PR-89基板
   調　整：レンズ絞りを開放にし、VIDEO OUTの波形が115±2 IREでクリップするように調整します。







PR－89　BOARD　(Component Side)



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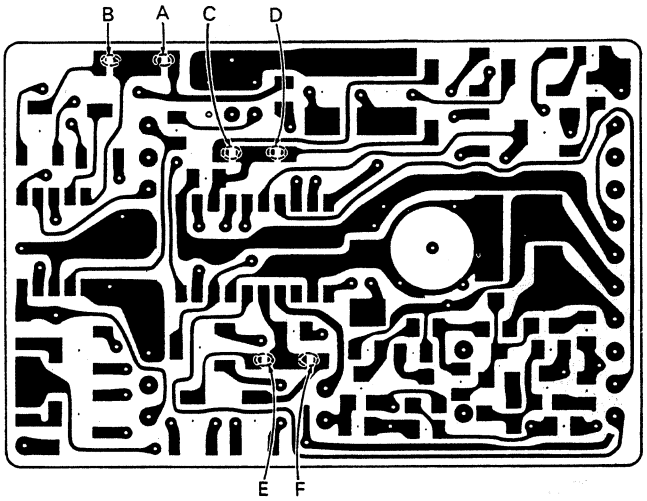
ステップ10. GAIN LIMIT調整

・セッティング

被　写　体	ホワイトウィンドゥチャート	測　定　器	オシロスコープ及び波形モニター

・準備

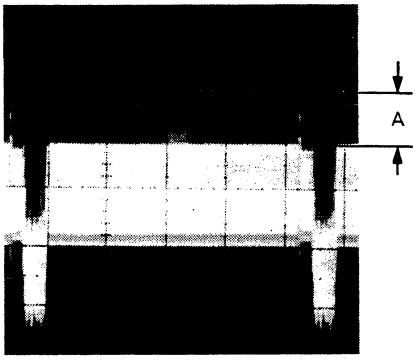
下図のように、A部、C部及びE部に半田を付け、B部、D部及びF部の半田をとります。



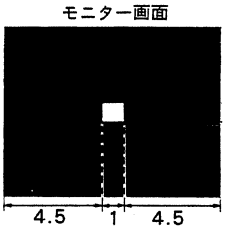
PR-89 BOARD(Component Side)

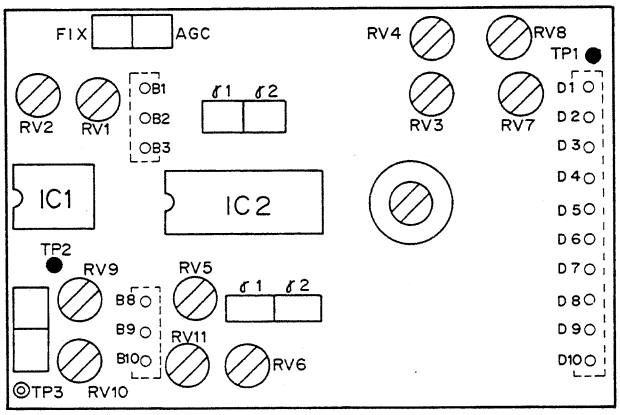
・調整手順

1. ホワイトウィンドウチャートを右図のように撮像します。
2. 測定点:TP2(GND:TP1)/PR-89基板
   トリガ:TP4(HD)/MB-136基板
   調整箇所:レンズ絞り
   規　格:A＝50±10mV



モニター画面



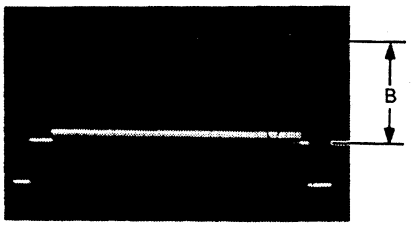


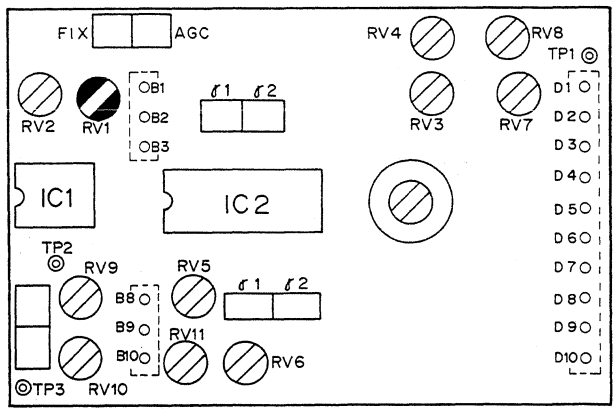
PR－89　BOARD　(Component Side)

規格を満足出来ない場合
・パターンボックスがPTB-100の時
⇨パターンボックスの輝度ボリュームで規格に合わせる。
・パターンボックスがPTB-500の時
⇨レンズの口径に合ったND-4フィルターをレンズにかぶせて再調整する。
・電球100Wを使用の時
⇨スライダックにて規格に合わせる。

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3. 測定点:VIDEO OUT端子
調整箇所:◐RV1/PR-89基板
規　　格:B＝100±10 IRE





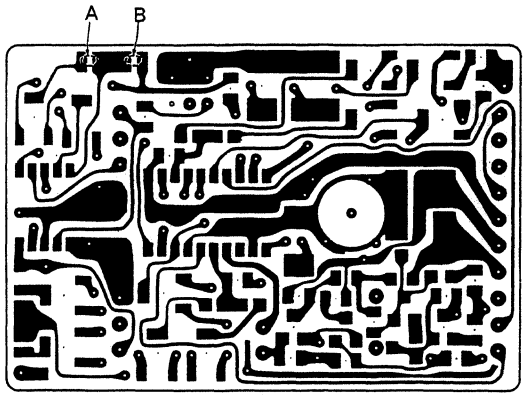
PR－89　BOARD　(Component Side)

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ステップ11. 調整後のセッティング

・セッティング

下図のように、A部に半田をつけ、B部の半田をとります。



PR-89 BOARD(Component Side)

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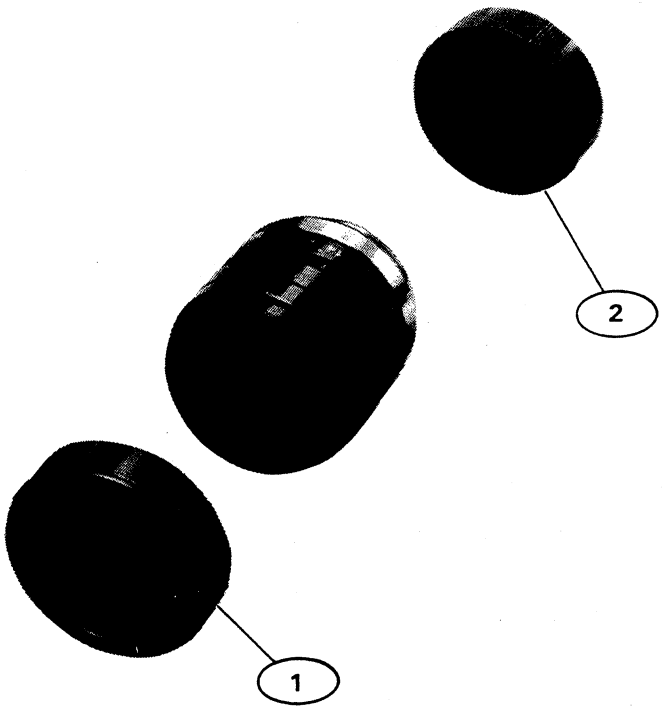
STANDARD LENS
VCL-16Y-M

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LENS

Standard Lens(VCL-16Y-M)

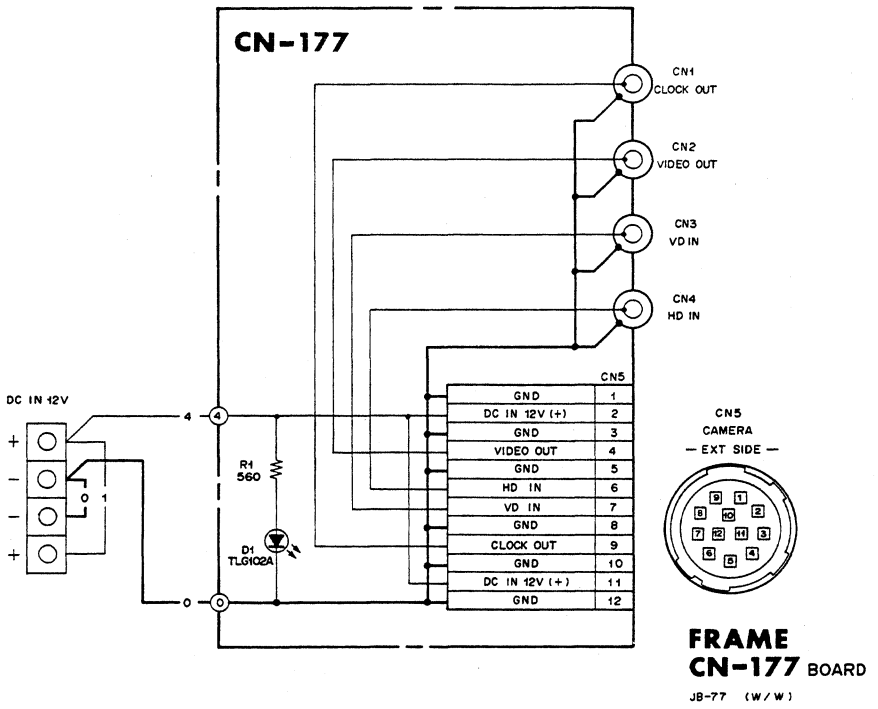
No.	Parts No.	Description	
1	3-707-313-01	CAP, FRONT (FOR VCL-16Y-M)	A
2	3-707-314-01	CAP, REAR	A



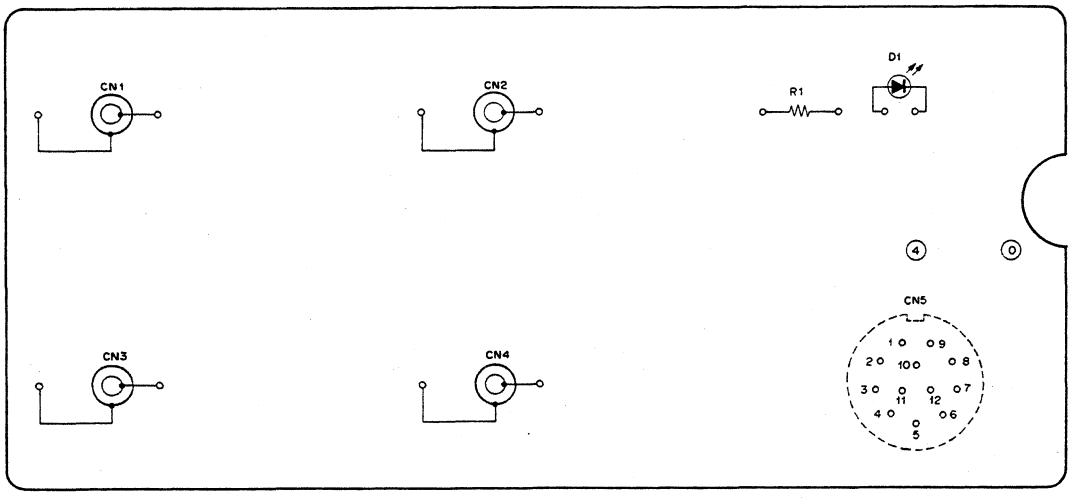
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SCHEMATIC DIAGRAM & MOUNTING DIAGRAM

JUNCTION BOX(JB-77)



FRAME
CN-177 BOARD
JB-77 (W/W)



CN-177 BOARD
— SOLDERING SIDE —
1-621-376-11
JB-77 (W/W)

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ELECTRICAL PARTS LIST

Ref. No.	Parts No.	Description
CN-177 BOARD		
	1-621-376-11	PRINTED CIRCUIT BOARD "CN-177"
D1	**8-719-800-33**	**TLG102A**
R1	**1-249-414-11**	**CARBON 560 5% 1/6 W**
FRAME		
	1-537-047-11	TERMINAL BOARD "DC IN +12V"
CN1	**1-562-382-12**	**RECEPTACLE, BNC "CLOCK OUT"**
CN2	**1-562-382-12**	**RECEPTACLE, BNC "VIDEO OUT"**
CN3	**1-562-382-12**	**RECEPTACLE, BNC "VD IN"**
CN4	**1-562-382-12**	**RECEPTACLE, BNC "HD IN"**
CN5	1-562-221-31	RECEPTACLE, 12P "CAMERA"

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TABLE OF CONTENTS

SCHEMATIC DIAGRAM & MOUNTING DIAGRAM ·····1
ELECTRICAL PARTS LIST·····2

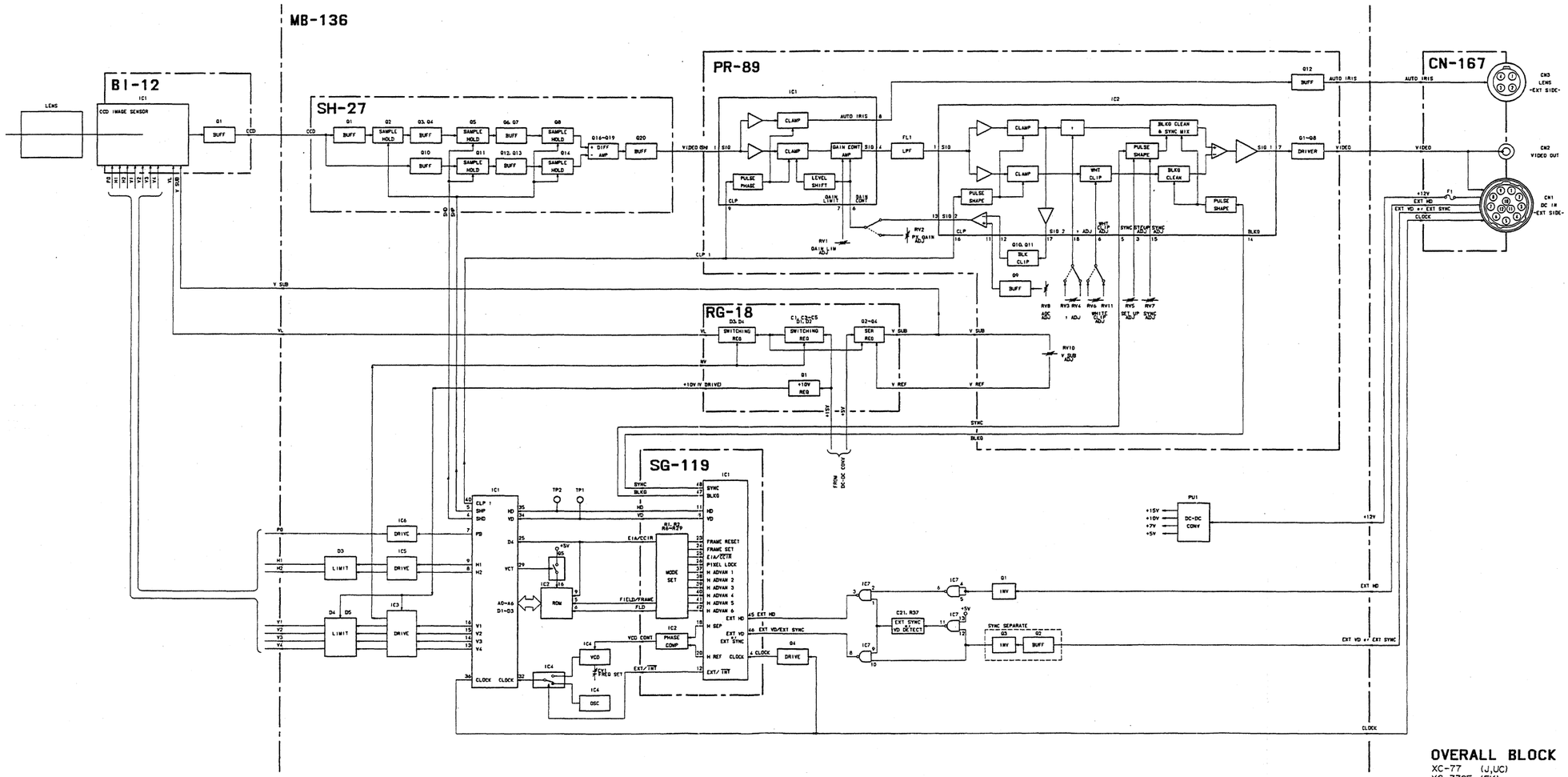
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JUNCTION BOX
JB-77

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SECTION A
DIAGRAM

A-1. BLOCK DIAGRAM



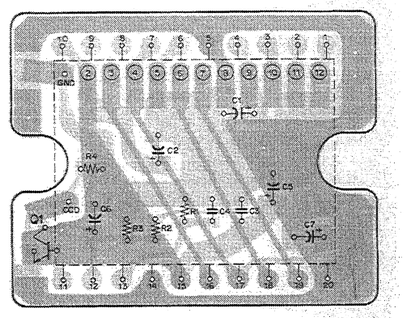
OVERALL BLOCK
XC-77 (J,UC)
XC-77CE (EK)

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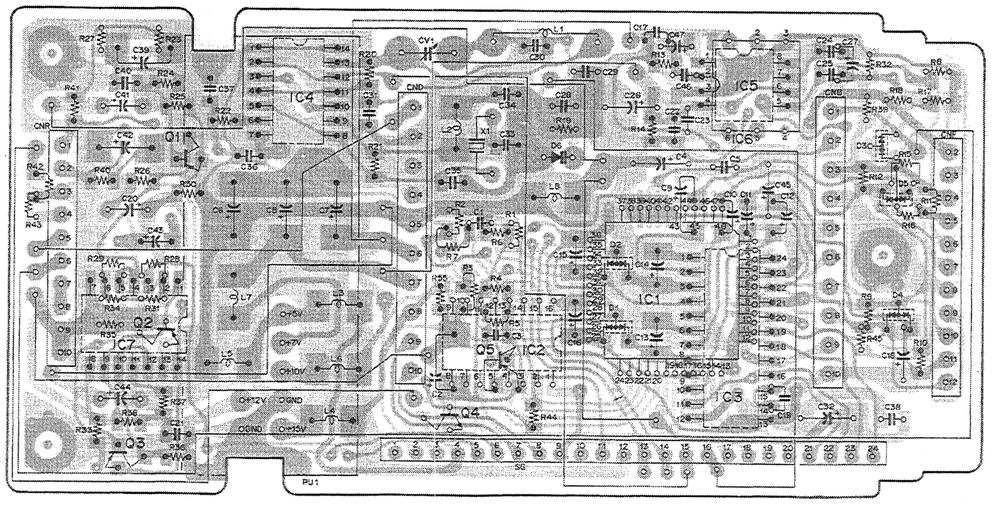
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A-2. MOUNTING DIAGRAM

BI-12 BOARD
CN-167 BOARD
MB-136 BOARD
PR-89 BOARD
RG-18 BOARD
SG-119 BOARD
SH-27 BOARD



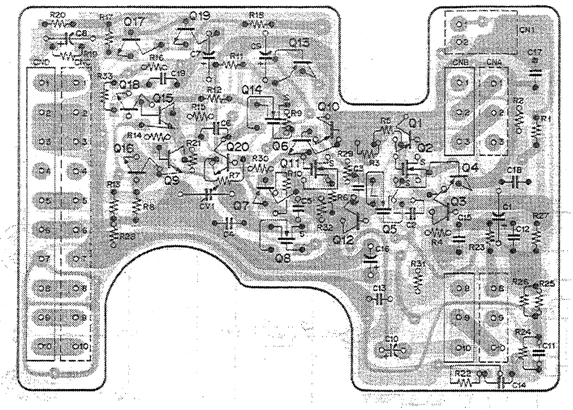
BI-12 BOARD
—SOLDERING SIDE—
1-621-913-11,12
XC-77 (J,UC)
XC-77CE (EK)



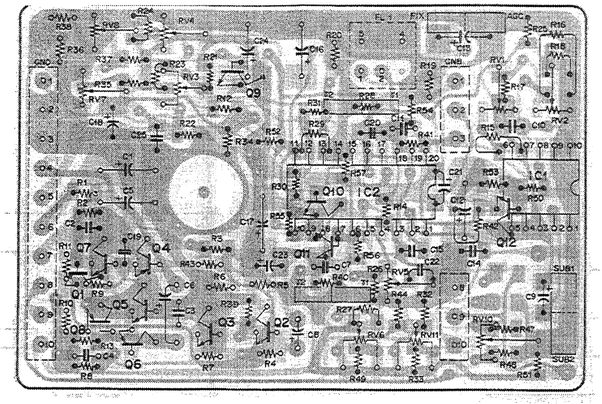
MB-136 BOARD
— SOLDERING SIDE —
1-621-909-11,12
XC-77 (J,UC)
XC-77CE (EK)

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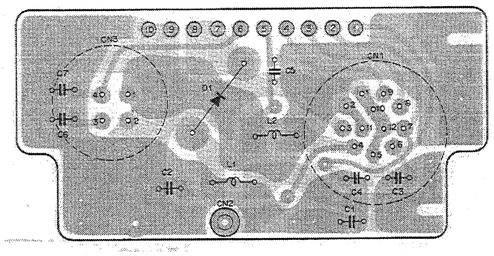
MOUNTING DIA MOUNTING DIA



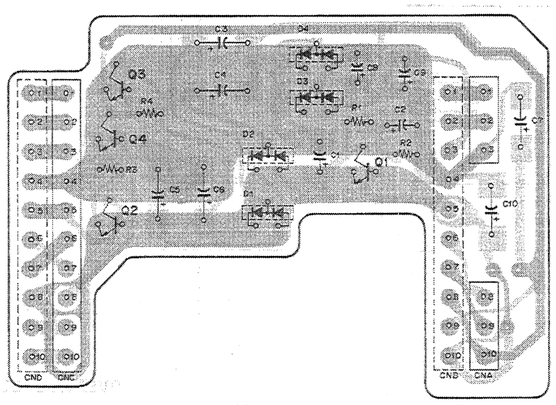
SH-27 BOARD
— SOLDERING SIDE —
1-621-911-11,12
XC-77 (J,UC)
XC-77CE (EK)



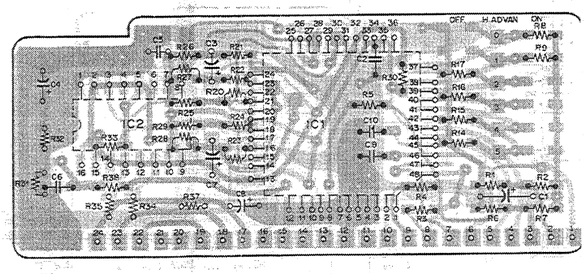
PR-89 BOARD
— SOLDERING SIDE —
1-621-909-11,12
XC-77 (J,UC)
XC-77CE (EK)



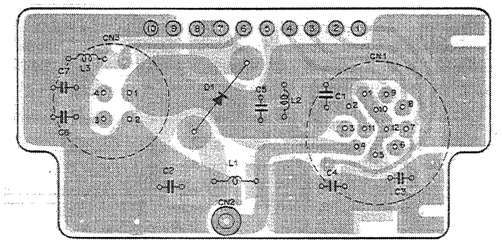
CN-167 BOARD
—SOLDERING SIDE —
1-621-914-11
XC-77 (J,UC) 10001~10100



RG-18 BOARD
– SOLDERING SIDE –
1-621-912-11
XC-77 (J,UC)



SG-119 BOARD
— SOLDERING SIDE –
1-621-910-11,12
XC-77 (J,UC)
XC-77CE (EK)

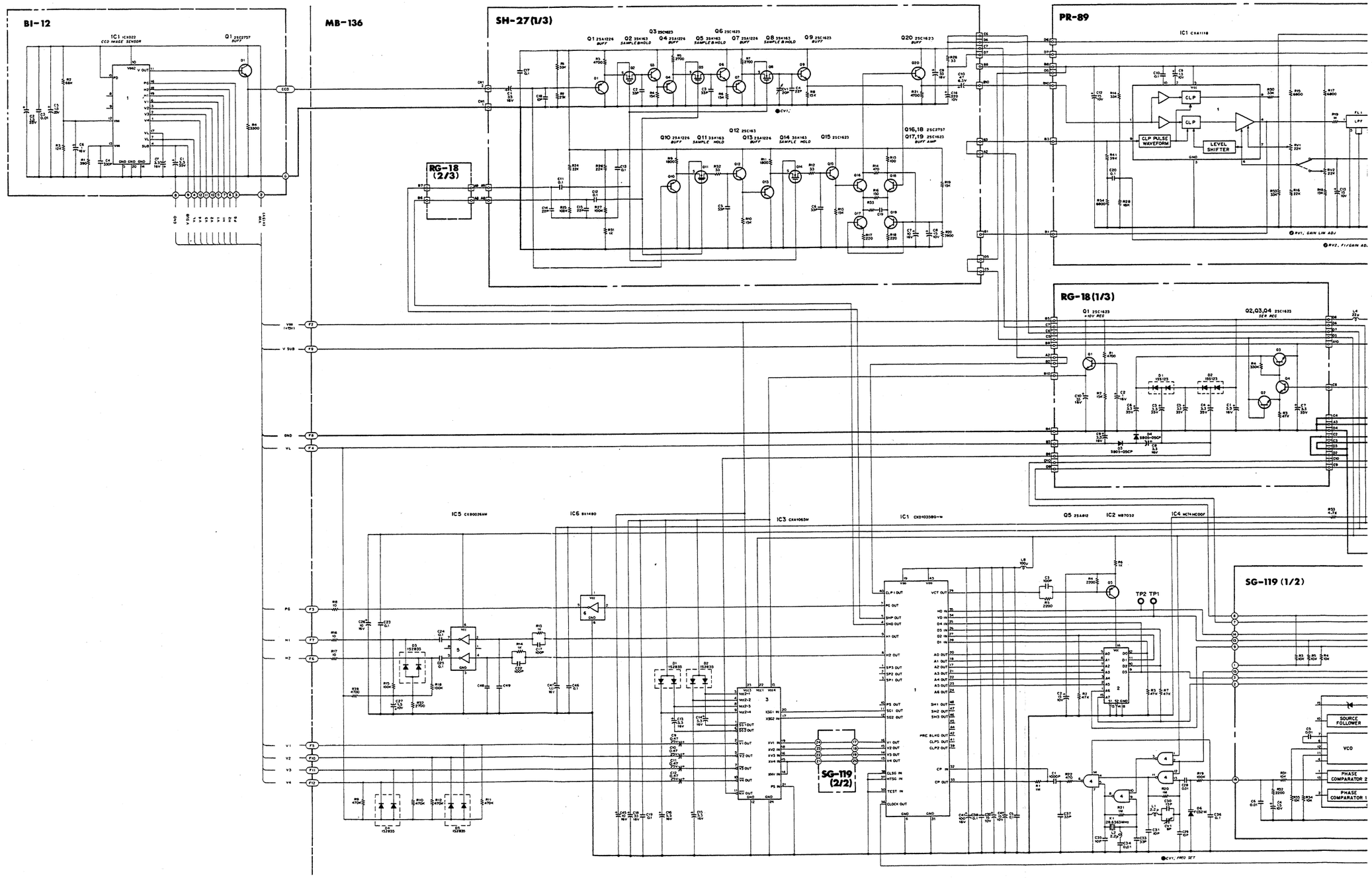


CN-167 BOARD
—SOLDERING SIDE —
1-621-914-12
XC-77 (J,UC) 10101 ~
XC-77CE (EK) 10001 ~

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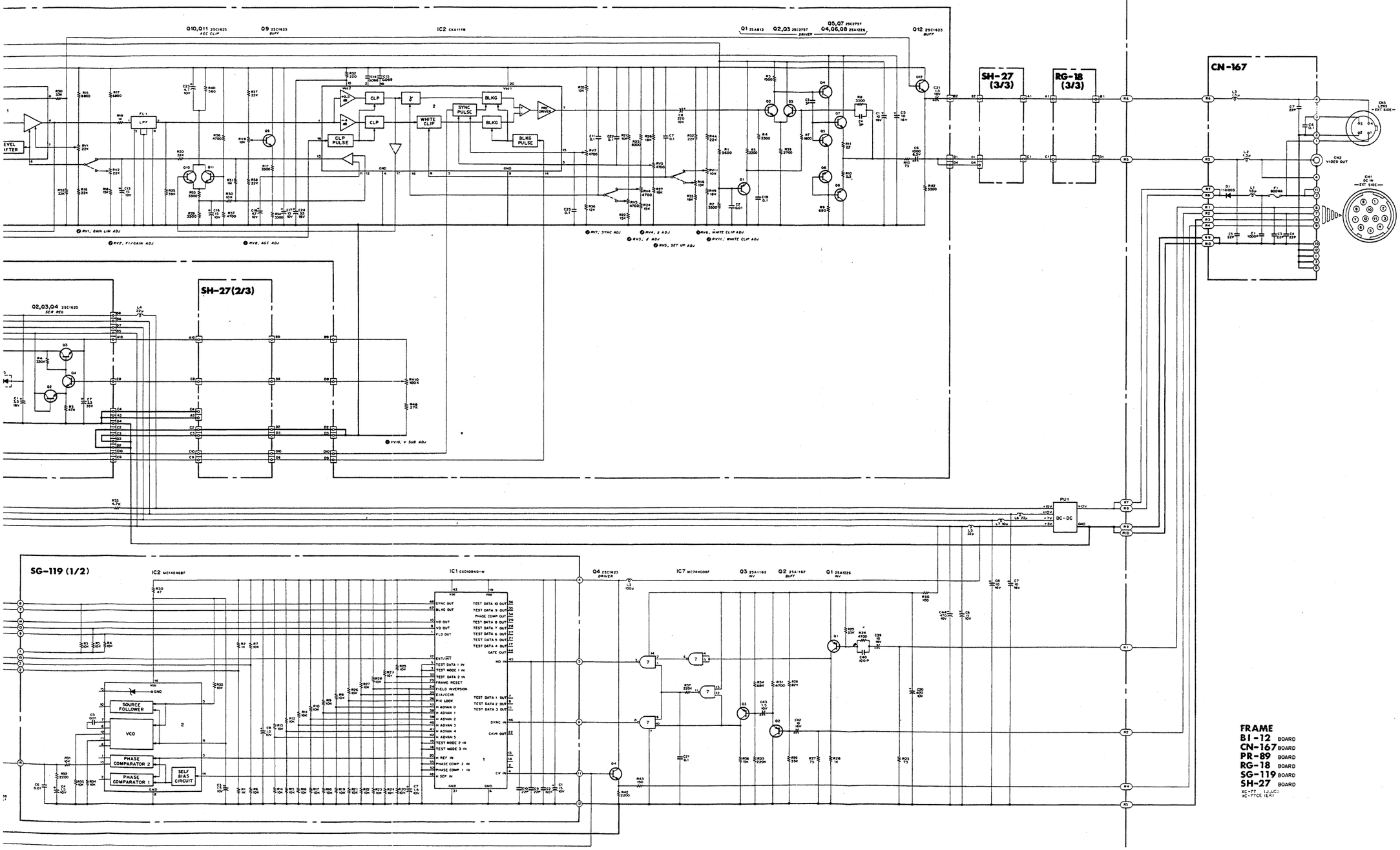
FRAME FRAME

A-3. SCHEMATIC DIAGRAM



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FRAME FRAME



FRAME
B1-12 BOARD
CN-167 BOARD
PR-89 BOARD
RG-18 BOARD
SG-119 BOARD
SH-27 BOARD
XC-77 (J,UC)
XC-77CE (EK)

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SECTION B
SEMICONDUCTOR

The circuit diagram of IC is obtaind from the IC data book published by the manufacturer.

TYPE PAGE

11DQ03..... B-2
1S2835..... B-2
1SS123..... B-2

2SA1162G..... B-2
2SA1226..... B-2
2SA812..... B-2

2SC1623..... B-2
2SC2757..... B-2

3SK263..... B-2

BX1480..... B-3

CXA1065M..... B-3
CXA1118M..... B-3
CXA1119M..... B-3

CXB0026AM.... B-4
CXD1035BQ-W.. B-4

FC52M..... B-2

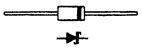
MB7052PF..... B-9

MC14046BCP... B-9

SB05-05CP.... B-2

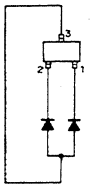
TC74HC00F.... B-9

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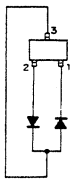


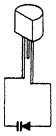
11D003

TOP VIEW (SCALE 4/1) 1S2835



TOP VIEW (SCALE 4/1) 1SS123





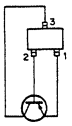
FC52M

TOP VIEW (SCALE 4/1) SB05-05CP



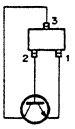
144-1

TOP VIEW (SCALE 4/1)

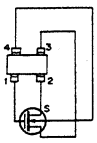


2SA1162G
2SA1226
2SA812

TOP VIEW (SCALE 4/1)



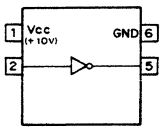
2SC1623
2SC2757



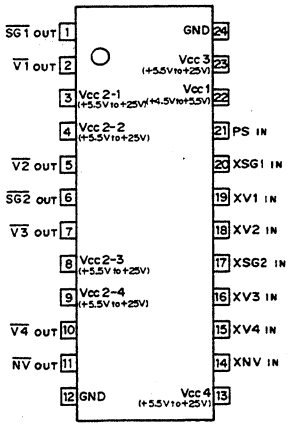
3SK163

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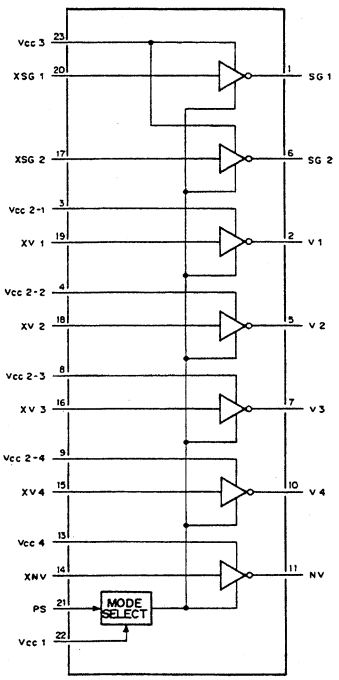
BX1480 (SONY)
PRECHARGE GATE DRIVER
— TOP VIEW —



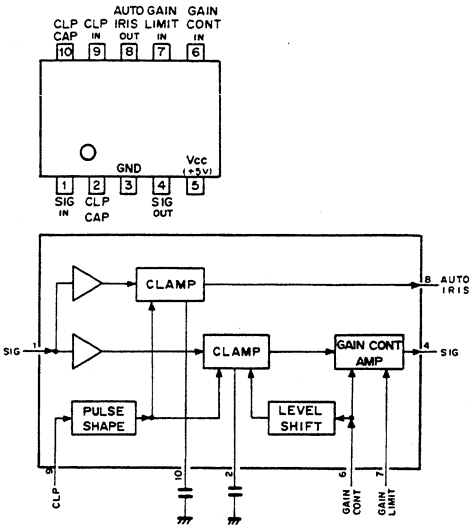
CXA1065M (SONY) FLAT PACKAGE
INVERTING DRIVER FOR CCD CLOCK WITH POWER SAVE
— TOP VIEW —



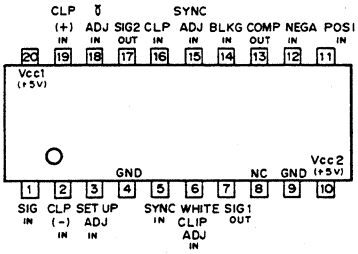
XV1-XV4 ; VERTICAL REGISTER TRANSMISSION CLOCK INPUT
V1 - V4 ; VERTICAL REGISTER TRANSMISSION CLOCK OUTPUT
XSG1, XSG2 ; SENSER GATE PULSE INPUT
SG1, SG2 ; SENSER GATE PULSE OUTPUT
XNV ; DRIVER INPUT
NV ; DRIVER OUTPUT
PS ; POWER SAVE INPUT
Vcc 1 ; BIAS VOLTAGE
Vcc 2-1 ; V1 OUTPUT PULSE VOLTAGE
Vcc 2-2 ; V2 OUTPUT PULSE VOLTAGE
Vcc 2-3 ; V3 OUTPUT PULSE VOLTAGE
Vcc 2-4 ; V4 OUTPUT PULSE VOLTAGE
Vcc 3 ; SG1, SG2 OUTPUT PULSE VOLTAGE
Vcc 4 ; NV OUTPUT PULSE VOLTAGE

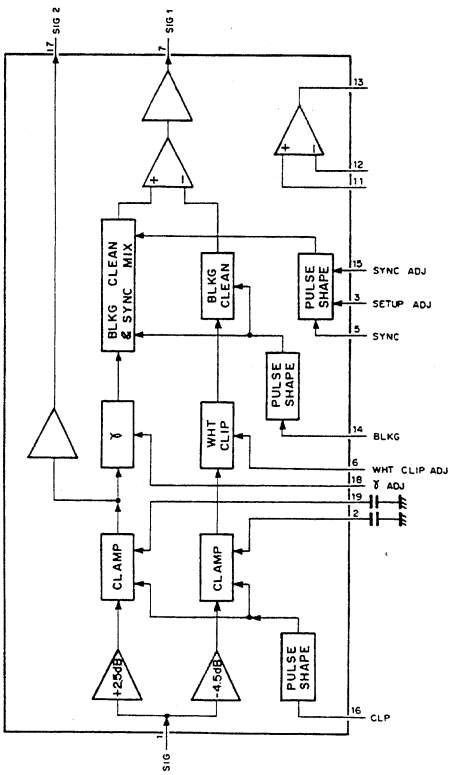


CXA1118M (SONY) FLAT PACKAGE
IRIS DRIVER/GAIN CONTROL AMPLIFIER



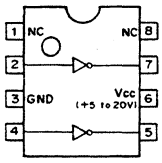
CXA1119M (SONY) FLAT PACKAGE
VIDEO SIGNAL PROCESSOR



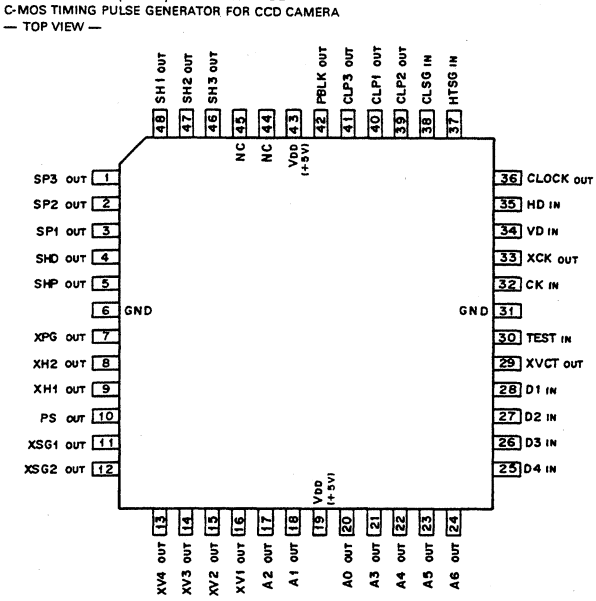


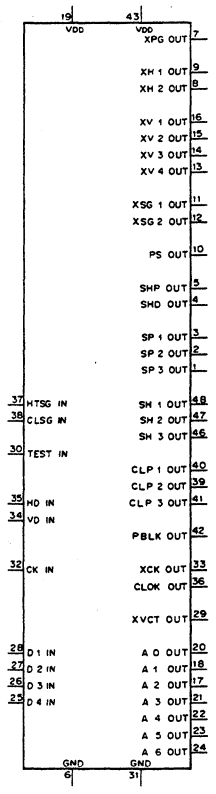
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CXB0026AM (SONY) FLAT PACKAGE
BIPOLAR MOS CLOCK DRIVER
— TOP VIEW —



CXD1035BQ-W (SONY) FLAT PACKAGE
C-MOS TIMING PULSE GENERATOR FOR CCD CAMERA
— TOP VIEW —





D1~D4 : EXTERNAL ROM DATA INPUT
A0~A6 : EXTERNAL ROM ADDRESS OUTPUT

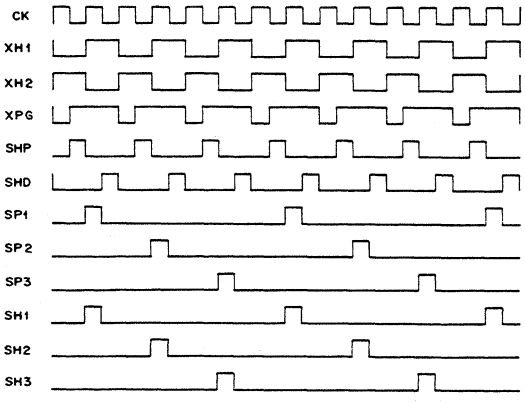
MODE SELECTION WITHOUT ROM

	H	L
D1	※	
D2	1-CHIP COLOR	B/W 3-CHIP COLOR
D3	FRAME	FIELD
D4	EIA (NTSC, PALM)	CCIR(PAL, SECAM)

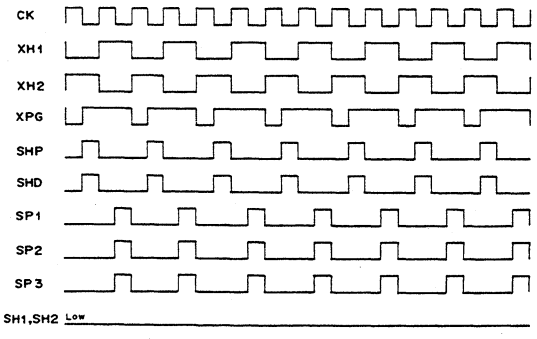
H : VDD
L : GND

※ ROM OFF 時には D1 は 必ず LOW にする
Connect D1 to GND without ROM (ROM OFF)

1-CHIP COLOR

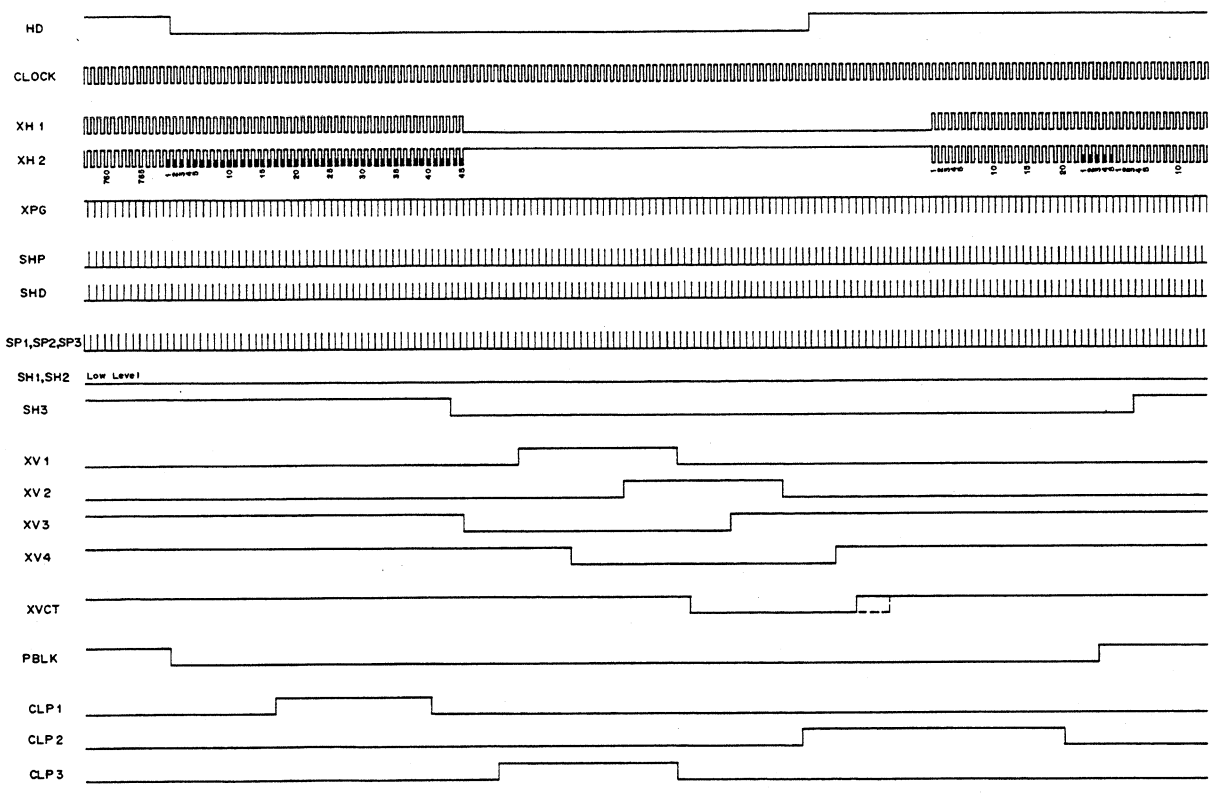


B/W 3-CHIP COLOR

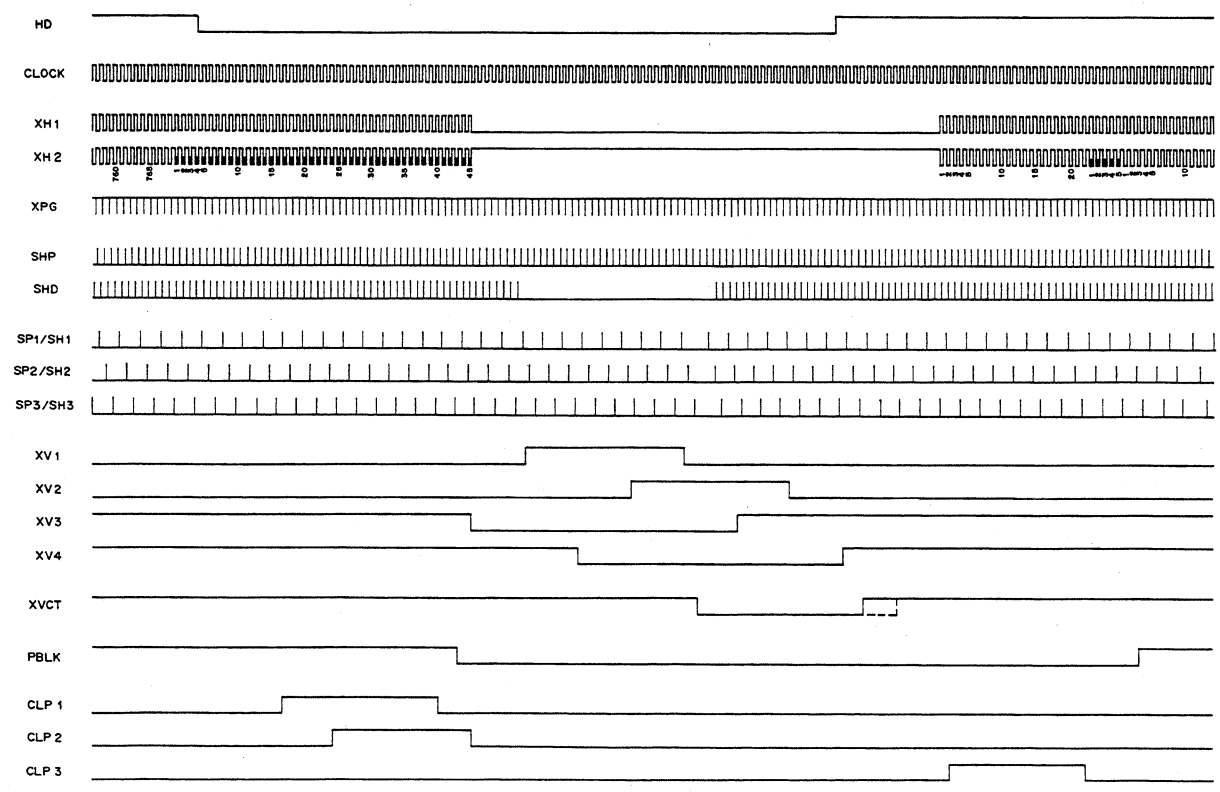


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EIA (NTSC,PALM) B/W,3-HIP COLOR

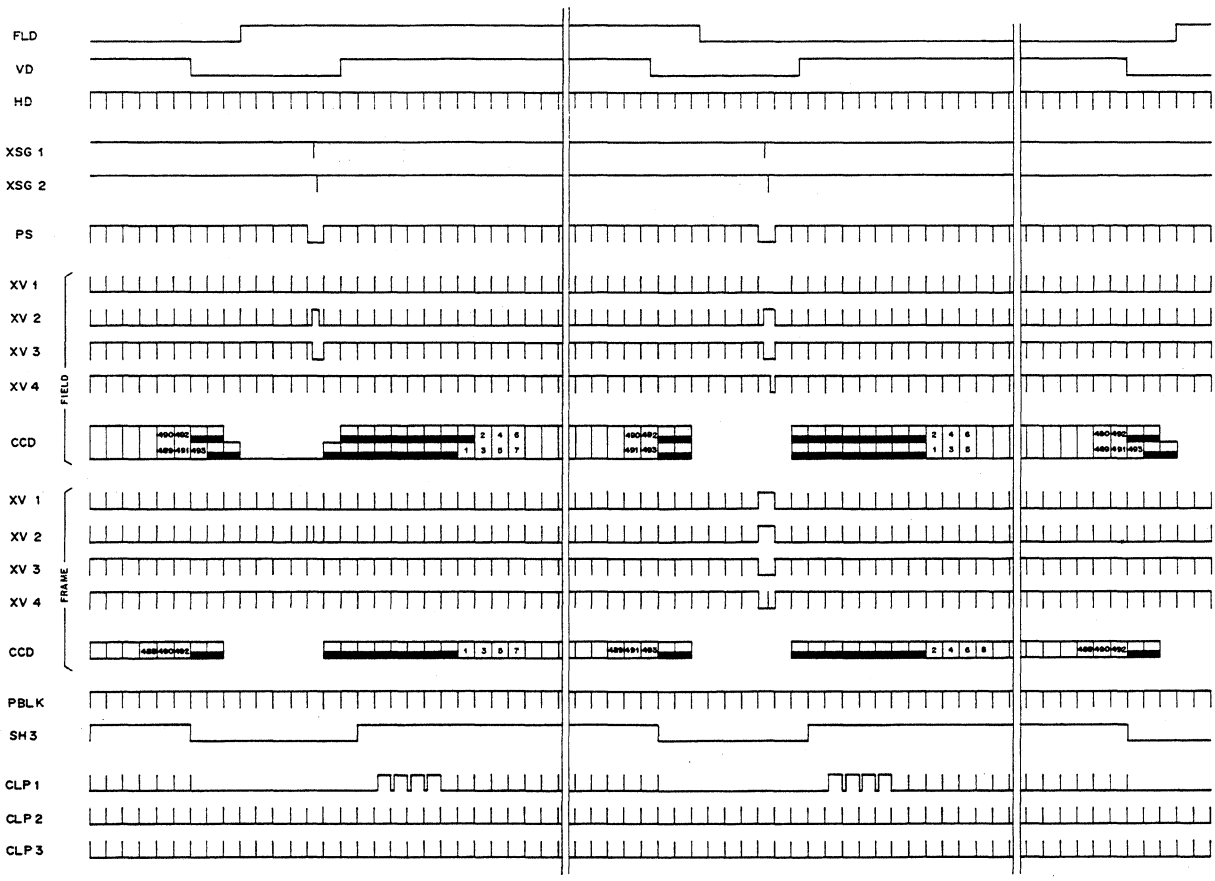


EIA(NTSC,PALM) 1-CHIP COLOR

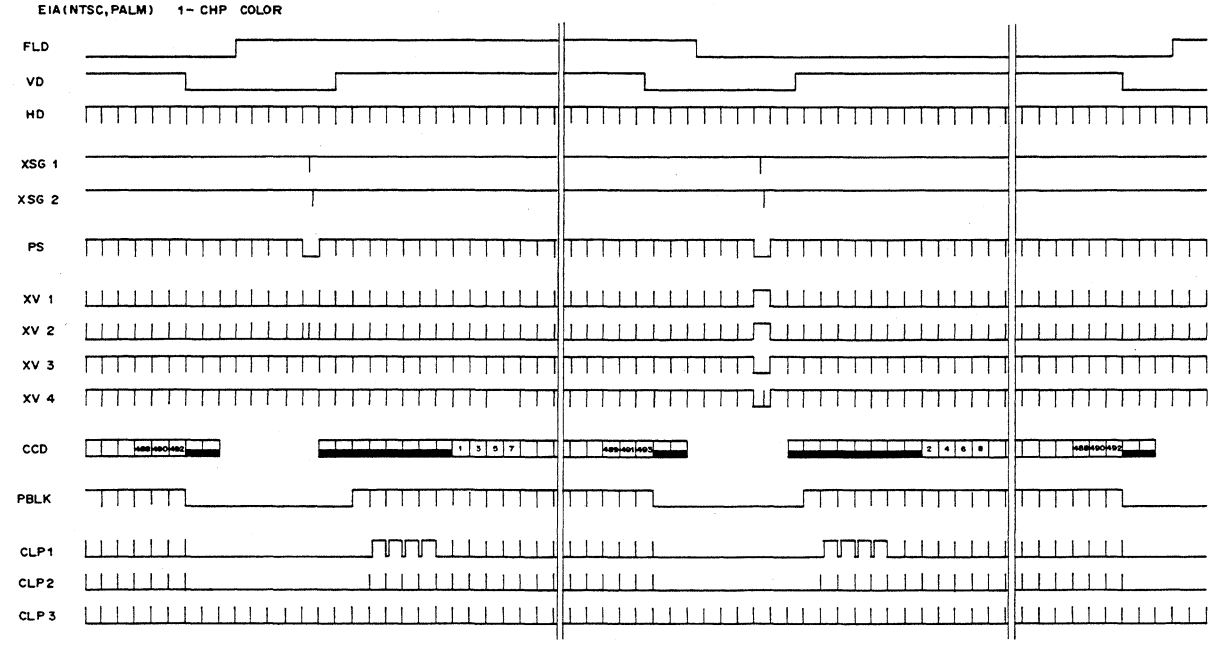


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EIA(NTSC,PALM) B/W,3-CHIP COLOR

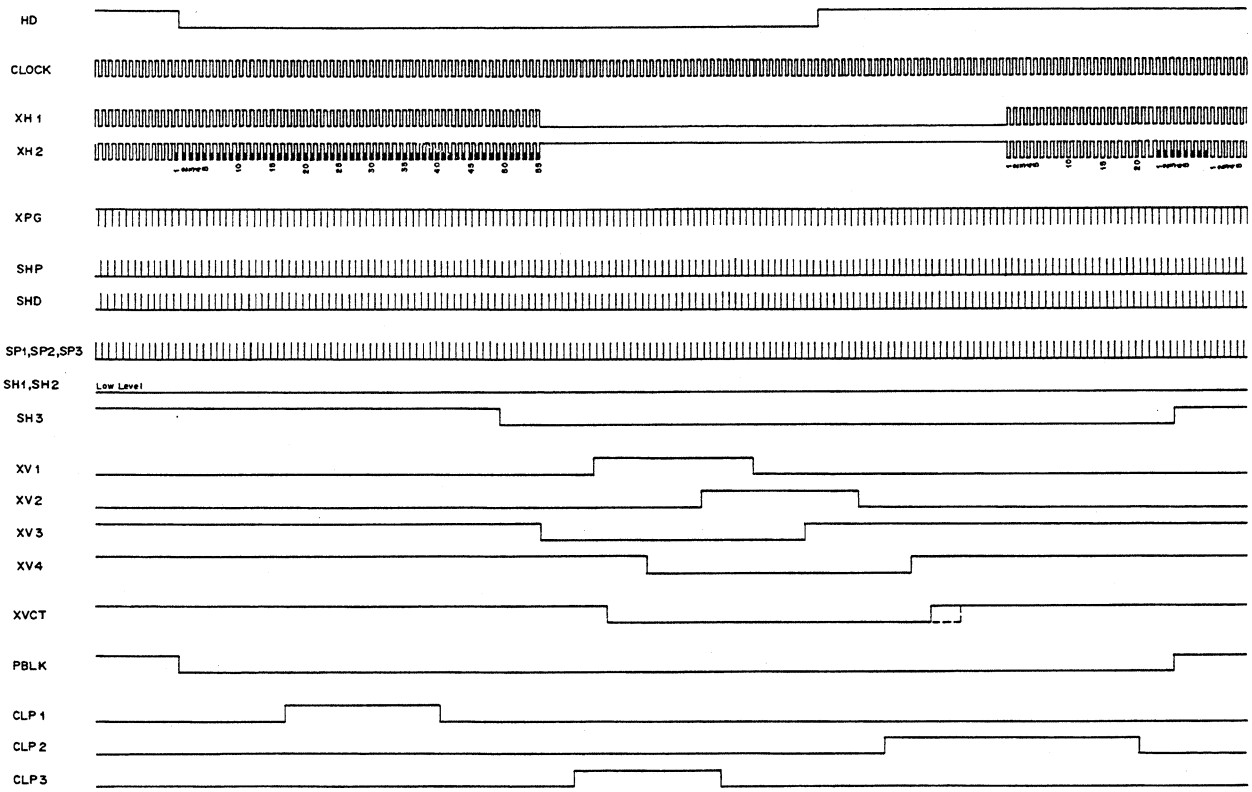


EIA(NTSC,PALM) 1-CHP COLOR

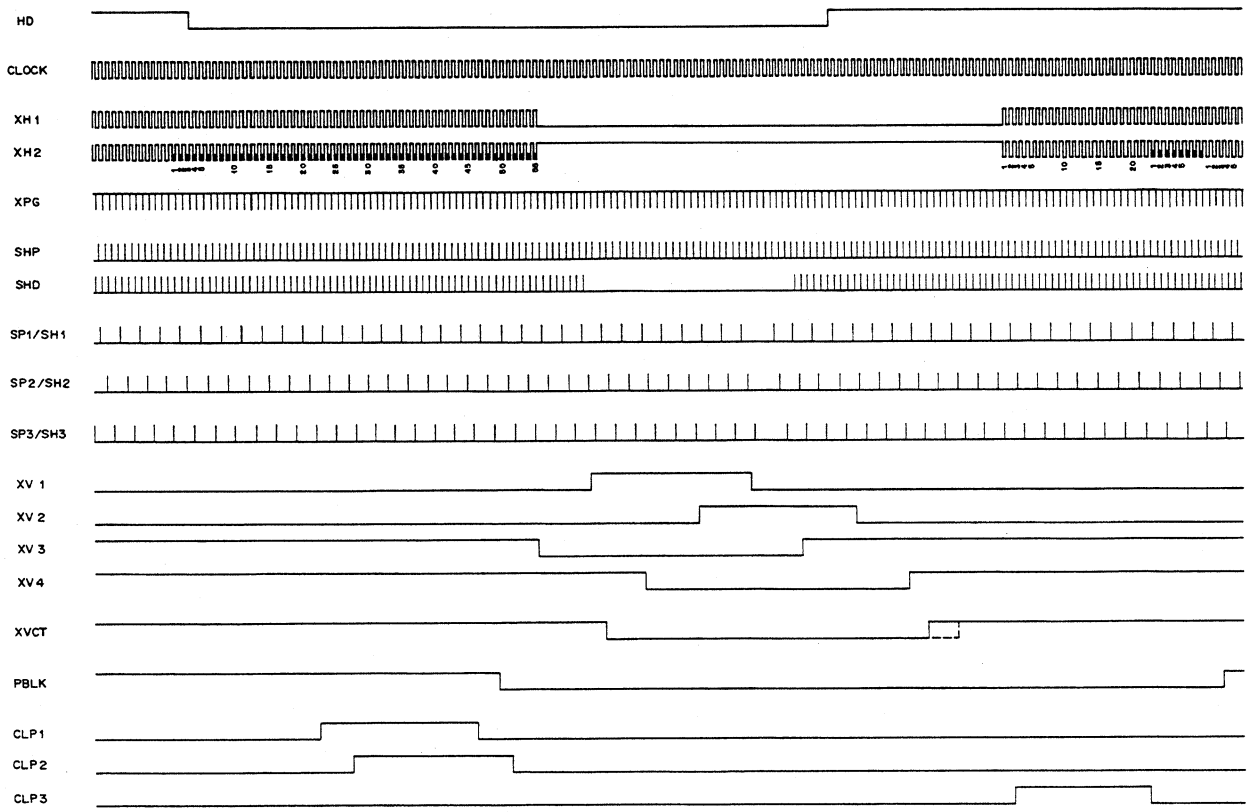


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CCIR (PAL, SECAM) B/W, 3CHIP COLOR

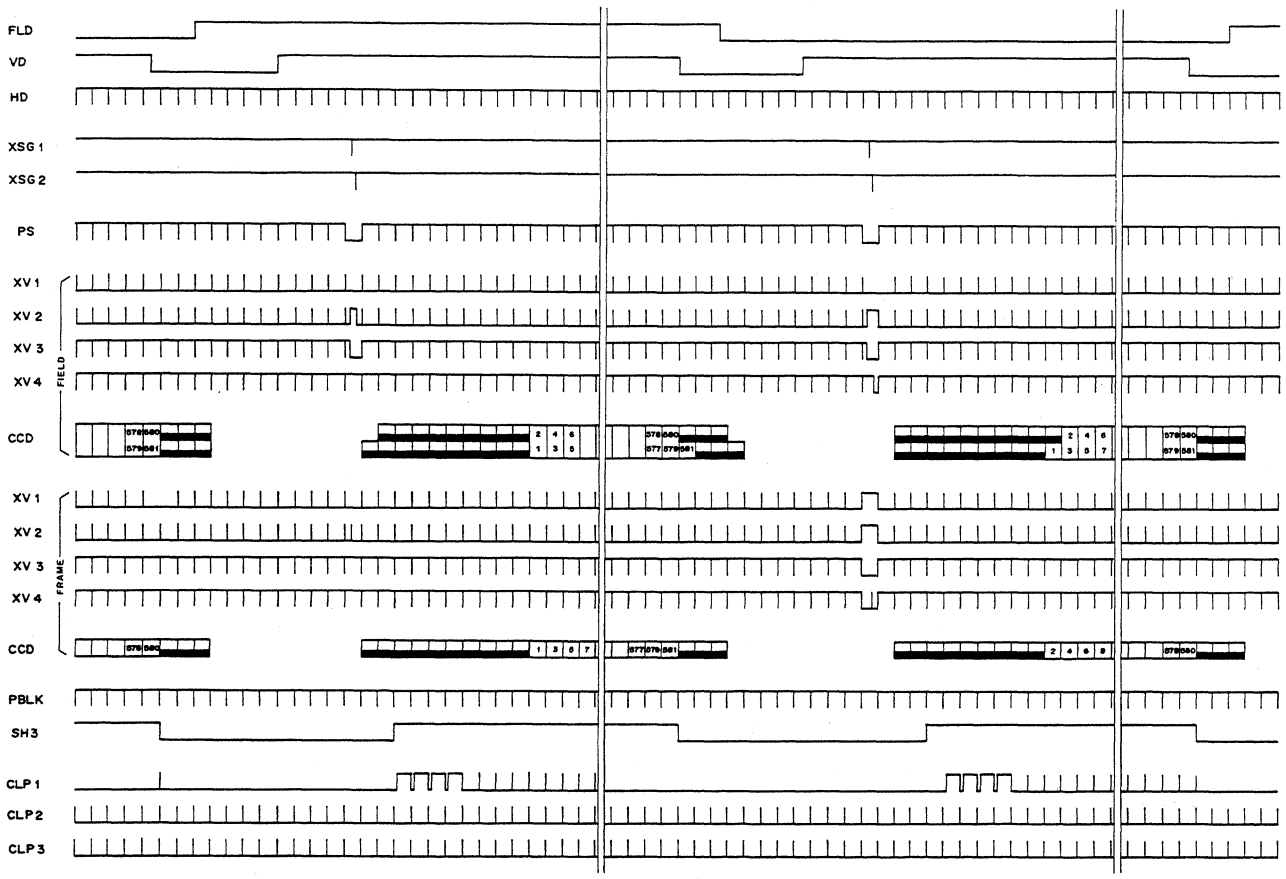


CCIR (PAL, SACAM) 1-CHIP COLOR

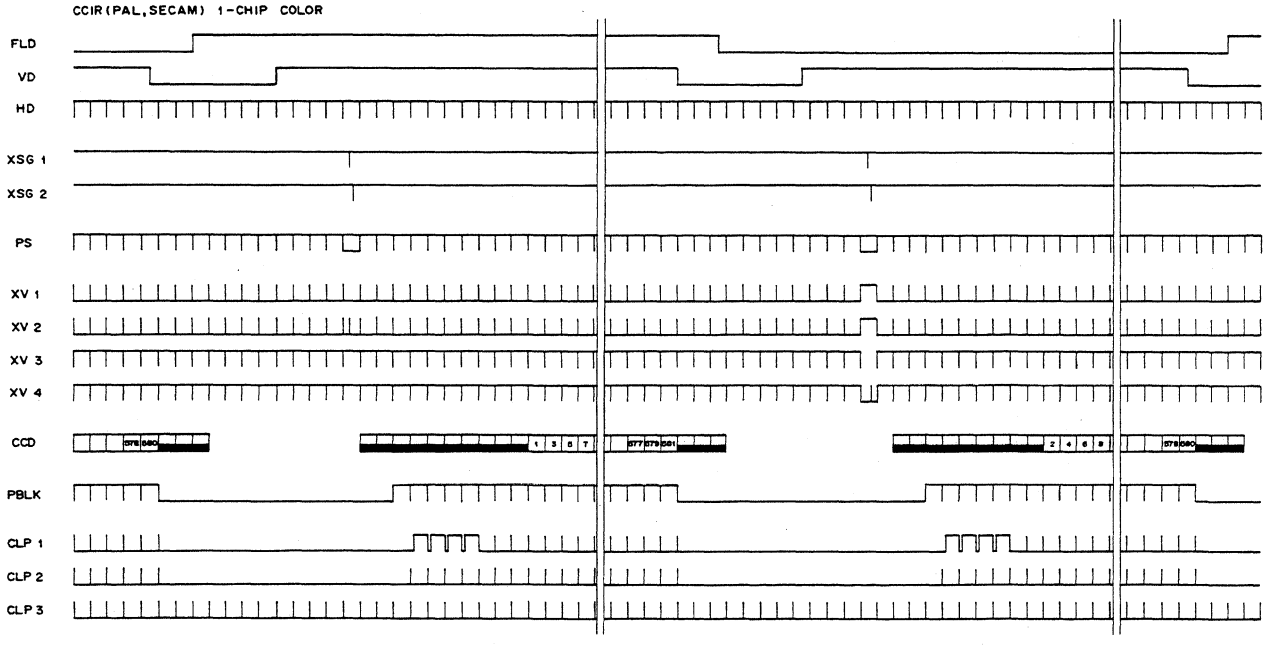


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CCIR(PAL,SECAM) B/W,3-CHIP COLOR



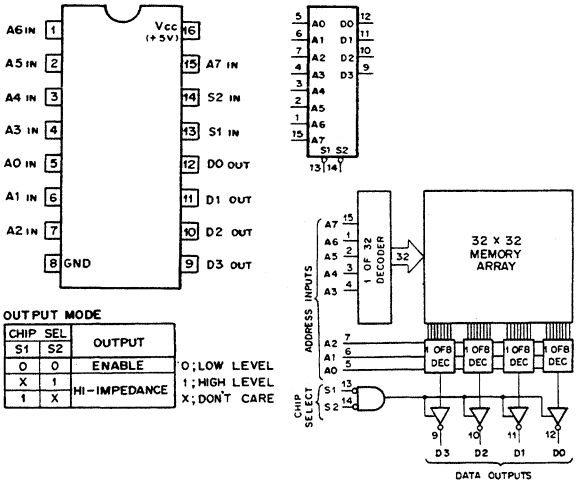
CCIR(PAL,SECAM) 1-CHIP COLOR



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SN74S287N

MB7052PF (FUJITSU) FLAT PACKAGE
1024-BIT (256x4) PROM (3-STATE OUTPUT)
— TOP VIEW —



OUTPUT MODE

CHIP SEL		OUTPUT
S1	S2	
0	0	ENABLE
X	1	HI-IMPEDANCE
1	X	

0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE

WORD/ADDRESS TABLE

WORD		ADDRESS INPUTS							
		A7	A6	A5	A4	A3	A2	A1	A0
0	00	0	0	0	0	0	0	0	0
1	01	0	0	0	0	0	0	0	1
2	02	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:	:
9	09	0	0	0	0	1	0	0	1
10	0A	0	0	0	0	1	0	1	0
11	0B	0	0	0	0	1	0	1	1
12	0C	0	0	0	0	1	1	0	0
13	0D	0	0	0	0	1	1	0	1
14	0E	0	0	0	0	1	1	1	0
15	0F	0	0	0	0	1	1	1	1
16	10	0	0	0	1	0	0	0	0
:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:
253	FD	1	1	1	1	1	1	0	1
254	FE	1	1	1	1	1	1	1	0
255	FF	1	1	1	1	1	1	1	1

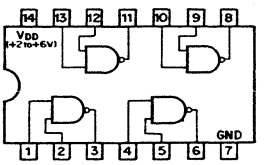
IN HEXADECIMAL
IN DECIMAL

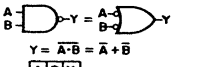
DATA CODE/ACTUAL DATA

DATA CODE		ACTUAL DATA			
		D3	D2	D1	DO
0	0	0	0	0	0
1	1	0	0	0	1
2	2	0	0	1	0
3	3	0	0	1	1
4	4	0	1	0	0
5	5	0	1	0	1
6	6	0	1	1	0
7	7	0	1	1	1
8	8	1	0	0	0
9	9	1	0	0	1
10	A	1	0	1	0
11	B	1	0	1	1
12	C	1	1	0	0
13	D	1	1	0	1
14	E	1	1	1	0
15	F	1	1	1	1

IN HEXADECIMAL
IN DECIMAL

TC74HC00F (TOSHIBA) FLAT PACKAGE
C-MOS 2-INPUT NAND GATE
— TOP VIEW —

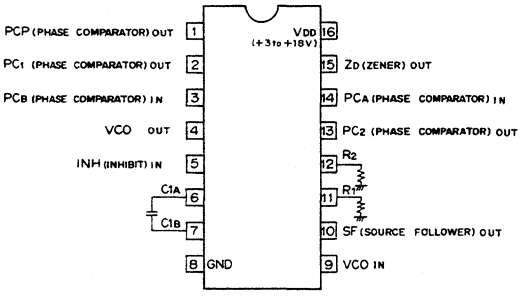


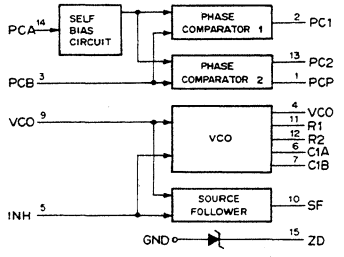


A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

0 ; LOW LEVEL
1 ; HIGH LEVEL

MC14046BCP (MOTOROLA)
C-MOS PHASE LOCKED LOOP
— TOP VIEW —





XC-77 (J, UC)
XC-77CE (EK)

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SECTION C
SPARE PARTS

C-1. PARTS INFORMATION

1. **Safety Related Component Warning**

   Components identified by shading marked with ⚠ on the schematic diagrams, exploded views and electrical spare parts list are critical to safe operation. Replace these components with Sony parts whose parts numbers appear as shown in this manual or in service bulletins and service manual supplements published by Sony.

2. Replacement Parts supplied from Sony Parts Center will sometimes have different shape and outside view from the parts which actually in use. This is due to "**accommodating the improved parts and/or engineering changes**" or "**standardization of genuine parts.**"

   - This manual's exploded views and electrical spare parts lists are indicating the parts numbers of "the standardized genuine parts at present".
   - Regarding engineering parts changes in our engineering department, refer Sony service bulletins and service manual supplements.

3. **Printed Components in Bold-Face type** on the exploded views and electrical spare parts list are normally stocked for replacement purposes. The remaining parts are not normally required for routine service work. Orders for parts not shown in Bold-Face type will be processed, but allow for additional delivery time.

4. Item with no part number and/or no description are not stocked because they are seldom required for routine service.

5. **Abbreviation**

REF. NO.	DESCRIPTION	REF. NO.	DESCRIPTION	REF. NO.	DESCRIPTION
C	CAPACITOR	**FL**	FILTER	**Q**	TRANSISTOR
CN	CONNECTOR	**IC**	IC	**RY**	VARIABLE RESISTOR
CV	VARIABLE CAPACITOR	**L**	INDUCTOR	**X**	OSCILLATOR
D	DIODE	**PU**	COMBINATION PARTS		

All capacitors are in micro farads unless otherwise specified.
All inductors are in micro henries unless otherwise specified.
All resistors are in ohms.

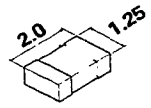
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C-2. ELECTRICAL PARTS

Parts that are not listed in the "reference numbers order list " are shown in following table.
Reference numbers are omitted.

CAPACITOR

CHIP CERAMIC CAPACITOR



220pF through 0.018μF(B) ± 10% 50WV
0.022μF through 0.068μF(F) $^{+80}_{-20}$ % 50WV
0.1μF(F) $^{+80}_{-20}$ % 25WV

Parts No. 1-163-□□□-00

Value	Parts No. – □□□ –
100pF	—
120	—
150	—
180	—
220	001
270	002
330	003
390	004
470	005
560	006
680	007
820	008

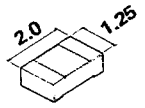
Value	Parts No. – □□□ –
0.001μF	009
0.0012	010
0.0015	011
0.0018	012
0.0022	013
0.0027	014
0.0033	015
0.0039	016
0.0047	017
0.0056	018
0.0068	019
0.0082	020

Value	Parts No. – □□□ –
0.01μF	021
0.012	022
0.015	023
0.018	024
0.022	033
0.027	—
0.033	034
0.039	—
0.047	035
0.056	—
0.068	036
0.082	—
0.1	038

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RESISTOR

CHIP RESISTOR



±5% 1/10W
0Ω through 3.3MΩ

Parts No. 1-216-□□□-00

Value	Parts No. – □□□ –
0Ω	295
1Ω	—
1.1	—
1.2	—
1.3	—
1.5	—
1.6	—
1.8	—
2	—
2.2	298
2.4	301
2.7	302
3	303
3.3	304
3.6	305
3.9	306
4.3	307
4.7	308
5.1	297
5.6	309
6.2	310
6.8	311
7.5	312
8.2	313
9.1	314
10Ω	001
11	002
12	003
13	004
15	005
16	006
18	007
20	008
22	009
24	010
27	011

Value	Parts No. – □□□ –
30	012
33Ω	013
36	014
39	015
43	016
47	017
51	018
56	019
62	020
68	021
75	022
82	023
91	024
100Ω	025
110	026
120	027
130	028
150	029
160	030
180	031
200	032
220	033
240	034
270	035
300	036
330	037
360	038
390	039
430	040
470	041
510	042
560	043
620	044
680	045
750	046
820	047

Value	Parts No. – □□□ –
910	048
1kΩ	049
1.1	050
1.2	051
1.3	052
1.5	053
1.6	054
1.8	055
2	056
2.2	057
2.4	058
2.7	059
3	060
3.3	061
3.6	062
3.9	063
4.3	064
4.7	065
5.1	066
5.6	067
6.2	068
6.8	069
7.5	070
8.2	071
9.1	072
10kΩ	073
11	074
12	075
13	076
15	077
16	078
18	079
20	080
22	081
24	082
27	083

Value	Parts No. – □□□ –
30	084
33kΩ	085
36	086
39	087
43	088
47	089
51	090
56	091
62	092
68	093
75	094
82	095
91	096
100kΩ	097
110	098
120	099
130	100
150	101
160	102
180	103
200	104
220	105
240kΩ	106
270	107
300	108
330	109
360	110
390	111
430	112
470	113
510	114
560	115
620	116
680	117
750	118
820	119

Value	Parts No. – □□□ –
910	120
1MΩ	121
1.1	122
1.2	123
1.3	124
1.5	125
1.6	126
1.8	127
2	128
2.2	129
2.4	130
2.7	131
3	132
3.3	133

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BI-12 BOARD

Ref No.	Part No.	Description
	1-621-913-12	PRINTED CIRCUIT BOARD "BI-12"
C1	1-135-079-21	TANTALUM CHIP 3.3 10% 35V
C2	1-135-084-21	TANTALUM CHIP 1.5 10% 25V
C4	1-163-129-00	CERAMIC CHIP 330PF 5% 50V
C5	1-135-084-21	TANTALUM CHIP 1.5 10% 25V
C6	1-135-091-00	TANTALUM CHIP 1 10% 16V
C7	1-135-092-21	TANTALUM CHIP 3.3 10% 16V
D1	8-719-815-55	1S1555
D2	8-719-815-55	1S1555
Q1	8-729-175-72	2SC2757-T33

CN-167 BOARD

Ref No.	Part No.	Description
	1-621-914-11	PRINTED CIRCUIT BOARD "CN-167"
C1	1-163-141-00	CERAMIC CHIP 0.001 5% 50V
C3	1-163-101-00	CERAMIC CHIP 22PF 5% 50V
C4	1-163-101-00	CERAMIC CHIP 22PF 5% 50V
C5	1-163-101-00	CERAMIC CHIP 22PF 5% 50V
C7	1-163-101-00	CERAMIC CHIP 22PF 5% 50V
D1	8-719-200-08	11DQ03
F1	1-532-775-21	FUSE, MICRO(SECONDARY)
L1	1-410-695-51	CHIP 1.5
L2	1-410-194-61	CHIP 1.5
L3	1-410-194-61	CHIP 1.5

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MB-136 BOARD

Ref No.	Part No.	Description
	A-7615-202-A	MOUNTED CIRCUIT BOARD "MB-136" WITH "SG-119" (J, UC)
	A-7615-212-A	MOUNTED CIRCUIT BOARD "MB-136" WITH "SG-119" (EK)
C1	1-163-141-00	CERAMIC CHIP 0.001 5% 50V
C2	1-135-097-21	TANTALUM CHIP 15 10% 10V
C3	1-163-117-00	CERAMIC CHIP 100PF 5% 50V
C4	1-135-097-21	TANTALUM CHIP 15 10% 10V
C6	1-135-097-21	TANTALUM CHIP 15 10% 10V
C7	1-135-093-21	TANTALUM CHIP 10 10% 16V
C8	1-135-093-21	TANTALUM CHIP 10 10% 16V
C9	1-135-083-00	TANTALUM CHIP 0.47 10% 25V
C10	1-135-083-00	TANTALUM CHIP 0.47 10% 25V
C11	1-135-083-00	TANTALUM CHIP 0.47 10% 25V
C12	1-135-083-00	TANTALUM CHIP 0.47 10% 25V
C13	1-135-092-21	TANTALUM CHIP 3.3 10% 16V
C14	1-135-092-21	TANTALUM CHIP 3.3 10% 16V
C15	1-135-092-21	TANTALUM CHIP 3.3 10% 16V
C16	1-135-092-21	TANTALUM CHIP 3.3 10% 16V
C17	1-163-117-00	CERAMIC CHIP 100PF 5% 50V
C18	1-135-165-95	TANTALUM CHIP 33 10% 16V
C20	1-124-472-11	ELECT 470 20% 10V
C22	1-163-117-00	CERAMIC CHIP 100PF 5% 50V
C26	1-135-093-21	TANTALUM CHIP 10 10% 16V
C27	1-135-095-00	TANTALUM CHIP 1.5 10% 10V
C29	1-163-093-00	CERAMIC CHIP 10PF 5% 50V
C30	1-163-097-00	CERAMIC CHIP 15PF 5% 50V
C32	1-135-097-21	TANTALUM CHIP 15 10% 10V
C33	1-163-105-00	CERAMIC CHIP 33PF 5% 50V
C35	1-163-093-00	CERAMIC CHIP 10PF 5% 50V
C39	1-135-093-21	TANTALUM CHIP 10 10% 16V
C40	1-163-117-00	CERAMIC CHIP 100PF 5% 50V
C41	1-127-518-11	ELECT(SOLID) 100 20% 16V
C44	1-124-472-11	ELECT 470 20% 10V
CNB	1-563-752-11	RECEPTACLE, 10P FEMALE
CND	1-563-752-11	RECEPTACLE, 10P FEMALE
CV1	1-141-299-11	CERAMIC 6PF

Ref No.	Part No.	Description
D1	8-719-100-03	1S2835
D2	8-719-100-03	1S2835
D3	8-719-100-03	1S2835
D4	8-719-100-03	1S2835
D5	8-719-100-03	1S2835
D6	8-719-907-19	FC52M-5
IC1	8-759-941-52	CXD1035BQ-W: SONY
IC3	8-752-031-03	CXA1065M: SONY
IC4	8-729-204-94	TC74HC00F: TOSHIBA
IC5	8-759-013-02	CXB0026AM: SONY
IC6	8-741-148-00	BX1480: SONY
IC7	8-759-204-94	TC74HC00F: TOSHIBA
L1	1-408-147-00	MICRO 2.2
L2	1-408-769-11	CHIP 2.2
L3	1-408-789-21	CHIP 100
L4	1-408-781-00	CHIP 22
L5	1-408-781-00	CHIP 22
L6	1-408-781-00	CHIP 22
L7	1-408-777-00	CHIP 10
L8	1-408-789-21	CHIP 100
PU1	1-464-780-11	DC-DC CONVERTER
Q1	8-729-122-63	2SA1226
Q2	8-729-216-22	2SA1162
Q3	8-729-216-22	2SA1162
Q4	8-729-100-66	2SC1623
Q5	8-729-100-76	2SA812
X1	1-567-708-12	28.6363MHz (J, UC)
	1-567-732-12	28.6363MHz (EK)

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Ref No.	Part No.	Description
PR-89 BOARD		
	A-7513-556-A	MOUNTED CIRCUIT BOARD "PR-89"
C1	**1-135-093-21**	**TANTALUM CHIP 10 10% 16V**
C3	**1-163-086-00**	**CERAMIC CHIP 3PF ±0.25PF 50V**
C4	**1-163-086-00**	**CERAMIC CHIP 3PF ±0.25PF 50V**
C5	**1-135-093-21**	**TANTALUM CHIP 10 10% 16V**
C6	**1-124-471-00**	**ELECT 1000 20% 6.3V**
C8	**1-124-444-00**	**ELECT 220 20% 10V**
C9	**1-135-095-00**	**TANTALUM CHIP 1.5 10% 10V**
C12	**1-135-097-21**	**TANTALUM CHIP 15 10% 10V**
C13	**1-135-097-21**	**TANTALUM CHIP 15 10% 10V**
C16	**1-135-097-21**	**TANTALUM CHIP 15 10% 10V**
C17	**1-135-097-21**	**TANTALUM CHIP 15 10% 10V**
C18	**1-135-096-21**	**TANTALUM CHIP 4.7 10% 10V**
C21	**1-135-095-00**	**TANTALUM CHIP 1.5 10% 10V**
C23	**1-135-096-21**	**TANTALUM CHIP 4.7 10% 10V**
C24	**1-135-165-95**	**TANTALUM CHIP 33 10% 16V**
CNB	1-566-475-11	RECEPTACLE, 3P MALE (2PCS)
CND	1-566-482-11	RECEPTACLE, 10P MALE
FL1	**1-409-427-11**	**LPF 14.3MHz**

Ref No.	Part No.	Description
IC1	**8-752-031-14**	**CXA1118M: SONY**
IC2	**8-752-031-15**	**CXA1119M: SONY**
Q1	**8-729-100-76**	**2SA812**
Q2	**8-729-175-72**	**2SC2757-T33**
Q3	**8-729-175-72**	**2SC2757-T33**
Q4	**8-729-122-63**	**2SA1226**
Q5	**8-729-175-72**	**2SC2757-T33**
Q6	**8-729-122-63**	**2SA1226**
Q7	**8-729-175-72**	**2SC2757-T33**
Q8	**8-729-122-63**	**2SA1226**
Q9	**8-729-100-66**	**2SC1623**
Q10	**8-729-100-66**	**2SC1623**
Q11	**8-729-100-66**	**2SC1623**
Q12	**8-729-100-66**	**2SC1623**
RV1	**1-230-871-11**	**METAL 22K**
RV2	**1-230-871-11**	**METAL 22K**
RV3	**1-230-869-11**	**METAL 4700**
RV4	**1-230-869-11**	**METAL 4700**
RV5	**1-230-869-11**	**METAL 4700**
RV6	**1-230-870-11**	**METAL 10K**
RV7	**1-230-869-11**	**METAL 4700**
RV8	**1-230-870-11**	**METAL 10K**
RV10	**1-230-874-11**	**METAL 100K**
RV11	**1-230-870-11**	**METAL 10K**

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RG-18 BOARD

Ref No.	Part No.	Description
	A-7513-558-A	MOUNTED CIRCUIT BOARD "RG-18"
C1	**1-135-092-21**	**TANTALUM CHIP 3.3 10% 16V**
C2	**1-135-091-00**	**TANTALUM CHIP 1 10% 16V**
C3	**1-135-079-21**	**TANTALUM CHIP 3.3 10% 35V**
C4	**1-135-079-21**	**TANTALUM CHIP 3.3 10% 35V**
C5	**1-135-079-21**	**TANTALUM CHIP 3.3 10% 35V**
C6	**1-135-079-21**	**TANTALUM CHIP 3.3 10% 35V**
C7	**1-135-079-21**	**TANTALUM CHIP 3.3 10% 35V**
C8	**1-135-092-21**	**TANTALUM CHIP 3.3 10% 16V**
C9	**1-135-092-21**	**TANTALUM CHIP 3.3 10% 16V**
C10	**1-135-165-95**	**TANTALUM CHIP 33 10% 16V**
CNA	1-563-750-11	RECEPTACLE, 3P FEMALE (2PCS)
CNB	1-566-482-11	RECEPTACLE, 10P MALE
CNC	1-563-752-11	RECEPTACLE, 10P FEMALE
CND	1-566-482-11	RECEPTACLE, 10P MALE
D1	**8-719-101-23**	**1SS123**
D2	**8-719-101-23**	**1SS123**
D3	**8-719-938-75**	**SB05-05CP**
D4	**8-719-938-75**	**SB05-05CP**
Q1	**8-729-100-66**	**2SC1623**
Q2	**8-729-100-66**	**2SC1623**
Q3	**8-729-100-66**	**2SC1623**
Q4	**8-729-100-66**	**2SC1623**

SG-119 BOARD

Ref No.	Part No.	Description
	A-7513-555-A	MOUNTED CIRCUIT BOARD "SG-119" (J, UC)
	A-7513-593-A	MOUNTED CIRCUIT BOARD "SG-119" (EK)
C1	**1-135-097-21**	**TANTALUM CHIP 15 10% 10V**
C3	**1-135-095-00**	**TANTALUM CHIP 1.5 10% 10V**
C4	**1-135-095-00**	**TANTALUM CHIP 1.5 10% 10V**
C7	**1-135-095-00**	**TANTALUM CHIP 1.5 10% 10V**
C8	**1-135-095-00**	**TANTALUM CHIP 1.5 10% 10V**
C9	**1-163-101-00**	**CERAMIC CHIP 22PF 5% 50V**
C10	**1-163-101-00**	**CERAMIC CHIP 22PF 5% 50V**
IC1	**8-759-941-40**	**CXD1084Q-W: SONY**
IC2	**8-759-009-02**	**MC14046BF: MOTOROLA**

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SH-27 BOARD

Ref No.	Part No.	Description
	A-7513-557-A	MOUNTED CIRCUIT BOARD ''SH-27''
C1	**1-135-165-95**	**TANTALUM CHIP 33 10% 16V**
C2	**1-163-105-00**	**CERAMIC CHIP 33PF 5% 50V**
C3	**1-163-105-00**	**CERAMIC CHIP 33PF 5% 50V**
C4	**1-163-101-00**	**CERAMIC CHIP 22PF 5% 50V**
C5	**1-163-105-00**	**CERAMIC CHIP 33PF 5% 50V**
C6	**1-163-105-00**	**CERAMIC CHIP 33PF 5% 50V**
C7	**1-135-093-21**	**TANTALUM CHIP 10 10% 16V**
C8	**1-135-097-21**	**TANTALUM CHIP 15 10% 10V**
C9	**1-135-165-95**	**TANTALUM CHIP 33 10% 16V**
C10	**1-124-224-00**	**ELECT 47 20% 6.3V**
C14	**1-163-101-00**	**CERAMIC CHIP 22PF 5% 50V**
C15	**1-163-101-00**	**CERAMIC CHIP 22PF 5% 50V**
C16	**1-126-176-11**	**ELECT 220 20% 10V**
C18	**1-163-093-00**	**CERAMIC CHIP 10PF 5% 50V**
CNA	1-566-475-11	RECEPTACLE, 3P MALE (2PCS)
CNB	1-563-750-11	RECEPTACLE, 3P FEMALE (2PCS)
CNC	1-566-482-11	RECEPTACLE, 10P MALE
CND	1-563-752-11	RECEPTACLE, 10P FEMALE
CN1	**1-566-426-11**	**RECEPTACLE, 2P MALE**
	1-563-936-11	PLUG, HOUSING
	1-563-940-11	**PULG, CONTACT**
CV1	**1-141-291-11**	**20PF**
Q1	**8-729-122-63**	**2SA1226**
Q2	**8-769-401-68**	**3SK163-2**
Q3	**8-729-100-66**	**2SC1623**
Q4	**8-729-122-63**	**2SA1226**
Q5	**8-769-401-68**	**3SK163-2**
Q6	**8-729-100-66**	**2SC1623**
Q7	**8-729-122-63**	**2SA1226**
Q8	**8-769-401-68**	**3SK163-2**
Q9	**8-729-100-66**	**2SC1623**
Q10	**8-729-122-63**	**2SA1226**
Q11	**8-769-401-68**	**3SK163-2**
Q12	**8-729-100-66**	**2SC1623**
Q13	**8-729-122-63**	**2SA1226**
Q14	**8-769-401-68**	**3SK163-2**
Q15	**8-729-100-66**	**2SC1623**
Q16	**8-729-175-72**	**2SC2757-T33**
Q17	**8-729-100-66**	**2SC1623**
Q18	**8-729-175-72**	**2SC2757-T33**
Q19	**8-729-100-66**	**2SC1623**
Q20	**8-729-100-66**	**2SC1623**

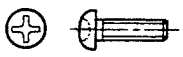
FRAME

Ref No.	Part No.	Description
	A-7575-093-A	**CCD UNIT (J, UC)**
	A-7575-096-A	**CCD UNIT (EK)**
CN1	1-563-786-11	RECEPTACLE, 12P MALE
CN2	1-562-382-00	RECEPTACLE, BNC
CN3	1-563-929-11	RECEPTACLE, 4P FEMALE

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C-3. EXPLODED VIEW
SCREW

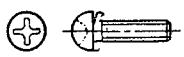
+B
Bzn-N



7-621-□□□-□□

SIZE	Parts No.
2 x 3	772-00
x 4	772-10
x 5	772-20
x 6	772-30
x 8	772-40
x 10	772-50
x 12	772-60
x 14	772-70
x 16	772-80
x 20	–
2.6 x 3	775-00
x 4	775-10
x 5	775-20
x 6	773-95
x 8	775-40
x 10	775-50
x 12	775-60
x 14	775-70
x 16	775-80
x 20	775-90

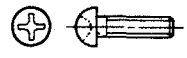
PRECISION +P
Bzn-N



7-627-□□□-□□

SIZE	Parts No.
1.7 x 1.6	552-18
x 1.8	–
x 2	552-28
x 2.2	–
x 2.5	552-08
x 2.8	–
x 3	552-38
x 3.5	552-78
x 4	552-48
x 4.5	–
x 5	552-58
x 5.5	–
x 6	–
2 x 1.8	554-38
x 2	553-18
x 2.2	–
x 2.5	553-28
x 2.8	554-58
x 3	553-38
x 3.5	554-18
x 4	553-48
x 4.5	553-58
x 5	554-28
x 5.5	–
x 6	553-68
x 7	553-88
x 8	553-98
x 10	553-78
2.6 x 2.8	556-08
x 3	–
x 3.5	556-28
x 4	556-38
x 4.5	556-48
x 5	556-58
x 5.5	–
x 6	556-78
x 7	–
x 8	–
x 9	–
x 10	–

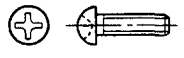
PRECISION +P
Cr-N



7-627-□□□-□□

SIZE	Parts No.
1.7 x 1.6	–
x 1.8	–
x 2	552-27
x 2.2	552-87
x 2.5	552-07
x 2.8	–
x 3	552-37
x 3.5	–
x 4	552-47
x 4.5	552-67
x 5	552-57
x 5.5	557-07
x 6	552-77
2 x 1.8	554-37
x 2	553-17
x 2.2	554-07
x 2.5	553-27
x 2.8	–
x 3	553-37
x 3.5	554-17
x 4	553-47
x 4.5	553-57
x 5	553-67
x 5.5	–
x 6	554-27
x 7	553-87
x 8	553-97
x 10	553-77
2.6 x 2.8	556-07
x 3	–
x 3.5	–
x 4	556-37
x 4.5	–
x 5	–
x 5.5	–
x 6	556-77
x 7	–
x 8	556-97
x 9	–
x 10	557-47

+P
Bzn-N

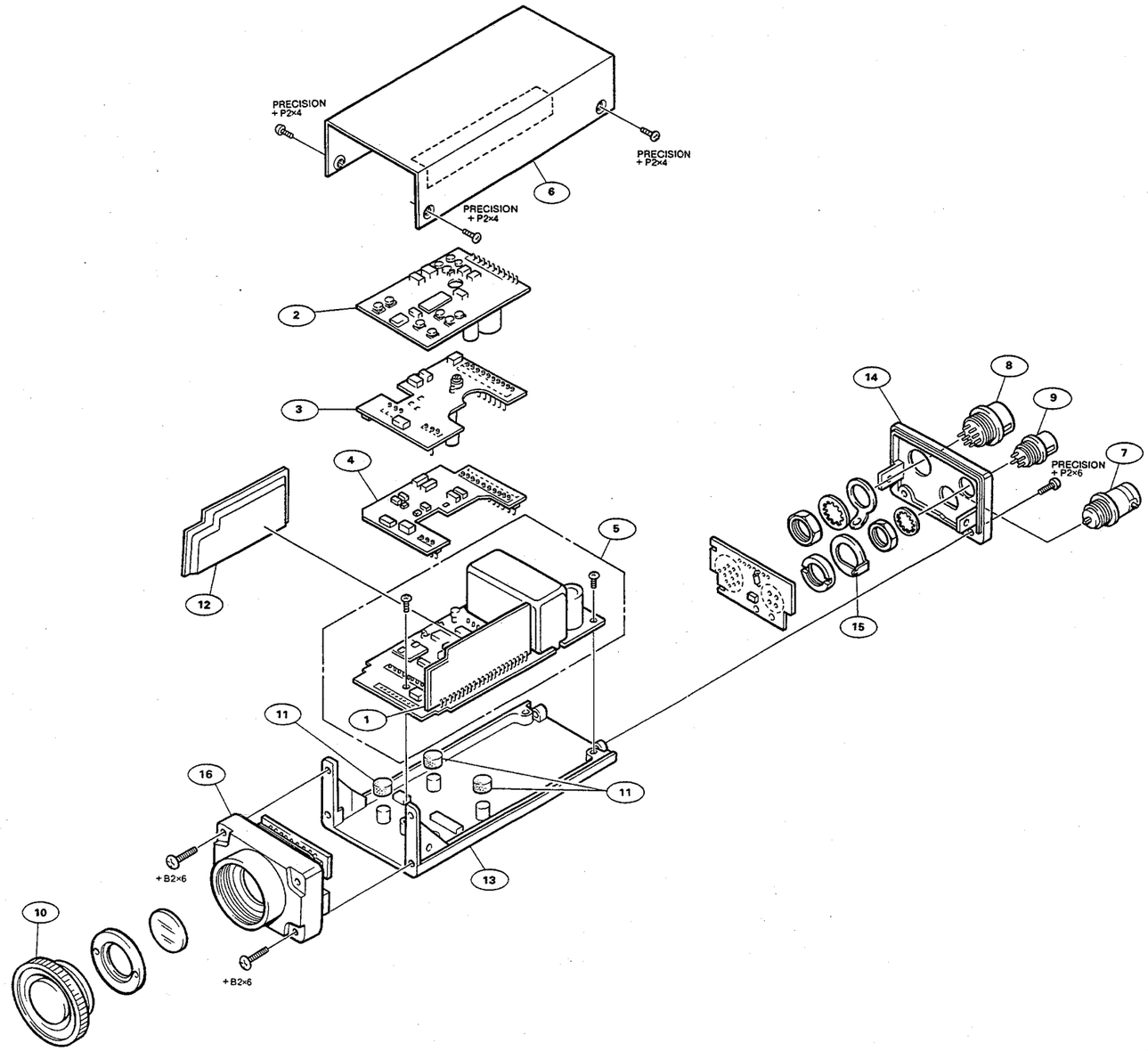


7-621-□□□-□□

SIZE	Parts No.
2 x 3	255-10
x 4	255-20
x 5	283-00
x 6	255-40
x 8	255-50
x 10	283-10
x 12	283-70
x 14	–
x 16	–
x 20	256-20
2.3 x 5	–
x 6	–
x 8	–
x 10	–
x 12	–
x 14	–
x 16	–
x 20	–
2.6 x 3	259-10
x 4	284-00
x 5	284-10
x 6	284-20
x 8	284-30
x 10	284-40
x 12	259-70
x 14	259-80
x 16	260-00
x 20	260-20

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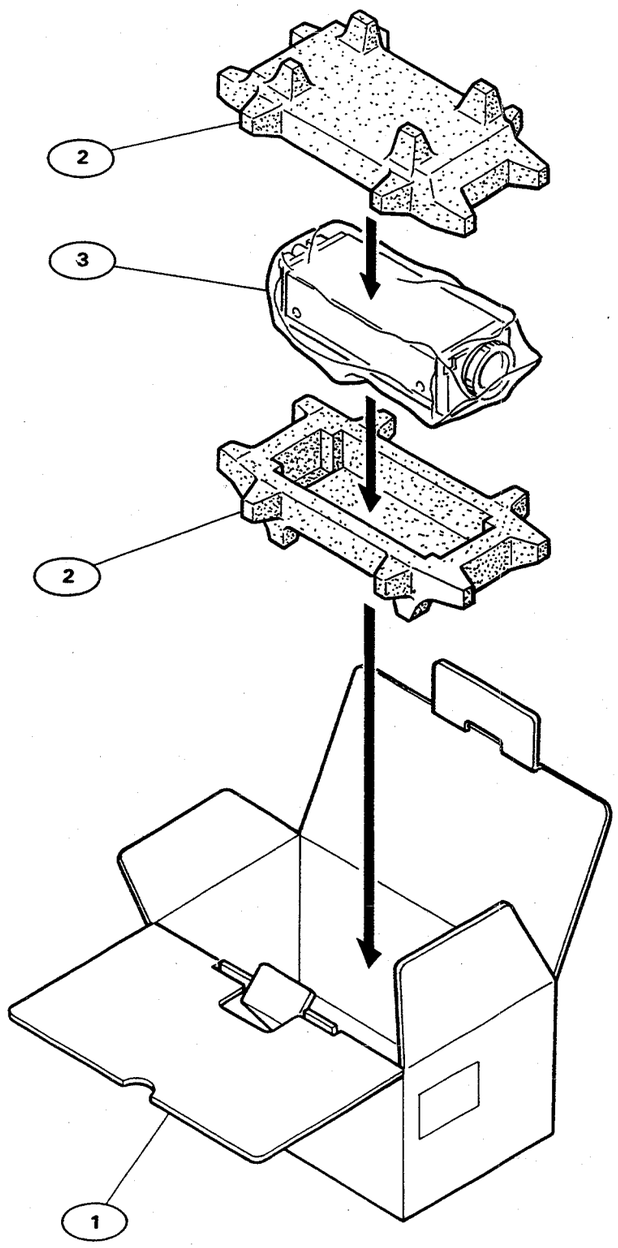
CAMERA MODULE



No.	Parts No.	Description
1	A-7513-555-A	MOUNTED CIRCUIT BOARD ''SG-119''
2	A-7513-556-A	MOUNTED CIRCUIT BOARD ''PR-89''
3	A-7513-557-A	MOUNTED CIRCUIT BOARD ''SH-27''
4	A-7513-558-A	MOUNTED CIRCUIT BOARD ''RG-18''
5	A-7615-202-A	MB-136 ASSY
6	X-3683-218-1	COVER ASSY
7	**1-562-382-12**	**RECEPTACLE, BNC ''VIDEO OUT''**
8	**1-563-786-11**	**RECEPTACLE, MALE, 12P ''DC IN/SYNC''**
9	**1-563-929-11**	**RECEPTACLE, FEMALE, 4P ''LENS''**
10	**2-042-385-04**	**CAP, C MOUNT**
11	3-683-277-01	BUSHING, INSULATING
12	3-683-278-01	PLATE, SHIELD, SG
13	3-683-285-01	CHASSIS
14	3-683-287-01	PANEL, REAR
15	3-718-804-01	LUG, GROUND
16	**A-7575-093-A**	**CCD BLOCK (UCJ)**
	A-7575-096-A	**CCD BLOCK (EK.)**

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C-4. PACKING MATERIAL AND ACCESSORY (SUPPLIED)



No.	Part No.	Description
1	3-683-295-01	CARTON, INDIVIDUAL
2	3-683-296-01	CUSHION
3	**3-701-618-00**	**BAG, POLY (FOR XC-77/77CE)**

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