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User Manual

TPRO-PCI

Synchronizable Timecode Generator
with PCI Bus Interface





TSAT-PCI

GPS-based Synchronizable
Timecode Generator
with PCI Bus Interface

Revision 2.2

KSI

a division of DSP*Con*, Inc.

For technical support, contact KSI toll-free at 866-KSI-KSI3

TPRO-PCI and TSAT-PCI USER MANUAL
Revision 2.2 —August 2001

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August 2001	2.1	PCI Interface Options	Updated subsystem product ID section Added -DCLOBNC
August 2001	2.2	Options	Included detailed descriptions of options

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Chapter One

Overview

Introduction

The TPRO-PCI is a precision clock that automatically synchronizes to standardized time code signals or (for TSAT-PCI configuration) to the GPS satellite system and can be read from the host computer.

Inputs to the TPRO-PCI are modulated time code (or GPS receiver signals for TSAT-PCI), host commands, and time tags.

Outputs are modulated IRIG-B time code, programmable start/stop time, and a programmable "heartbeat" pulse rate.

The board also can generate interrupts on the PCI bus (if enabled). Interrupt sources include the heartbeat, time tag, FIFO data available, and/or at the programmable start time.

The clock will automatically synchronize to specified time code signals. A status bit advises the host of synchronization status. In the absence of Timecode input or GPS the board will start counting at 000 days, 00 hours, 00 minutes, 00 seconds at power-on. The clock time can also be set by user command.

1.1 - Distinguishing Between TPRO-PCI and TSAT-PCI Boards

Visually

Hold the board with the component side up, with the gold edge fingers pointing towards you, and the metal bracket on the left-hand side. In the upper left-hand corner, just above P1, locate the white circle (about 1.9 cm (0.75 inch) diameter). In the center of this circle are two holes (one has a round pad, the other has a square pad). If a component (C1) is installed in these holes, the board is a TSAT-PCI, otherwise it is a TPRO-PCI. (There are several other differences, but this is the most obvious one.)

Software

Examine the Subsystem Product ID number, shown in the Specifications section.

1.2 - Package Contents

The TSAT-PCI is delivered with a 100-foot cable with connectors pre-installed, GPS receiver/antenna (housed together in a single enclosure), and a user's manual. The TPRO-PCI is delivered with mating connector (15 pin), and a user's manual.

1.3 - Numbering Convention

In this manual, the prefix "0x" indicates that the number is in hexadecimal (base 16) format. Sometimes this prefix is omitted if such format is obvious.

Chapter Two

Specifications

2.1 - TPRO-PCI Specifications
(board only)

Timecode Input

Code Format (autodetect)	IRIG-A (A132), IRIG-B (B122), NASA36
Amplitude	1.2 Vp-p min, 8.0 Vp-p max
Polarity	Detected automatically
Modulation Ratio	2:1 min, 3:1 typ, 4:1 max
Input Impedance	> 10 K ohms
Timing Accuracy	Better than 100 ppm (not suitable for tape playback)
Common Mode Voltage	Differential input, ± 100 V max

IRIG-B Output

Code Format	IRIG-B (B122)
Amplitude (mark)	2.6 Vp-p (type)
Modulation Ratio	3:1
Output Impedance	600 ohms

Time-Tag Input

Input Voltage	-0.5V min, +0.8V max for logic 0 +2.0V min, +5.5 max for logic 1 Tags rising edge
Input Current	< 5 µA for logic 0 <5 µA for logic 1
Rise/Fall Time	500 nS max
Repetition Rate	1000 events per second max
Timing Resolution	1 µS

1PPS Sync Input (option –M only)

Input Voltage	2.4 V min, 16.0 V max (high) (500 uA max at 5 vin, 12 mA max at 16 Vin)
Rise/Fall Time	500 nS max
Trigger Edge	Rising
1PPS Accuracy	Must be 100 ppm or better

Match Output

Output Voltage	3.8 V min at 6 mA (high) 0.4 V max at –6 mA (low)
Setability	1 µS

On-Board Clock

Resolution	1 µS
Range	366:23:59:59.999999
Date Format	Integer (001-366)
Synchronization Time	< 8 seconds
Stability	Disciplined to timecode: $1x10^{-6}$ Undisciplined: $2x10^{-7}$

PCI Interface

Interface	PCI Spec. 2.1 compliant	
I/O	64 bytes	
DMA Transfers	None	
General	Occupies 32 consecutive 16-bit I/O and memory addresses (64 bytes)	
Chipset Vendor ID	0x10b5 (PLX Technology, Inc.)	
Chipset Product ID	0x9050 (PLX 9050 Chip	
Subsystem Vendor ID	0x1347 (KSI)	
Subsystem Product ID	TPRO-PCI	0x9050 (standard)
	TPRO-PCI-M	0x9051
	TPRO-PCI-HB1PPS	0x9052
	TPRO-PCI-FXB	0x9052
	TPRO-PCI-LOR1	0x9052
	TPRO-PCI-M-HB1PPS	0x9053
	TSAT-PCI	0x9070 (standard)
	TSAT-PCI-HB1PPS	0x9072
	TSAT-PCI-FXA	0x9072

General

Size	H 106.7 mm, L 174.6 mm (H 4.2”, L 6.875”)
Power (from PCI bus)	+5 Vdc @ 425 mA max, +12 Vdc @ 225 mA max, -12 Vdc @ 50 mA max
Operating Temperature	-30 to +70 C (-22 to +158 F)
Storage Temperature	-40 to +80 C (-40 to +176 F)
Connectors	BNCs for timecode input and output; DB15 (socket) for timecode input, output, heartbeat output, match output, time-tag input, and 1 PPS input.

Heartbeat Output

Output Voltage	3.8 V min at 6 mA (high) 0.4 V max at –6 mA (low)
Wave Shape	Pulse or Squarewave (programmable)
Pulse Width	150 nS min, 450 nS max
Pulse Polarity	Negative
Squarewave	45% - 55%
Timing	Falling edge on-time (pulse or squarewave)
Range	1.000 µS – 21.845 mS in 1 µS steps (1 MHz – 45.7771 Hz)
Power-on default rate	100 PPS (pulse)

2.2 - TSAT-PCI Specifications

(GPS receiver only)

GPS Receiver/Antenna

Number of Satellites	6
Acquisition Time (cold start)	5 minutes type, 15 min max
Re-acquisition Time	< 1 minute
Frequency	1575 MHz (receive only) (L1 band, C/A code {SPS})
Sync to UTC	Within ± 1.0 µS max (antenna in stationary position)
Position	25 m SEP (w/o SA) (82 feet)
Altitude	0 m to +18,000 m (0 to +59,055 feet)
Size	147 mm Dia, 100 mm H (5.8” Dia, 3.9” H)
Pole Mount	1.00” I.D., 14 tuns/inch straight (not tapered)
Operating Temp	-30 to +70 C (-22 to +158 F)
Storage Temp	-55 to +100 C (-67 to +212 F)
Waterproof	Submersion to 1 m
Salt Fog	MIL-STD-202F, Method 101D Condition B

2.3 - Options

-M Synchronizes to 1PPS input instead of timecode **(TPRO-PCI Only)**

-HB1PPS Provides a 1 Pulse Per Second (1PPS) on the HeartBeat output at power up. The HeartBeat (P1-Pin-6) can either be programmed to a pulse or square wave and the falling edge is on time. The specified rate must be an exact multiple of 1.000mS. The range of programmable rates is:

Minimum Rate (lowest frequency):	65,534 Seconds (0.0152593 Hz)
Maximum Rate (highest frequency):	2 mS (500 Hz)
Pulse Width (time low, pulse mode only):	1 mS (typical)
Programming Resolution:	1 mS

This option cannot be combined with options –FXA, –FXB, –HDRV

-FXA Provides an RS-422 driver for the Heartbeat Output, and provides the same range of pulse rates as the -HB1PPS Option. The 15-pin D-type connector provides the Heartbeat Output on pin 6 (normally low, pulses high) and pin 8 (normally high, pulses low). The rising edge of pin 6 (falling edge of pin 8) is *on-time*. The pulse width is approximately 1 mS. The power-on default pulse rate is once per second (1PPS). The Match function can still be used to provide an interrupt, if desired. However, the Match Output pin has been eliminated. There are *no jumpers* installed on header JP9. **(TSAT-PCI only)**
This option cannot be combined with options –HB1PPS or –HDRV.

-FXB Provides an RS-422 driver for the Heartbeat Output, and provides the same range of pulse rates as the -HB1PPS Option. The 15-pin D-type connector provides the Heartbeat Output on pin 6 (normally low, pulses high) and pin 8 (normally high, pulses low). The rising edge of pin 6 (falling edge of pin 8) is *on-time*. The pulse width is approximately 1 mS. The power-on default pulse rate is once per second (1PPS). The Match function can still be used to provide an interrupt, if desired. However, the Match Output pin has been eliminated. There are *no jumpers* installed on header JP9. **(TPRO-PCI only)**
This option cannot be combined with options –HB1PPS or –HDRV.

-HDRV Provides an RS-422 driver for the Heartbeat Output. The 15-pin D-type connector provides the Heartbeat Output on pin 6 (normally low, pulses high) and pin 8 (normally high, pulses low). The rising edge of pin 6 (falling edge of pin 8) is *on-time*. The power-on default pulse rate is one hundred times per second (100PPS). The Match function can still be used to provide an interrupt, if desired. However, the Match Output pin has been eliminated. There are *no jumpers* installed on header JP9.
This option cannot be combined with options –FXA, –FXB, –HB1PPS.

-LOR1 The purpose of this option is to provide the board with three different outputs on a three-pin header. 1 Mega-Hertz Output (1MHZ), 1 Pulse Per Second Output (1PPS), and a Ground Output. The 3-pin header is located on JP11 pins 6, 7, & 8.

The 3-pin header is designated as follows:
1. JP11 pin 6 is 1MHZ
2. JP11 pin 7 is 1PPS
3. JP11 pin 8 is Ground

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-DCLOBNC Provides a DC Shift level output on J2 BNC connector and P1 D-type connector pin 9. The BNC or the 15-pin D-type connector provides a DC Shift level output with the rising edge on time. The modulated IRIG-B output is eliminated with this option.

-RECONN The purpose of this option is to provide reinforced connectors for the board. Both the BNC and the DB-15 connectors are glued to the board to ensure stability under stressed conditions.

Device drivers for major operating systems (contact KSI at 866-KSI-KSI3 for more information)

2.4 - Accessories

CAB-BO1

The CAB-BO1 is a cable, which provides multiple connections for a variety of inputs and outputs via the DB-15 connector on the board. BNC connectors are extended from the DB-15 connector in the following manner.

Inputs:	Pin #
Time Tag (external event)	4

Outputs	Pin#
HeartBeat	6
Match Time	8
3Mhz	14

CAB-BO2

This cable is for TPRO-PCI with option –M only.
The CAB-BO2 is a cable which provides multiple connections for a variety of inputs and outputs via the DB-15 connector on the board. BNC connectors are extended from the DB-15 connector in the following manner.

Inputs:	Pin #
Time Tag (external event)	4
1PPS (Pulse Per Second)	15

Outputs	Pin#
HeartBeat	6
Match Time	8
3Mhz	14

TRIM-CAB-D-D-100

This cable is used as an extension cord for boards using the Trimble GPS Receiver. It consists of a 100’ cable with DB-15 connectors (one male, one female) on the ends. It connects to a board on one end and to the standard TRIM-CAB-STD cable on the other end. It does not connect directly to the Trimble GPS Receiver.

TRIM-CAB-STD

This is the standard 100’ cable for the Trimble GPS Receiver.

2.5 - P1 Connector Pinout

for TSAT-PCI (only)

The GPS receiver/antenna cable plugs into the 15-pin P1 connector. Additionally, some pins may interface to the user's equipment. It is the user's responsibility to modify the antenna cable connector, if necessary, to access the

"User Connection" pins. A description of the pinout of the supplied cable is shown below.

P1 Pin	Antenna Pin	**Antenna Connection**	**Color**	**User Connection**
1				Do not connect
2				Do not connect
3	1	+12 Volts	Red	
4				Time Tag Input
5	9	Ground	Black	Ground
6				Heartbeat Output
7		Ground	Shield	
8				Match Output
9	11	1PPS+	Orange/White	
10	5	RXD+	Yellow	
11	4	RXD-	Brown	
12	3	TXD+	Orange	
13	2	TXD-	Violet	
14	12	1PPS-	Black/White	
15	8	Battery	Green	

The antenna cable wires are twisted pairs, as follows:

Red with Black (pins 3 & 5)
Yellow with Brown (pins 10 & 11)
Org/Wht with Blk/Wht (pins 9 and 14)
Orange with Violet (pins 12 & 13)
Green with Blue (pins 15 & none)

The following antenna cable wires are connected at the antenna end, but not at P1:

Antenna	**Pin Color**
6	White
7	Gray
10	Blue

The pigtail on the 15-pin end of the cable is used for custom options (if any).

2.6 - P1 Connector Pinout

for TPRO-PCI (only)

P1 Pin	User Connection
1	Timecode Input + (same as J1 BNC center)
2	Timecode Input- (same as J1 BNC shield)
3	Do Not Connect
4	Time Tag Input
5	Ground
6	Heartbeat Output
7	Ground
8	Match Output
9	IRIG-B Output (same as J2 BNC center)
10-13	Do Not Connect
14	Factory Test Point (3.0 MHz)
15	1PPS Sync Input (-M option only)

The Timecode Input can be applied either to pins 1 and 2 of P1 or to the J1 BNC connector (this is the connector closest to P1). The Timecode Input is a differential signal (i.e. - Timecode Input- is isolated from ground).

It is acceptable to connect Timecode Input- to ground.

The IRIG-B output can be taken either from pin 9 of P1 or from the J2 BNC connector (this is the connector farthest from P1). The IRIG-B output is a single-ended signal (i.e. - it is referenced to ground).

2.7 - Timecode Input BNC Connector (J1)

The timecode input BNC connector is located nearest the 15-pin D-type connector.

2.8 - IRIG-B Output BNC Connector (J2)

The IRIG-B output BNC connector is located farthest from the 15-pin D-type connector.

Chapter Three

Configuration

3.1 - Base Address

The base address is configured by the host computer's PCI BIOS software.

3.2 - Interrupt Request Level

The interrupt request (IRQ) level is configured by the host computer's PCI BIOS software.

3.3 - Time Tag Enable/Disable

The Time Tag Enable/Disable is configured by JP10. Since each Time Tag causes data to be put into the FIFO, unexpected Time Tags result in unexpected data in the FIFO. Some users may want to keep the Time Tag signal connected, but prevent it from putting data into the FIFO. To disable Time Tags, connect the jumper between JP10 pins 2 and 3. For normal operation (time tags enabled), connect JP10 pins 1 and 2 (this is the default configuration as shipped from the factory).

It is often helpful to disable time tags while developing application software.



If the Time Tag input is pulsed faster than 1000 events/second, and JP10 is has pins 1 and 2 connected, erratic operation may occur.

JP10 is the only user-configurable setting. All other jumpers are for factory use only.

Chapter Four

Installation

4.1 - GPS Receiver/Antenna
(TSAT-PCI Only)

The mounting location should be free of objects, which might obstruct satellite visibility from straight overhead to within 20 degrees of the horizon in all directions. Obstructions that block a significant portion of the sky will result in degraded performance. Specifically, the GPS receiver may track fewer than 4 satellites, which would prevent it from obtaining time synchronization. The GPS receiver attempts to track satellites spread out as far as possible across the sky to optimize the timing accuracy. The GPS receiver/antenna must be mounted with the connector side pointing down and must be spaced at least 1m (39 inches) away from other GPS antennas.

Mount the antenna at the desired location. Connect the round end of the supplied cable to the antenna.

The GPS receiver/antenna's manufacturer does not recommend any means of lightning protection.

KSI recommends that weatherproofing compound be applied to the antenna connection.

Weatherproofing kit P/N 221213 is available from Andrews Corporation (800-255-1479). This kit includes butyl rubber, plastic tape, and instructions.

4.2 - Install Board into Computer

Shutdown the computer, then turn it's power switch off and unplug the line cord.

Open the computer. The board can be installed into any unused PCI slot.



The board and/or the computer can be damaged by static electricity. Before installing the board, discharge static buildup by touching the metal frame of the computer with one hand and the protective bag containing the board with the other, then open the protective bag.

Verify that jumper setting JP10 is set as described on the previous page.

Remove the metal plate on the rear panel at the desired location, then plug the board in. Attach the top of the mounting bracket with the screw from the metal plate.

Close the computer, plug in the line cord, start the computer. Depending on which operating system you are using, you may get a message identifying new hardware. This message may indicate that the hardware is of "unknown type." This is normal. Exit the "Found New Hardware" dialog box. *Do not* click on "Have Disk".

The TPRO–PCI (and TSAT–PCI) operates automatically as soon as the host computer system does the power-on reset. To change the operating parameters or read data consult the Programming section.

An on-board LED (LED1) flashes a status pattern to assist in diagnosing installation errors. The pattern is a sequence of short and long flashes. Trailing short flashes are deleted so the status pattern can repeat more frequently.

Flash Position	Meaning of Short (cleared) Flash	Meaning of Long (set) Flash
1	GPS satellite receiver being used for time reference	Modulated time code input being used for time reference
2	Synchronization to better than 5µs verified with last 5 seconds	Synchronization to better than 5µs not verified within last 5 seconds
3	1PPS Pulse from GPS satellite receiver is OK	1 PPS pulse from GPS satellite receiver is bad. In applications with modulated time code inputs only, this status bit will always be set.
4	GPS satellite receiver serial data being received OK	No serial data being received from GPS satellite receiver. In applications with modulated time code inputs only, this status bit will always be set.
5	GPS satellite receiver is tracking enough satellites for accurate UTC time.	GPS satellite receiver is not tracking enough satellites for accurate UTC time. In applications with modulated time code inputs only, this status bit will always be set.
6	Time code input being decoded	Time code input not decodable. In applications without modulated time code inputs, this status bit will always be set.
7	If using 1PPS, set NEXT 1PPS TIME command sequence has been performed. Used for -M option only	Waiting for “SET NEXT 1PPS TIME” command. Used for -M option only

Chapter Five

Board Operation

5.1 - TSAT-PCI

The TSAT-PCI obtains time from the GPS satellites, synchronizes its on-board clock to this time, and provides an IRIG-B output from its on-board clock.

GPS consists of a set ("constellation") of approximately 30 satellites. They are in relatively high, circular orbits, inclined about 55 degrees relative to the equator, and circle the Earth about once every 12 hours. Thus, several satellites are above the horizon at all times anywhere on Earth. The receiver needs to track at least four satellites simultaneously to determine time and position. Best accuracy is achieved when the satellites being tracked are scattered widely across the sky; the receiver automatically attempts to choose satellites based on maximum apparent separation. Thus, it is important that the antenna have a clear view of as much sky as possible (and be mounted with the connector pointed down, for the same reason). The satellites do not remain at a fixed location in the sky.

Occasionally the receiver stops tracking a satellite and begins searching for another one, causing fluctuations in the number of satellites tracked (between five and eight).

The most common complaint new GPS users have is that the time needed to begin tracking satellites varies each time the unit is turned-on, or that it seems to take a long time to begin tracking. Refer to the Specifications section for typical and maximum times, and note that significant variations around the “typical” time are normal. If it hasn't established synchronization after the maximum time specified, the most likely reason is that the antenna does not have an unobstructed view of the sky. Try re-locating the antenna. Note that the GPS receiver is built into the antenna housing; additional filtering cannot be installed.

When power is applied, the GPS receiver automatically begins searching for GPS satellite signals. After the receiver has been operating for a few minutes and has calculated the position (longitude, latitude, and altitude), the position is saved in memory. Having this saved position results in faster re-acquisition the next time power is applied. A large capacitor on the board provides voltage to the receiver's memory. If the cable between the board and the receiver is disconnected, or if the computer isn't turned on for about 10 days, the receiver's position memory will be lost, which will result in a slightly longer acquisition time the next time that power is applied.

The time obtained is in Coordinated Universal Time (UTC) format. This means the same time (and date) is received in all parts of the world, regardless of local time zone. UTC is 5 hours ahead of Eastern Standard Time (EST) in the United States in winter, and 4 hours ahead of Eastern Daylight Time (EDT) in summer. UTC is not adjusted for Daylight Saving time. For example, 10:00 PM in New York on July 3 rd is 02:00 July 4th UTC. The Gregorian date consists of the year, month, and day (e.g., 1997-09-19 for September 19, 1997). The Gregorian date can be read from the board, however, the Gregorian date is not transmitted in the IRIG-B output. Instead, the IRIG-B output transmits the Julian date (an integer from 001-366 representing the day number in the year). This limitation is due to the standard definition of the IRIG-B code format.

The on-board clock continues to increment time ("freewheel") while not tracking satellites. When power is first applied, time begins freewheeling from 000:00:00:00, then jumps to the correct time when synchronization is established.

5.2 - TPRO-PCI

The TPRO-PCI obtains time from the timecode input, synchronizes its on-board clock to this time, and provides an IRIG-B output from its on-board clock. The timecode input consists of an amplitude-modulated sinewave (carrier frequency is 1 kHz for IRIG-B or NASA36, or 10 kHz for IRIG-A). The code format is automatically detected.

The board does not significantly load the timecode input, and (since it is a very low frequency), cable impedance mismatches do not significantly degrade the signal either. Thus, a single timecode source can drive at least 10 inputs, cable termination is not necessary, cable length can be up to several hundred feet, and a variety of cable types can be used. Usually, coaxial cable (RG-58 or RG-59 type) with BNC connectors is used. Multiple boards can be driven by placing a BNC "T" connector at each board, and connecting the timecode input in a daisy-chain configuration.

Another approach is to take the IRIG-B output from one board to the timecode input of the next board (a loop-through configuration). The loop-through configuration has the advantage that if the signal is lost at some point, all boards downstream of the break will continue to have the same time (driven by the first board's freewheeling clock). Also, this eliminates the need for having BNC "T" connectors.

The board automatically synchronizes to the incoming timecode. An on-board 6 MHz crystal oscillator is phase-locked to the timecode carrier frequency. This results in timing resolution down to 1µS, despite the fact that the input carrier is only 1 kHz (or 10 kHz for IRIG-A). Also, this precludes using timecode from sources with unstable timebases (e.g., playback from tape or digital storage).

By definition, the timecode format standard (IRIG-B, NASA36, or IRIG-A) specifies the format for transmitting the date to be an integer (001-366). This is referred to as the Julian date. Note that the date is not in year, month, day (Gregorian) format. The user's software can convert from Julian date to Gregorian date, but be careful. First, the user's software needs to know whether the current year is a leap year. Second, the user's software must account for the fact that, when freewheeling, before synchronizing, the board will report an invalid Julian date (000).

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Chapter Six

Programming

General Information

From a programming standpoint, the board appears to be a PCI-to-ISA bridge device. This means that the PCI bus "sees" the board as a device, which has 32 consecutive 16-bit memory locations (64 bytes) and 32 consecutive 16-bit I/O locations (64 bytes). During startup, the PCI BIOS (part of the host computer) mapped these locations somewhere in the absolute address space.

The 32 memory locations and the 32 I/O locations serve exactly the same functions. In actual use, only one of these (either memory or I/O) is used; the other is ignored. On host computers using Intel CPUs (e.g., Pentium, 486, etc.) use the I/O locations. On host computers using Motorola CPUs (e.g., the 68000 family) use the memory locations (because Motorola does not have "I/O" instructions).

The locations of the board's registers are specified as "Base + Offset". The offsets are constants, as described in the next section. The "Base" is chosen by the PCI BIOS during startup. There is a separate "Base" for the memory and I/O locations.

Time is read as four 16-bit words. It is in binary-coded decimal format. Status is read as a single 16-bit word. Time tags and, for the TSAT-PCI, GPS information (longitude, latitude, altitude, and Gregorian date), are read by first sending a command to the board, then reading ten 16-bit words from a first-in-first-out (FIFO) register.

The user's software must wait a small amount of time after sending each command. This admittedly cumbersome requirement is because the on-board processor places a higher priority on maintaining the time than on processing commands. The actual amount of time needed to process a command depends on when the command was received relative to the on-board time. The section on commands specifies the amount of time needed to assure that the command was received. There is no restriction on reading from the board.

Each 16-bit word is located on an even address. Although many of the registers use only eight bits, always read and write registers as 16-bit entities. Do not attempt an 8-bit access on an odd address location.

6.1 - Register Locations

Location Read Usage Write Usage

Base + 0x00 FIFO Interrupt Control Port
Base + 0x02 Status Register Command Port
Base + 0x04 De-assert Reset
Base + 0x06 Assert Reset
Base + 0x08 Clock: Days
Base + 0x0a Clock: Hours through Minutes
Base + 0x0c Clock: Seconds through 10 mS
Base + 0x0e Clock: 1 mS through 1 uS
Base + 0x10 Clear Flags
Base + 0x12 Simulate Time Tag
Base + 0x14
Base + 0x16
Base + 0x18
Base + 0x1a
Base + 0x1c
Base + 0x1e
Base + 0x20
Base + 0x22
Base + 0x24
Base + 0x26
Base + 0x28
Base + 0x2a
Base + 0x2c
Base + 0x2e
Base + 0x30
Base + 0x32
Base + 0x34
Base + 0x36
Base + 0x38
Base + 0x3a
Base + 0x3c
Base + 0x3e
(Blank boxes are reserved for future use).

6.2 - Using the FIFO

The board uses a first-in-first-out (FIFO) register for providing multi-word responses. Each of these responses consists of ten 16-bit words, of which only the lower 8-bits are actually used. A bit in the Status Register indicates whether data is ready in the FIFO. The user's software must check that status bit before reading *each* word from the FIFO.

There can be a delay of up to 200 uS before all ten words are written into the FIFO. This is because the on-board CPU writes this data, but it also maintains the time (days through milliseconds) in software, and places a higher priority on maintaining time than filling the FIFO. Thus, it is not uncommon for, say, only three of the words to be written, then a substantial delay, then the remaining seven words written into the FIFO. The user's software must allow for such operation (i.e. - it must not give up just because it has not read all ten words before the status indicates FIFO empty. Either wait 200 uS before beginning reading, or allow for enough retries if FIFO empty status is detected prematurely.)

To check the FIFO Ready flag, read the Status Register (at Base + 0x02). If the least significant bit is a zero, there is data in the FIFO. If this bit is a one, the FIFO is empty.

The FIFO holds 512 words (i.e. - 51 responses). Letting these responses stack up in the FIFO is acceptable, but the user's software is responsible for knowing what each of the responses is.

During initialization, the user's software must flush the FIFO. Do this by reading the FIFO until the FIFO Ready flag is a one. This may take up to 512 reads, maximum.

Responses to user commands echo the command in the first two words from the FIFO. This can be useful in sorting out multiple responses stacked up in the FIFO.

6.3 - Reading Clock Time

The present ("clock") time is read as four 16-bit words. Reading the first word latches all four words, thus the latency time between reading them does not affect the accuracy. This also means that it is important to read the least significant word first, as this causes the other words to be latched. It is not necessary to read all four words if the application does not need the complete clock time.

Notes

- These locations are read-only. A different sequence is used to set the time. Refer to sections 8.5 and 8.6 for an explanation of setting the time.
- It is also necessary to examine the status register to determine if the time is valid.
- The Julian date (not Gregorian date) is reported.
- The value range for Days is 000-366. Be sure the variable that stores Days can accommodate this range. If you assign Days to an 8-bit integer (with a range of 000-255) you will get an unpleasant surprise in mid-September!

Within each 16-bit word there are four "nibbles" (groupings of 4 bits each). Each nibble is decoded separately, representing a single binary-coded-decimal (base 10) digit.

Location	Most Significant Nibble	Nibble	Nibble	Lease Significant Nibble
Base + 0x0e	10^0 mS	10^2 µS	10^1 µS	10^0 µS
Base + 0x0c	10^1 Seconds	10^0 Seconds	10^2 mS	10^1 mS
Base + 0x0a	10^1 Hours	10^0 Hours	10^1 Minutes	10^0 Minutes
Base + 0x08	(reserved)	10^2 Days	10^1 Days	10^0 Days

For example, if the time is day 123, hour 11, minute 58, second 17.654321, the time will be read as follows:

Location	Contents	
Base + 0x0e	0x4321	
Base + 0x0c	0x1765	
Base + 0x0a	0x1158	
Base + 0x08	0xU123	(U = Unknown)

6.4 - Sending Commands

Commands are sent to the board by writing to the Command Port at Base + 0x02. A small delay is required after sending each word. There is no way to "read-back" a command once it has been sent.

Commands consist of one or more 16-bit words, of which only the lower 8-bits are actually used. These lower 8-bits are further divided into two 4-bit "nibbles." For some commands, the high nibble is a constant, and the low nibble contains the data. For other commands both the high and low nibbles are constant.

It is necessary to wait at least 100 uS after sending each command word before sending anything else to the command port.

Function	Command
Reset Firmware	4f
Enable Sync	4d
Disable Sync	4e
Report Firmware Version in FIFO	e9
Report Number of GPS Satellites in FIFO (TSAT-PCI only)	5c
Report Altitude & Gregorian Date in FIFO	5d
Report Longitude in FIFO (TSAT-PCI only)	5e
Report Latitude in FIFO (TSAT-PCI only)	5f
Clear Holding Register	f0
Put 10^2 Days in Holding Register	50-53
Put 10^1 Days in Holding Register	60-69
Put 10^0 Days in Holding Register	70-79
Put 10^1 Hours or 10^{-1} Seconds in Holding Register	80-89
Put 10^0 Hours or 10^{-2} Seconds in Holding Register	90-99
Put 10^1 Minutes, 10^{-3} Seconds, or 16^3 Heartbeat in Holding Register	a0-af
Put 10^0 Minutes, 10^{-4} Seconds, or 16^2 Heartbeat in Holding Register	b0-bf
Put 10^1 Seconds, 10^{-5} Seconds, or 16^1 Heartbeat in Holding Register	c0-cf
Put 10^0 Seconds, 10^{-6} Seconds, or 16^0 Heartbeat in Holding Register	d0-df
Put Propagation Delay 10^3 µS in Holding Register	30-39
Put Propagation Delay 10^2 µS in Holding Register	20-29
Put Propagation Delay 10^1 µS in Holding Register	10-19
Put Propagation Delay 10^0 µS in Holding Register	00-09
Copy Holding Register to Clock Time or Propagation Time	e0
Copy Holding Register to Start/Stop Time (Days-Seconds)	e1
Copy Holding Register to Start Time (10^{-1} to 10^{-6} Seconds)	e2
Copy Holding Register to Stop Time (10^{-1} to 10^{-6} Seconds)	e3
Copy Holding Register to Clock Time on next 1PPS (-M Option only)	4c
Copy Holding Register to Heartbeat, Pulse Mode, at next period	e5
Copy Holding Register to Heartbeat, Pulse Mode, immediately	e6
Copy Holding Register to Heartbeat, Squarewave Mode, at next period	e7
Copy Holding Register to Heartbeat, Squarewave Mode, immediately	e8
Copy Holding Register to Year	ea

6.5 - Setting Clock Time

(Not applicable for boards with -M option)

The clock time is set by commanding the days, hours, minutes, and seconds. The milliseconds and microseconds cannot be commanded; they are reset to 000000 when the command is sent.

It is first necessary to load the time into the Holding Register. First, a command is sent to clear the Holding Register.

Then, one at a time, each digit (hundreds of days down to ones of seconds) is written into the Holding Register.

There is a separate command for loading each of these digits. The upper 4-bits of the command identify which digit is being loaded, the lower 4-bits contain the actual data to load. Once all the digits have been loaded, a command is sent to set the time (the board does this by copying the Holding Register into the clock).

For example, to set the clock to day 123, hour 11, minute 58, second 17, send the following sequence of commands to the Command Port:

```
0x00f0                                  ; Clear the Holding Register
0x0051      0x0062      0x0073          ; Day 123
0x0081 0x0091                           ; Hour 11
0x00a5 0x00b8                           ; Minute 58
0x00c1 0x00d7                           ; Second 17
0x00e0                                  ; Set Clock Time
```

Notes

- If no timecode input is present (TPRO-PCI), or the GPS receiver is not tracking satellites (TSAT-PCI), the board will accept the time set sequence described above and continue to increment time ("freewheel"). However, when a valid timecode (TPRO-PCI) is input, or when the GPS receiver begins tracking satellites (TSAT-PCI), the clock's time will jump to the decoded time, unless the above sequence was preceded with a Disable Sync command (described in section 8.12).
- While freewheeling, the In-Sync status bit will be false.
- The user's software must ensure that the commanded values are in the appropriate ranges. The board does not error-check the data before loading the clock. Commanding invalid values (e.g., 39 hours) will cause erratic operation.

6.6 - Setting Clock Time
(TPRO-PCI with -M Option Only)

The clock time is set by commanding the days, hours, minutes, and seconds. The milliseconds and microseconds cannot be commanded; they are reset to 000000 when the *next* one-pulse-per-second (1PPS) occurs. The clock time of the *next* one-pulse-per-second (1PPS) is commanded to the board.

It is first necessary to load the time into the Holding Register. First, a command is sent to clear the Holding Register.

Then, one at a time, each digit (hundreds of days down to ones of seconds) is written into the Holding Register.

There is a separate command for loading each of these digits. The upper 4-bits of the command identify which digit is being loaded, the lower 4-bits contain the actual data to load. Once all the digits have been loaded, a command is sent to arm the clock.

For example, to set the clock to day 123, hour 11, minute 58, second 17, send the following sequence of commands to the Command Port:

```
0x00f0                                  ; Clear the Holding Register
0x0051      0x0062      0x0073          ; Day 123
0x0081      0x0091                      ; Hour 11
0x00a5      0x00b8                      ; Minute 58
0x00c1      0x00d7                      ; Second 17
0x004c                                  ; Arm the clock for next 1PPS
```

After sending the 0x004c command, the board will set the milliseconds and microseconds to 000000 when the first 1PPS occurs (the seconds do not increment). Then, on the second 1PPS pulse, the time (seconds) begin incrementing.

Notes

- If both 1PPS and Timecode inputs are present, the board will sync to the incoming timecode and ignore the 1PPS.
- Commands 0x004d and 0x004e (Enable/Disable Sync) apply both to the 1PPS and the timecode input. Commands 0x00e0 (set clock) and 0x00ea (set year) are not applicable to boards with the -M option.
- The user's software must ensure that the commanded values are in the appropriate ranges. The board does not error-check the data before loading the clock. Commanding invalid values (e.g., 39 hours) will cause erratic operation.



#1–The board expects the 1PPS input to be continuous. If the 1PPS signal stops pulsing after the board establishes initial sync, the board will continue to increment time ("freewheel"). However, if the 1PPS signal resumes after a period of freewheeling, the board may reset the clock time to 000:00:00:00.000000. This is because the 1PPS occurs outside of a narrow window in which the board expects it, either because the 1PPS has moved or because the board's time has drifted during freewheeling.

#2–The arm command (0x004c) must be sent no sooner than 50 mS after the previous 1PPS occurred, and no later than 50 mS before the next (arming) 1PPS occurs.

6.7 - Setting the Year
(not applicable for boards with -M option)

Whether synchronized to GPS or timecode, or freewheeling, the IRIG-B output will count from day 365 to day 001, unless the year is set to a leap year. Once set to a leap year, the IRIG-B output will count from 365 to 366, then to 001. The TSAT-PCI obtains the year from the GPS satellites. The year can also be set by command (if the GPS receiver is not connected). The TPRO-PCI requires that the year be set by command to function properly at the end of a leap year. The board will increment the year when the day rolls over to 001. Also, setting the year enables the board (TPRO-PCI and TSAT-PCI) to compute the Gregorian date (YYYY-MM-DD) from the year and Julian date.

Set the year by sending the command sequence "0x006n 0x007n 0x008n 0x009n 0x00ea" to the command port. For example, to set the year to 2003, send "0x0062 0x0070 0x0080 0x0093 0x00ea".

The year is reset to 0000 when power is first applied, or when any of the following occur: system reset, firmware reset (command 0x004f), or writing to the "Assert Reset" or "De-assert Reset" addresses. Year 0000 is treated as a *n*on-leap year, and is *not* incremented to 0001 at the end of the year.

6.8 - Reading the Year, Gregorian Date, and Altitude
(not applicable for boards with -M option)

The GPS receiver's computation for the altitude (TSAT-PCI only) and Gregorian date (TSAT-PCI and TPRO-PCI) are reported in the FIFO in response to the 0x005d command. Altitude is in units of meters above mean sea level.

Gregorian date is year, month, day (e.g. 1997-09-30 for September 30, 1997).

Word	Bits 7 – 4	Bits 3 – 0
0 (first)	5	D
1	5	D
2	10^1 Day	10^0 Day
3	10^5 meters	10^4 meters
4	10^3 meters	10^2 meters
5	10^1 meters	10^0 meters
6	10^{-1} meters	0
7	10^1 Year	10^0 Year
8	10^3 Year	10^2 Year
9 (last)	10^1 Month	10^0 Month

The board increments the Gregorian date approximately one second after time rolls over from 23:59:59 to 00:00:00 (HH:MM:SS). This occurs on every date in every year. It is not specific to Year 2000 (Y2K). For this reason, the Gregorian date should not be used during minutes 59 and 00, to avoid rollover problems.

6.9 - Report Longitude
(TSAT-PCI only)

The GPS receiver's computation for longitude is put into the FIFO in response to the 0x005e command.

Units are degrees, minutes, and fractions of minutes. The response is in the following format:

Word	Bits 7 – 4	Bits 3 – 0
0 (first)	5	e
1	5	e
2	0	10^2 Degrees
3	10^1 Degrees	10^0 Degrees
4	10^1 Minutes	10^0 Minutes
5	10^{-1} Minutes	10^{-2} Minutes
6	10^{-3} Minutes	10^{-4} Minutes
7	reserved	reserved
8	reserved	reserved
9 (last)	reserved	reserved

Note

If the reported value is less than 180 degrees, the longitude is east (Europe, Africa, Asia, etc.) If the reported value is greater than or equal to 180 degrees, subtract 180 degrees to obtain west longitude (USA, Canada, Central & South America, etc.) For example, the reported value for Los Angeles, CA, USA, will be about 298 degrees. Since this is greater than 180, subtract 180 to get the correct value: 118 degrees West. Be sure to convert minutes to decimal degrees before comparing to 180 degrees.

6.10 - Report Latitude

(TSAT-PCI only)

The GPS receiver's computation for latitude is put into the FIFO in response to the 0x005f command.

Units are degrees, minutes, and fractional minutes. Latitudes north of the equator are reported as 0-90 degrees, latitudes south of the equator are reported as 180+ degrees South (i.e. - if the reported value is greater than or equal to 180, subtract 180 degrees and change the sign to negative (south)). Be sure to convert minutes to decimal degrees before comparing to 180 degrees. The response is in the following format:

Word	Bits 7 – 4	Bits 3 – 0
0 (first)	5	f
1	5	f
2	0	10^2 Degrees
3	10^1 Degrees	10^0 Degrees
4	10^1 Minutes	10^0 Minutes
5	10^{-1} Minutes	10^{-2} Minutes
6	10^{-3} Minutes	10^{-4} Minutes
7	reserved	reserved
8	reserved	reserved
9 (last)	reserved	reserved

6.11 - Report Number of GPS Satellites Being Tracked
(TSAT-PCI only)

The GPS receiver automatically determines which satellites to track. The number (quantity) of satellites being tracked is reported in the FIFO in response to sending command 0x005c to the command port. The response is of the following form:

Word	Bits 7 – 4	Bits 3 – 0
0 (first)	5	c
1	5	c
2	reserved	reserved
3	reserved	reserved
4	reserved	reserved
5	reserved	reserved
6	reserved	reserved
7	0	Number of Satellites
8	reserved	reserved
9 (last)	reserved	reserved

The number of satellites tracked is for diagnostic purposes only. The number of satellites ranges from 0 to 8, inclusive. Valid time and position require that at least four satellites be tracked. The In-Sync flag in the Status Register must be used to actually determine whether the board is synchronized and providing valid position.

There is no difference in timing accuracy when 5, 6, 7, or 8 satellites are being tracked. It is normal for the number to fluctuate between 5 and 8 as the GPS receiver picks different satellites to optimize the timing.

It is normal for the number of satellites to be between 0 and 3 during acquisition and re-acquisition.

6.12 - Enable/Disable Sync

The board can be forced to freewheel by sending the Disable Sync command. Sending this command causes the board to ignore the timecode input, the 1PPS input (-M only), and the GPS input (TSAT-PCI only). Normal operation is restored by sending the Enable Sync command.

To send the Disable Sync command, write 0x004e to the command port. To send the Enable Sync command, write 0x004d to the command port.

The power-on default is to Enable Sync.

6.13 - Reading the Status Register

The Status Register consists of one 16-bit word, of which only the lower 8 bits are used. The Status Register is read from location Base + 0x02, and is formatted as follows:

Bit	Name	Meaning When 0	Meaning When 1
0 (LSB)	FIFO Ready Flag	FIFO Ready (data available)	FIFO empty
1	Timecode Present	Timecode Input has no detectable signal	Timecode input has a signal present
2	In-Sync Flag	Clock is freewheeling GPS position is invalid	Clock is synced to timecode or GPS and GPS position is valid
3	Match Flag	Start time has not occurred	Start time has occurred
4	Heartbeat Flag	Heartbeat has not occurred	Heartbeat has occurred
5	Heartbeat Int. Mask	PCI bus interrupt disabled for heartbeat	PCI bus interrupt occurs on each heartbeat
6	Match Int. Mask	PCI bus interrupt disabled for start time	PCI bus interrupt occurs at the start time
7	FIFO Ready Int. Mask	PCI bus interrupt disabled for FIFO data available	PCI bus interrupt occurs when FIFO data available
8-15	(reserved)	(reserved)	(reserved)

Notes

- Bit 2 (In-Sync Flag) is the only bit to examine when determining the validity of the time (and position for TSAT-PCI).
- Bit 1 (Timecode Present) is for diagnostic purposes only. It only indicates that the amplitude of the Timecode Input is adequate for detection. It does not indicate whether the input is valid. This bit will always be zero for TSAT-PCI.
- Bits 5, 6, and 7 provide a means for reading-back the corresponding bits in the Interrupt Control Port.
- Bits 3 and 4 may be true ("1") when power is first applied. The user's software must clear bits 3 and 4 before using them.

6.14 - Interrupt Control Port

The board can generate interrupts when the FIFO has data, when each heartbeat occurs, and/or when the commanded Start time occurs. Each of these is separately enabled via the Interrupt Control Port, and any, all, or none can be enabled simultaneously.

The Interrupt Control Port is a single 16-bit word, of which only 3 bits are actually used. It is located at Base + 0x00, and is write-only. The bits in the Interrupt Control Port are defined as follows:

Bit	Name	Writing 0 Action	Writing 1 Action
0-4	(reserved)	(reserved)	(reserved)
5	Heartbeat Interrupt Mask	No PCI interrupt on heartbeat	Heartbeat causes PCI interrupt
6	Match Interrupt Mask	No PCI interrupt at start time	Start time causes PCI interrupt
7	FIFO Ready Int. Mask	No PCI interrupt when data is available in FIFO	PCI interrupt when data is available in FIFO
8-15	(reserved)	(reserved)	(reserved)

The board generates the same interrupt regardless of whether it was caused by heartbeat, Start time, or FIFO data available. After an interrupt, the user's software must interrogate the board to determine which of these was the cause.

The power-on default is to have all interrupts disabled. Also, sending the Assert Reset command disables all interrupts.



The FIFO Ready interrupt occurs each time the FIFO goes from being empty to having data. If the user's software quickly detects that the first word has been written into the FIFO and reads it out, it is possible for the FIFO to momentarily be empty. Thus, when the second word is put into the FIFO, another interrupt is generated. The solution is to disable the FIFO Ready interrupt until all 10 words have been read from the FIFO, then re-enable the interrupt.

6.15 - Setting the Propagation Delay Correction

This command is used to correct for delays due to cable length (timecode or GPS cables). Most applications do not need to compensate for cable delays because the delay is on the order of a hundred nanoseconds, while the clock's resolution is 1 microsecond. However, introducing a deliberate (large) offset can be helpful in situations where the board is used to trigger an instrument slightly *before* a particular time.

The range of the propagation correction is -1000 µS to +8999 µS. The power-on default is zero. To specify the propagation delay, first clear the Holding Register, then write four words (representing each of the digits in the delay value), then send the Set Clock Time/Propagation Time command. When specifying negative delays, a special number sequence is used. Specify delays from -1000 µS to -1µS by sending values of 9000 to 9999, respectively.

For example, to specify a correction of +4567 uS, send the following sequence of commands to the command port:

```
0x00f0                                          ; Clear the Holding Register
0x0034      0x0025      0x0016      0x0007      ; Specifies +4567 uS
0x00e0                                          ; set propagation correction
```

6.16 - Setting the Start/Stop ("Match") Times

(Not applicable for boards with –FXA, -FXB, or –HDRV options)

The match output (P1 pin 8) goes high at the Start time and low at the Stop time. The match interrupt occurs at the Start time (not at the Stop time). The match flag (in the Status Register) goes true at the Start time and remains true until the user clears it with a software command.

The Start and Stop times are each specified by first clearing the Holding Register, then commanding the days-through-seconds portion of the time, sending a set command, then sending the milliseconds through microseconds, then another set command.

For example, to command a Start time of day 123, hour 11, minute 58, second 17.456789, send the following sequence to the command port:

```
0x00f0                                  ; Clear Holding Register
0x0051      0x0062      0x0073          ; Day 123
0x0081      0x0091                      ; Hour 11
0x00a5      0x00b8                      ; Minute 58
0x00c1      0x00d7                      ; Second 17
0x00e1                                  ; send days-seconds
0x0084      0x0095      0x00a6          ; xx.456xxx seconds
0x00b7      0x00c8      0x00d9          ; xx.xxx789 seconds
0x00e2                                  ; send Start time
```

To specify the Stop time, the sequence is the same, except the final command is 0x00e3 (instead of 0x00e2).

The sequence must be completed at least 50 mS before the commanded time occurs.

The match output and interrupt (if enabled) will operate regardless of whether the board is in-sync or freewheeling.

6.17 - Programming the Heartbeat Output

(Not applicable for boards with -HB1PPS, -FXA, -FXB, -LOR1 options)

The heartbeat output (P1 pin 6) can be programmed to be either a pulse or a squarewave. The specified rate must be an exact multiple of 1.000 uS. The range of programmable rates is:

Minimum Rate (lowest frequency):	21.845 mS (45.7771 Hz)
Maximum Rate (highest frequency):	1.000 uS (1.000 MHz)
Pulse Width (time low, pulse mode only)	150 nS min, 450 nS max (negative polarity)

To specify the rate (or frequency), compute the divide number N as follows. Note that N must be exactly divisible by 3, meaning that the specified period must be an exact multiple of 1.000 uS.

To specify a period for a pulse or squarewave, compute N as follows:

$N = 3t/10^{-6}$ t is the period in seconds

To specify a frequency for a pulse or squarewave, compute N as follows:
$N = 3 * 10^{6}/F$ F is the frequency in Hertz

Not all values of N are acceptable. Verify that the computed value is evenly divisible by 3 and that it is in the range of 3 to 65,535, inclusive.

Convert N into hexadecimal (base 16) notation. For example, if the desired output frequency is 10 kHz, N=300 (base 10), converted to hexadecimal notation yields N= 0x012c. Send the hexadecimal number to the board by outputting the following sequence to the command register.

```
0x00f0                                          ; Clear the Holding Register
0x00a0      0x00b1      0x00c2      0c00dc      ; specifies N = 0x012c
```

The heartbeat output can be programmed to be a squarewave or a pulse, and can be programmed to begin immediately or at the beginning of the next cycle. Send one of the following commands to command port:

```
0x00e5      ; Pulse mode, starts at beginning of next cycle
0x00e6      ; Pulse mode, starts immediately
0x00e7      ; Squarewave, starts at beginning of next cycle
0x00e8      ; Squarewave, starts immediately
```

The heartbeat output is present regardless of whether the board is in-sync or freewheeling.

The power-on default is 100 PPS, pulse mode.

6.18 - Programming the Heartbeat Output

(-HB1PPS, -FXA, -FXB, and –LOR1 Options Only)

The heartbeat output (P1 pin 6) can be programmed to be either a pulse or a squarewave. The specified rate must be an exact multiple of 1.000 mS. The range of programmable rates is:

Minimum Rate (lowest frequency):	65.534 Seconds (0.0152593 Hz)
Maximum Rate (highest frequency):	2 mS (500 Hz)
Pulse Width (time low, pulse mode only)	1 mS (typical)
Programming Resolution	1 mS

To specify the rate (or frequency), compute the divide number N as follows.

To specify a period for a pulse or squarewave, compute N as follows:
N = t/.001 t is the period in seconds

To specify a frequency for a pulse or squarewave, compute N as follows:
N = 1000/F F is the frequency in Hertz

Verify that the computed value is in the range of 2 to 65,534, inclusive.

Convert N into hexadecimal (base 16) notation. For example, if the desired output period is once every 25 seconds, N=25,000 (base 10), converted to hexadecimal notation yields N= 0x61a8. Send the hexadecimal number to the board by outputting the following sequence to the command register.

```
0x00f0                                          ; Clear the Holding Register
0x00a6      0x00b1      0x00ca      0c00d8      ; specifies N = 0x61a8
```

The heartbeat output can be programmed to be a squarewave or a pulse, and can be programmed to begin immediately or at the beginning of the next cycle. Send one of the following commands to command port:

```
0x00e5      ; Pulse mode, starts at beginning of next cycle
0x00e6      ; Pulse mode, starts immediately
0x00e7      ; Squarewave, starts at beginning of next cycle
0x00e8      ; Squarewave, starts immediately
```

The heartbeat output is present regardless of whether the board is in-sync or freewheeling.

The power-on default is 1PPS, pulse mode.

6.19 - Using the Time Tag Input

When the rising edge of the Time Tag Input (P1 pin 4) occurs, the clock time is latched into a temporary register, then this register is loaded into the FIFO. An interrupt on the PCI bus is generated, if enabled. The user's software determines that a time tag has occurred in one of two ways: Either by examining the least significant bit of the Status Register (FIFO Ready flag) to see if it is a zero, or by waiting for an interrupt. Since the clock time is latched when the rising edge occurs, the Time Tag data will be correct regardless of how long it takes to read the FIFO.

For test purposes, a time tag event can be simulated by writing (any value) to Base + 0x12. The result is indistinguishable from a time tag event on P1 pin 4.

The FIFO response to either of these events is:

Word	Bits 7 – 4	Bits 3 – 0
0 (first)	0	0
1	0	0
2	0	10^2 Days
3	10^1 Days	10^0 Days
4	10^1 Hours	10^0 Hours
5	10^1 Minutes	10^0 Minutes
6	10^1 Seconds	10^0 Seconds
7	10^{-1} Seconds	10^{-2} Seconds
8	10^{-3} Seconds	10^{-4} Seconds
9 (last)	10^{-5} Seconds	10^{-6} Seconds

For example, if the time tag occurs at day 123, hour 11, minute 58, second 17.456789, the contents read from the FIFO will be:

Word	Contents	
0 (first)	0xUU00	(U = Unknown)
1	0xUU00	
2	0xUU01	
3	0xUU23	
4	0xUU11	
5	0xUU58	
6	0xUU17	
7	0xUU45	
8	0xUU67	
9 (last)	0xUU89	

Notes

- The Julian date (not the Gregorian date) is reported.
- Erratic operation may result if the rate of time tags exceeds 1000 per second.
- Refer to section 3.3 regarding jumper JP10.
- There may be a delay of up to 200 uS before time tag data is available in the FIFO.
- Some older boards repeated words 2 and 3 in bytes 0 and 1, respectively.

6.20 - Report Firmware Version

The version of the embedded firmware is reported in the FIFO in response to the 0x00e9 command. For example, firmware version 7A104221 is reported as:

Word	Bits 7 – 4	Bits 3 – 0
0 (first)	E	9
1	E	9
2	7	A
3	1	0
4	4	2
5	2	1
6	unknown	unknown
7	unknown	unknown
8	unknown	unknown
9 (last)	unknown	unknown

Notes

- Firmware version is for diagnostic purposes only. It is not possible to determine which options are present, nor which version is more recent, by examining the version number.
- The firmware version is also printed on the label on device U19.
- Some older boards ignore the 0x00e9 command.

6.21 - Clear Flags Port

Once the Match and/or Heartbeat flag(s) get set, it is necessary to clear the flag by writing a one to the appropriate bit of this register at location Base + 0x10.

Bit	Name	Writing 0 Action	Writing 1 Action
0-2	(reserved)	(reserved)	(reserved)
3	Clear Match	Match flag does not change	Clear match flag to zero
4	Clear Heartbeat	Heartbeat flag does not change	Clear heartbeat flag to zero
5-15	(reserved)	(reserved)	(reserved)

Note

If used as an interrupt, the user's software needs to clear the Match Flag each time the Start time occurs. Failure to do so will result in missed interrupts (if enabled) until the flag is cleared.

If used as an interrupt, the user's software needs to be fast enough to clear the Heartbeat Flag each time a heartbeat occurs. Failure to do so will result in missed interrupts (if enabled) until the flag is cleared.

6.22 - Reset Firmware

This command is for diagnostic purposes only; it should not be used during normal operation. Writing 0x004f to the command port causes the embedded firmware to reset. This command does not reset the hardware or the PCI bus interface. Wait at least 8 seconds after sending this command before commanding or interrogating the board.

6.23 - Assert/De-assert Reset

These commands are for diagnostic purposes only. Sending the Assert Reset command holds the hardware reset signal on the board in the asserted state. This stops the on-board CPU and clears the interrupt masks and Match and Heartbeat Flags. The only command that the board will respond to in this state is the De-assert Reset command. The PCI bus interface is not affected.

Send the Assert Reset command by writing any data value to location Base + 0x06. Send the De-assert Reset command by writing any data value to Base + 0x04. Wait at least 8 seconds after sending the De-assert Reset command before commanding or interrogating the board.

Note

#1–After the Assert Reset command is sent, the diagnostic light on the rear panel stops flashing (it may be either lit or not lit). This can be used as an indication to determine if the user's software is capable of writing to the board (i.e. - that the PCI bus addressing is working correctly).

#2–Sending the De-assert Reset command without first sending an Assert Reset command will also reset the board.

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