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DSP TECHNOLOGY INC.

MODEL 1402E

USER MANUAL

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TABLE OF CONTENTS

INTRODUCTION 4

SPECIFICATIONS 5

FRONT PANEL INDICATORS AND CONTROLS 7

INSTALLATION AND OPERATION 9

PROGRAMMING 11

APPENDIX A: PROGRAM EXAMPLES 16

SCHEMATICS 17

WARRANTY 18

SECTION I

INTRODUCTION

DSP MODEL 1402
PROGRAMMABLE AMPLIFIER WITH ANTIALIASING FILTER

* **Programmable amplifier gains of up to 5000**
* **Choice of Butterworth-, Bessel-, or Elliptic-Type Filter**
* **Programmable frequency cutoff for filters**
* **Programmable 0-, 4- or 8-pole Filter Attenuation Characteristic**
* **Cutoff frequencies from 100Hz to 100kHz**
* **Pre- and Post-Filter Amplifiers for high sensitivity without filter saturation**
* **State of the art instrumentation amplifier specifications**
* **Compatible with the TRAQ Analog Bus (TRAQAB)**

DSP Technology's Model 1402 is a high-gain instrumentation amplifier and antialiasing filter for use with the TRAQ I data acquisition system. Intended for use with strain gage, thermocouple, acoustical, and accelerometer transducers, the programmable filter characteristics and optional filter types cover a range of cutoff frequencies between 100Hz and 100kHz.

The rugged CAMAC package can be used in severe environments from airborne applications to explosives testing. Its modular construction allows immediate reconfiguration for changing applications without expensive system interaction problems.

Specifically matched to the Model 2812, an 8 channel 12 bit ADC front end to the TRAQ I system, the transducer signal conditioner is backed by a system of up to 256 front end converters and as much as 16 Megawords of data storage per system.

TYPICAL 1402 FILTER BODE PLOT (8 POLE BUTTERWORTH)

SECTION 2

SPECIFICATIONS

INDICATORS	LED indicates overload condition (each channel) LED indicates when module is addressed
INPUT	
Type:	Differential LEMO. DC-coupled.
Impedance:	>20 MOhm
Level:	± 10 Volts
Protection:	± 30 Volts
GAIN	
Gain:	
PreFilter:	x1 - x100 Programmable (1-2-5 sequence)
PostFilter:	x1 - x 50 Programmable (1-2-5 sequence)
Accuracy:	1.0%
Stability:	0.3% @ 10 - 40 degrees C
Bandwidth	
Gain x1-x500	100 kHz (3dB)
> x1000	50 kHz
Common Mode Rejection:	>70 dB @ 60Hz 30 dB + PreFilter Gain(dB) @ 100 kHz
Voltage Range:	+/- 12 V
Noise:	< 15nV/sqrt(Hz) @ max gain RTI
Output:	>5mV @ x1 PostGain
Input:	<15 uV @ x100 PreGain
Offset:	Adjustable to zero (programmable)
FILTER	
Types:	Butterworth 4 pole Butterworth 8 pole Bessel 4 pole Bessel 8 pole Elliptic Optional (programmable)
Pass Band Characteristic:	
Butterworth:	0 dB (maximally flat)
Elliptic:	±0.1 dB ripple
Bessel:	±0.3 dB ripple
Stop Band Characteristic:	
Butterworth:	48 dB per octave
Elliptic:	80 dB minimum

Bessel:	72 dB minimum
Cut-off Frequency(Fco):	
Ranges:	10Hz-100kHz in 4 decades (programmable)
Resolution:	200 steps per decade (programmable)
Interchannel Phase Accuracy:	+/- 1.0 Degree (DC - Fco) +/- 0.5 Degree (DC - Fco) for gains less than 200
CALIBRATION	Internal 12-bit (0.025%) DAC can be switched into amplifier input for calibration purposes.
ANALOG BUS	Output signals of 1402 channels may be programmed to be transferred (via a high-impedance, buffered analog bus) to modules which are compatible with the TRAQ analog bus. (MCTRAQAB mating connector)
OUTPUT	
Type:	Single-ended LEMO. DC coupled
Impedance:	< 50 Ohm
Level:	+/- 10 V Full Scale @ 15 mA
PACKAGING	
Type:	CAMAC #1 Module Conforms to ESONE/IEEE583 standard.
Channels:	2 per module
Power:	10 Watts per channel (typical)
+6 Volts	900 mA
+24 Volts	325 mA
-24 Volts	325 mA
Weight:	2 lb
OPTIONS	
EXCITATION	1402E
Type	10 mA (max) constant current 0 - 11 V compliance
Connection	LEMO
Channels	2 per module

SECTION 3

FRONT PANEL INDICATORS AND CONTROLS

The front panel is divided into 3 sections

System Status

Channel Status

Channel Input/Output

3.1 SYSTEM STATUS

3.1.1

Name N

Purpose Indicates module access via CAMAC

Type LED - red

3.2 CHANNEL STATUS

Channel status is displayed for each channel independently.

3.2.1

Name CAL

Purpose Channel Mode indicator

OFF : Amplifier/Filter mode
ON : Calibrate mode

Type LED - green

3.2.2

Name OVLD

Purpose Channel Signal level indicator

ON: Signal amplitude in filter section exceeds fullscale limit.

Type LED - Red

3.3 SIGNAL INPUT/OUTPUT

Each channel has independent input and outputs.

3.3.1

Name	INPUT
Purpose	Channel Signal Input connection
Full Scale	4 mVolt(x5000 gain) - 20 Volts(x1 gain), Bipolar
Protection	30 Volts MAX
Impedance	>20 MOhm
Type	Differential LEMO DPL-00.425 - chh

1: Negative (-) Input
2: Positive (+) Input

3.3.2

Name	OUTPUT
Purpose	Channel Amplifier/Filter Output.
Full Scale	20 Volts, Bipolar (+/- 5 mA)
Type	LEMO F00.025 - chh

3.4 REAR PANEL CONNECTION

Connection to the TRAQ ABus is made at the rear of the DSP1402 module. This attaches the DSP1402 channel outputs to supplemental signal conditioning or processing modules. The TRAQ ABus outputs are isolated from the front panel channel outputs to minimize interference. Refer to the installation and programming sections for information on the use of the TRAQ ABus.

3.4.1

Name	TRAQ ABus
Purpose	Connects DSP1402 Outputs to TRAQ ABus.
Type	40 Pin IDC type connector

Pin Description

SECTION 4

INSTALLATION AND OPERATION

The DSP1402 Amplifier/Filter module may be used in various configurations, with a number of associated signal conditioning and data acquisition instruments. This section discusses issues important during installation and use in order to acheive the full capability of the DSP1402.

4.1 SIGNAL CONNECTION

Input connection to the DSP1402 module is made at the front panel using differential miniature coaxial connectors (LEMO type). The high input impedance (1 MOhm) , high sensitivities (x2000), and wide bandwidth (100 KHz) involved requires care in establishing a reliable and accurate signal path. All low level signals should be differentially driven (+/-) with a separate ground shield enclosing each signal cable. Common mode (noise or interference appearing on both sides of the differential signal) rejection is maximized by use of differential (balanced) signals.

Ground shields should be connected in a "star" configuration, namely all tied to one common point, in order to minimize ground currents. A ground reference must be established between the DSP1402 and the signal source in order to maintain the common mode voltage range.

4.2 AMPLIFIER CONFIGURATION

Overall channel amplification factor is set by the combination of the pre-amplifier and post-amplifier gains. There can be a number of gain combinations yielding the same channel sensitivity. Selection of the appropriate one can affect system performance. The selection is a trade off between noise and distortion. In general, highest gain settings should be selected in the pre-amp section. The post-amp gain is then set to establish the channel amplification. Such an approach will maximize the DSP1402 signal to noise ratio by limiting the amplification of the noise contribution from the pre-amp and filter sections.

Situations where this approach is not recommended include signal sources containing high level out-of-band frequency components. Pre-amplification can thus result in overdriving the filter section. This will lead to distortions extending to the lower frequency components. In these situations, reducing the pre-amp gain to avoid saturation in later stages will require larger levels of amplification following the filter section.

Each DSP1402 channel has an overload detector that indicates the relative signal level at the input to the filter section. The OVLD front panel indicator and CAMAC LAM will trigger when a signal level exceeds the nominal fullscale range of the filter (+/-10V). A headroom (margin) of 50% is provided to handle transient overloads.

4.3 FILTER

Low pass cutoff frequency is programmed from 10Hz to 100KHz. Cutoff is defined here as being the frequency where the channel gain is - 3dB (0.707) of the DC (0 Hz) gain. Filter frequency is selected by specifying a range (decade grouping) and a sub-multiplier. For example, a 250 Hz cutoff is set by programming for the 1KHz range (101 - 1KHz) and a submultiplier of 0.25. The actual code programmed into the DSP1402 is determined by the transfer equation (see section on programming).

Filter characteristics are also selectable via program control. These types are Butterworth or Bessel. Elliptic or a custom option filter types are also available. Each has a unique rolloff characteristic, either in the frequency or time domain. The principle features and applications of these types is shown in Table 4.1.

TABLE 4.1 FILTER TYPES and APPLICATIONS

Type	Characteristics	Application
Butterworth	6 dB/octave/pole Maximally Flat	Uniform/flat gain
Bessel	<6 dB/octave/pole Minimum group delay Poor frequency cut-off	Time domain analysis Pulse/risetime measurements
Elliptical	>6dB/octave/pole Excellent cutoff frequency definition Poor phase response	Frequency domain analysis Signals close to Nyquist

SECTION 5

PROGRAMMING

The DSP1402 is divided into two (2) identical channels, referenced as Channel 1 and Channel 2. Within each channel, programmable registers determine mode of operation and control settings for both the amplifier and filter functions. This section describes these registers and their function.

Module programming conforms to CAMAC (IEEE583) standard protocol. Valid commands are acknowledged with CAMAC X (i.e. X=1). CAMAC Q is set when data is valid during a read or the register was available during a write operation.

5.1 MODE REGISTERS

These registers set/interrogate channel configuration, amplifier gain and module ID. All registers are both readable and writable, with the CAMAC write function code corresponding to the register number + 16. Subaddress CAMAC codes are used for channel addressing.

All registers are non-volatile (i.e. retain their contents on loss of power) provided the SAVE REGISTERS command has been executed. On power-up the registers must be read and written back to the unit in order to fully reestablish the previous operating mode.

NOTE

> All 1402 registers MUST be initialized on powerup. This includes all filter sectin registers and both channels, regardless whether the channel or filter section is to be used. Failure to do so may result in erratic behavior or increased noise levels.

Internally all registers are 12 bits in length. Bits are numbered [1..12] where bit12 is the MSB and bit1 is the LSB (Least Significant Bit). Only the specified bits for each command are decoded or interpreted by the hardware. Undefined bits in each register may be used by the application program without affecting the unit.

5.1.1

Name	**MODE**	
Purpose	Amplifier and Filter mode control.	
Definition	10 Bits encoded	
	Channel 1	Channel 2
Write	F(16) A(0)	F(16) A(4)
Read	F(0) A(0)	F(0) A(4)

5.1.1 Mode Register continued

Description

Filter Type	[D1..D2]
Bessel 8 Pole	0
Butterworth 8 Pole	1
reserved	2
reserved	3

TRAQ Bus Select	[D3..D5]
Bus line 1	0
...	...
Bus line 8	7

TRAQ Bus Enable	D6
Disable 1402 Channel	0
Enable	1

Filter Order	[D7..D9]
None (no filter)	1
4 Pole	2
8 Pole	4

Calibrate Mode	D10
Normal	0
Calibrate	1

Example Set Channel 1 for Filter type= Butterworth 8,no TRAQ connection, 8Poles, not calibrate mode

F(16)A(0) Data = 0 100 0 000 01 =0101Hex

5.1.2

Name	AMPLIFIER GAIN	
Purpose	Set amplifier gain sections	
Definition	6 Bits encoded	
	Channel 1	Channel 2
Write	F(16)A(1)	F(16)A(5)
Read	F(0)A(1)	F(0)A(5)
Description	Controls pre-amplifier and post-amplifier gain settings.	

PreAmp	x1	x10	x100
D1..D3	1	2	4

PostAmp	x1	x1.25	x2	x5	x10	x20	x50	x100
D4..D6	0	1	2	3	4	5	6	7

PreAmp	x1000 (optional)
D7	1

5.1.3

Name	OFFSET	
Purpose	Set channel zero (offset)	
Definition	12 bits offset binary	
	Channel 1	Channel 2
Write	F(16) A(2)	F(16) A(6)
Read	F(0) A(2)	F(0) A(6)

Description: Controls pre-amp offset over a range of +/- 0.5 Fullscale. Note: reading offset register returns programmed value.

Example: Set channel 1 offset to voltage V.
F(16) A(2) Data=(Volts*4096/Full Scale) + 2048.

5.1.4

Name	REFERENCE	
Purpose	Set reference input signal level.	
Definition	12 bits offset binary	
	Channel 1	Channel 2
Write	F(16) A(3)	F(16) A(7)
Read	F(0) A(3)	F(0) A(7)

Description: Controls programmable reference voltage which is used as the channel input source in CALIBRATE mode. Range is +/- 0.5Fullscale. Note: Reading reference register returns programmed value.

Example: Set channel 1 reference to voltage V.
F(16) A(3) Data = (Volts*4096/FullScale) + 2048.

5.1.5

Name	CUTOFF	
Purpose	Set filter cutoff frequency	
Definition	10 bits encoded	
	Channel 1	Channel 2
Write	F(17) A(0)-A(7)	F(17) A(8)-A(15)
Read	F(1)	F(1)

Description: Controls cutoff frequency (-3dB point) of selected filter type. All subaddresses (0-7 or 8-15) MUST be programmed explicitly. Note: Reading cutoff register returns programmed value.

Range	Frequency Range	[D9..D10]	Fmax
100	10..100Hz	0	100
1K	100 .. 1KHz	1	1000
10K	1K .. 10KHz	2	10KHz
100K	10k .. 100 kHz	3	100KHz

SubMultiplier	[D1..D8]
0.1	20
..	..
0.5	100
..	..
1.0	200

The filter consists of 4 sub-sections. Each section must be programmed for the appropriate cutoff frequency. Frequency is determined by a 10 bit code which is determined by the type of filter desired.

Butterworth 8 Pole

Each section is programmed with the same frequency code corresponding to the desired cutoff frequency.

Fcutoff = SubMultiplier * Fmax / 200

submultiplier = 200 * Fcutoff / Fmax

Example:

```
function u1402ButterworthFco(freq : integer) : integer;
{compute 1402 fco code for cutoff freq (in Hz) for Butterworth}
begin
     FFACTOR := 200;  {Butterworth Filter Factor}
     range := 10; decade := -1;
     repeat
       range := range * 10;
       decade := decade + 1;
       mult := (FFACTOR * freq) div range;
     until (mult<255) or (decade>=3);
     if (mult>255) then mult := 255;
     u1402fco := 256 * decade + mult;
end;
```

Bessel 8 Pole

Each section is programmed to a unique value as determined by the desired cutoff frequency.

Section	Chan1	Chan2	FFactor
1	A0, A1	A8, A9	2.1583
2	A2, A3	A10, A11	1.9260
3	A4, A5	A12, A13	1.8066
4	A6, A7	A14, A15	1.7537

The following code is an example subroutine which computes the required stage filter codes for a specified filter type and cutoff frequency.

```
procedure u1402FCOtoCode(Ftype : integer; Freq : real; stage : integer;
                         var dec,cutoff : integer);

var
  FCal  : real;
  range  : real;
  decade : real;
  mult   : real;
  fco    : integer;
  SFactor : array[1..4] of real;
  i : integer;

 begin
  case FType of
0 : begin                    {bessel 8 pole}
      SFactor[1] := 2.1583;      {section 1 cutoff}
      SFactor[2] := 1.9260;
      SFactor[3] := 1.8066;
      SFactor[4] := 1.7537;
  end;

1 : for i := 1 to 4 do SFactor[i] := 1.0;  {Butterworth 8 pole}

else
 for i := 1 to 4 do SFactor[i] := 1.0
 end;  {reserved type}

FCal := 200*SFactor[Stage];
range := 10;
decade := -1;
repeat
   range := range*10;
   decade := decade +1;
   mult := FCal*Freq / range;
until (Mult<255) or (decade>=3);
if (mult>255) then mult := 255;
fco := round(mult);
dec := round(decade);
cutoff := fco;
end;

{************************************************************************}
```

5.1.6

Name	ID	
Purpose	Read Module Identifier	
Definition	12 bits	
	Channel 1	Channel 2
Write	not available	not available
Read	F(3) A(0)	F(3) A(1)
Description	Returns module ID = 1402	

5.2 CONTROL REGISTERS

These commands determine the DSP1402 operating mode and return status information about the module.

5.2.7

Name	ENABLE LAM
Purpose	Enable Channel LAM on Dataway
Definition	Channel 1 Channel 2 F(26) A(0) F(26) A(1)
Description	Enables channel's LAM (indicating signal overload) onto CAMAC dataway. Does not affect INTERROGATE LAM command.

5.2.8

Name	DISABLE LAM
Purpose	Disable Channel LAM from Dataway
Definition	Channel 1 Channel 2 F(24) A(0) F(24) A(1)
Description	Disables channel's LAM from CAMAC dataway. Does not affect INTERROGATE LAM command.

5.2.9

Name	INTERROGATE LAM
Purpose	Returns LAM status
Definition	Channel 1 Channel 2 F(8) A(0) F(8) A(1)
Description	Returns channel's LAM status in CAMAC Q register. CAMAC Q is set (Q=1) if LAM is ON, indicating channel overload occurred.

5.2.10

Name	CLEAR LAM
Purpose	Clears LAM status
Definition	Channel 1 Channel 2 F(10) A(0) F(10) A(1)
Description	Clears channel's LAM status register. LAM status is set if channel signal overload occurs. This status is latched, i.e. remains set when overload condition is removed.

5.2.11

Name	SAVE
Purpose	Saves current mode register settings.
Definition	F(25) A(0)
Description	Stores currrent register contents in non-volatile memory for subsequent recall. On power-up or execution of the RECALL command the saved values are recalled.
Example	To save the module's configuration for future recall: F(25) A(0) Data = XXXX (not used)

5.2.12

Name	RECALL

Purpose — Restores previously stored mode settings .

Definition — F(27) A(0)

Description — Recalls register contents stored in non-volatile memory by means of SAVE command. To restore the unit to the correct configuration, each register must be explicitily read and then written back to the unit.

Example — To restore unit to "saved" configuration:

```
RECALL    F(25) A(0)
```

Read/Write all regs

```
For i := 0 to 15 do
  begin
  F( 0) A(i)   /* read the amp registers */
  F(16) A(i)     /* write back out */
  F( 1) A(i)   /* read the filter regs */
  F(17) A(i)     /* write back out */
  end.
```

5.3 CAMAC COMMAND SUMMARY

F0	A0	read	Mode register Channel 1
F0	A1	read	Amplifier gain Channel 1
F0	A2	read	Offset Channel 1
F0	A3	read	Reference Channel 1
F0	A4	read	Mode register Channel 2
F0	A5	read	Amplifier gain Channel 2
F0	A6	read	Offset Channel 2
F0	A7	read	Reference channel 2
F1	A0	read	Channel 1 FCO stage 1
F1	A1	read	FCO stage 2
..	..	..	...
F1	A7	read	FCO stage 8
F1	A8	read	Channel 2 FCO stage 1
F1	A9	read	Channel 2 FCO stage 2
..	..	..	...
F1	A15	read	Channel 2 FCO stage 8
F3	A0	read	Channel 1 ID
F3	A1	read	Channel 2 ID
F8	A0	read	Channel 1 LAM status
F8	A1	read	Channel 2 LAM status
F10	A0	exec	Channel 1 LAM clear
F10	A1	exec	Channel 2 LAM clear
F16	A0	write	Channel 1 Mode register
F16	A1	write	Channel 1 Amplifier gain
F16	A2	write	Channel 1 Offset
F16	A3	write	Channel 1 Reference
F16	A4	write	Channel 2 Mode
F16	A5	write	Channel 2 Amplifier Gain
F16	A6	write	Channel 2 Offset
F16	A7	write	Channel 2 Reference
F17	A0	write	Channel 1 FCO stage 1
F17	A1	write	FCO stage 2
..	..	..	...
F17	A7	write	FCO stage 8
F17	A8	write	Channel 2 FCO stage 1

5.3 CAMAC COMMAND SUMMARY

F17	A9	write		FCO stage 2
..	..	..	...	
F17	A15	write	Channel 2	FCO stage 8
F24	A0	exec	Channel 1 LAM disable	
F24	A1	exec	Channel 2 LAM disable	
F25	A0	exec	SAVE	
F26	A0	exec	Channel 1 LAM enable	
F26	A1	exec	Channel 2 LAM enable	
F27	A0	exec	RECALL	

APPENDIX A: Programming Examples

The following listings demonstrates control of DSP1402 registers and functions. The programs are written in PASCAL (Borland Turbo V3 for MS-DOS) and call standard DSP9200 CAMAC 6001/2 drivers.

```
{=============================================================================
MODULE  :u1402E
PURPOSE :1402E utilities
FILE    :u1402E.inc
CONTENTS:
General utilities for 1402 filter/amp

-----------------------------------------------------------------------
REVISION HISTORY
04/27/87 miller created
06/02/87 miller added reference register access
                changed Offset address per Rev A
03aug88  mm     created from u1402.inc
13aug88  mm     added u1402FCOwrite/Read for individual sections
=============================================================================}

procedure  u1402AmpRead(        chan : integer;
                           var PreGain  : integer;
                           var PostGain : integer;
                           var Offset   : integer);
{
 return Amplifier gain/offset setttings
}
var
  i : integer;

begin
if (Chan=0) then uA := 1 else uA := 5;
uF := 0;
cami(uN,uF,uA,uD,uQ,uX);

if (uD AND $0040)<>0 then
   Pregain := 1000
else
  begin
  i := uD and $0007;          {lower 3 bits}
  case i of
  1: PreGain := 1;
  2: PreGain := 10;
  4: PreGain := 100;
  else Rcode:= INVALID; PreGain := 99; end;
  end;

i := (uD shr 3) and $0007;  {shift down}
```

```
case i of
0: PostGain := 1;
1: PostGain := 1;      {1.25 not supported here}
2: PostGain := 2;
3: PostGain := 5;
4: PostGain := 10;
5: PostGain := 20;
6: PostGain := 50;
7: PostGain := 100;
else RCode := INVALID; PreGain := 99; end;

uA := uA + 1;                    {old calib DAC}
cami(uN,uF,uA,uD,uQ,uX);
Offset := uD and $0FFF;          {12 bits}

end;
{*************************************************************************}

procedure u1402ModeRead(    Chan       : integer;
                        var FilterType : integer;
                        var NofPoles   : integer;
                        var TraqAddr   : integer;
                        var CalMode    : boolean);
{
read 1402 mode register
}
var
  i : integer;

begin
  if (Chan=0) then uA := 0 else uA := 4;
  uF := 0;
  cami(uN,uF,uA,uD,uQ,uX);
  FilterType := uD and $0003;    {lower 2 bits}
  TraqAddr   := (uD shr 2) and $000F;   {DB3-DB6}
  if (TraqAddr>=8) then TraqAddr := TraqAddr-7 else TraqAddr := 0;

  i  := (uD shr 6) and $0007;   {DB7-DB9}
  case i of
    1 : NofPoles := 0;
    2 : NofPoles := 4;
    4 : NofPoles := 8;
    else NofPoles := 9 end;    {invalid number}

  if ((uD shr 9) and $0001)=NONE then CalMode := FALSE else CalMode := TRUE;
end;
{*************************************************************************}
```

```
procedure u1402CalRead(  chan : integer; var CalValue : integer);
{
  read calibration register
}
begin
  if (Chan=0) then uA := 3 else uA := 7;
  uF := 0;
  cami(uN,uF,uA,uD,uQ,uX);
  CalValue := uD;
end;
{*************************************************************************}
procedure u1402CoeffRead( chan : integer; var Decade,CutOff : integer);

{
 read Filter Cutoff coefficient
}
begin
  if (Chan=0) then uA := 0 else uA := 2;
  uF := 1;
  cami(uN,uF,uA,uD,uQ,uX);
  Cutoff := uD and $00FF;   {lower 8 bits}
  Decade := (uD shr 8) and $0003  {db9 and 10}
end;
{*************************************************************************}
procedure  u1402AmpWrite( chan : integer;
                          PreGain  : integer;
                          PostGain : integer;
                          Offset   : integer);

{
 load 1402 Amplifier gain/offset setttings
}
var
  i : integer;

begin
i := 4;                          {gain x100}
if (PreGain>500) then i := $0040;   {db7 set}
if (PreGain<=500) then i := 4;
if (PreGain<=50) then i := 2;       {x10}
if (PreGain<=5) then  i := 1;       {x1}
uD := i;          {preamp}

i := 7;
if (PostGain<=50) then i := 6;
if (PostGain<=20) then i := 5;
if (PostGain<=10) then i := 4;
if (PostGain<=5) then i := 3;
if (PostGain<=2) then i := 2;
if (PostGain<=1) then i := 0;
uD := (i shl 3) or uD;          {post amp}
```

```
{
write('WriteAMP:Pre:',PreGain:2,i:2);
writeln(' Post:',PostGain:2,i:2,' uD:',___toHexStr(uD));
}

if (Chan=0) then uA := 1 else uA := 5;
uF := 16;
camo(uN,uF,uA,uD,uQ,uX);
{repeat until keypressed;}
uA := uA + 1;                          {new offset is old calib}
camo(uN,uF,uA,Offset,uQ,uX);
end;
{*************************************************************************}

procedure u1402ModeWrite( Chan       : integer;
                          FilterType : integer;
                          NofPoles   : integer;
                          TraqAddr   : integer;
                          CalMode    : boolean);
{
write 1402 mode register
}
var
  i,j : integer;


begin
  if (CalMode) then uD := $0200 else uD := 0;   {set DB10}
  case NofPoles of
  0 : i := 1;
  4 : i := 2;
  8 : i := 4;
  else NofPoles := 0; i := 1 end;  {invalid so set to 0 poles}

  if (TraqAddr>0) and (TraqAddr<9) then
    j := 7 + TraqAddr        {set enable bit and 0..7}
  else
    j := 0;                  {disable}

  uD := uD or (i shl 6) or (j shl 2) or FilterType;
  if (Chan=0) then uA := 0 else uA := 4;
  uF := 16;
  camo(uN,uF,uA,uD,uQ,uX);
{
  writeln('Traq code:',TraqAddr:2,' j=',j:1);
  repeat until keypressed;
}
end;
{*************************************************************************}
```

```
procedure u1402CalWrite(  chan : integer; CalValue : integer);
{
  write calibration register
}
begin
  uD := CalValue;
  if (Chan=0) then uA := 3 else uA := 7;     {old offset}
  uF := 16;
  camo(uN,uF,uA,uD,uQ,uX);
end;
{*********************************************************************}
procedure u1402CoeffWrite( chan : integer; Decade,CutOff : integer);

{
 write Filter Cutoff coefficient
}
var
  i,iBase : integer;

begin
  uD := (Decade shl 8) or (CutOff and $00FF);
  if (Chan=0) then iBase := 0 else iBase := 8;
  uF := 17;
  for i := 0 to 7 do
    begin
    uA := iBase + i;
    camo(uN,uF,uA,uD,uQ,uX);
    end;
end;
{*********************************************************************}
procedure u1402FcoWrite(chan,stage,Range,FCO : integer);
{
 write Filter Cutoff coefficient for a stage[1..4] (1402E)
}
var
  i,iBase : integer;

begin
  uD := (Range shl 8) or (FCO and $00FF);
  if (Chan=0) then iBase := 2*(stage-1) else iBase := 8+2*(stage-1);
  uF := 17;
  for i := 0 to 1 do
    begin
    uA := iBase + i;
    camo(uN,uF,uA,uD,uQ,uX);
    end;
end;
{*********************************************************************}
```

```
procedure u1402FcoRead(chan,stage : integer;
                       var range,fco : integer);

begin
  if (Chan=0) then uA := 2*(stage-1) else uA := 8+2*(stage-1);
  uF := 1;
  cami(uN,uF,uA,uD,uQ,uX);
  fco := uD and $00FF;   {lower 8 bits}
  Range := (uD shr 8) and $0003  {db9 and 10}
end;
{*************************************************************************}



procedure u1402IDWrite(id : integer);

var
 i : integer;

begin
  uF := 19; uA := 0; uD := id;
  for i := 0 to 1 do  camo(uN,uF,i,uD,uQ,uX);       {write ID}
end;
{*************************************************************************}
procedure u1402IDRead(var id : integer);

begin
  uF := 3; uA := 0;
  cami(uN,uF,uA,ID,uQ,uX);       {write ID}
end;
{*************************************************************************}
procedure u1402LamClear( chan : integer);
{
 clear channels lam
}
begin
 uF := 10; uA := Chan;
 camo(uN,uF,uA,ud,uQ,uX);
end;
{*************************************************************************}
procedure u1402LamDisable( chan : integer);
{
 disable channels lam
}
begin
 uF := 24; uA := Chan;
 camo(uN,uF,uA,ud,uQ,uX);
end;
{*************************************************************************}
```

```
procedure u1402LamEnable( chan : integer);
{
 enable channels lam
}
begin
 uF := 26; uA := Chan;
 camo(uN,uF,uA,ud,uQ,uX);
end;
{*************************************************************************}
function u1402LamInternal( chan : integer) : boolean;
{
 interrogates 1402 channels internal lam
}
begin
  uF := 8; uA := Chan;
  cami(uN,uF,uA,ud,uQ,uX);
  if (uQ=1) then u1402LamInternal := TRUE else u1402LamInternal := FALSE;
end;
{*************************************************************************}
procedure u1402Save;
{
 save 1402 registers in XICOR EEPROM
}
begin
  uF := 25; uA := 0;
  camo(uN,uF,uA,uD,uQ,uX);
end;
{*************************************************************************}
procedure u1402Recall;
{
 recall 1402 registers;
}
begin
  uF := 27; uA := 0;
  camo(uN,uF,uA,uD,uQ,uX);
end;
{*************************************************************************}
procedure u1402Default( i : integer);
{
  Set 1402 channel to default settings
}

begin
  uPreAmp[i] := 1;
  uPostAmp[i] := 1;
  uOffset[i] := 2048;
  uFTYpe[i] := 1;
  uFPoles[i] := 0;
  uFRange[i] := 1;
  uFCO[i] := 200;
  uTraqBus[i] := 0;
  uCal[i] := FALSE;
```

```
  uRef[i] := 2048;
  uID     := 1402;
  for j := 1 to 4 do
    begin
    ueFRange[i,j] := 1;
    ueFCO[i,j] := 200;
    end;

  u1402AmpWrite(i,uPreAmp[i],uPostAmp[i],uOffset[i]);
  u1402ModeWrite(i,uFType[i],uFPoles[i],uTraqBus[i],uCal[i]);
  u1402CalWrite(i,uRef[i]);
  u1402CoeffWrite(i,uFRange[i],uFCO[i]);
  for j := 1 to 4 do u1402FCOWrite(i,j,ueFRange[i,j],ueFCO[i,j]);
  u1402IDWrite(uID);
end;
{*************************************************************************}
procedure u1402CfgShow;
{
 display 1402 configuration
}
var
  i,j : integer;

begin
pushwindow;
selectwindow(vPMain);
clrscr;
writeln('1402 CHANNEL CONFIGURATION : Module ID ',uID:6);
writeln;
write('A:PRE=',uPreAmp[0]:2,' POST=',uPostAmp[0]:3,' OFFSET=',uOffset[0]:4);
writeln(' CAL=',uCAL[0],' REF=',uRef[0]:4);
write(' POLES=',uFPoles[0]:1,' TYPE=',uFType[0]:1,' RANGE=',uFRange[0]:2,' FCO=',
uFCO[0]:3);
writeln(' TRAQ=',uTraqBus[0]:1);
writeln(' SECTION 1   SECTION 2   SECTION3  SECTION4');
for j := 1 to 4 do write('RANGE=',ueFRange[0,j]:1,' FCO=',ueFCO[0,j]:3,' ');
writeln;

writeln;
write('B:PRE=',uPreAmp[1]:2,' POST=',uPostAmp[1]:3,' OFFSET=',uOffset[1]:4);
writeln(' CAL=',uCAL[1],' REF=',uRef[1]:4);
write(' POLES=',uFPoles[1]:1,' TYPE=',uFType[1]:1,' RANGE=',uFRange[1]:2,' FCO=',
uFCO[1]:3);
writeln(' TRAQ=',uTraqBus[1]:1);
writeln(' SECTION 1   SECTION 2   SECTION3  SECTION4');
for j := 1 to 4 do write('RANGE=',ueFRange[0,j]:1,' FCO=',ueFCO[0,j]:3,' ');
popwindow;
end;
{*************************************************************************}
```

```
procedure u1402Show;
{show Configure 1402 Filter/Amp}

var
  i,j : integer;
begin
ErrorMsg[0] := chr(0);

for i := 0 to 1 do
  begin
  u1402AmpRead(i,uPreAmp[i],uPostAmp[i],uOffset[i]);
  u1402ModeRead(i,uFType[i],uFPoles[i],uTraqBus[i],uCal[i]);
  u1402CalRead(i,uRef[i]);
  u1402CoeffRead(i,uFRange[i],uFCO[i]);
  for j := 1 to 4 do u1402FCORead(i,j,ueFRange[i,j],ueFCO[i,j]);
  u1402IDRead(uID);
  end;
u1402CfgShow;
end;
{*************************************************************************}
procedure u1402FCOtoCode(Ftype : integer; Freq : real; stage : integer;
                         var dec,cutoff : integer);

var
  FCal  : real;
  range  : real;
  decade : real;
  mult   : real;
  fco    : integer;
  SFactor : array[1..4] of real;
  i : integer;

  begin
  case FType of
   0 : begin
       SFactor[1] := 2.1583;      {section 1 cutoff}
       SFactor[2] := 1.9260;
       SFactor[3] := 1.8066;
       SFactor[4] := 1.7537;
       end;

   1 : for i := 1 to 4 do SFactor[i] := 1.0;  {Butterworth 8 pole}
   else for i := 1 to 4 do SFactor[i] := 1.0 end;  {not yet done}

   FCal := 200*SFactor[Stage];
   range := 10;
   decade := -1;
   repeat
        range := range*10;
        decade := decade +1;
        mult := FCal*Freq / range;
{       writeln('mult:',mult:3,' range:',range:2,' decade:',decade:2);}
```

```
    until (Mult<255) or (decade>=3);
    if (mult>255) then mult := 255;
    fco := round(mult);
{   writeln(' F3dB:',Freq*Fcal/200:6,' Range :',round(decade):1,'  FCO:',fco:3);}
    dec := round(decade);
    cutoff := fco;
    end;

{*************************************************************************}
{*************************************************************************}
```

SCHEMATICS

ECO #1017

DSP Technology Inc.

SINGLE LEVEL BILL OF MATERIAL REPORT

Assembly: A-1402E-01 (ASSY: PCB, 1402E)
Revision: B
As of: 07/28/90

Date: 08/02/90

	Component	Description	Qty Per	As of	Until	Reference
1.	0100-0102	RES: RC07 1K OHM 5% 1/4W	6.00	06/08/87	12/31/99	R6,R7,R97,R103,R196 R209
2.	0100-0121	RES 5% 1/4W CC RESISTOR R=120	2.00	05/15/87	12/31/99	R2,R9
3.	0100-0132	RES 5% 1/4W CC RESISTOR R=1.3K	2.00	05/15/87	12/31/99	R1,R8
4.	0100-0241	RES 5% 1/4W CC RESISTOR R=240	8.00	06/30/88	12/31/99	R213, R214, R236 - R241
5.	0100-0472	RES 5% 1/4W CC RESISTOR R=4.7K	1.00	06/08/87	12/31/99	R3
6.	0100-0473	RES CF,5% 1/4W R=47K	2.00	05/15/87	12/31/99	R4,R5
7.	0150-0499	RMF RN55D 1% MF RES R=49.9	2.00	08/01/88	12/31/99	R91,R202
8.	0150-1002	RES 1% 1/4W MF RESISTOR R=10.0K	10.00	08/01/88	12/31/99	R98,R106,R185,R190,R224,R227,R84,R197,R83,R193
9.	0150-1004	RMF RN55D 1% METAL FILM RES R=1.00M	4.00	06/08/87	12/31/99	R100,R101,R194,R206
10.	0150-2002	RMF RN55D 1% R=20.0K	12.00	06/30/88	12/31/99	R96,R102,R107,R108,R188,R189,R195,R210,R222,R225,R228,R229
11.	0150-2490	RMF RN55D 1% METAL FILM RES R=249	4.00	06/08/87	12/31/99	R104,R192,R223,R226
12.	0150-3400	RES RN55D 1% R=340	2.00	08/01/88	12/31/99	R178,R183
13.	0150-4991	RMF RN55D 1% METAL FILM RES R=4.99	4.00	06/19/87	12/31/99	R85,R184,R217,R235
14.	0150-4992	RES: 1% 1/4W R=49.9K	2.00	06/30/88	12/31/99	R125,R187
15.	0151-1252	RES RMF RN55C 0.25% R=12.570K	4.00	06/30/88	12/31/99	R10,R66,R124,R179
16.	0151-1402	RES: RN55C 0.25% R=14.0K	2.00	06/30/88	12/31/99	R30,R144
17.	0151-1482	RES RMF RN55C 0.25% R=14.860K	2.00	06/18/87	12/31/99	R47,R159
18.	0151-1762	RES: RN55C 0.25% R=17.60K	2.00	06/30/88	12/31/99	R46,R160
19.	0151-1802	RES RMF RN55C 0.25% R=18.00K	16.00	05/20/87	12/31/99	R21,R23,R34,R39,R57 R59,R69,R74,R115 R120,R128,R133,R151 R156,R164,R169
20.	0151-1813	RES RMF RN55C 0.25% R=182.3K	16.00	05/20/87	12/31/99	R20,R25,R35,R38,R56 R61,R70,R73,R116 R119,R129,R132,R152 R155,R165,R168
21.	0151-2232	RES RMF RN55C 0.25% R=22.34K	2.00	06/08/87	12/31/99	R31,R143
22.	0151-2492	RES RN55C 24.9K OHM 1/8W .1%	16.00	08/01/89	12/31/99	R16,R17,R41,R42,R52,R53,R76,R77,R112,R113,R136,R137,R147, R148,R172,R173
23.	0151-3052	RES: RN55C 0.25% R=30.50K	2.00	06/30/88	12/31/99	R65,R180
24.	0151-6402	RES RMF RN55C 0.25% R=64.000K	2.00	06/08/87	12/31/99	R11,R123
25.	0152-1002	RMF: RN55C 0.1% R=10K	2.00	06/30/88	12/31/99	R89,R200
26.	0152-1003	RES: RN55C 0.1% R=100K	2.00	06/30/88	12/31/99	R88,R199
27.	0152-1621	RMF: RN55C 0.1% R=1.62K	16.00	06/30/88	12/31/99	R22,R24,R33,R40,R58 R60,R68,R75,R114 R121,R127,R134,R150 R157,R163,R170
28.	0152-1824	RMF: RN55C 0.1% R=1.82M	16.00	09/01/88	12/31/99	R19,R26,R36,R37,R55,R62,R71,R72 R117,R118,R130,R131,R153 R154,R166,R167
29.	0152-2502	RMF: RN55C 0.1% R=25K	16.00	09/01/88	12/31/99	R14,R27,R28,R45,R50,R63,R81,R82 R126,R139,R140,R149,R162,R175 R181,R182
30.	0152-9530	RES: RN55C 0.1% R=953 OHM	2.00	06/30/88	12/31/99	R90,R201
31.	0200-0511	RPK RES PK BNS 4308R-101-511	1.00	05/15/87	12/31/99	RP3
32.	0201-0102	RPK RES PK BNS 4310R-101-102	2.00	06/30/88	12/31/99	RP1,RP2
33.	0350-0104	RES VAR. 12T 1/4" TOP ADJ BOURNS 3	2.00	06/08/87	12/31/99	R220,R233
34.	0350-0501	RES VAR. 12T 1/4" TOP ADJ R=500 BO	8.00	06/08/87	12/31/99	R218,R219,R221,R230 R231,R232,R216,R234
35.	0500-0101	CSM C=100PF CDE # CD5FC101J03	8.00	08/01/88	12/31/99	C62,C67-C73
36.	0500-0151	CSM C=150PF 5% ARCO DM05-151J03	1.00	06/30/88	12/31/99	C3
37.	0500-0200	CSM C=20PF 5% ARCO DM05-200J03	14.00	07/20/90	12/31/99	C29,C53-C58,C60,C61,C63-C66,C78
38.	0520-0104	CMC 0.1UF CNTLB:CZ20A104M2 KEM:C322	42.00	06/30/88	12/31/99	C10,C11,C18-C20,C32,C33,C40-C42

	Component	Description	Qty Per	As of	Until	Reference

DSP Technology Inc.

SINGLE LEVEL BILL OF MATERIAL REPORT

Assembly: A-1402E-01 (ASSY: PCB, 1402E)

Revision: B

As of: 07/28/90

Date: 08/02/90

	Component	Description	Qty Per	As of	Until	Reference
39.	0521-0104	CMC C=0.1UF MONO CENTRALAB CZ20A104	8.00	06/30/88	12/31/99	C12,C15,C21,C24,C35,C38,C44,C47
40.	055422	RES: 1% 1/2W MF RESISTOR R=4.22K	2.00	08/01/88	12/31/99	R109,R191
41.	0600-0396	CTE TANT CAP C=39UF 10V KEMET T362B	1.00	05/15/87	12/31/99	C5
42.	0600-0685	CAP TANT 6.8UF 35V .250 LEAD SP	15.00	06/30/88	12/31/99	C1,C2,C4,C6-C8,C27,C28,C30,C31,C50-C52,C79,C80
43.	1000-4448	DGS DIODE SIL. SWITCH 1N4448	11.00	06/08/90	12/31/99	CR1,CR7,CR8,CR9A,CR9B,CR10A,CR10B,CR11A,CR11B,CR12A,CR12B
44.	1020-0759	ZENER, V=12.0 MOT 1N759	4.00	06/30/88	12/31/99	CR3-CR6
45.	1030-5624	DSR: DIODE RECT 3A GE 1N5624/BYM56	1.00	05/15/87	12/31/99	CR2
46.	1300-2907	TRP TRANSISTOR PNP SIL GP 2N2907	4.00	06/30/88	12/31/99	Q1 - Q4
47.	1750-0001	ICS SN7401	1.00	06/08/87	12/31/99	5A
48.	1760-0002	ICS SN74LS02	1.00	05/15/87	12/31/99	7A
49.	1760-0004	ICS SN74LS04	2.00	05/15/87	12/31/99	6A,3R
50.	1760-0139	ICS SN74LS139	1.00	05/15/87	12/31/99	4C
51.	1760-0221	ICS SN74LS221	1.00	05/15/87	12/31/99	4A
52.	1760-0279	ICS SN74LS279	1.00	05/15/87	12/31/99	5C
53.	1760-0374	ICS SN74LS374	2.00	05/15/87	12/31/99	3C,8C
54.	1760-0534	ICS SN74LS534	2.00	05/15/87	12/31/99	9A,9A
55.	1760-0642	ICS SN74LS642	2.00	05/15/87	12/31/99	10A,11A
56.	1851-0059	PRM: PROG/F 1850-0001, 1402-01 6C	1.00	06/19/87	12/31/99	6C
57.	1851-0072	PRM:1402 SVCS M/F 1850-0001	1.00	06/30/88	12/31/99	7C
58.	1857-0026	PAL: PROG/F 1856-0106, 1402-01 5B	1.00	06/19/87	12/31/99	5B
59.	1857-0027	PAL: PROG/F 1856-0100, 1402-01 6B	1.00	06/19/87	12/31/99	6B
60.	1857-0028	PAL: PROG/F 1856-0106, 1402-01 7B	1.00	06/19/87	12/31/99	7B
61.	1865-2210	ICD EEPROM XICOR X2210	3.00	05/15/87	12/31/99	8B-10B
62.	2000-0005	AMP: INSTRMNT, PMI AMP05EY	2.00	05/15/87	12/31/99	3N,10N
63.	2000-0084	ICA: OP AMP, TL084	2.00	06/30/88	12/31/99	5P,8P
64.	2000-4082	IC: OP AMP, MC34082	6.00	06/30/88	12/31/99	2D,10D,2F,11F,2K,11K
65.	2000-4084	IC: OP AMP, MC34084	8.00	06/30/88	12/31/99	3E,10E,3H,10H,3J,10J 3M,10M
66.	2010-0339	ICS QUAD COMPARATOR LM339	2.00	06/08/87	12/31/99	3Q,10Q
67.	2020-0003	VRF VOLT REF 10V PMI REF01CP	1.00	06/30/88	12/31/99	6P
68.	2030-0317	ICS IC VOL REG NAT LM317T	1.00	05/15/87	12/31/99	VR1
69.	2030-0337	IC: VOLT REG, NEG ADJ, LM337T	1.00	05/15/87	12/31/99	VR2
70.	2060-7528	DAC: CMOS, DUAL, 8BIT, AD7528JN	8.00	05/15/87	12/31/99	5E,8E,5H,8H,5J,8J,5M 8M
71.	2070-0202	AMX: ANLG MUX, DG202CJ	2.00	05/15/87	12/31/99	2C,10C
72.	2070-0509	AMX: DUAL, HI-3-509-5	8.00	06/30/88	12/31/99	1E,11E,1H,11H,1J,11J,1M,11M
73.	2070-0528	MUX: ANL,8CH SIL1CONIX DG528CJ	2.00	05/15/87	12/31/99	1A,3A
74.	2070-0529	MUX: DG529CJ	8.00	06/30/88	12/31/99	5F,8F,5G,8G,5K,8K,5L,8L
75.	2070-1307	AMX: 12S GSET, NAT LF13007	2.00	05/15/87	12/31/99	3D,9D
76.	2070-7512	ICS DUAL ANALOG SWTCH AD7512DIJ	2.00	06/30/88	12/31/99	3P,10P
77.	2070-7590	MUX: ANL,QUAD SPST AD7590DIKN	2.00	06/30/88	12/31/99	1N,12N
78.	3100-0302	FUSE 3AMP LITTLEFUSE 251003	3.00	05/15/87	12/31/99	F1-F3
79.	5000-0008	SKT CAMBION 703-1308-01-04-10	3.00	06/30/88	12/31/99	5M,8N,6P
80.	5000-0014	SKT CAMBION 703-1314-01-04-10	3.00	05/29/87	12/31/99	5A, 3P, 10P
81.	5000-0016	SKT CAMBION 703-1316-01-04-10	14.00	06/30/88	12/31/99	6C,7C,1E,11E,1H,11H,1J,11J,1M,11M,1N,5N,8N,12N
82.	5000-0018	SKT CAMBION 703-1318-01-04-10	15.00	06/30/88	12/31/99	1A,3A,8B-10B,5F,8F,5G,8G,5K,8K,5L,8L,3N,10N
83.	5000-0020	SKT CAMBION 703-1320-01-04-10	15.00	05/29/87	12/31/99	8A-11A,5B-7B,5E,8E 5H,8H,5J,8J,5M,8M
84.	5250-3703	JCK FUS CAMBION 450-3703-01-06-00	6.00	05/15/87	12/31/99	F1-F3

Component	Description	Qty Per	As of	Until	Reference

DSP Technology Inc.

SINGLE LEVEL BILL OF MATERIAL REPORT

Assembly: A-1402E-01 (ASSY: PCB, 1402E)
Revision: B
As of: 07/28/90

Date: 08/02/90

	Component	Description	Qty Per	As of	Until	Reference
85.	5500-0018	HDR 40 PIN R/A 4 WALL 3M#3595-5002	1.00	05/15/87	12/31/99	J1
86.	6520-7547	DAC: 12 BIT, AD7547JN	2.00	06/30/88	12/31/99	5N,8N
87.	6849-0002	INS BERGQUIST 3223-07-FR-54	2.00	05/15/87	12/31/99	VR1,VR2
88.	6850-0006	PNL: SPECIAL GUIDE RAIL	2.00	08/08/88	12/31/99	
89.	6852-0031	PNL REAR #1 DWG #2812-03-FD	1.00	05/15/87	12/31/99	
90.	7000-0056	PCB:1402-01 4L REV. B2	1.00	05/15/87	12/31/99	

Component Description Qty Per As of Until Reference

Assembly: A-1402E-02 (ASSY: FP MECH, 1402E)
Revision:
As of: 04/28/90

	Component	Description	Qty Per	As of
1.	1040-0001	DLE LED GREEN LITRONIX LDG1152	2.00	06/08/87
2.	1040-0002	DLE LED RED HP HLMP-1301	3.00	06/08/87
3.	5510-0001	CON RA 00.250 TEF+NUT & WASHER	2.00	05/04/87
4.	5510-0002	CON HOOD LEMO GCD00.020.LA	2.00	06/08/87
5.	5510-0007	NUT FOR LEMO 5510-0001 RA00.240	2.00	06/18/87
6.	5511-0001	CONN: PNL MT 2P LEMO ERA 0S 302 CNL	2.00	03/17/87
7.	5511-0004	HDW GND LUG 2P LEMO GCA 0S 255 LT	2.00	05/04/87
8.	6851-0083	PNL: FR, 1402E	1.00	06/30/88
9.	6852-0001	SCR:FT PNL JCK DEUTCH D7500M4B4	1.00	03/17/87

Component	Description	Qty Per	As of

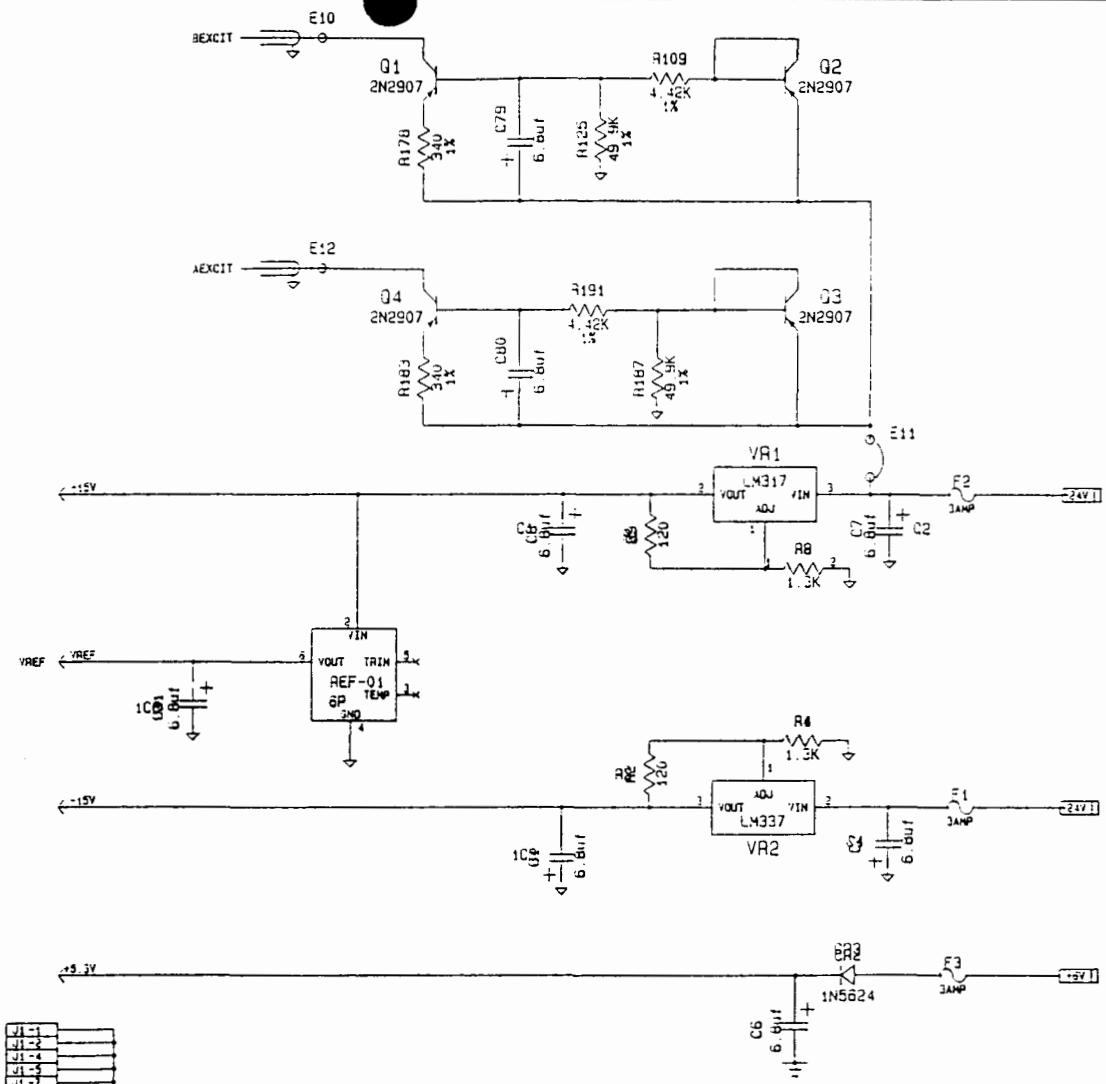
Assembly: A-1402E-02 (ASSY: FP MECH, 1402E)

Until	Reference
12/31/99	DS2,DS4
12/31/99	DS1,DS3,DS5
12/31/99	OUTPUT
12/31/99	OUTPUT
12/31/99	LOIS WANTS THESE
12/31/99	
12/31/99	INPUT
12/31/99	
12/31/99	

Until Reference

SYMBOLS:

- CAMAC EDGE CONNECTOR
- EXTERNAL CONNECTOR
- CONTINUE ON SAME SHEET
- CONTINUE ON DIFFERENT SHEET
- UNUSED PIN
- JUMPERS
- FRONT PANEL
- COMPONENT VALUE VARIES. SEE SHT 16 FOR APPROPRIATE VALUE WITH EACH MODEL OPTION



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL CAPACITORS ARE IN uf.
2. ALL RESISTORS ARE IN OHMS.
3. GROUNDS ARE AS FOLLOWS:
   - DIGITAL GROUND
   - ANOLOG GROUND
4. # NOT USED

REV	DESCRIPTION	DATE	APVD
	UP DATE SCH TO MATCH BOARD	3/3/88	
3	ECO 1005	4/89	
4	ECO 1007	5/11/94	
	2900 RELEASE		

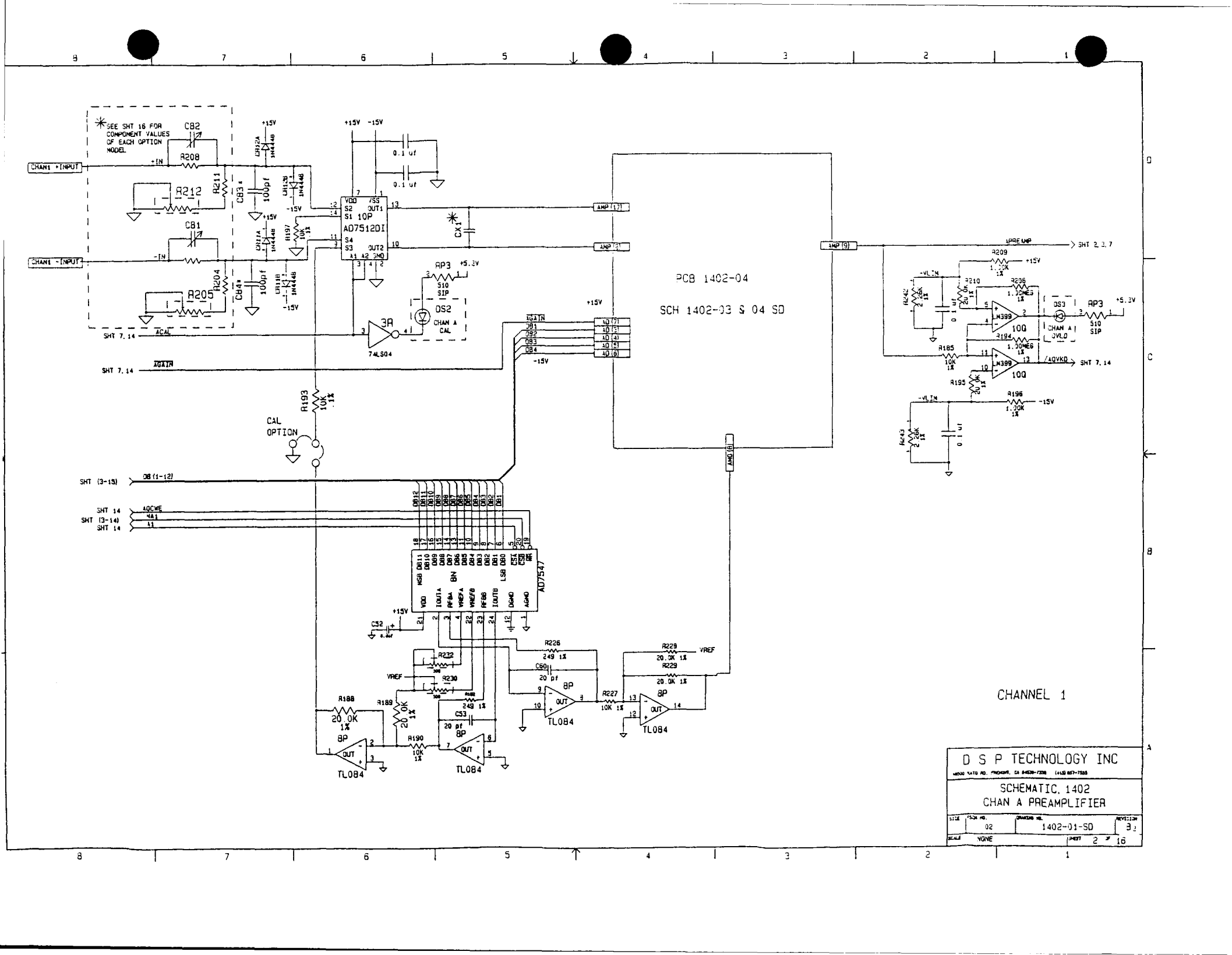
REVISIONS

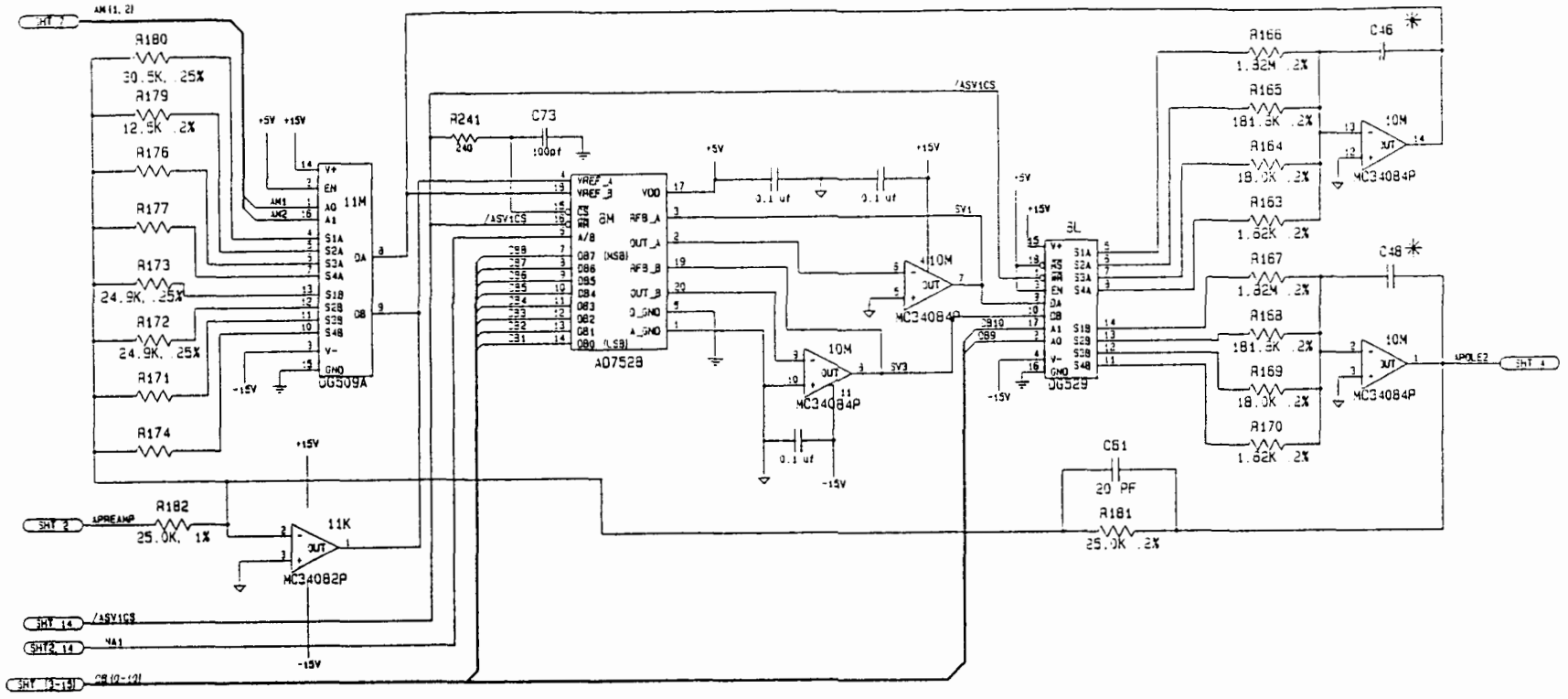
SIGNATURES	DATE
DRAWN	C.RUIGOMEZ
CHECKED	
APPROVED	
ISSUED	

D S P TECHNOLOGY INC

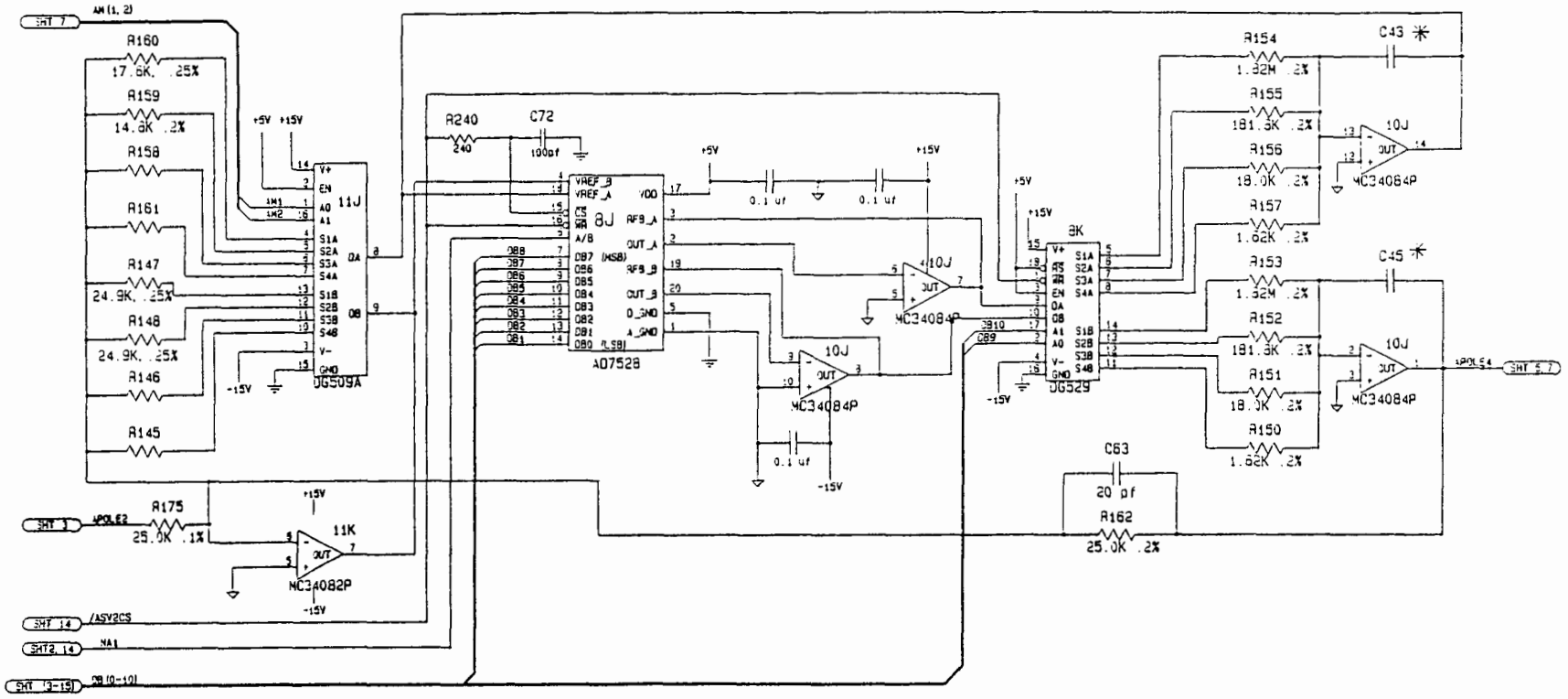
SCHEMATIC. 1402
VOLTAGE REGULATION

SIZE	TECH NO.	DRAWING NO.	REVISION
	01	1402-01-SO	B2
SCALE: NONE		SHEET 1 OF 16	


SEE SHT 16 FOR COMPONENT VALUES OF EACH OPTION MODEL
CHAN1 +INPUT
CHAN1 -INPUT
C82
C81
R208
R212
R211
R205
R204
C83
C84
100pf
+15V
-15V
0.1 uf
AD7512DI
R197
10K 1%
CX1
RP3
510 SIP
+5.3V
DS2
CHAN A CAL
3A
74LS04
SHT 7, 14
ACAL
AGAIN
DB1
DB2
DB3
DB4
R193
10K 1%
CAL OPTION
SHT (3-15)
DB (1-12)
SHT 14
AQCME
SHT (3-14)
A1
AD7547
C52
R232
R230
VREF
R226
249 1%
C60
20 pf
R229
20.0K 1%
R227
10K 1%
R188
20.0K 1%
R189
20.0K 1%
C53
R190
10K 1%
TL084
8P
AMP (7)
AMP (8)
AMP (9)
PCB 1402-04
SCH 1402-03 & 04 SD
PREAMP
SHT 2, 3, 7
R209
1.00K 1%
R210
20K 1%
R206
1.30ME3 1%
R194
1.30ME6 1%
R185
10K 1%
R195
20K 1%
R196
1.00K 1%
R243
2.26K 1%
M399
100
DS3
CHAN A OVLO
RP3
510 SIP
+5.3V
/AQVKD
SHT 7, 14
CHANNEL 1
D S P TECHNOLOGY INC
SCHEMATIC, 1402
CHAN A PREAMPLIFIER
02
1402-01-SD
B
SCALE NONE
SHEET 2 OF 16



O S P TECHNOLOGY INC			
SCHEMATIC, 1402			
STATE VARIABLE SECTION 1			
SIZE	FSCM NO.	DRAWING NO.	REVISION
	03	1402-01-SD	B2
SCALE NONE		SHEET 3 OF 25	

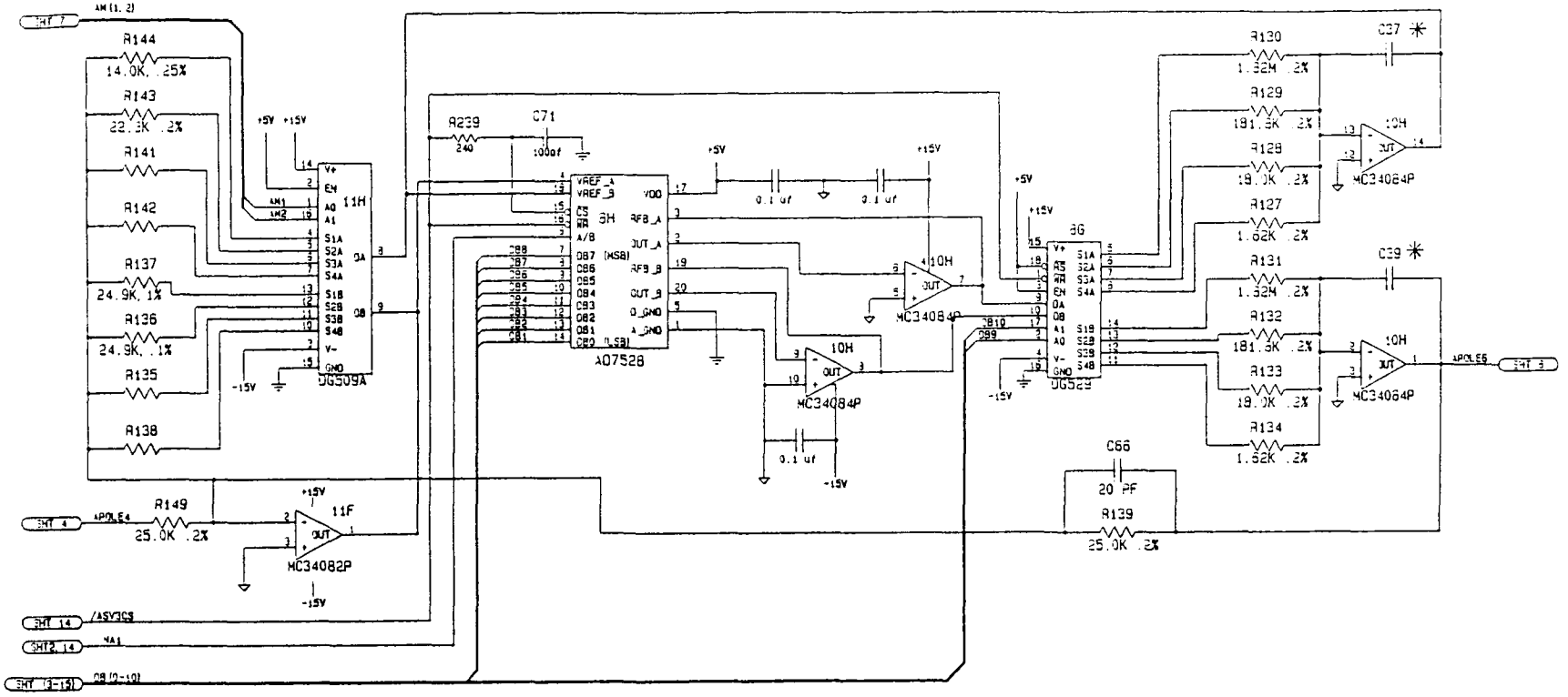


CHANNEL 1
SECTION 2

D S P TECHNOLOGY INC

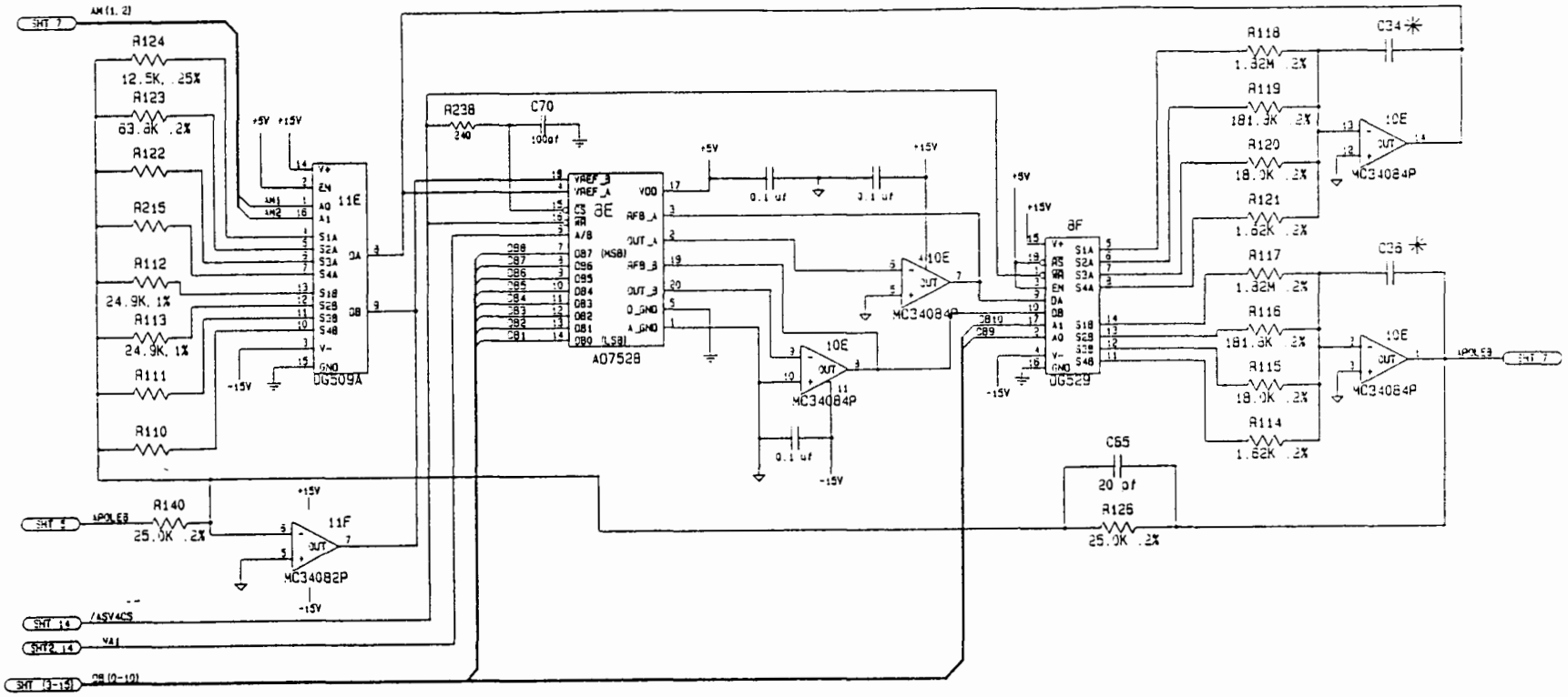
SCHEMATIC, 1402
STATE VARIABLE SECTION 2

SIZE	TECH NO.	DRAWING NO.	REVISION
	04	1402-01-SD	B 2
SCALE NONE		SHEET 4 OF 45	



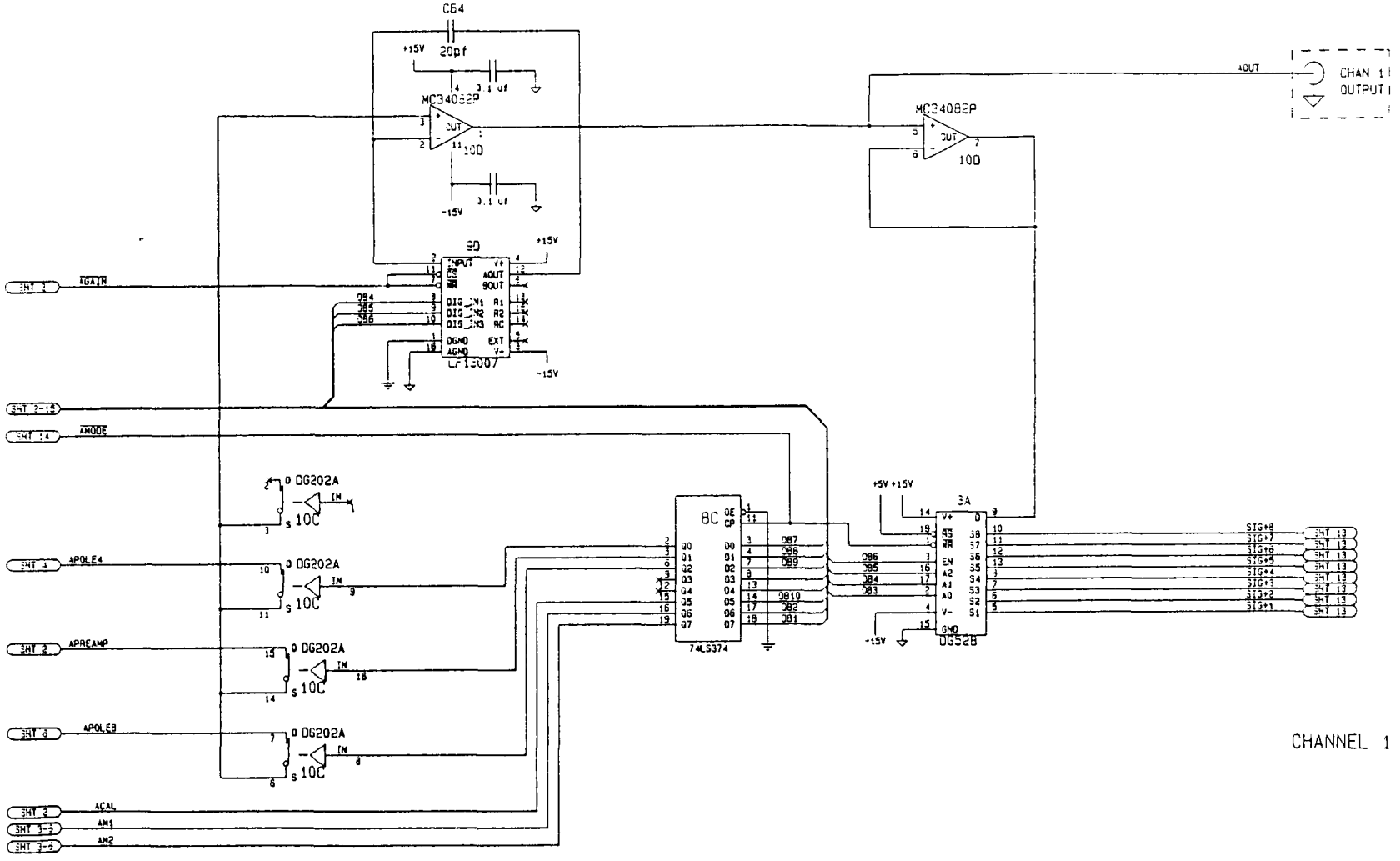
CHANNEL 1
SECTION 3

D S P TECHNOLOGY INC		
SCHEMATIC, 1402 STATE VARIABLE SECTION 3		
SIZE:	TECH NO. 05	DRAWING NO. 1402-01-SD
REVISION: B2		
SCALE: NONE	SHEET 3 OF 10	



CHANNEL 1
SECTION 4

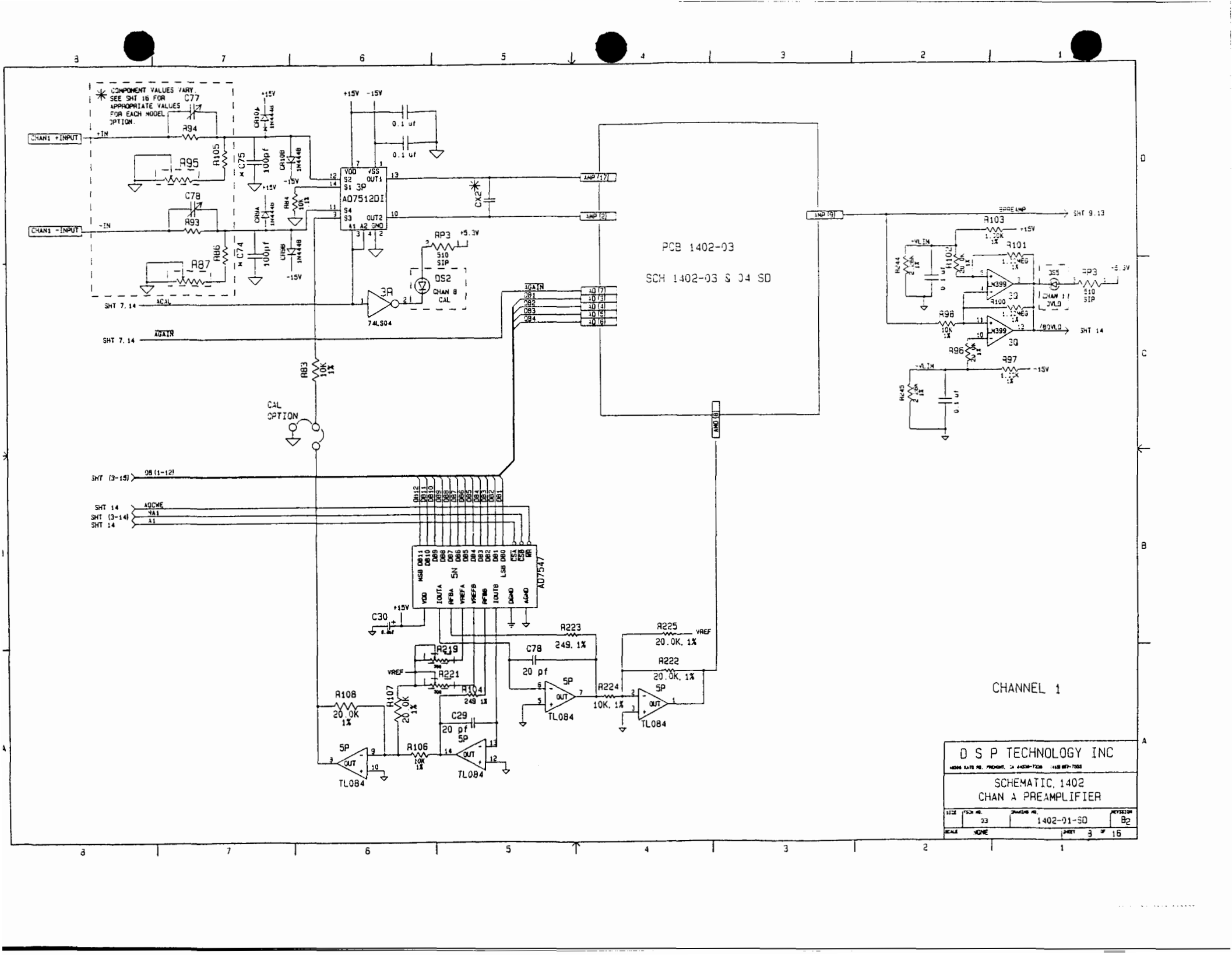
O S P TECHNOLOGY INC		
SCHEMATIC, 1402 STATE VARIABLE SECTION 4		
SIZE: D	TECH NO.: 06	DRAWING NO.: 1402-01-SD
SCALE: NONE	SHEET 5 OF 16	REVISION: B.2

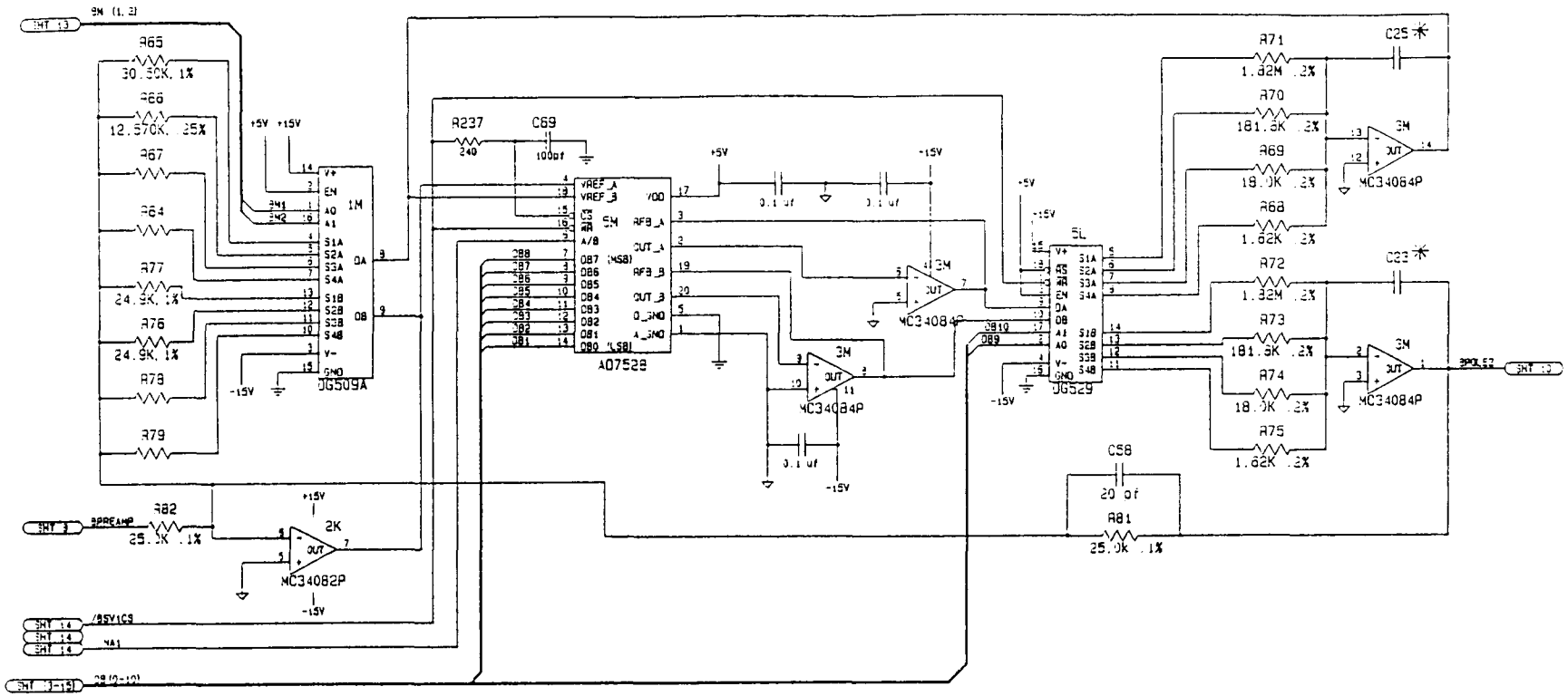


D S P TECHNOLOGY INC

SCHEMATIC, 1402
CHAN A POST AMPLIFIER

SIZE	FSCM NO.	DRAWING NO.	REVISION
	07	1402-01-SD	B2
SCALE NONE		SHEET 7 OF 16	


COMPONENT VALUES VARY. SEE SHT 16 FOR APPROPRIATE VALUES FOR EACH MODEL OPTION.
CHAN1 +INPUT
CHAN1 -INPUT
AD7512DI
74LS04
AD7547
TL084
LM399
PCB 1402-03
SCH 1402-03 & 04 SD
CAL OPTION
CHANNEL 1
D S P TECHNOLOGY INC
SCHEMATIC, 1402
CHAN A PREAMPLIFIER
1402-01-SD
B2

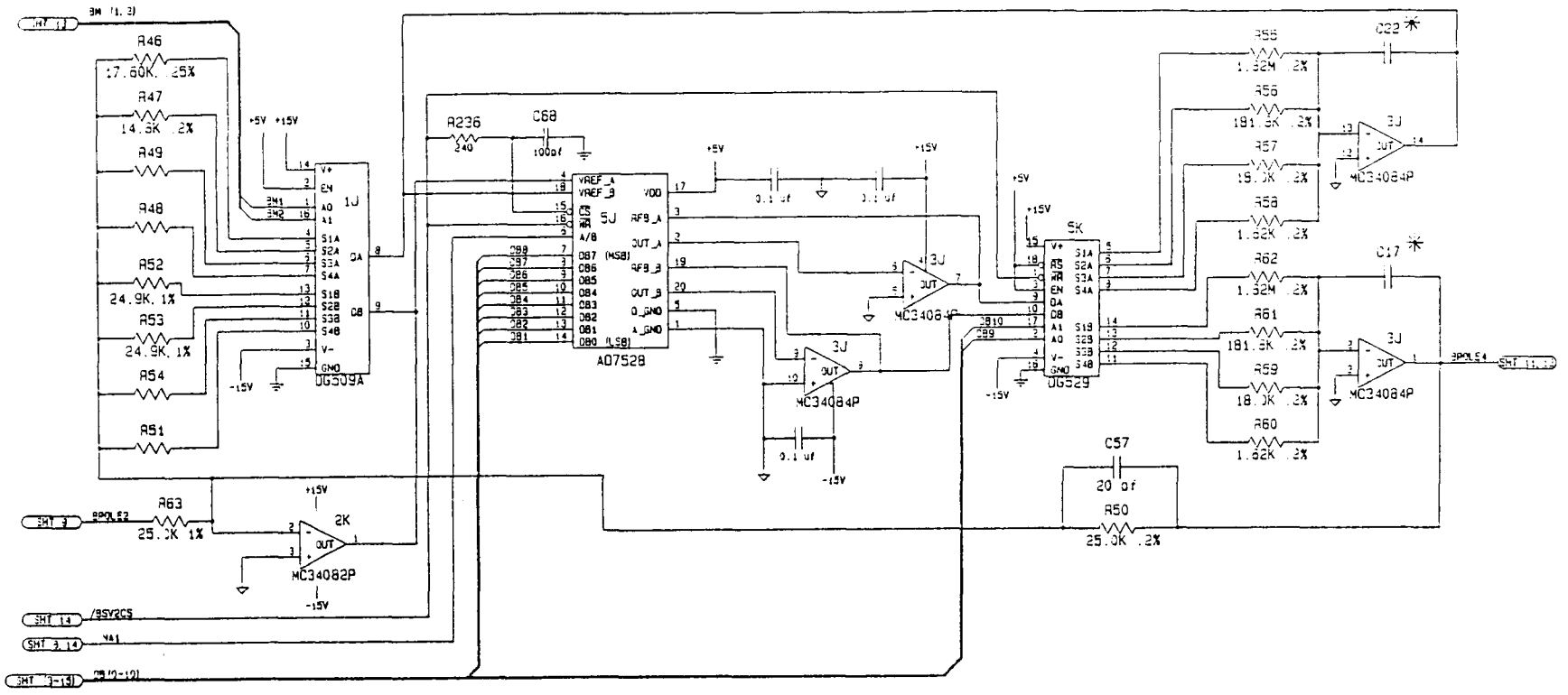


CHANNEL 2
SECTION 1

D S P TECHNOLOGY INC

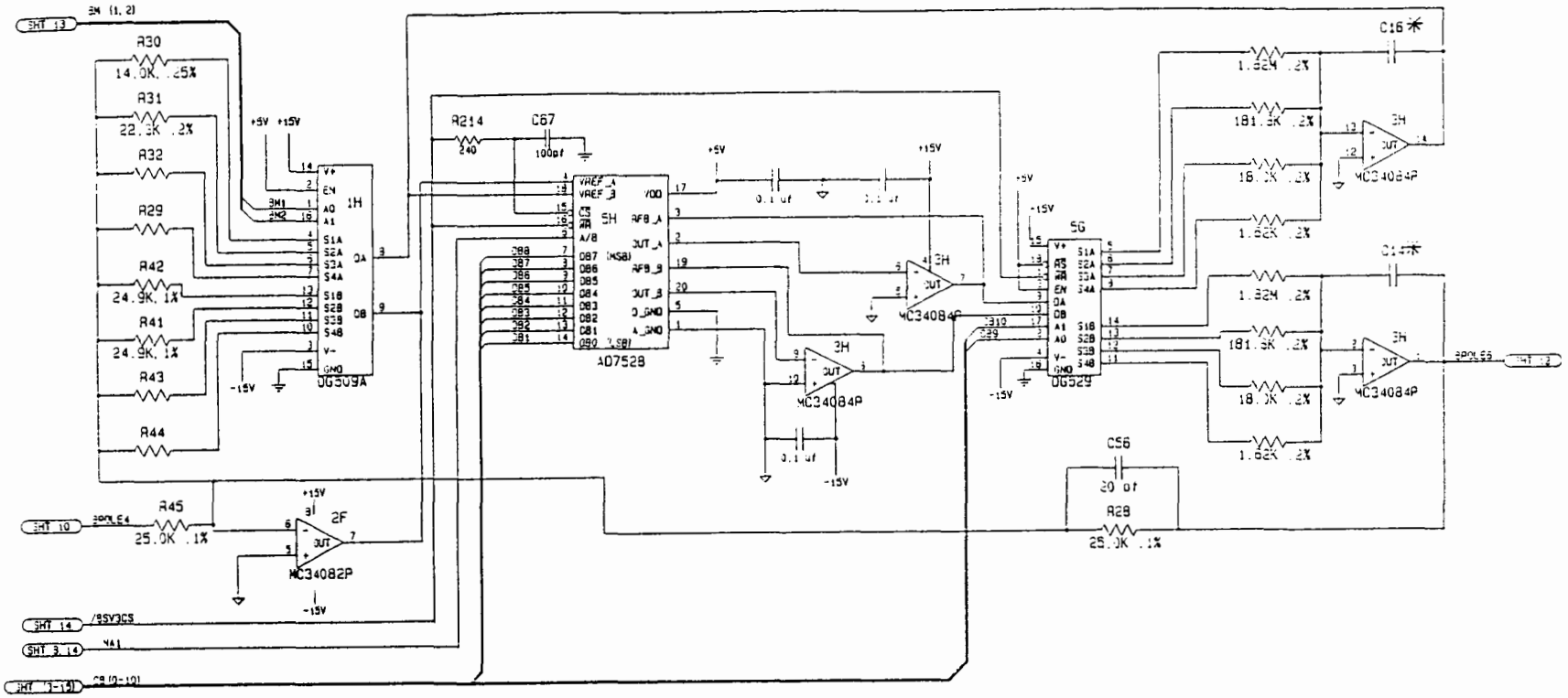
SCHEMATIC, 1402
STATE VARIABLE SECTION 1

SIZE	DRAWING NO.	REVISION
	09 1402-01-SD	B 2
SCALE NONE	SHEET 3 OF 16	



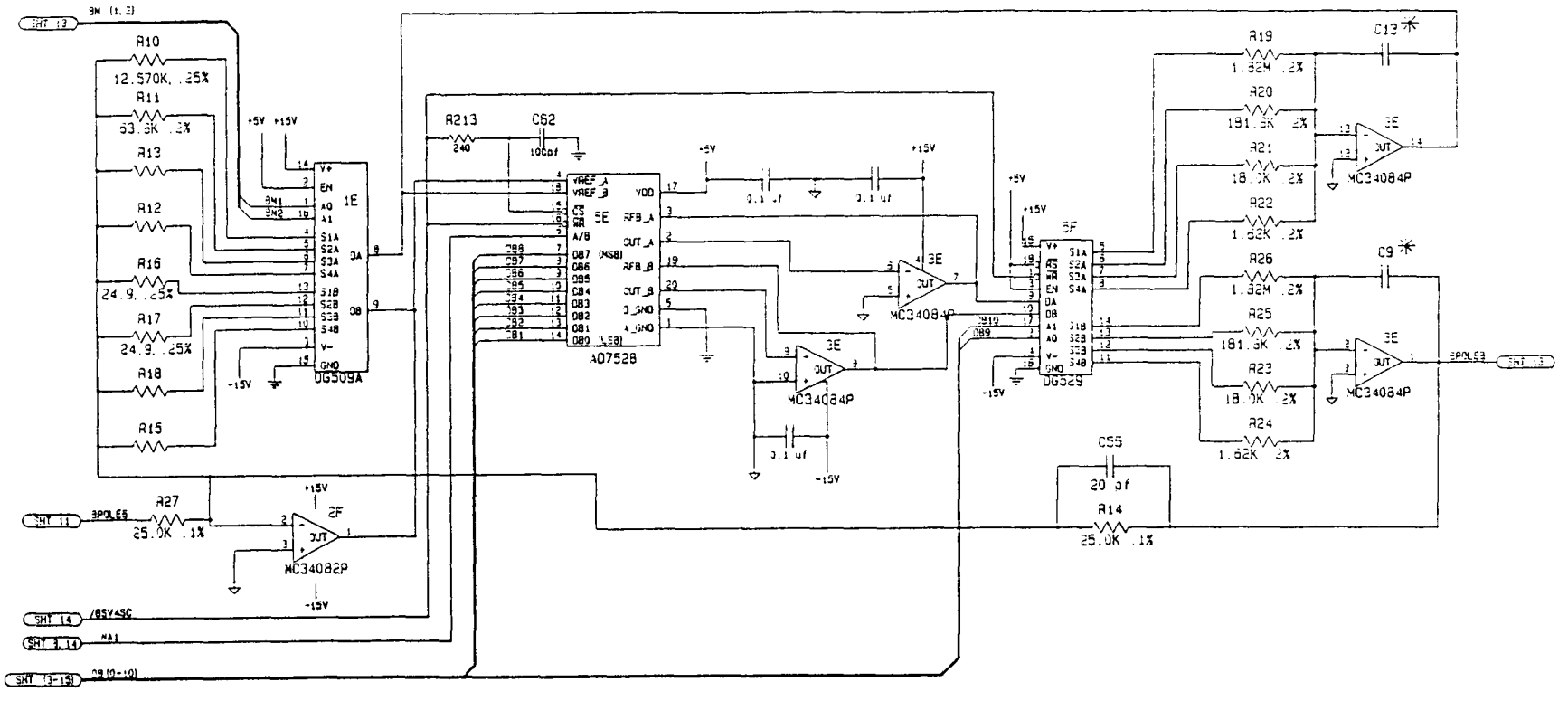
CHANNEL 2
SECTION 2

D S P TECHNOLOGY INC			
SCHEMATIC, 1402 STATE VARIABLE SECTION 2			
SIZE B	TECH NO. 10	DRAWING NO. 1402-01-SD	REVISION B2
SCALE NONE		SHEET 10 OF 16	



CHANNEL 2
SECTION 3

O S P TECHNOLOGY INC			
SCHEMATIC, 1402 STATE VARIABLE SECTION 3			
SIZE: B	TECH NO.: 11	DRAWING NO.: 1402-01-SD	REVISION: B2
SCALE: NONE		SHEET 11 OF 15	



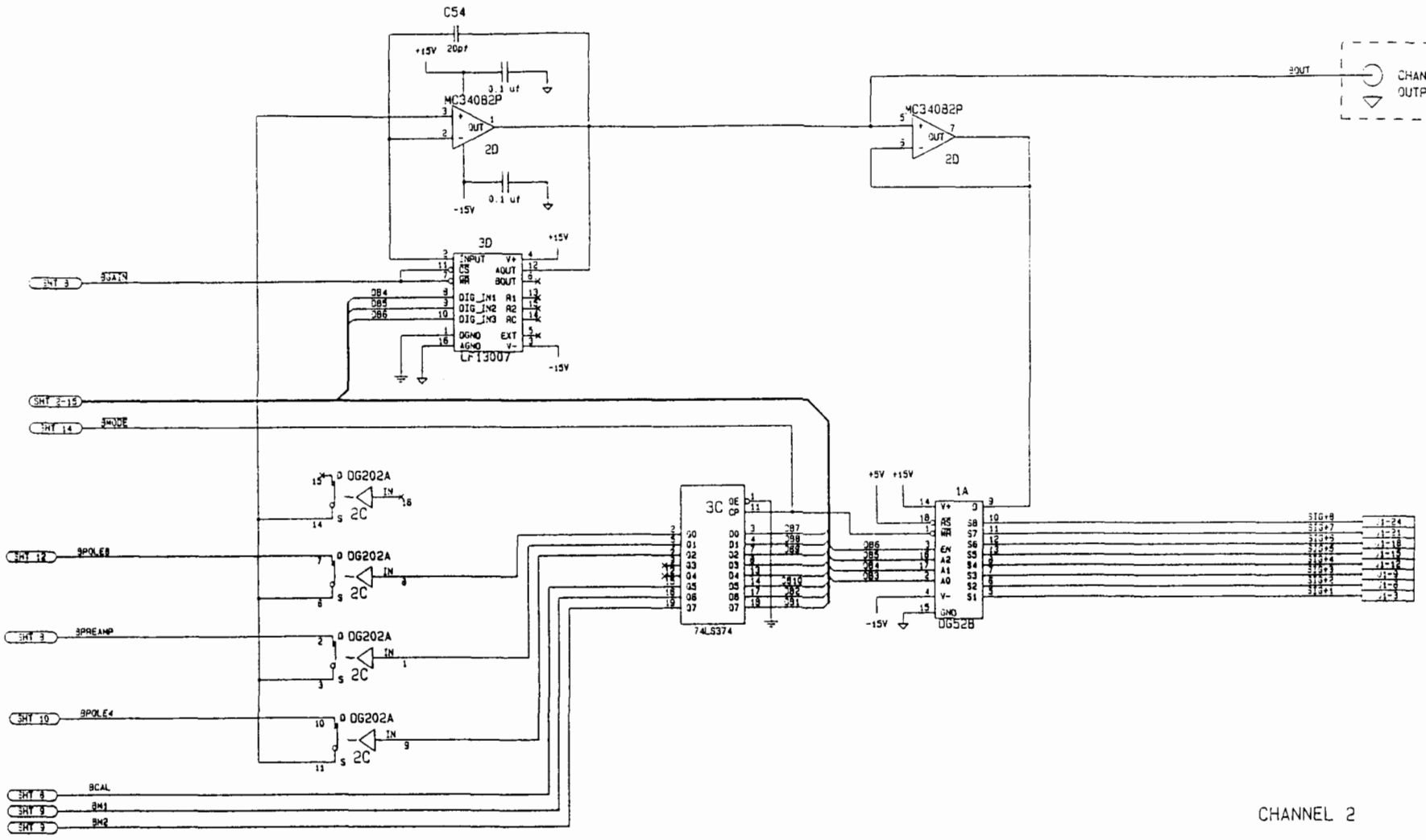
CHANNEL 2
SECTION 4

D S P TECHNOLOGY INC

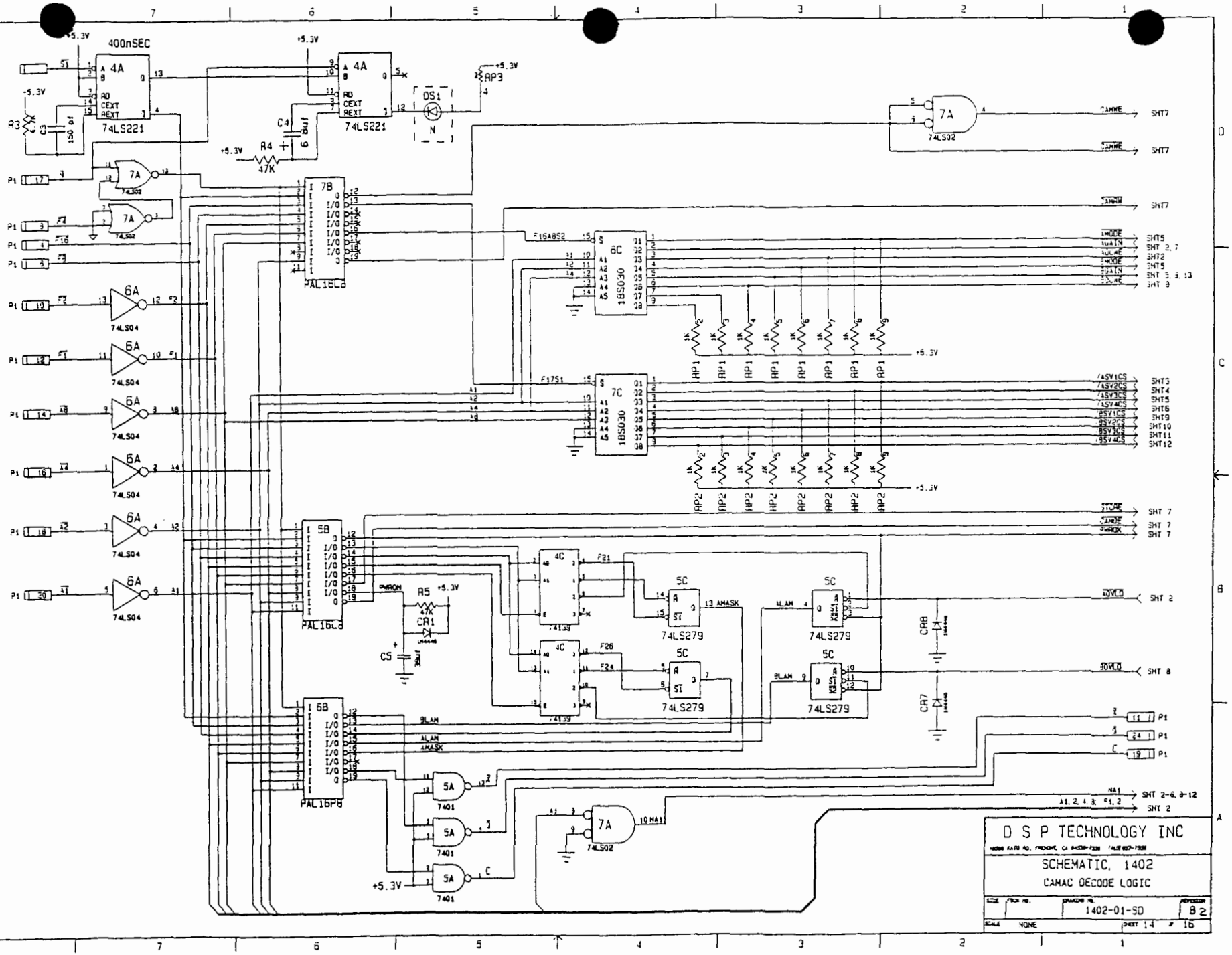
SCHEMATIC, 1402
STATE VARIABLE SECTION 4

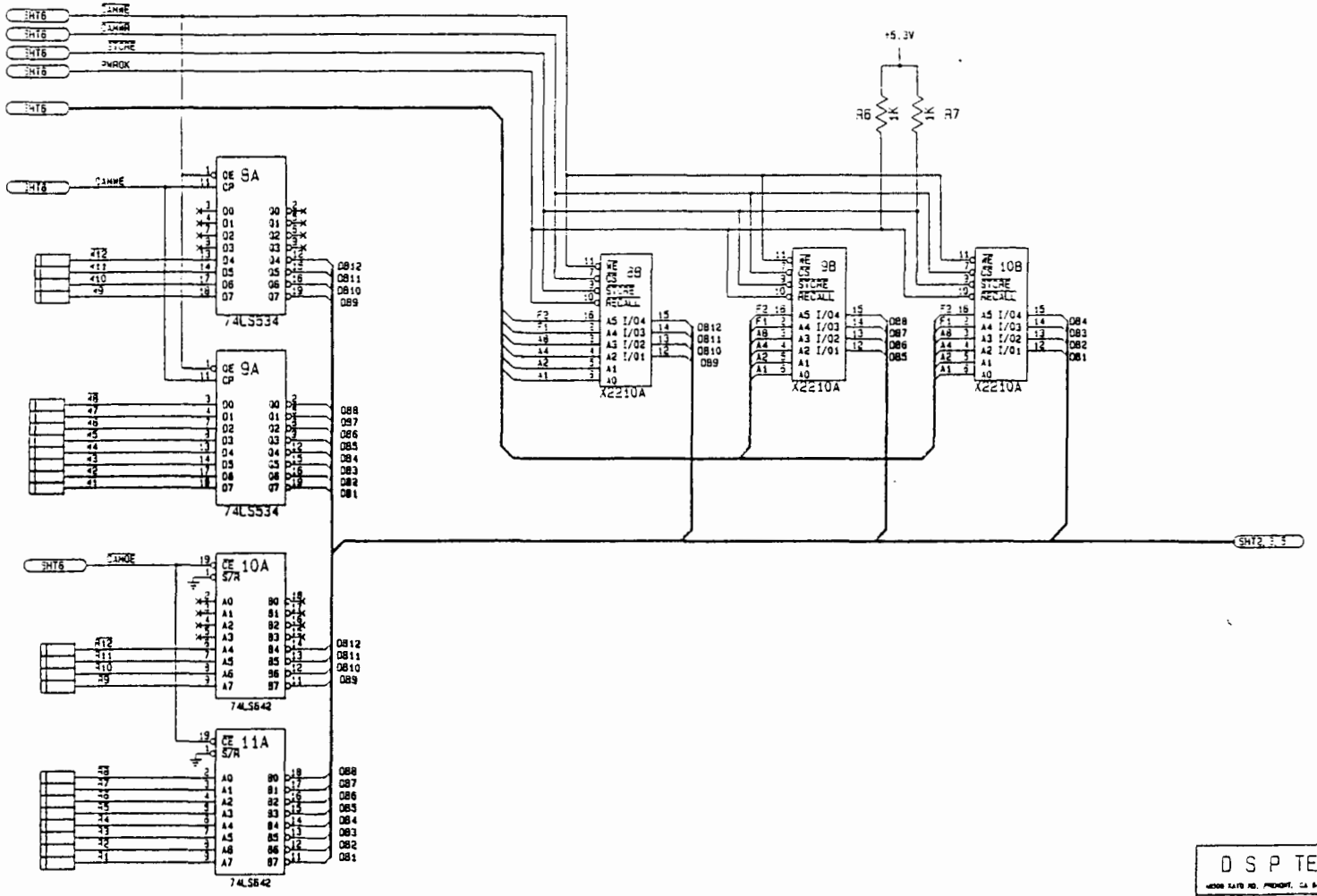
SIZE	TECH NO.	DRAWING NO.	REVISION
	12	1402-01-SD	B

SCALE NONE SHEET 12 OF 16



D S P TECHNOLOGY INC			
SCHEMATIC, 1402 CHAN B POST AMPLIFIER			
SIZE	FSCM NO.	DRAWING NO.	REVISION
	13	1402-01-SD	B_2
SCALE NONE		SHEET 13 OF 16	


400nSEC
74LS221
74LS04
74LS02
74LS279
74LS139
7401
PAL16L8
PAL16P8
18S030
D S P TECHNOLOGY INC
SCHEMATIC, 1402
CAMAC DECODE LOGIC
1402-01-SD
B 2
NONE
SHEET 14 OF 16



D S P TECHNOLOGY INC

SCHEMATIC, 1402
DATABUS

SIZE	FSCM NO.	DRAWING NO.	REVISION
		1402-01-SD	B2
SCALE NONE		SHEET 15 OF 16	

REVISIONS

COMPONENT	COMPONENT VALUES			
	OPTION GBL	OPTION GBH	OPTION ABH	OPTION ABL
R86	22	22	90.9K, 1%	90.9K, 1%
R87	NO LOAD	NO LOAD	20K VAR	20K VAR
R93	1.00K, 1%	1.00K, 1%	909K, 1%	909K, 1%
R94	1.00K, 1%	1.00K, 1%	909K, 1%	909K, 1%
R95	NO LOAD	NO LOAD	20K VAR	20K VAR
R105	22	22	90.9K, 1%	90.9K, 1%
R204	22	22	90.9K, 1%	90.9K, 1%
R205	NO LOAD	NO LOAD	20K VAR	20K VAR
R207	1.00K, 1%	1.00K, 1%	909K, 1%	909K, 1%
R208	1.00K, 1%	1.00K, 1%	909K, 1%	909K, 1%
R211	22	22	90.9K, 1%	90.9K, 1%
R212	NO LOAD	NO LOAD	20K VAR	20K VAR
CX1	100 pf	100 pf	27 pf	27 pf
CX2	100 pf	100 pf	27 pf	27 pf
C9	6800 pf	680 pf	680 pf	6800 pf
C13	" "	" "	" "	" "
C16	" "	" "	" "	" "
C17	" "	" "	" "	" "
C22	" "	" "	" "	" "
C23	" "	" "	" "	" "
C25	" "	" "	" "	" "
C34	" "	" "	" "	" "
C36	" "	" "	" "	" "
C37	" "	" "	" "	" "
C39	" "	" "	" "	" "
C43	" "	" "	" "	" "
C45	" "	" "	" "	" "
C46	" "	" "	" "	" "
C48	" "	" "	" "	" "
C77	NO LOAD	NO LOAD	5.5-18pf VAR	5.5-18pf VAR
C78	" "	" "	" "	" "
C81	" "	" "	" "	" "
C82	" "	" "	" "	" "

SIGNATURES		DATE
DESIGNED	J. CHURCH	5/2/90
DRAWN		
CHECKED		
APPROVED		
ISSUED		

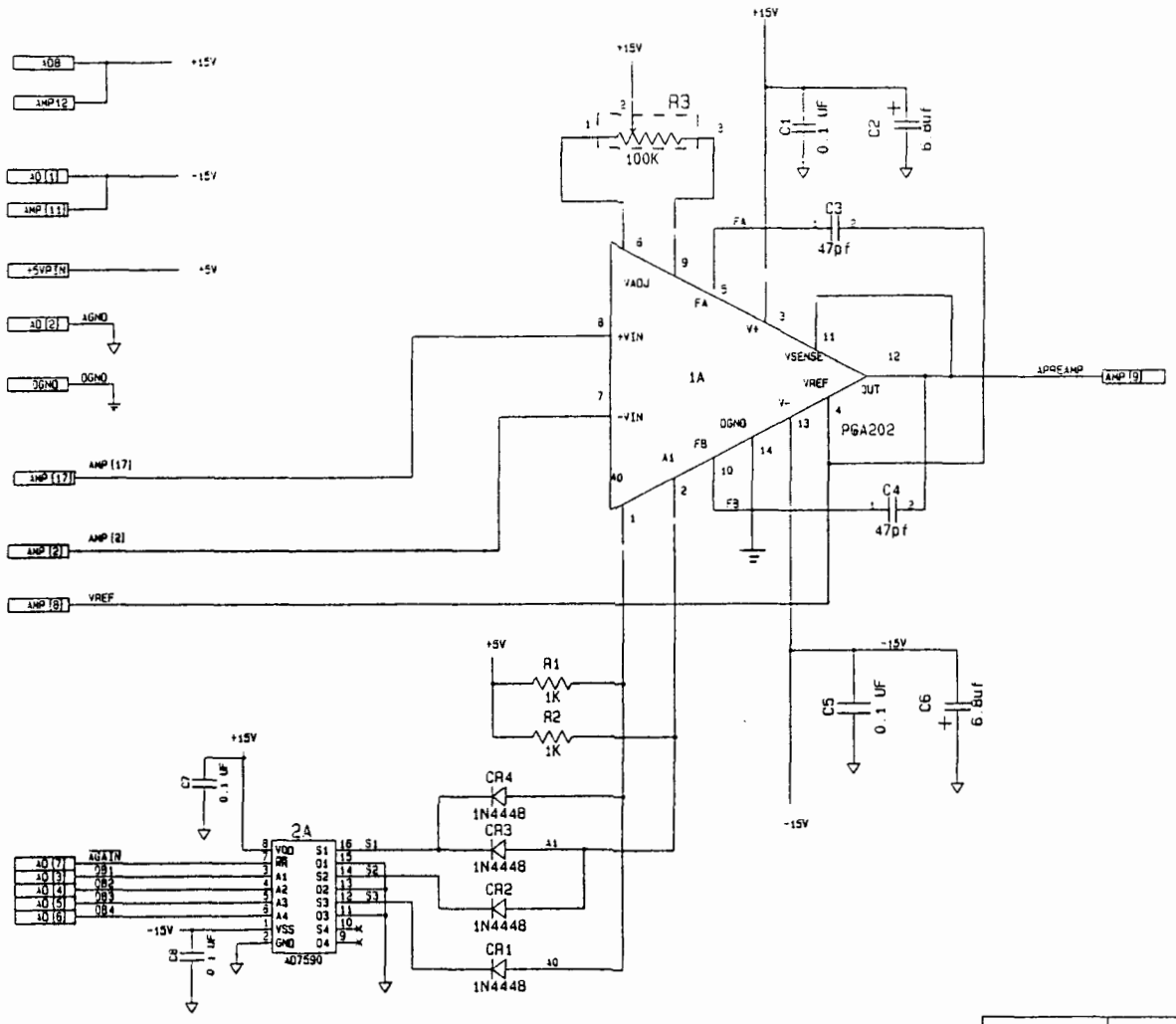
D S P TECHNOLOGY INC

SCHEMATIC 1402
OPTION COMPONENT VALUES

SIZE 8 | SCH NO. | DRAWING NO. 1402-01-SD | REVISION 82

SCALE NONE | SHEET 16 OF 16

P-CAD



SYMBOLS:

SINGLEPIN CONNECTOR

UNUSED PIN

1. ALL CAPACITORS ARE IN uf.
2. ALL RESISTORS ARE 1/4W 5% AND IN OHMS.

REVISIONS

REV	DESCRIPTION	BY	APVD	DATE

SIGNATURES	DATE
DESIGNED J. CHURCH	9/14/90
DRAWN	
CHECKED	
APPROVED	10/1/90
ISSUED	

D S P TECHNOLOGY INC

1402 PIGGYBACK

SIZE	DWG NO.	DRAWING NO.	REVISION
B	01	1402E-03-04	A

SCALE NONE SHEET 1 OF 1

REVISION HISTORY

DATE	BY	DESCRIPTION
06/03/87	Miller	Released
08/20/87	LeBrun	Revised specifications
11/15/87	Miller	Corrections to programming algorithm
11jul88	Miller	Added CAMAC COMMAND summary
10aug88	Miller	Preamp x1000 gain
		Filter FCO programming details
26Sep88	Miller	All registers MUST be initialized on powerup
		Added Appendix A:Program examples

WARRANTY

dsp Technology Inc.

PRODUCT WARRANTY

(Excludes Software)

DSP TECHNOLOGY ("DSP") warrants its products to be free from defects in material and workmanship and to meet DSP's performance specifications. The warranty period is one year from the date of shipment to the buyer. The warranty is limited by the paragraphs below.

RETURN TO FACTORY

If a buyer discovers a defect in a DSP product covered by this agreement, buyer's exclusive remedy is to ship the product back to DSP's Fremont factory, where DSP will, at its option, either repair or replace the product. This remedy applies if DSP receives the returned product on or before the tenth day after the expiration of the warranty period and the buyer notifies DSP of the defect before returning the product.

COST TO BUYER OF REPAIRS OR REPLACEMENT

Buyer must prepay freight charges to DSP. DSP will pay standard return freight to buyer. Buyer will be charged for premium freight if that method of transport is requested by buyer. There is no other charge for repair or replacement during the warranty period.

TRANSFERRABLE WARRANTIES

In addition to the foregoing warranty, DSP also provides the buyer the transferrable warranty, if any, provided to DSP by the manufacturers of other products such as terminals and disk systems supplied by SEC as part of a total system.

LIMITATION OF WARRANTY AND LIABILITY

The foregoing constitutes DSP's entire warranty, expressed, implied, and/or statutory (except as to title), and to any other party for any breach of such warranty and for damages, whether direct, special, incidental, or consequential. Other than as expressly provided in this document, no warranties expressed or implied, including any warranty of merchantability or fitness for a particular purpose are made. No employee, representative, or agent or seller has any authority expressed or implied to alter or supplement the terms of this warranty.

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