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CV8 Carrier Board
Technical Reference

Document Number 500-00355

Revision 1.02

April 1999

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Preface

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1 Introduction

1.1. Purpose of This Manual

This manual describes the features, architecture, and specifications of the CV8 Carrier Board. It will help you understand how the function libraries described in the *CV8 Carrier Board User Guide* operate within the board. You can also use this information to program the board at a driver level, extend the standard hardware functionality, or obtain more information to do custom configurations.

In addition to describing the function libraries, the *CV8 Carrier Board User Guide* shows you how to install and configure the board, as well as loading and running some of the sample code provided with the board.

1.2. References Documents

In addition to the CV8 Carrier Board Technical Reference and User Guide, you will also find the following documentation helpful.

- TIM-40 TMS320C4x Module Specification, Texas Instruments, Version 1.01.
- TMS320C4x Users Guide, 1996
- *SCV64 User Guide*, Tundra Semiconductor
- DSP~LINK3 Specification Revision 1.00

1.3. Definition of Key Terms

C4x	TMS320C40 or TMS320C44 Texas Instruments Digital Signal Processor
COMM Port	8-Bit parallel communication port on TMS320C40 and TMS320C44 DSPs. Used for communication between processors at up to 20 megabytes per second (50 MHz).
PEROM	Electrically erasable programmable read-only memory. Can be erased and reprogrammed in-circuit.
JTAG	Serial boundary-scan interface used to control test and on-chip emulation functions of DSPs.
XDS510	A JTAG interface for controlling the on-chip emulation functions of the TMS320C44.

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Global Shared Bus

A shared bus that all 4 CPU Nodes can gain Master control to read/write DSPLINK3 directly, and Far Global SRAM via the SCV64 Local Bus. CPU Node A can also access the SCV64 chip internal registers, and become VME64 bus master via the Global Shared Bus and SCV64 Local Bus.

SCV64 Local Bus

A shared bus that all 4 CPU Nodes, and a VME64 Master can become Master of to access the Far Global SRAM. CPU Node A can also access the SCV64 internal registers and become VME64 master via the SCV64 Local Bus.

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2 General Description

The CV8 Carrier Board is a TIM-40 carrier board for use within VME systems. The 6U VME board features four TIM-40 module sites. TIM-40 modules define a family of DSP modules, based on TMS320C4x processors, designed for use in multiple DSP systems. Spectrum offers a range of single and dual processor TIM-40 modules that can be used with the CV8 Carrier Board.

2.1. Features

- Flexible architecture consisting of four TMS320C4x-based processor nodes (nodes A, B, C, and D) provided by four TIM-40 sites
- Support for single or double width TIM-40 modules
- Up to 480 MFLOPS performance can be achieved using four dual-processor TIM-40 modules for a total of eight 60 MHz TMS320C4x processors
- Internal TMS320C4x communication port (COMM Port) connections between processor nodes
- VME64 interface with Master/Slave capability
- Ten COMM Ports from the processor nodes accessible on front panel connectors
- One on-board DSP~LINK3 module site
- One external DSP~LINK3 connector
- Serial port provided by a full duplex UART
- Non-intrusive multi-processor debugging in real-time using JTAG interface
- Up to 2M x 32-bit 1 wait-state SRAM shared between all processor nodes
- TIM-40 Application Specific Pins accessible on front panel and VME P2 connectors
- Three user-defined LEDs on the front panel

2.1.1. Scaleable Modular Architecture

With its four module sites that are compatible with Texas Instruments' TIM-40 specification, the CV8 Carrier Board can be configured with one to eight 'C4x DSPs. This results in an architecture that can be scaled from 60 to 480 MFLOPS of processing power with varying memory capacity. Modules can run independently from the host processor by booting from their own 32Kbyte PEROM. This also allows multi-processing operating systems to identify each module and its processing and memory capabilities when dynamically determining system configurations. A wide range of modules are available from Spectrum providing the flexibility of different memory and analog I/O combinations for each TIM-40 site. Single or double width TIM-40 module can be accommodated.

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2.1.2. VME64 Interface

The Master/Slave VME64 interface of the CV8 Carrier Board is implemented using the SCV64 interface chip providing typical rates of 44 MByte/s.

Slave A16/A24/A32 - D64/D32/D16/D08

Master A24/A32 - D64/D32/D16/D08 with Slot 1 controller capabilities.

2.1.3. TMS320C4x Communication Port Interfaces

The TMS320C4x communication ports (COMM Ports) are used for inter-processor communication both internally and externally to the CV8 Carrier Board. The COMM Ports provide bi-directional asynchronous communication between TMS320C4x processors at 20 Mbytes-per-second. They are ideal for passing large data sets between processors without loading any shared resource, such as the Far Global SRAM. All four nodes are connected to each other internally and there are 10 front panel COMM Port connections shared amongst the nodes.

2.1.4. Shared Memory Resources

The shared bus architecture allows the TIM-40 module sites and the VME host to access a shared bank of on-board SRAM. Three configurations of one wait-state 20 nanosecond SRAM are available:

- 512 KB (128K x 32-bit)
- 2 MB (512K x 32-bit)
- 8 MB (2M x 32-bit)

2.1.5. DSP~LINK3 Interface

DSP~LINK3 modules can be used with the CV8 Carrier Board via the DSP~LINK3 interface. The DSP~LINK3 module site allows Spectrum DSP~LINK3 modules to be installed right on the CV8 Carrier Board while the DSP~LINK3 ribbon cable connector allows external DSP~LINK3 boards to be connected to the CV8 Carrier Board. The CV8 Carrier Board is also available in a configuration with the DSP~LINK3 interface routed to the VME P2 connector on boards that do not have the PIC connector installed. The interface is directly accessible to all processors nodes.

Spectrum offers a range of boards and modules with DSP~LINK3 interfaces that can be used with the CV8 Carrier Board, including IndustryPack® modules.

The DSP~LINK3 interface is an open standard for Spectrum's I/O interface. It defines a 32-bit wide, 40 Mbyte-per-second I/O interface with low interrupt latency. The full DSP~LINK3 specifications are freely available from Spectrum. DSP~LINK3 is electrically compatible the DSP~LINK2 specification and can be used with DSP~LINK2 with the appropriate mechanical adapter available from Spectrum.

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2.1.6. JTAG Interface Debug Support

JTAG-based debugging uses the 'C4x's dedicated debug port to minimize the intrusiveness of the debugger on your application. Two JTAG interfaces for multiprocessor, C source debugging are supported on the CV8 Carrier Board:

- An XDS can be connected via the front panel JTAG connectors.
- C source debugging software can access the on-board Test Bus Controller (TBC) from the VME backplane.

Only one interface can be used at a time. A JTAG chain of up to two CV8 Carrier Boards can be connected together through the front panel JTAG connectors providing multiprocessor JTAG support for up to 16 processors. The first board in the JTAG chain must interface to either an XDS via its front panel JTAG IN connector, or to the debugging software accessing the TBC from the VME bus.

2.1.7. Serial Port Interface

A serial port is available on the front panel of the CV8 Carrier Board. It is driven by a 16C550 UART and is accessible from the Global Bus of TIM-40 site A.

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2.2. Board Layout

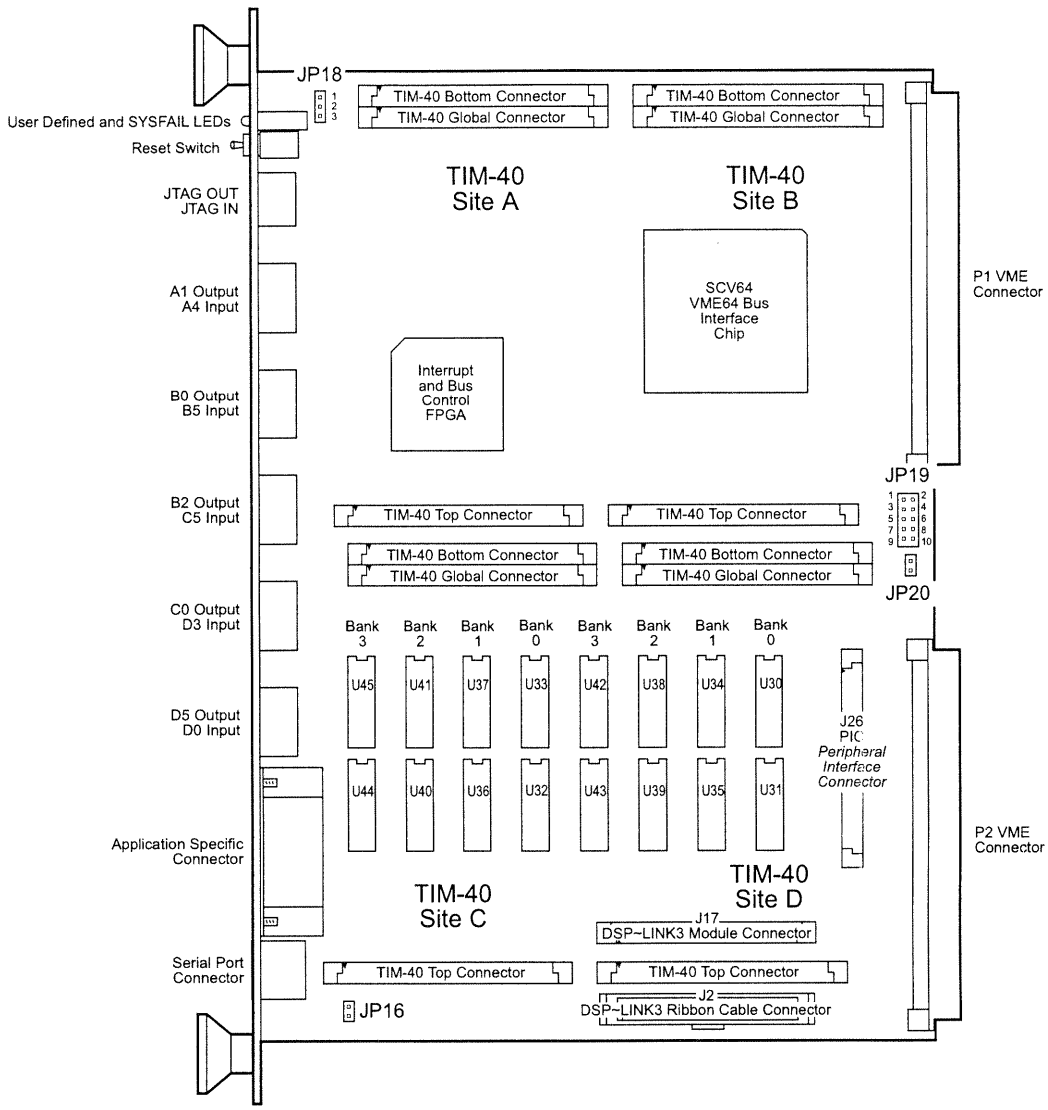


Figure 1 CV8 Connector and Jumper Locations

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Table 1 CV8 Jumper Summary

Jumper	Description	Pins	OUT	IN
JP16	DSP~LINK3 IRQ[0..3] to Node A	1-2	Disabled	Enabled*
JP19	VME Base Address A27	1-2	1	0*
(default address =	VME Base Address A28	3-4	1*	0
0x1000 0000)	VME Base Address A29	5-6	1	0*
	VME Base Address A30	7-8	1	0*
	VME Base Address A31	9-10	1	0*
JP20	Application Specific Interrupt	1-2	Disabled*	Enabled

*Default

2.3. Front Panel

The front panel has ten external C4x COMM Ports, an RS-232 UART port, JTAG IN and OUT interfaces, and an Application Specific Connector. There is also a reset switch, three user defined LEDs, and one VME SYSFAIL LED. See the following figure.

Reset Switch The front panel reset switch resets all TIM-40 Nodes, board logic and peripherals, including the SCV64 VME64 interface chip.

SYSFAIL LED The SYSFAIL LED is connected to the SCV64 /SYSFLED signal. The LED is lit when the /SYSFLED line is active (low). Refer to the SCV64 documentation for further information on its function.

User Defined LEDs Three LED indicators are user defined. They are controlled through Node A register accesses. User LED 1 flashes upon reset if the boot kernel supplied by Spectrum is used on Node A.

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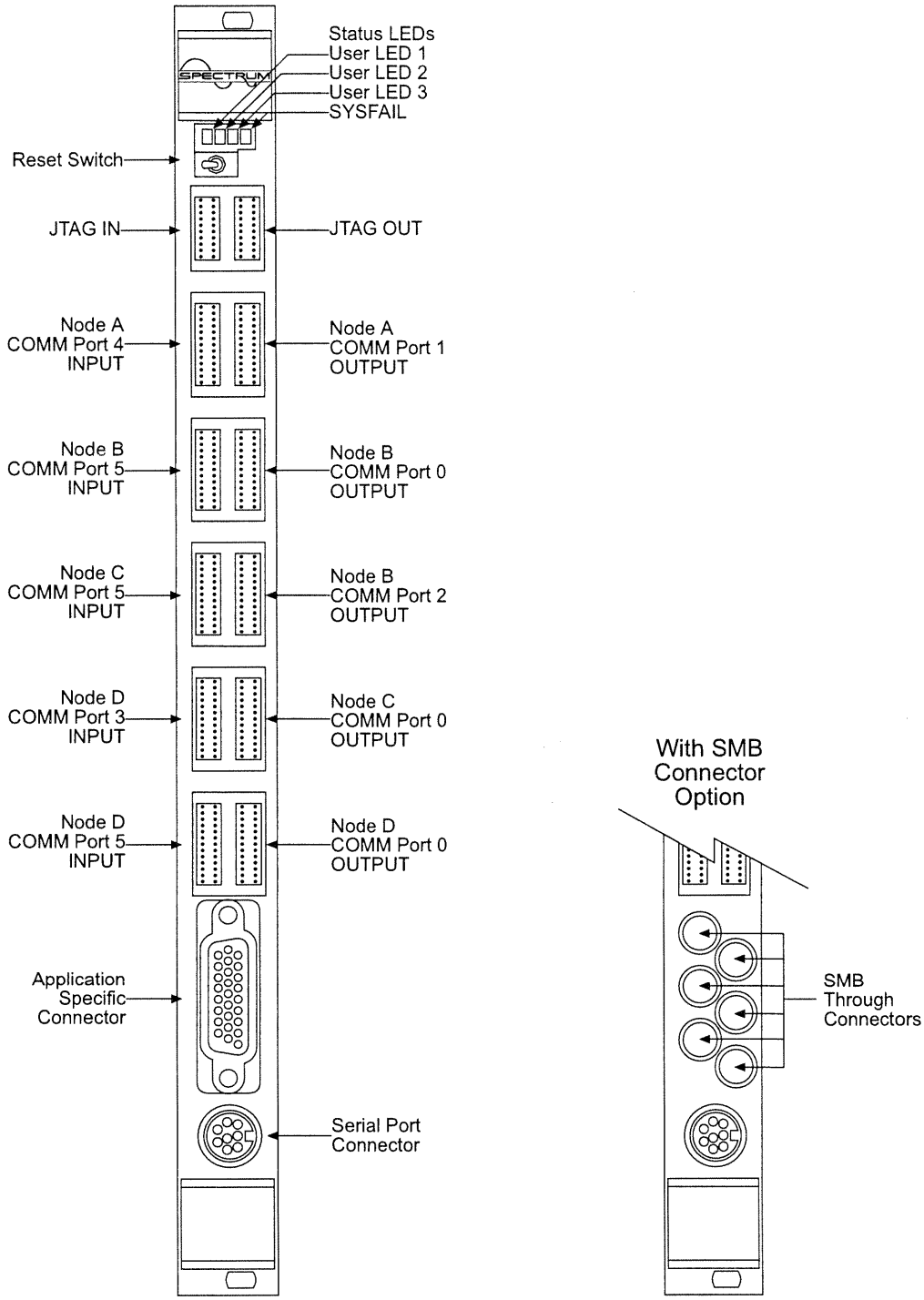


Figure 2 CV8 Front Panel

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2.4. Bus Architecture

Several different communication buses are used on the CV8 Carrier Board to connect the TIM-40 sites, memory devices, and interface circuitry as shown in the following diagram.

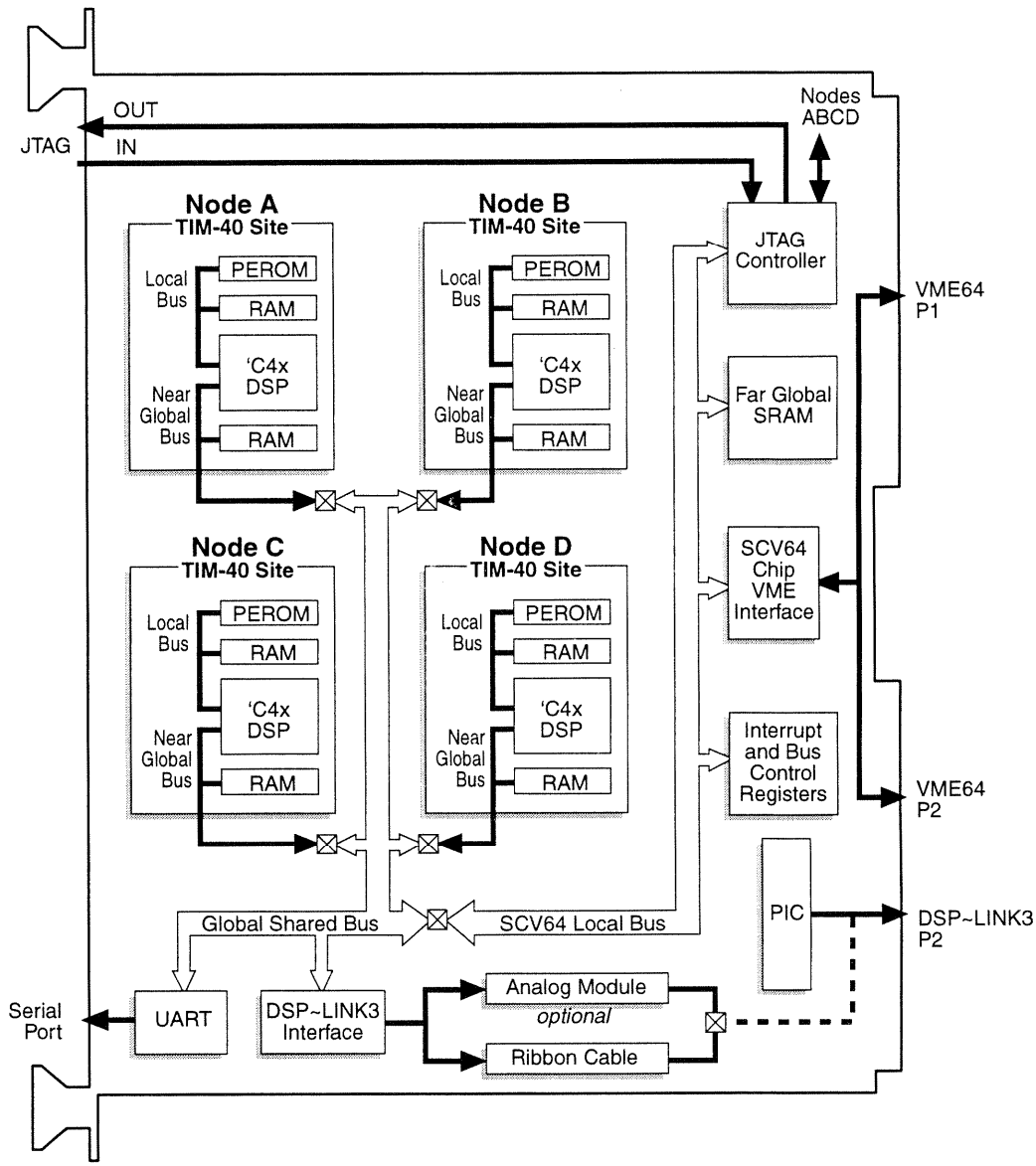


Figure 3 CV8 Block Diagram

Local Bus The Local Bus address range is specific to a single 'C4x DSP, and is therefore not shared with other processors or nodes. It is a private memory bus of a particular 'C4x.

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Near Global Bus

The Near Global Bus refers to the Global Bus of each TIM-40 site. The SRAM located on 'C44 Global Bus is one wait state. The Near Global Bus SRAM of a node cannot be accessed by the DSPs of any other nodes.

Global Shared Bus

The Global Shared Bus interconnects the:

- Buffered Global Buses of each TIM-40 site via the Global Connectors
- DSP~LINK3 Interface
- Serial port UART
- Interface between the SCV64 Local Bus and the Global Shared Bus

SCV64 Local Bus

The SCV64 Local Bus of the SCV64 chip is connected to the

- Global Shared Bus interface buffer for Node A access
- Far Global SRAM
- Registers for the Interrupt Controller and Bus Arbitration
- JTAG Controller

2.5. 'C4x Communication Port Architecture

There are ten COMM port connections provided to the front panel of the CV8 board. As well, there is full interconnections between all four C4x based TIM-40 modules such that any C4x may directly communicate with any other module on board.

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Routing of the 'C4x COMM ports to the 10 external COMM port connectors is shown in the following diagram. Arrows indicate the default port direction after the board is initialized.

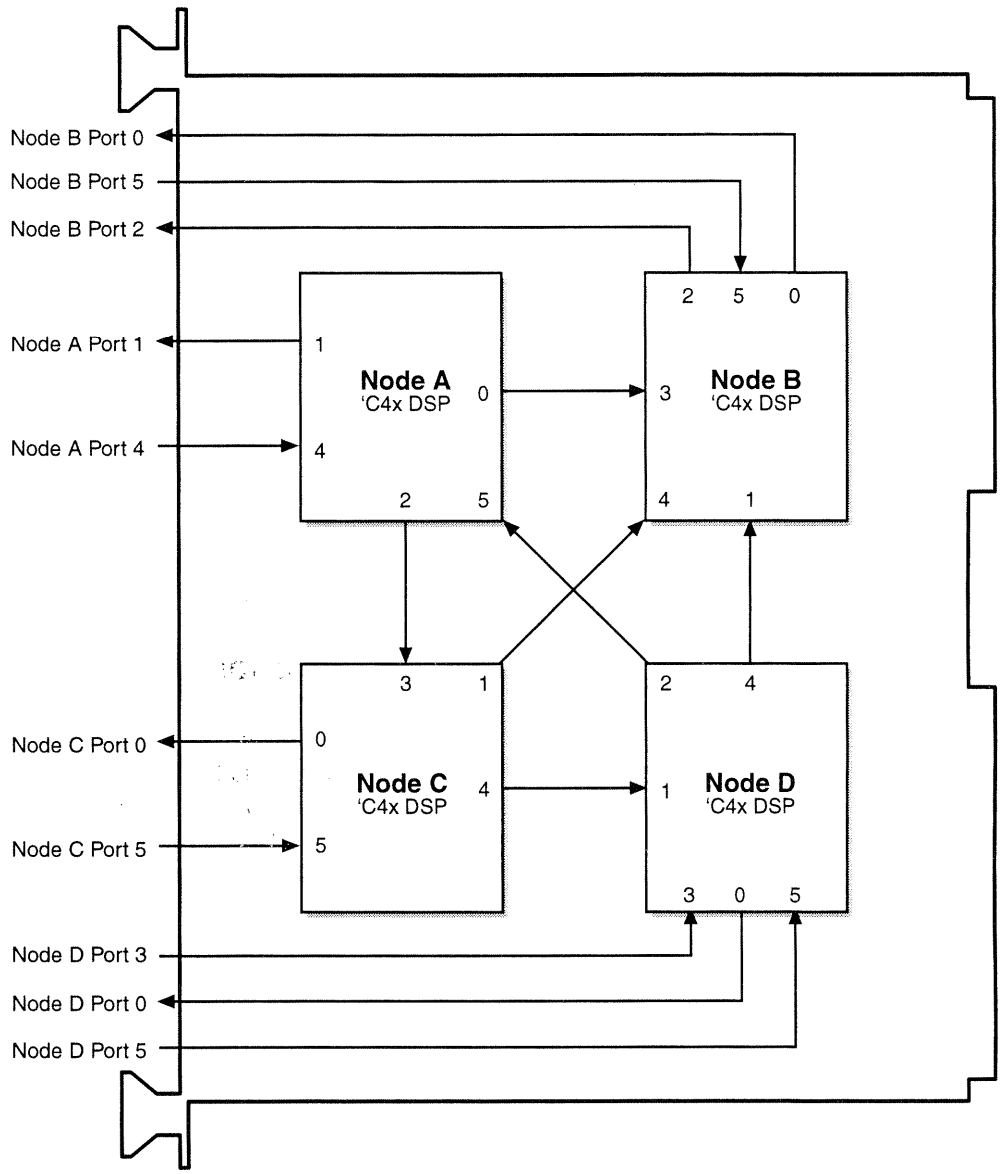


Figure 4 CV8 COMM Port Architecture

TIM-40 sites A and C only route 5 of their 6 available COMM Port connections. COMM Port 3 from site A and COMM Port 2 from site C are not routed.

2.6. Resetting the CV8 Carrier Board

The CV8 Carrier Board is reset upon system power up. Hardware components on the board can also be reset via a front panel reset switch, host software on the VME bus, and

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via JTAG. The following table shows the CV8 Carrier Board hardware is initialized by each type of reset.

Table 2 Reset Summary

CV8 Carrier Board Hardware Reset	Power Up	RST Switch	VME Host Software	JTAG IN
All TIM-40 sites	✓	✓	✓	✓
DSP~LINK3 slave devices	✓	✓	✓	✓
VME bus Interface	✓	✓		
Serial port 16C550 UART	✓	✓		✓
LED*x* registers	✓	✓	✓	
VCONTROL register	✓	✓	✓	
Round Robin Time-Slot register	✓	✓	✓	
Host Interrupt Clear register	✓	✓	✓	
JTAG /GRESET line	✓	✓	✓	✓

When the processor nodes are reset with any of the above methods, the 'C4x processor IIOF lines are tristated so that each 'C4x can read its boot mode selection jumpers. To enable its IIOF signals a 'C4x must then execute an IACK cycle.

2.6.1. Power Up Reset

The VME bus /SYSRST signal resets all CV8 Carrier Board hardware when it is asserted.

The CV8 Carrier Board is held in reset for approximately 250 milliseconds after power on for on board initialization. Once this is complete, the on board reset logic is released.

2.6.2. Reset Switch

The Reset switch on the front panel asserts the /EXTRST line of the SCV64 chip when activated.

2.6.3. VME Host Reset

Any VME master on the VME64bus can reset the CV8 Carrier Board using the using the *VME64 Slave Reset* register at offset address 0300 0000h from the board's VME base address. The following CV8 Carrier Board devices and resources are reset:

- All TIM-40 sites
- LED*x* registers
- VCONTROL register

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- Round Robin Time-Slot register
- Host Interrupt Clear register
- JTAG /GRESET line

Once a reset has been asserted, the CV8 Carrier Board is held in reset until it is released from reset through this register.

- To reset the CV8 Carrier Board, a host on the VME64 bus writes a "1" to bit D0 of this register.
- To release the CV8 Carrier Board from reset, a host on the VME64 bus writes a "0" to bit D0 of this register.
- To determine whether the CV8 Carrier Board is being held in reset, a host on the VME64 bus reads the state of bit D0. If bit D0 is set to "1", then the CV8 Carrier Board is being held in reset.

2.6.4. JTAG Reset

Setting the /GRESET input of the JTAG IN connector (J10 pin 20) to 0 volts resets

- All processor nodes
- JTAG Out
- The Test Bus Controller (TBC)
- Support logic

The tri-state /GRESET lines are buffered and can be connected across many CV8 Carrier Board board through JTAG cables. Multiple CV8 Carrier Boards can be simultaneously reset this way when the /GRESET line is asserted. This prevents damage due to COMM Port direction contention on CV8 Carrier Boards that are connected together via their COMM Ports.

Note: Only the /GRESET line is buffered; the other JTAG lines are not buffered. As a result, only the /GRESET line will function properly across more than two boards connected by JTAG cables.

To resume normal operation, the /GRESET signal must be tristated by an external driver. Pull up resistors on the board can then place the line at 5 volts.

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3 Installation

This section provides a brief description of how to configure and install the CV8 Carrier Board into a computer. Refer to the *CV8 Carrier Board User Guide* for further information on installing, configuring, debugging, and running CV8 Carrier Board software.



Caution: Before handling the CV8 Carrier Board or a module, ensure that you and the components are properly grounded to prevent damage from electrostatic discharge.

3.1. System Requirements

- VME or VME64 system with an available 6U slot
- A TIM-40 'C4x processor module installed in node A to provide an H1 clock source to the CV8 Carrier Board
- Texas Instruments' Floating point development tool software (compiler and debugger)

3.2. Configuring the CV8 Carrier Board

Configure the on board jumpers to suit your application. Refer to the *Board Layout* section in the *General Description* chapter for information on the jumper settings.

3.3. Installing TIM-40 Modules on the Board

Your CV8 Carrier Board may already contain TIM-40 modules. If it doesn't, or you are adding modules to it, follow the these instructions to install them on the CV8 Carrier Board.

Note: If you are installing TIM-40 modules in sites C or D, you will not be able to install a DSP~LINK3 module on to the board, unless it is through the DSP~LINK3 ribbon cable connector. If you are installing a module in site D you will also not be able to use the PIC connector.

The following figure shows the location of the modules on the CV8 Carrier Board and the mounting hardware for the sites.

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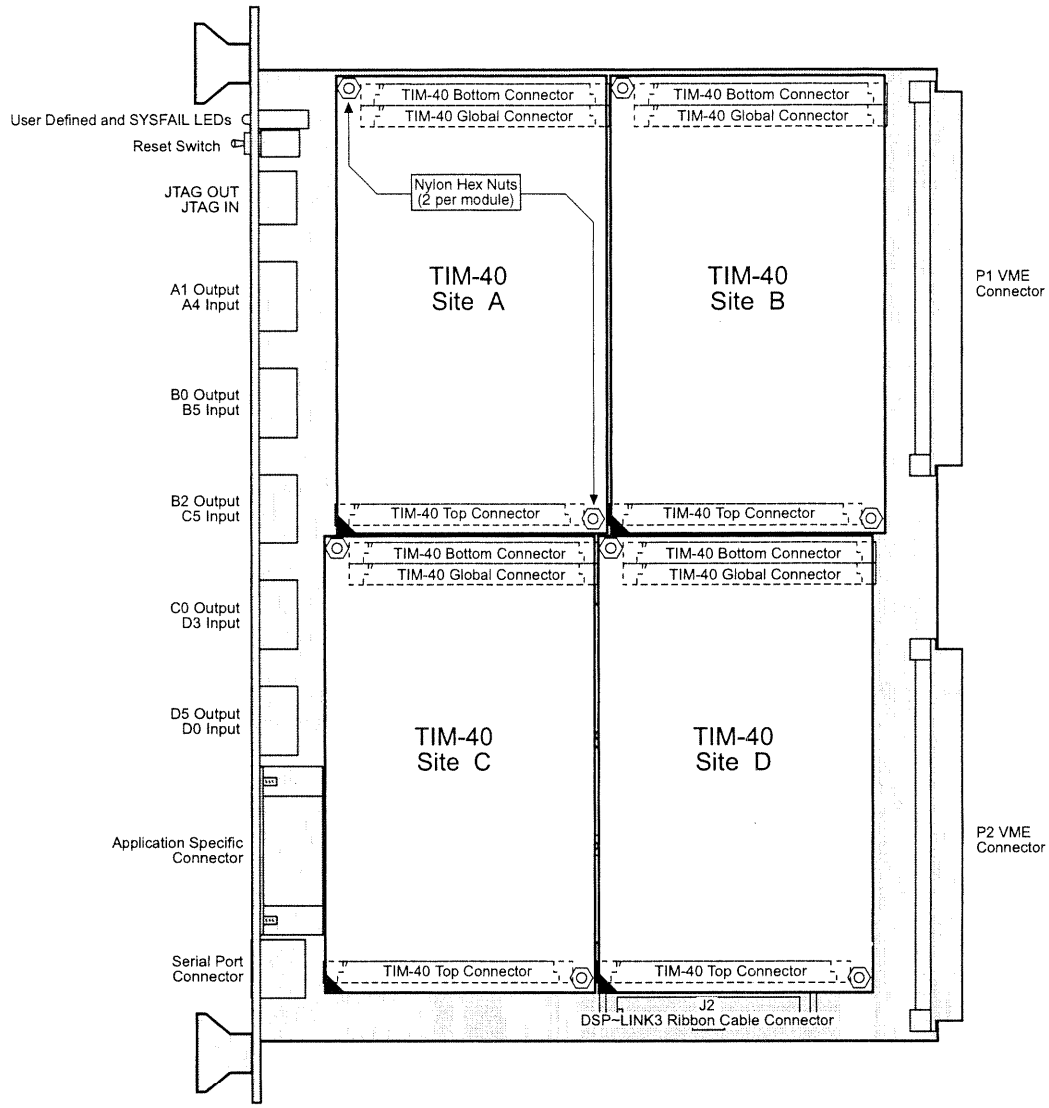


Figure 5 TIM-40 Module Installation



Caution: Before handling the CV8 Carrier Board or a module, ensure that you and the components are properly grounded to prevent damage from electrostatic discharge.

1. Use the nylon mounting posts on the TIM-40 sites to position the TIM-40 module.
2. Press down on the module to mate the top, bottom, and global connectors.
3. Secure the module on to the CV8 Carrier Board by screwing the nylon hex nuts that came with the module on to the mounting posts.

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3.4. Installing DSP~LINK3 Modules on the Board

Your CV8 Carrier Board may already contain a DSP~LINK3 module. If it doesn't, or you are adding modules to it, follow the these instructions to install it on the CV8 Carrier Board.

Note: If you are installing TIM-40 modules in sites C or D, you will not be able to install a DSP~LINK3 module. If you are installing a module in site D you will also not be able to use the PIC connector.

The following figure shows the location of the modules on the CV8 Carrier Board and the mounting hardware for the sites.

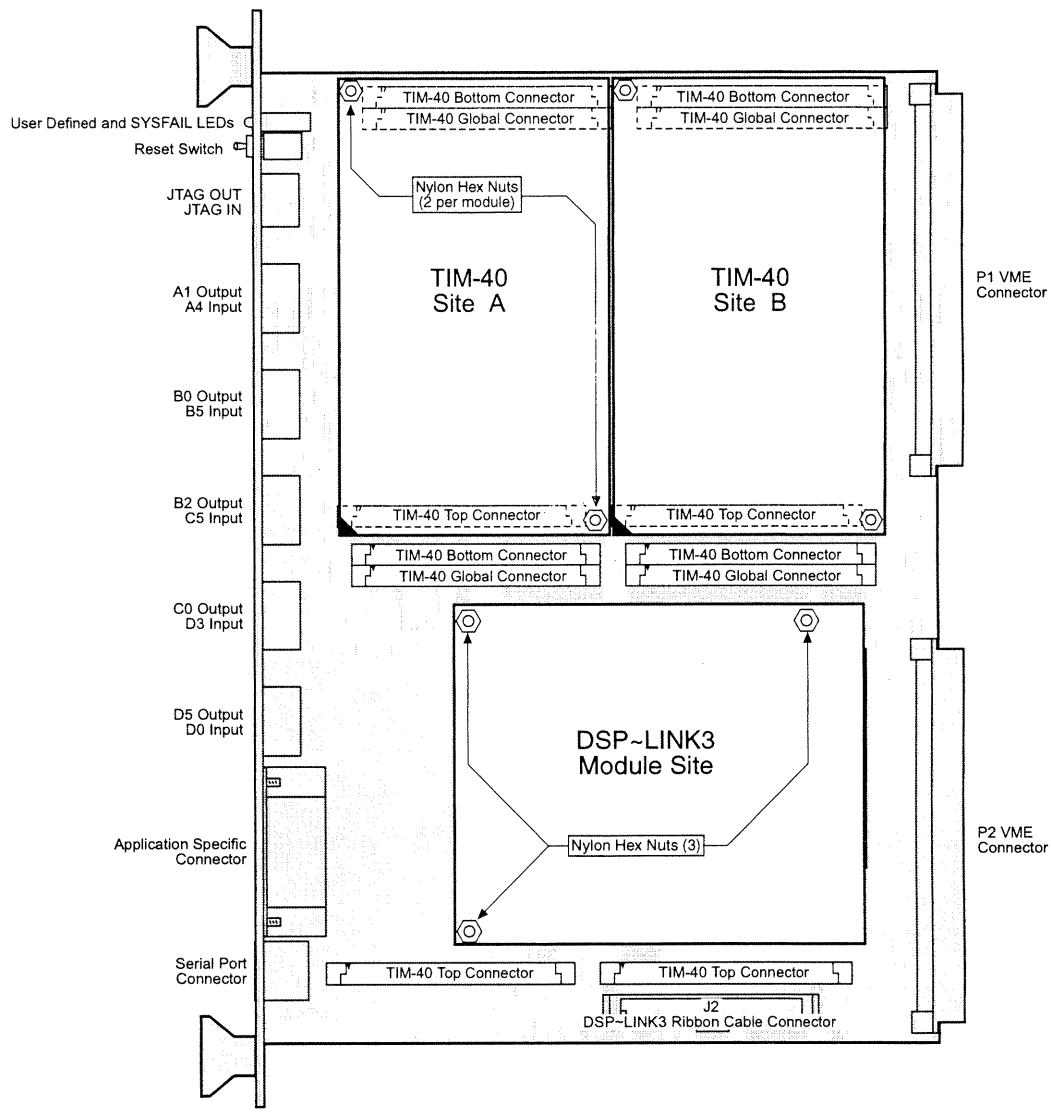


Figure 6 DSP~LINK3 Module Installation

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Caution: Before handling the CV8 Carrier Board or a module, ensure that you and the components are properly grounded to prevent damage from electrostatic discharge.

Follow these instructions to install a DSP~LINK3 module on to the CV8 Carrier Board.

1. There are three nylon mounting posts on the CV8 Carrier Board. Position the DSP~LINK3 module on to the CV8 Carrier Board over the nylon mounting posts.

2. Secure the module to the CV8 Carrier Board by screwing the three 3mm nylon hex nuts to the mounting posts.

3.5. Installing and Cabling the CV8 Carrier Board

After the jumpers on the CV8 Carrier Board have been configured, it can be installed in a VME chassis and any other connections can be made.

1. Ensure that all hardware is powered off.

2. Attach any DSP~LINK3 cables or DSP~LINK3 module to the board.

3. Install the CV8 Carrier Board into an empty VME slot of the VME chassis.

4. Attach the COMM Port, JTAG, serial port, and Application Specific Connector cables to the board if you are using them.

5. The hardware can now be powered on.

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4 TIM-40 Nodes

The CV8 Carrier Board accommodates single and double width TIM-40 modules on its four TIM-40 module sites (sites A, B, C, and D). Each site has three 80-way connectors, supporting the top, bottom and optional Global Bus connectors.

The TIM-40 module specification was developed by Texas Instruments to deliver the full performance of TMS320C4x DSP's on a standardized parallel processing element. The standard provides physical, electrical interface, and system characteristics for module development. Modules are installed on TIM-40 carrier boards which connect the modules to each other and to the host system. Spectrum offers a variety of TIM-40 modules with various configurations including single and multiple TMS320C40, single and multiple TMS320C44 with SRAM, DRAM, or specialized I/O. Complete information on the TIM-40 specification can be found in the TIM-40 TMS320C4x Module Specification available from Texas Instruments.

Site A is designated as the master node and therefore has access to more resources than sites B, C, or D. The resources accessible to the sites are summarized in the following list.

All Sites (A, B, C, and D)	Site A Only
• DSP~LINK3 Interface	• SCV64 chip registers
• Shared SRAM	• VME bus as a master
	• Serial port UART

4.1. Global Bus

The global bus of each site is buffered onto the global shared bus to allow each 'C4x processor access to the shared SRAM (Far Global SRAM) via STRB1. Access to the shared SRAM is granted to any of the TIM-40 sites or a VME by an arbitrator circuit.

The general global memory map for each TIM40 Node is shown in the following table.

The shared SRAM on the global bus is accessed via STRB1 control through the global connector. The CV8 Carrier Board decodes STRB1 and it's associated control signals to access the various resources available to each site. The Global Bus Control Register is configured for external READY logic control for STRB1.

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Table 3 TIM-40 Global Bus Memory Map

C4x Address	Site A Access	Site B, C, and D Access
8000 0000h - 8FFF FFFFh	Reserved for TIM-40 Global Memory	Reserved for TIM-40 Global Memory
9000 0000h	VME64 IACK Space	Reserved
9100 0000h	SCV64 Register Set Base Address	
92*xx xxxx*h	Node A Interrupt Status/Clear Register	Node A Interrupt Set Register
93*xx xxxx*h	Application Specific Interrupt Status/Clear Register	
94*xx xxxx*h	Host Interrupt Clear Register	
95*xx xxxx*h	Node ID Register*	
9600 0000h	VCONTROL Register	Reserved
9600 0001h	VSTATUS Register*	
9600 0002h	VOFFSET Register*	
9600 0003h - 97FF FFFFh	Reserved	
9700 0001h	LED1 Register	
9700 0002h	LED2 Register	
9700 0003h	LED3 Register	
9700 0004h - 97FF FFFFh	Reserved	
9800 0000h	16C550 UART Registers Base Address	
99*xx xxxx*h	Round Robin Timeslot Register	
9A00 0000h - 9CFF FFFFh	Reserved	
9D*xx xxxx*h	DSP~LINK3 reset register	
9E00 0000h	DSP~LINK3 Standard Access space	
9F00 0000h	DSP~LINK3 Standard Fast Access space	
A000 0000h	DSP~LINK3 /RDY controlled space	
A100 0000h	DSP~LINK3 /ASTRB Access space	
A200 0000h - AF00 0000h	Reserved	
B000 0000h - BFFF FFFFh	Shared 32-bit SRAM (128K to 2048K)	
C000 0000h - FDFF FFFFh	VME64 A32 Space	Reserved
FE00 0000h - FE3F FFFFh	Default A24:D16 Space	
FE40 0000h - FE7F FFFFh	Default A24:D32 Space	
FE80 0000h - FFFF BFFFh	VME64 A32 Space	
FFFF C000h - FFFF FFFFh	Default A16:D16 Space	

* Read Only

Wait states on /STRB1 are only generated by the /RDY line. /STRB1 uses a 1K page size (32-bit words) and the STRB SWITCH is active.

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4.2. Register Address Decoding

The Global Shared Bus addresses for many registers are decoded using only the upper 8 address bits; the remaining lower 24 bits can be any value. Therefore, a particular register can be seen at every location within its corresponding 24-bit address range. For example, the Node ID Register addressed at 95*xx xxxx*h (see the following memory map) can be accessed at 9500 0000h, 95FF FFFF, and all locations in between these two addresses.

The following registers on the Global Shared Bus decode their addresses using only the upper 8 address bits:

- Node A Interrupt Status/Clear Register
- Application Specific Interrupt Status/Clear Register
- Host Interrupt Clear Register
- Node ID Register
- Round Robin Timeslot Register
- DSP~LINK3 reset register

4.3. VME64 Bus Access

Only TIM-40 site A can access the VME64 bus. Refer to the VM64 Interface chapter for information on how the VME64 is accessed.

4.4. Communication Ports

Each site is connected to the others via COMM Ports. Each COMM Port can communicate at up to 20 Mbytes per second. Because 'C44 processors only have four COMM Ports, not all internal or external COMM Ports from each node may be available, but a COMM Port link to Node A is usually present regardless of which 'C4x processor is used on the node.

4.5. Front Panel Serial Port

An RS-232 serial port on the front panel is supported by a 16C550 UART accessible to Node A. The UART provides one input and one output channel. The UART used is the TL16C550B Asynchronous Communications Element from Texas Instruments, or equivalent.

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The serial port output is driven by a MAX232A or equivalent RS-232 driver, with an output voltage of ± 8 Volts. The front panel connector is an 8-pin Mini-DIN connector. The signals presented on the front panel are

Data	Control
• TxD+ (tied to ground)	• DTR
• TxD-	• CTS
• RxD+ (tied to ground)	• Ground
• RxD	

The UART is clocked from the BAUDCLK of the SCV64 (32 MHz ÷ 13 = 2.461538 MHz) and provides asynchronous communications to 153.85 kbps. The highest standard data rate provided is 38.4 kbps. The 16C550 uses a standard divide by 16 on the master clock to generate its baud rate clock. A second divisor register is then used to set the input and output baud rate according to the following formula:

$$Baud\ Rate = \frac{32\ \text{MHz}}{13 \times 16 \times Divisor\ Register}$$

For example, A divisor register of 1 gives 153.85 kbps, and a divisor register of 4 gives 38.46 kbps (38.4 kbps with an error of 0.16%).

The registers for the device are mapped to Node A's local bus memory as shown in the following table. Complete details on using this UART can be found in the *TL16C550B Asynchronous Communications Element datasheet*.

Table 4 Node A UART Registers

Address	DLAB*	(R)ead/(W)rite	Register	Description
9800 0000h	0	R	RBR	Receiver Buffer Register
		W	THR	Transmitter Holding Register
	1	R/W	DLL	Divisor Latch (LSB)
9800 0001h	0	R/W	IER	Interrupt Enable Register
	1	R/W	DLM	Divisor Latch (MSB)
9800 0002h	*X*	R	IIR	Interrupt Identification Register
		W	FCR	FIFO Control Register
9800 0003h	*X*	R/W	LCR	Line Control Register
9800 0004h	*X*	R/W	MCR	MODEM Control Register
9800 0005h	*X*	R/W	LSR	Line Status Register
9800 0006h	*X*	R/W	MSR	MODEM Status Register
9800 0007h	*X*	R/W	SCR	Scratch Register

*The Divisor Latch Access Bit (DLAB) is the MSB (bit 7) of the Line Control Register (LCR).

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4.6. 'C4x IIOF Lines

The IIOF0, IIOF1, and IIOF2 lines of each node are used primarily as interrupt inputs for the CV8 Carrier Board. Each node's initialization code should configure the IIOF0, IIOF1, and IIOF2 lines of its 'C4x as level-triggered inputs. The IIOF3 line should be initialized as an output to support the TIM-40 /CONFIG signal. The IIOF lines of each node are assigned according to the following table. Refer to the *Interrupt Handling* chapter for further information.

Table 5 TIM-40 IIOF Line Assignment

Line	Node	Assignment
IIOF0	A*	Application Specific Interrupt if JP20 is installed.
		Logical OR of DSP~LINK3 IRQs 0 to 3 if JP16 is installed.
		DSP~LINK3 IRQ0
	B	DSP~LINK3 IRQ1
	C	DSP~LINK3 IRQ2
	D	DSP~LINK3 IRQ3
IIOF1	A	Node B, C, or D Interrupt via *Node A Interrupt Set* register.
	BCD	Application Specific Interrupt if JP20 is installed.
IIOF2	A	SCV64 Interrupts. Logical OR of KIPL[0..2] lines from SCV64.
	All**	VME Host Interrupt via the *VME64 Interrupt Set* register.
IIOF3	All	TIM-40 /CONFIG signal configured as an output.

* IIOF0 interrupts on Node A are latched and are cleared via the *Application Specific Interrupt Clear* register.

** VME Host interrupts on Node A IIOF2 are handled differently than on nodes B, C, and D. Refer to the *Interrupt Handling* chapter for further information.

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4.7. Cycle Types and Cycle Performance

The number of wait states required for accesses to the various memory devices, interface IC's, and registers on the CV8 Carrier Board is shown in the following table.

Table 6 Cycle Types

Access Type	Wait States from a C4x over Shared Global Bus	SCV64 Cycles from VME64 Slave Access
UART Read	3	N/A
UART Write	3	N/A
IIOF2 Interrupt Control Register	1	N/A
DSP~LINK3	/RDY controlled	N/A
Global SRAM	1	2 write, 1read

4.8. Clock Sources

TIM-40 clock input pins are supplied with a 60 MHz clock source. If a TIM-40 module requires a different clock speed, it will have to have its own on board clock source. The CV8 Carrier Board can support TIM-40 modules with clock frequencies up to 60 Mhz.

Note: The CV8 Carrier Board does not support TIM-40 modules with on board clock frequencies higher than 60 MHz. Mixed clock speeds are not supported; all TIM-40 modules must be the same clock speed.

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4.9. User Defined TIM-40 Pins

Eight User Defined Pins (UDPs) are routed to the front panel connectors on the CV8 Carrier Board from each TIM-40 site. See the *Front Panel Connectors* section for pinouts. The PCB traces for these lines are designed to ensure excellent signal integrity and immunity from digital noise on the board. A cross-section of the physical layout of these traces is shown in the following diagram.

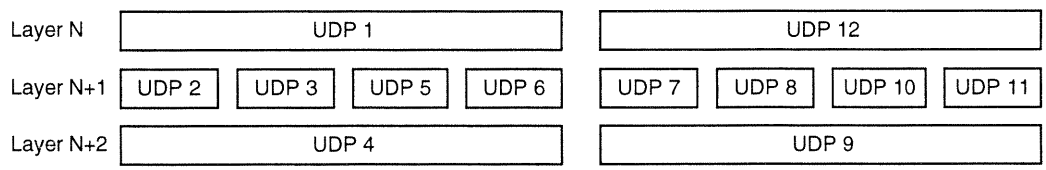


Figure 7 User Defined Pin PCB Trace Cross Section

On custom designed TIM-40 modules, signal grounds should be routed to User Defined Pins 1, 4, 9 and 12.

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5 VME64 Bus Interface

The CV8 Carrier Board interface to the VME64 bus is based on Tundra Semiconductor Corporation's SCV64 VME64 Interface chip. This chip enables the CV8 Carrier Board to act as a master or a slave on the VME64 bus, and also provides VME interrupt capabilities.

A host on the VME64 bus can access the Far Global SRAM or the Test Bus Controller on a slave CV8 Carrier Board in A24 or A32 address modes.

As a VME master, the CV8 Carrier Board supports A16, A24, or A32 transactions from TIM-40 site A to the VME64 bus through the SCV64 chip. All access to the VME64 bus as a master is done on TIM-40 site A. Only site A can access the SCV64 registers to produce interrupts back to the host, set up DMA transfers, and perform mailbox and timer actions.

The CV8 Carrier Board supports Auto-Syscon capabilities allowing it to become the System Controller board when placed in slot 0 of the VME backplane. The SCV64 becomes the VMEbus system controller if the VME bus signal BGin3* is low upon a low to high transition on the /PWRRST or /SYSRST VME bus signals

Upon reset, the SCV64 is in Bus-Isolation Mode (BI-Mode) which isolates the SCV64 from the VME64 bus. The SCV64 is released from BI-Mode by a write to the SCV64 Location Monitor from either Node A of the CV8 Carrier Board or from an external host on the VME bus.

Note: Unaligned transfers (UAT) are not supported.

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5.1. VME64bus A32 Mode Slave Memory Map

A host (as a master) on the VME bus can access the areas on the CV8 Carrier Board shown in the following memory map table.

Table 7 VME64 Host Byte Address Memory Map

VME64 Byte Address BASE+	Access
0000 0000h - 00FF FFFFh	Far Global SRAM Memory Space
0100 0000h	Test Bus Controller Register Base Address
0200 0000h - 02FF FFFFh	Reserved
0300 0000h	VME64 Slave Reset
0400 0000h	VME64 Slave /CONFIG Status*
0500 0000h	VME64 Interrupt Set
0600 0000h - 07FF FFFFh	Reserved

* Read Only

Note: Byte, word and longword accesses are supported to the Far Global SRAM.

5.2. Automatic VME64 Base Address Configuration

By default, the CV8 Carrier Board supports the SCV64 AUTOBAR mode for initializing its VME base address. In this mode the SCV64 fetches the VME64 base address, as set by the J19 jumper block, and loads it into its VME base address register upon power up. The jumpers provide the upper 5 bits of the 32-bit VME64 address. This is the base address location of the CV8 Carrier Board within the VME64 memory map. The default setting of J19, for example, sets the binary value of bits [A31..A27] of the VME address lines to 11101. This corresponds to a VME base address of 0x1000 0000. The following table shows the binary values for the first four base addresses.

Table 8 Base Address Table (JP19)

A31 (Pin 9-10)	A30 (Pin 7-8)	A29 (Pin 5-6)	A28 (Pin 3-4)	A27 (Pin 1-2)	Base Address
In	In	In	Out	In	0x10000000
In	In	In	Out	Out	0x18000000
In	In	Out	In	In	0x20000000
In	In	Out	In	Out	0x28000000

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This CV8 Carrier Board implements this mode by using the KFC pins of the SCV64 chip. Upon power up or reset KFC2 is high and KFC0 is low while the data bus to the SCV64 is driven with the base address set by jumper block J19. For further information on configuring the VME base address within the SCV64 chip, refer to the *SCV64 User Manual*.

5.3. Node A Access to the VME64 Bus

Node A of the CV8 Carrier Board can access the VME64 bus as a master via its Global Bus. It can access the A32, A24:D16, A24:D32, and A16:D16 spaces on the VME bus. Each of these spaces is mapped to a specific range of the Node A Global Bus memory map as shown in the following memory maps.

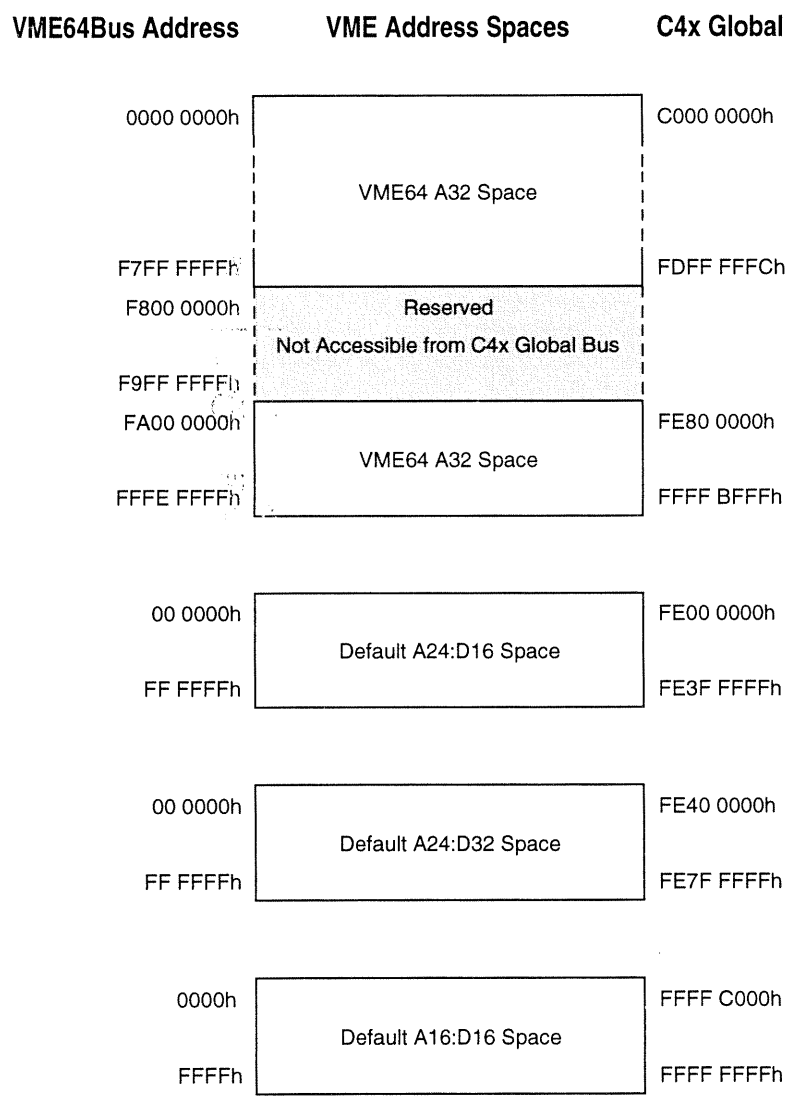


Figure 8 Node A Access to the VME Bus

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6 Far Global SRAM

The Far Global SRAM is located on the SCV64 Local Bus and is accessible from the Global Shared Bus and the VME64 bus. Any TIM-40 site can read and write to the Far Global SRAM from the TIM-40 Global Bus. A host on the VME64 bus can read and write to the Far Global SRAM as a master. This allows it to act as a memory interface between the VME64 bus and the TIM-40 nodes.

6.1. Memory Configuration

The Far Global SRAM consists of four banks of memory (banks 0 to 3). Each bank consists of four one wait-state, 20 ns, 8-bit SRAM chips. The total amount of memory is dependent upon the size of the memory devices that are installed.

Memory Device Size	Total Far Global Memory
128K x 8-bit	512 KB
512K x 8-bit	2 MB
2M x 8-bit	8 MB

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6.2. Memory Map

The VME and TIM-40 Global Bus memory address ranges for the different amounts of Far Global SRAM are shown in the following figure.

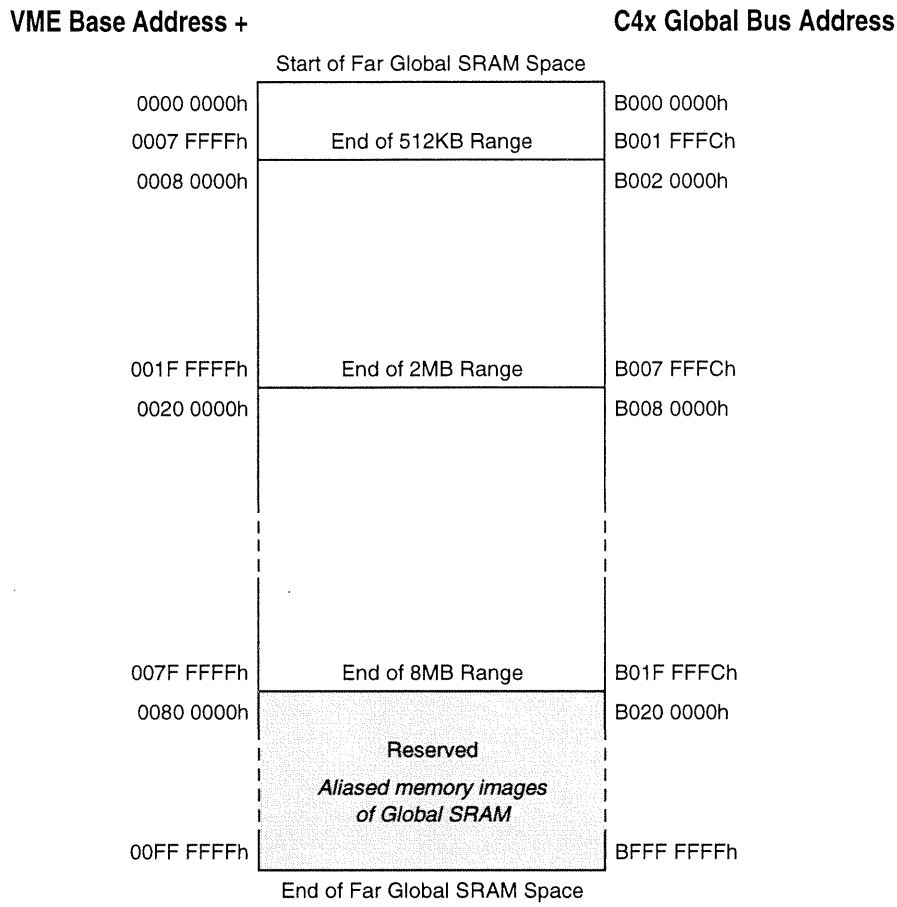


Figure 9 SRAM Memory Map

6.3. VME64 to C4x Global Bus Address Translation

The VME64 bus is byte addressed, while the C4x Global Bus is 32-bit word addressed. As a result, each C4x Global Bus address spans four VME64 bus addresses on the Far Global SRAM. For example, the 32 data bits of C4x Global Bus address B002 0000h correspond to the four bytes mapped at VME offset address 0008 0000h.

VME Offset Address	C4x Global Bus Address B002 0000h (bit D31..D0)
0008 0000h	D7..D0
0008 0001h	D15..D8
0008 0002h	D23..D16
0008 0003h	D31..D24

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7 DSP~LINK3 Interface

The DSP~LINK3 interface allows external DSP~LINK3 I/O modules to be attached to the CV8 Carrier Board through the ribbon cable connector or by the mezzanine connector. Both connectors can be used at the same time.

The DSP~LINK3 interface may also be present on the VME P2 connector on CV8 Carrier Boards specified for this option. Boards with this option can be identified by the presence of resistor packs R63 to R78 located just above the DSP~LINK3 module connector (J17). Refer to the *On Board Connectors* section in this manual for further details and a diagram showing the location of the resistor packs.

The CV8 Carrier Board can support up to 4 slave DSP~LINK3 devices. If a DSP~LINK3 module is installed, up to 3 additional devices can be connected to the DSP~LINK3 connector(s); otherwise, up to 4 devices can be connected to DSP~LINK3 connector(s). The ribbon cable can be up to 12 inches (30 cm) long.

Any 'C4x node can access the DSP~LINK3 interface from its global bus; but it cannot be accessed from the VME64 bus.

The DSP~LINK3 reset line is controlled from Node A through the *DSP~LINK3 Reset* register. It is asserted by writing a "1" to the register or by any board reset condition. A DSP~LINK3 reset should be at least 1 µs long.

7.1. DSP~LINK3 Operating Modes

The CV8 Carrier Board supports the three data transfer modes and the address page turn (/ASTRB) cycle of the DSP~LINK3 interface. The timing of the DSP~LINK3 interface for the CV8 Carrier Board is based on multiples of the DSP's H1 clock. For example, the length of a Standard Fast transfer DSP~LINK3 is 5 times the DSP's H1 clock signal. If a H1 cycle is about 33 ns, for the 60 MHz DSP, then a Standard Fast transfer is about 165 ns. The following table describes the different transfer modes of the interface.

Standard — For slave boards that are similar to DSP~LINK1 slave boards and operate with a fixed, minimum 130 ns access time. Cycle time is 7 times H1.

Standard Fast — For DSP~LINK3 slave boards that have fast, fixed access times. Cycle time cycle is 5 times H1.

RDY Controlled — For DSP~LINK3 slave boards that require variable length access times. /DSTRB is active until the slave asserts the DSP~LINK3 ready signal (/RDY) to end the cycle.

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/ASTRB Cycle For slave boards that require more than the 16 KWords of addressing provided by the standard DSP~LINK3 address lines. The bus master uses the /ASTRB cycle to place the page address onto the DSP~LINK3 data lines. It determines which address page is accessed on the slave board. This allows access to up to 2^{14} address pages with each address page having an address depth of 2^{14}. The /ASTRB Cycle has the same timing as the Standard Fast transfer cycle.

Each mode occupies its own 64K address space on the Global Shared Bus. The following table shows how the CV8 Carrier Board supports the different DSP~LINK3 operating modes.

Table 9 DSP~LINK3 Operating Modes

Mode	Base Address
Standard Access	9E00 0000h
Fast Standard Access	9F00 0000h
Ready Control Access	A000 0000h
Address Strobe Control	A100 0000h

7.2. Interface Signals

The DSP~LINK3 interface consists of two 16-bit bi-directional buffers for data, a16-bit address latch, and a control signal buffer. The control signals are terminated via a SCSI terminator. The DSP~LINK3 interface signals are:

- 32 data I/O lines: D[31..0]
- 16 address outputs: A[15..0] A15 and A14 are used for slave device (board) selection.
- Read (/RD), write (/WR), and reset (/RST) outputs
- Tri-state ready (/RDY) input
- 4 interrupt inputs (IRQ0 to IRQ3). Each interrupt is routed to the IIOF0 line of a specific 'C4x node; IRQ0 to Node A, IRQ1 to Node B, and so on. By installing jumper J24, all IRQs can also be routed to the IIOF0 line of Node A's embedded 'C44 through an OR gate.

Refer to *DSP~LINK3 specification* for details (available from Spectrum's internet web site at http://www.spectrumsignal.com)

7.3. DSP~LINK3 Reset

The DSP~LINK3 reset line is controlled from Node A through the *DSP~LINK3 Reset* register. This register is located at address 9D00 0000h of Node A's Global Bus. The

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DSP~LINK3 reset line is asserted by writing a “1” to the register by writing a “1” to the LSB of this register and released by writing a “0” to the LSB.

The DSP~LINK3 reset line will also be asserted during any board reset condition.

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8 JTAG Interface and Debug Capability

The CV8 Carrier Board supports JTAG in-circuit emulation from a built in 74ACT8990 Test Bus Controller and a debug monitor. JTAG in-circuit emulation is fed by the VME64 host via the Test Bus Controller, or C Source Debugging can be done through the JTAG connectors to an emulator board running a debug monitor on an adjacent computer.

Each of the 'C4x processors has a JTAG interface for debug purposes. JTAG data lines are routed to each available 'C4x node in turn. The 74ACT8990 Test Bus Controller permits the VME64 interface to operate the JTAG chain. Additionally, there are two JTAG connectors, JTAG IN and JTAG OUT, which can route the JTAG chain off-board. If a JTAG IN connection with a clock signal is present the Test Bus Controller is automatically disconnected. Two boards can be connected through the JTAG chain to support debugging of up to 16 processors.

The full JTAG chain is shown in the following diagram. Unoccupied TIM-40 sites are bypassed. For multiple processor TIM-40 modules, refer to the TIM-40 module documentation for information on the order in which the processors are connected in the JTAG scan path.

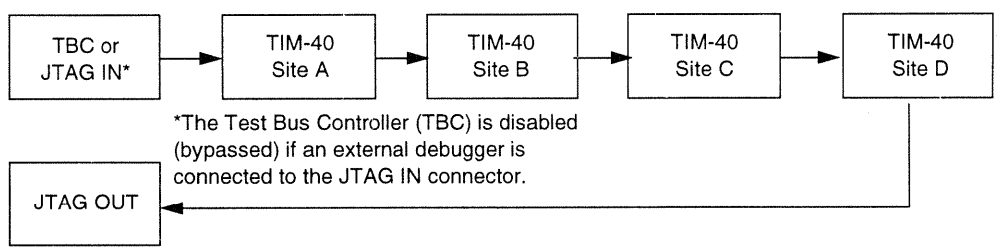


Figure 10 JTAG Chain

The JTAG IN input is buffered to reduce the load on an external JTAG device. The JTAG OUT output is buffered to guarantee enough drive to external JTAG loads.

For multiple CV8 Carrier Boards, the JTAG cable of the external debugger should be connected only to the JTAG IN of the first board. The JTAG OUT of the first board should be connected to the JTAG IN of second board. The JTAG OUT of the second board should be connected to the JTAG IN of third board and so on.

Note: All hardware must be powered off before the JTAG cable are connected and the JTAG chain is set up.

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9 Interrupt Handling

9.1. Overview

The following diagram shows how interrupts are routed on the CV8 Carrier Board.

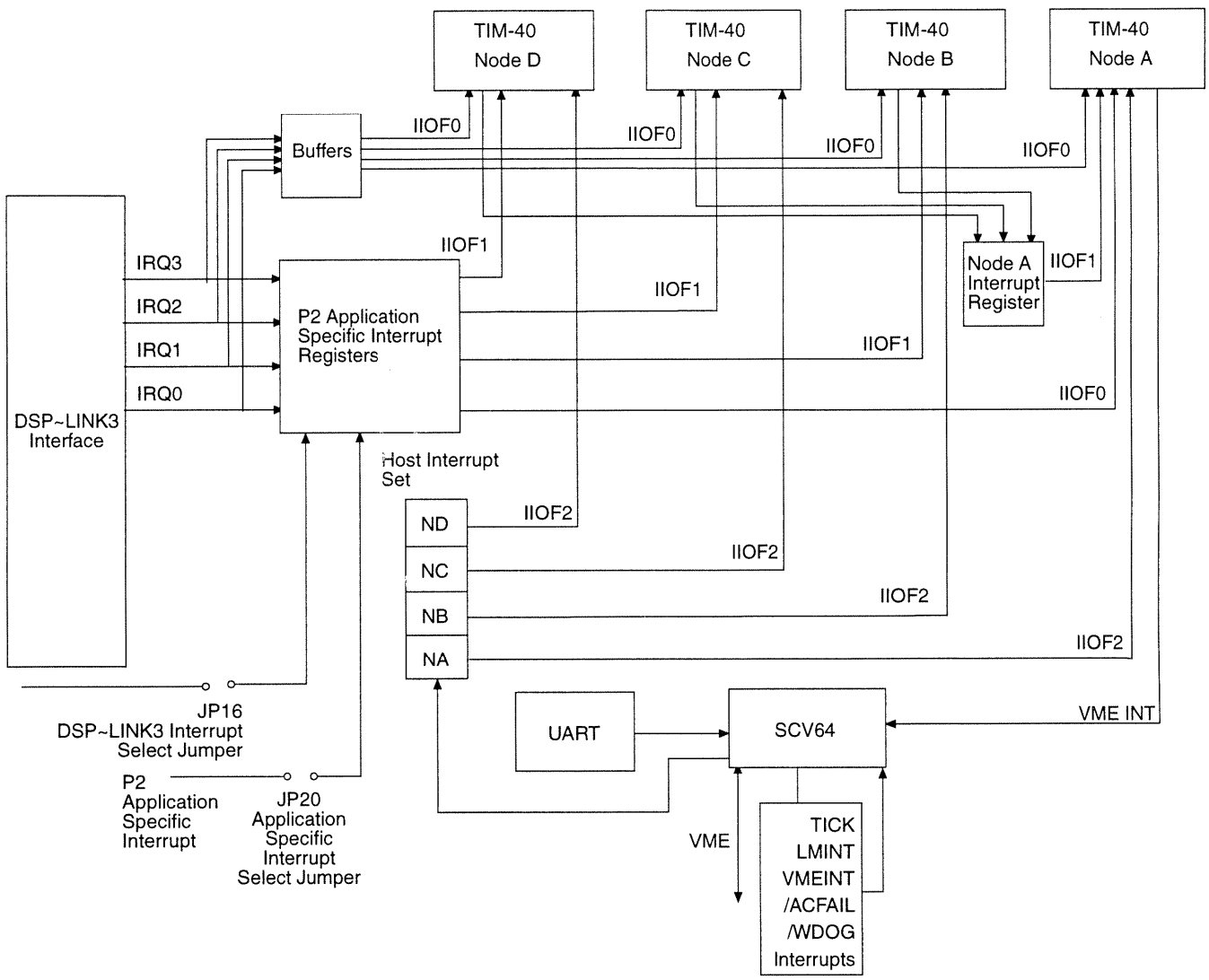


Figure 11 Interrupt Block Diagram

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This next diagram shows the workings of the P2 Application Specific Interrupt Register and the Jumpers JP16 and JP20.

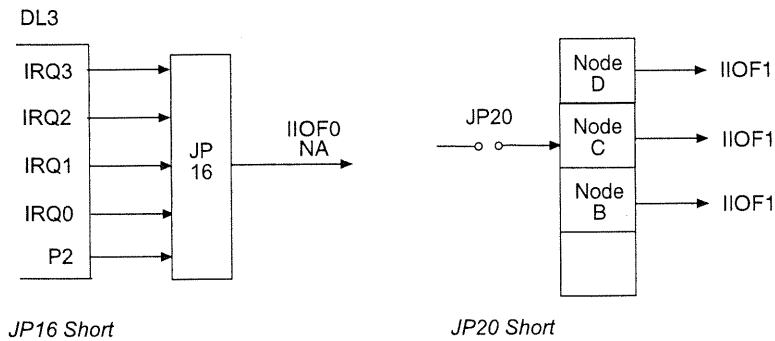


Figure 12 P2 Application Specific Interrupt Registers

9.2. SCV64 Chip to Node A Interrupts

Interrupts to the IIOF2 line of Node A from the SCV64 chip are routed to the chip's /LIRQ input lines. The following table shows how these interrupts are mapped to the SCV64 chip interrupt inputs.

Table 10 SCV64 Interrupt Inputs to Node A

SCV64 Interrupt Input	Description
/LIRQ0	Host Interrupt Register
/LIRQ1	TL16C550 UART chip interrupt signal
/LIRQ3	SCV64 chip /TICK signal
/LIRQ4	SCV64 chip /LMINT signal
/LIRQ5	SCV64 chip /VMEINT signal
/L7IACF	VME bus /ACFAIL signal
/L7IMEM	SCV64 chip /WDOG signal

The SCV64 maps these interrupt signals on its KIPL[0..2] lines. The CV8 Carrier Board performs a logical OR of these KIPL[0..2] signals to generate the IIOF2 signal for Node A.

The C4x on Node A generates an IACK cycle to the SCV64 to clear these interrupts.

9.3. VME Host Interrupts to Any Node

A host on the VME64 bus can cause an interrupt to any node on the CV8 Carrier Board. The interrupt asserts the IIOF2 line on the particular node.

The *VME64 Interrupt Set Register* (offset 0500 0000h from the board's VME base address) is used to generate the interrupt. The Host Interrupt Clear Register (9400 0000h

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from the node's Global Bus) to clear the interrupt. The structure of these registers is the same. Each node is represented by one of the register's lower 4 bits as shown.

D31..D4	D3	D2	D1	D0
Reserved	Node D Interrupt	Node C Interrupt	Node B Interrupt	Node A Interrupt

Figure 13 VME64 Interrupt Register Structure

A host on the VME bus generates an interrupt to a particular node by writing a "1" to the corresponding bit in the VME64 Interrupt Set Register. This asserts the IIOF2 line to the node. Any number of interrupt bits can be set, allowing the host to interrupt multiple nodes with one write operation to the VME64 Interrupt Register.

An interrupted node clears the interrupt by writing a "1" to its bit in the *Host Interrupt Clear* Register. CV8 Carrier Board circuitry prevents a node from clearing a VME host interrupt to another node. For example, Node B cannot clear a VME host interrupt to Node C by writing a "1" to bit D2 of the Host Interrupt Clear Register. This write would have no effect on the Node C interrupt. As a result, any node can clear its own interrupt by writing Fh (1111 binary) to the lower four bits of this register.

To clear an interrupt received on its IIOF2 line, Node A must also generate an IACK cycle. Its IIOF2 line is driven from the SCV64 chip, while the IIOF2 lines for nodes B, C, and D are driven directly from CV8 Carrier Board circuitry. This allows other interrupts, such as UART and VME bus interrupts, to generate IIOF2 interrupts on Node A through the SCV64 chip. The IACK cycle is executed by generating a SCV64 read cycle and presenting the interrupt level on KADDR(1..3) with KADDR(16..19) = 1111b.

Refer to the *Registers* section of this manual for more information on these registers.

9.4. Node A to VME Bus Interrupts

Node A of the CV8 Carrier Board can send vectored interrupts to the VME64 bus using two of the internal SCV64 registers: the VMEbus Interrupter Vector register and the VMEbus Interrupter Requester register Only Node A can access the SCV64 register set. The base address for the SCV64 register set that Node A uses is 9100 0000h. Refer to the *SCV64 User Guide* for a complete description of how to generates interrupts on the VME64 bus by using these SCV64 registers.

9.5. Node B, C, and D to Node A IIOF1 Interrupts

TIM-40 sites B, C, and D can interrupt TIM-40 site A by writing a "1" to the Node A bit (bit D0) of the *Node A Interrupt Set* register. This generates an interrupt on Node A's IIOF1 line. Node A can identify which node produced the interrupt by reading the *Node A Interrupt Clear* register. Bits D1 to D3 of this register are used to interrupting node. Each bit represents a node. A "1" in the bit position indicates which node caused the interrupt. To clear the interrupt, Node A writes a "1" to the bit position corresponding to

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the interrupting node in the *Node A Interrupt Clear* register. Refer to the *Registers* section of this manual for more information on these registers.

9.6. DSP~LINK3 Interrupts

Four DSP~LINK3 active-low, level-sensitive interrupts are individually mapped to the IIOF0 inputs of the four 'C4x nodes. Additionally, jumper JP16 can configure all of these interrupts to be routed to the IIOF0 of the Node A embedded 'C44 through a quad-input OR gate, so that any interrupt on IRQ0 to IRQ3 will interrupt Node A. During 'C4x node configuration, these inputs are routed through tri-state buffers on the CV8 Carrier Board to prevent any interference with the 'C4x node boot mode selection during power up initialization. All four DSP~LINK3 interrupts are driven by open collector drivers so that more than one device on DSP~LINK3 can drive the same IRQ line. The IIOF outputs to the TIM-40 sites are tri-stated until the IACK input for each TIM-40 is asserted to indicate the boot period is finished.

The default routing for the DSP~LINK3 (JP16 not installed) is shown in the following table.

Table 11 DSP~LINK3 Interrupt Routing

DSP~LINK3 Interrupt Source	C4x IIOF0 Input Interrupt Destination
IRQ0	TIM-40 site A
IRQ1	TIM-40 site B
IRQ2	TIM-40 site C
IRQ3	TIM-40 site D

The CV8 Carrier Board does not latch the DSP~LINK3 interrupts. Refer to the documentation on each module for information on acknowledging and clearing DSP~LINK3 interrupts.

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9.7. Application Specific Interrupt

The VME P2 connector on the CV8 Carrier Board has an Application Specific Interrupt line that is enabled on the board by installing JP20. This negative edge-triggered Application Specific interrupt input is internally latched on the CV8 Carrier Board. This interrupt is simultaneously sent to the IIOF1 lines of nodes B, C, and D, as well as the IIOF0 line of Node A.

Each 'C4x node must clear its own Application Specific interrupt by writing a "1" to the *Application Specific Interrupt Clear* register. Refer to the *Registers* section of this manual for more information on this register.

9.8. C4x Interrupts on IIOF3

The TIM-40 modules IIOF3 are typically used as a source for the /CONFIG line, or for an on-module interrupt source. IIOF3 is **NOT** brought out to the VME64 C4x carrier board from the TIM-40 nodes.

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9.9. Sending and Receiving Interrupts

The following table lists what registers are used to send/receive interrupts and what acknowledgments are needed to clear interrupt signals.

Table 12 Interrupt Generation/Handling

Interrupt Generation:		
Source	**Destination**	**Description**
VME device	Node (B,C,D)	Write to VME Interrupt Register (base + 0x5000000)
VME device	Node A	Set SCV64 Interrupt registers to respond to VME Interrupt Level and vector
Node A	VME device	Write to VINT register on the SCV64 chip (base + 0x91000000 + 0x08C)
Node (B,C,D)	VME device	Not available
Node (B,C,D)	Node A	Write to Node A Interrupt Register (base + 0x92000000 on Node (B,C,D))
Node A	Node (B,C,D)	Not available
DSP~LINK3	Node (A,B,C,D)	Hardware controlled
Node (A,B,C,D)	DSP~LINK3	Not available
App.Specific	Node (A,B,C,D)	Hardware controlled
Node (A,B,C,D)	App.Specific connector	Not available
Interrupt Handling:		
Source	**Interrupt**	**Description**
VME device	Node (A,B,C,D)	Write to Host Interrupt Clear Register (base + 0x5000000)
Node A	VME device	VME device specific
Node (B,C,D)	VME device	Not available
Node (B,C,D)	Node A	Write to Node A Interrupt Clear Register (base + 0x92000000 on Node A)
Node A	Node (B,C,D)	Not available
DSP~LINK3	Node (B,C,D)	Not latched, so not necessary to clear them
DSP~LINK3	Node A	Write to App.Specific Interrupt Clear Register (base + 0x93000000)
Node (A,B,C,D)	DSP~LINK3	Not available
App.Specific	Node (A,B,C,D)	Write to App.Specific Interrupt Clear Register (base + 0x93000000)
Node (A,B,C,D)	App.Specific connector	Not available

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10 Registers

A variety of registers are accessible on the CV8 Carrier Board. Registers are accessible from one or more of the following address busses depending upon their function

- Global Bus of TIM-40 site A
- Global Busses of TIM-40 Sites B, C, and D
- Host on the VMEbus

Registers specific to the CV8 Carrier Board reside on an FPGA chip on the board. These registers are described in this section. Complete information on registers that are part of the SCV64 VME64 interface, 16C550 UART, or ACT8990 Test Bus Controller chips can be found in their respective manuals.

SCV64 VME64 Interface Registers

Refer to the *SCV64 User Manual* for register descriptions. Registers from 9100 0000h to 9100 01FFh are 32-bit, except for those from 9100 0080h to 9100 00BFh, which are only 8-bit.

16C550 UART Registers

Refer to the *TL16C550B Asynchronous Communications Element datasheet* for register descriptions. These registers are low byte addressed.

ACT8990 Test Bus Controller Registers

Refer to Texas Instruments' *ACT8990 Test Bus Controller* datasheet for register descriptions.

The following table summarizes the addresses for the registers specific to the CV8 Carrier Board and also gives the base addresses for registers on the SCV64 VME64 interface, 16C550 UART, or ACT8990 Test Bus Controller chips.

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Table 13 Register Address Summary

Address			
Site A	**Sites BCD**	**VME Offset**	**Register**
9100 0000h	na	na	*SCV64 Registers*
9200 0000h	na	na	Node A Interrupt Clear
na	9200 0000h	na	Node A Interrupt Set
9300 0000h	9300 0000h	na	Application Specific Interrupt Clear
9400 0000h	9400 0000h	na	Host Interrupt Clear
9500 0000h	9500 0000h	na	Node ID
9600 0000h	na	na	VCONTROL
9600 0001h*	na	na	VSTATUS
9600 0002h*	na	na	VOFFSET
9700 0001h	na	na	LED1
9700 0002h	na	na	LED2
9700 0003h	na	na	LED3
9800 0000h	na	na	*16C550 UART Registers*
9900 0000h	na	na	Round Robin Timeslot
9D00 0000h	na	na	DSP~LINK3 Reset
na	na	0100 0000h	*Test Bus Controller Registers*
na	na	0300 0000h	VME64 Slave Reset
na	na	0400 0000h*	VME64 Slave /CONFIG Status
na	na	0500 0000h	VME64 Interrupt Set

*Read Only

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Node A Interrupt Clear Register

Bus	Site A	Site BCD	VME Offset
Address	9200 0000h	na	na

D31..	..D8
Reserved	

D7	D6	D5	D4	D3	D2	D1	D0
Reserved				Node D	Node C	Node B	Reserved

This register is used by Node A to identify and clear the source of interrupts on its IIOF1 line. The IIOF1 line on Node A is configured to receive interrupts generated by nodes B, C, and D.

- To identify which node generated the IIOF1 interrupt, Node A reads this register. A "1" in the corresponding bit, indicates which node generated the interrupt. For example, a "1" in bit D2 indicates that Node C generated an interrupt to the IIOF1 line of Node A.
- To clear a Node A IIOF1 interrupt, Node A writes a "1" to the appropriate bit in this register. For example, if Node C generated an IIOF1 interrupt to Node A, then it would be cleared by Node A writing a "1" to bit D2 of this register.

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Node A Interrupt Set Register

Bus	Site A	Site BCD	VME Offset
Address	na	9200 0000h	na

D31..	..D8
Reserved	

D7	D6	D5	D4	D3	D2	D1	D0
Reserved				Node D	Node C	Node B	Node A

This interrupt is used by nodes B, C, or D to generate interrupts to the IIOF1 line of Node A.

- To generate an interrupt to the IIOF1 line of Node A, Node B, C, or D writes the value 01h to this register.

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Application Specific Interrupt Clear Register

Bus	Site A	Site BCD	VME Offset
Address	9300 0000h	9300 0000h	na

D31..							..D8

D7	D6	D5	D4	D3	D2	D1	D0
Reserved				Node D	Node C	Node B	Node A

This register is used by all nodes to clear Application Specific interrupts. It is also used by Node A to clear a DSP~LINK3 interrupt received on its IIOF0 line.

The Application Specific Interrupt line of the VME P2 connector causes interrupts to be generated on the IIOF0 line of Node A, and on the IIOF1 lines of nodes B, C, and D. The IIOF0 line of node A also receives DSP~LINK3 IRQ0 interrupts and can be configured to receive an interrupt whenever DSP~LINK3 IRQ1, IRQ2, or IRQ3 interrupts are generated.

Note: Although nodes B, C, and D receive DSP~LINK3 interrupts, they do not have to clear them because the interrupts are not latched. DSP~LINK3 interrupts received by Node A, though, are latched on its IIOF0 line and must be cleared.

- To clear Application Specific interrupts received by any of the nodes, a node writes a "1" to its corresponding register bit. For example, Node C would clear it interrupt by writing a "1" to bit D2.
- To clear a DSP~LINK3 or Application Specific interrupt received by the Node A IIOF1 line, Node A writes a "1" to bit D0 of this register.

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Host Interrupt Clear Register

Bus	Site A	Site BCD	VME Offset
Address	9400 0000h	9400 0000h	na

D31..							..D8

D7	D6	D5	D4	D3	D2	D1	D0
Reserved				Node D	Node C	Node B	Node A

This register is used by all nodes to clear interrupts generated by a host on the VME bus.

- To clear VME host interrupts received on its IIOF2 lines, the interrupted node writes a "1" to its assigned bit position in this register. For example, Node B would clear a VME host interrupt received on its IIOF2 line by writing a "1" to bid D1 of this register. Bit D1 is the bit position assigned to Node B.

Only interrupts from a host on the VMEbus (not the CV8 Carrier Board) can generate VME host interrupts to nodes B, C, or D. However, Node A can receive interrupts from a host on the VMEbus *and* from a number of on-board sources. All these interrupts are routed to Node A from the SCV64 chip via its /LIRQ0 pin.

Note: Interrupts received on IIOF2 of Node A must be cleared by an IACK cycle performed by Node A, and by writing a "1" to bit D0 of this register. The IACK cycle is needed to clear the interrupt from the SCV64 chip.

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Node ID Register

Bus	Site A	Site BCD	VME Offset
Address	9500 0000h*	9500 0000h*	na

*Read-only

D31..	..D8
Reserved	

D7	D6	D5	D4	D3	D2	D1	D0
Reserved				Node D	Node C	Node B	Node A

This read-only register is used by all nodes to identify which node they are. Only one bit is set within the Node ID read only register at any time. This allows software programs running on a TIM-40 module to identify the CV8 Carrier Board node in which the module is installed.

- To identify itself, a node reads this register. The bit position that is set to "1" indicates the nodes identity. For example, if bit D2 is set to "1", then the node reading the register would identify itself as Node C.

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VCONTROL Register

Bus	Site A	Site BCD	VME Offset
Address	9600 0000h	na	na

D31..	..D8
Reserved	

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	KFC2	KFC1	KFC0	KSIZE1	KSIZE0	KADDR1	KADDR0

Node A uses this register to control the SCV64 Local Bus for VME64 master accesses. The bits control the state the KSIZE, KFC, and lower two KADDR lines of the SCV64 chip. A "1" sets the line high; a "0" sets the line low. Refer to the *SCV64 User Manual* for further information on the function of these lines.

KADDR[1..0] Sets the lower address bits of the SCV64 local bus.

KSIZE[1..0] Sets the Local Bus Data Transfer Size. This code indicates the number of bytes (including current cycle) to be transferred to complete the operation Directly affects D32, D16, or D8 address modifiers.

KSIZE1	KSIZE0	Data Transfer Size
0	0	4 bytes
1	1	3 bytes
1	0	2 bytes
0	1	1 byte

KFC[2..0] Sets the type of access performed (User or Supervisor Program, or Data accesses). These signals are used during power-up to determine AUTOBAR configuration, and LIRQ2/KIACK pin definition. Directly affects the address modifiers used for the VME64 Master cycle.

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VSTATUS Register

Bus	Site A	Site BCD	VME Offset
Address	9600 0001h*	na	na

*Read Only

D31..	..D8
Reserved	

D7	D6	D5	D4	D3	D2	D1	D0
Reserved			VECTERR	ACCERR	KIPL2	KIPL1	KIPL0

This register return the interrupt levels, interrupt vector status, and cycle status for the VME64 interface as indicated by the associated lines on the SCV64. A "1" indicates that the line is high; a "0" indicates that the line is low. Refer to the *SCV64 User Manual* for further information on the function of these lines.

KIPL[2..0] The state of the CPU Interrupt Priority Level (KIPL) lines from the SCV64 chip. The SCV64 channels all interrupt sources to 7 CPU interrupt levels. The lines are used to encode the 7 CPU interrupt levels.

ACCERR Status of the last bus cycle access made by the SCV64 chip. Set to "1" if there was a bus error.

VECTERR Status of the interrupt vector currently on the local data bus. Set to "1" if the vector is not valid. An invalid auto-vectored interrupt would set this bit, denoting a non-valid vector value on the bus.

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VOFFSET Register

Bus	Site A	Site BCD	VME Offset
Address	9600 0002h*	na	na

*Read Only

D31..	..D8
Reserved	

D7	D6	D5	D4	D3	D2	D1	D0
Reserved			A31	A30	A29	A28	A27

This register returns the value of the VME64 base address as set by the J19 jumper block. The jumpers provide the upper 5 bits of the 32-bit VME64 address. This is the base address location of the CV8 Carrier Board within the VME64 memory map. Refer to the *SCV64 User Manual* for further information on configuring the VME base address within the SCV64 chip.

Note: In the default AUTOBAR mode, the SCV64 fetches the VME64 base address and loads it into its VME base address register upon power up.

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LEDx Registers

Bus	Site A	Site BCD	VME Offset
LED1 Address	9700 0001h	na	na
LED2 Address	9700 0002h	na	na
LED3 Address	9700 0003h	na	na

D31..	..D8
Reserved	

D7	D6	D5	D4	D3	D2	D1	D0
Reserved							LED *x*

These registers are used by Node A to monitor and control the three user defined LEDs on the front panel of the CV8 Carrier Board. Each LED has its own register.

- To turn the LED on, write a "1" to bit D0 of the register corresponding to the LED.
- To turn the LED off, write a "0" to bit D0 of the register corresponding to the LED.
- To determine whether an LED is turned on, read bit D0 of the register corresponding to the LED. If D0 is set to "1", then the LED is on.

Note: The SYSFAIL LED on the front panel is connected directly to the VME SYSFAIL signal. It has no associated register.

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Round Robin Timeslot Register

Bus	Site A	Site BCD	VME Offset
Address	9900 0000h	na	na

D31..	..D8
Reserved	

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Timeslot Period						

This register is used by Node A to control the bus mastering period assigned to a TIM-40 node.

The register stores a 7-bit value [D6..D0] which is loaded into a counter that controls the bus mastering period. This counter is clocked by every second transition of Node A's H1 clock and is reset upon transferring control from a TIM-40 node to a different TIM-40 node. For example, a value of 15 gives a timeslot period of 30 H1 clock cycles from Node A.

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DSP~LINK3 Reset Register

Bus	Site A	Site BCD	VME Offset
Address	9D00 0000h	na	na

D31..	..D8
Reserved	

D7	D6	D5	D4	D3	D2	D1	D0
Reserved							Reset

This register is used by Node A to reset the DSP~LINK3 interface. It is also used to clear the DSP~LINK3 reset. Writing a bit value of 1 in D0 asserts the reset line to the DSP~LINK3 interface.

- To reset the DSP~LINK3 interface, write a "1" to bit D0 of this register.
- To clear the DSP~LINK3 reset, write a "0" to bit D0 of this register.
- To determine whether the DSP~LINK3 interface is in a reset state, read bit D0 of this register. If it is set to "1", then the interface is in a reset state.

Note: The Node A TIM-40 **must** clear the bit (set it to "0") to de-assert the reset line.

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VME64 Slave Reset Register

Bus	Site A	Site BCD	VME Offset
Address	na	na	0300 0000h

D31..	..D8
Reserved	

D7	D6	D5	D4	D3	D2	D1	D0
Reserved							Reset

This register is used by a host on the VME64 bus to reset the CV8 Carrier Board. When this bit is asserted, the following CV8 Carrier Board devices and resources are reset:

- All TIM-40 sites
- LED*x* registers
- VCONTROL register
- Round Robin Time-Slot register
- Host Interrupt Clear register
- JTAG /GRESET line

Once a reset has been asserted, the CV8 Carrier Board is held in reset until it is released from reset through this register. Although the JTAG /GRESET line is asserted upon reset, no other CV8 Carrier Board peripherals are reset.

- To reset the CV8 Carrier Board, a host on the VME64 bus writes a "1" to bit D0 of this register.
- To release the CV8 Carrier Board from reset, a host on the VME64 bus writes a "0" to bit D0 of this register.
- To determine whether the CV8 Carrier Board is being held in reset, a host on the VME64 bus reads the state of bit D0. If bit D0 is set to "1", then the CV8 Carrier Board is being held in reset.

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VME64 Slave /CONFIG Status Register

Bus	Site A	Site BCD	VME Offset
Address	na	na	0400 0000h*

*Read Only

D31..	..D8

D7	D6	D5	D4	D3	D2	D1	D0
Reserved							/CONFIG

A host on the VME64bus uses this register to determine the status of the TIM-40 Node /CONFIG line on the CV8 Carrier Board. All TIM-40 Node have their /CONFIG line tied together and pulled up with a resistor. The /CONFIG line is therefore a active-low logical OR of the /CONFIG lines of all the nodes; it is high unless any of the nodes pulls the /CONFIG line low.

- To determine the state of the CV8 Carrier Board /CONFIG line, a host on the VME64 bus reads bit D0 of this register. If bit D0 is set to "1", then the /CONFIG line is high.

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VME64 Interrupt Set Register

Bus	Site A	Site BCD	VME Offset
Address	na	na	0500 0000h

D31..							..D8
Reserved							

D7	D6	D5	D4	D3	D2	D1	D0
Reserved				Node D	Node C	Node B	Node A

This register is used by a host on the VME64 bus to interrupt any node on the CV8 Carrier Board. It can also be used to determine whether a node has cleared its interrupt, but it *cannot* be used to clear this interrupt from the VME host.

- To interrupt a particular CV8 Carrier Board node, a host on the VME64 bus writes a "1" to the bit (bits D0 to D3) corresponding to the node being interrupted.

- To determine if a node has cleared its particular interrupt, a host on the VME64 bus reads the bit positioning corresponding to that node. If the bit is set to "1", then there is an VME64 interrupt pending on that node which has not been cleared.

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11 Specifications

The CV8 Carrier Board is electrically compliant with the VME64 bus specifications.

Table 14 CV8 Carrier Board Specifications

Current Consumption (no TIM-40 modules)	
+5 Volts	1.3 Amperes
+12 Volts	0 Amperes
-12 Volts	0 Amperes
Power	6.5 Watts
Height	6U
Length	VME type “C”
Width	1 VME slot
Operating Temperature	0ºC to 45ºC

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12 Front Panel Connectors

The CV8 Carrier Board has the following front panel connectors:

- 'C4x COMM Ports (10)
- JTAG IN
- JTAG OUT.
- Serial Port
- Application Specific Pins (option)
- SMB connectors (option)

The location and pin numbering of the connectors is shown in the following figure. A CV8 Carrier Board with the Application Specific Connector option is shown so that the Application Specific Connector pinout can be described. The SMB connector option does not require a pinout designation, as each SMB connector is only a pass through connector to the other side of the front panel.

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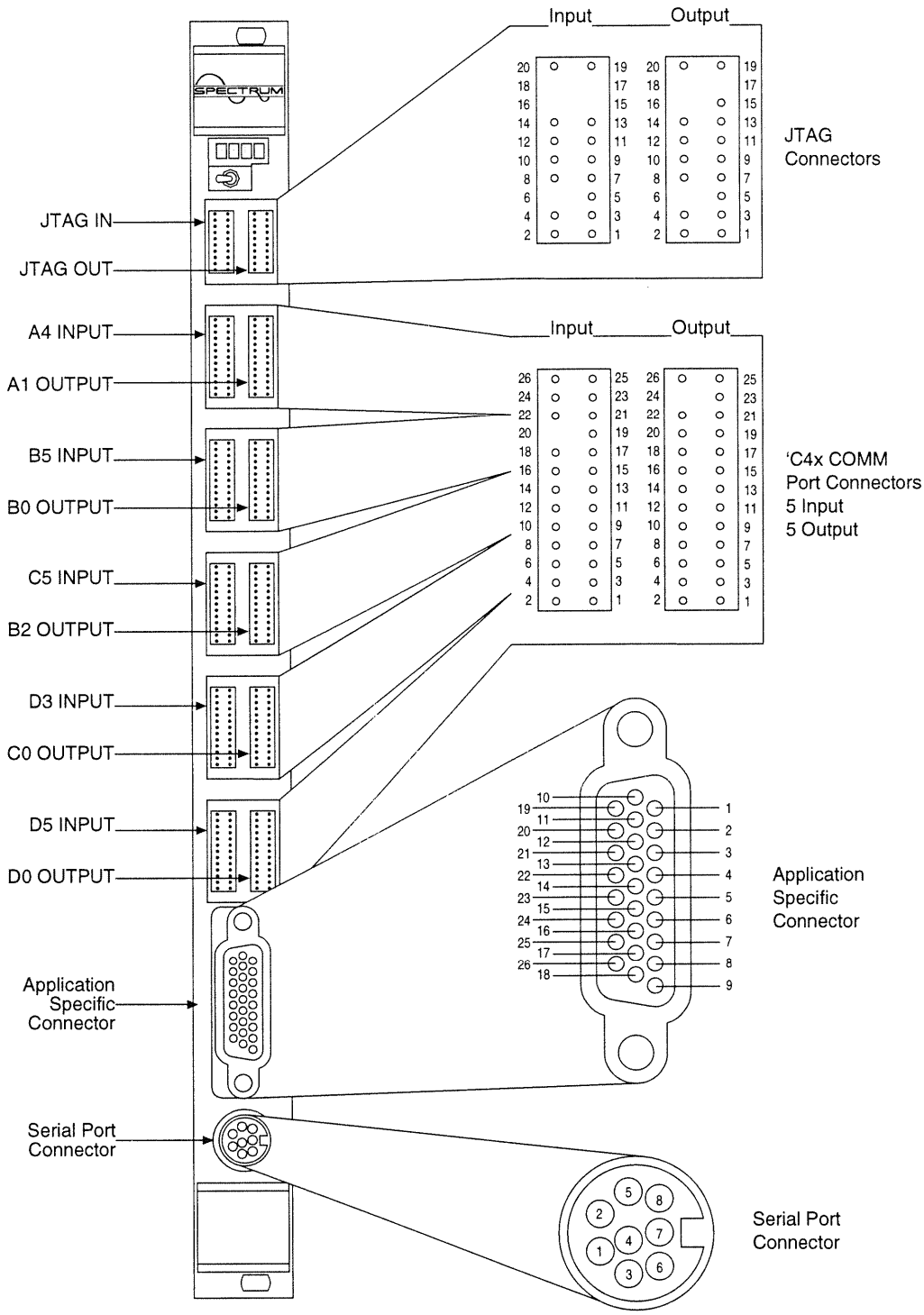


Figure 14 CV8 Front Panel Connectors

Note: Refer to the TIM-40 Specification for a description of the TIM-40 connectors.

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12.1. JTAG Connectors

JTAG connection is available on the front panel by a pair of 20-pin 0.050" high-density connectors (Samtec TMS-110-01-T-D-RA or equivalent).

Table 15 COMM Port Connector Pinouts

JTAG IN			
Pin	Signal	Pin	Signal
1	TMS	2	/TRST
3	TDI	4	GND
5	Presence	6	Key
7	TDO	8	GND
9	TCK_RET	10	GND
11	TCK	12	GND
13	EMU0	14	EMU1
15	Key	16	Key
17	Key	18	Key
19	/CONFIG	20	/GRESET

JTAG OUT			
Pin	Signal	Pin	Signal
1	TMS	2	/TRST
3	TDO	4	GND
5	SENSE	6	Key
7	TDI	8	GND
9	TCK_RET	10	GND
11	TCK	12	GND
13	EMU0	14	EMU1
15	Key	16	N/C
17	Key	18	Key
19	/CONFIG	20	/GRESET

12.2. 'C4x COMM Port Connections

Ten buffered 'C4x COMM Ports from the CV8 Carrier Board are available on the front panel via 26-pin 0.050" pitch high-density connectors (Samtec TMS-113-01-T-D-RA or equivalent). The connectors are keyed to prevent accidental connection of outputs to outputs.

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Table 16 COMM Port Connector Pinouts

Input			
Pin	Signal	Pin	Signal
1	CD0	2	GND
3	CD1	4	GND
5	CD2	6	GND
7	CD3	8	GND
9	CD4	10	GND
11	CD5	12	GND
13	CD6	14	GND
15	CD7	16	GND
17	/CREQ	18	GND
19	/CACK	20	Key
21	/CSTRB	22	GND
23	/CRDY	24	GND
25	DIRIN	26	DIROUT

Output			
Pin	Signal	Pin	Signal
1	CD0	2	GND
3	CD1	4	GND
5	CD2	6	GND
7	CD3	8	GND
9	CD4	10	GND
11	CD5	12	GND
13	CD6	14	GND
15	CD7	16	GND
17	/CREQ	18	GND
19	/CACK	20	GND
21	/CSTRB	22	GND
23	/CRDY	24	Key
25	DIRIN	26	DIROUT

12.3. Application Specific Connector

The Application Specific Connector presents the User Defined Pin (UDP) signals from TIM-40 sites C and D to the front panel. The connector uses a high-density, 26-pin female subminiature D connector (AMP 748481-5 or equivalent). The last two characters indicate the source of the UDP. For example UDP D:5 corresponds to UDP 5 from TIM-40 site D.

Table 17 Application Specific Connector Pinout

Pin	Signal	Pin	Signal	Pin	Signal
1	UDP C:1	10	UDP C:2	19	UDP C:4
2	UDP C:5	11	UDP C:3	20	UDP C:6
3	UDP C:8	12	UDP C:7	21	UDP C:9
4	UDP C:11	13	UDP C:10	22	UDP C:12
5	UDP D:2	14	UDP D:3	23	UDP D:4
6	UDP D:5	15	UDP D:6	24	UDP D:1
7	UDP D:9	16	UDP D:7	25	UDP D:8
8	UDP D:11	17	UDP D:10	26	UDP D:12
9	N/C	18	N/C		

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12.4. Serial Port Connector

The front panel serial port connector uses an 8-pin Mini-DIN connector (AMP 749179-1 or equivalent).

Table 18 Serial Port Connector Pinout

Pin Number	Input / Output	Signal
1	Output	DTR Data Terminal Ready
2	Input	CTS Clear to Send
3	Input	RxD- Received data "-"
4	tied to ground	Signal ground
5	Output	TxD- Transmitted data "-"
6	tied to ground	TxD+ Transmitted data "+"
7	Not connected	N/C
8	tied to ground	RxD+ Received data "+"

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13 On Board Connectors

The CV8 Carrier Board on board connectors consist of the

- P1 and P2 VME backplane connectors
- DSP~LINK3 module and ribbon cable connectors
- Four TIM-40 site connectors
- Peripheral interface connector (PIC)

The following figure shows the location of these connectors.

The DSP~LINK3 signals are routed to rows A and C if the DSP~LINK3 resistor packs RP63 to RP78 (located above the DSP~LINK3 Module Connector) are installed on the CV8 Carrier Board.

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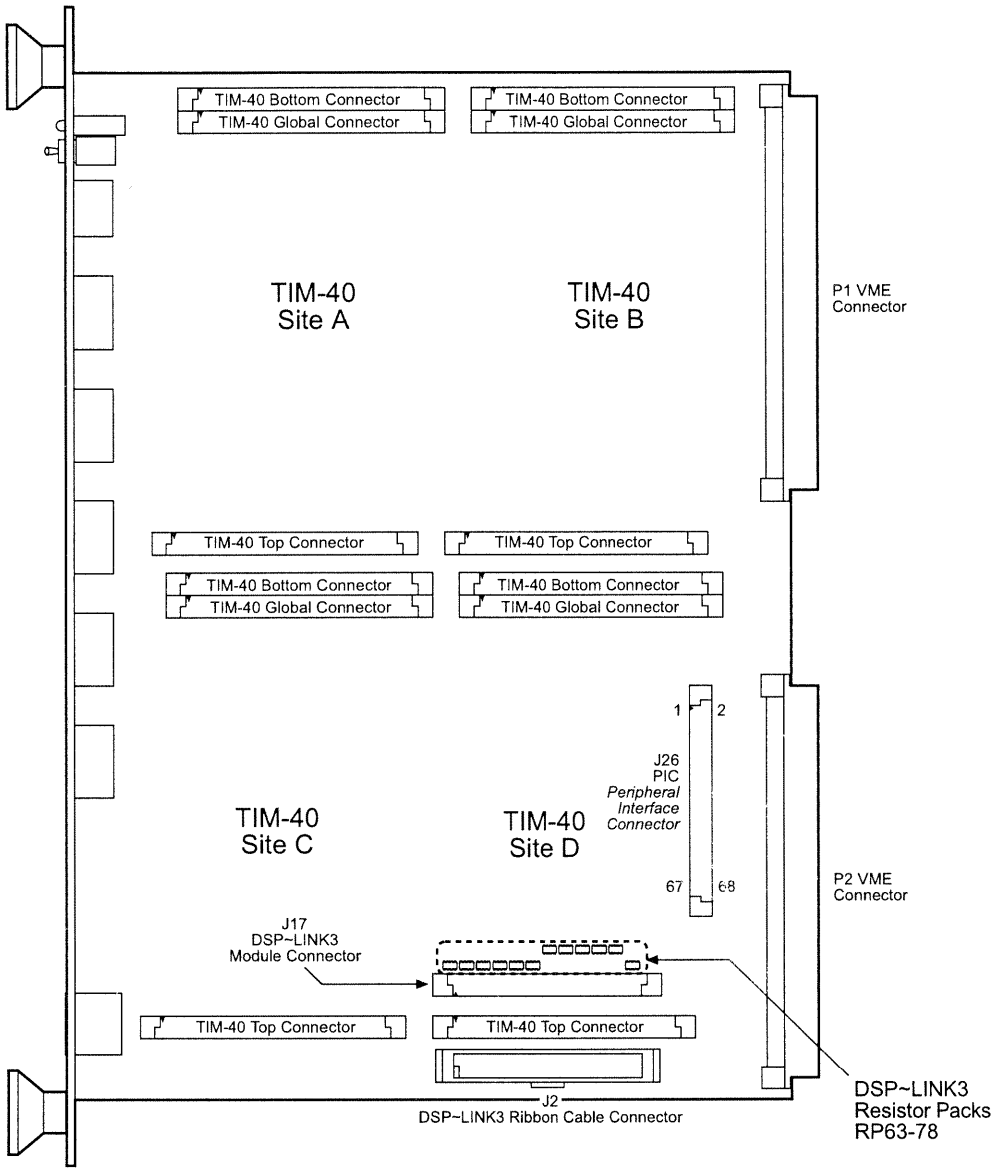


Figure 15 On Board Connectors

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13.1. VME Connector

The P1 VME Connector uses a standard 96 pin DIN 3 row connector.

Table 19 P1 VME Connector Pinout

Pin	Row A Signal	Row B Signal	Row C Signal
1	D00 - I/O	/BBSY	D08 - I/O
2	D01 - I/O	/BCLR	D09 - I/O
3	D02 - I/O	/ACFAIL	D10 - I/O
4	D03 - I/O	/BG0IN	D11 - I/O
5	D04 - I/O	/BG0OUT	D12 - I/O
6	D05 - I/O	/BG1IN	D13 - I/O
7	D06 - I/O	/BG1OUT	D14 - I/O
8	D07 - I/O	/BG2IN	D15 - I/O
9	GND	/BG2OUT	GND
10	SYSCLK - IN	/BG3IN	/SYSFAIL
11	GND	/BG3OUT	/BERR
12	/DS1	/BR0	/SYSRESET
13	/DS0	/BR1	/LWORD
14	/WRITE	/BR2	AM5 - I/O
15	GND	/BR3	A23 - I/O
16	/DTACK	AM0 - I/O	A22 - I/O
17	GND	AM1 - I/O	A21 - I/O
18	/AS	AM2 - I/O	A20 - I/O
19	GND	AM3 - I/O	A19 - I/O
20	/IACK	GND	A18 - I/O
21	/IACKIN	N/C	A17 - I/O
22	/IACKOUT	N/C	A16 - I/O
23	AM4 - I/O	GND	A15 - I/O
24	A07 - I/O	/IRQ7	A14 - I/O
25	A06 - I/O	/IRQ6	A13 - I/O
26	A05 - I/O	/IRQ5	A12 - I/O
27	A04 - I/O	/IRQ4	A11 - I/O
28	A03 - I/O	/IRQ3	A10 - I/O
29	A02 - I/O	/IRQ2	A09 - I/O
30	A01 - I/O	/IRQ1	A08 - I/O
31	-12V	N/C	+12V
32	+5V	+5V	+5V

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13.2. VME P2 Connector

The P2 VME backplane connector is a 5 row, 160-pin DIN connector. It carries:

- P2 signals for the VME64 bus
- User Defined Pin (UDP) signals for TIM-40 sites A and B
- Peripheral Interface Connector signals
- DSP~LINK3 interface signals (optional)

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Table 20 VME P2 Connector Pinout

Pin #	Row Z Signal	Row A Signal	Row B Signal	Row C Signal	Row D Signal
1	UDPB12	App. Spec. IRQ or PIC3*	+5V	DL3A15 or PIC4	UDPB2
2	GND	DL3A14 or PIC5	GND	DL3A13 or PIC6	NC
3	UDPB11	DL3A12 or PIC7	RESERVED	DL3A11 or PIC8	UDPB3
4	GND	DL3A10 or PIC9	A24 - I/O	DL3A9 or PIC10	NC
5	UDPB10	DL3A8 or PIC11	A25 - I/O	DL3A7 or PIC12	UDPB4
6	GND	DL3A6 or PIC13	A26 - I/O	DL3A5 or PIC14	NC
7	UDPB9	DL3A4 or PIC15	A27 - I/O	DL3A3 or PIC16	UDPB5
8	GND	DL3A2 or PIC17	A28 - I/O	DL3A1 or PIC18	NC
9	UDPB8	DL3A0 or PIC19	A29 - I/O	DL3R/W or PIC20	UDPB6
10	GND	/DL3RESET or PIC21	A30 - I/O	GND or PIC22	NC
11	UDPB7	/DL3DSTRB or PIC23	A31 - I/O	GND or PIC24	UDPB1
12	GND	/DL3ASTRB or PIC25	GND	GND or PIC26	NC
13	UDPA11	/DL3RDY or PIC27	+5V	GND or PIC28	UDPA1
14	GND	/DL3INT0 or PIC29	D16 - I/O	/DL3_INT2 or PIC30	NC
15	UDPA10	/DL3INT1 or PIC31	D17 - I/O	/DL3_INT3 or PIC32	UDPA6
16	GND	NC or PIC33	D18 - I/O	NC or PIC34	NC
17	UDPA9	DL3D31 or PIC35	D19 - I/O	DL3D30 or PIC36	UDPA5
18	GND	DL3D29 or PIC37	D20 - I/O	DL3D28 or PIC38	NC
19	UDPA8	DL3D27 or PIC39	D21 - I/O	DL3D26 or PIC40	UDPA4
20	GND	DL3D25 or PIC41	D22 - I/O	DL3D24 or PIC42	NC
21	UDPA7	DL3D23 or PIC43	D23 - I/O	DL3D22 or PIC44	UDPA3
22	GND	DL3D21 or PIC45	GND	DL3D20 or PIC46	NC
23	UDPA12	DL3D19 or PIC47	D24 - I/O	DL3D18 or PIC48	UDPA2
24	GND	DL3D17 or PIC49	D25 - I/O	DL3D16 or PIC50	NC
25	Z25	DL3D15 or PIC51	D26 - I/O	DL3D14 or PIC52	NC
26	GND	DL3D13 or PIC53	D27 - I/O	DL3D12 or PIC54	NC
27	Z27	DL3D11 or PIC55	D28 - I/O	DL3D10 or PIC56	NC
28	GND	DL3D9 or PIC57	D29 - I/O	DL3D8 or PIC58	NC
29	Z29	DL3D7 or PIC59	D30 - I/O	DL3D6 or PIC60	NC
30	GND	DL3D5 or PIC61	D31 - I/O	DL3D4 or PIC62	NC
31	Z31	DL3D3 or PIC63	GND	DL3D2 or PIC64	GND
32	GND	DL3D1 or PIC65	+5V	DL3D0 or PIC66	VPC
I/O = Input / Output, IN = Input, OUT = Output, NC = Not Connected					

*Pin 1 on Row A is configured as the Application Specific Interrupt if JP20 is installed.

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13.3. PIC Connector

The 68-pin PIC connector near TIM-40 site D provides access to the VME64 P2 connector. The connector is a Hirose FX4C-68P-1.27DSA. Pin descriptions are given in the following table.

Table 21 PIC Connector Pinout

Pin Number	VME64 P2 Connector	Pin Number	VME64 P2 Connector
1	GND	2	GND
3	A1 (PIC3)	4	C1 (PIC4)
5	A2 (PIC5)	6	C2 (PIC6)
7	A3 (PIC7)	8	C3 (PIC8)
9	A4 (PIC9)	10	C4 (PIC10)
11	A5 (PIC11)	12	C5 (PIC12)
13	A6 (PIC13)	14	C6 (PIC14)
15	A7 (PIC15)	16	C7 (PIC16)
17	A8 (PIC17)	18	C8 (PIC18)
19	A9 (PIC19)	20	C9 (PIC20)
21	A10 (PIC21)	22	C10 (PIC22)
23	A11 (PIC23)	24	C11 (PIC24)
25	A12 (PIC25)	26	C12 (PIC26)
27	A13 (PIC27)	28	C13 (PIC28)
29	A14 (PIC29)	30	C14 (PIC30)
31	A15 (PIC31)	32	C15 (PIC32)
33	A16 (PIC33)	34	C16 (PIC34)
35	A17 (PIC35)	36	C17 (PIC36)
37	A18 (PIC37)	38	C18 (PIC38)
39	A19 (PIC39)	40	C19 (PIC40)
41	A20 (PIC41)	42	C20 (PIC42)
43	A21 (PIC43)	44	C21 (PIC44)
45	A22 (PIC45)	46	C22 (PIC46)
47	A23 (PIC47)	48	C23 (PIC48)
49	A24 (PIC49)	50	C24 (PIC50)
51	A25 (PIC51)	52	C25 (PIC52)
53	A26 (PIC53)	54	C26 (PIC54)
55	A27 (PIC55)	56	C27 (PIC56)
57	A28 (PIC57)	58	C28 (PIC58)
59	A29 (PIC59)	60	C29 (PIC60)
61	A30 (PIC61)	62	C30 (PIC62)
63	A31 (PIC63)	64	C31 (PIC64)
65	A32 (PIC65)	66	C32 (PIC66)
67	N/C	68	N/C

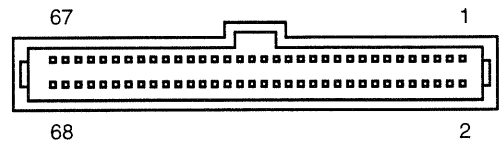
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13.4. DSP~LINK3 Connectors

Connector pinouts for the DSP~LINK3 module and ribbon cable connectors are given in the following tables. Refer to the *DSP~LINK3 Specification* for complete information.

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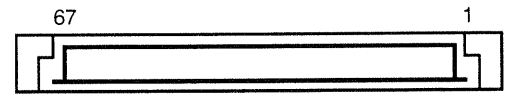
Table 22 DSP~LINK3 Ribbon Cable Connector Pinout



Pin Number	Signal	Pin Number	Signal
1	VCC	2	A15
3	A14	4	A13
5	A12	6	A11
7	A10	8	A9
9	A8	10	A7
11	A6	12	A5
13	A4	14	A3
15	A2	16	A1
17	A0	18	R/W_
19	/RESET	20	GND
21	/DSTRB	22	GND
23	/ASTRB	24	GND
25	/RDY	26	GND
27	/INT0	28	GND
29	/INT1	30	GND
31	/INT2	32	GND
33	/INT3	34	GND
35	D31	36	D30
37	D29	38	D28
39	D27	40	D26
41	D25	42	D24
43	D23	44	D22
45	D21	46	D20
47	D19	48	D18
49	D17	50	D16
51	D15	52	D14
53	D13	54	D12
55	D11	56	D10
57	D9	58	D8
59	D7	60	D6
61	D5	62	D4
63	D3	64	D2
65	D1	66	D0
67	GND	68	RSVD

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Table 23 DSP~LINK3 Module Connector Pinout



Pin Number	Signal	Pin Number	Signal
1	VCC (+5 V)	35	A15
2	A14	36	A13
3	A12	37	A11
4	A10	38	A9
5	A8	39	A7
6	A6	40	A5
7	A4	41	A3
8	A2	42	A1
9	A0	43	R/W_
10	/RESET	44	GND
11	/DSTRB	45	GND
12	/ASTRB	46	GND
13	/RDY	47	GND
14	/INT0	48	/INT2
15	/INT1	49	/INT3
16	D31	50	D30
17	D29	51	D28
18	D27	52	D26
19	D25	53	D24
20	D23	54	D22
21	D21	55	D20
22	D19	56	D18
23	D17	57	D16
24	D15	58	D14
25	D13	59	D12
26	D11	60	D10
27	D9	61	D8
28	D7	62	D6
29	D5	63	D4
30	D3	64	D2
31	D1	65	D0
32	RSVD	66	RSVD
33	VCC (+5 V)	67	VCC (+5 V)
34	+12 V (unfiltered)	68	-12 V (unfiltered)

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Appendix A Device Registers

This appendix briefly describes the default register settings for the SCV64 and 16550 UART chips on the CV8 Carrier Board. The following table shows the default values that are programmed into the registers by the initialization code supplied with the CV8 Carrier Board.

Table 24 SCV64 Register Initialization

Global Bus	VME Offset	Register	Value
000h	000h	DMA Local Address	00000000h
001h	004h	DMA VMEbus Address	00000000h
002h	008h	DMA Transfer Count	00000000h
003h	00Ch	Control and Status	05000800h
004h	010h	VMEbus Slave Base Address	See notes
005h	014h	Rx FIFO Data	Read only
006h	018h	Rx FIFO Address Register	Read only
007h	01Ch	Rx FIFO Control Register	Read only
008h	020h	VMEbus/VSB Bus Select	00000000h
009h	024h	VMEbus Interrupter Vector	00000000h
00Ah	028h	Access Protect Boundary	00000000h
00Bh	02Ch	Tx FIFO Data Output Latch	Read only
00Ch	030h	Tx FIFO Address Output Latch	Read only
00Dh	034h	Tx FIFO AM Code and Control Bit Latch	Read only
00Eh	038h	Location Monitor FIFO Read Port	Read only
00Fh	03Ch	SCV64 Mode Control	2400E401h
010h	040h	Slave A64 Base Address	00000000h
011h	044h	Master A64 Base Address	00000000h
012h	048h	Local Address Generator	Read only
013h	04Ch	DMA VMEbus Transfer Count	Read only
014h to 01Fh	050h to 07Ch	Reserved	
020h	080h	Status Register 0	00000000h
021h	084h	Status Register 1	00000080h
022h	088h	General Control Register	0000001Ch
023h	08Ch	VMEbus Interrupter Requester	00000000h
024h	090h	VMEbus Requester Register	000000CFh
025h	094h	VMEbus Arbiter Register	00000034h
026h	098h	ID Register	Read only
027h	09Ch	Control and Status Register	00000002h
028h	0A0h	Level 7 Interrupt Status Register	Read only

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Table 24 SCV64 Register Initialization

Global Bus	VME Offset	Register	Value
029h	0A4h	Local Interrupt Status Register	Read only
02Ah	0A8h	Level 7 Interrupt Enable Register	00000001h
02Bh	0ACh	Local Interrupt Enable Register	00000001h
02Ch	0B0h	VMEbus Interrupt Enable Register	00000000h
02Dh	0B4h	Local Interrupts 1 and 0 Control Register	000000ABh
02Eh	0B8h	Local Interrupts 3 and 2 Control Register	00000098h
02Fh	0BCh	Local Interrupts 5 and 4 Control Register	000000BAh
030h	0C0h	Miscellaneous control register	00000000h
031h	0C4h	Delay line control register	Dynamically configured by kernel
032h	0C8h	Delay line status register 1	Dynamically configured by kernel
033h	0CCh	Delay line status register 2	Dynamically configured by kernel
034h	0D0h	Delay line status register 3	Dynamically configured by kernel
035h	0D4h	Mailbox register 0	Not used
036h	0D8h	Mailbox register 1	Not used
037h	0DCh	Mailbox register 2	Not used
038h	0E0h	Mailbox register 3	Not used
039h to 07Fh	0E4h to 1FCh	Reserved	

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