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TMS320DM368 Evaluation Module

User's Guide



Literature Number: SPRUI80
August 2016

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About This Manual

This document describes the board level operations of the DM368 Evaluation Module (EVM). The EVM is based on the Texas Instruments TMS320DM368 Processor.

The DM368 Evaluation Module is a table-top card that allows engineers and software developers to evaluate certain characteristics of the DM368 processor, to determine if the processor meets the designers' application requirements. Evaluators can create software to execute onboard, or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The DM368 Evaluation Module is sometimes referred to as the DM368 EVM or EVM.

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing:

equations

!rd = !strobe&rw

Information About Cautions

This book may contain cautions.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage software, hardware, or other equipment. The information in a caution is provided for your protection. Read each caution carefully.

Related Documents, Application Notes and User Guides

Information regarding the TMS320DM368 can be found at the following Texas Instruments website: http://www.ti.com

Table 0-1. Manual History

Revision	History
A	Alpha Release

Table 0-2. Board History

PWB Revision	History
A	Alpha Release

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Introduction to the DM368 EVM

This chapter provides a description of the DM368 EVM, along with the key features and a block diagram of the circuit board.

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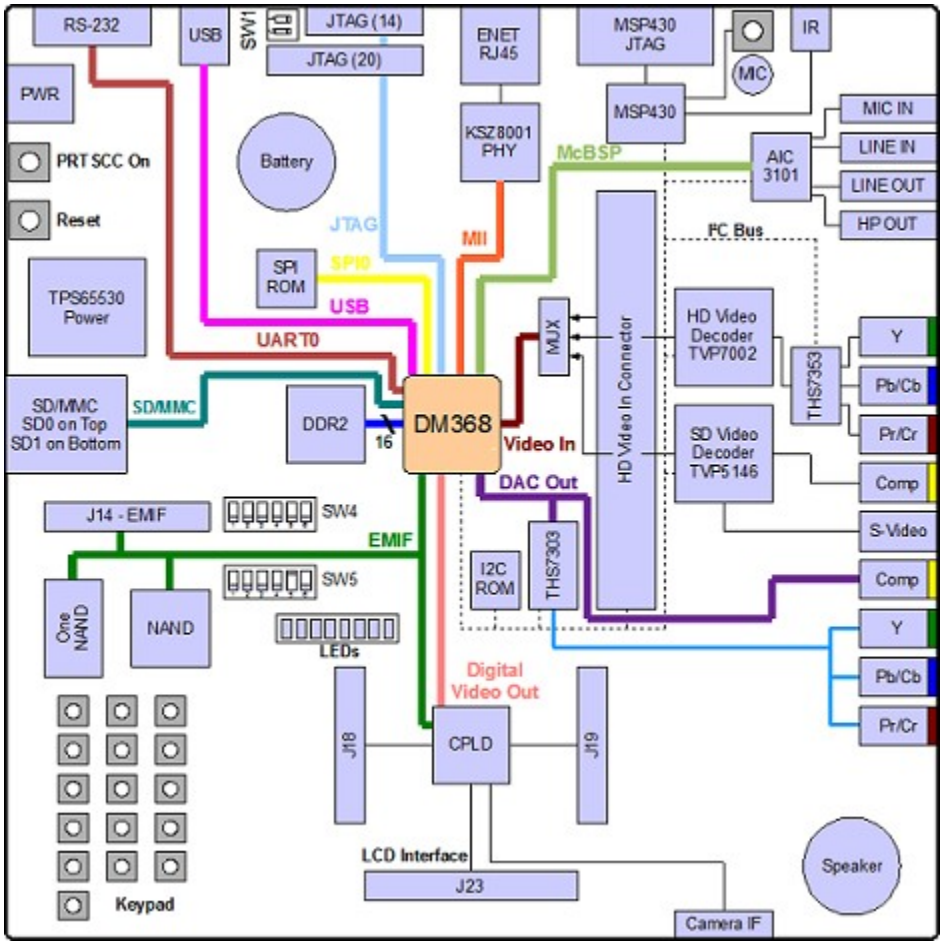
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1.1 Key Features

The DM368 EVM is a standalone development platform that enables users to evaluate and develop applications for the TMS320DM368 processor. Schematics, logic equations, and application notes are available to ease hardware development and reduce time to market.

Figure 1-1. Block Diagram DM368 EVM



The EVM comes with a full complement of onboard devices that suit a wide variety of application environments. Key features include:

- A Texas Instruments DM368 processor with an ARM9 processor operating up to 300 MHz.
- 1 video input port that supports composite or S video (NTSC or PAL formats)
- 1 set of 3 component video inputs that support capture up to 720P resolution
- 1 composite video DAC output (NTSC or PAL formats)
- 1 set of 3 component video DACs that support up to 720P resolution
- 128 Mbytes of DDR2 DRAM
- UART interface
- Micro SD, SD/MMC Card interface
- 2 Gigabytes NAND Flash
- 128 Megabytes of One NAND
- AIC3101 stereo codec
- USB2 interface
- 10/100 MBS RMII Ethernet interface
- SPI EEPROM

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- IR Remote Interface through MSP430
- Configurable boot load options
- 8 user LEDs/16 user push button switches
- Single voltage power supply (+5 V)
- Expansion connectors for daughter card use
- 14-Pin TI JTAG/20-Pin ARM JTAG interfaces

Figure 1-2. DM368 EVM



1.2 Functional Overview of the DM368 EVM

The DM368 on the EVM interfaces to onboard peripherals through the 8/16-bit wide Async EMIF peripheral interface pins. The DDR2 memory is connected to its own dedicated 16-bit wide bus. The Async EMIF bus is also connected to the NAND and One NAND flash.

Onboard video decoders and on-chip encoders interface video streams to the DM368 processor. One composite channel and one set of three component channel encoders and decoders are standard on the EVM. On-screen display functions are implemented in software on the DM368 processor.

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An onboard AIC3101 codec allows the DSP to transmit and receive analog audio signals. The I^2C bus is used for the codec control interface, while the McBSP controls the audio stream. Signal interfacing is done through 3.5-mm audio jacks that correspond to microphone input, headphone output, line input, and line output.

The EVM includes eight user LEDs, 16 user push-button switches, and an IR interface which provides the user with application interaction.

An included +5-V external power supply is used to power the board. Onboard switching voltage regulators provide the +1.2 to 1.35-V CPU core voltage, +3.3 V for peripherals and +1.8 V for DDR2 memory.

The DM368 EVM has a 10/100 ethernet interface, which provides a standard high-speed link to other devices.

The onboard media card interface allows the user to conveniently load and store data from a variety of standard memory card formats. An on-chip real time clock is integrated into the DM368 for time-based applications.

1.3 Basic Operation

The EVM is designed to work with TI's Code Composer Studio™ IDE, or standard GDB tool environments. Code Composer Studio (CCS)communicates with the board through an external JTAG emulator.

1.4 Memory Map

The DM368 processor has a byte-addressable address space. There are some limitations to byte addressing, which are determined by peripheral interconnection to the DM368 device. Program code and data can be placed anywhere in the unified address space. Addresses are multiple sizes, depending on hardware implementation. Refer to the appropriate device data sheets for more details.

Figure 1-3 shows the address space of a generic DM368 processor on the left with specific details of how each region is used on the right. By default, the internal memory sits at the beginning of the address space. Portions of memory can be remapped in software as L2 cache rather than fixed RAM.

The part incorporates a dual EMIF interface. One dedicated EMIF directly interfaces to the DDR2 memory, and the other EMIF has two separate addressable regions called chip-enable spaces (CE0 and CE1). The NAND Flash, one NAND, and CPLD are mapped into these chip-enable spaces.

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Figure 1-3. DM368 EVM Memory Map

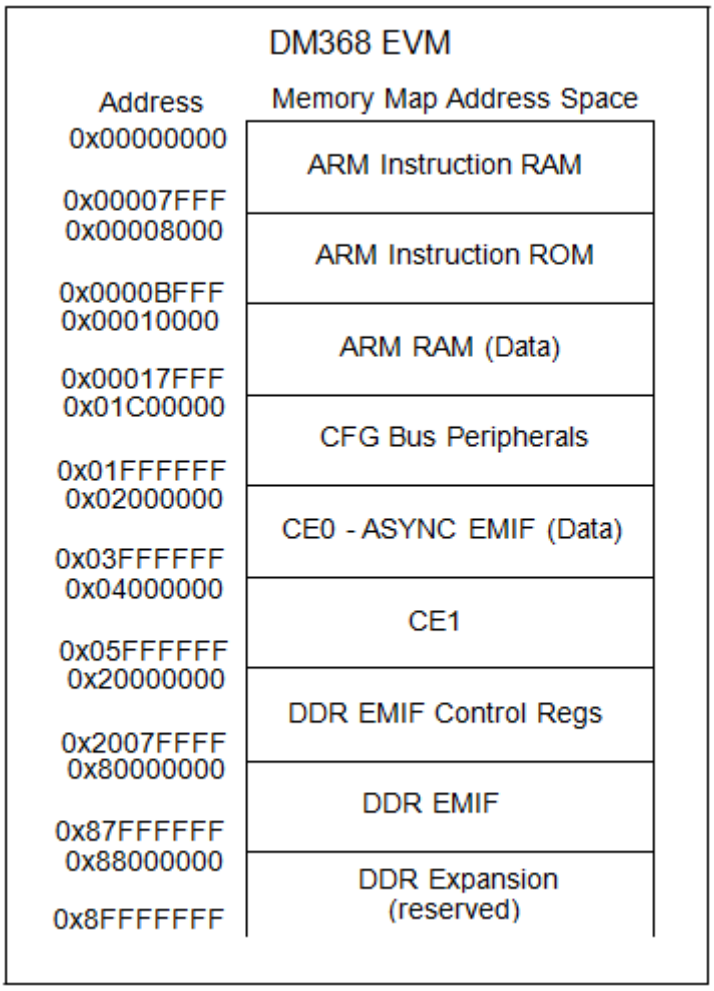
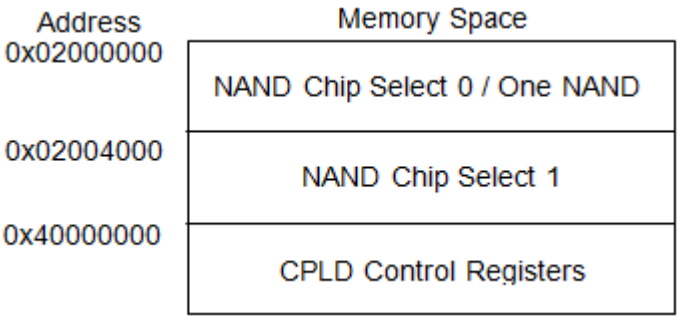


Figure 1-4 shows a break out of the memory spaces.

Figure 1-4. DM368 EVM Chip Enable Memory Space



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1.5 Boot and Configuration Switch Settings

The EVM has a configuration switch that allows users to control the boot and EMIF configuration state of the processor when it is released from reset. The SW4 switch determines the source for processor booting. By default, the switches are configured to NAND Flash Boot. The EMIF configuration switch must be set accordingly. This switch configures the DM368 pin muxing at RESET. The default for the pin muxing is shown in Table 1-1 and Table 1-2. For additional pin muxing requirements, refer to the D365 data sheet.

Table 1-1. SW4, ARM Boot Mode Select

Pos 3	Pos 2	Pos 1	HW Code	Boot Mode
ON	ON	ON	0 0 0	NAND Boot(1)
ON	ON	OFF	0 0 1	ASYNC EMIF
ON	OFF	ON	0 1 0	MMC/SD Boot
ON	OFF	OFF	0 1 1	UART Boot
OFF	ON	ON	1 0 0	USB Boot
OFF	ON	OFF	1 0 1	SPI Boot
OFF	OFF	ON	1 1 0	EMAC Boot
OFF	OFF	OFF	1 1 1	HPI Boot

(1) Default setting.

Table 1-2. SW4, ARM EMIF Configuration Mode Select

Pos 6	Pos 5	Pos 4	HW Code	Configuration Mode
ON	ON	ON	0 0 0	8-bit AEMIF Configuration(1)
ON	ON	OFF	0 0 1	16-bit AEMIF Configuration

(1) Default setting.

1.6 Power Supply

The EVM operates from a single +5-V external power supply connected to the main power input (J7), a 2.5-MM barrel-type plug. Internally, the +5-V input is converted into +1.2 V to 1.35 V, +1.8 V, and +3.3 V, using Texas Instruments TPS65530 power management IC and various linear regulators. The +1.2-V to 1.35-V supply is used for the DSP core, while the +3.3-V supply is used for the I/O buffers of the DSP and other chips on the board. The +1.8-V supply is used for DM368 DDR2 memory, and other on-chip peripherals.

1.7 DM368 User Interface Module with Touch Screen

The DM368 EVM can be used with the DM368 User Interface Module (UIM) with touch screen. The DM368 UIM plugs into the DM368 EVM, and is shown in Figure 1-3. Table 1-3 shows the mating of the connectors on the DM368 EVM to the connectors on the DM368 UIM.

Table 1-3. DM368 – Mating UIM Connectors

DM368 Connector	Mating UIM Connectors
J18	J2
J19	J1
J23	J6

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Board Components

This chapter describes the operation of the major board components on the DM368 EVM.

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2.1 Asynchronous EMIF Interface

An asynchronous 16-bit EMIF with two chip enables divides up the address space and allows for asynchronous accesses on the EVM. This interface connects to the NAND, One NAND, and CPLD registers on the EVM board.

2.1.1 NAND Flash

The DM368 has 2 gigabytes of NAND flash memory mapped into the CE0 space. The NAND flash memory is used primarily for boot loading and file systems on the DM368 EVM. The CE0 selects the device, and must be configured to 8 bits wide when accessing the NAND.

Switch SW5, position 1 (OFF) selects CE0 mapped to NAND. The NAND and One NAND interface share the same CE0 chip select, so only one device can be operational at any given time.

When the NAND flash interface is selected, the spare address lines can be used by the internal DM368 keypad interface. This interface is enabled by setting a control bit in the CPLD to enable the onboard CBTLV switches to the keypad matrix.

2.1.1.1 One NAND

The EVM supports 128 Megabytes of One NAND. This interface is 16 bits wide, and CE0 must be configured for 16-bit wide operation when using One NAND. Switch SW5, position 1 (ON) selects the One NAND device. When the One NAND is selected, the onboard NAND is not available. Because the One NAND uses all the asynchronous EMIF address lines, the on-chip keypad controller on the DM368 cannot be used when the One NAND is selected.

NOTE: In this version of DM368 EVM, One NAND is not populated.

2.1.1.2 CPLD Interface

The DM368 incorporates an Altera EPM2210, 256 Ball Grid Array(BGA) CPLD. The CPLD incorporates a number of internal registers, glue logic, and I/O multiplexing to allow for a flexible development platform. The CPLD is accessed through EMIF CE1. The interface is 8 bits wide. All registers show up as four mirror images in the memory window; due to 32-bit addressing and 8-bit data mapping, BA0 and BA1 are not used in the memory decoder for registers.

Address lines A7-A3, A0, BA0, and BA1 are not used in the decoder, so that these lines can be used by the keypad decoder. The base address of CE1 is 0x0400 0000. Each additional register is accessed on an increment of 0x0000 0008.

The addresses are in the following format: A13, A12, A11, A10, A9, A8, Ax, Ax, Ax, Ax, Ax, A2, A1, Ax, Ax.

The following sections describe the registers and their function. A list of the registers is shown in Table 2-1.

Table 2-1. CPLD Registers

Reg #	Entire Address	Address A13-A8	Address A2-A1	Function	R/W
0	0x0400 0000	0 0 0 0 0 0	0 0	CPLD Version	R
1	0x0400 0008	0 0 0 0 0 0	0 1	Test Register	R,W
2	0x0400 0010	0 0 0 0 0 0	1 0	LED Register	R,W
3	0x0400 0018	0 0 0 0 0 0	1 1	Board Mux Control	R,W
4	0x0400 0400	0 0 0 0 0 1	0 0	Board Switch Register	R
5	0x0400 0408	0 0 0 0 0 1	0 1	Power Control Register	R,W
6	0x0400 0410	0 0 0 0 0 1	1 0	GPIO Video Register	R,W
7	0x0400 0418	0 0 0 0 0 1	1 1	Media Card Status	R
8	0x0400 0800	0 0 0 0 1 0	0 0	DILC Output Pin Mapping	R,W

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Table 2-1. CPLD Registers (continued)

Reg #	Entire Address	Address A13-A8	Address A2-A1	Function	R/W
9	0x0400 0808	0 0 0 0 1 0	0 1	DILC Input Pin Mapping	R
10	0x0400 0810	0 0 0 0 1 0	1 0	Imager Internal I/O Direction Register 0	R,W
11	0x0400 0818	0 0 0 0 1 0	1 1	Imager Internal I/O Mux Register 0	R,W
12	0x0400 0A00	0 0 0 0 1 1	0 0	Imager Internal I/O Mux Register 1	R,W
13	0x0400 0A08	0 0 0 0 1 1	0 1	Imager Internal I/O Direction Register 1	R,W
14	0x0400 0A10	0 0 0 0 1 1	1 0	Imager Internal I/O Mux Register 2	R,W
15	0x0400 0A18	0 0 0 0 1 1	1 1	Imager Internal I/O Mux Register 3	R,W
16	0x0400 1000	0 0 0 1 0 0	0 0	Imager Internal I/O Direction Register 2	R,W
17	0x0400 1008	0 0 0 1 0 0	0 1	Imager Internal I/O Mux Register 4	R,W
18	0x0400 1010	0 0 0 1 0 0	1 0	Imager Internal I/O Mux Register 5	R,W
19	0x0400 1018	0 0 0 1 0 0	1 1	Board RESET Register	R,W
720	0x0400 F800	1 1 1 1 1 0	0 0	CCD Internal I/O Direction Register 1	R,W
721	0x0400 F808	1 1 1 1 1 0	0 1	CCD Internal I/O Read/Write Register 1	R,W
722	0x0400 F810	1 1 1 1 1 0	1 0	CCD Internal I/O Direction Register 2	R,W
723	0x0400 F818	1 1 1 1 1 0	1 1	CCD Internal I/O Read/Write Register 2	R,W
724	0x0400 FC00	1 1 1 1 1 1	0 0	CCD Internal I/O Direction Register 3	R,W
725	0x0400 FC08	1 1 1 1 1 1	0 1	CCD Internal I/O Read/Write Register 3	R,W

2.1.1.2.1 Register 0, CPLD Version

This read only, 8-bit register contains the 4-bit board type and the 4-bit CPLD version for version control. The default value is 0x21 for the DM368 EVM.

2.1.1.2.2 Register 1, Test Register

This read only, 8-bit register has a default value of 0xA5, and can be read and written to test the memory interface.

2.1.1.2.3 Register 2, LED Register

This 8-bit, read/write register controls the user LEDs. A data bit of 0 in each bit location turns on an LED. Similarly, a 1 turns off the LED in each bit position.

2.1.1.2.4 Register 3, Board Mux Control Register

This 8-bit, read/write control register (default = 0x00) controls the keypad, AIC, SD, Ethernet, and Video In multiplexers, as shown in Table 2-2.

Table 2-2. Register 3, Board Mux Control Register Field Descriptions

Bit	Signal	Function
7	EMIF_KEYPAD_CTL	0 = Addresses on muxes (ONE NAND mode) 1 = Addresses are available for keypad
6	SEL_SD1_GPIO_CTL	0 = Enables SD card slot 1 1 = Signals for SD1 card slot 1 go to CPLD imager GPIO
5	SEL_AICn_GPIO_CTL	0 = Enables McBSP signals to AIC3101 codec 1 = McBSP signals go to CPLD for imager GPIO
4	Advanced LCD/Touch panel	0 = Normal mode 1 = Advanced mode for Avnet LCD panel

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Table 2-2. Register 3, Board Mux Control Register Field Descriptions (continued)

Bit	Signal	Function
3	SEL_ENET_GPIO_CTL	0 = Enable Ethernet signals to PHY 1 = Ethernet signals go to CPLD for imager GPIO
2	DECODER_IMAGER_S2_CTL	001 = Selects TVP7002 as input to DM368 video input port 010 = Selects imager as input to DM368 video input port 101 = Selects TVP5146 as input to DM368 video input port
1	DECODER_IMAGER_S1_CTL	
0	DECODER_IMAGER_S0_CTL	

2.1.1.2.5 Register 4, Board Switch Register

This 8-bit, read only register mirrors the values set on switch SW5. These signals are shown in Table 2-3.

Table 2-3. Register 4, Board Switch Register Field Descriptions

Bit	SW5 Position	Signal
7-6	Reserved	N/A
5	1	SEL_NAND_LOW 0 = NAND mapped to CE0 1 =ONE NAND mapped to CE0
4	2	SEL_EXTRA1
3	3	SEL_EXTRA2
2	4	SEL_EXTRA3
1	5	CPU_VSEL1 0 = Vcore at 1.2 V 1 = Vcore at 1.35 V
0	6	SEL_NTAS_MODE

2.1.1.2.6 Register 5, Power Control Register

This 8-bit, read/write register controls onboard voltage regulator functions. The default data value is 0b00000000. These controls are shown in Table 2-4.

Table 2-4. Register 5, Power Control Register Field Descriptions

Bit	Signal	Function
7	LCD_OE_5V	0,1 = Sets U32 FDC6331L Pin to 0,1
6	ENABLE_LCD_3V3	0 = Disables U31 TPS74701 1 = Enables U31 TPS74701
5	Reserved	
4	EN7	0,1 = Sets U14 TPS65530 EN7 pin to 0,1
3	ENAFE	0,1 = Sets U14 TPS65530 ENAFE pin to 0,1
2	SEQ56	0,1 = Sets U14 TPS65530 SEQ56 pin to 0,1
1	EN56	0,1 = Sets U14 TPS65530 EN56 pin to 0,1
0	ENABLE_LCD_15V	0 = Disables U34 TPS61080 register 1 = Enables U34 TPS61080 register

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2.1.1.2.7 Register 6, GPIO Video Register

This 8-bit, read/write register controls the mapping of GPIO30/32/33, VDIN_WE, and DRV_BUS. The default data value is 0b00000000. These controls are shown in Table 2-5.

Table 2-5. Register 6, GPIO Video Register Field Descriptions

Bit	Signal	Function
7-6	Reserved	
5	C_FIELD	1 = DM368 Ball E13 mapped to EXP CONN CCD_FIELD
4	C_WE	1 = DM368 Ball E13 mapped to EXP CONN CCD_WEN
3	24 BIT COLOR	1 = Map GPIO30,32,33 to G1,R0,R1 on LCD EXP CONNS
2	C_WE_FLD_VBUS_DRV	1 = DM368 BALL E13 Drives U4, TPS2065
1	GIO33_VBUS_DRV	1 = GIO33 drives U4, TPS2065
0	VBUS_DRV_ALT	1 = Drives VBUS ENABLE to U4, TPS2065

ENABLE VBUS_DRV (U4, TPS2065) = 1 when any of the following occur:

- When SW5-2 (SEL_EXTRA1_ = 1 for test
- When VBUS_DRV_ALT = 1

ENABLE VBUS_DRV (U4, TPS2065) = DM368 GIO33 when GIO33_VBUS_DRV = 1

ENABLE VBUS_DRV (U4, TPS2065) = DM368 Ball E13 when C_WE_FLD_VBUS_DRV = 1

2.1.1.2.8 Register 7, Media Card Status

This 8-bit, read-only register reads the Insert and Write Protect status of media cards. The functions of these bits are shown in Table 2-6.

Table 2-6. Register 7, Media Card Status Field Descriptions

Bit	Signal	Function
7-6	Reserved	Reads 0
5	SD_MMC_1 WRITE PROTECT	0 = Write Protect
4	SD_MMC_1 INSERT	0 = Insert
3-1	Reserved	Reads 0
0	SD_MMC_0 INSERT	0 = Insert

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2.1.1.2.9 Register 8, DILC Output Pin Mapping

This 8-bit, read/write register maps the DM368 GPIO and SPI2 pins to the DILC connector. The default data value is 0b11111111. The mapping of these pins is shown in Table 2-7.

Table 2-7. Register 8, DILC Output Pin Mapping Field Descriptions

Bit	Signal	Function
7	DILC_DRV_VBUS	Register drives DILC DRV_VBUS pin when bit 6 = 0
6	DILC_DRV_VBUS_IO	0 = Internal register bit 7 drives DILC pin
5	DILC_VBUS_DET_DRV	Register drives DILC pin VBUS_DET when bit 4 = 0
4	DILC_VBUS_DET_IO	0 = Internal register bit 5 drives DILC pin
3	Reserved	N/A
2	CPU_GPIO32_IO	0 = IN, SPI2_DILC drives GIO32 1 = OUT, GIO32 drives SPI2_DILC
1	CPU_GPIO31_IO	0 = IN, SPI2_DILC drives GIO31 1 = OUT, GIO31 drives SPI2_DILC
0	CPU_GPIO30_IO	0 = IN, SPI2_DILC drives GIO30 1 = OUT, GIO30 drives SPI2_DILC

2.1.1.2.10 Register 9, DILC Input Pin Mapping

This 8-bit, read-only register maps the DILC pins to read contents on this register. The mapping of these pins is shown in Table 2-8.

Table 2-8. Register 9, DILC Input Pin Mapping Field Descriptions

Bit	Function
7	Reserved
6	Reads value of DILC connector pin GIO_DILC_DRV_VBUS1
5	Reads value of DILC connector pin GIO_DILC_DRV_DET
4	Reserved
3	Reads value of DILC connector pin GIO_DILC_DOCK_DET
2	Reads value of DILC connector pin GIO_DILC_CAM_PWR_DECT
1	Reads value of DILC connector pin GIO_DILC_AVJ_DET
0	Reads value of DILC connector pin GIO_DILC_CHG_CTL

2.1.1.2.11 Register 10, Imager Internal I/O Direction Register 0

This 8-bit, read/write register controls DM368 GPIO to IMAGER connector pin input and output mapping. The default data value is 0b11111111. This mapping is shown in Table 2-9.

Table 2-9. Register 10, Imager Internal I/O Direction Register 0 Field Descriptions

Bit	Function	Mapping
7	0 = GPIO_MD8 to DM368 pin	0 = Outputs 1 = DM368 pins are inputs
6	0 = GPIO_MD7 to DM368 pin	0 = Outputs 1 = DM368 pins are inputs
5	0 = GPIO_MD6 to DM368 pin	0 = Outputs 1 = DM368 pins are inputs
4	0 = GPIO_MD5 to DM368 pin	0 = Outputs 1 = DM368 pins are inputs

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Table 2-9. Register 10, Imager Internal I/O Direction Register 0 Field Descriptions (continued)

Bit	Function	Mapping
3	0 = GPIO_MD4 to DM368 pin	0 = Outputs 1 = DM368 pins are inputs
2	0 = GPIO_MD3 to DM368 pin	0 = Outputs 1 = DM368 pins are inputs
1	0 = SPI4_SDI_GPIO_MD2 to DM368 pin	0 = Outputs 1 = DM368 pins are inputs
0	0 = GPIO_MD1 to DM368 pin	0 = Outputs 1 = DM368 pins are inputs

2.1.1.2.12 Register 11, Internal I/O Mux Register 0

This 8-bit, read/write register controls DM368 GPIO Muxing to IMAGER connector pin input. The default data is 0b00000000. Table 2-10 shows this muxing.

Table 2-10. Register 11, Internal I/O Mux Register 0 Field Descriptions

Bit	Muxing
7	0 = GPIO_MD4 MUX SELB
6	0 = GPIO_MD4 MUX SELA
5	0 = GPIO_MD3 MUX SELB
4	0 = GPIO_MD3 MUX SELA
3	0 = SPI4_SDI_GPIO_MD2 MUX SELB
2	0 = SPI4_SDI_GPIO_MD2 MUX SELA
1	0 = GPIO_MD1 MUX SELB
0	0 = GPIO_MD1 MUX SELA

2.1.1.2.13 Register 12, Internal I/O Mux Register 1

This 8-bit, read/write register controls DM368 GPIO Muxing to IMAGER connector pin input. The default data is 0b00000000. Table 2-11 shows this muxing.

Table 2-11. Register 12, Internal I/O Mux Register 1 Field Descriptions

Bit	Muxing
7	0 = GPIO_MD8 MUX SELB
6	0 = GPIO_MD8 MUX SELA
5	0 = GPIO_MD7 MUX SELB
4	0 = GPIO_MD7 MUX SELA
3	0 = GPIO_MD6 MUX SELB
2	0 = GPIO_MD6 MUX SELA
1	0 = GPIO_MD5 MUX SELB
0	0 = GPIO_MD5 MUX SELA

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2.1.1.2.14 Register 13, Imager Internal I/O Direction Register 1

This 8-bit, read/write register controls DM368 GPIO to IMAGER connector pin input and output mapping. The default data is 0b00000000. This mapping is shown in Table 2-12.

Table 2-12. Register 13, Imager Internal I/O Direction Register 1 Field Descriptions

Bit	Function	Mapping
7	0 = GPIO_MD16 to DM368 pin	0 = Outputs 1 = DM368 pins are inputs
6	0 = GPIO_MD15 to DM368 pin	0 = Outputs 1 = DM368 pins are inputs
5	0 = GPIO_MD14 to DM368 pin	0 = Outputs 1 = DM368 pins are inputs
4	0 = GPIO_MD13 to DM368 pin	0 = Outputs 1 = DM368 pins are inputs
3	0 = GPIO_MD12 to DM368 pin	0 = Outputs 1 = DM368 pins are inputs
2	0 = GPIO_MD11 to DM368 pin	0 = Outputs 1 = DM368 pins are inputs
1	0 = GPIO_MD10 to DM368 pin	0 = Outputs 1 = DM368 pins are inputs
0	0 = GPIO_MD9 to DM368 pin	0 = Outputs 1 = DM368 pins are inputs

2.1.1.2.15 Register 14, Imager Internal I/O Mux Register 2

This 8-bit, read/write register controls DM368 GPIO Muxing to IMAGER connector pin input. The default data is 0b00000000. Table 2-13 shows this muxing.

Table 2-13. Register 14, Imager Internal I/O Mux Register 2 Field Descriptions

Bit	Muxing
7	0 = GPIO_MD12 MUX SELB
6	0 = GPIO_MD12 MUX SELA
5	0 = GPIO_MD11 MUX SELB
4	0 = GPIO_MD11 MUX SELA
3	0 = GPIO_MD10 MUX SELB
2	0 = GPIO_MD10 MUX SELA
1	0 = GPIO_MD9 MUX SELB
0	0 = GPIO_MD9 MUX SELA

2.1.1.2.16 Register 15, Imager Internal I/O Mux Register 3

This 8-bit, read/write register controls DM368 GPIO Muxing to IMAGER connector pin input. The default data is 0b00000000. Table 2-14 shows this muxing.

Table 2-14. Register 15, Imager Internal I/O Mux Register 3 Field Descriptions

Bit	Muxing
7	0 = GPIO_MD16 MUX SELB
6	0 = GPIO_MD16 MUX SELA
5	0 = GPIO_MD15 MUX SELB
4	0 = GPIO_MD15 MUX SELA

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Table 2-14. Register 15, Imager Internal I/O Mux Register 3 Field Descriptions (continued)

Bit	Muxing
3	0 = GPIO_MD14 MUX SELB
2	0 = GPIO_MD14 MUX SELA
1	0 = GPIO_MD13 MUX SELB
0	0 = GPIO_MD13 MUX SELA

2.1.1.2.17 Register 16, Imager Internal I/O Direction Register 3

This 8-bit, read/write register controls DM368 GPIO to IMAGER connector pin input and output mapping. The default data is 0b00000000. This mapping is shown in Table 2-15.

Table 2-15. Register 16, Imager Internal I/O Direction Register 3 Field Descriptions

Bit	Function	Mapping
7	Reserved	
6	0 = CCD_DDS_RST to DM368 pin	0 = Outputs 1 = DM368 pins are inputs
5	0 = PWM_CCD_SUB to DM368 pin	0 = Outputs 1 = DM368 pins are inputs
4	0 = GPIO_TACH to DM368 pin	0 = Outputs 1 = DM368 pins are inputs
3	0 = GPIO_MST_SLV to DM368 pin	0 = Outputs 1 = DM368 pins are inputs
2	0 = GPIO_MD19 to DM368 pin	0 = Outputs 1 = DM368 pins are inputs
1	0 = GPIO_MD18 to DM368 pin	0 = Outputs 1 = DM368 pins are inputs
0	0 = GPIO_MD17 to DM368 pin	0 = Outputs 1 = DM368 pins are inputs

2.1.1.2.18 Register 17, Imager Internal I/O Mux Register 4

This 8-bit, read/write register controls DM368 GPIO Muxing to IMAGER connector pin input. The default data is 0b00000000. Table 2-16 shows this muxing.

Table 2-16. Register 17, Imager Internal I/O Mux Register 4 Field Descriptions

Bit	Muxing
7	0 = GPIO__MS T_SLV MUX SELB
6	0 = GPIO MST_SLV MUX SELA
5	0 = GPIO_MD19 MUX SELB
4	0 = GPIO_MD19 MUX SELA
3	0 = GPIO_MD18 MUX SELB
2	0 = GPIO_MD18 MUX SELA
1	0 = GPIO_MD17 MUX SELB
0	0 = GPIO_MD17 MUX SELA

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2.1.1.2.19 Register 18, Imager Internal I/O Mux Register 5

This 8-bit, read/write register controls DM368 GPIO Muxing to IMAGER connector pin input. The default data is 0b00000000. Table 2-17 shows this muxing.

Table 2-17. Register 18, Imager Internal I/O Mux Register 5 Field Descriptions

Bit	Muxing
7-6	Reserved
5	0 = CCD_DDS_RST MUX SELB
4	0 = CCD_DDS_RST MUX SELA
3	0 = PWM_CCD_SUB MUX SELB
2	0 = PWM_CCD_SUB MUX SELA
1	0 = GPIO_TACH MUX SELB
0	0 = GPIO_TACH MUX SELA

2.1.1.2.20 Imager Multiplexer Mapping

The CPLD GPIO functions are incorporated through the CPLD control registers mapping selected CPLD and imager pins to the DM368 GPIO. Each CPLD mapping function consists of 1-bit direction control and 2 bits of multiplexer control. Most multiplexing has only one or two options, but the 2 bits in the multiplexing control allow the expansion of options for later revisions.

Many of the I/O bits are shared with other onboard functions, and are selected in interface groups through the CBT control bits in CPLD Register 3, as shown in Table 2-18.

Imager IO Dir Control selects the direction for the CPLD pin mapping to imager connection mapping. The definition of input is Input-to-CPLD, thus, output from connector; the definition of output is output from CPLD, thus, input to the connector. All DM368 I/O bits mapped by the multiplexer must be mapped to match the imager IO direction control. That is, if the CPLD is selected as an input, the corresponding mapping pin selected on the DM368 should be selected as an input.

Table 2-18. Imager Multiplexer Mapping

Pin	CPLD Imager IO Dir Bit	Imager Name	Imager-Mux Bit	Mux Selection (0)(1)	Requires CBT selection over-ride (CPLD Reg and bit)	Mux Selection (0)(1)	Requires CBT selection over-ride (CPLD Reg and bit)
	None (OUTPUT)	SPI4_CLK	None	SPI4_CLK			
	None (OUTPUT)	SPI4_SDO	None	SPI4_SDO			
B16	cpld_reg16(6)	CCD-RST	cpld-reg18(5)(4)	GIO3	Yes, cpld_reg3(3)	GIO40	Yes, cpld_reg3(6)
B15	cpld_reg16(5)	CCD-SUB	cpld-reg18(3)(2)	GIO92	Yes, cpld_reg3(2)(1)(0)	GIO92	Yes, cpld_reg3(2)(1)(0)
C14	cpld_reg16(4)	GPIO-TACH	cpld-reg18(1)(0)	GIO1	Yes, cpld_reg3(3)	GIO38	Yes, cpld_reg3(6)
C8	cpld_reg16(3)	MST-SLV	cpld-reg17(7)(6)	GIO35	No	GIO35	No
C6	cpld_reg16(2)	GPIO-MD19	cpld-reg17(5)(4)	GIO37	No	GIO37	No
C7	cpld_reg16(1)	GPIO-MD18	cpld-reg17(3)(2)	GIO31	No	GIO31	No
C9	cpld_reg16(0)	GPIO-MD17	cpld-reg17(1)(0)	GIO87	Yes, cpld_reg3(2)(1)(0)	GIO87	Yes, cpld_reg3(2)(1)(0)
C10	cpld_reg13(7)	GPIO-MD16	cpld-reg15(7)(6)	GIO44	Yes, cpld_reg3(5)	GIO44	Yes, cpld_reg3(5)
C11	cpld_reg13(6)	GPIO-MD15	cpld-reg15(5)(4)	GIO45	Yes, cpld_reg3(5)	GIO45	Yes, cpld_reg3(5)
C12	cpld_reg13(5)	GPIO-MD14	cpld-reg15(3)(2)	GIO46	Yes, cpld_reg3(5)	GIO46	Yes, cpld_reg3(5)
C13	cpld_reg13(4)	GPIO-MD13	cpld-reg15(1)(0)	GIO47	Yes, cpld_reg3(5)	GIO47	Yes, cpld_reg3(5)

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Table 2-18. Imager Multiplexer Mapping (continued)

Pin	CPLD Imager IO Dir Bit	Imager Name	Imager-Mux Bit	Mux Selection (0)(1)	Requires CBT selection over-ride (CPLD Reg and bit)	Mux Selection (0)(1)	Requires CBT selection over-ride (CPLD Reg and bit)
C15	cpld_reg13(3)	GPIO-MD12	cpld-reg14(7)(6)	GIO88	Yes, cpld_reg3(2)(1)(0)	GIO88	Yes, cpld_reg3(2)(1)(0)
C16	cpld_reg13(2)	GPIO-MD11	cpld-reg14(5)(4)	GIO89	Yes, cpld_reg3(2)(1)(0)	GIO89	Yes, cpld_reg3(2)(1)(0)
B1	cpld_reg13(1)	GPIO-MD10	cpld-reg14(3)(2)	GIO86	Yes, cpld_reg3(2)(1)(0)	GIO86	Yes, cpld_reg3(2)(1)(0)
B2	cpld_reg13(0)	GPIO-MD9	cpld-reg14(1)(0)	GIO85	Yes, cpld_reg3(2)(1)(0)	GIO85	Yes, cpld_reg3(2)(1)(0)
B3	cpld_reg10(7)	GPIO-MD8	cpld-reg12(7)(6)	GIO48	Yes, cpld_reg3(5)	GIO48	Yes, cpld_reg3(5)
B4	cpld_reg10(6)	GPIO-MD7	cpld-reg12(5)(4)	GIO91	Yes, cpld_reg3(2)(1)(0)	GIO91	Yes, cpld_reg3(2)(1)(0)
B11	cpld_reg10(5)	GPIO-MD6	cpld-reg12(3)(2)	GIO90	Yes, cpld_reg3(2)(1)(0)	GIO90	Yes, cpld_reg3(2)(1)(0)
B12	cpld_reg10(4)	GPIO-MD5	cpld-reg12(1)(0)	GIO49	Yes, cpld_reg3(5)	GIO49	Yes, cpld_reg3(5)
B13	cpld_reg10(3)	GPIO-MD4	cpld-reg11(7)(6)	GIO2	Yes, cpld_reg3(3)	GIO39	Yes, cpld_reg3(6)
B17	cpld_reg10(2)	GPIO-MD3	cpld-reg11(5)(4)	GIO4	Yes, cpld_reg3(3)	GIO41	Yes, cpld_reg3(6)
B18	cpld_reg10(1)	SPI4_SDI_GPIO_MD2	cpld-reg11(3)(2)	GIO5	Yes, cpld_reg3(3)	GIO42	Yes, cpld_reg3(6)
A4	cpld_reg10(0)	GPIO-MD1	cpld-reg11(1)(0)	GIO6	Yes, cpld_reg3(3)	GIO43	Yes, cpld_reg3(6)

2.1.1.2.21 Register 19, Board RESET/EXTCLK Select Register

This 8-bit, read/write register allows the user to select reset to major external peripherals and select an external clock for the DM368 EXT PIN (B19). The default data is 0b00000000. Table 2-19 shows the mapping of these bits.

Table 2-19. Register 19, Board RESET/EXTCLK Select Register Field Descriptions

Bit	RESET Signal	State Action
7	EXTCLK_ENABLE	1 = Enable CPLD to drive EXTCLK 0 = Disable EXTCLK, tristate PLD drive of EXTCLK
6	EXT_CLK_SEL1	00 = Select 9.28 MHz 01 = Select 18.56 MHz 10 = Select 37.125 MHz 11 = Select 74.2 5MHz
5	EXT_CLK_SEL0	
4	CCD_RESET	1 = CCD_DDS_RST 0 = CCD_DDS_RST driven low when mux output is selected
3	ETHERNET_RESET	1 = Force reset to Logic 0 0 = Map reset to CPLD inputs
2	TVP7002_RESET	1 = Force reset to Logic 0 0 = Map reset to CPLD inputs
1	AIC3106_RESET	1 = Force reset to Logic 0 0 = Map reset to CPLD inputs

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Table 2-19. Register 19, Board RESET/EXTCLK Select Register Field Descriptions (continued)

Bit	RESET Signal	State Action
0	TVP5146_RESET	1 = Force reset to Logic 0 0 = Map reset to CPLD inputs

The external clock on the DM368 CPLD is 74.25 MHz. This clock can be divided and input into the DM368 EXTCLK pin (B19).

2.1.1.2.22 Register 20, Interrupt Select Register

This 8-bit, read/write register controls the interrupt source to GPIO0 of the DM368 processor. The default data is 0b00000000. Table 2-20 shows the mapping of these bits.

Table 2-20. Register 20, Interrupt Select Register Field Descriptions

Bit	Muxing
7-2	Reserved
1	0 = selects CPLD_CONN_GPIO7
0	1 =selects MSP430_int

When 00 is selected on bits 0 and 1, CPLD Register 3 (4) selects source of interrupt.

2.1.1.2.23 Register 720, CCD Internal I/O Direction Register 1

This 8-bit, read/write register controls CPLD GPIO to CCD Connector pin input and output mapping. The default data is 0b11111111. Table 2-21 shows the mapping of these bits.

Table 2-21. Register 720, CCD Internal I/O Direction Register 1 Field Descriptions

Bit	Signal	State Action
7	0 = GPIO_0.7DIR	0 = Outputs, 1 = Inputs
6	0 = GPIO_0.6DIR	0 = Outputs, 1 = Inputs
5	0 = GPIO_0.5DIR	0 = Outputs, 1 = Inputs
4	0 = GPIO_0.4DIR	0 = Outputs, 1 = Inputs
3	0 = GPIO_0.3DIR	0 = Outputs, 1 = Inputs
2	0 = GPIO_0.2DIR	0 = Outputs, 1 = Inputs
1	0 = GPIO_0.1DIR	0 = Outputs, 1 = Inputs
0	0 = GPIO_0.0DIR	0 = Outputs, 1 = Inputs

2.1.1.2.24 Register 721, CCD Internal I/O Read/Write Register 1

This 8-bit, read/write register controls CPLD GPIO input on read, and output value on write. The default data is 0b00000000. Table 2-22 shows the mapping of these bits.

Table 2-22. Register 721, CCD Internal I/O Read/Write Register 1 Field Descriptions

Bit	Signal	State Action
7	0 = GPIO_0.7	Write bit when DIR = 0 Read bit when DIR = 1
6	0 = GPIO_0.6	Write bit when DIR = 0 Read bit when DIR = 1
5	0 = GPIO_0.5	Write bit when DIR = 0 Read bit when DIR = 1

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Table 2-22. Register 721, CCD Internal I/O Read/Write Register 1 Field Descriptions (continued)

Bit	Signal	State Action
4	0 = GPIO_0.4	Write bit when DIR = 0 Read bit when DIR = 1
3	0 = GPIO_0.3	Write bit when DIR = 0 Read bit when DIR = 1
2	0 = GPIO_0.2	Write bit when DIR = 0 Read bit when DIR = 1
1	0 = GPIO_0.1	Write bit when DIR = 0 Read bit when DIR = 1
0	0 = GPIO_0.0	Write bit when DIR = 0 Read bit when DIR = 1

2.1.1.2.25 Register 722, CCD Internal I/O Direction Register 2

This 8-bit, read/write register controls CPLD GPIO to CCD Connector pin input and output mapping. The default data is 0b11111111. Table 2-23 shows the mapping of these bits.

Table 2-23. Register 722, CCD Internal I/O Direction Register 2 Field Descriptions

Bit	Signal	State Action
7	0 = GPIO_1.7DIR	0 = Outputs, 1 = Inputs
6	0 = GPIO_1.6DIR	0 = Outputs, 1 = Inputs
5	0 = GPIO_1.5DIR	0 = Outputs, 1 = Inputs
4	0 = GPIO_1.4DIR	0 = Outputs, 1 = Inputs
3	0 = GPIO_1.3DIR	0 = Outputs, 1 = Inputs
2	0 = GPIO_1.2DIR	0 = Outputs, 1 = Inputs
1	0 = GPIO_1.1DIR	0 = Outputs, 1 = Inputs
0	0 = GPIO_1.0DIR	0 = Outputs, 1 = Inputs

2.1.1.2.26 Register 723, CCD Internal I/O Read/Write Register 2

This 8-bit, read/write register controls CPLD GPIO input on read, and out value on write. The default data is 0b00000000. Table 2-24 shows the mapping of these bits.

Table 2-24. Register 723, CCD Internal I/O Read/Write Register 2 Field Descriptions

Bit	Signal	State Action
7	0 = GPIO_0.7	Write bit when DIR = 0 Read bit when DIR = 1
6	0 = GPIO_0.6	Write bit when DIR = 0 Read bit when DIR = 1
5	0 = GPIO_0.5	Write bit when DIR = 0 Read bit when DIR = 1
4	0 = GPIO_0.4	Write bit when DIR = 0 Read bit when DIR = 1
3	0 = GPIO_0.3	Write bit when DIR = 0 Read bit when DIR = 1
2	0 = GPIO_0.2	Write bit when DIR = 0 Read bit when DIR = 1

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Table 2-24. Register 723, CCD Internal I/O Read/Write Register 2 Field Descriptions (continued)

Bit	Signal	State Action
1	0 = GPIO_0.1	Write bit when DIR = 0 Read bit when DIR = 1
0	0 = GPIO_0.0	Write bit when DIR = 0 Read bit when DIR = 1

2.1.1.2.27 Register 724, CCD Internal I/O Direction Register 3

This 8-bit, read/write register controls CPLD GPIO to CCD Connector pin input and output mapping. The default data is 0b11111111. Table 2-25 shows the mapping of these bits.

Table 2-25. Register 724, CCD Internal I/O Direction Register 3 Field Descriptions

Bit	Signal	State Action
7	0 = GPIO_2.7DIR	0 = Outputs, 1 = Inputs
6	0 = GPIO_2.6DIR	0 = Outputs, 1 = Inputs
5	0 = GPIO_2.5DIR	0 = Outputs, 1 = Inputs
4	0 = GPIO_2.4DIR	0 = Outputs, 1 = Inputs
3	0 = GPIO_2.3DIR	0 = Outputs, 1 = Inputs
2	0 = GPIO_2.2DIR	0 = Outputs, 1 = Inputs
1	0 = GPIO_2.1DIR	0 = Outputs, 1 = Inputs
0	0 = GPIO_2.0DIR	0 = Outputs, 1 = Inputs

2.1.1.2.28 Register 725, CCD Internal I/O Read/Write Register 3

This 8-bit, read/write register controls CPLD GPIO to CCD input on read, and out value on write. The default data is 0b00000000. Table 2-26 shows the mapping of these bits.

Table 2-26. Register 725, CCD Internal I/O Read/Write Register 3 Field Descriptions

Bit	Signal	State Action
7	0 = GPIO_0.7	Write bit when DIR = 0 Read bit when DIR = 1
6	0 = GPIO_0.6	Write bit when DIR = 0 Read bit when DIR = 1
5	0 = GPIO_0.5	Write bit when DIR = 0 Read bit when DIR = 1
4	0 = GPIO_0.4	Write bit when DIR = 0 Read bit when DIR = 1
3	0 = GPIO_0.3	Write bit when DIR = 0 Read bit when DIR = 1
2	0 = GPIO_0.2	Write bit when DIR = 0 Read bit when DIR = 1
1	0 = GPIO_0.1	Write bit when DIR = 0 Read bit when DIR = 1
0	0 = GPIO_0.0	Write bit when DIR = 0 Read bit when DIR = 1

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2.1.2 Keypad Interface

The DM368 has an internal keypad controller. The keypad interface is multiplexed with the address lines on the asynchronous EMIF. CBTLV multiplexers are used to redirect the keypad interface to the keypad matrix. This interface can only be used when CE0 is in the NAND configuration. A control bit in the CPLD enables the Mux select on the CBTLV multiplexers. The 16-bit switch keypad matrix is set up on a 4 × 4 matrix on the EVM. The mapping of the switches are shown in Table 2-27.

Table 2-27. Keypad Layout

	Key-A0	Key-A0	Key-A1	Key-A1
Key-B0	SW6 / KEY 2	SW7 / LEFT	SW8 / EXIT	SW9 / DOWN
Key-B0	SW10 / ENTER	SW11 / UP	SW12 KEY 1	SW13 / RIGHT
Key-B1	SW14 / MENU	SW15 / REC	SW16 / REW	SW17 / SKIP-
Key-B1	SW18 / STOP	SW19 / FF	SW20 / SKIP+	SW2 / PLAY/ PAUSE

2.1.3 DDR2 Memory Interface

The DM368 device incorporates a dedicated 16-bit wide DDR2 memory bus. The EVM uses a single 1-gigabit 16-bit wide memory on this bus, for a total of 128 megabytes of memory for program, data, and video storage. The internal DDR controller uses a PLL to control the DDR memory timing. Memory refresh for DDR2 is handled automatically by the DM368 internal DDR controller.

2.1.4 Media Card Interface

The EVM supports one Micro SD and one SD/MMC media card interface. The MMC/SD0 port is dedicated to the Micro SD media card. The insert and write protect status can be read through the CPLD register. The MMC/SD1 port is configured to a second SD/MMC media card. This port is multiplexed through CBTLV switches to be used as general purpose I/O pins when the CPLD is appropriately configured for I/O multiplexing. The insert and write protect pin status can be read through the CPLD register.

2.1.5 UART Interface

The internal UART0 on the DM368 device is driven to connector P1. The UART interface is routed to the RS-232 line drivers prior to being brought out to a DB-9 connector, P1.

2.1.6 USB Interface

The DM368 incorporates an on-chip USB II controller. This interface is brought out to a mini A/B connector. Two jumpers are provided to make a flexible host peripheral, and USB On The Go interface. J26 is used to manually select the ID pin state. J6 is used to add additional capacitance to VBUS for host mode operation. A TPS2065 is used to power VBUS through a DRV_VBUS signal for host mode applications. The CPLD selects the source pin for DRV_VBUS signals through the internal CPLD registers.

2.2 Input Video Port Interfaces and Imager Input Ports

The DM368 EVM supports composite, component, or imager video capture. CBT multiplexers selected through the CPLD registers chose the interface connected to the DM368 video input port. A Texas Instruments TVP5146 is used to decode composite video or S-video inputs into the device. J15 is used for the S-video inputs, and J13 for the composite inputs on the EVM.

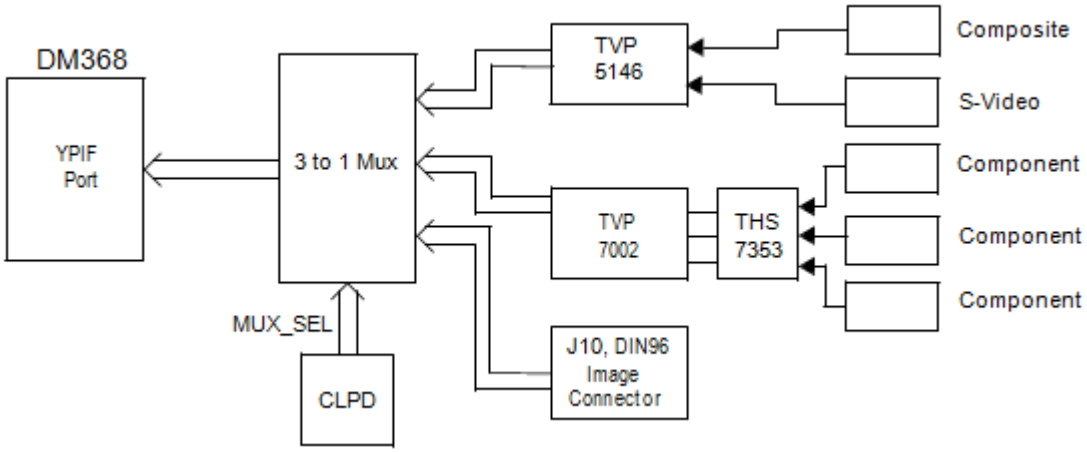
A TVP7002 provides component image capture up to 720P resolution.

J11, J8, and J9 interface to a THS7353 amplifier and filter, which interfaces directly to the TVP7002, which drives the DM368 input port.

J10, a DIN96 connector allows users to support imager interfaces. This is mapped directly to the video input port through the CBT mux. Figure 2-1 shows this mapping.

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Figure 2-1. DM368 EVM Input Video Mapping



2.2.1 On-Chip Video Output DAC

The DM368 incorporates one TV composite video output DAC and three component video DACs to interface to composite and component video outputs. The TV Out DAC is filtered and driven to RCA jack J16.

The component output DACs are driven into a THS7303 video amplifier, and output to RCA connectors J21, J17, and J20.

2.2.2 LCD Video Connectors

The DM368 incorporates three interface connectors, J18, J19, and J23, for digital video output for interfacing to LCD displays. The pinouts for these displays are detailed in Chapter 3.

2.3 AIC3101 Interface

The EVM uses a Texas Instruments TLV320AIC3101 stereo codec for input and output of audio signals. The codec samples the analog signals on the microphone or line inputs, and converts them into digital data to be processed by the DSP. When the DSP is finished with the data, it uses the codec to convert the samples back into analog signals on the line output, so the user can hear the output.

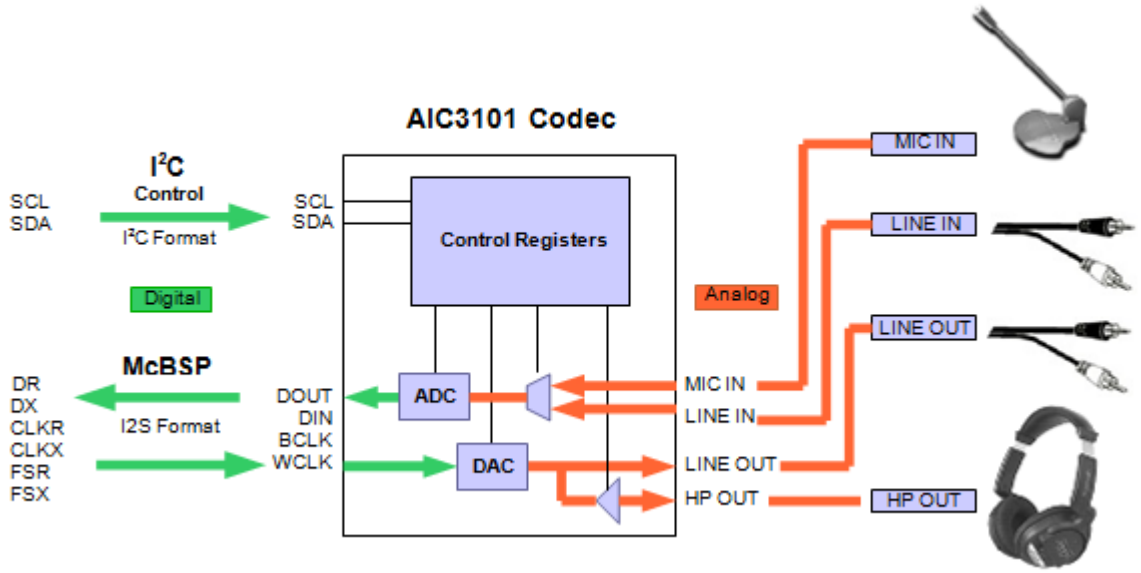
The codec communicates using two serial channels, one to control the codec's internal configuration registers and one to send and receive digital audio samples. The I^2C bus is used as the AIC3101 control channel. The control channel is generally only used when configuring the codec, and is typically idle when audio data is being transmitted.

The McBSP of the DM368 is used as the bidirectional data channel. All audio data flows through the data channel. Many data formats are supported based on the three variables of sample width, clock signal source, and serial data format. The EVM examples generally use a 16-bit sample width with the codec in master mode, to generate the frame sync and bit clocks at the correct sample rate without effort on the DSP side.

The codec is clocked through a 27-MHz oscillator. The internal sample rate generator subdivides the default system clock to generate common audio frequencies. The sample rate is set by a codec register. Figure 2-2 shows the codec interface on the DM368 EVM.

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Figure 2-2. DM368 EVM CODEC Interface



2.4 On-Chip Voice Codec

The DM368 integrates a single-channel voice codec. The input for this codec is connected to the onboard microphone M1. The output of this codec is connected to the onboard speaker SPK1.

2.5 On-Chip Analog to Digital Converter (ADC)

The DM368 has an on-chip 6-channel analog to digital converter (ADC). Four of the channels are interfaced to onboard voltages, and two channels are connected to test points, as shown in Table 2-28.

Table 2-28. On-Chip Analog to Digital Converter

Channel	Input Signal
ADC_CH0	CCD_PSMON
ADC_CH1	VCC_3V3
ADC_CH2	CPU_VCC_1V8
ADC_CH3	VCC_1V2
ADC_CH4	TP37
ADC_CH5	TP36

2.6 On-Chip RTC

The DM368 integrates an on-chip real time clock. The real time clock is battery-backed up through the TPS65510 and BHT1 battery. The EVM is not shipped with a backup battery. The mode of operation for the real time clock is configured through the SW23 switch, as defined in Chapter 3.

2.7 Ethernet Interface

The DM368 incorporates an internal MII ethernet MAC, which interfaces to a Mircel 10/100 ethernet Phy. The 10/100-Mbit interface is isolated and brought out to an RJ-45 standard ethernet connector, P2. The ethernet address is stored in the onboard I²C EEPROM manufacturing.

For GPIO modes of operation, when the MII interface is not used, CBTLV multiplexes and directs the I/O to the onboard CPLD used as imager expansion I/Os.

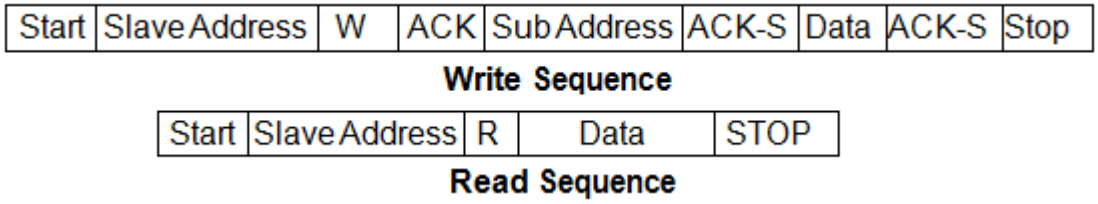
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The RJ-45 has two LEDs integrated into its connector. The LEDs are green and yellow, and indicate the status of the ethernet link. The green LED, when on, indicates a link, and when blinking, indicates link activity. The yellow LED, when illuminated, indicates full duplex mode.

2.8 I²C Interface

The I²C bus on the DM368 is ideal for interfacing to the control registers of many devices. On the DM368 EVM, the I²C bus is used to configure the video decoders, stereo codec, video amplifiers, I2C EEPROM, and communicate with the MSP430. An I²C ROM is also interfaced through the serial bus. The format of the bus is shown in Figure 2-3.

Figure 2-3. I²C Bus Format



The addresses of the onboard peripherals are shown in Table 2-29.

Table 2-29. I²C Memory Map

Device	Address	R/W	Function
AIC3101	0x18	R/W	CODEC
MSP430	0x25	R/W	IR Controller
THS7303	0x2C	R/W	Video Output Amplifier
THS7353	0x2E	R/W	Video Input Amplifier
CAT24C256	0x50	R/W	I²C EEROM
TVP7002	0x5C	R/W	Component Decoder
TVP5146	0x5D	R/W	Composite 1 Decoder

2.8.1 MSP430

The DM368 EVM incorporates an infrared remote interface using a MSP430 microcontroller. The I²C interface is used on the DM368 processor to communicate to the MSP430. The MSP430 acts as a slave device on the I²C bus.

2.9 Daughter Card Interfaces

The EVM provides expansion connectors that can be used to accept plug-in daughter cards. The daughter card allows users to build on their EVM platform to extend its capabilities, and provide customer and application-specific interfaces. The asynchronous EMIF is brought out to J14. The video digital output port is brought out to the daughter card interface along with I/O, and the imager interface is brought out to a DIN96 connector.

2.10 DM368 CPU and Video Clocks

The DM368 EVM uses a 24-MHz crystal to generate the main input clock. The DM368 has multiple internal PLLs, which can multiply the input clock to generate the internal clocks. The PLL multipliers are set through the software on the DM368 device.

The real time clock uses a 32,768-Hz crystal.

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2.11 Battery

The DM368 EVM incorporates a battery holder, to provide backup power to the internal real time clock when the power is not applied to the board. The optional battery should be +3-V 20-mm coin-type lithium single cell.

Some common part numbers for batteries which should operate in the EVM are shown in Table 2-30.

Table 2-30. Battery Part Numbers

Part Numbers
CR2032
DL2032
BR2032
CR2025
BR2025
CR2016
BR2016
DL2016

These batteries are available from Duracell, Eveready, Panasonic, Ray-O-Vac, Sanyo, Sony, Sieko, Toshiba, Varta, and other battery manufacturers.

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Physical Description

This chapter describes the physical layout of the DM368 EVM and its interfaces.

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3.1 Board Layout

The DM368 EVM is a 8.0 × 8.7 inch (203 × 221 mm), ten (10) layer printed circuit board, powered by an external +5-V-only power supply. Figure 3-1 shows the layout of the top side of the DM368 EVM.

Figure 3-1. DM368 EVM, Interfaces Top Side

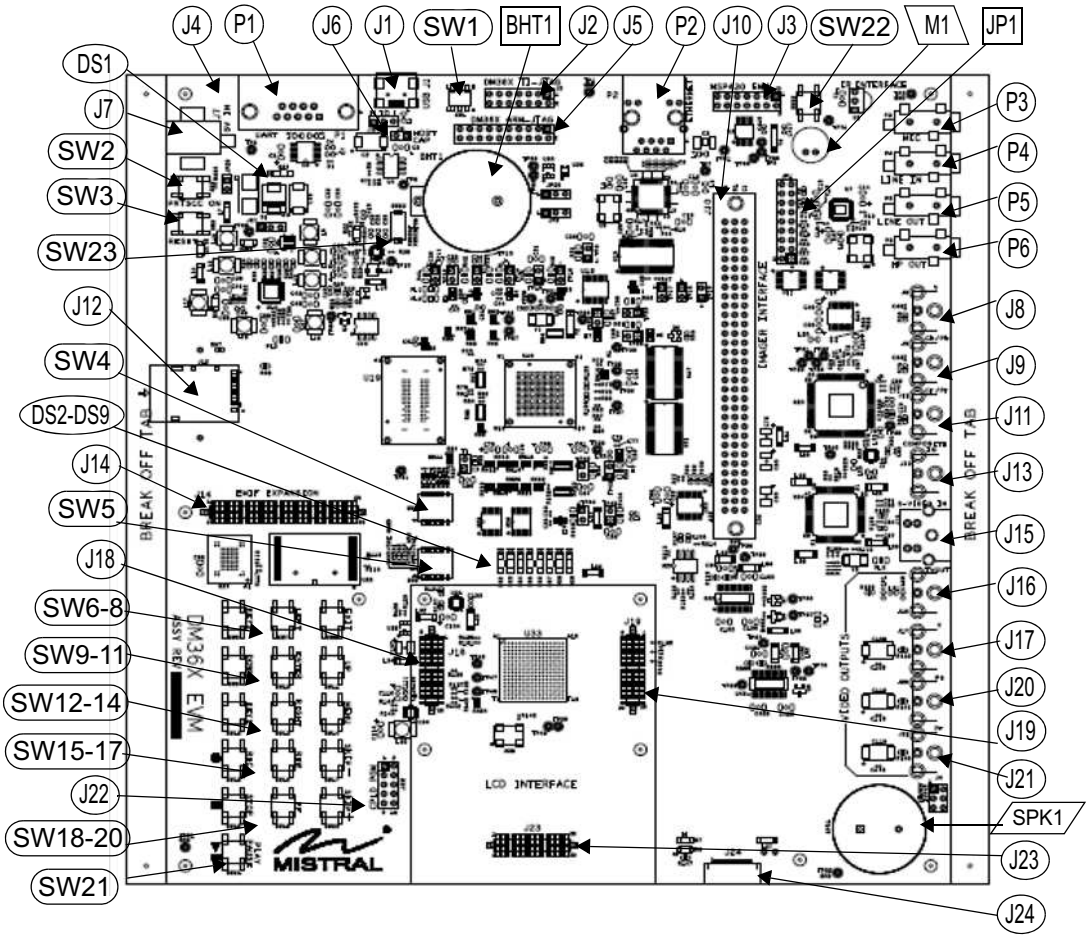
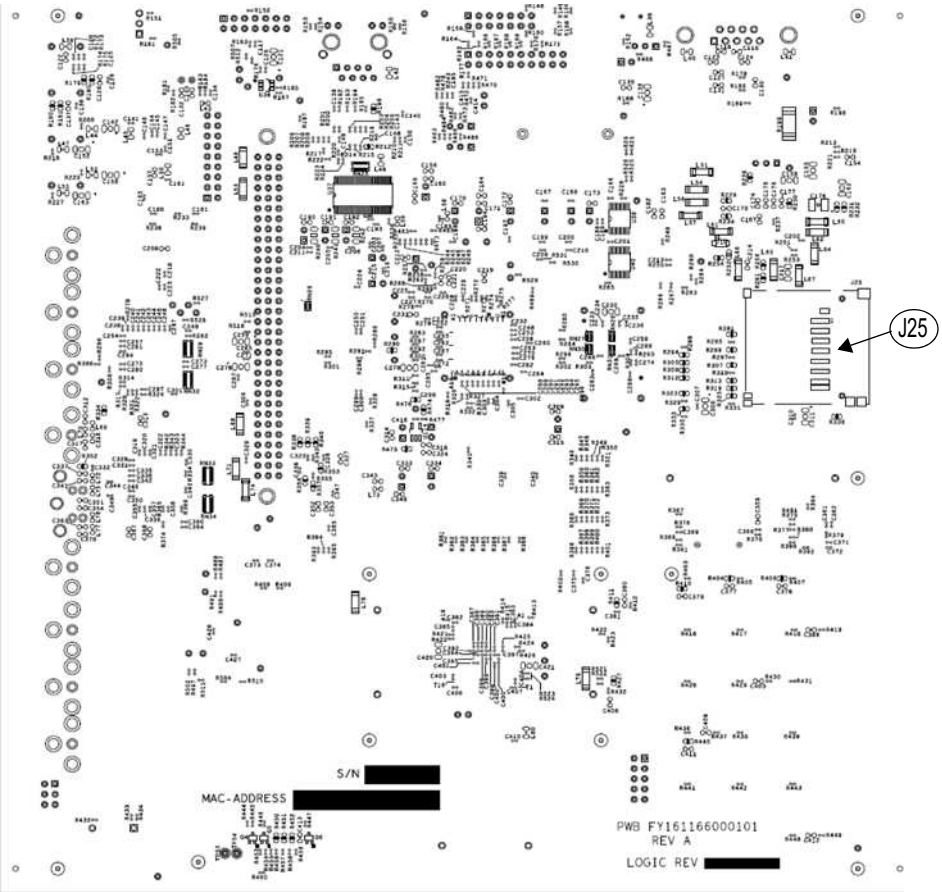


Figure 3-2 shows the layout of the bottom side of the DM368 EVM.

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Figure 3-2. DM368 EVM, Interfaces Bottom Side



3.2 Connectors

The DM368 EVM has numerous connectors, option jumpers, and interfaces to control and provide connections to various peripherals, as shown in Table 3-1. These connectors and jumpers are described in the following sections.

Table 3-1. DM368 Connectors

Connector	Size	Function
J1	1 × 4	USB MiniAB connector
J2	2 × 7	14-pin TI JTAG emulation header
J3	7 × 2	MSP430 JTAG header
J4	3 × 2	Spare jumper holder
J5	10 × 2	20-pin ARM JTAG emulation header
J6	2 × 1	USB capacitor select
J7	2	+5 Volts In
J8	2	Y component video in, RCA jack (Grn)
J9	2	Pb component video in, RCA jack (Blue)
J10	32 × 3	Imager interface
J11	2	Pr component video in, RCA jack (Red)
J12	2	Micro SD card interface
J13	2	CVBS/Y input, RCA jack (Yellow)
J14	30 × 2	EMIF/UPHI DC interface

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Table 3-1. DM368 Connectors (continued)

Connector	Size	Function
J15	4	S-video In, DIN connector
J16	2	Composite TV out, RCA jack (Yellow)
J17	2	Y component video output, RCA jack (Green)
J18	15 × 2	Video output DC
J19	15 × 2	Video output DC
J20	2	Pb component video output, RCA jack (Blue)
J21	2	Pr component video output, RCA jack (Red)
J22	5 × 2	CPLD programming header
J23	15 × 2	I/O interface header
J24	20 × 1	DILC host connector
J25	9	MMC/SD card interface (not populated)
P1	9	RS-232 UART
P2	6	Ethernet interface
P3	4	Microphone in
P4	4	Line in
P5	4	Line out
P6	4	Headphone out
U1	3	Infrared interface
SPK1	2	Speaker
BHT1	2	Battery holder
M1	2	Microphone

3.2.1 J1, USB MiniAB Connector and Jumpers

Connector J1 is a mini A/B USB connector. The pinout for the J1 connector is shown in Table 3-2.

Table 3-2. J1, MiniAB USB Connector

Pins	Signal
1	USB_VBUS_CONN
2	USB_DM
3	USB_DP
4	USB_ID
5	GND

The EVM incorporates the ability to toggle the ID pin on the USB connector through software control. The USB_ID pin on the DM368 controls this function.

For USB ON The Go mode, remove jumper J6. This allows the cable to configure the ID pin on the DM368 processor.

The EVM supplies up to 500 mA of current to the USB_VBUS through a TPS61092 DC-DC converter. This is enabled through the DM368 DRV_VBUS pin. J50 supplies extra capacitance for host mode operations. Remove J50 for USB On The Go operations. Spare jumpers can be stored on connector J4.

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3.2.2 J2, 14-Pin External JTAG Connector

Connector J2 is a 2 × 7 double-row male header with pin 6 clipped to serve as a key. This is the standard interface used by JTAG emulators to interface to Texas Instruments processors. The pinout for the connector is shown in Figure 3-3.

Figure 3-3. J2, 14-Pin External JTAG Connector



The signal names for each pin are shown in Table 3-3.

Table 3-3. J2, 14-Pin External JTAG Connector

Pin	Signal Name	Pin	Signal Name
1	TMS	2	TRST-
3	TDI	4	GND
5	PD	6	no pin - key
7	TDO	8	GND
9	TCKRET	10	GND
11	TCK	12	GND
13	EMU0	14	EMU1

NOTE: EMU0/EMU1 mode must be selected for ICEPICK mode.

3.2.3 J3, MSP430 JTAG Header

The J3, MSP430 JTAG header is located on the top side of the board, and used to provide a programming interface to the MSP430 microcontroller. The pinout for the J3 connector is shown in Table 3-4. This connector is typically for factory use only.

Figure 3-4. J3, MSP430 JTAG Header

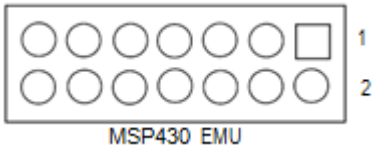


Table 3-4. J3, MSP430 JTAG Header

Pin	Signal	Pin	Signal
1	430_TDO/TDI	2	NC
3	NC	4	MSP430_3V3
5	NC	6	NC
7	TCK	8	NC

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Table 3-4. J3, MSP430 JTAG Header (continued)

Pin	Signal	Pin	Signal
9	GND	10	NC
11	NC	12	NC
13	NC	14	NC

3.2.4 J4, Spare Jumper Holder

J4 is a 3 × 2 connector used to hold unused jumper plugs that from time to time may be required in other connectors or jumpers on the D365 EVM. The pins on this connector are not connected to any signals.

3.2.5 J5, 20-Pin ARM JTAG Emulation Header

The J5 emulation header is located on the top side of the board, and used to provide an interface to ARM-compatible JTAG emulators. The pinout for this connector is shown in Table 3-5.

Table 3-5. J5, 20-Pin ARM JTAG Emulation Header

Pin	Signal	Pin	Signal
1	VCC_3V3	2	VCC_3V3
3	ARM_TRSTn	4	Ground
5	ARM_TDI	6	Ground
7	ARM_TMS	8	Ground
9	ARM_TCK	10	Ground
11	ARM_TCKRET	12	Ground
13	ARM_TDO	14	Ground
15	ARM_RSTn	16	Ground
17	NC	18	Ground
19	NC	20	Ground

NOTE: The EMU0/EMU1 switch must be set to ARM mode.

3.2.6 J6, USB Capacitance Select

The J6 jumper is used to provide more capacitance when the USB connector is used in the host mode. When the jumper is shorted, the extra capacitance is provided. These open and shorted position are shown in Figure 3-5 and their functions described in Table 3-6.

Figure 3-5. J6, USB Capacitance Select

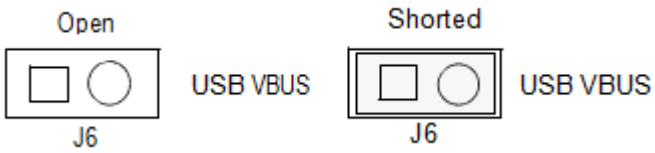


Table 3-6. J6, USB Capacitance Select

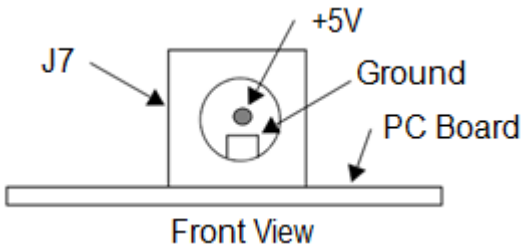
Position	Function
Open	6.8-µF capacitance
Shorted	106.8-µF capacitance

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3.2.7 J7, +5-V Input

Connector J7 is the input power connector. This connector brings in +5 V to the EVM. This is a 2.5-mm jack. The inside of the jack is tied to through a fuse to VCC_5V. The other side is tied to ground and LED DS1. Figure 3-6 shows this connector as viewed from the card edge.

Figure 3-6. J7, +5-V Input Connector



3.2.8 J12, Micro SD Card Connector

The J12 Micro SD card interface connector is located on the top side of the board, and is used to provide an interface to a Micro SD card. The pinout for the J12 connector is shown in Table 3-7.

Table 3-7. J12, Micro SD Card Connector

Pin	Signal	Pin	Signal
1	SD_DATA2	2	SD_DATA3
3	SD_CMD	4	VCC_3V3
5	SD_CLK	6	GND
7	SD_DATA0	8	SD_DATA1
9	SD/MMC.INS	10	GND
11	GND	12	GND
13	GND	14	GND

3.2.9 J10, Imager

Connector J10 is a 32 × 3 connector used to interface to external imager logic. The pinout for this connector is shown in Table 3-8.

Table 3-8. J10, Imager Interface

Pin	Signal	Pin	Signal	Pin	Signal
A1	Ground	B1	GPIO_MD10	C1	GND_STB
A2	Ground	B2	GPIO_MD9	C2	GND_STB
A2	CCD_PSMON	B2	GPIO_MD8	C2	3V3_STB
A4	GPIO_MD1	B4	GPIO_MD7	C4	5V_DC_J6
A5	5V_DC_J6	B5	5V_DC_J6	C5	5V_DC_J6
A6	GND_MTR	B6	MOT_PWR	C6	GPIO_MD19
A7	GND_MTR	B7	MOT_PWR	C7	GPIO_MD18
A8	NC	B8	CCD_DATA0	C8	GPIO_MST_SLV
A9	CDD_DATA2	B9	CCD_DATA15	C9	GPIO_MD17
A10	Ground	B10	CCD_DATA1	C10	GPIO_MD16
A11	CDD_DATA3	B11	GPIO_MD6	C11	GPIO_MD15
A12	Ground	B12	GPIO_MD5	C12	GPIO_MD14
A13	CDD_DATA4	B13	GPIO_MD4	C13	GPIO_MD13
A14	Ground	B14	Ground	C14	GPIO_TACH
A15	CDD_DATA5	B15	PWM_CCD_SUB	C15	GPIO_MD12

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Table 3-8. J10, Imager Interface (continued)

Pin	Signal	Pin	Signal	Pin	Signal
A16	Ground	B16	CCD_DDSRST	C16	GPIO_MD11
A17	CDD_DATA6	B17	GPIO_MD3	C17	I2C_DATA
A18	Ground	B18	GPIO_MD2	C18	I2C_SCLK
A19	CDD_DATA7	B19	SPI4_SDO	C19	VCC_CCD15V
A20	Ground	B20	SPI4_SCLK	C20	VCC_CCD15V
A21	CDD_DATA8	B21	Ground	C21	VCC_CCD_N75V
A22	Ground	B22	CDD_PCLK	C22	VCC_CCD_N75V
A23	CDD_DATA9	B23	Ground	C23	3V3_CCD
A24	Ground	B24	CDD_WEN	C24	3V3_CCD
A25	CDD_DATA10	B25	Ground	C25	5V_DC_J6
A26	Ground	B26	CDD_FIELD	C26	5V_DC_J6
A27	CDD_DATA11	B27	Ground	C27	Ground
A28	Ground	B28	CDD_HSYNC	C28	Ground
A29	CDD_DATA12	B29	Ground	C29	3V3A_CCD
A30	Ground	B30	CDD_VSYNC	C30	3V3A_CCD
A31	CDD_DATA13	B31	Ground	C31	AGND_IMAGER
A32	Ground	B32	CDD_DATA14	C32	AGND_IMAGER

3.2.10 J14, EMIF/UPI DC Interface

Table 3-9. J14, EMIF/UPI DC Interface

Pin	Signal	Pin	Signal
2	Ground	1	Ground
4	EM_D0	3	EM_D1
6	EM_D2	5	EM_D3
8	EM_D4	7	EM_D5
10	EM_D6	9	EM_D7
12	Ground	11	Ground
14	EM_D8	13	EM_D9
16	EM_D10	15	EM_D11
18	EM_D12	17	EM_D13
20	EM_D14	19	EM_D15
22	Ground	21	Ground
24	EM_WAIT	23	EM_CLK
26	Ground	25	Ground
28	EM_CE0	27	EM_ADV
30	Ground	29	Ground
32	EM_CE1	31	EM_WE
34	Ground	33	Ground
36	EMIF_SEL	35	EM_OE
38	Ground	37	Ground
40	EM_BA0	39	EM_BA1
42	EM_A0	41	EM_A1
44	EM_A2	43	EM_A3
46	EM_A4	45	EM_A5
48	Ground	47	Ground

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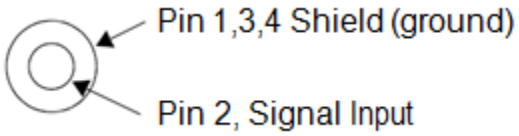
Table 3-9. J14, EMIF/UPI DC Interface (continued)

Pin	Signal	Pin	Signal
50	EM_A6	49	EM_A7
52	EM_A8	51	EM_A9
54	EM_A10	53	EM_A11
56	EM_A12	55	EM_A13
58	VCC_3V3	57	VCC_3V3
60	VCC_5V	59	VCC_5V

3.2.11 J8, Y Component Video In, RCA Jack (Green)

J8 is an RCA jack used as a Y component input to the THS7353, U15, pin 3. Figure 3-7 shows this connector as viewed from the card edge.

Figure 3-7. J8, Y Component Video In, RCA Jack



The pinouts are shown in Table 3-10.

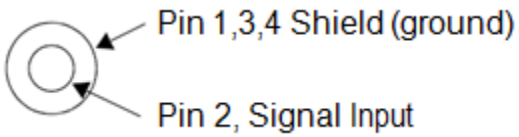
Table 3-10. J8, Y Component Video In, RCA Jack

Pin	Signal Name
1	TVP_AGND
2	CH2-INA, U15, Pin 3
3	TVP_AGND
4	TVP_AGND

3.2.12 J9, Pb Component Video In, RCA Jack (Blue)

J9 is an RCA jack used as a Pb component input to the THS7353, U15, pin 4. Figure 3-8 shows this connector as viewed from the card edge.

Figure 3-8. J9, Pb Component Video In, RCA Jack



The pinouts are shown in Table 3-11.

Table 3-11. J9, Pb Component Video In, RCA Jack

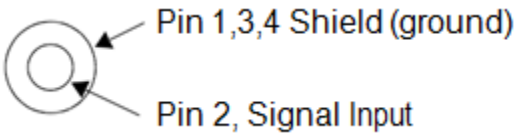
Pin	Signal Name
1	TVP_AGND
2	CH3-INA, U15, Pin 4
3	TVP_AGND
4	TVP_AGND

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3.2.13 J11, Pr Component Video In, RCA Jack (Red)

J11 is an RCA jack used as a Pr component input to the THS7353, U15, pin 2. Figure 3-9 shows this connector as viewed from the card edge.

Figure 3-9. J9, J11, Pr Component Video In, RCA Jack



The pinouts are shown in Table 3-12.

Table 3-12. J11, Pr Component Video In, RCA Jack

Pin	Signal Name
1	TVP_AGND
2	CH1-INA, U15, Pin 2
3	TVP_AGND
4	TVP_AGND

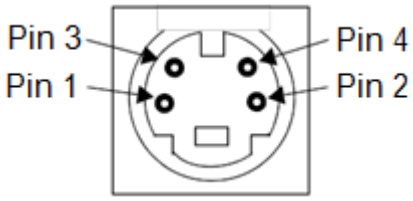
3.2.14 J15, S-Video In

Connector J15 is a four-pin mini din connector which interfaces to the TVP5146 encoder, U24. This connector brings in a video signal (LUMA) to pin 9 on the TVP5146. Figure 3-10 shows this connector as viewed from the card edge.

CAUTION

Do not plug into this connector with the power on.

Figure 3-10. J15, Front View, Mini Din Connector



The pinouts are shown in Table 3-13.

Table 3-13. J15, S-Video In, Mini Din Connector

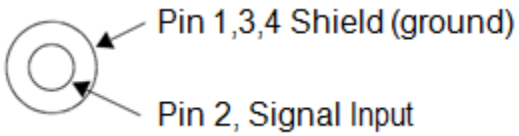
Pin	Signal Name
1	GND
2	GND
3	VI_1_C, U24, Pin 2
4	GND

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3.2.15 J13, CVBS/Y Input, RCA Jack (Yellow)

J13 is an RCA jack used as the CVBS/Y input to the TVP5146. Figure 3-11 shows this connector as viewed from the card edge.

Figure 3-11. J13, CVBS/Y Input, RCA Jack



The pinouts are shown in Table 3-14.

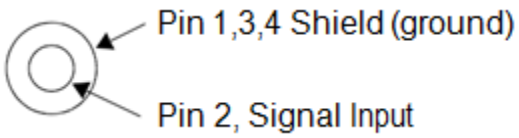
Table 3-14. J13, CVBS/Y Input, RCA Jack

Pin	Signal Name
1	DEC_GND
2	VI_2_B, U24, Pin 8, TVP5146
3	DEC_GND
4	DEC_GND

3.2.16 J16, Composite TV Out, RCA Jack (Yellow)

J16 is an RCA jack used as a TV output from the DM368. This connector brings out a TV signal. Figure 3-12 shows this connector as viewed from the card edge.

Figure 3-12. J16, Composite TV Out RCA Jack



The pinouts are shown in Table 3-15.

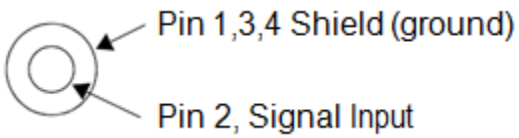
Table 3-15. J16, Composite TV Out, RCA Jack

Pin	Signal Name
1	DEC_GND
2	U18-3, Pin A10
3	DEC_GND
4	DEC_GND

3.2.17 J17, Y Component Video Out, RCA Jack (Green)

J17 is an RCA jack used as a green component output from the THS7303 DAC, U23, pin 17, signal CH2-OUT. Figure 3-13 shows this connector as viewed from the card edge.

Figure 3-13. J17, Y Component Video Out, RCA Jack



The pinouts are shown in Table 3-16.

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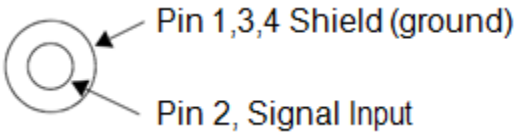
Table 3-16. J17, Y Component Video Out, RCA Jack

Pin	Signal Name
1	DEC_GND
2	THS7303 DAC, U23, pin 19, signal CH2-OUT
3	DEC_GND
4	DEC_GND

3.2.18 J20, Pb Component Video Out, RCA Jack (Blue)

J20 is an RCA jack used as a Pb component output from the THS7303 DAC, U23, pin 15, signal CH3-OUT. Figure 3-14 shows this connector as viewed from the card edge.

Figure 3-14. J20, Pb Component Video Out, RCA Jack



The pinouts are shown in Table 3-17.

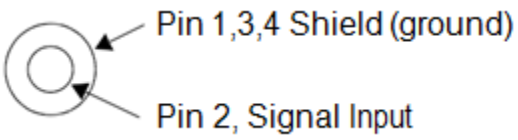
Table 3-17. J20, Pb Component Video Out, RCA Jack

Pin	Signal Name
1	DENC_GND
2	THS7303 DAC, U23, pin 15, signal CH3-OUT
3	DENC_GND
4	DENC_GND

3.2.19 J21, Pr Component Video Output, RCA Jack (Red)

J21 is an RCA jack used as a Pr component output from the THS7303 DAC, U23, pin 19, signal CH1-OUT. Figure 3-15 shows this connector as viewed from the card edge.

Figure 3-15. J21, Pr Component Video Out, RCA Jack



The pinouts are shown in Table 3-18.

Table 3-18. J21, Pr Component Video Out, RCA Jack

Pin	Signal Name
1	DENC_GND
2	THS7303 DAC, U23, pin 19, signal CH1-OUT
3	DENC_GND
4	DENC_GND

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3.2.20 J18, J19, Video Output DC

Connectors J18 and J19 make up the interface to the video output DC interface. The signals on each of these connectors are shown in Table 3-19 and Table 3-20.

Table 3-19. J18, Video Output DC

Pin	Signal	Pin	Signal
1	BL_6V6	2	LCD_3V3
3	BL_6V6_RTN	4	LCD_3V3
5	Ground	6	Ground
7	VDOUT_VSYNC	8	NC
9	Ground	10	LCD_V5
11	VDOUT_HSYNC	12	LCD_V5
13	Ground	14	Ground
15	VDOUT_VCLK	16	CDOUT_FIELD
17	Ground	18	15V_LCD
19	BAT_VIN	20	15V_LCD
21	BAT_VIN	22	Ground
23	SPI1_SDI	24	VDOUT_EXTCLK
25	SPI1_SDENA0	26	I2C_DATA
27	SPI1_SDO	28	I2C_SCLK
29	SPI SCLK	30	Ground

Table 3-20. J19, Video Output DC

Pin	Signal	Pin	Signal
1	VDOUT_Y0	2	VDOUT_C0
3	R1_GIO33	4	Ground
5	VDOUT_Y1	6	VDOUT_C1
7	R1_GIO32	8	Ground
9	VDOUT_Y2	10	VDOUT_C2
11	R1_GIO30	12	Ground
13	VDOUT_Y3	14	VDOUT_C3
15	Ground	16	Ground
17	VDOUT_Y4	18	VDOUT_C4
19	Ground	20	Ground
21	VDOUT_Y5	22	VDOUT_C5
23	Ground	24	Ground
25	VDOUT_Y6	26	VDOUT_C6
27	Ground	28	Ground
29	VDOUT_Y7	30	VDOUT_C7

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3.2.21 J22, CPLD Programming Header

The J22, CPLD programming header, is for use by the factory. This header is not intended to be used outside the factory. The signals on this header are shown in Table 3-21.

Table 3-21. J22, CPLD Programming Header

Pins	Signal	Pins	Signal
1	ISR_TCK	2	Ground
3	ISR_TDO	4	VCC_3V3
5	ISR_TMS	6	NC
7	NC	8	NC
9	ISR_TDI	10	Ground

3.2.22 J23, I/O Interface Header

Connector J23 is an I/O interface header allowing the user to connect external logic to interface with the I/O pins on the CPLD U33. The signals on this header are shown in Table 3-22.

Table 3-22. J23, I/O Interface Header

Pins	Signal	Pins	Signal
2	VCC_1V8	1	VCC_1V8
4	NC	3	NC
6	CPLD.COMM_GIO6	5	CPLD.COMM_GIO7
8	CPLD.COMM_GIO16	7	CPLD.COMM_GIO17
10	CPLD.COMM_GIO54	9	CPLD.COMM_GIO67
12	CPLD.COMM_GIO65	11	CPLD.COMM_GIO31
14	CPLD.COMM_GIO63	13	CPLD.COMM_GIO64
16	CPLD.COMM_GIO62	15	CPLD.COMM_GIO61
18	CPLD.COMM_GIO60	17	CPLD.COMM_GIO59
20	CPLD.COMM_GIO58	19	CPLD.COMM_GIO57
22	CPLD.COMM_GIO56	21	CPLD.COMM_GIO32
24	NC	23	NC
26	NC	25	NC
28	CPLD.CONN_RESETn	27	NC
30	Ground	29	Ground

3.2.23 J24, DILC Host Connector

J24 is the DILC host connector. The signals on this connector are shown in Table 3-23.

Table 3-23. J24, DILC Host Connector

Pins	Signal
1	CAM_PWR
2	CAM_PWR
3	SPI2_SCLK_DILC
4	Ground
5	SPI2_SDO_DILC
6	Ground
7	SPI2_SDI_DILC
8	Ground
9	LINEOUT

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Table 3-23. J24, DILC Host Connector (continued)

Pins	Signal
10	AVJ_DET
11	TP53
12	TP33
13	GIO_DILC_CHG_CTL
14	CD1
15	CD2
16	VBUS1
17	TP54
18	Ground
19	TVOUT
20	Ground
MP1	Ground
MP2	Ground

3.2.24 J25, MMC/SD Connector

The J25 MMC/SD connector is located on the bottom side of the board, and used to provide an interface to a MMC/SD card. The pinout for the J25 connector is shown in Table 3-24.

Table 3-24. J25, MMC/SD Connector

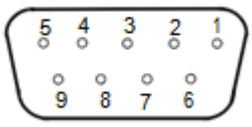
Pin	Signal	Pin	Signal
1	CONN_SD1_DATA3	2	CONNSD1_CMD
3	GND	4	VCC_3V3
5	CONN_SD1_CLK	6	GND
7	CONN_SD1_DATA0	8	CONN_SD1_DATA1
9	CONN_SD1_DATA2	10	WP, VCC_3V3
11	GND	12	CARD_DETECT

NOTE: In this version of DM368 EVM, the MMC/SD Connector (J25) is Not Populated.

3.2.25 P1, RS-232 UART

The P1 connector is a 9-pin male D-connector which provides a UART interface to the EVM. This connector interfaces to the MAX 3221 RS-232 line driver (U3) and is located on the top side of the board. A view of the connector from the card edge is shown in Figure 3-16. The signals present on this connector are defined in Table 3-25.

Figure 3-16. P1, DB9 Male Connector



The pin numbers and their corresponding signals are shown in Table 3-25. This corresponds to a standard dual row to DB-9 connector interface used on personal computers.

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Table 3-25. P1, RS-232 UART Pinout

Pin	Signal Name
1	NC
2	R_IN, U3, Pin 8
3	T_OUT, U3, pin 13
4	NC
5	GND
6	NC
7	Pin 8
8	Pin 7
9	NC

3.2.26 P2, Ethernet Interface

The P2 connector is located on the top side of the board, and used to provide an ethernet interface. P2 integrates the magnetics and standard RJ-45 connector. Table 3-26 and Table 3-27 show the signals present on the magnetics interface and the connector side.

Table 3-26. P2, Magnetics and LEDs Interface Signals

Pin	Signal	Pin	Signal
1	TX+, U5, Pin 41	2	TX-, U5, Pin 40
3	RX+, U5, Pin 33	4	VDD_3V3A
5	VDD_3V3A	6	RX-, U5, Pin 32
7	NC	8	GND_E_NET
9	VCC_3V3A	10	EPHY_LED2
11	VCC_3V3A	12	EPHY_LED0

The ethernet connector incorporates 2 LEDs, which give link and transmit status from the ethernet controller.

Table 3-27. P2, RJ-45 Connector

Pin	Signal	Pin	Signal
1	TXD+	2	TXD-
3	RXD+	4	TXD-CT
5	RXD-CT	6	RXD-
7	NC	8	GND
9	LED1+	10	LED1-
11	LED2+	12	LED2-

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3.2.27 P3, Microphone In

The microphone input, P3, is a 3.5-mm stereo jack. Both inputs are connected to the microphone, making it monaural. The signal is connected to signals MIC2R and MIC2L of the TVL320AIC3101. The signals on the plug are shown in Figure 3-17. The pinouts are shown in Table 3-28.

Figure 3-17. P3, Microphone Input Jack

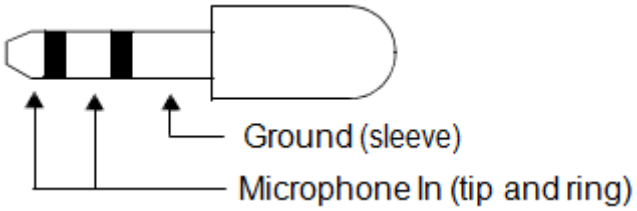


Table 3-28. P3, Microphone Input Jack

Pin	Signal Name
1	GND_AIC
2	MIC2L, MIC2R, U7, Pins 14,16
3	MIC2L, MIC2R, U7, Pins 14,16
4	GND_AIC

3.2.28 P4, Line In

Connector P4 is an audio stereo line input to the TVL320AIC3101, U7, on the EVM. The input connector is a 3.5-mm stereo jack. The signals on the mating plug are shown in Figure 3-18. The pinouts are shown in Table 3-29.

Figure 3-18. P4, Audio Stereo Line In Jack

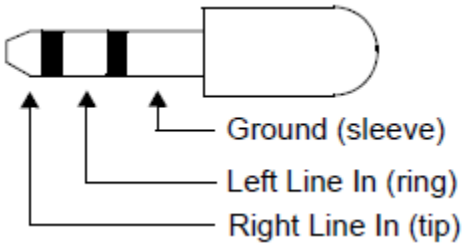


Table 3-29. P4, Audio Stereo Line In

Pin	AIC3101 Signal
1	GND_AIC
2	LINE1LP, U7, Pin 10
3	LINE1RP, U7, Pin 12
4	GND_AIC

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3.2.29 P5, Line Out

The connector P5, is an audio stereo output from the TVL320AIC3101, U7, on the EVM. The output connector is a 3.5-mm stereo jack. The signals on the mating plug are shown in Figure 3-19. The pinouts are shown in Table 3-30.

Figure 3-19. P5, Audio Line Out Stereo Jack

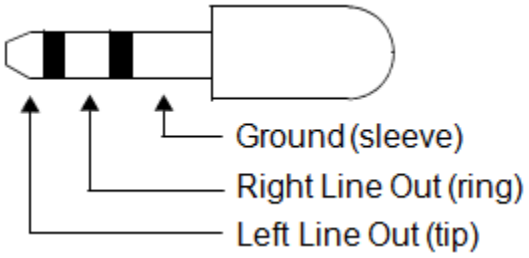


Table 3-30. P5, Audio Line Out Stereo Jack

Pin	AIC3101 Signal
1	GND_AIC
2	LEFT_LO+, U7, Pin 27
3	RIGHT_LO+, U7, Pin 29
4	NC

3.2.30 P6, Headphone Out

The P6 connector is a 3.5-mm stereo headphone output from the TVL320AIC3101, U7, on the EVM. This connector is located on the top side of the board. A view of the connector from the card edge is shown in Figure 3-20. The signals present on this connector are defined in Table 3-31.

Figure 3-20. P6, Headphone Out Interface

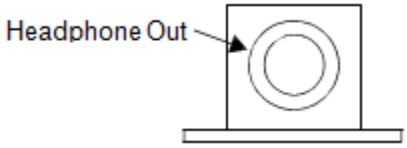


Table 3-31. P6, Headphone Out Interface

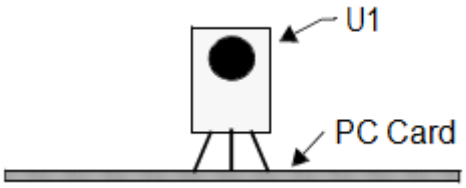
Pin	AIC3101 Signal
1	GND_AIC
2	HPLOUT, U7, Pin 19
3	HPROUT, U7, Pin 23
4	NC

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3.2.31 U1, Infrared Interface

U1 is an infrared receiver mounted on the edge of the board. This device interfaces to the MSP430 mircrocontroller. The view of U1 is shown from a board edge view in Figure 3-21.

Figure 3-21. U1, IR Interface, Card Edge View



The receiver supports interaction with an Infrared remote control included with the EVM. The pinouts are shown in Table 3-32.

Table 3-32. U1, Infrared Interface

U1 Pin	MSP430 Signal, Pin
1	P1.2/TA1/A1+/A4-, U2, Pin 4
2	GND
3	VCC_3V3

3.2.32 SPK1, Speaker Interface

The speaker interface SPK1 provides a speaker output driven directly from the DM368 processor. The connections going to the processor are shown in Table 3-33.

Table 3-33. SPK1, Speaker Interface

SPK1 Pin	DM368 Name, Pin
1	SPP, U18, Pin B9
2	SPN, U18, Pin A9

3.2.33 BHT1, Battery Interface

BHT1 is a holder for a BA2032SM battery. The signals on each pin are shown in Table 3-34.

Table 3-34. BHT1, Battery Interface

BHT1 Pin	BHT1 Connection
1	VBK, Up, Pin 13
2	Ground

3.2.34 M1, Microphone Interface

The microphone interface, M1, provides a microphone input directly into the DM368 processor. The connections going to the processor are shown in Table 3-35.

Table 3-35. M1, Microphone Interface

M1 Pin	DM368 Signal Name, Pin
1	MICIP, U18-9, Pin B8
2	MICIN, U18-9, Pin C9

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3.3 LEDs

The EVM has nine (9) LEDs located on the top side of the board. Information regarding the LEDs are shown in Table 3-36.

Table 3-36. LEDs

LED #	Use	Color
DS1	+5 Volts present	Green
DS2	User control through MSP430 I^2C	Green
DS3	User control through MSP430 I^2C	Green
DS4	User control through MSP430 I^2C	Green
DS5	User control through MSP430 I^2C	Green
DS6	User control through MSP430 I^2C	Green
DS7	User control through MSP430 I^2C	Green
DS8	User control through MSP430 I^2C	Green
DS9	User control through MSP430 I^2C	Green

3.4 Switches

The EVM has twenty-three (23) switches. The functions of these switches are shown in Table 3-37.

Table 3-37. Switches

Switch	Function	Type	Silkscreen
SW1	EMU0/EMU1 Control	2 Position DIP	
SW2	PRTSC ON	Push Button/Momentary	PRTSCC
SW3	RESET Switch	Push Button/Momentary	RESET
SW4	Boot/Config Select	6 Position DIP	SW4
SW5	Board Select	6 Position DIP	SW5
SW6	User Readable	Push Button/Momentary	KEY2
SW7	User Readable	Push Button/Momentary	LEFT
SW8	User Readable	Push Button/Momentary	EXIT
SW9	User Readable	Push Button/Momentary	DOWN
SW10	User Readable	Push Button/Momentary	ENTER
SW11	User Readable	Push Button/Momentary	UP
SW12	User Readable	Push Button/Momentary	KEY1
SW13	User Readable	Push Button/Momentary	RIGHT
SW14	User Readable	Push Button/Momentary	MENU
SW15	User Readable	Push Button/Momentary	REC
SW16	User Readable	Push Button/Momentary	REW
SW17	User Readable	Push Button/Momentary	SKIP -
SW18	User Readable	Push Button/Momentary	STOP
SW19	User Readable	Push Button/Momentary	FF
SW20	User Readable	Push Button/Momentary	SKIP +
SW21	Short to Ground	Push Button/Momentary	PLAY PAUSE
SW22	Short to Ground	Push Button/Momentary	
SW23	PRTSC Mode	2 Position DIP	

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3.4.1 SW1, EMU0/1 Select Switch

SW1 is a 2-position DIP switch providing four options in selecting the state of the EMU0 and EMU1 pins on the TMS320DM368 processor. A view of the switch is shown in Figure 3-22. The selection options with this switch are listed in Table 3-38.

Figure 3-22. SW1, EMU0/1 Select Switch

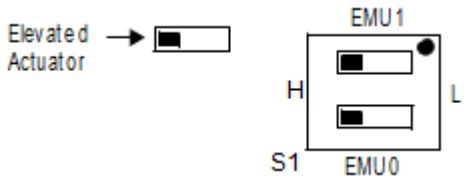


Table 3-38. SW1, EMU0/1 Select

State at Reset		Function
EMU1	**EMU0**	
L(0)	L(0)	Reserved
L(0)	H(1)	Reserved
H(1)	L(0)	Reserved
H(1)	H(1)	ICE PICK Mode (the factory shipped configuration) Both ARM and DSP JTAG-enabled

3.4.2 SW2, PWCTRO0 Push-Button

Switch SW2 is a push-button momentary switch that forces the PWCTRO0 signal on the DM368, U18-11, pin J3, to ground when the switch is depressed.

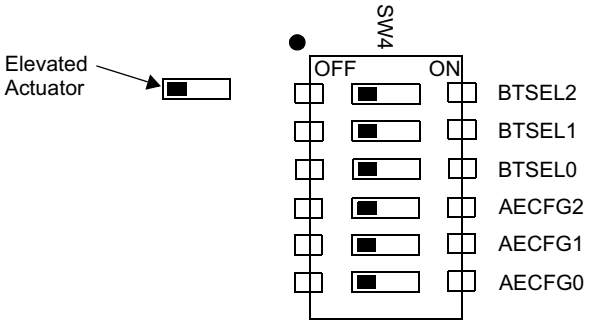
3.4.3 SW3, RESET Push-Button

Switch SW3 is a push-button momentary switch that resets the processor when depressed.

3.4.4 SW4, Boot Mode and Configuration Select

Switch SW4 is a 6-position DIP switch used to select the ARM boot mode and processor configuration. The first three positions select the ARM boot mode. The last three positions select the processor configuration. Figure 3-23, Table 3-39, and Table 3-40 show these options.

Figure 3-23. SW4, Boot Mode and Configuration Select



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Table 3-39. SW4, Boot Mode Select

Pos 1 BTSEL2	Pos 2 BTSEL1	Pos 3 BTSEL0	HW Code	Boot Mode
OFF	OFF	OFF	0 0 0	NAND Boot(1)
OFF	OFF	ON	0 0 1	ASYNC EMIF
OFF	ON	OFF	0 1 0	MMC/SD Boot
OFF	ON	ON	0 1 1	UART Boot
ON	OFF	OFF	1 0 0	USB Boot
ON	OFF	ON	1 0 1	SPI Boot
ON	ON	OFF	1 1 0	EMAC Boot
ON	ON	ON	1 1 1	HPI Boot

(1) Default setting.

Table 3-40. SW4, Configuration Select

Pos 4 AECFG2	Pos 5 AECFG1	Pos 6 AECFG0	HW Code	Configuration Mode
OFF	OFF	OFF	0 0 0	8-bit AEMIF Configuration(1)
ON	ON	OFF	1 1 0	16-bit AEMIF Configuration

(1) Default setting.

3.4.5 SW5, Board Configuration Select

Switch SW5 is a 6-position switch that configures specific board functions. Figure 3-24 shows the switch as it appears on the EVM.

Figure 3-24. SW5, Board Configuration Select

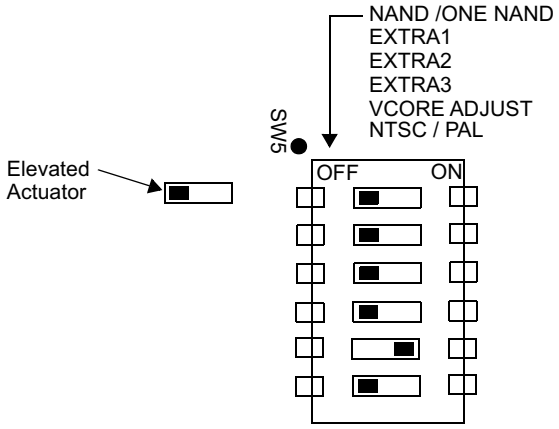


Table 3-41 shows the function of each switch position on SW5.

Table 3-41. SW5, Board Configuration Select

Position	State	Bit Value	Function
1	OFF	0	SELNAND(1)
	ON	1	SELONENAND
2	OFF	0	Reserved(1)
	ON	1	Reserved

(1) Default

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Table 3-41. SW5, Board Configuration Select (continued)

Position	State	Bit Value	Function
3	OFF	0	Reserved(1)
	ON	1	Reserved
4	OFF	0	Reserved(1)
	ON	1	Reserved
5	OFF	0	Vcore = 1.2 V
	ON	1	Vcore = 1.35 V(1)
6	OFF	0	NTSC (CPLD register bit)(1)
	ON	1	PAL (CPLD register bit)

3.4.6 SW6 - SW21, Function Push-Buttons

Switches SW6 through SW21 are push-button momentary switches that are inputs in to the DM368 processor. These switches can be read with software, and their function is determined by the application.

3.4.7 SW22, MSP430 IO0 Push-Button

Switch SW22 is a push-button momentary switch reserved for future use.

3.4.8 SW23, PRTSC Mode Select

Switch SW23 is a 2-position DIP switch that allows the user to select power control and real time clock mode on the DM368. Figure 3-25 shows the switch as it appears on the EVM.

Figure 3-25. SW23, PRTSC Mode Select

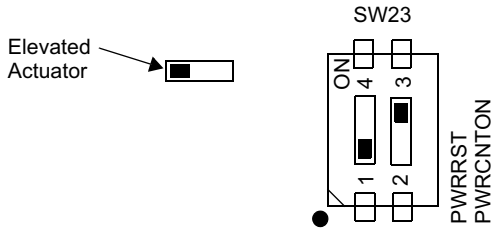


Table 3-42 shows the setting for SW23.

Table 3-42. SW23, PRTSC Mode Select

Position		Signal Level	DM368 Mode
1	2		
0	0	0 0	Reserved
0	1	0 1	RTC and GPIO available(1)
0	1	1 0	Reserved
0	1	1 1	Reserved

(1) Default setting.

3.5 Jumpers

The following sections describe the jumpers on the DM368 EVM.

3.5.1 JP1, Jumper Block

Jumper block JP1 allows the user to connect signals from the DM368 processor to the TVL320AIC3101, U7. The signals on this 9 × 2 header are shown in Table 3-43.

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Table 3-43. JP1, Jumper Block

Pin	Signal Name	Pin	Signal Name
2	AIC_McBSP_CLKX	1	AIC_BCLK, U7, Pin 2
4	AIC_McBSP_CLKR	3	AIC_BCLK, U7, Pin 2
6	AIC_McBSP_FSX	5	AIC_WCLK
8	AIC_McBSP_FSR	7	AIC_WCLK
10	AIC_McBSP_DX	9	AIC_DIN
12	AIC_McBSP_DR	11	AIC_DOUT
14	I2C_DATA	13	SDA, U7, Pin 9
16	I2C_SCLK	15	SDL, U7, Pin 8
18	Ground	17	Ground

3.5.2 JP2, Unpopulated Jumper

Jumper JP2 is unpopulated and not used.

3.5.3 JP28, Unpopulated Jumper

Jumper JP28 is unpopulated and not used.

3.5.4 JP29, Unpopulated Jumper

Jumper JP29 is unpopulated and not used.

3.5.5 J26, USB ID Select

The J26 jumper is used to pull the USB_ID line on USB connector high or low. The selections are shown in Figure 3-26 and Table 3-44.

Figure 3-26. J26, USB ID Select

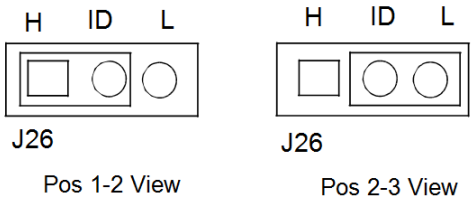


Table 3-44. J26, USB ID Select

Position	Function
1 - 2	USB_ID pulled high(1)
2 - 3	USB_ID pulled low

(1) Factory-shipped configuration

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3.5.6 J27, U14 LL8 Voltage Select

The J27 jumper is used to select the voltage input to U14, Pin 27, LL8. The selections are shown in Figure 3-27 and Table 3-45.

Figure 3-27. U14 LL8 Voltage Select

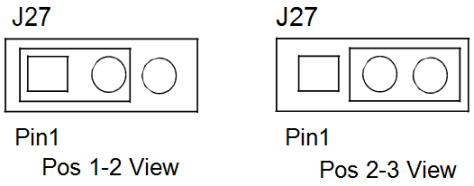


Table 3-45. U14 LL8 Voltage Select

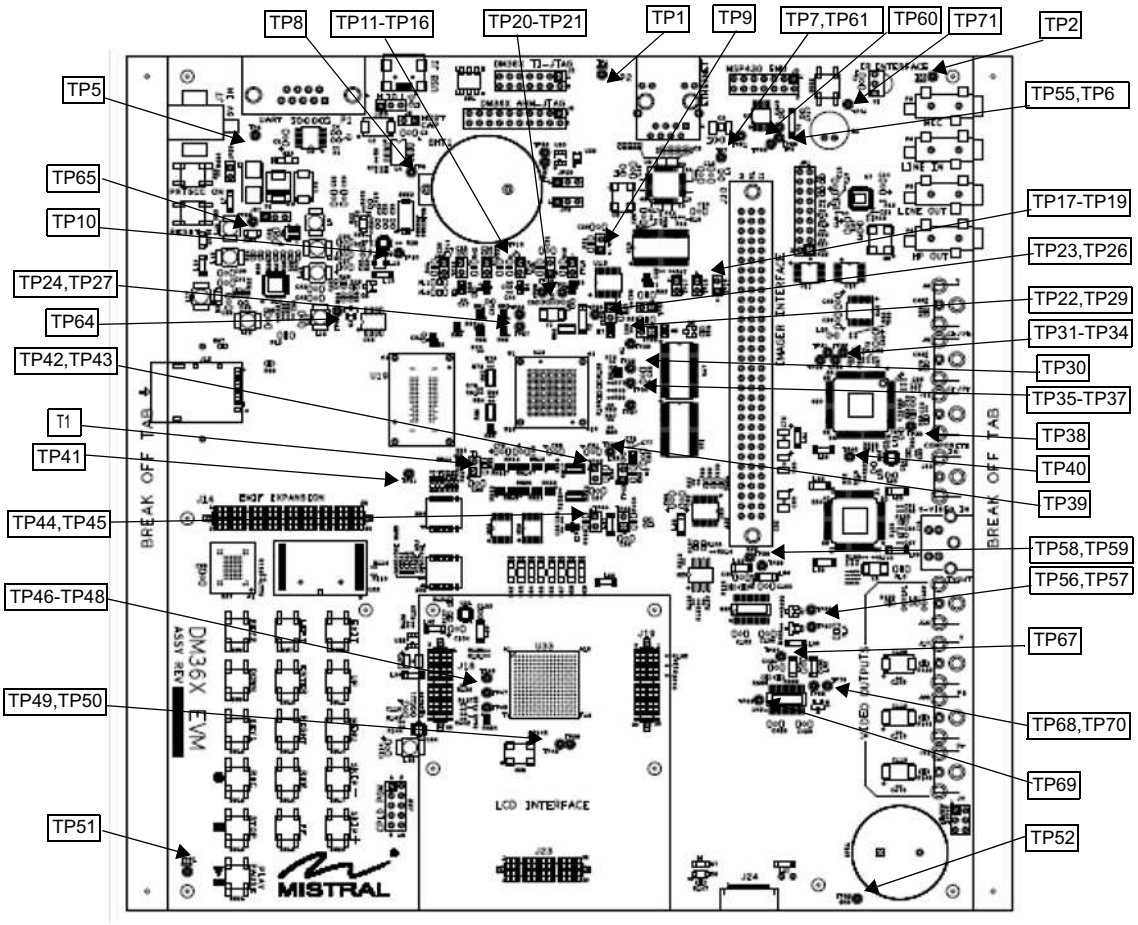
Position	Function
1 - 2	VCC5_IN Selected(1)
2 - 3	VCC_3V3 Selected

(1) Factory-shipped configuration

3.6 Test Points

The EVM has 55 test points. Figure 3-28 and Figure 3-29 identify the position of each test point. Table 3-46 lists each test point and the signal appearing on that test point.

Figure 3-28. DM368 EVM, Top Side Test Points



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Figure 3-29. DM368 EVM, Bottom Side Test Points

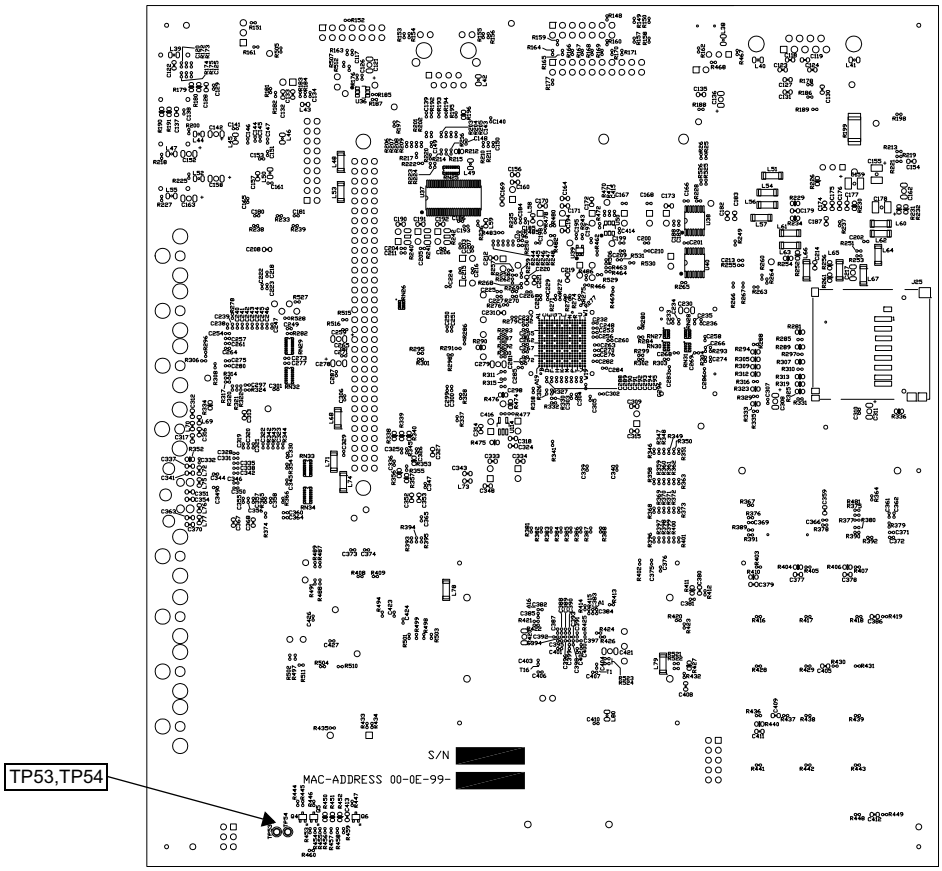


Table 3-46. DM368 EVM Test Points

TP#	Schematic Page	Signal	TP#	Schematic Page	Signal
TP1	52	GND	TP46	20	U33A, F2, B1.IO_21
TP2	52	GND	TP47	23	U33A, P7, B4.IO_47
TP5	52	VCC_5V	TP48	23	U33A, P11, B4.IO_21
TP6	44	U2, Pin 6, MP430_IO2	TP49	20	U33A, M4, B1.IO_58
TP7	43	U5, Pin 25, INT#PHYAD0	TP50	20	U33A, P2, B1.IO_65
TP8	18	VCC_3V3, VBUS_OCn2, U4, Pin 5	TP51	52	GND
TP10	47	U9, Pin6, PWMON	TP52	52	GND
TP20	10	U18-13, L1, MXI1	TP53	41	J24, Pin 11,12, BAT_CHG
TP21	10	U18-13, K1, MXO1	TP54	41	J24, Pin 17
TP24	13	U18-14, R1, RSV1(NC)	TP55	44	U2, Pin 7, MP430_IO5
TP26	10	DM360 RESETn, U18-13, H3	TP56	50	CPU_VCC_3V3
TP27	13	U18-14, R4, RSV2(NC)	TP57	50	CPU_VCC_3V3
TP30	13	U18-14, A1, RSV0(NC)	TP58	50	U30, Pin 23/24, 1OUT_1/2
TP31	35	U20, Pin 24, HSOUT	TP59	50	U30, Pin 17/18, 2OUT_1/2
TP32	35	U20, Pin 22, FIDOUT	TP60	44	U2, Pin 5, MP430_IO1
TP33	35	U20, Pin 25, SOGOUT	TP61	44	U2, Pin 2, MP430_IO0
TP34	35	U20, Pin 23, VSOUT	TP64	48	U14, Pin 34, CIN
TP35	12	U18-9, C9, LINEO	TP65	48	U14, Pin 36, SW7
TP36	11	U18-10, A6, ADC_CH5	TP67	51	U42, Pin 23/24, 1OUT1_1/2

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Table 3-46. DM368 EVM Test Points (continued)

TP#	Schematic Page	Signal	TP#	Schematic Page	Signal
TP37	11	U18-10, D7, ADC_CH4	TP68	51	U42, Pin 17/18, 2OUT1/2
TP38	35	U20, Pin 80, EXT_CLK	TP69	51	U42, Pin 4, 1EN
TP39	7	VREF, U18-3, D11	TP70	51	PWCTR_OUT1
TP40	52	GND	TP71	44	MSP430_3V3
TP41	52	GND			

There are 18 power test points on the EVM. These test points provide a convenient mechanism to check the multiple power supplies of the EVM. Table 3-47 shows the voltages for each test point and what the supply is used for.

Table 3-47. Power Test Points

Access Test Point	Schematic Page	Voltage	Shunt	Power Domain
T1	13	+1.8 V	0.02 Ω	VCC_1V8, U18-14, R12, CPU_VDD_DDR
TP9	13	+3.3 V	0.02 Ω	VCC_3V3, U18-14, P5, CPU_VDDSHV
TP11	13	+1.2 V	0.02 Ω	VCC_1V2, U18-14, R3
TP12	4	+3.3 V	0.02 Ω	VCC_3V3
TP13	4	+1.8 V	0.02 Ω	VCC_1V8
TP14	13	+1.8 V	0.02 Ω	VCC_1V8, U18-14, N4
TP15	13	+1.2 V	0.02 Ω	VCC_1V2, U18-14, J14, CPU_VDD
TP16	11	+1.8 V	0.02 Ω	VCC_1V8, U18-10, G9
TP17	13	+1.8 V	0.02 Ω	VCC_1V8, U18-14, E5
TP18	14	+1.8 V	0.02 Ω	1V8_BB_UP, U18-11, K6
TP19	14	+1.2 V	0.02 Ω	1V2_BB_UP, U18-11, K7,J6
TP22	12	+1.8 V	0.02 Ω	VCC_1V8, U18-9, E9
TP23	10	+1.8 V	0.02 Ω	VCC_1V8, U18-13, L6
TP29	12	+3.3 V	0.02 Ω	VCC_3V3, U18-9, E10
TP42	13	+3.3 V	0.02 Ω	VCC_3V3, U18-14, R14, CPU_VDDSHV10
TP43	7	+1.8 V	0.02 Ω	VCC_1V8, U18-3, D10
TP44	7	+1.2 V	0.02 Ω	VCC_1V2, U18-3, E12
TP45	13	+1.2 V	0.02 Ω	VCC_1V2, U18-14, M14, CPU_VDDS

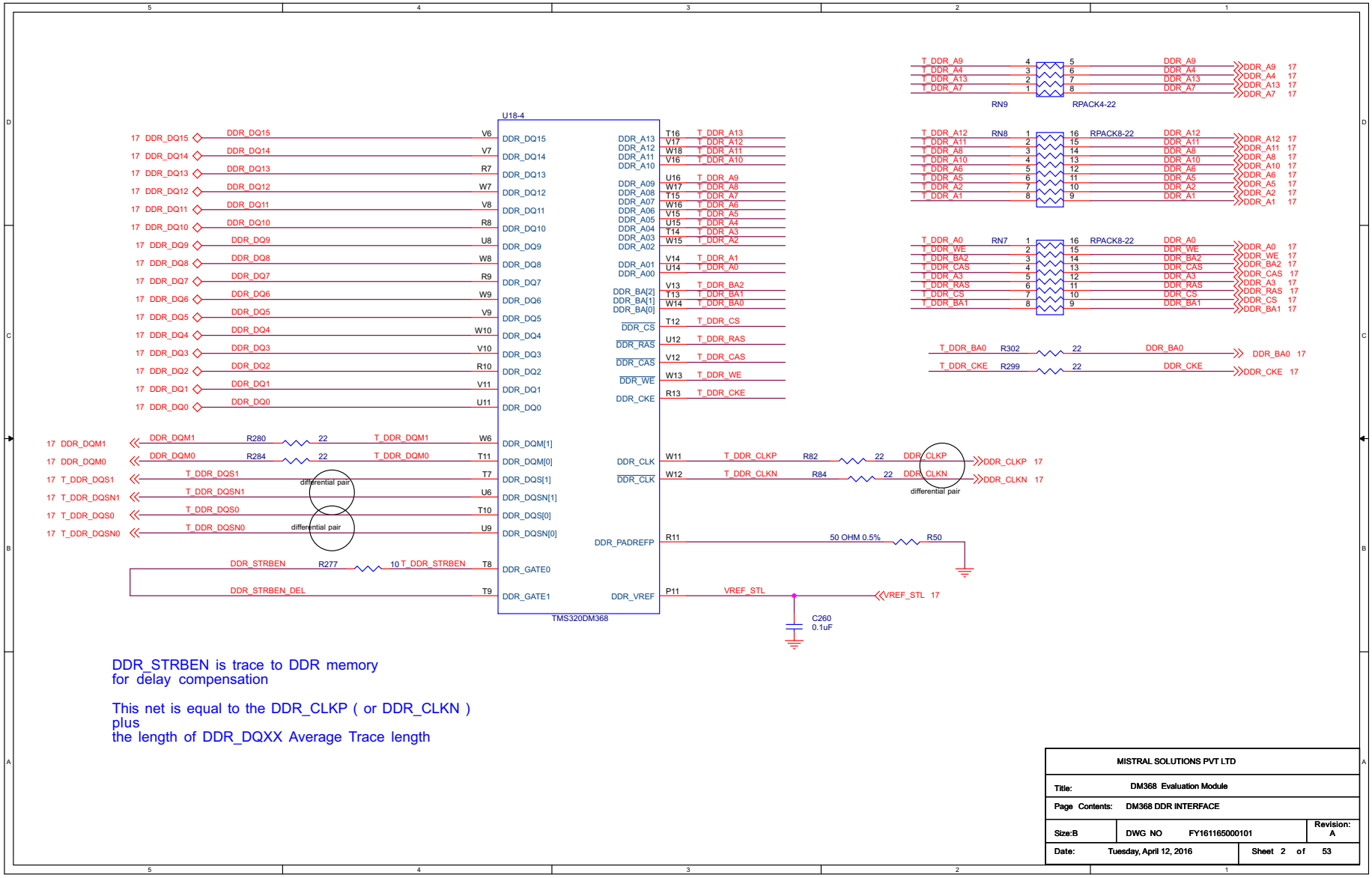
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Schematics

This appendix contains the schematics for the DM368 EVM.

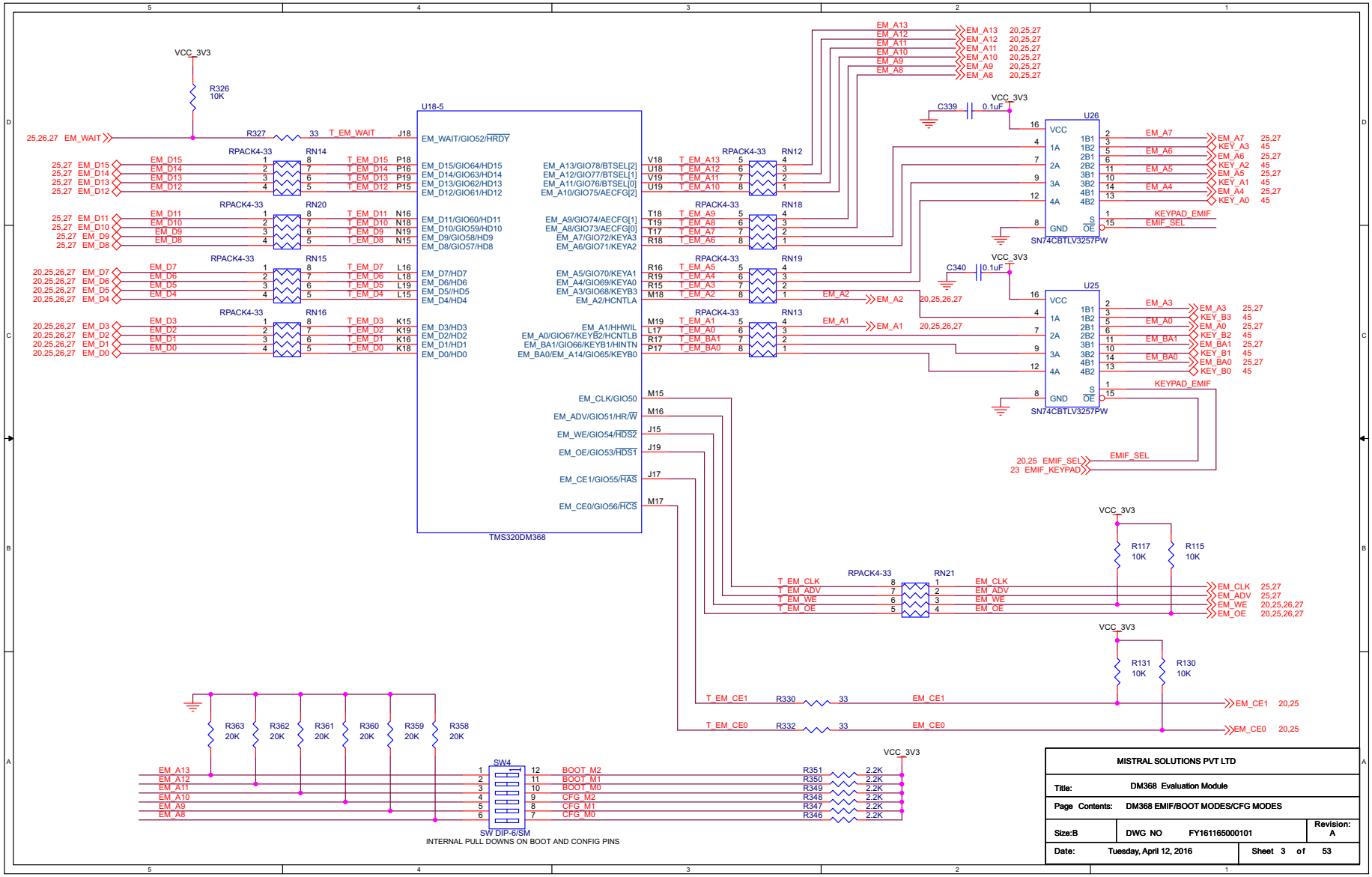
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Figure A-1. DM368 DDR Interface



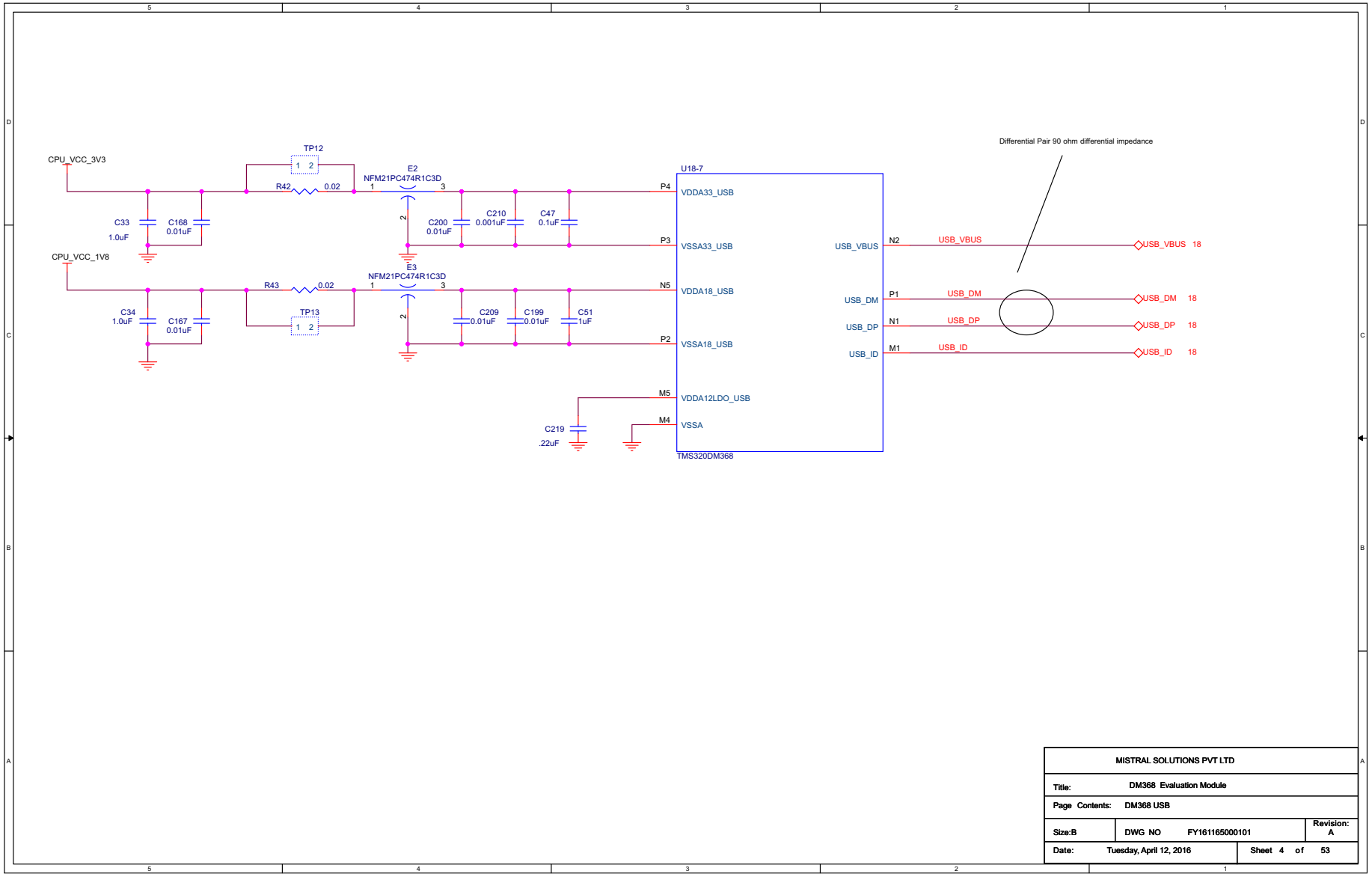
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Figure A-2. DM368 EMIF/Boot Modes/CFG Modes



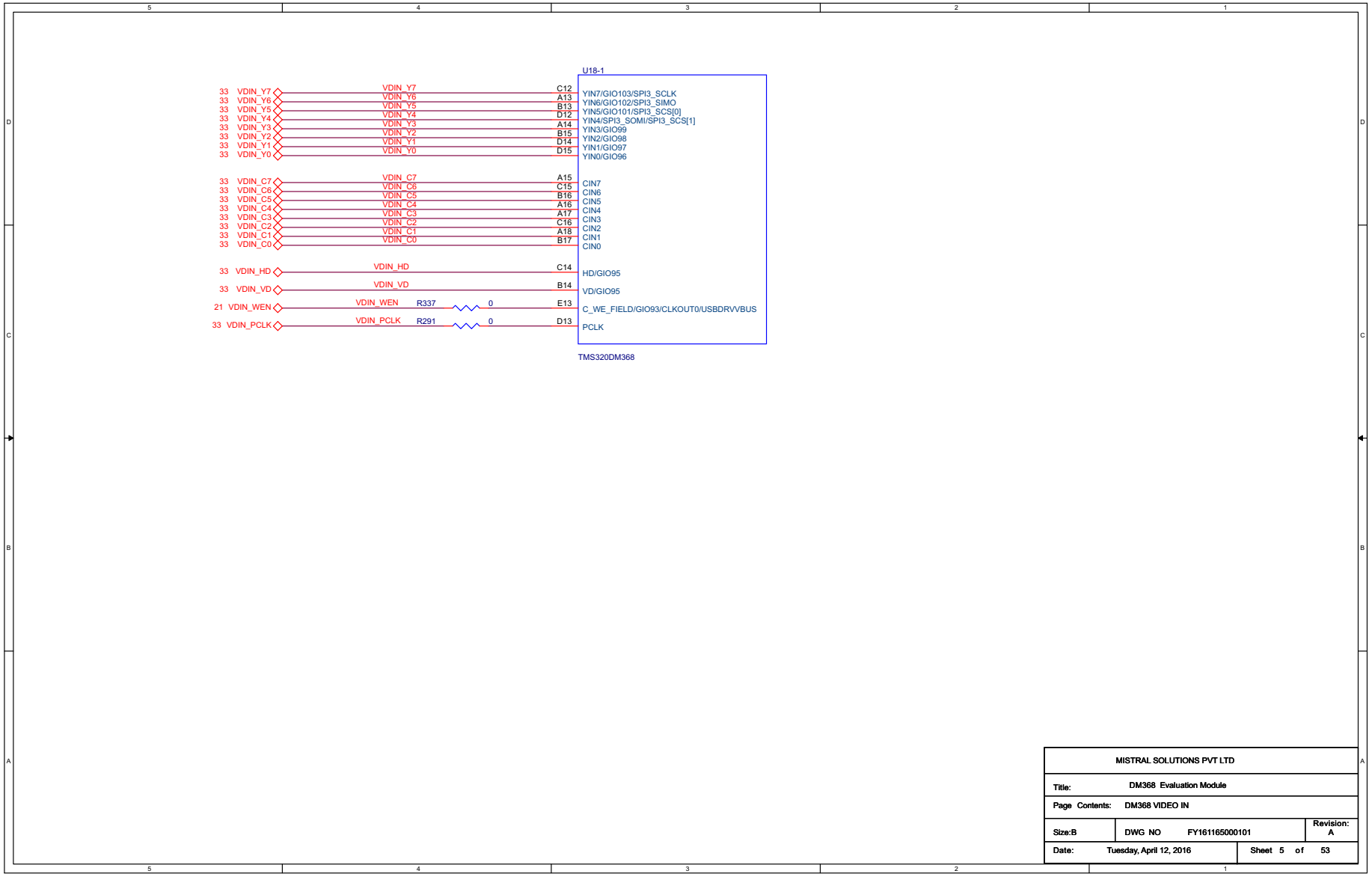
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Figure A-3. DM368 USB



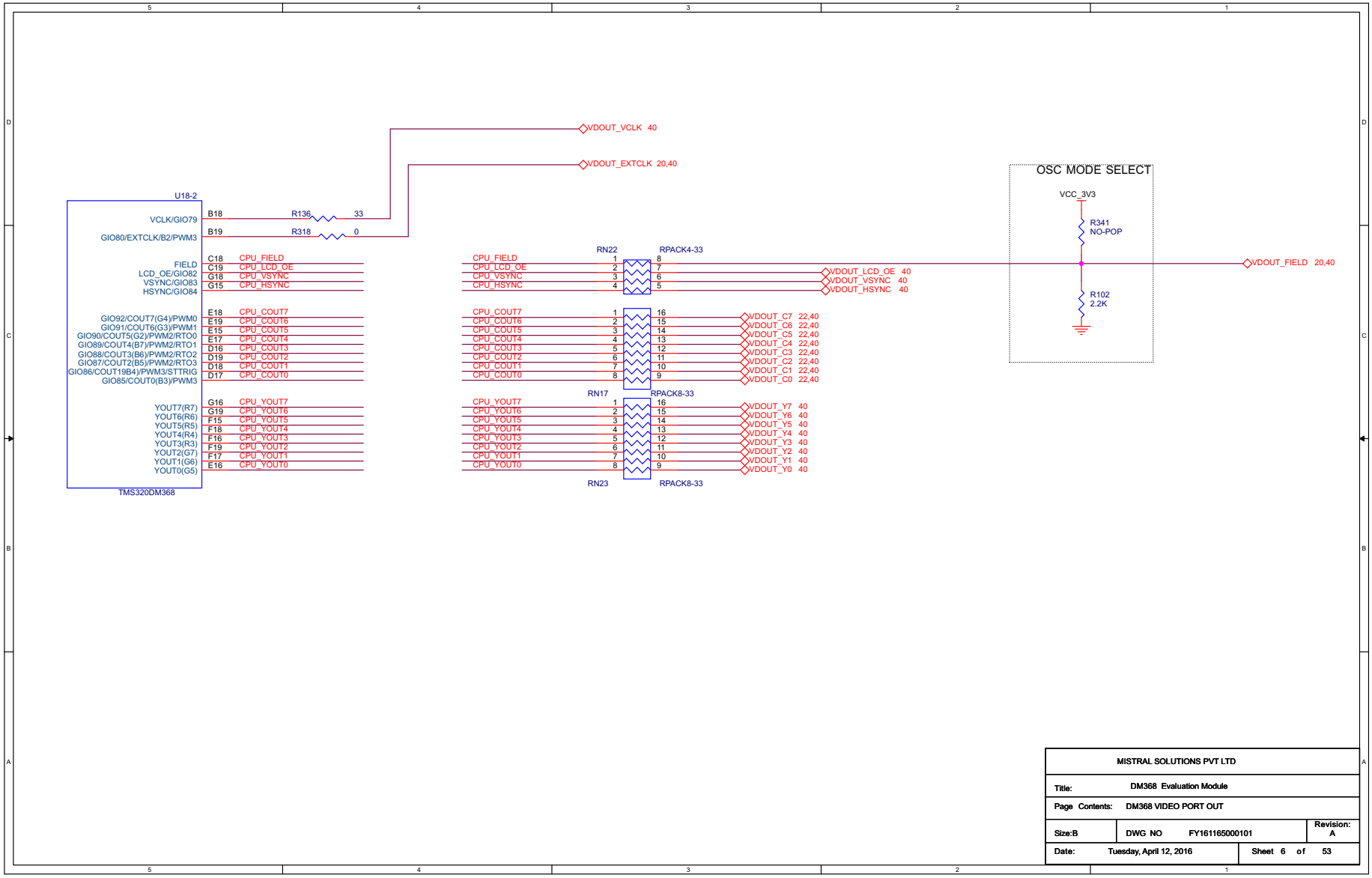
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Figure A-4. DM368 Video In



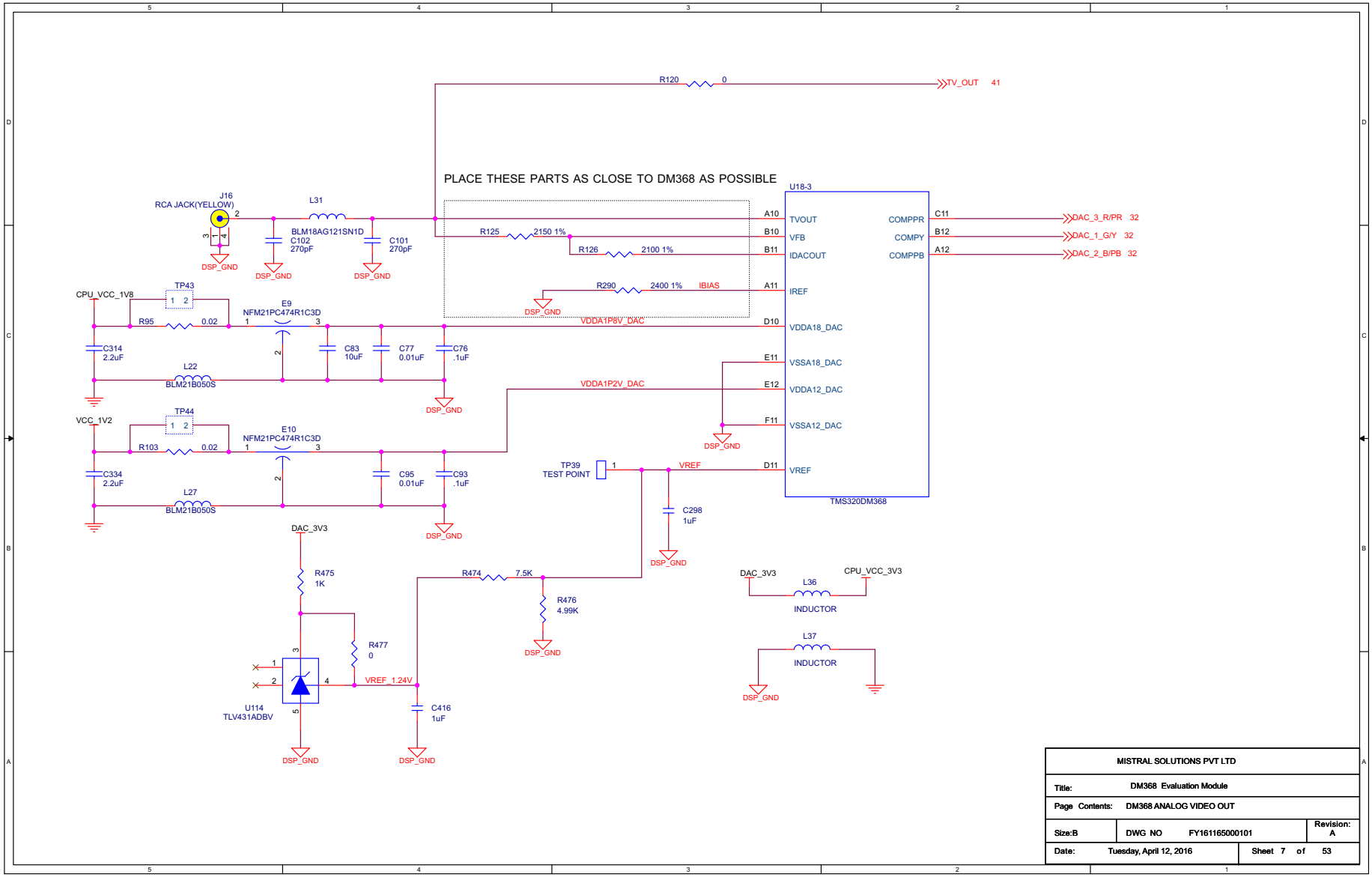
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Figure A-5. DM368 Video Port Out



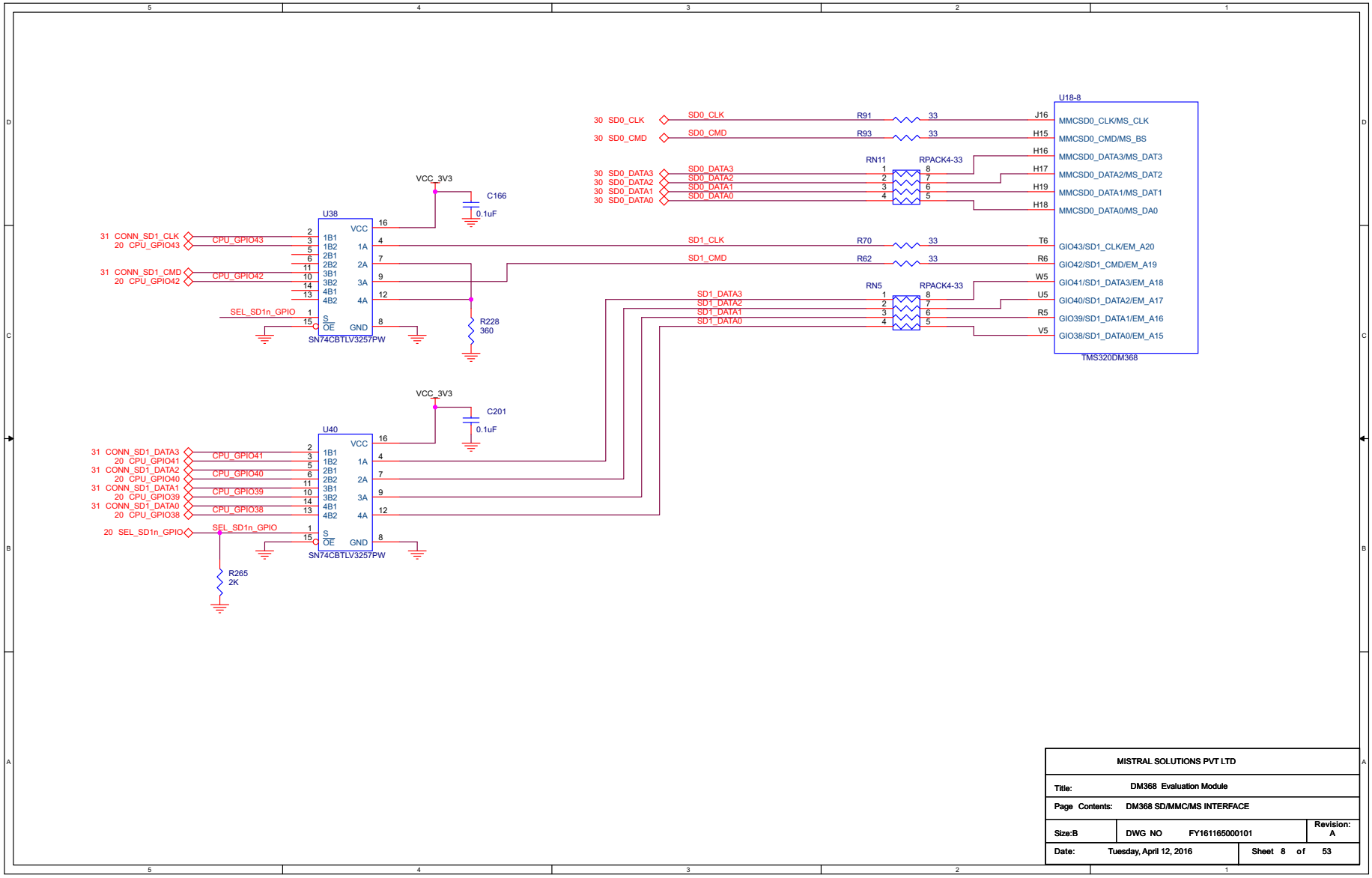
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Figure A-6. DM368 Analog Video Out



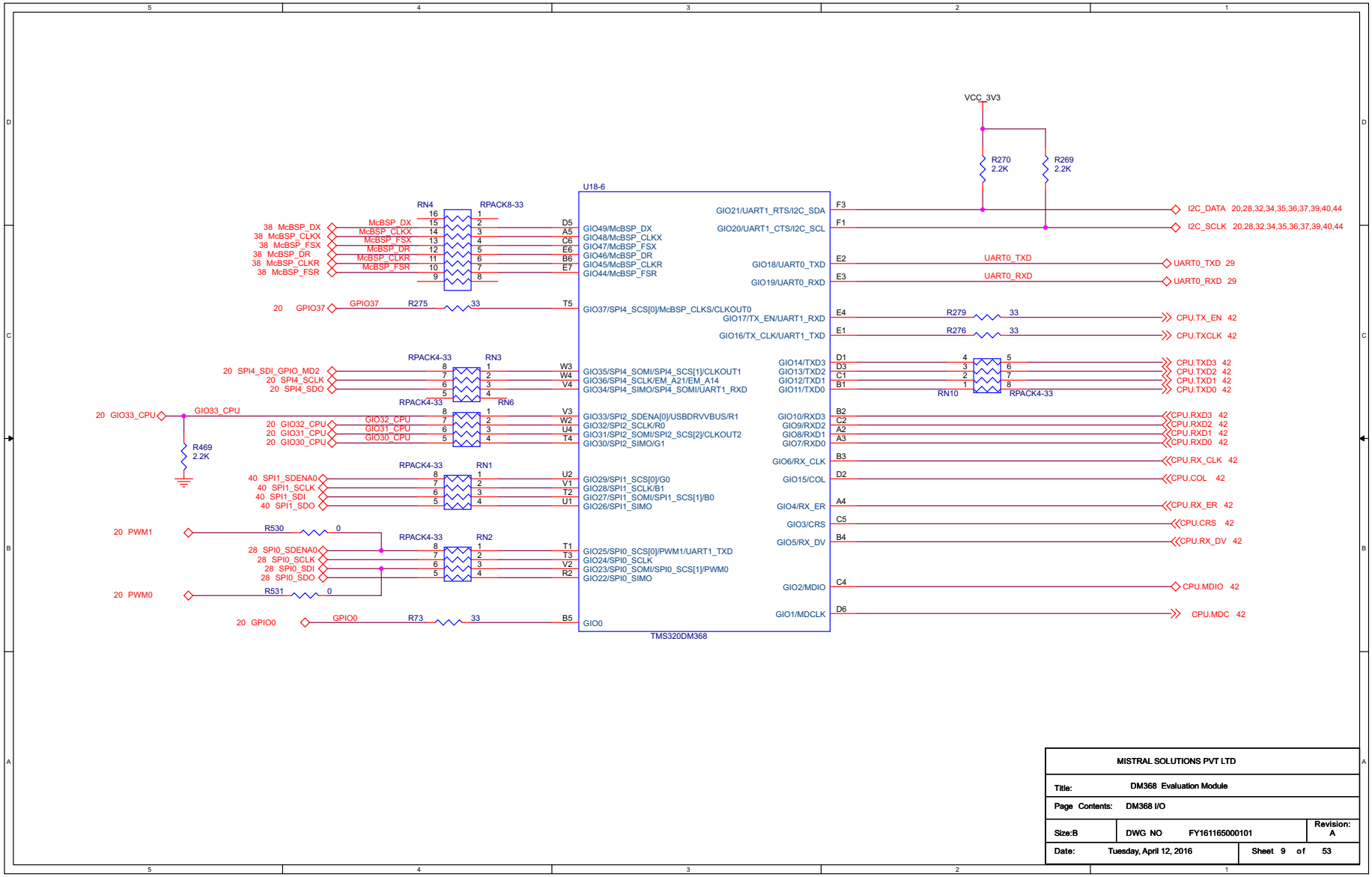
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Figure A-7. DM368 SD/MMC/MS Interface



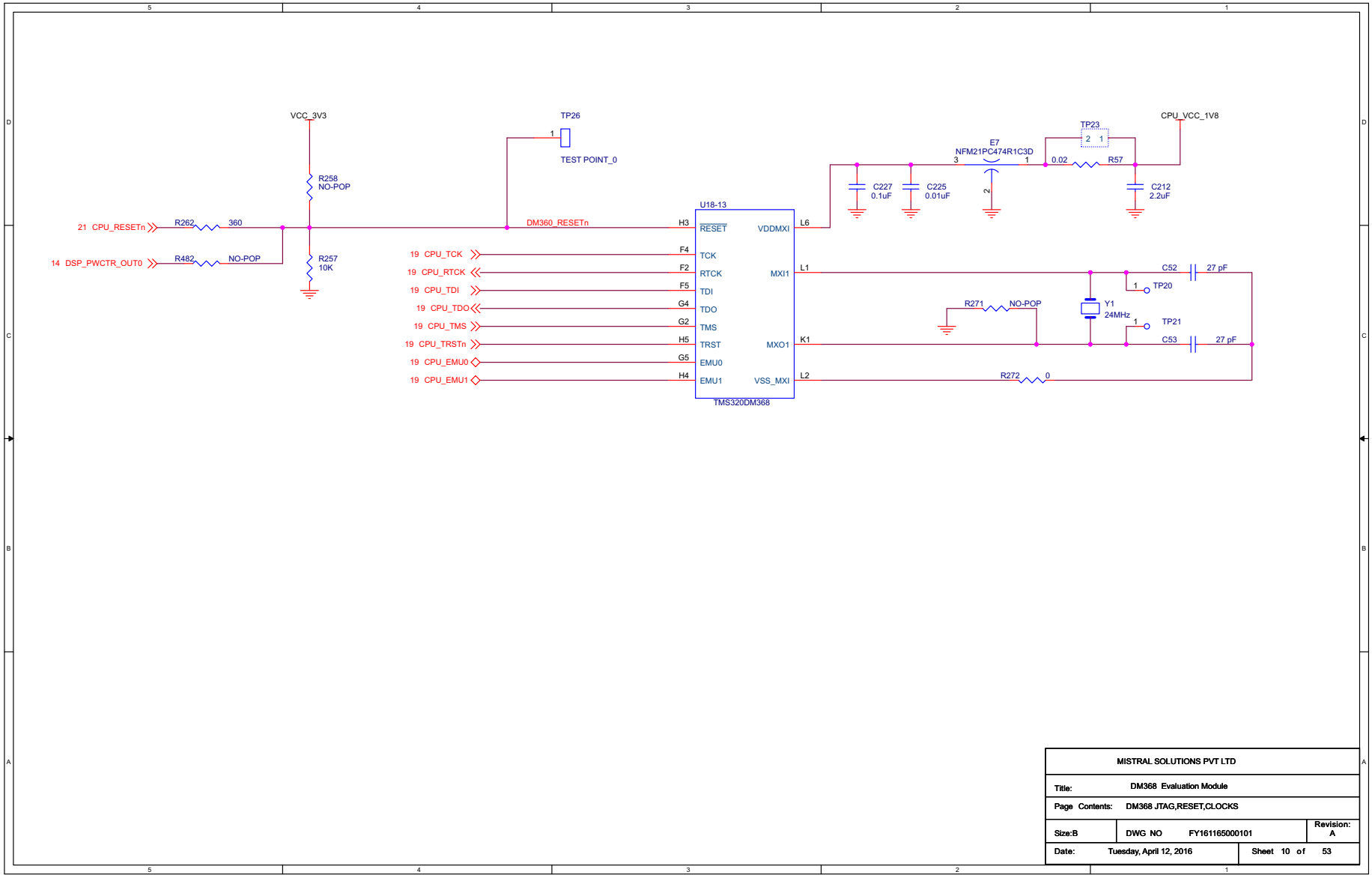
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Figure A-8. DM368 I/O



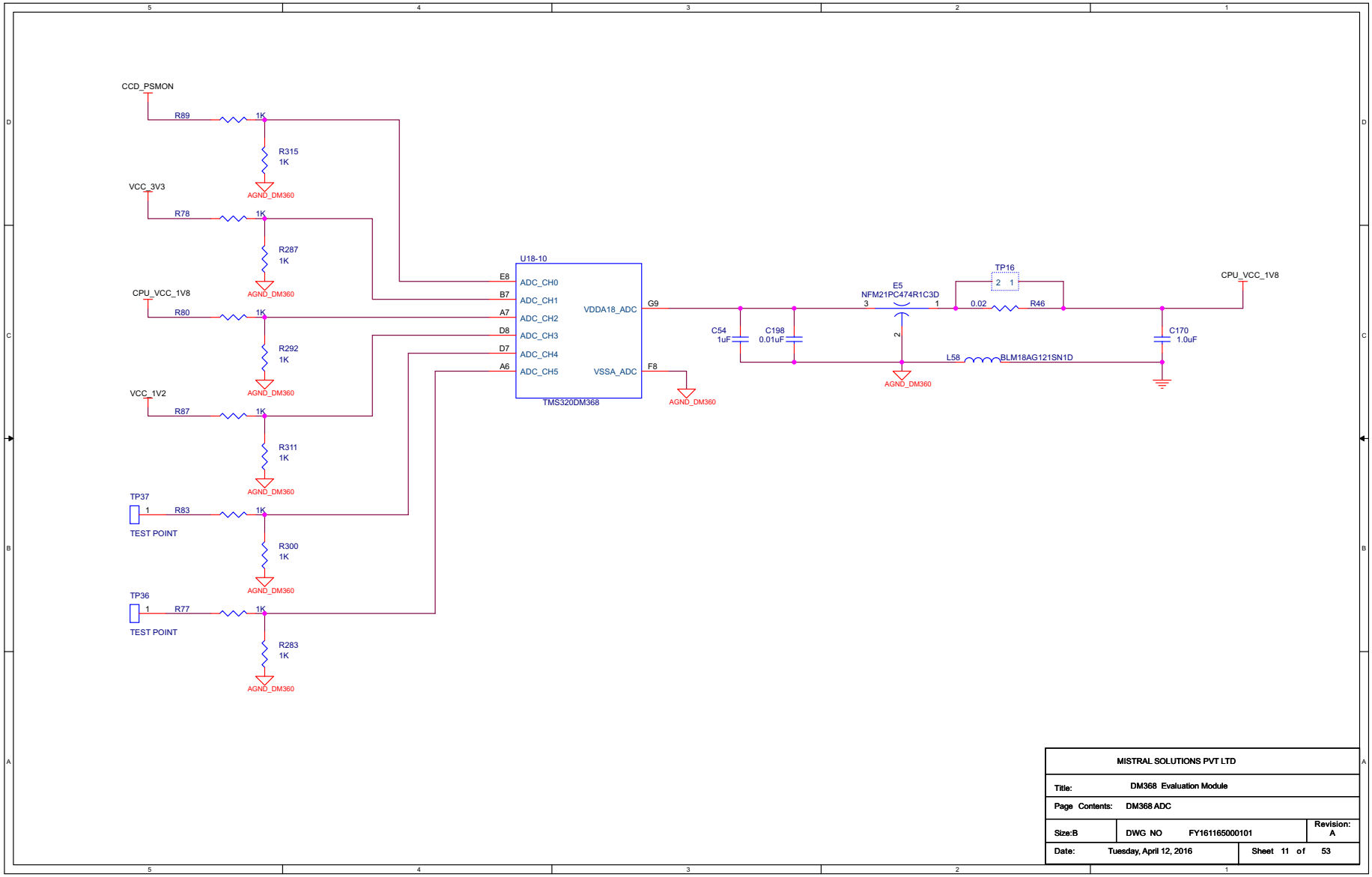
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Figure A-9. DM368 JTAG, Reset, Clocks



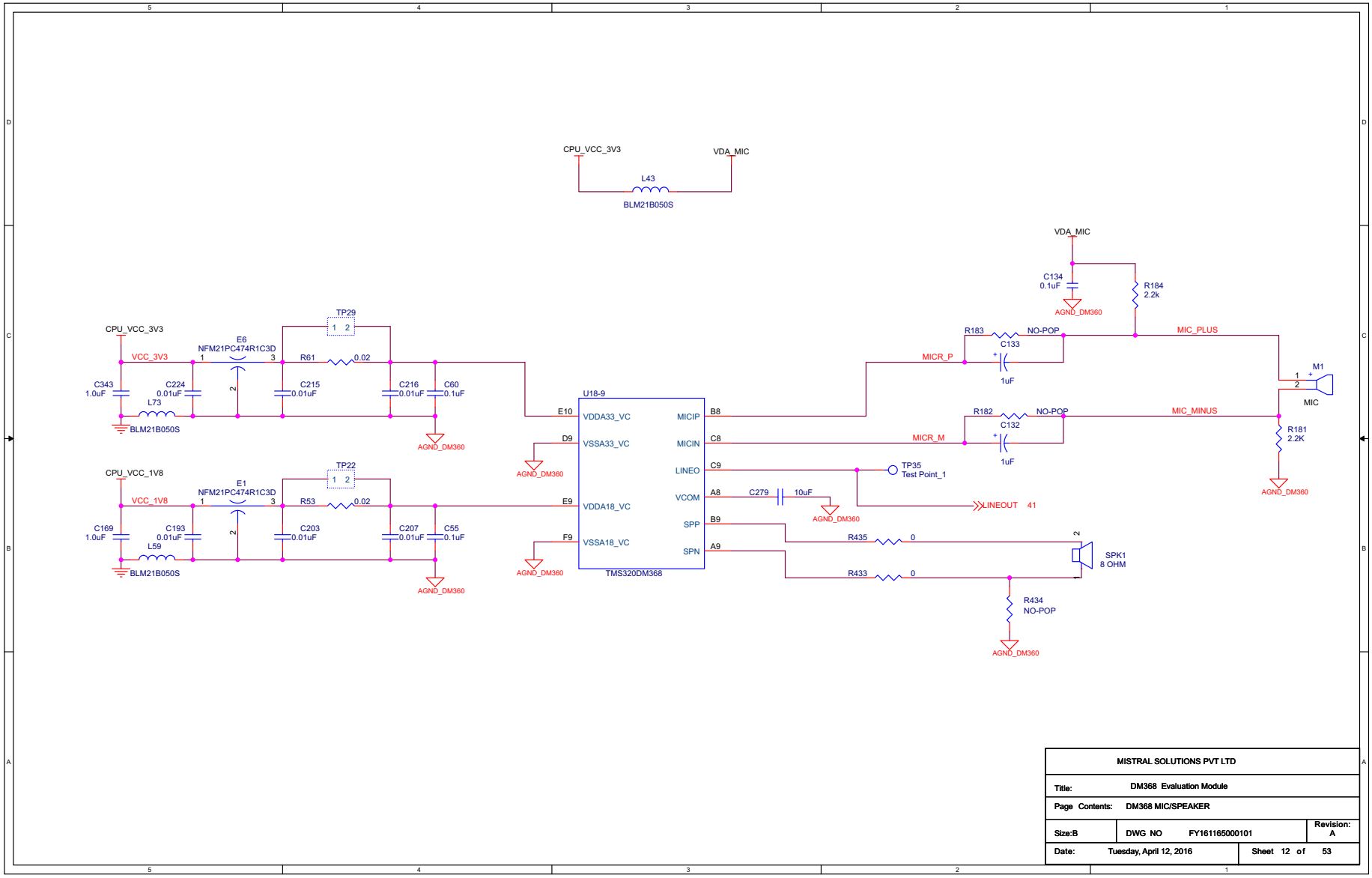
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Figure A-10. DM368 ADC



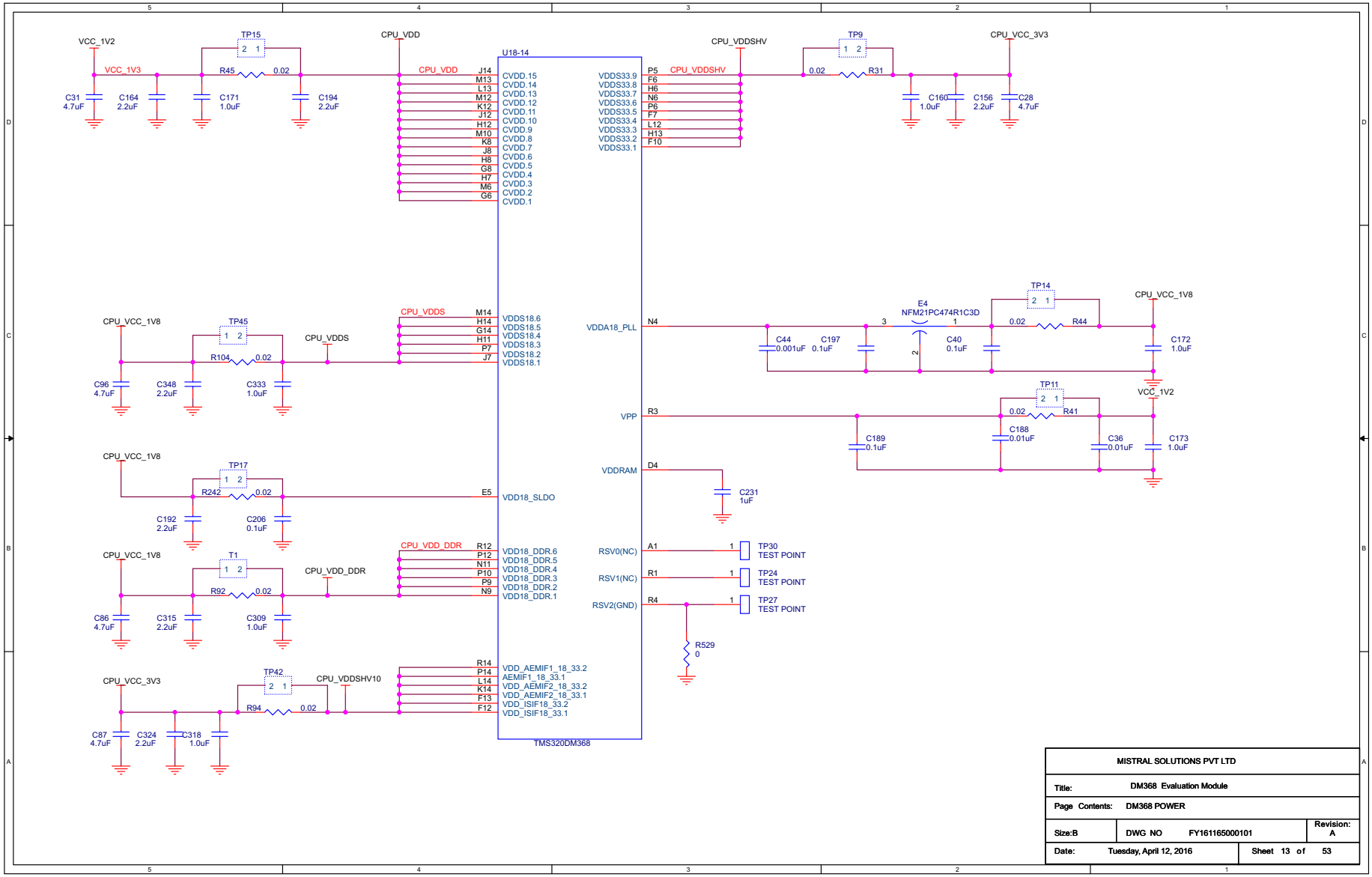
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Figure A-11. DM368 MIC and Speaker



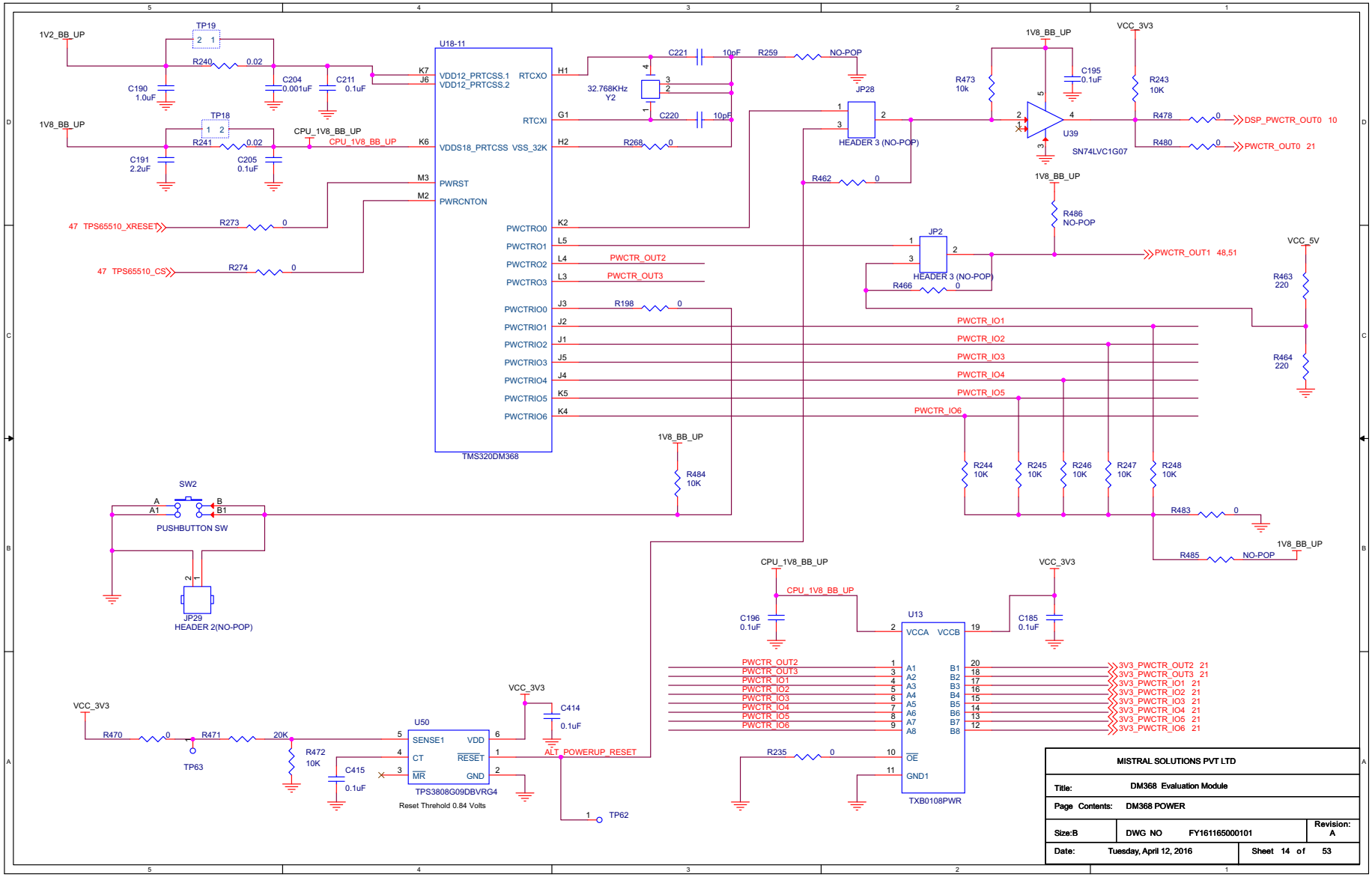
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Figure A-12. DM368 Power (1 of 3)



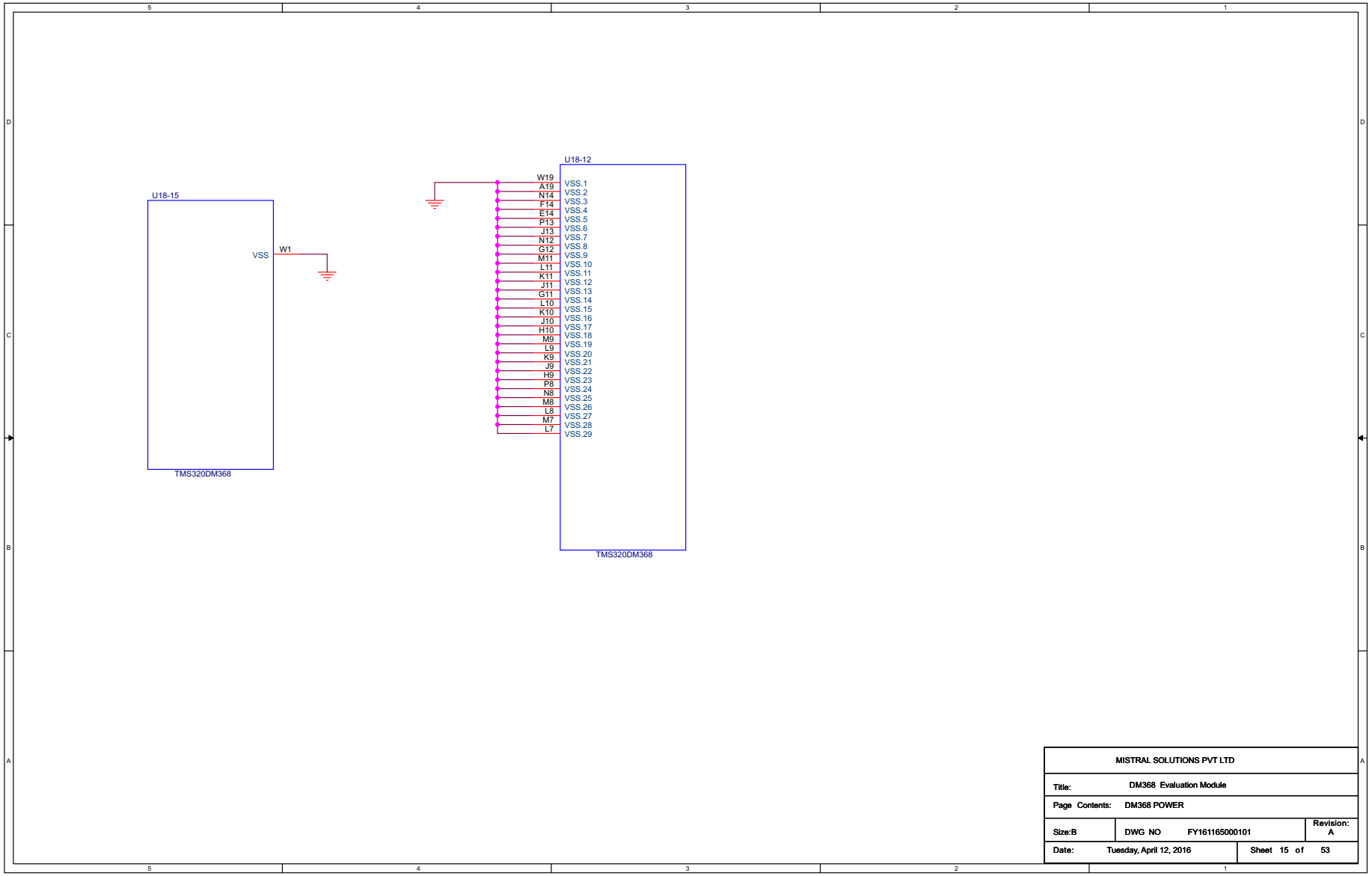
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Figure A-13. DM368 Power (2 of 3)



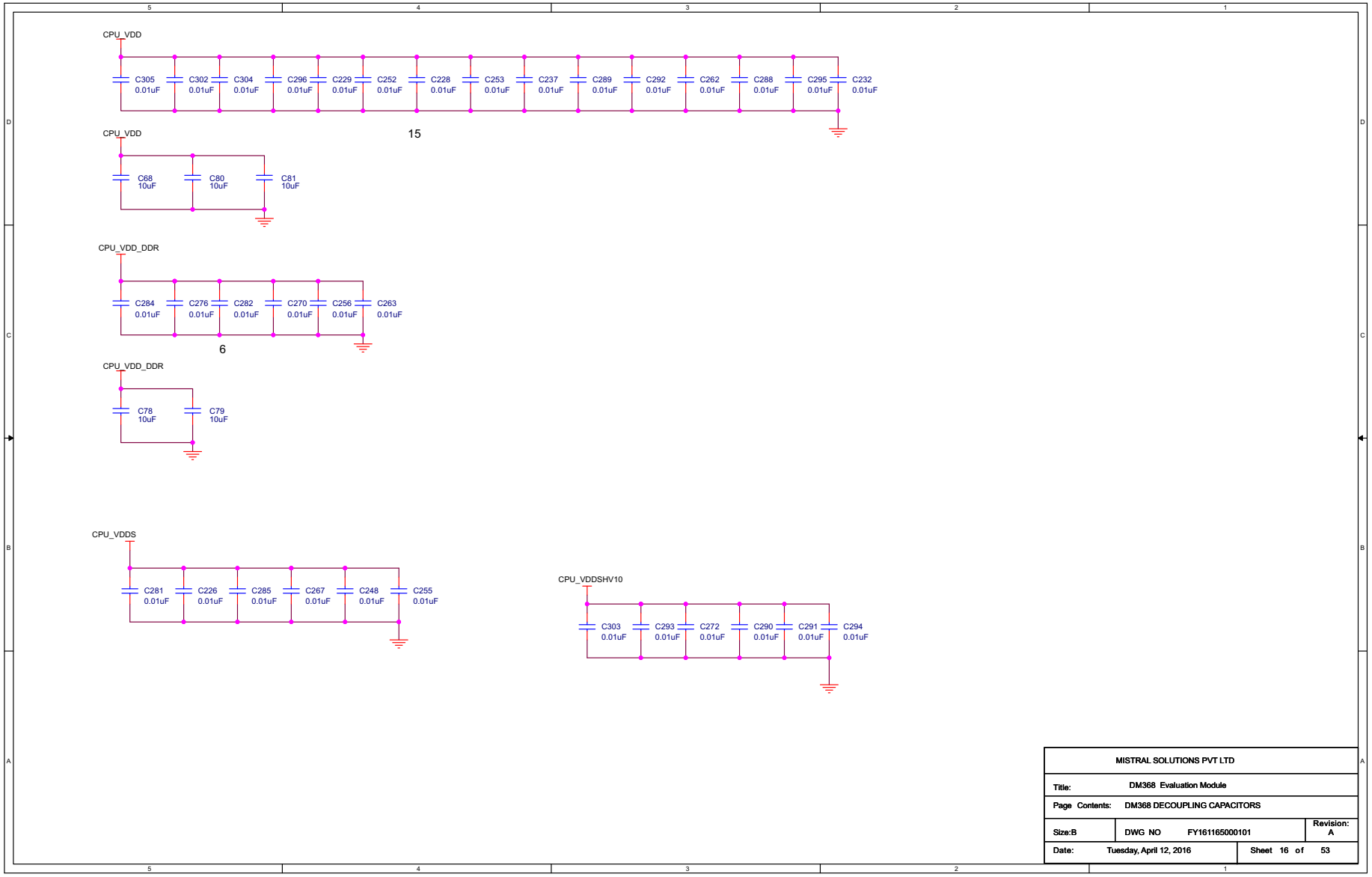
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Figure A-14. DM368 Power (3 of 3)



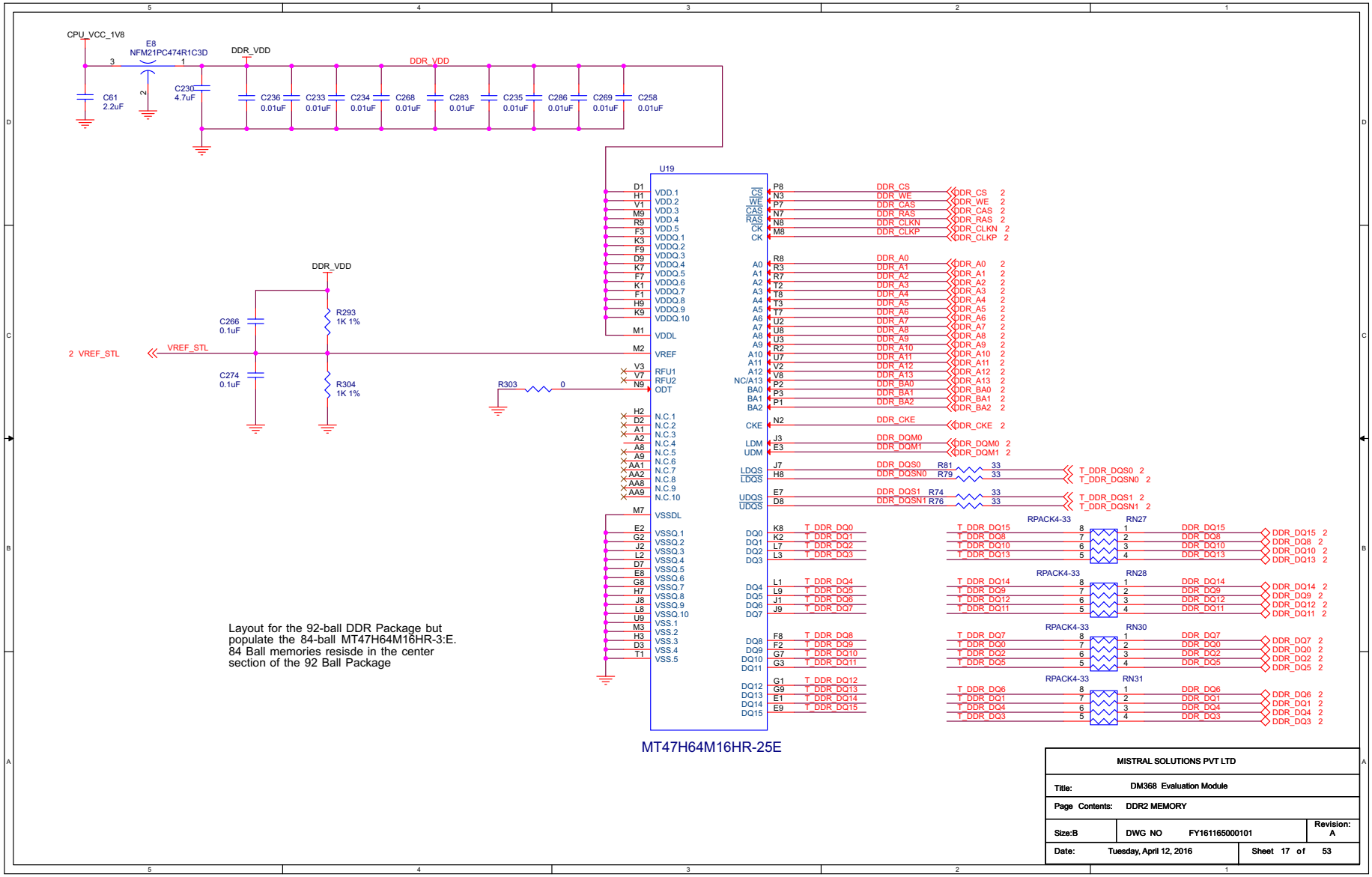
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Figure A-15. DM368 Decoupling Capacitors



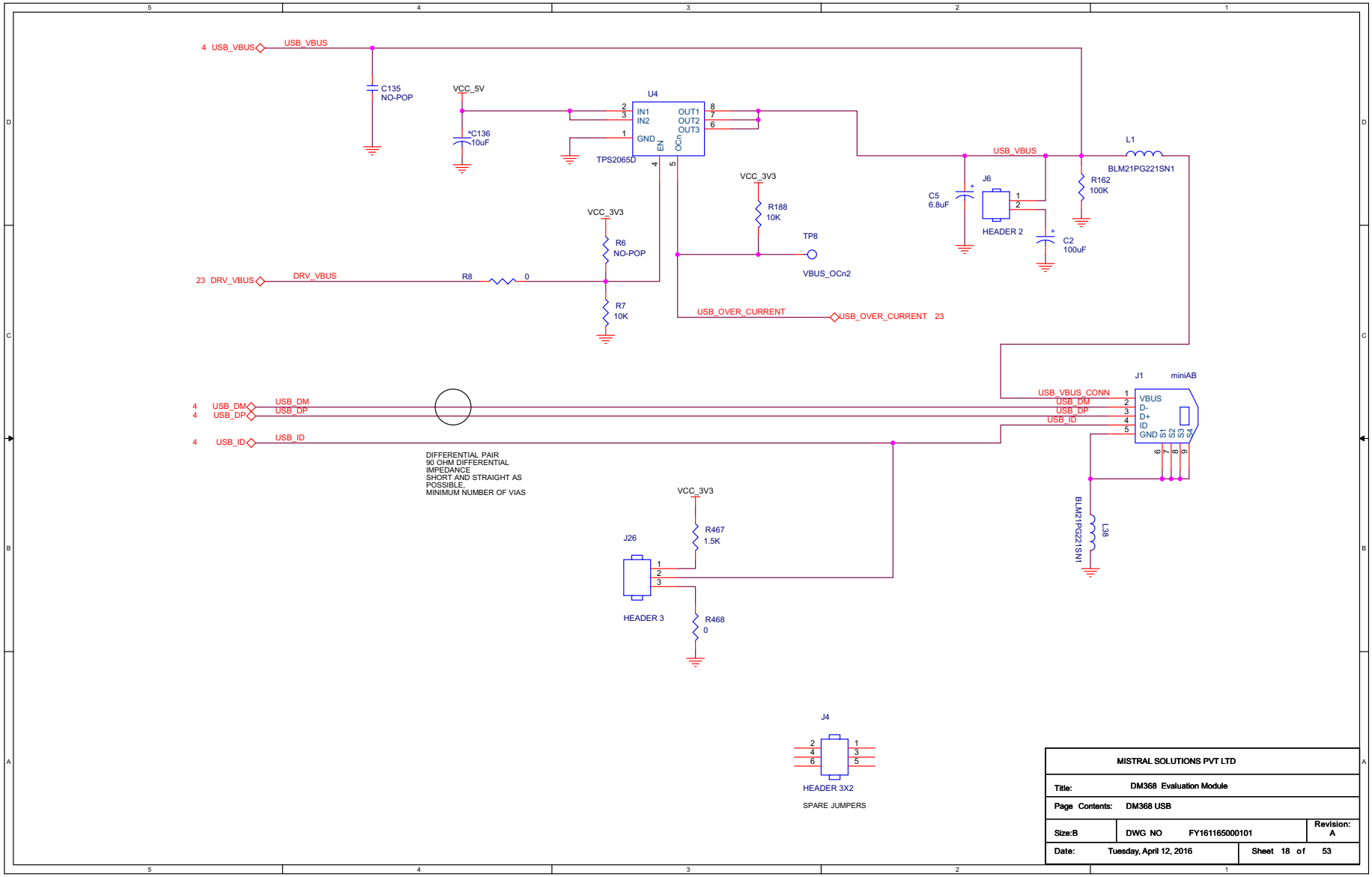
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Figure A-16. DM368 DDR2 Memory



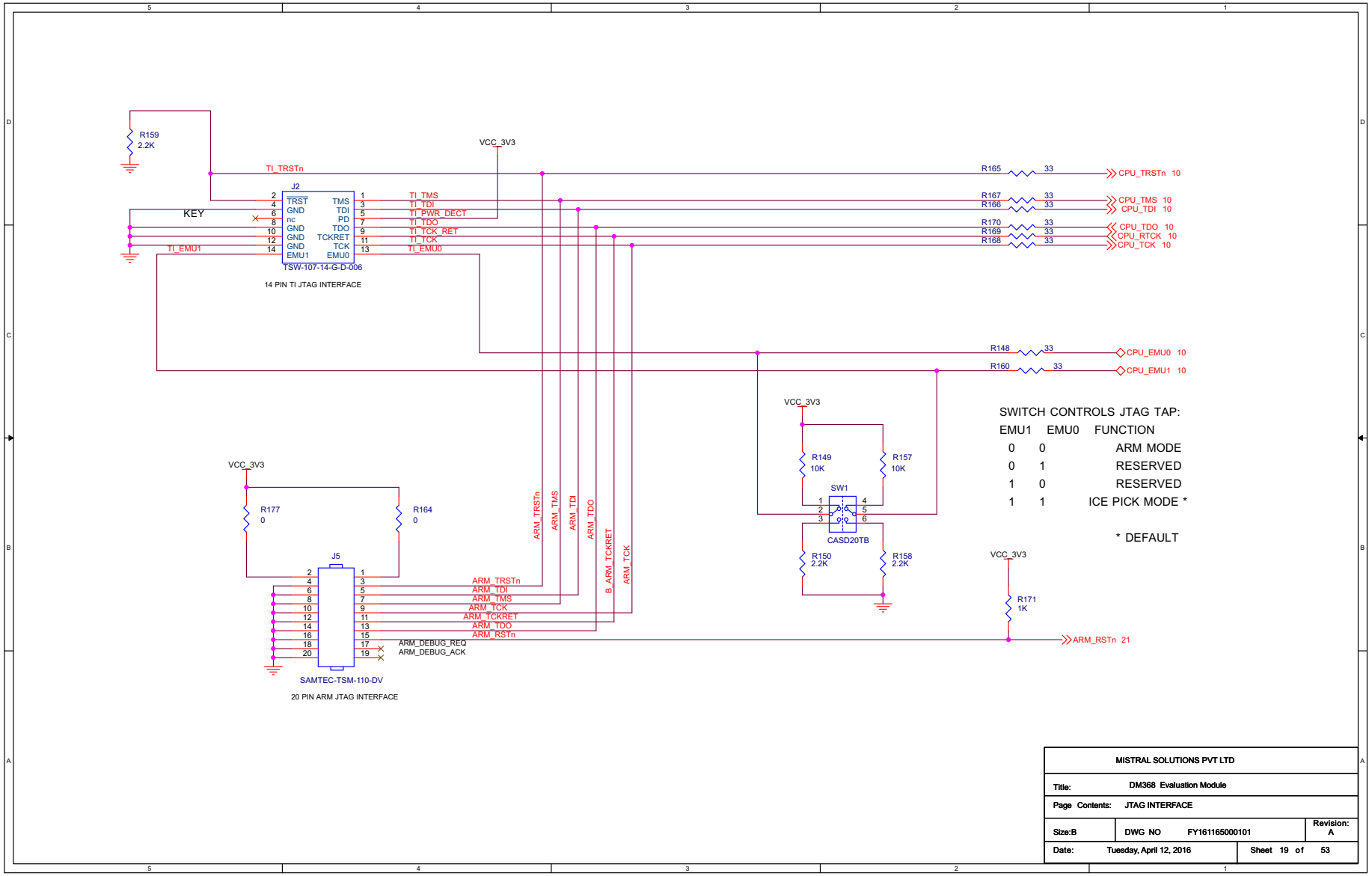
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Figure A-17. DM368 USB



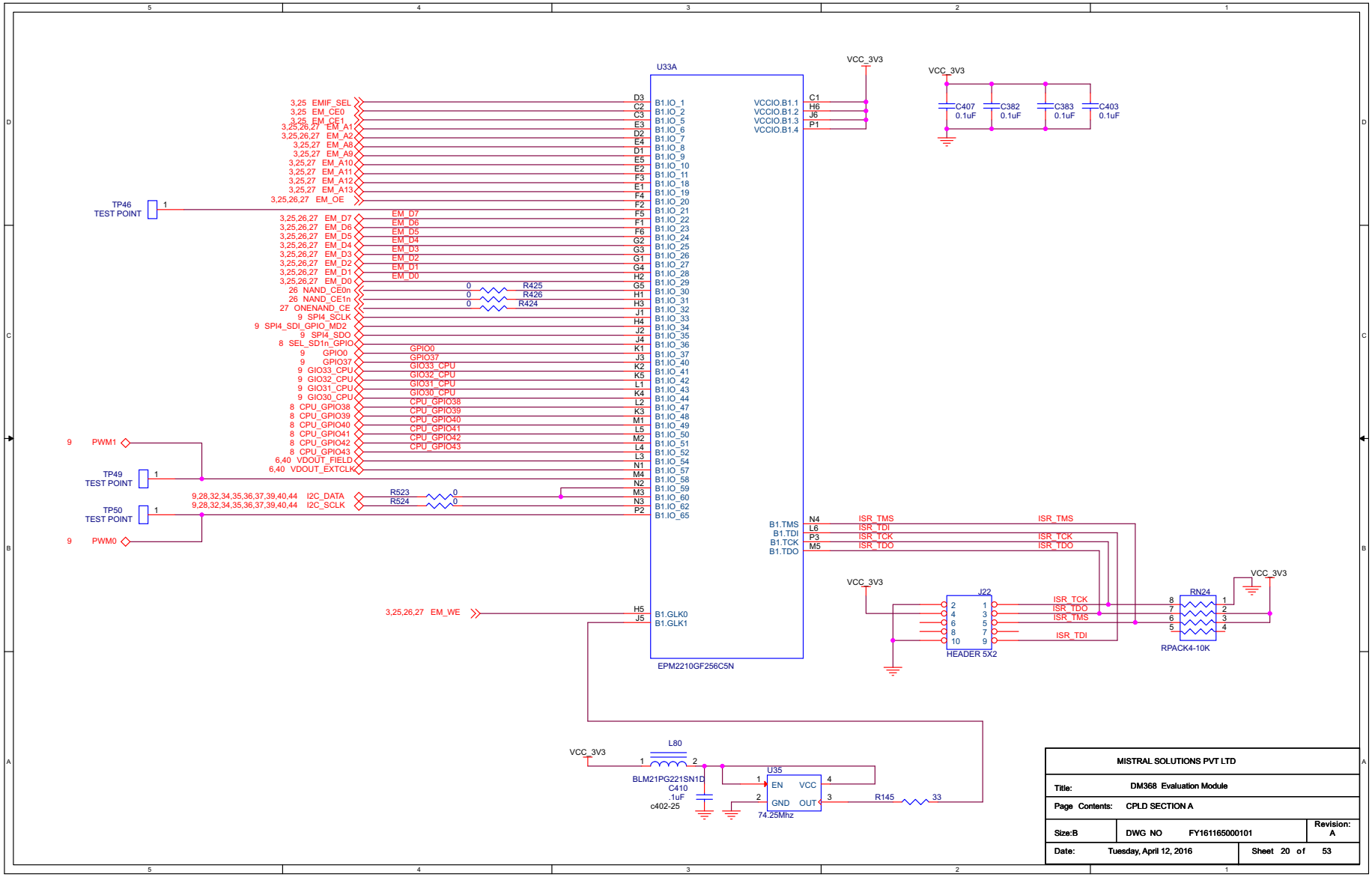
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Figure A-18. JTAG Interface



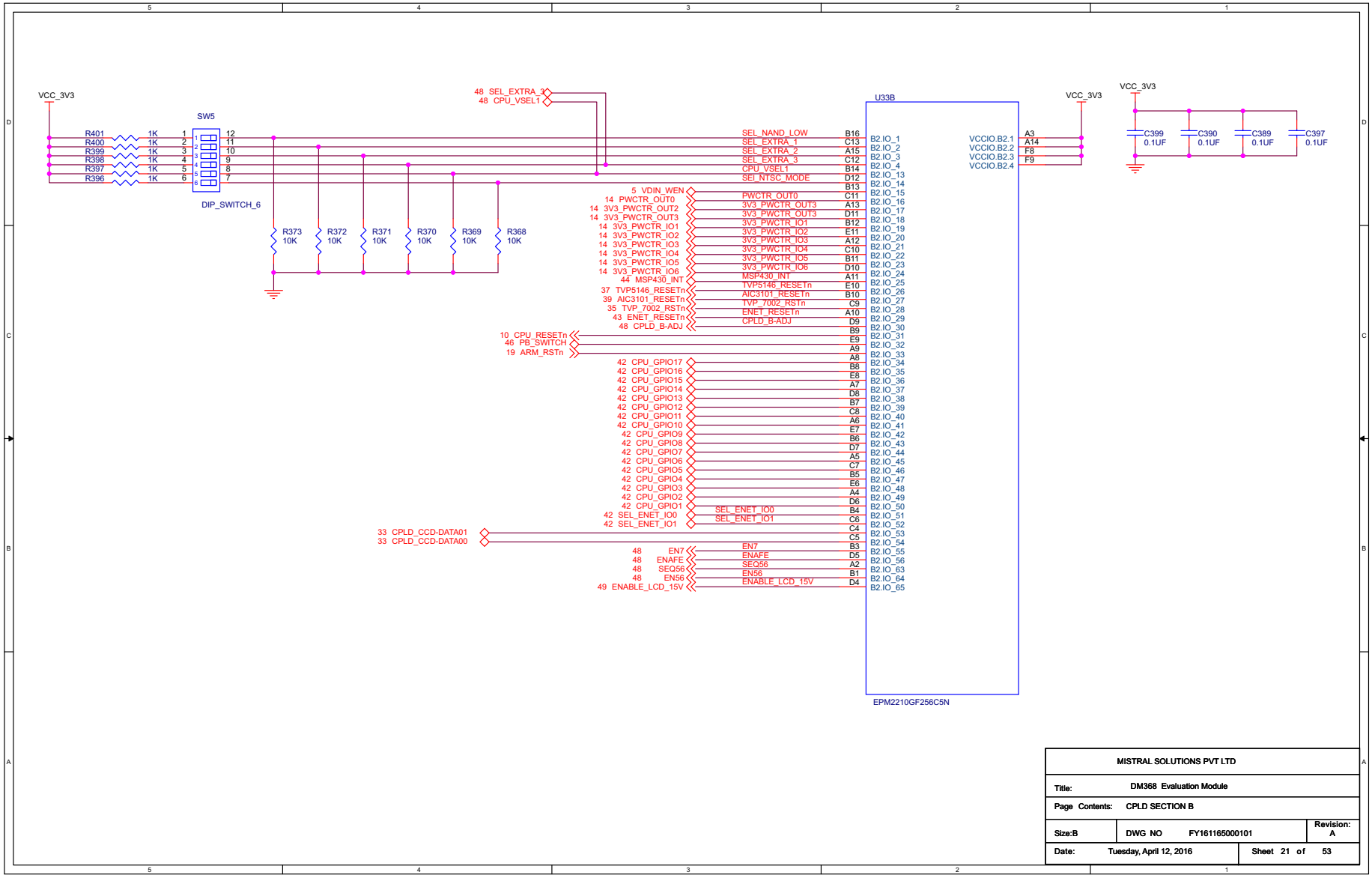
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Figure A-19. CPLD Section A



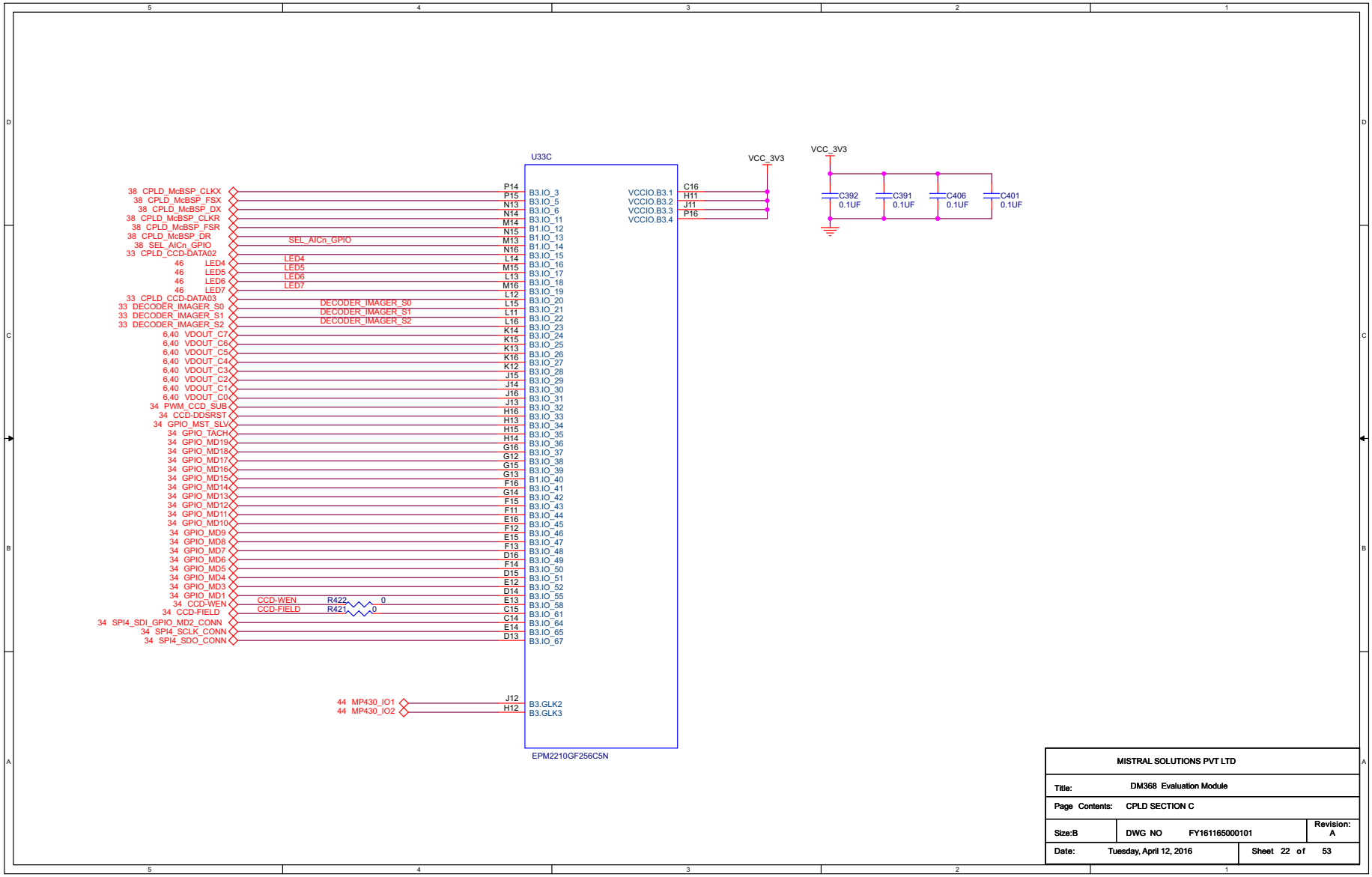
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Figure A-20. CPLD Section B



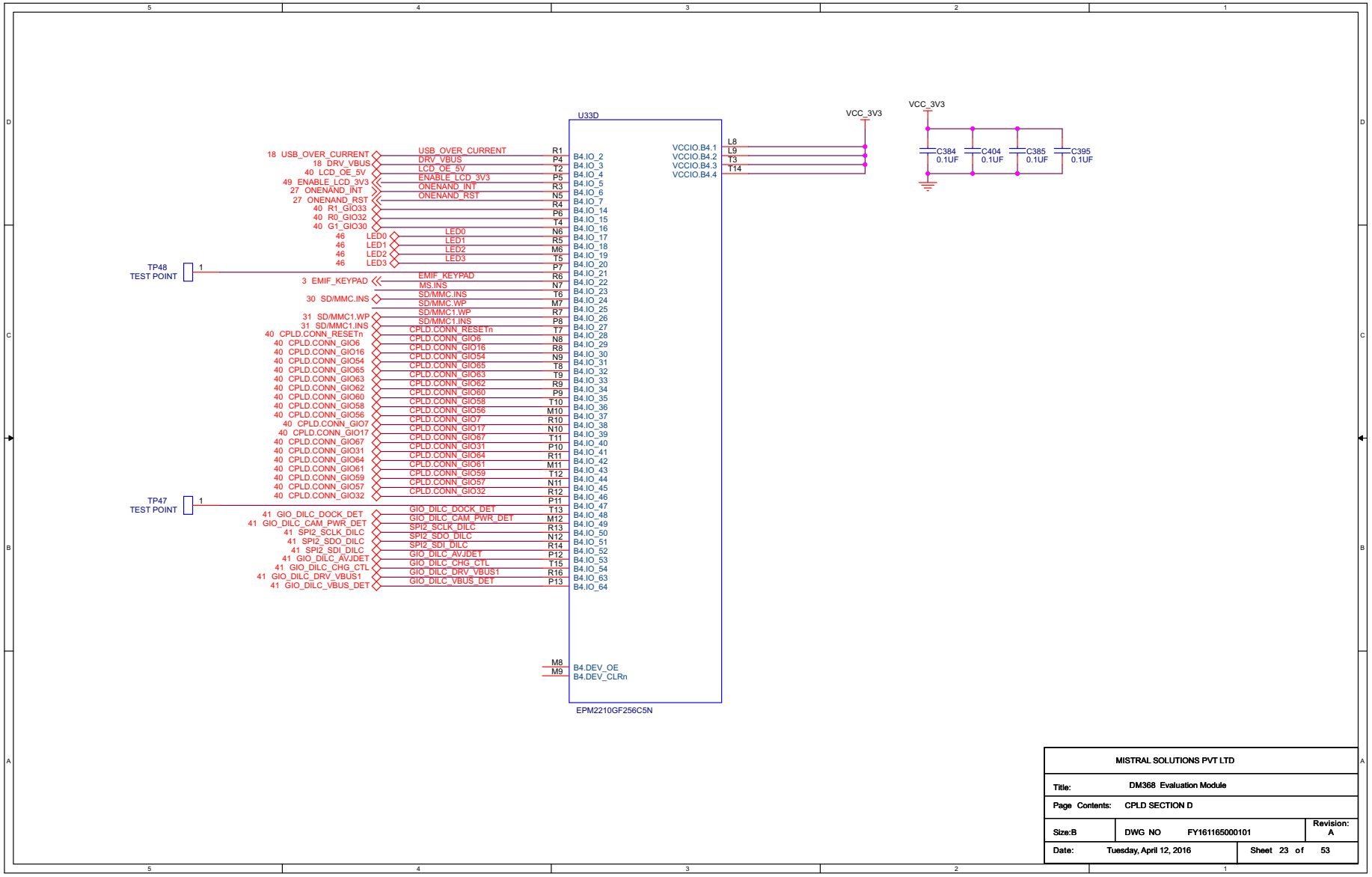
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Figure A-21. CPLD Section C



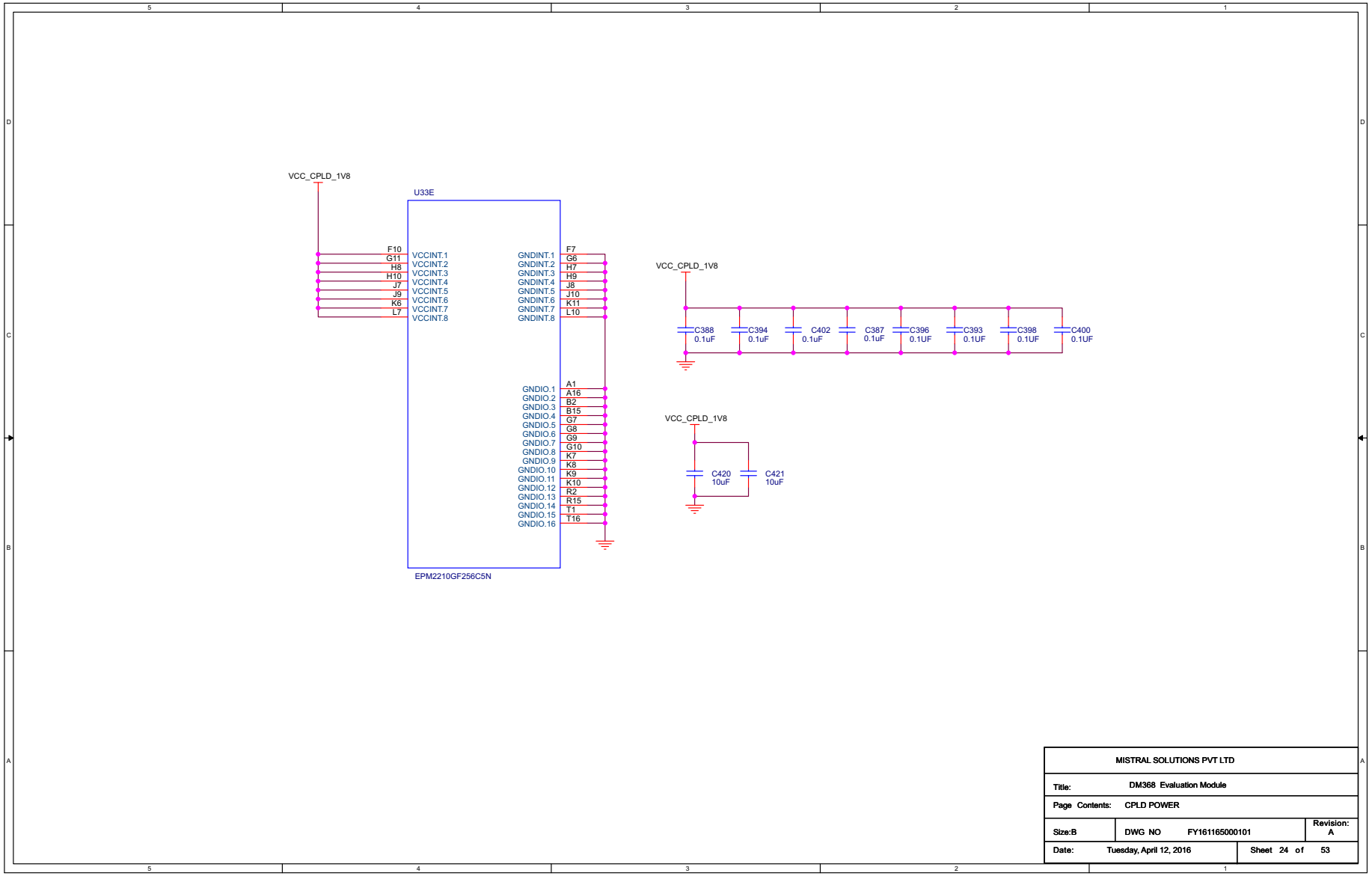
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Figure A-22. CPLD Section D



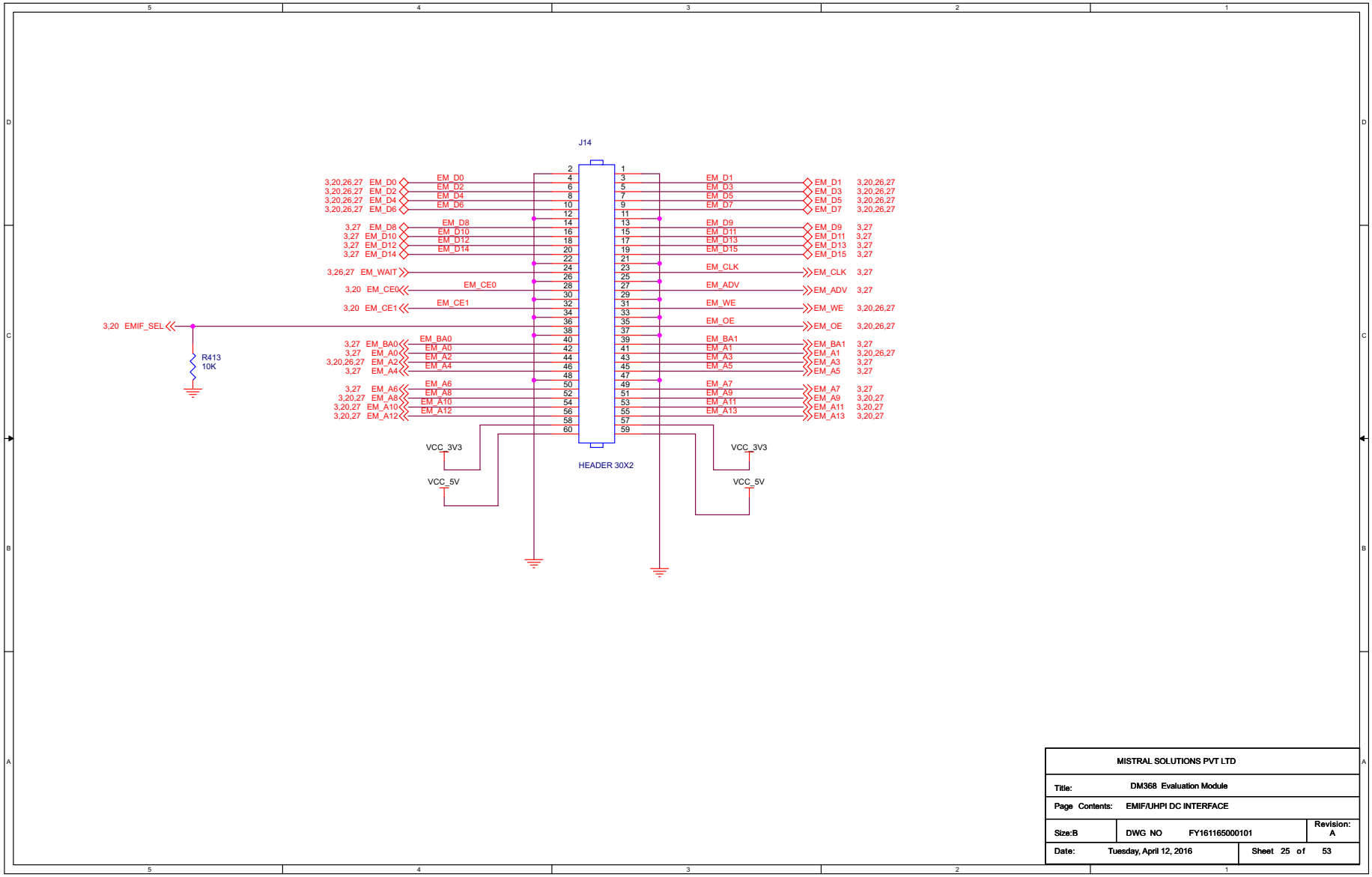
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Figure A-23. CPLD Power



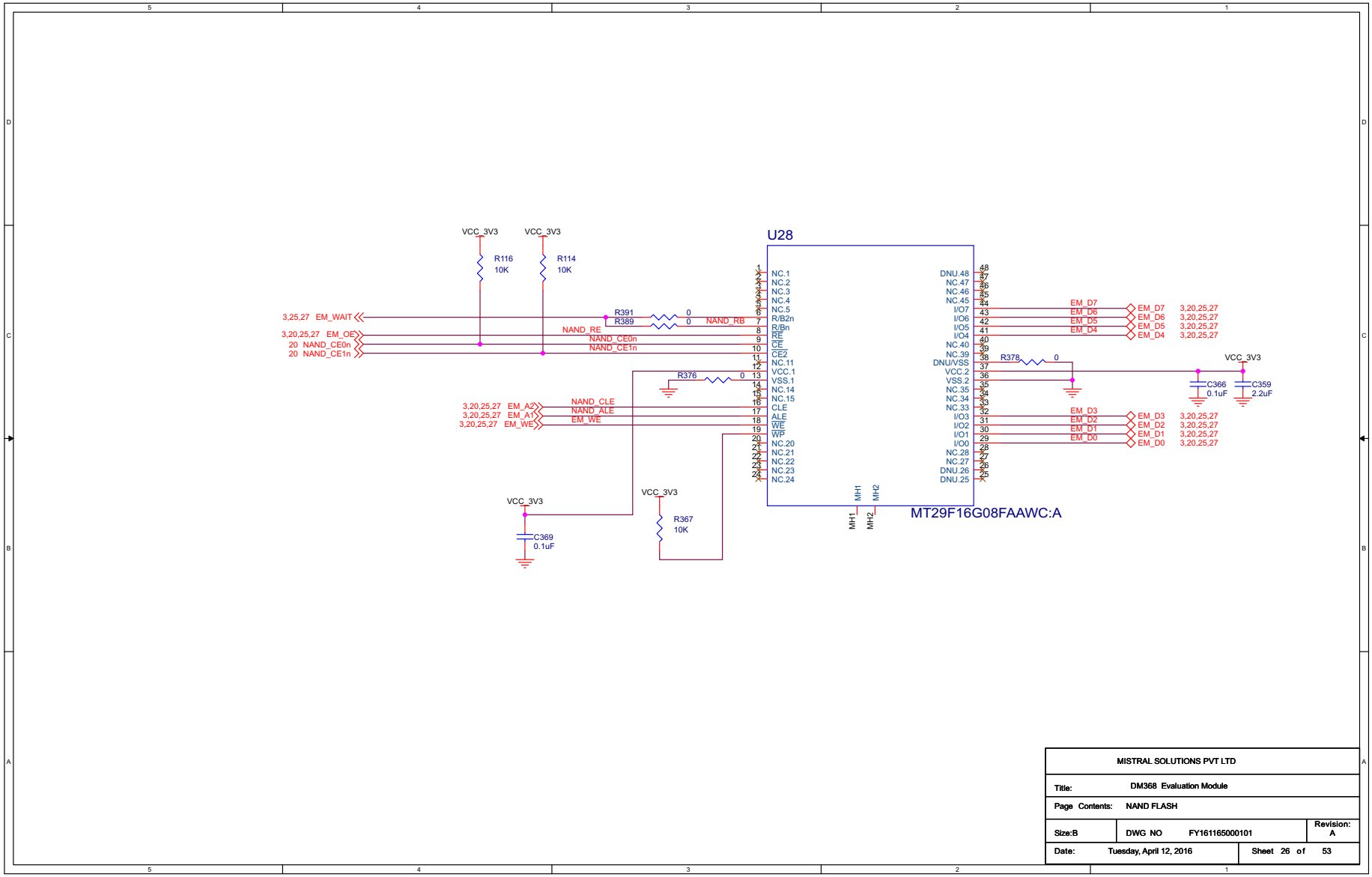
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Figure A-24. EMIF/UHPI DC Interface



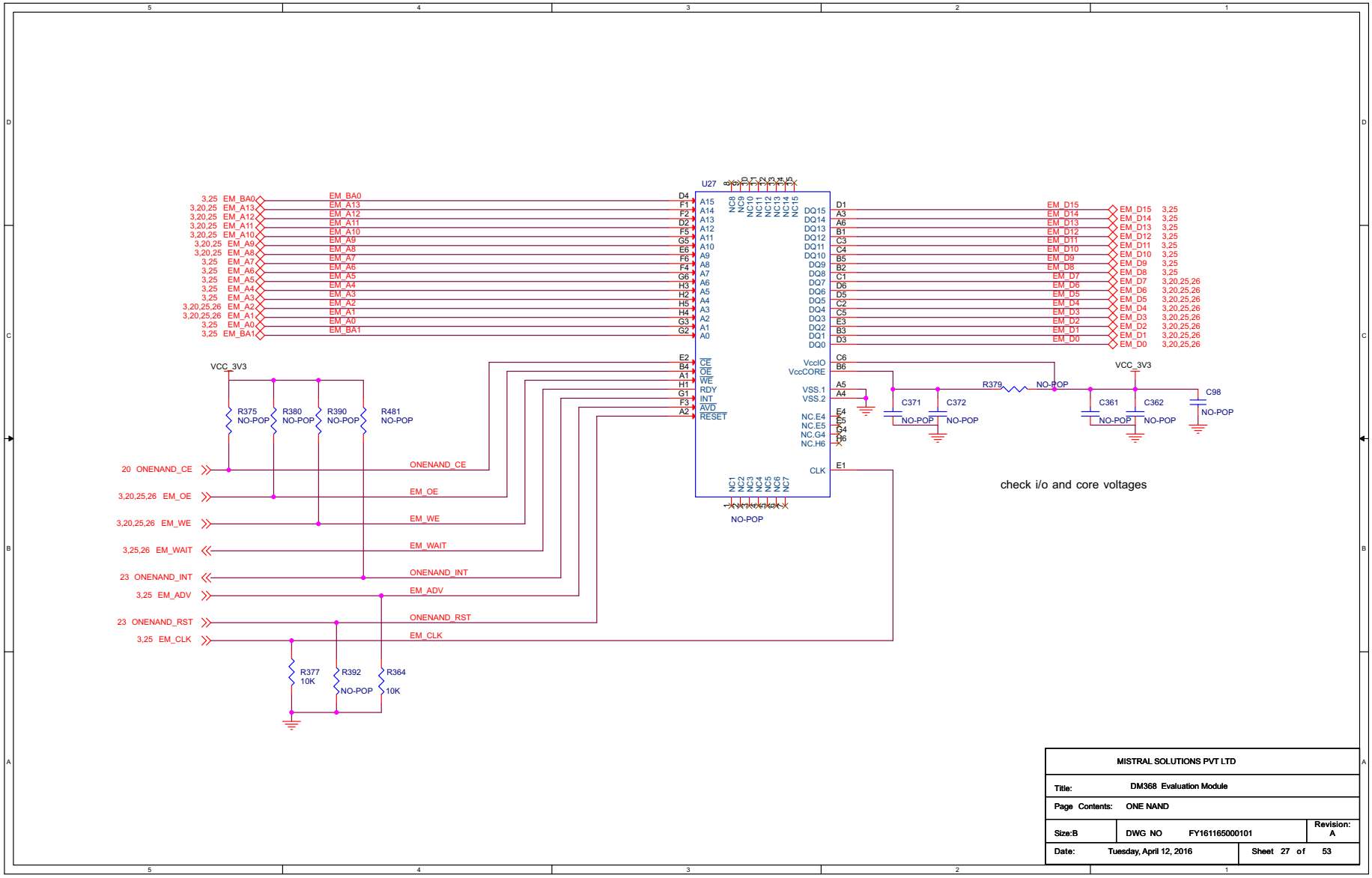
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Figure A-25. NAND Flash



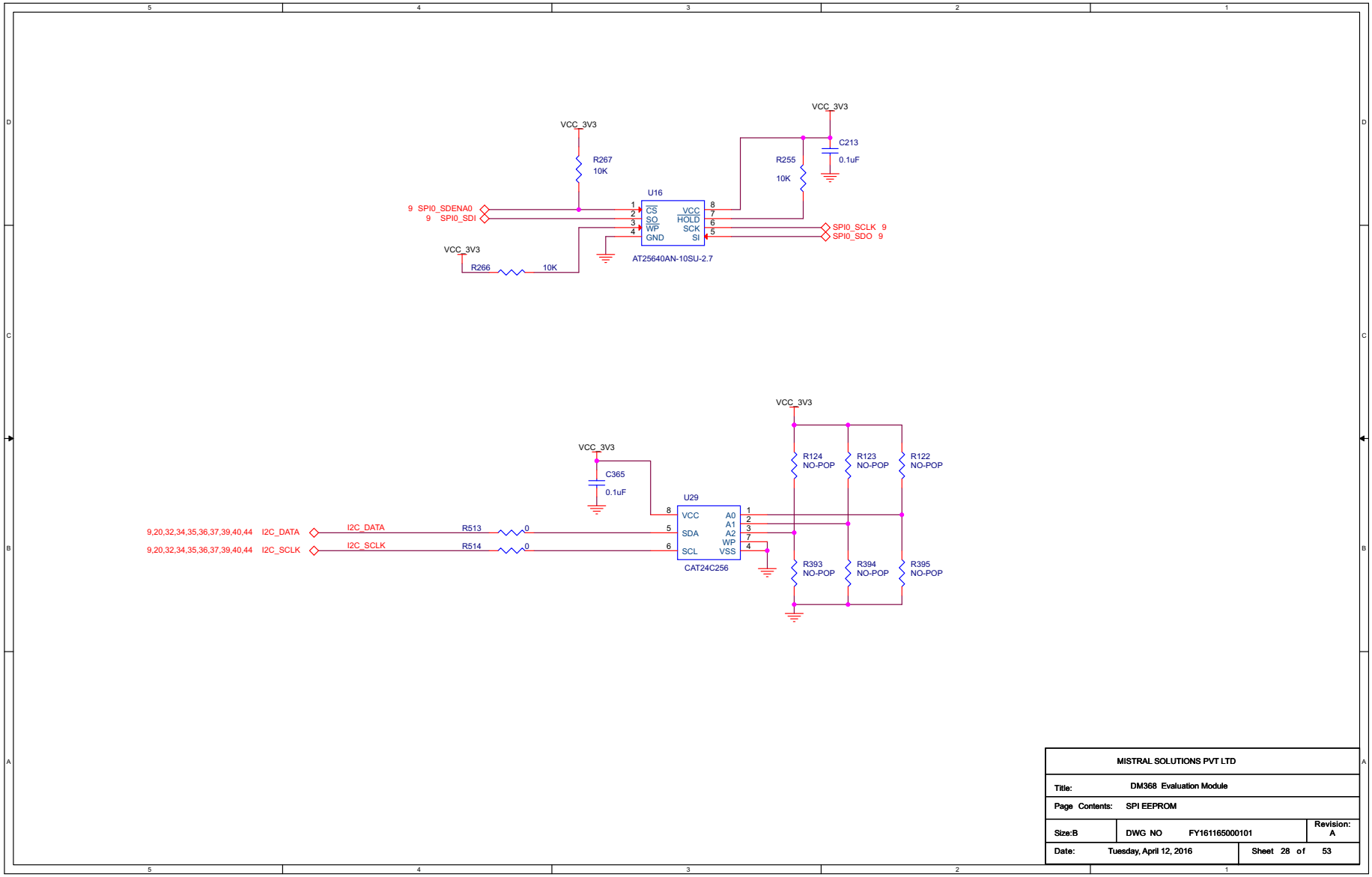
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Figure A-26. One NAND



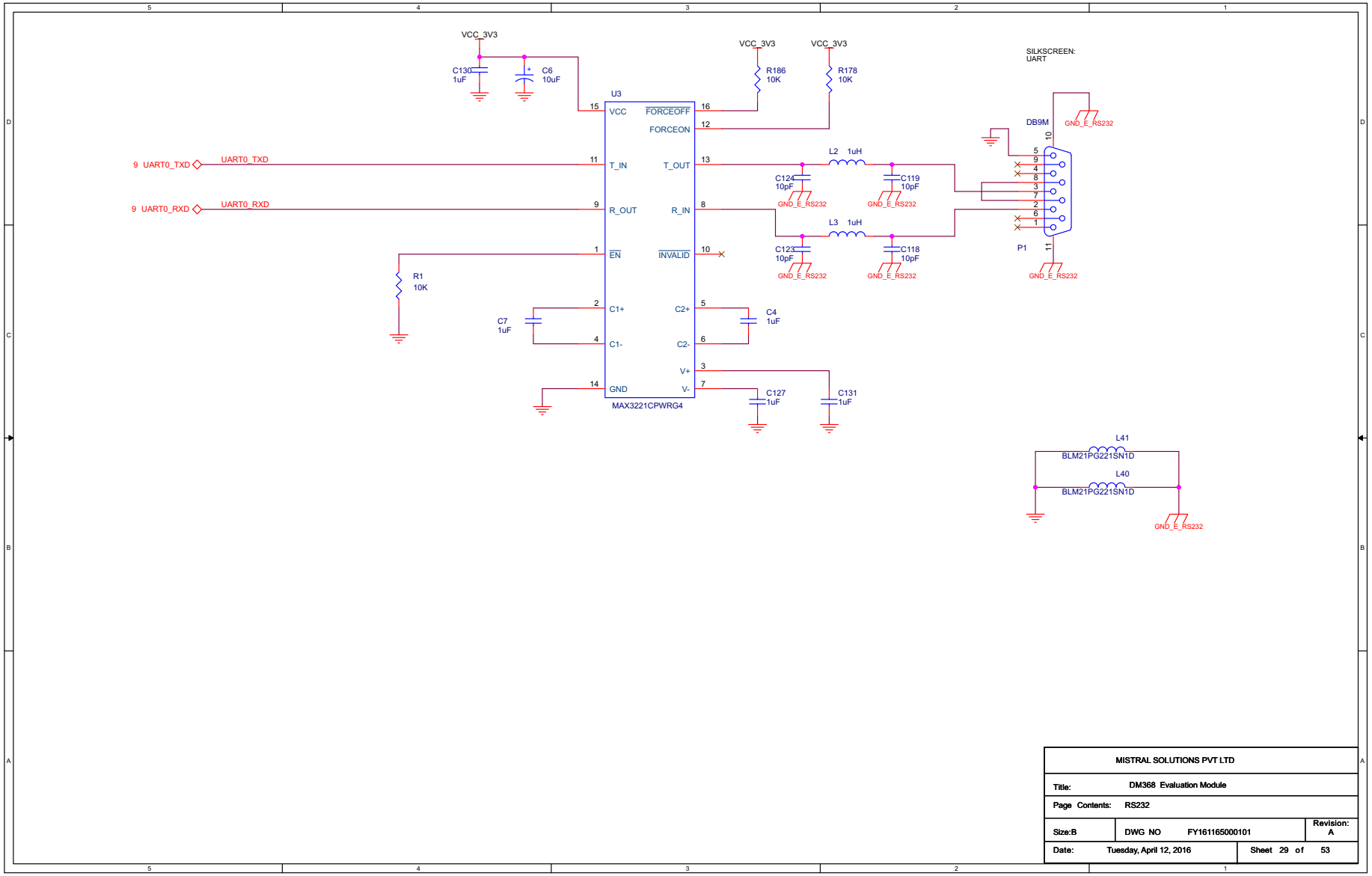
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Figure A-27. SPI EEPROM



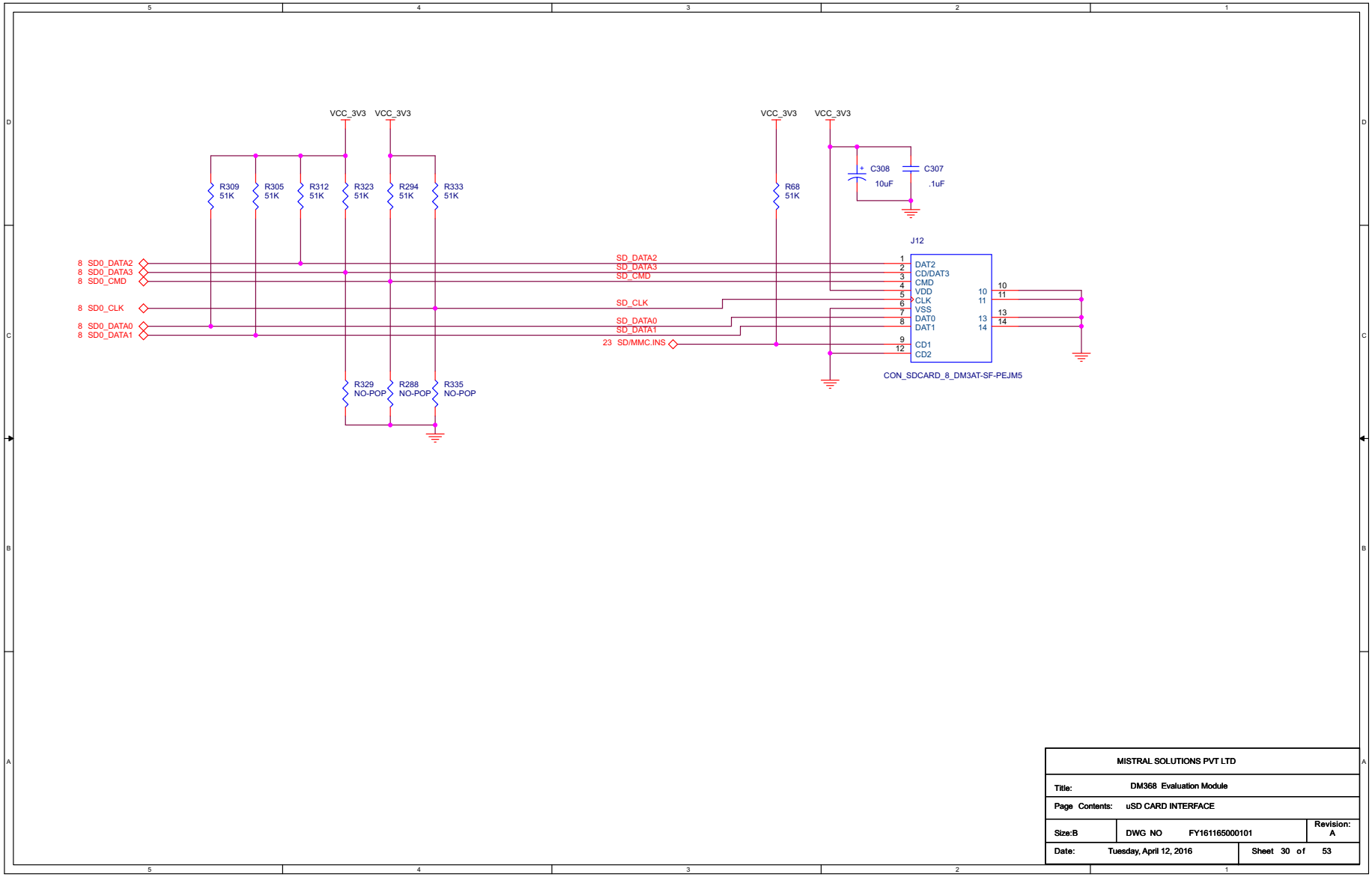
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Figure A-28. RS232



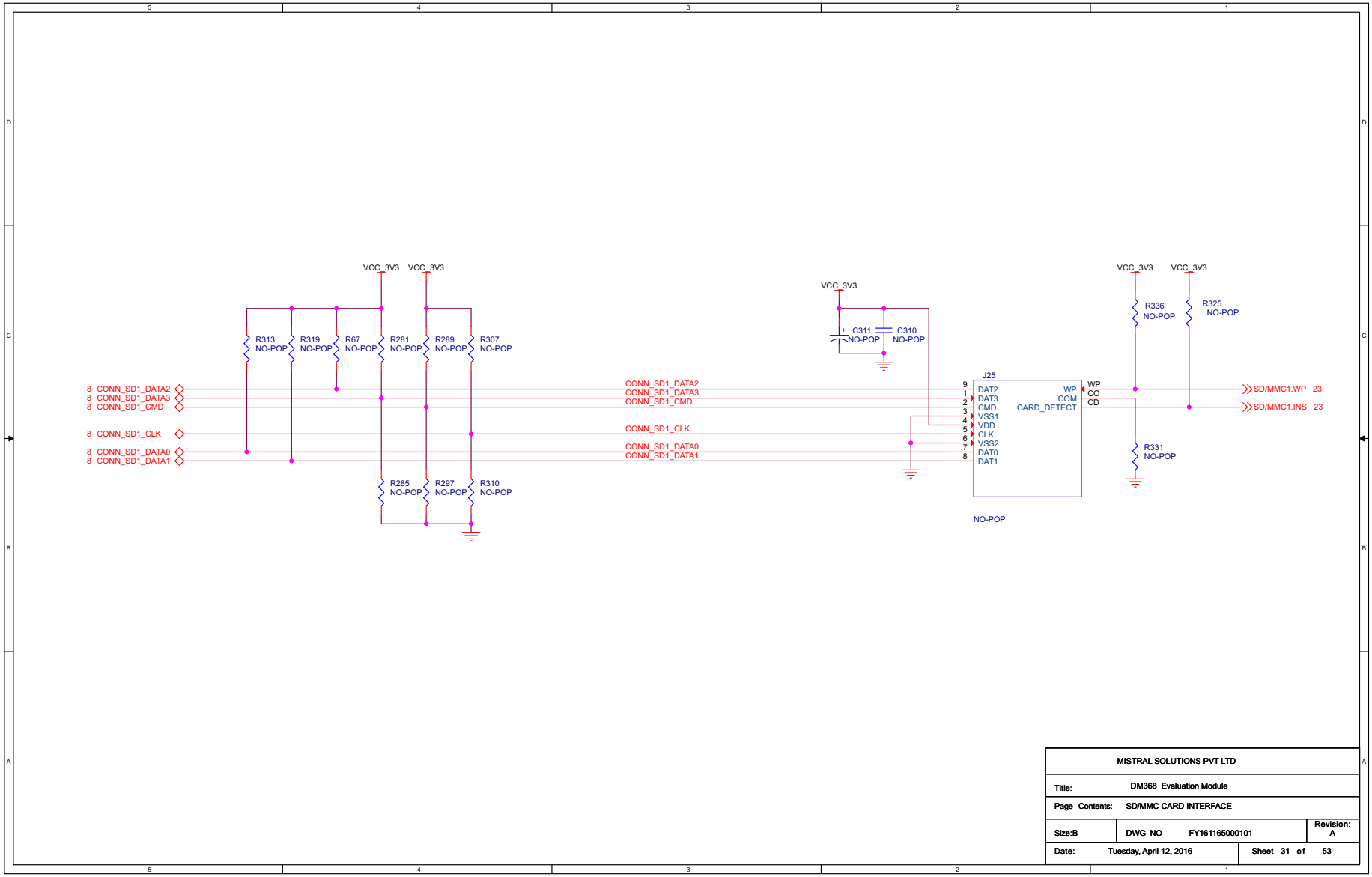
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Figure A-29. µSD Card Interface



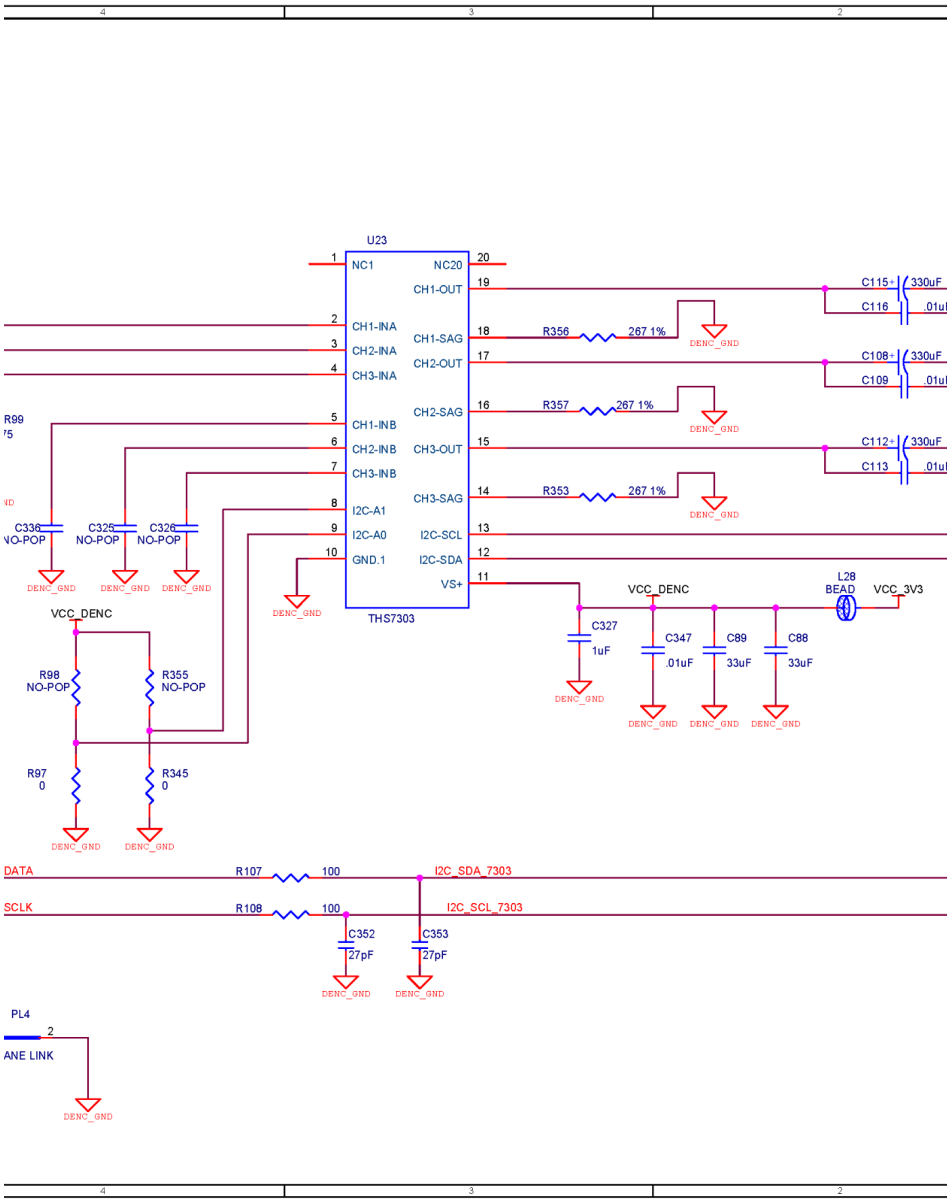
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Figure A-30. SD/MMC Card Interface



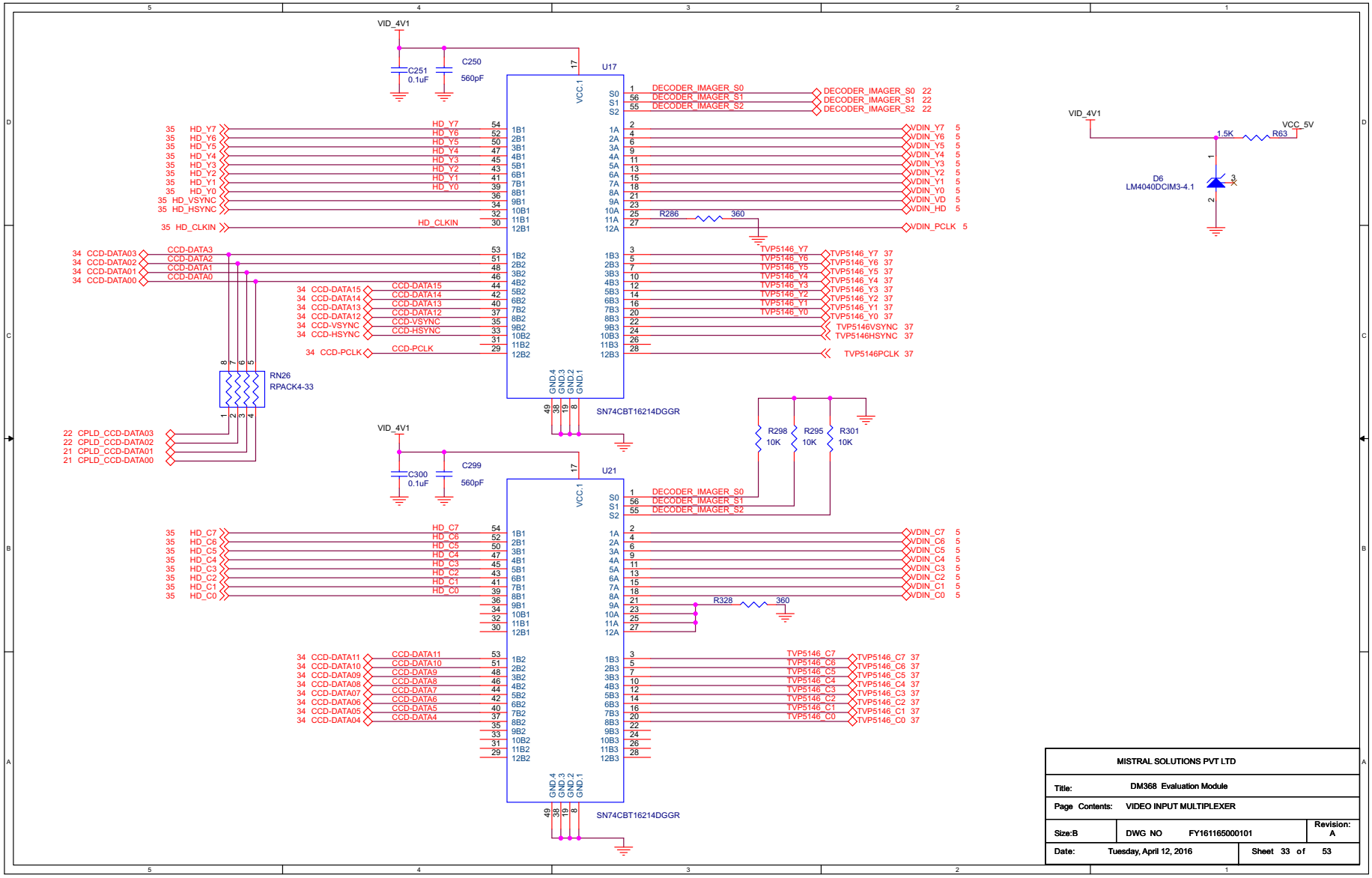
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Figure A-31. Component Video Output



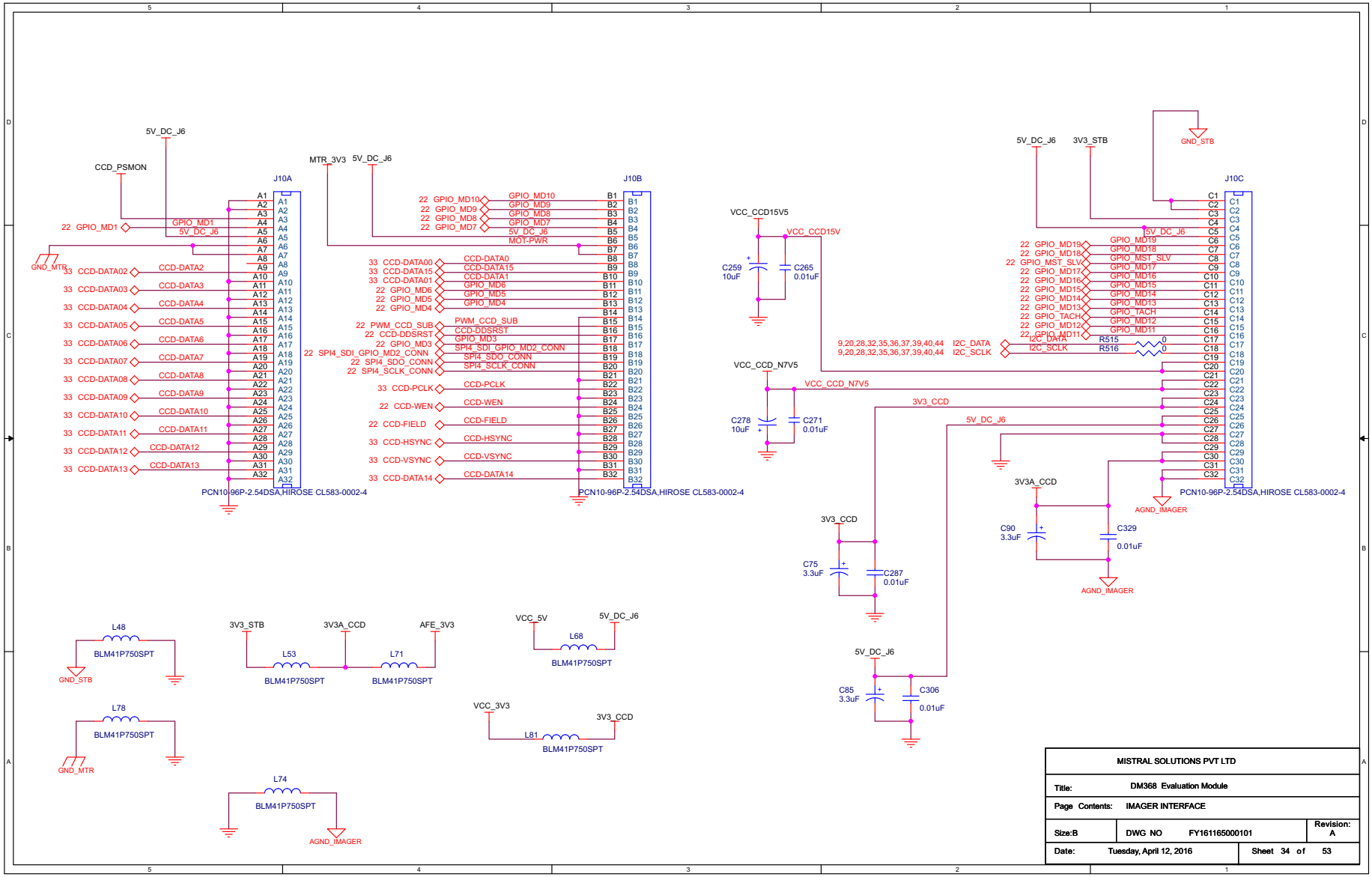
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Figure A-32. Video Input Multiplexer



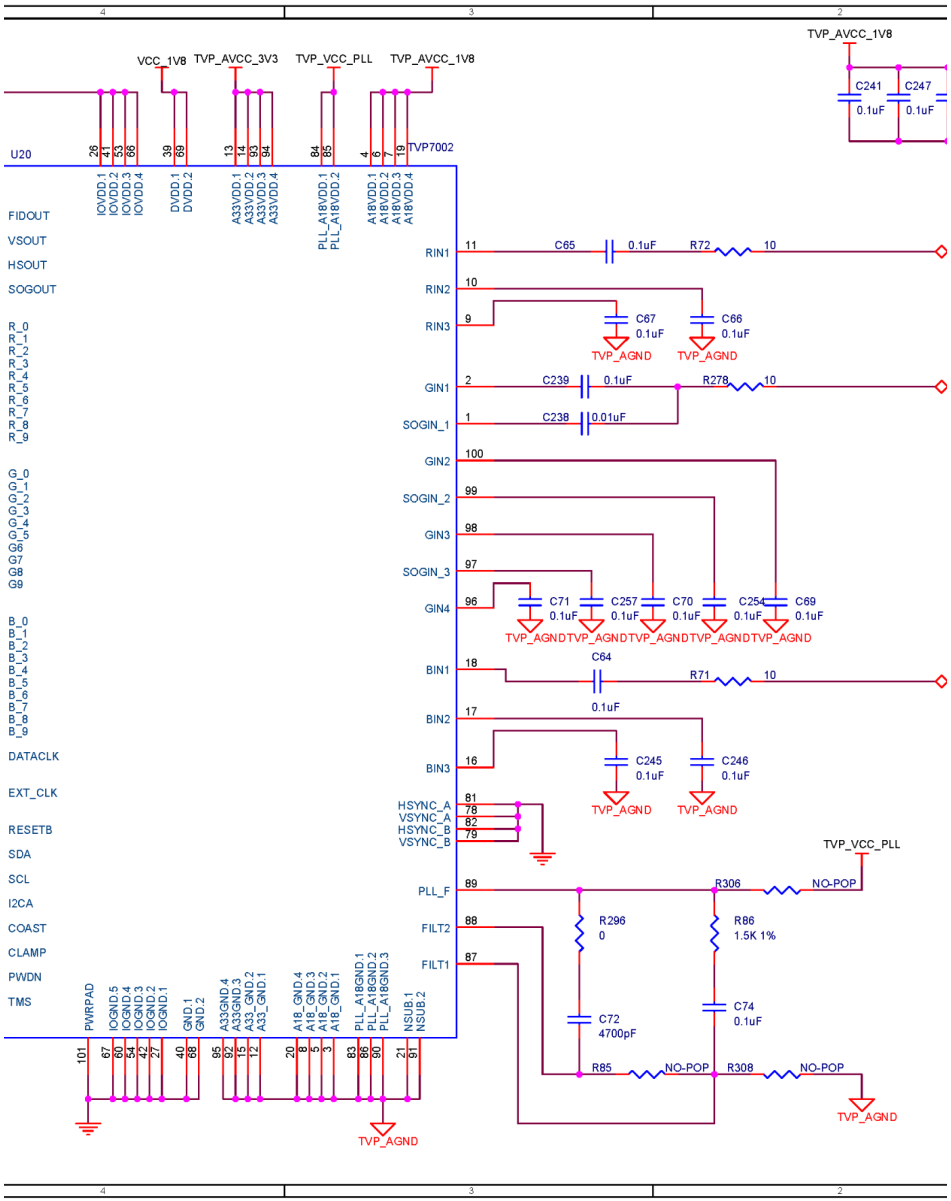
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Figure A-33. Imager Interface



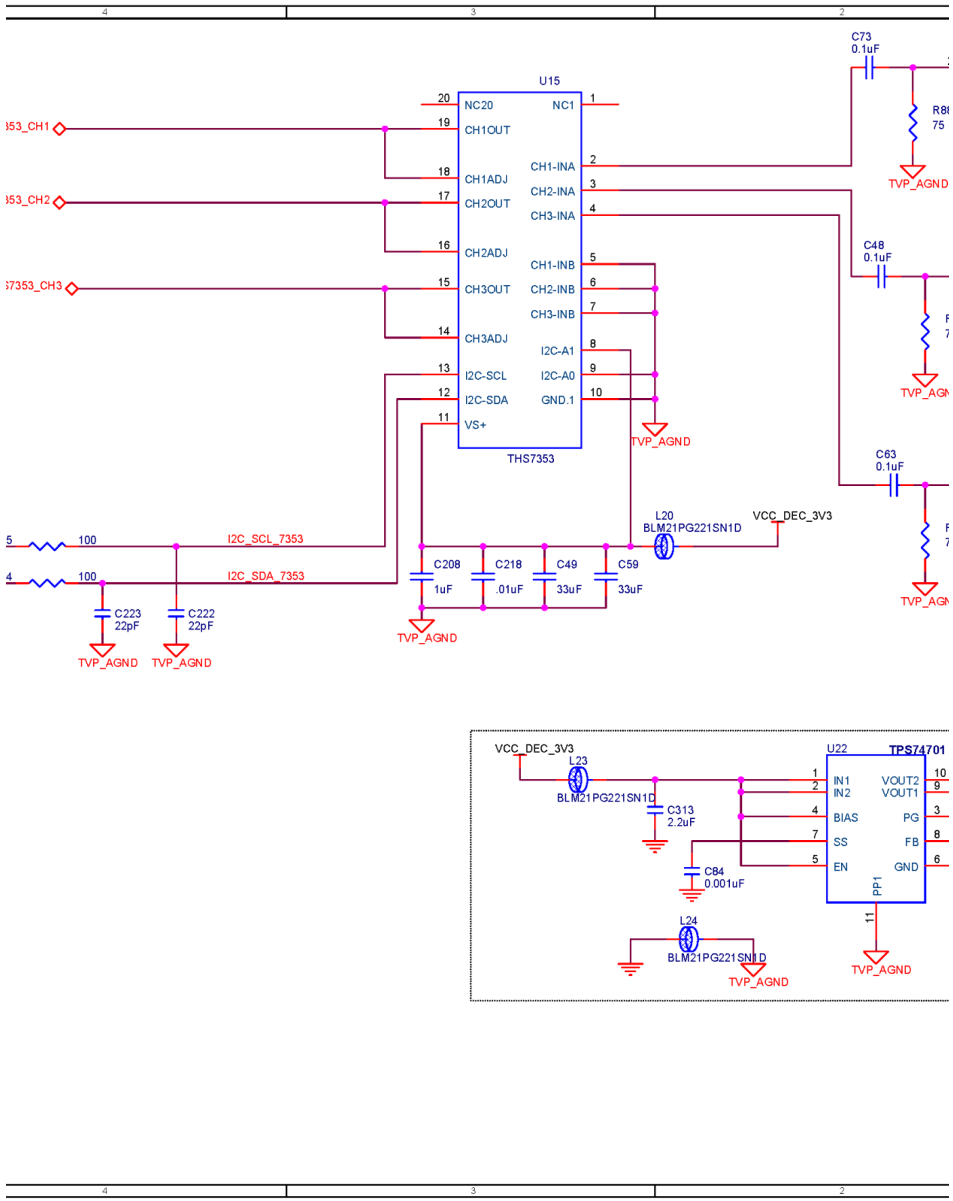
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Figure A-34. TVP7002 HD Video In (1 of 2)



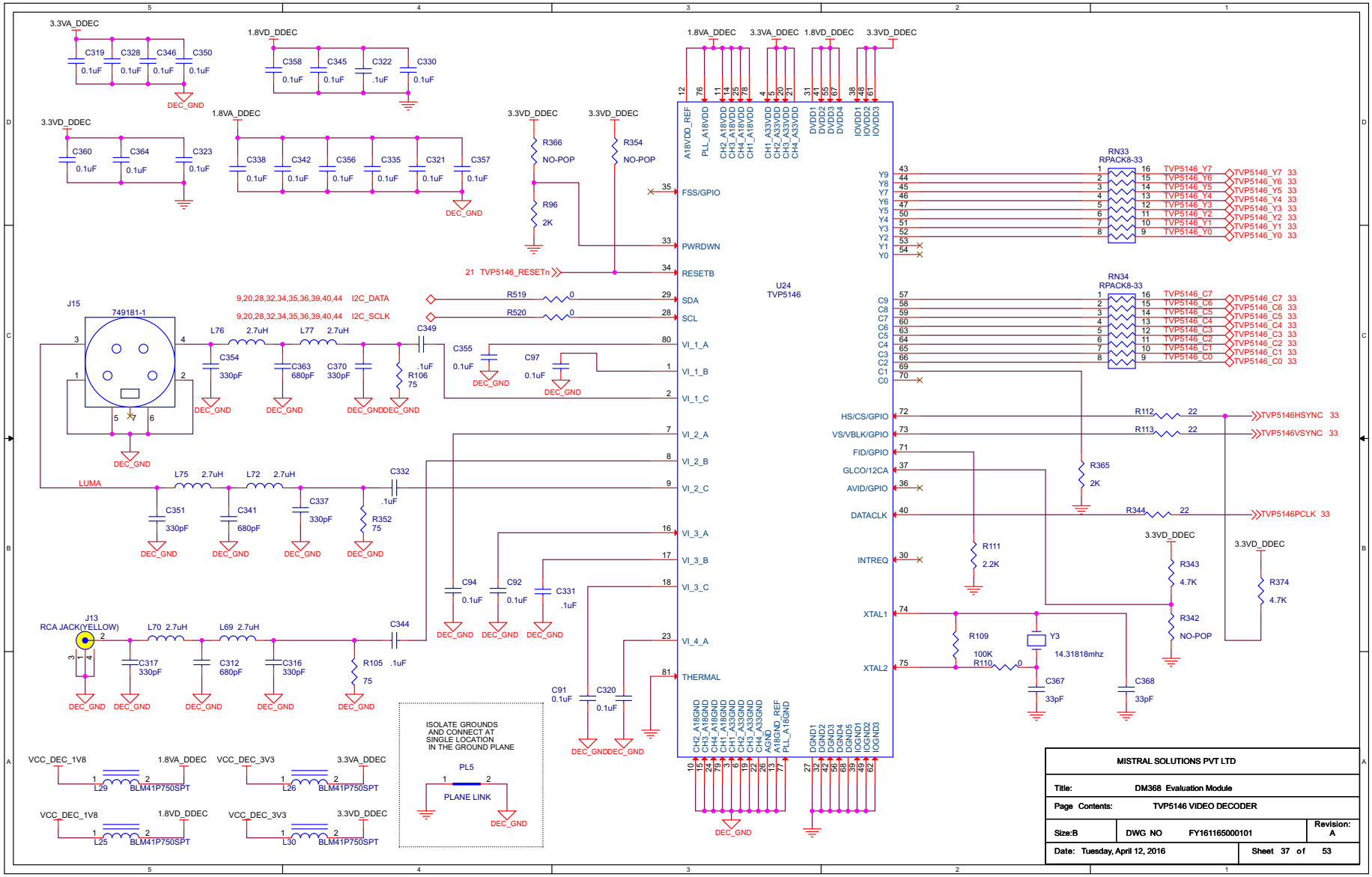
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Figure A-35. TVP7002 HD Video In (2 of 2)



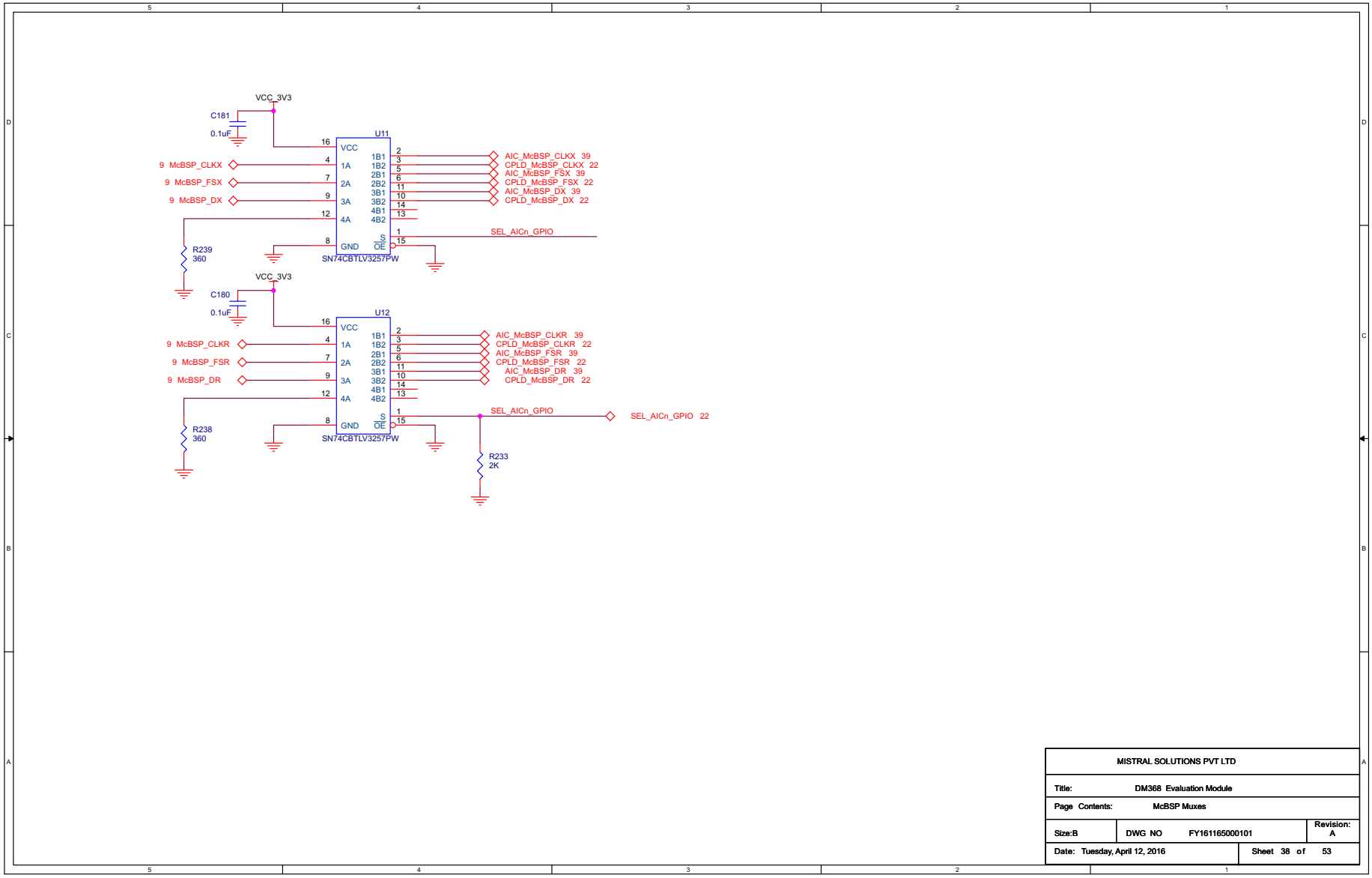
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Figure A-36. TVP5146 Video Decoder



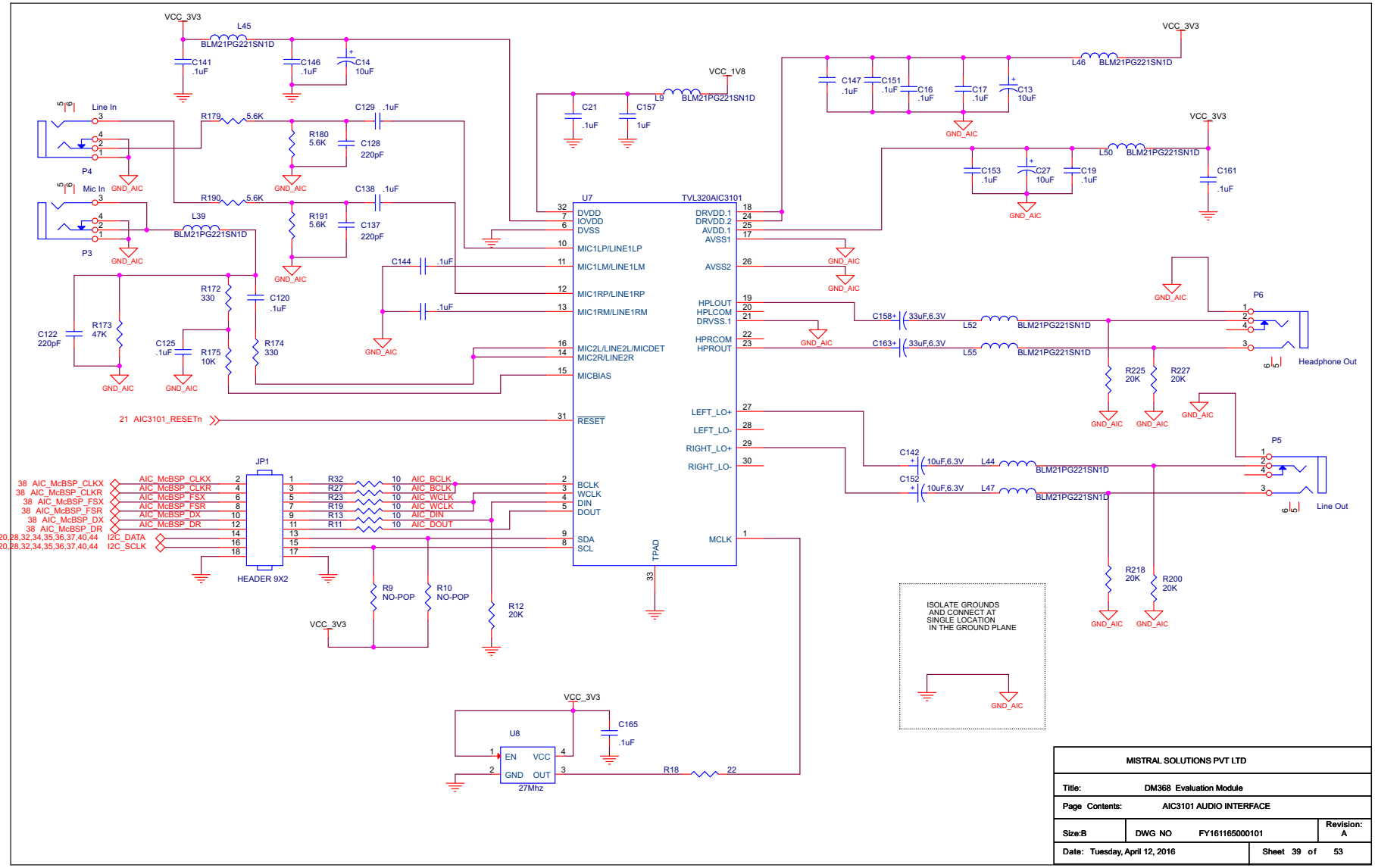
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Figure A-37. McBSP Muxes



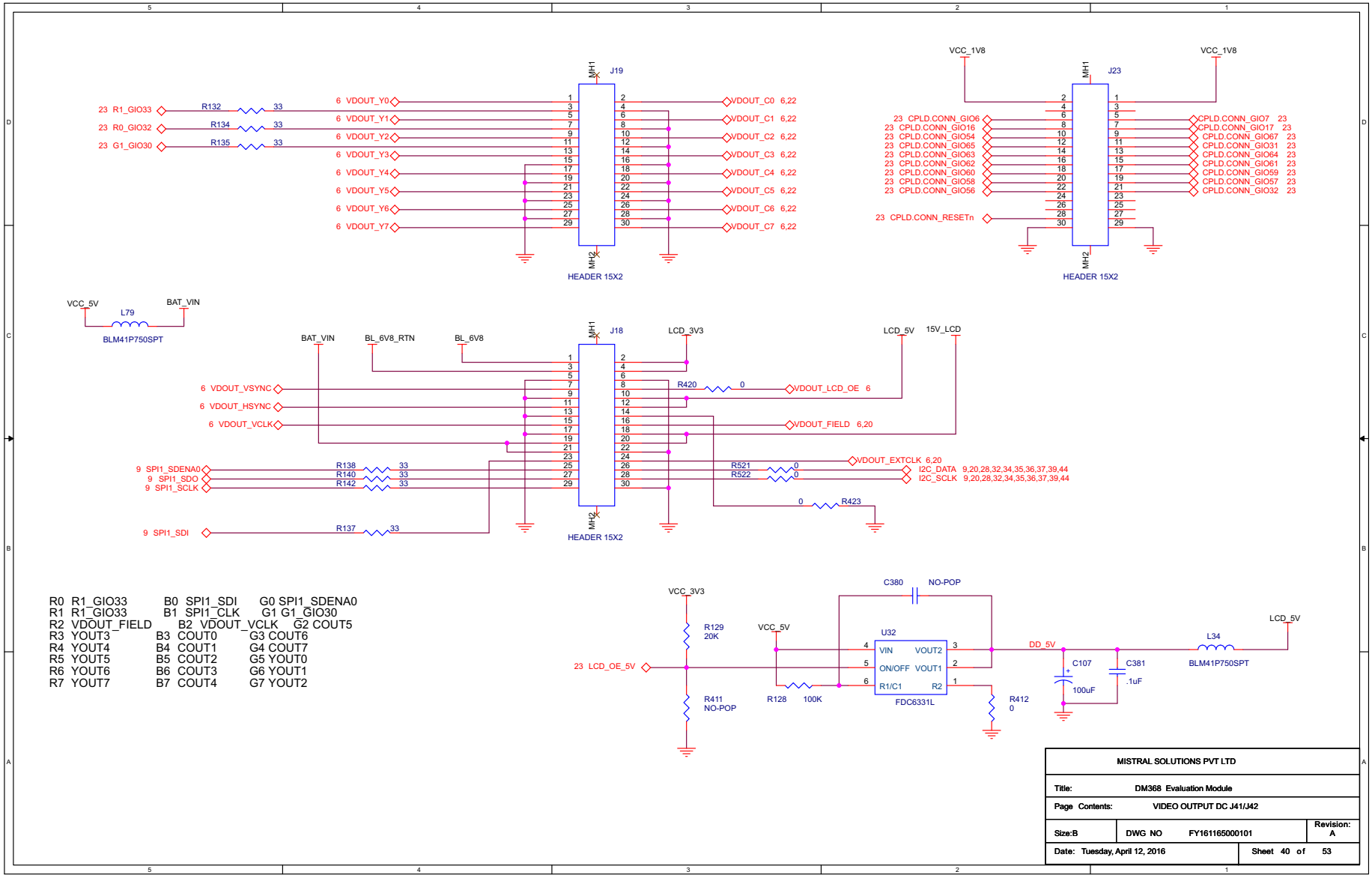
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Figure A-38. AIC3101 Audio Interface



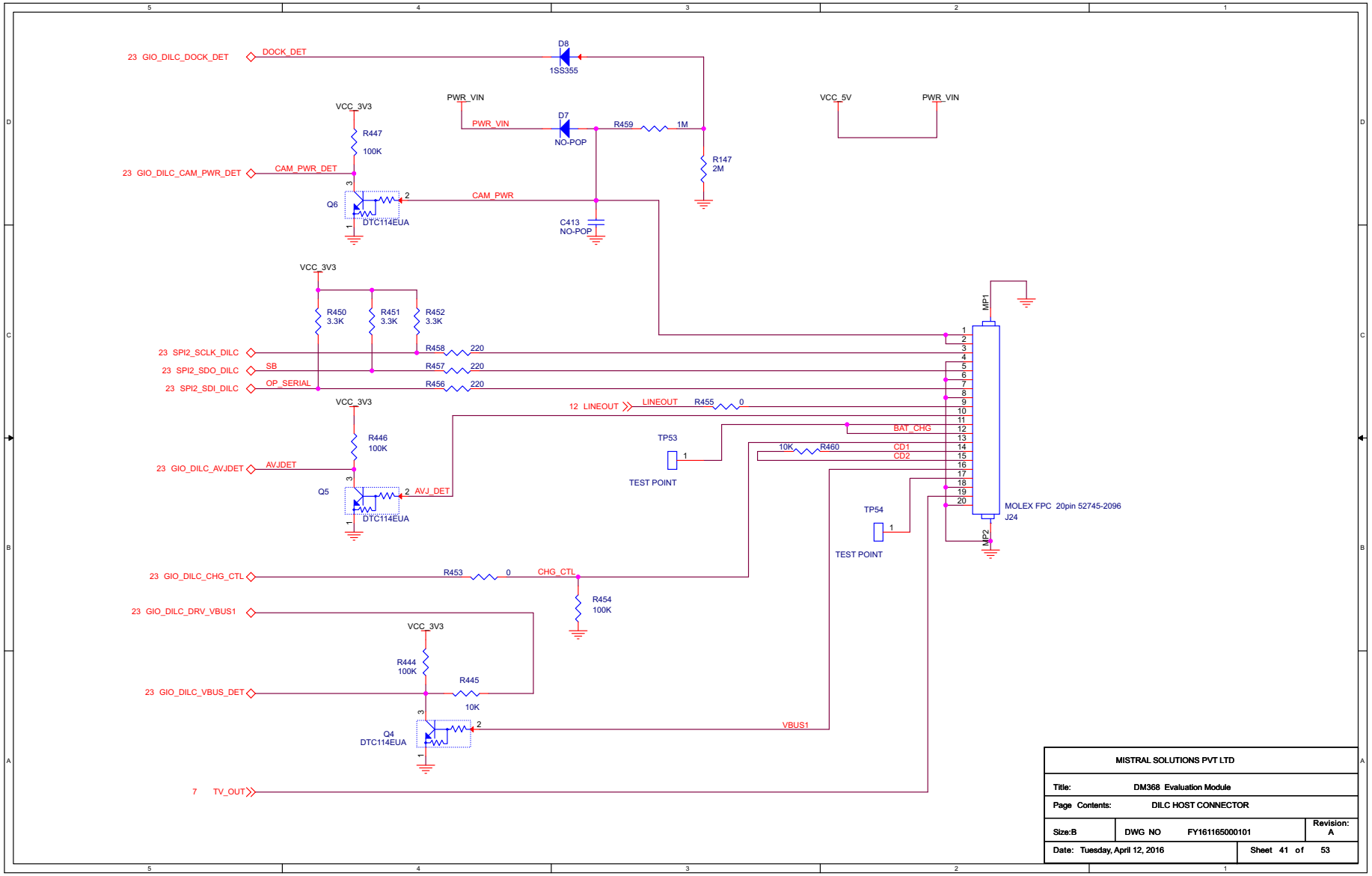
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Figure A-39. Video Output DC J41/J42



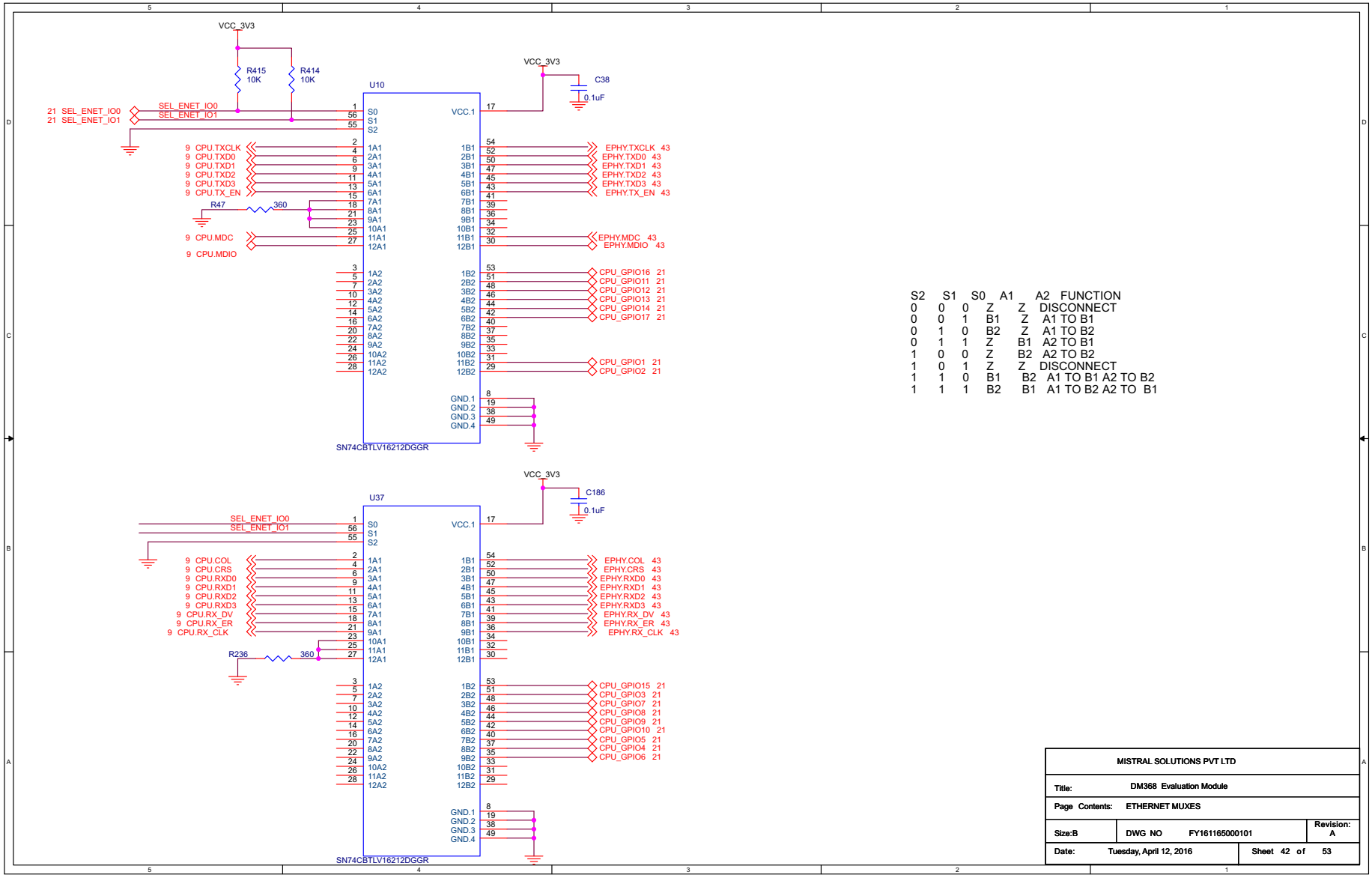
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Figure A-40. DILC Host Connector



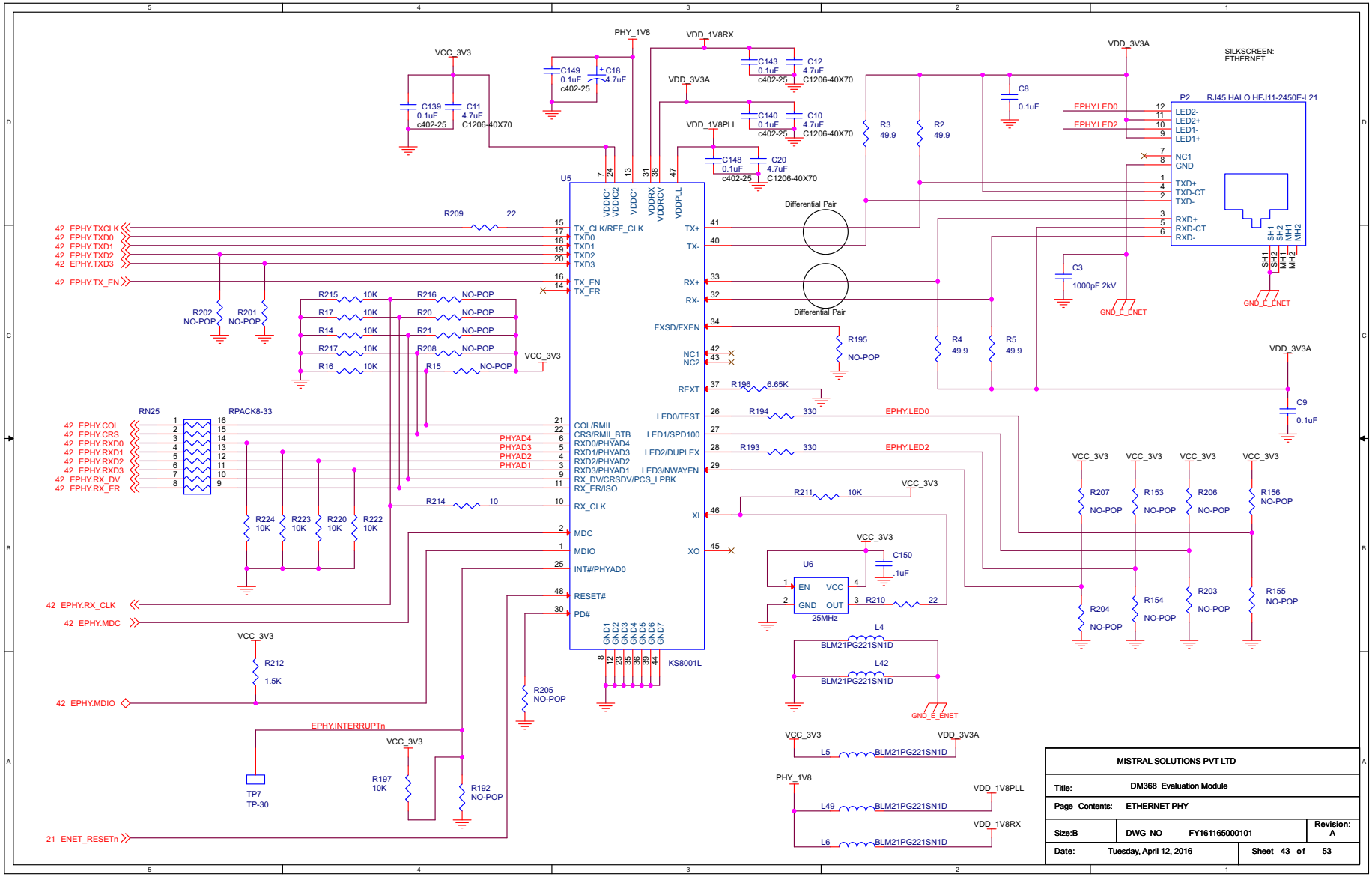
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Figure A-41. Ethernet Muxes



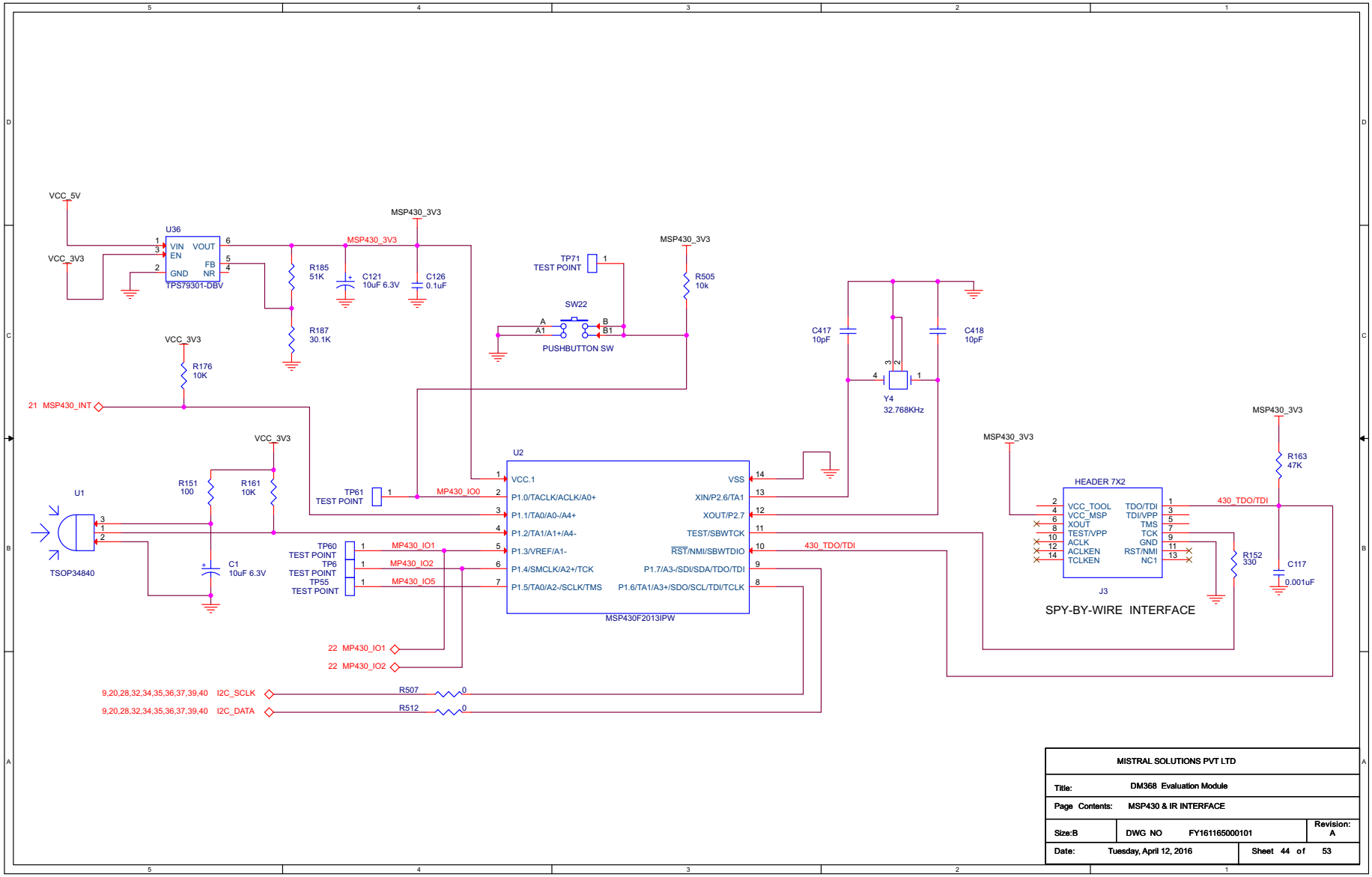
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Figure A-42. Ethernet PHY



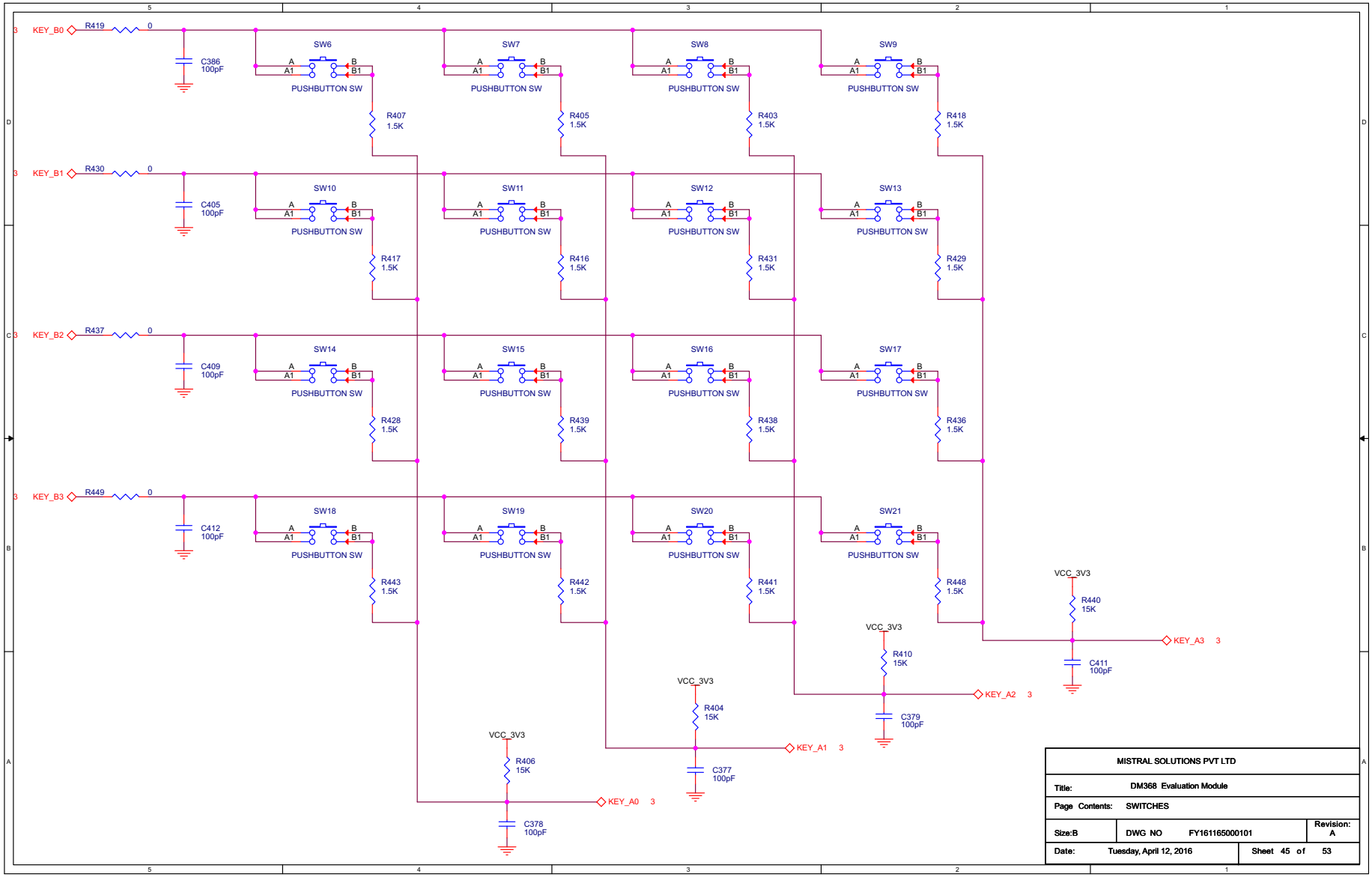
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Figure A-43. MSP430 and IR Interface



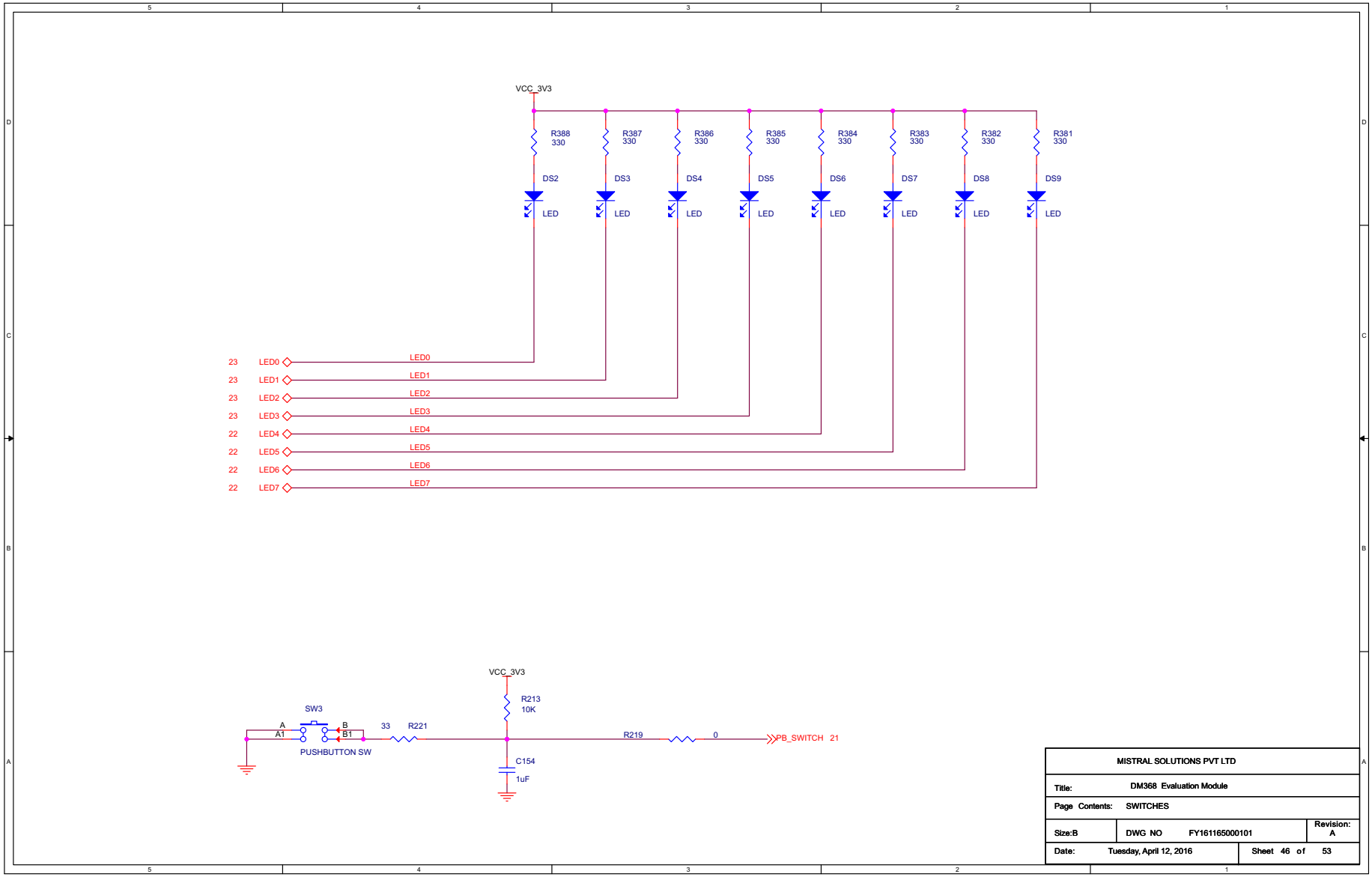
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Figure A-44. Switches (1 of 2)



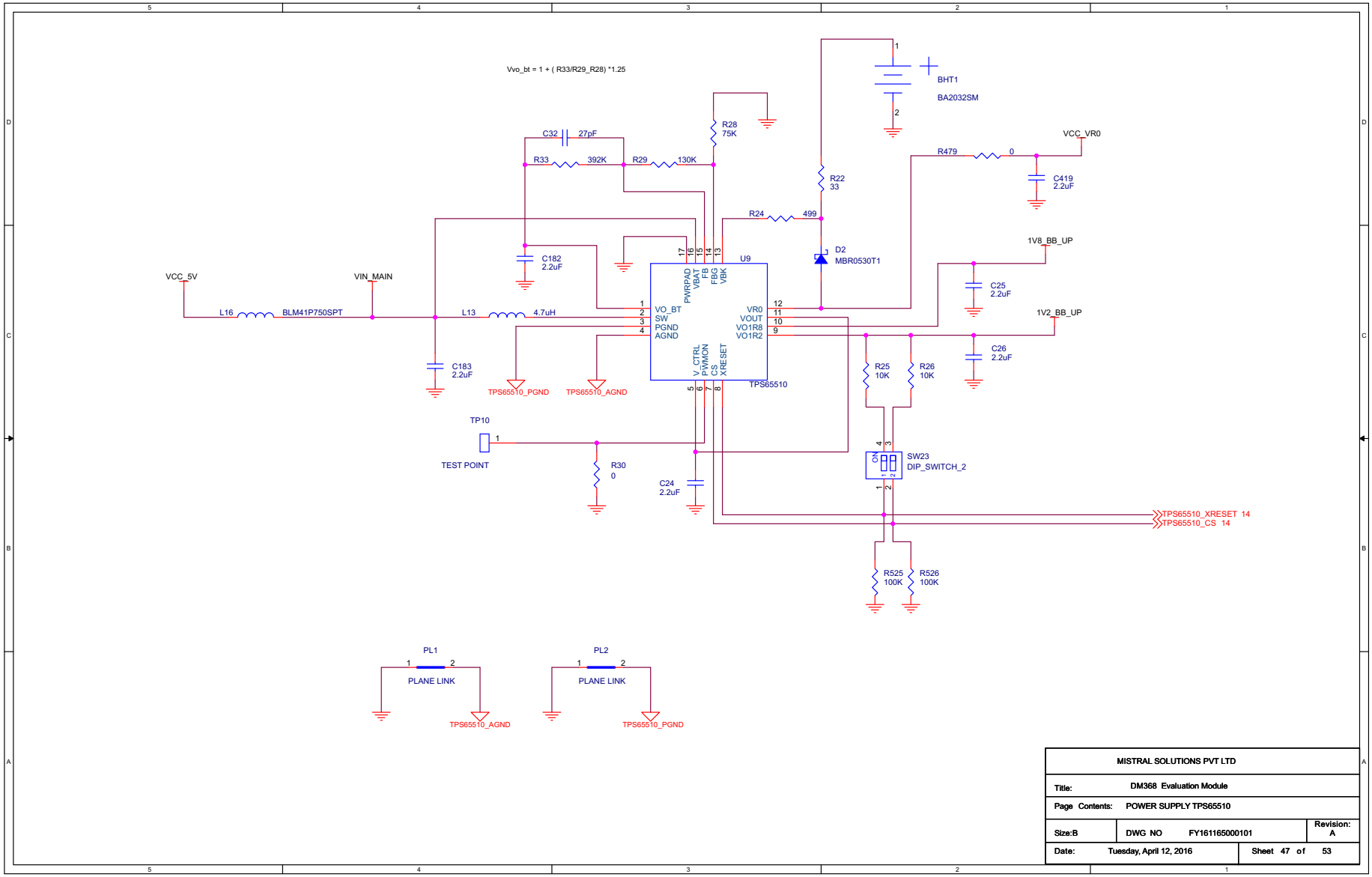
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Figure A-45. Switches (2 of 2)



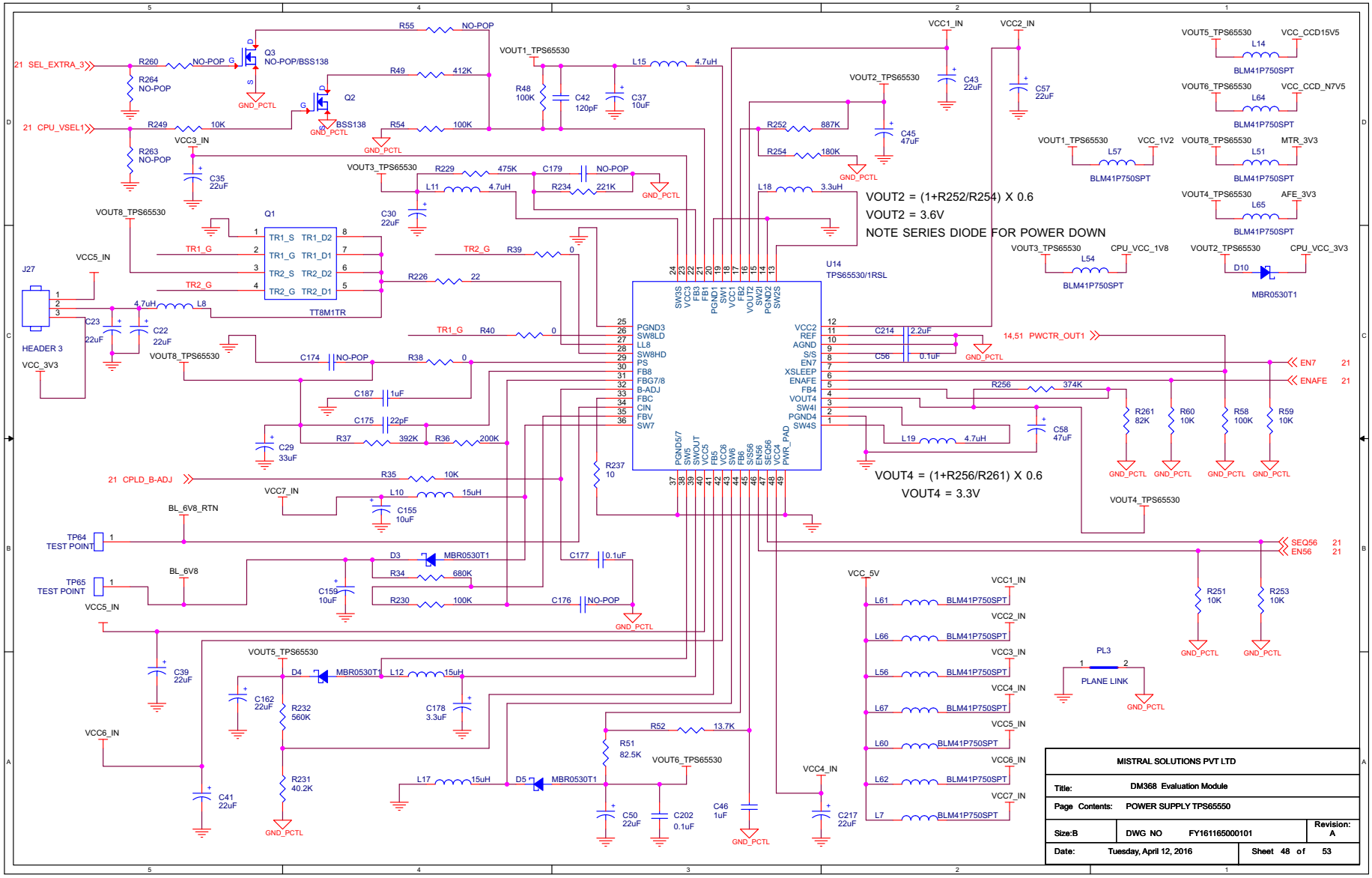
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Figure A-46. Power Supply TPS65510



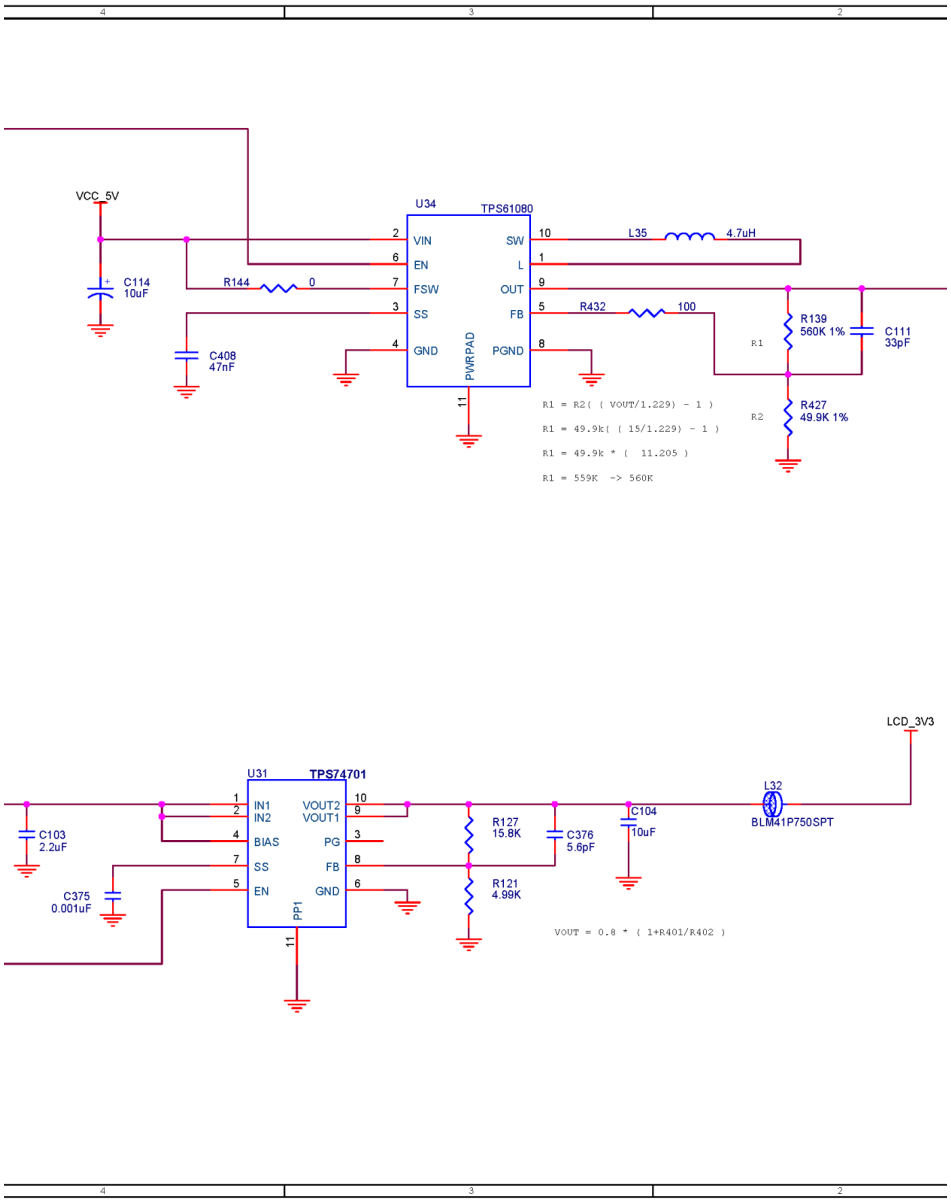
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Figure A-47. Power Supply TPS65550



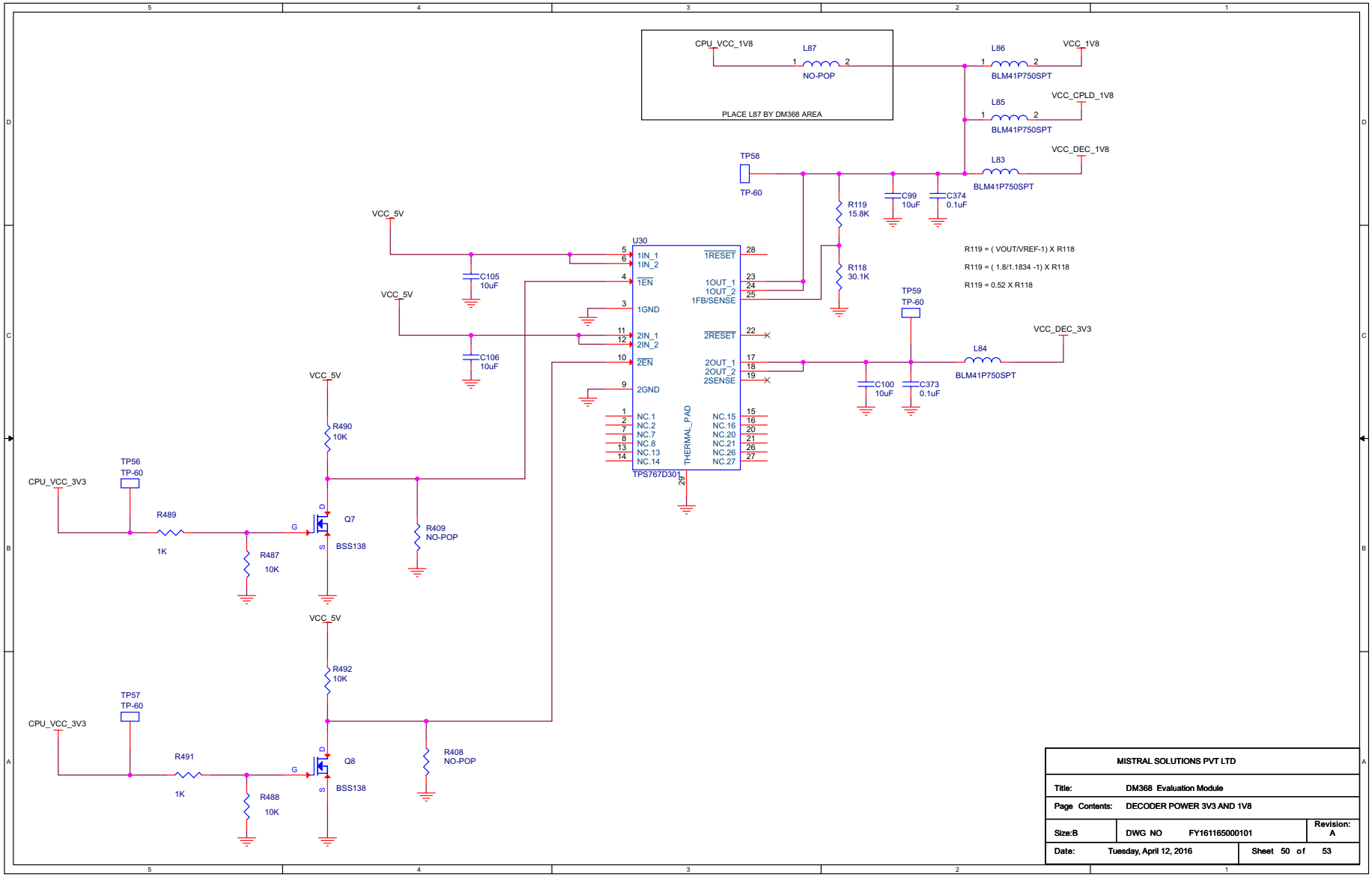
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Figure A-48. Power Supply



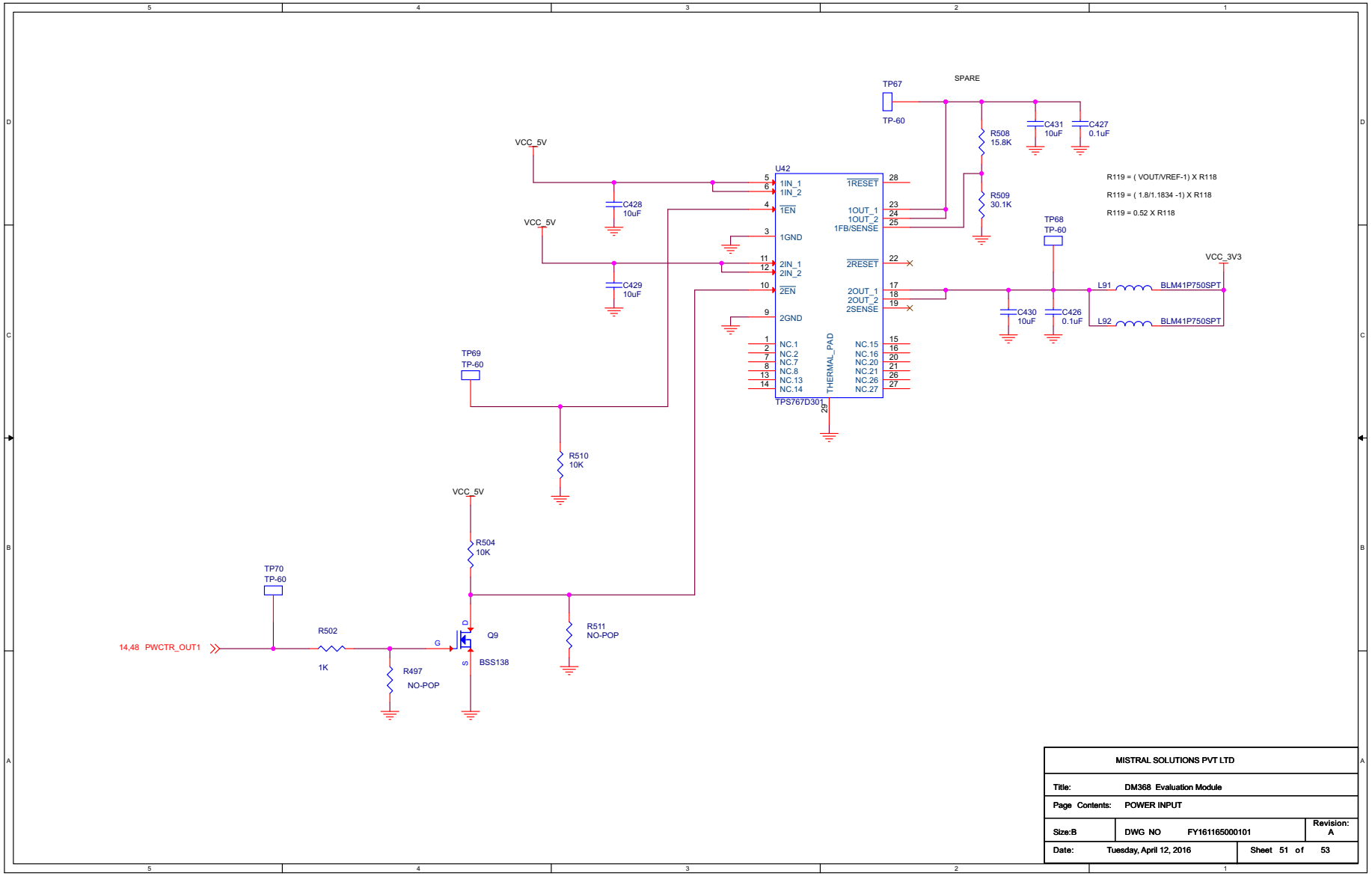
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Figure A-49. Decoder Power 3V3 and 1V8



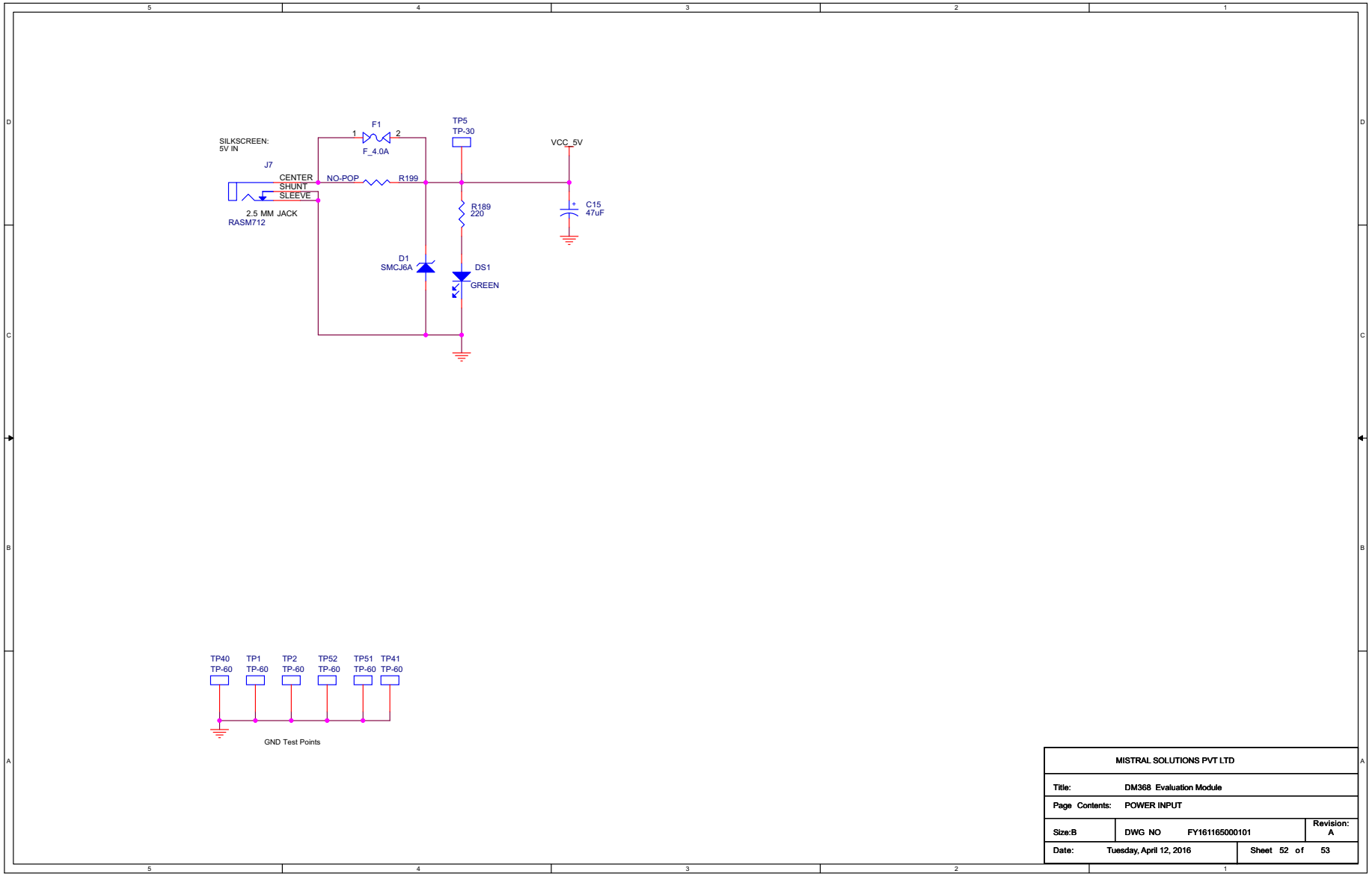
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Figure A-50. Power Input (1 of 2)



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Figure A-51. Power Input (2 of 2)

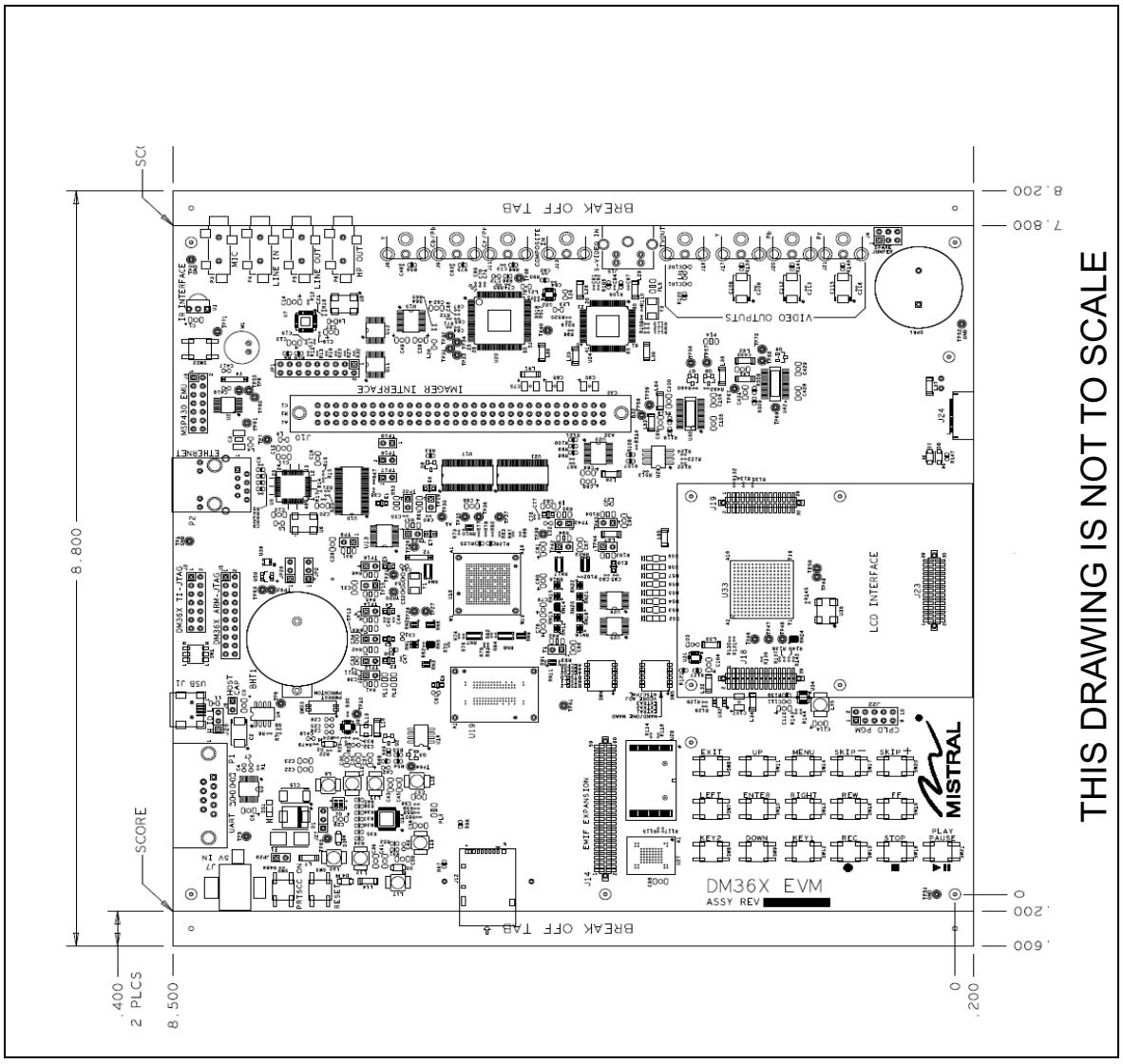


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Mechanical Information

This appendix contains the mechanical information about the DM368 EVM.

Figure B-1. Mechanical Schematic



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