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TMS320LF2407
Evaluation Module

Technical Reference

2001 **DSP Development Systems**

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TMS320LF2407
Evaluation Module
Technical Reference

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SPECTRUM DIGITAL, INC.
12502 Exchange Dr., # 440 Stafford, TX. 77477
Tel: 281.494.4505 Fax: 281.494.5310
sales@spectrumdigital.com www.spectrumdigital.com

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About This Manual

This document describes the board level operations of the TMS320LF2407 evaluation module (EVM). The EVM is based on the Texas Instruments TMS320LF2407 Digital Signal Processor.

The TMS320LF2407 EVM is a table top card to allow engineers and software developers to evaluate certain characteristics of the TMS320LF2407 DSP to determine if the processor meets the designers application requirements. Evaluators can create software to execute onboard or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The TMS320LF2407 will sometimes be referred to as the LF2407, F2407, or C24XX.

Program listings, program examples, and interactive displays are shown is a special italic typeface. Here is a sample program listing.

equations
!rd = rw &! strb;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments TMS320LF2407 Users Guide
Texas Instruments TMS320 Fixed Point Assembly Language Users Guide
Texas Instruments TMS320 Fixed Point C Language Users Guide
Texas Instruments TMS320 Fixed Point C Source Debugger Users Guide

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Chapter 1

Introduction to the TMS320LF2407 Evaluation Module

This chapter provides you with a description of the TMS32LF2407 Evaluation Module along with the key features and a block diagram of the circuit board.

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1.0 Overview of the TMS320LF2407 EVM

The TMS320LF2407 evaluation module(EVM) is a stand-alone card that lets evaluators examine certain characteristics of the LF2407 digital signal processor(DSP) to determine if this DSP meets their application requirements. Furthermore, the module is an excellent platform to develop and run software on the LF2407 family of processors.

The LF2407 EVM is shipped with a TMS320LF2407 DSP. The EVM allows full speed verification of LF2407 code. With 544 words of onchip data memory, 128K words of onboard memory, onchip flash rom, on chip UART, and an MP7680 Digital to Analog Converter, the board can solve a variety of problems as shipped. Four expansion connectors are provided to interface to any necessary evaluation circuitry not provided on the as shipped configuration.

To simplify code develop and shorten debugging time a number of user interfaces are available.

1.1 Key Features of the TMS320LF2407 EVM

The LF2407 EVM has the following features:

- LF2407 operating at 30 MIPS with 128K words of zero wait state memory
- 16 channels of 10 bit onchip Analog to Digital Conversion with auto sequencer
- Dual event managers multiple PWM and capture channels on chip
- DAC7625 Four(4) Channel Digital to Analog converter
- On chip UART with RS232 Drivers
- 32K words of on chip Flash ROM
- CAN Interface with drivers
- User Switches and LEDs
- 4 Expansion Connectors (data, address, I/O, and control)
- On board IEEE 1149.1 JTAG Connection for Optional Emulation
- 5 volt power input, (onboard 3.3 volt regulators)

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1.2 Functional Overview of the TMS320LF2407 EVM

Figure 1-1 shows a block diagram of the basic configuration for the LF2407 EVM. The major interfaces of the EVM include the target ram, analog interface, CAN interface, serial boot rom, user leds and switches, RS232 interface, SPI data logging interface, and expansion interface.

The LF2407 interfaces to 128K Words of zero wait-state static memory. An external I/O interface supports 65,000 parallel I/O ports. An onchip CAN and RS232 serial port are available on the expansion connector.

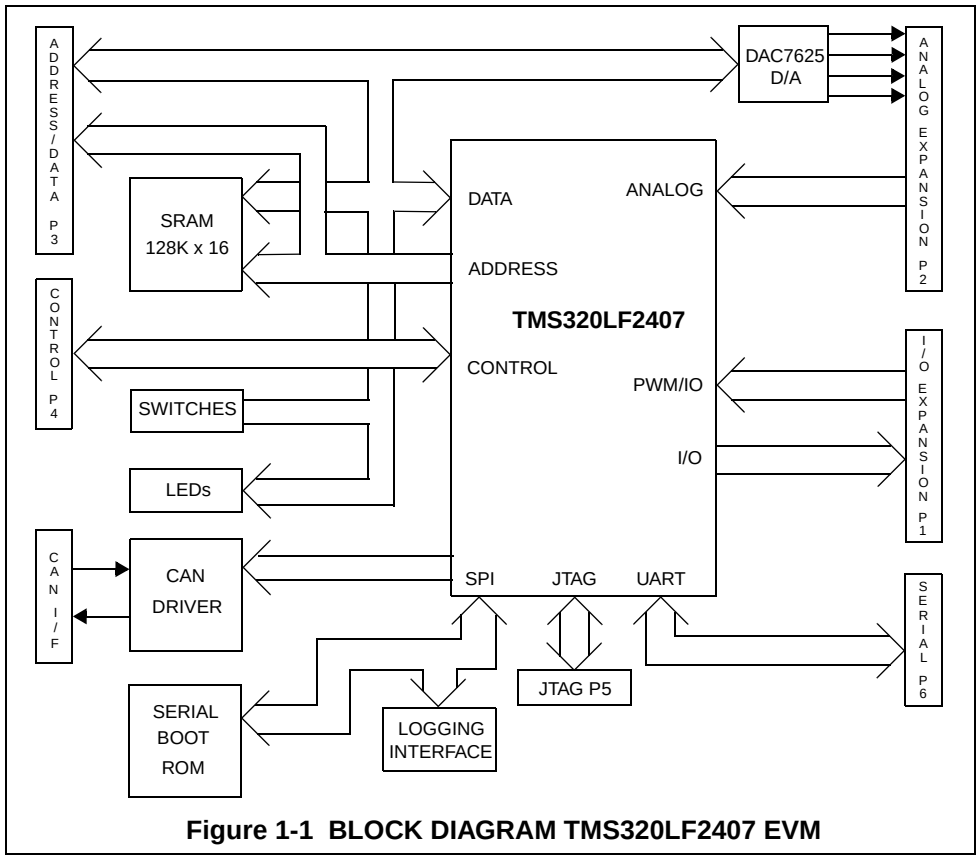


Figure 1-1 BLOCK DIAGRAM TMS320LF2407 EVM

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Chapter 2

Operation of the TMS320LF2407 Evaluation Module

This chapter describes the operation of the TMS32LF2407 Evaluation Module along with the key interfaces and an outline of the circuit board.

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2.0 The TMS320LF2407 EVM Operation

This chapter describes the LF2407 Evaluation module, its key components, and how they operate. It also provides information on the EVM's various interfaces. The LF2407 EVM consists of six major blocks of logic.

- LF2407 external memory
- Digital to Analog Interface
- On Chip Serial Interface
- LEDs and Switches
- On Chip CAN Interface
- Serial boot ROM/ SPI Logging Interface
- Expansion interface
- JTAG Interface

2.1 The TMS320LF2407 EVM Board

The LF2407 EVM is a 3U sized board which is powered by an external 5 Volt only power supply. Figure 2-1 shows the layout of the LF2407 EVM.

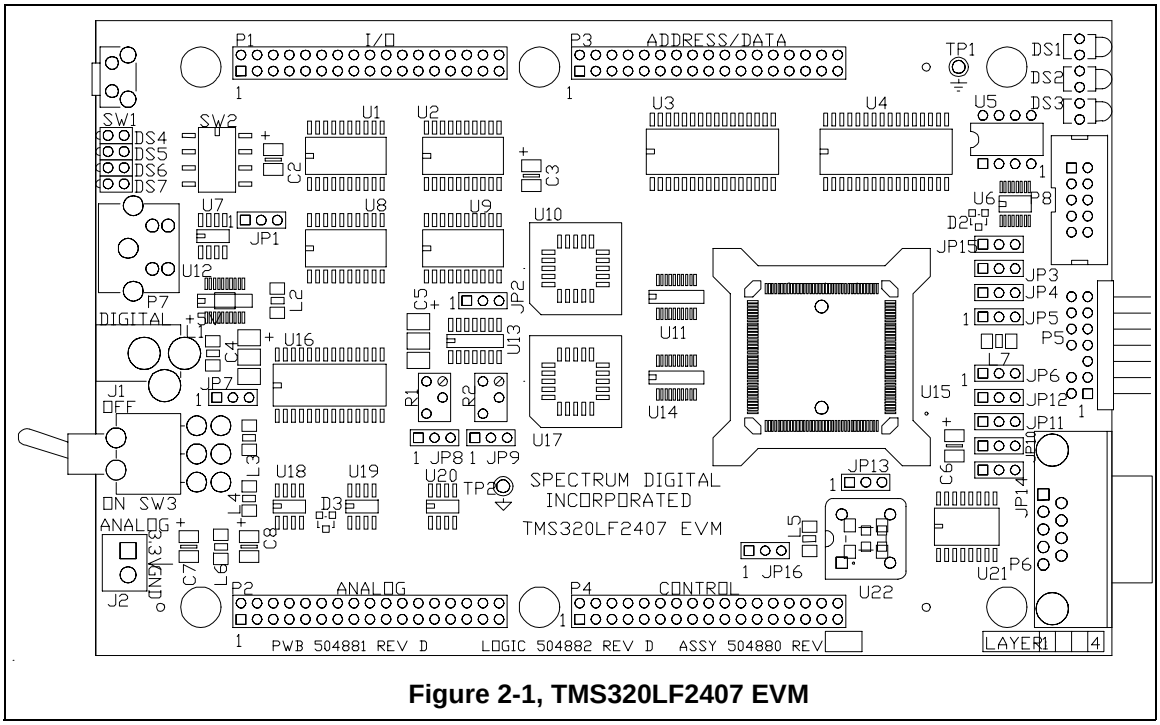


Figure 2-1, TMS320LF2407 EVM

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2.1.1 Power Connector

The LF2407 is powered by a 5 volt only power supply which is available with the module. An on board low drop out 3.3 volt regulator provides the 3.3 volt power. The board requires 750 milliamps at 5 volts. The power is supplied via 2 millimeter jack J1. If expansion boards are connected to the module a higher amperage power supply may be necessary.

2.2 TMS320LF2407 Memory Interface

The EVM includes 64k Words of zero wait-state program ram memory and 64k words of zero wait-state data ram memory, providing a total of 128k words of off chip static ram.

It is important to remember that internal memory has a higher precedence than the external memory. For more information on the memory in the device populated in your EVM card please refer to Texas Instruments TMS320LF2407 Users Guide. Futhermore, it is important to take into account that external memory is affected by wait-states. Wait state generation for off-chip memory space (data, program, or I/O) is done with the Wait State Generation Register(WSGR). To obtain zero waitstate off-chip memory bits in the WSGR must be appropriately programmed. The board powers up with 7 wait-states. The EVM board does not generate wait states via the ready signal for external program and data memory accesses.

External memory decode is done via U17 a GAL16V8. The generic array device selects the RAM, or on board peripherals. The equations for the GAL are included in Appendix A. The figure below shows a zero wait state program space memory read followed by a data space memory write.

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Figure 2-2 below shows the memory timing on the EVM320LF2407.

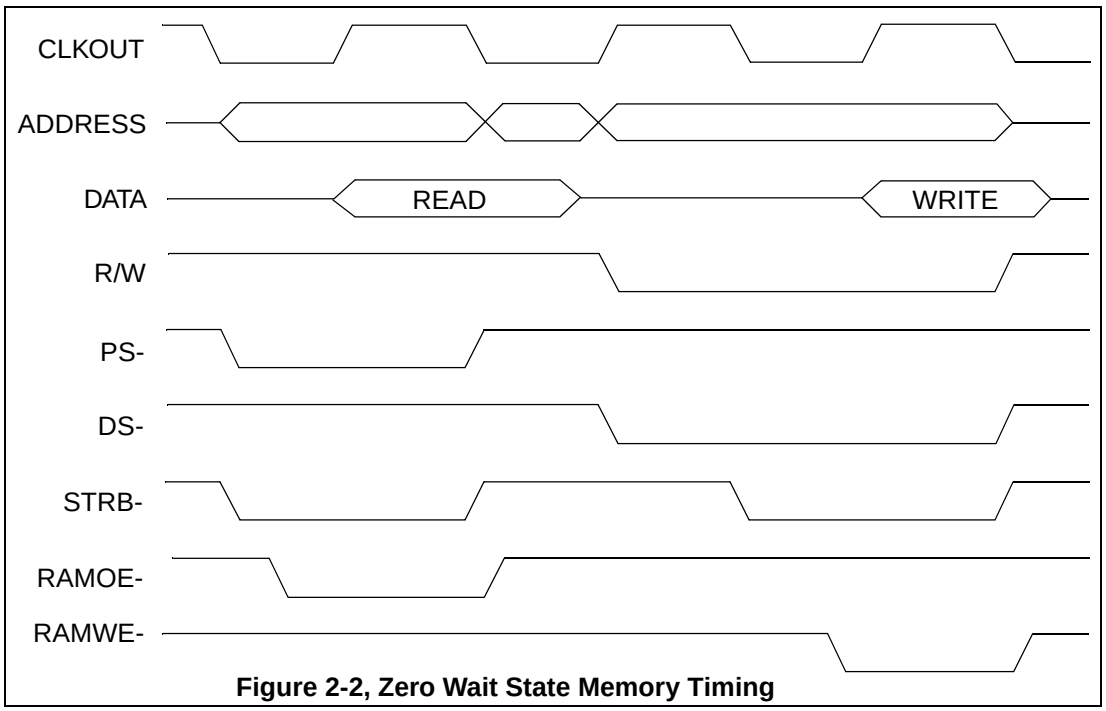


Figure 2-2, Zero Wait State Memory Timing

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2.2.1 Program Memory

There are two configurations for program memory. The selection of these configurations is done by the position of jumper, JP6. If JP6 is in the 2-3 position then the DSP is in microcomputer mode and the internal flash memory is enabled from 0x0000 to 0x7fff. If JP6 is in position 1-2 then the internal FLASH/ROM is disabled and the entire program address range is available to external memory.

Shown below are the two program memory configurations:

Program Space
MP/MC- = 1, JP6(1-2)
Microprocessor Mode

Hex	
0000 003F	Interrupts External RAM
0040 7FFF	External RAM
8000 87FF	On-Chip SARAM PON=1, External PON=0
8800 FDFF	External RAM
FE00 FEFF	On-Chip DARAM B0 (CNF = 1) External RAM (CNF = 0)
FF00 FFFF	On-Chip DARAM B0' (CNF = 1) External RAM (CNF = 0)

Program Space
MP/MC- = 0, JP6(2-3)
Microcomputer Mode

Hex	
0000 003F	Interrupts (On-chip) Flash
0040 7FFF	On Chip Flash
8000 87FF	On-Chip SARAM PON=1, External PON=0
8800 FDFF	External RAM
FE00 FEFF	On-Chip DARAM B0 (CNF = 1) External RAM (CNF = 0)
FF00 FFFF	On-Chip DARAM B0' (CNF = 1) External RAM (CNF = 0)

Figure 2-3, Program Memory Configurations

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2.2.2 Data Memory

The data memory configuration is shown below. External RAM is enabled from 0x8000-0xffff.

Hex	
0000 005F	Memory-Mapped Register and Reserved
0060 007F	On-Chip DARAM B2
0080 01FF	Reserved
0200 02FF	On-Chip DARAM B0 (CNF = 0) Reserved (CNF = 1)
0300 03FF	On-Chip DARAM B1' (CNF = 0) Reserved (CNF = 1)
0400 07FF	Reserved
0800 0FFF	SARAM DON=1 External DON=0
1000 6FFF	Illegal
7000 73FF	Peripheral Memory-Mapped Registers (System, ADC, SCI, SPI, I/O, Interrupts)
7400 743F	Peripheral Memory-Mapped Registers (Event Manager A)
7440 74FF	Reserved
7500 753F	Event Manager B
7540 77FF	Reserved
7800 7FFF	Illegal
8000 FFFF	External RAM JP7 = 1-2

Figure 2-4, Data Memory Configuration

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2.2.3 I/O Space

The I/O map for the TMS320LF2407 EVM is shown below:

Hex	
0000 0004	D/A Converter
0005 0007	Reserved
0008	4 Position DIP Switch
0009 000B	Reserved
000C	LEDs
000D 7FFF	Reserved
8000 FFFF	External

Figure 2-5, I/O Space Configuration

2.3 User Switches and LEDs

The TMS320LF2407 EVM has 4 switches and 4 LEDs that are available for user applications.These devices are I/O mapped at locations 0x0008 and 0x000C respectively on data bits D0-D3. To access these devices the “IN” and “OUT” instructions are used. Refer to sections 2.13 and 2.16 for more detail on these two items.

2.4 Oscillator Selection

The TMS320LF2407 EVM is equipped with a 7.37 Megahertz oscillator. The core CPU receives CLKIN/2 (CPUCLK). After resets the PLL Clock Module defaults to CPUCLK/4 yielding approximately a 2 Mhz clkout. The PLL can be programmed to CPUCLK*4 which results in 30 Mhz output clock. The user should refer to the “PLL Clock Module” section in the TMS320LF2407 User’s guide for more information.

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2.5 Digital to Analog Converter

The TMS320LF2407 EVM provides four (4) 12-bit D/A channels. The output is from 0 to 3.3 volts DC. The converter is mapped into I/O address space 0x0000 to 0x0004. Locations 0x0000 through 0x0003 are used for the data holding registers for channels 1-4 respectively. I/O address 0x0004 is used to transfer values in the holding registers to the converters. For instance you can write to the 4 holding registers and transfer all 4 to the converters at the same time. Information about programming this converter can be found in Appendix C.

Table 1: DAC I/O Addresses

I/O Address	Channel #
0x0000	1
0x0001	2
0x0002	3
0x0003	4
0x0004	Transfer

2.6 Expansion Bus

The TMS320LF2407 EVM has an expansion bus which brings out all of the signals from the DSP. This expansion bus allows the user to design custom circuitry to be used with his application without having to design a CPU card. In addition this interface is used by Spectrum Digital for all of its add-on modules.

2.6.1 TMS320LF2407 EVM Expansion Connector

Expansion boards interface to the TMS320LF2407 EVM via an expansion bus. This expansion bus is divided into 4 double row header connectors. This section contains the signal definitions and pin numbers for each of the connectors.

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2.6.1.1 Expansion I/O Connector

The definition of P1, which has the I/O signals is shown below.

Table 2: P1 I/O

Pin #	Signal	Pin #	Signal
1	VCC, +5 Volts	2	VCC, +5 Volts
3	PWM1/IOPA6	4	PWM2/IOPA7
5	PWM3/IOPB0	6	PWM4/IOPB1
7	PWM5/IOPB2	8	PWM6/IOPB3
9	PWM7/IOPE1	10	PWM8/IOPE2
11	PWM9/IOPE3	12	T1PWM/T1CMP/IOPB4
13	T2PWM/T2CMP/IOPB5	14	T3PWM/T3CMP/IOPF2
15	* TDIRA/IOPB6	16	* TCLKINA/IOPB7
17	GND	18	GND
19	BOOTEN-/XF	20	* BIO/IOPC1
21	* CAP1/QEP1/IOPA3	22	* CAP2/QEP2/IOPA4
23	* CAP3/IOPA5	24	* CAP4/QEP3/IOPE7
25	RESERVED	26	* PDPINTA-
27	SCITXD/IOPA0	28	* SCIRXD/IOPA1
29	* SPISIMO/IOPC2	30	* SPISOMI/IOPC3
31	* SPICLK/IOPC4	32	* SPISTE/IOPC5
33	GND	34	GND

***** Signal is interfaced through a quick switch to allow 5 volt tolerant inputs.

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2.6.1.2 Expansion Analog Connector

The definition of P2, which has the analog signals is shown below.

Table 3: P2 Analog

Pin #	Signal	Pin #	Signal
1	VCCA, +5V Analog	2	VCCA, +5V Analog
3	TMS2/IOPD7	4	* IOPF6
5	ADCIN2	6	ADCIN3
7	ADCIN4	8	ADCIN5
9	ADCIN6	10	ADCIN7
11	ADCIN8	12	ADCIN9
13	ADCIN10	14	ADCIN11
15	ADCIN12	16	ADCIN13
17	AGND	18	AGND
19	ADCIN14	20	ADCIN15
21	VREFHI	22	VREFLO
23	ADCIN0	24	ADCIN1
25	DACOUT1	26	DACOUT2
27	DACOUT3	28	DACOUT4
29	RESERVED	30	RESERVED
31	RESERVED	32	XINT2-/ADCSOC/IOPD1
33	AGND	34	AGND

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2.6.1.3 Expansion Address and Data Connector

The definition of P3, which has the address and data signals is shown below.

Table 4: P3 Address/Data

Pin #	Signal	Pin #	Signal
1	A0	2	A1
3	A2	4	A3
5	A4	6	A5
7	A6	8	A7
9	A8	10	A9
11	A10	12	A11
13	A12	14	A13
15	A14	16	A15
17	GND	18	GND
19	D0	20	D1
21	D2	22	D3
23	D4	24	D5
25	D6	26	D7
27	D8	28	D9
29	D10	30	D11
31	D12	32	D13
33	D14	34	D15

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2.6.1.4 Expansion Control Connector

The definition of P4, which has the control signals is shown below.

Table 5: P4 Control

Pin #	Signal	Pin #	Signal
1	VCC, +5 Volts	2	VCC, +5 Volts
3	DS-	4	PS-
5	IS-	6	WR-/IOPC0
7	WE-	8	RD-
9	STRB-	10	R/W-
11	READY	12	PDPINTB-
13	RS-	14	TRGRESET-
15	* PWM10/IOPE4	16	XINT1-/IOPA2
17	GND	18	GND
19	XINT2-/ADCSOC/IOPD1	20	CAP5/QEP4/IOPF0
21	CAP6/IOPF1	22	VISOE-
23	CANTX/IOPC6	24	CANRX/IOPC7
25	PWM10/IOPE4	26	PWM11/IOPE5
27	PWM12/IOPE6	28	T4PWM/T4CMP/IOPF3
29	TDIRB/IOPF4	30	TCLKINB/IOPF5
31	Expansion CLKIN	32	CLKOUT/IOPE0
33	GND	34	GND

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2.7 JTAG Interface.

The TMS320LF2407 Evaluation Module is supplied with a 14 pin header interface, P5. This is the standard interface used by JTAG emulators to interface to Texas Instruments DSPs. The pinout for the connector is shown below:

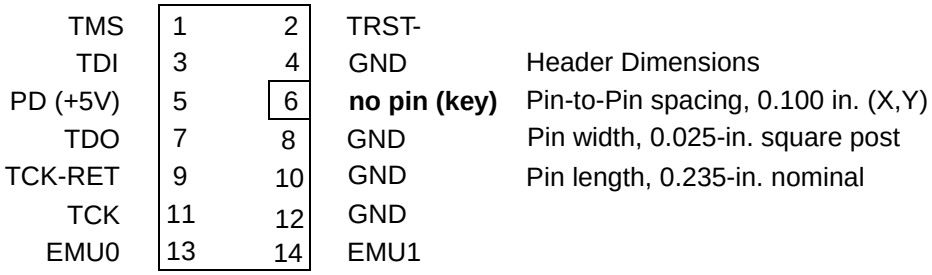


Figure 2-6, JTAG Connector Pinout

2.8 Logging Interface

The TMS320LF2407 has an on board SPI data logger interface which is compatible with the Spectrum Digital SPI515 emulator. This interface allows high speed data transfer logging using the LF2407's SPI port. The pin out for this connector is shown in the table below.

Table 6: Logging Interface

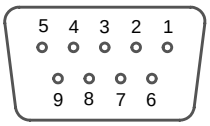
Pin #	Signal	Pin #	Signal
1	STE	2	GND
3	SPI Dataout	4	GND
5	SPICLK	6	GND
7	SPI Data In	8	GND
9	NC	10	GND

To direct the SPI port to the data logging interface jumper JP4 needs to be set to the 2-3 position.

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2.9 On-Chip Asynchronous Serial Port

The TMS320LF2407 DSP has an on-chip asynchronous serial port. This port is brought out to connector P6 on the EVM320LF2407. Connector P6 is a DB9 female connector. This RS232 connector allows the user to connect an external instrument or computer to the EVM320LF2407. This means data can be logged or commands given to the control algorithm. The user should refer to documentation on jumpers JP10, JP11, JP12, and JP14 prior to using this serial port. The pin positions for the P6 connector as viewed from the edge of the EVM320LF2407.



The pin numbers and their corresponding signals are shown in the table below:

Table 7: P6 RS232 Pinout

Pin #	PC (female)	SD EVM
2	Rx, input	Tx, output
3	Tx, output	Rx, input
4	DTR, output	Reset/CTS, input
5	GND	GND
8	CTS, input	RTS, output

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2.10 CAN Interface

The EVM320LF2407 has a CAN interface which provides an additional high speed serial interface. A 4 pin mini-DIN female connector, P7, is used to interface to the CAN bus. The pinouts for this connector are shown in the figure and table below. The CAN termination resistor is controlled by jumper JP12.

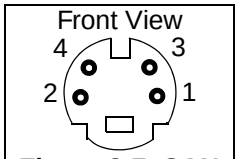


Figure 2-7, CAN Connector

Table 8: CAN Connector Signals

Pin #	Signal
1	CANH
2	CANL
3	GND
4	5 volt power out

WARNING !

Pins 3 and 4 are used for powering the Optically Isolated CAN interface. Because +5 volts is present on pin 4 do **NOT** connect pins 3 and 4 in normal operation.

2.10.1 CAN Mating Plugs

A 4 pin mini-DIN male plug can be used to mate with the P7 connector. A source for these plugs is shown in the table below.

Table 9: CAN Mating Plugs

Vendor	Part #
Digikey	CP-2040
LZR Electronics	MD40

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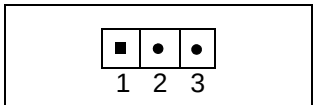
2.11 EVM320LF2407 Jumpers

The TMS320LF2407 EVM has 16 jumpers which determine how features on the EVM are utilized. The table below lists the jumpers and their function. The following sections describe the use of each jumper.

Table 10: EVM320LF2407 Jumpers

Jumper #	Size	Function
JP1	1 x 3	CAN Termination Select
JP2	1 x 2	CAN Input Select
JP3	1 x 3	Serial RAM Write Protect Select
JP4	1 x 3	SPI Port Routing Select
JP5	1 x 3	Flash/Watchdog Select
JP6	1 x 3	MP/$\overline{MC}$ Select
JP7	1 x 3	Analog Power Select
JP8	1 x 3	VREF HI Select
JP9	1 x 3	VREF LO Select
JP10	1 x 3	Host Reset Select
JP11	1 x 3	BIO Hardware Handshaking
JP12	1 x 3	SCI Receive Select
JP13	1 x 3	Clock Input Select
JP14	1 x 3	DTS/RTS Select
JP15	1 x 3	SPI/SCI Bootloader Selection
JP16	1 x 3	BOOTEN Select

Each jumper on the TMS320LF2407 EVM is a 1x3 jumper. Each jumper must have the selection 1-2 or 2-3. The #2 pin is the center pin. The #1 pin has a square solder pad and can be seen from the solder side of the printed circuit board. This pin is usually marked with a '1' on the boards silkscreen. A top view of this type of jumper is shown below.



1x3 Jumper Layout

WARNING !
Unless noted otherwise, all jumpers must be installed in either the 1-2 or 2-3 position

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The figure below shows the position of the jumpers on the LF2407 EVM.

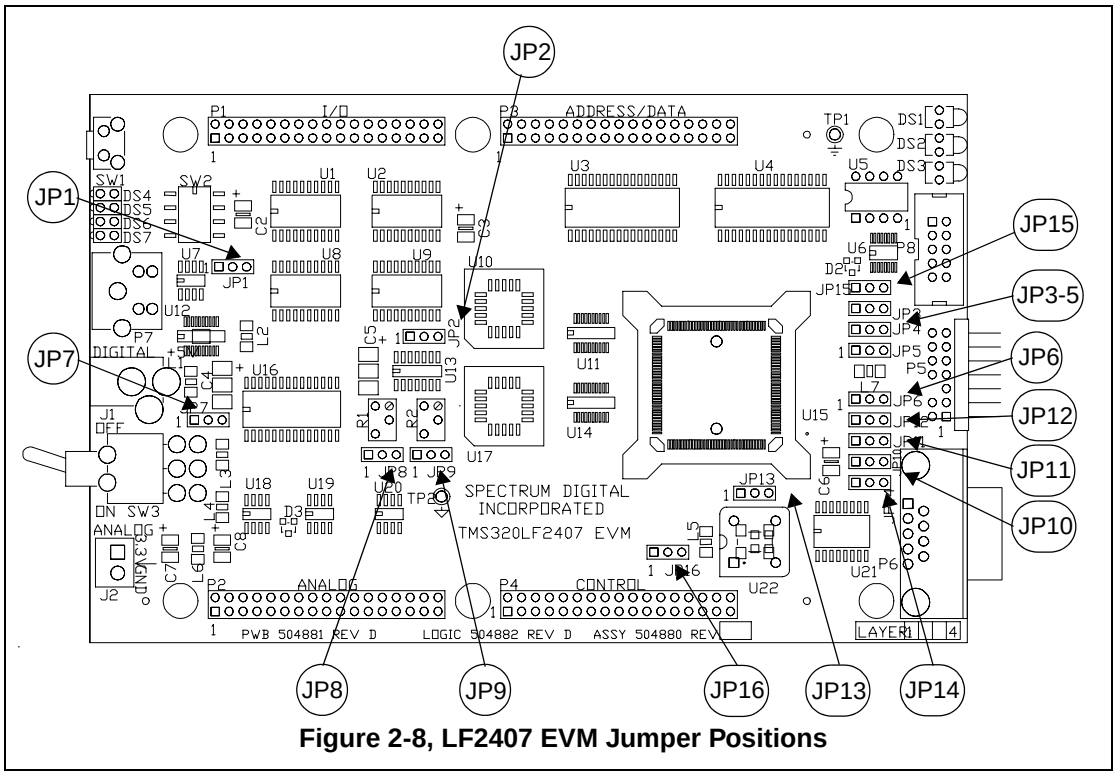


Figure 2-8, LF2407 EVM Jumper Positions

2.11.1 Jumper JP1, Enable/Disable CAN Terminator

Jumper JP1 enables or disables the CAN termination resistor. Using position 2-3 enables the termination resistor. If position 1-2 is used the termination resistor is disabled. The table below shows the positions and their functions.

Table 11: Jumper JP1

Position	Function
1-2	Disable Termination Resistor
2-3	Enable Termination Resistor

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2.11.2 Jumper JP2, CAN Input Select

Jumper JP2 is used to select the source of the CANRX input signal. If position 1-2 is selected the CAN input signal is connected to the CAN receiver. Using position 2-3 allows the CANRX/IOPC7 connected to the expansion connector P4, pin 24 to be used as the signal source. The table below shows the positions and their functions.

Table 12: Jumper JP2

Position	Function
1-2	CAN Connector, P7
2-3	Expansion Connector

2.11.3 Jumper JP3, Serial ROM Write Protect Select

The serial ROM can be write protected to prevent a spurious cycles from corrupting the contents of the serial ROM.

Jumper JP3 is used to select the protect/unprotect mode of the serial ROM. If position 1-2 is used the ROM is writable. Using position 2-3 write protects the ROM. The table below shows the positions and their functions.

Table 13: Jumper JP3

Position	Function
1-2	Write enabled
2-3	Write protected

2.11.4 Jumper JP4, SPI Port Routing Select

Jumper JP4 is used to select the routing of the SPI port. The SPI port can be routed to the Expansion connector/Serial ROM or to the P8 data logging connector. If position 2-3 is used the SPI is routed to the data logging connector. Using position 1-2 routes the SPI to the Expansion connector/Serial ROM. The table below shows the positions and their functions.

Table 14: Jumper JP4

Position	Function
1-2	SPI routed to expansion connector/serial ROM
2-3	SPI routed to P8 data logging connector

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2.11.5 Jumper JP5, Enable/Disable Flash Programming

Jumper JP5 is connected to the VCCP pin of the TMS320LF2407. On the LF2407 device this pin enables the programming of the internal flash memory. It also allows disabling the watchdog timer module. Refer to the LF2407 User's Guide for the programming sequence to disable the watchdog timer. The table below shows the positions and their functions.

Table 15: Jumper JP5

Position	Function
1-2	Disable Flash Programming
2-3	Enable Flash Programming

2.11.6 Jumper JP6, MP/$\overline{MC}$ - Enable/Disable Internal FLASH ROM

Jumper JP6 is connected to the MP/$\overline{MC}$ pin on the TMS320LF2407. When the jumper is in position 1-2 the internal FLASH ROM is disabled. If the shorting plug is in the 2-3 position the internal memory is then enabled. The table below shows the positions and their functions.

Table 16: Jumper JP6

Position	Function
1-2	Internal ROM/FLASH disabled (microprocessor mode)
2-3	Internal ROM/FLASH enabled (microcomputer mode)

2.11.7 Jumper JP7, Analog Power Supply Select

Jumper JP1 selects the source of the power for the analog logic on the EVM320LF2407. In the 1-2 position filtered digital power is used to power the analog logic on the EVM. If the 2-3 position is used, power to the analog section of the EVM is supplied via terminal block connector P2. The table below shows the positions and their functions.

Table 17: Jumper JP7

Position	Function
1-2	Selects digital power for analog logic
2-3	Selects connector P2 as analog power source

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2.11.8 Jumper JP8, VREFHI Select

Jumper JP8 is used to select the source for the VREFHI pin on the TMS320LF2407. Position 1-2 selects the VCCA power which is +3.3 volts. If position 2-3 is used trim pot R1 is used which allows a variable VREF High from 0-3.3 volts. The table below shows the positions and their functions.

Table 18: Jumper JP8

Position	Function
1-2	VCCA (+3.3V VrefH)
2-3	Trim Pot R1 (0-3.3V VrefH)

2.11.9 Jumper JP9, VREFLO Select

Jumper JP9 is used to select the source for the VREFLO pin on the TMS320LF2407. Position 1-2 selects the Analog ground. If position 2-3 is used trim pot R2 is used The table below shows the positions and their functions.

Table 19: Jumper JP9

Position	Function
1-2	Analog Ground (VrefL)
2-3	Trim Pot R2 (0-3.3V VrefL)

2.11.10 Jumper JP10, Enable/Disable Host Reset via DTR-

Jumper JP10 allows the generation of system resets from the serial port P7. When position 2-3 is used this feature is enabled meaning the system is reset when pin 4 (DTR-) is pulled low. This feature is disabled when position 1-2 is used. The table below shows the positions and their functions.

Table 20: Jumper JP10

Position	Function
1-2	Disabled
2-3	Reset from P4, pin4 (DTR-) enabled

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2.11.11 Jumper JP11, Enable/Disable RTS to BIO-/IOPC1

Jumper JP11 enables the serial port P6 RTS- to the DSP's BIO-/IOPC1 pin. Using position 1-2 disables this feature, while position 2-3 enables it. This is used when hardware handshaking is required on a serial port communication protocol.

Note:

If this feature is enabled (2-3) then you **must not** drive the BIO-/IOPC1 pin from the control connector P4

The table below shows the positions and their functions.

Table 21: Jumper JP11

Position	Function
1-2	Disables P6 RTS- to BIO-/IOPC3
2-3	Enables P6 RTS- to BIO-/IOPC3

2.11.12 Jumper JP12, Enable/Disable RXD to SCIRXD/IOPA1

Jumper JP12 enables the serial port P6 RXD to the DSP's SCIRXD/IOPA1 pin. If position 1-2 is selected this features is enabled. Selecting position 2-3 disables this feature and the SCIRXD/IOPA! pin is available on the expansion connector.

Note:

If this feature is enabled (1-2) then the SCIORXD/IO pin from the Control connector P4 is ignored.

The table below shows the positions and their functions.

Table 22: Jumper JP12

Position	Function
1-2	Enables P6 RXD to DSP SCIRXD/IO
2-3	Disables P6 RXD to DSP SCIRXD/IO

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2.11.13 Jumper JP13, Oscillator Source Select

Jumper JP13 is used to select the source of the TMS320LF2407 Clockin. Jumper position 1-2 selects the onboard oscillator. If position 2-3 is used the clock is from pin 31 on the Control connector P4. The table below shows the positions and their functions.

Table 23: Jumper JP13

Position	Function
1-2	Selects Onboard Oscillator
2-3	Selects Pin 31 on Control connector P4

2.11.14 Jumper JP14, DTS/RTS Select

Jumper JP14 is used to select the DTS or RTS signal for interrupts to the DSP. If position 1-2 is selected the DTS signal is used to interrupt the DSP. Using position 2-3 allows the RTS signal to interrupt the DSP. The table below shows the positions and their functions.

Table 24: Jumper JP14

Position	Function
1-2	DTS is selected
2-3	RTS is selected

2.11.15 Jumper JP15, SPI/SCI Bootloader Select

The jumper JP15 allows the user to select the source of the on chip bootloader. The user can either select the SPI or SCI resource on the TMS320LF2407. Using position 1-2 selects the SPI as the bootloader source. The 2-3 position allows the SCI to be used as the source. The table below shows the positions and their functions.

Table 25: Jumper JP15

Position	Function
1-2	Use SPI
2-3	Use SCI

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2.11.16 Jumper JP16, Booten Select

The EVM320LF2407 has the ability to load code from an external serial EEPROM via the on chip boot loader or the RS-232 serial link. To use the bootloader function the DSP must be in microcontroller mode (JP6). For serial ROM boot loading the SPI is routed to the serial ROM (JP4), and JP16 must be in the 2-3 position. JP15 should be set to SPI. For RS-232 boot loading JP4 is a “don’t care”. JP6 is again in microcontroller mode. JP15 is set to SCI. Using position 1-2 disables the on chip serial boot loader. The table below shows the positions and their functions.

Table 26: Jumper JP16

Position	Function
1-2	Disable boot loading
2-3	Enables boot loading

2.12 Status LEDs

The TMS320LF2407 EVM has three status light emitting diodes. Two of these are under software control. DS3 is ‘on’ when power is applied. These are shown in the table below.

Table 27: Status LEDs

LED #	Color	Controlling Signal	On Signal State
DS1	Red	W/R-/IOPC0 on DSP	1
DS2	Yellow	BIO-/IOPC1 on DSP	1
DS3	Green	Power On	N/A

2.13 User Programmable LEDs

The EVM320LF2407 has four user programmable light emitting diodes. These LEDS are programmed by writing a binary values to address 0x000C in I/O space. The table below shows the values to turn on the LEDs.

Table 28: User Programmable LEDs

LED #	Color	Controlling Value	On Signal State
DS4	Red	0x01	1
DS5	Red	0x02	1
DS6	Red	0x04	1
DS7	Red	0x08	1

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2.14 Resets

There are multiple resets for the TMS320LF2407 EVM. The first reset is the power on reset which is generated by the power regulator, U12. This device waits until power is within the specified voltage range before releasing the power on reset pin to the TMS320LF2407.

There is also a system reset RS- which is both input and output from the TMS320LF2407. Internal conditions such as a watchdog time-out will cause the RS- pin to go low. External sources such as the push button(SW1), Host reset pin 4 on P4, and pin 13 on the Control connector P4 can generate a reset condition.

2.15 Reset Switch

Switch SW1 is the user RESET switch. By momentarily depressing this switch the $\overline{RS}$ signal is asserted to the TMS320LF2407 DSP.

2.16 User Readable Switches

The EVM320LF2407 has four a position DIP switch, SW2. Each position can be manually set by the user and read by the DSP. This switch can be read from I/O location 0x0008. A position on the “ON” position will read as a “1”. The table below shows the values read for the respective positions.

Table 29: User Programmable LEDs

Position	Value Read	Switch State
1	0x01	On
2	0x02	On
3	0x04	On
4	0x08	On

2.17 ON/OFF Switch

Switch SW3 controls both the analog and digital power. Flipping this switch to the “ON” position powers up the EVM.

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2.18 Test Points

Two test points are provided on the TMS320LF2407 EVM. They are connected to the GND, and analog ground planes. These are used for connecting test instrument's ground probes. The table below shows the test points and their signals.

Table 30: Test Points

Test Point #	Signal
TP1	GND
TP2	Analog Ground

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Appendix A

TMS320LF2407 EVM PAL Equations

This appendix lists the two PAL logic equations that are used on the TMS320LF2407 Evaluation Module (EVM).

Topic **Page**

A.1	**Decode PAL Equations**	**A-2**
A.2	**Glue Logic PAL Equations**	**A-5**

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A.1 Decode PAL Equations

The following PAL equations are used for the decode logic

```
/*
**  504883a.tdl
**  Drawing Number: 504883a
**  Title: TMS320LF2407 EVM Decode
**  Customer Name: Spectrum Digital Inc.
**  Company: Spectrum Digital Inc.
**  Engineer: Ron Peterson
*/
504883(in     A2,             /* A2              */
              A3,             /* A3              */
              A15,            /* A15             */
              Rw,             /* R/W-            */
              !We,            /* WE-             */
              !Rd,            /* RD-             */
              !Ps,            /* PS-             */
              !Ds,            /* DS-             */
              !Is,            /* IS-             */
              !Strb,          /* STRB-           */
              !WR;            /* WR-             */


          out
              !Ramoe,         /* SRAM Ouput Enable */
              !Buffen;        /* I/O Buffer Enable  */

          io
              !Ramwe,         /* SRAM Write Enable  */
              !Dac,           /* DAC Register Write  */
              !Xfer,          /* DAC Output Transfer */
              !Leds,          /* LED Write Strobe    */
              !Switches;      /* Switch Read Strobe  */

      )
{

/* Uncomment next line for test vectors */
#define TEST_VEC

/* Define Address Ranges */

#define DAC             ( Is & !A15 & !A3 & !A2 )
#define XFER            ( Is & !A15 & !A3 &  A2 )
#define SWITCHES        ( Is & !A15 &  A3 & !A2 )
#define LEDS            ( Is & !A15 &  A3 &  A2 )
```


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```
/* Output enables */

Ramoe.oe      = 1;
Ramwe.oe      = 1;
Dac.oe        = 1;
Xfer.oe       = 1;
Leds.oe       = 1;
Switches.oe   = 1;
Buffen.oe     = 1;


/* equations */

Ramoe    = (( Ds | Ps ) & Rw & Strb );

Ramwe    = (( Ds | Ps ) & We );

Dac      = ( DAC & We );

Xfer     = ( XFER & We );

Switches = ( SWITCHES & Rw & Strb );

Leds     = ( LEDS & We );

Buffen   = (( DAC | LEDS | SWITCHES ) & Strb );


/* Part assignment */

putpart("g16v8", "504883a",
        A2, A3, A15, WR, We, Strb, Rw, Is, Ps, GND,
        Ds, Ramoe, Ramwe, Dac, Xfer, Leds, Switches, Rd, Buffen, VCC );

#ifdef TEST_VEC

/* Test Vectors */
test( Strb, Rw, We, Ds, Ps, Is, A15, A3, A2 =>
        Ramoe, Ramwe, Dac, Xfer, Leds, Switches, Buffen )
{

/* Test Ram */
( 1, 0, 1, 1, 1, 1, 0, 0, 0 => 1, 1, 1, 1, 1, 1, 1 );
( 0, 0, 0, 1, 0, 1, 0, 0, 0 => 1, 0, 1, 1, 1, 1, 1 );          /* Ram Data Write */
( 0, 0, 0, 0, 1, 1, 0, 0, 0 => 1, 0, 1, 1, 1, 1, 1 );          /* Ram Prog Write */
( 0, 1, 1, 1, 0, 1, 0, 0, 0 => 0, 1, 1, 1, 1, 1, 1 );          /* Ram Data Read */
( 0, 1, 1, 0, 1, 1, 0, 0, 0 => 0, 1, 1, 1, 1, 1, 1 );          /* Ram Prog Read */
```


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```
/* I/O Tests */
( 1, 0, 1, 1, 1, 1, 0, 0, 0 => 1, 1, 1, 1, 1, 1, 1 );
( 0, 0, 0, 1, 1, 0, 0, 0, 0 => 1, 1, 0, 1, 1, 1, 0 );          /* Write Dac's       */
( 0, 0, 0, 1, 1, 0, 0, 0, 1 => 1, 1, 1, 0, 1, 1, 1 );          /* Update Dac's      */
( 0, 1, 1, 1, 1, 0, 0, 1, 0 => 1, 1, 1, 1, 1, 0, 0 );          /* Read Switches */
( 0, 0, 0, 1, 1, 0, 0, 1, 1 => 1, 1, 1, 1, 0, 1, 0 );          /* Write LED's       */
}

#endif

}
```


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A.2 Glue Logic PAL Equations

The following PAL equations are used for the glue logic control.

```
/*
**  504884b.tdl
**  Drawing Number: 504884
**  Title: TMS320LF2407 EVM Decode
**  Customer Name: Spectrum Digital Inc.
**  Company: Spectrum Digital Inc.
**  Engineer: Ron Peterson
*/
504884(inA0,                    /* DSP address a0              */
        A1,                     /* DSP address a1              */
        !Dac,                   /* DAC Write Strobe            */
        !Xfer,                  /* DAC Write Strobe            */
        !TrgReset,              /* Target Power On Reset       */
        SwReset,                /* Reset Switch                */
        HostReset,              /* Serial Port Reset Input     */
        !PowerOnReset;          /* Power On Reset              */


out RS;
out  !DacCs;
      io
      RsEn,
      La0,                      /* Latched A0          */
      La1;                      /* Latched A1          */

)
{



/* Uncomment next line for test vectors */
/* #define TEST_VEC     */

/* Output enables */

Dac_Cs.oe = 1;
La0.oe    = 1;
La1.oe    = 1;
RsEn.oe   = 1;
Rs.oe     = RsEn;
```


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```
/* equations */

La0    = (  Dac & A0 )
           | ( !Dac & La0 );

La1    = (  Dac & A1 )
           | ( !Dac & La1 );

RsEn     = ( SwReset | TrgReset | HostReset | PowerOnReset);

Rs       = 1;
Dac_Cs = Dac;

  /* Part assignment */

putpart("g16v8", "504884b",
        _, Dac, Xfer, SwReset, TrgReset, A0, A1, HostReset, PowerOnReset, GND,
        _, _, La0, La1, _, Dac_Cs, Rs, RsEn,  _,  VCC );

#ifdef TEST_VEC
/* Test Vectors */
test( Reset, TrgReset, Dac, A1, A0 => La0, La1 )
{
/* Put in known state */
( 1, 1, 0, 0, 0 => 0, 0 );

/* Test Reset */
        ( 1, 0, 1, 0, 0 => 0, 0 );   /* Onboard Reset        */
        ( 0, 1, 1, 0, 0 => 0, 0 );   /* Target Reset         */

/* Test Latch */
        ( 1, 1, 1, 0, 0 => 0, 0 );   /* Latch closed         */
        ( 1, 1, 1, 1, 1 => 0, 0 );   /* Holding old value    */
        ( 1, 1, 0, 1, 1 => 1, 1 );   /* Open Latch           */
        ( 1, 1, 1, 1, 1 => 1, 1 );   /* Close latch          */
        ( 1, 1, 1, 0, 0 => 1, 1 );   /* Holding old value    */
}
#endif
}
```

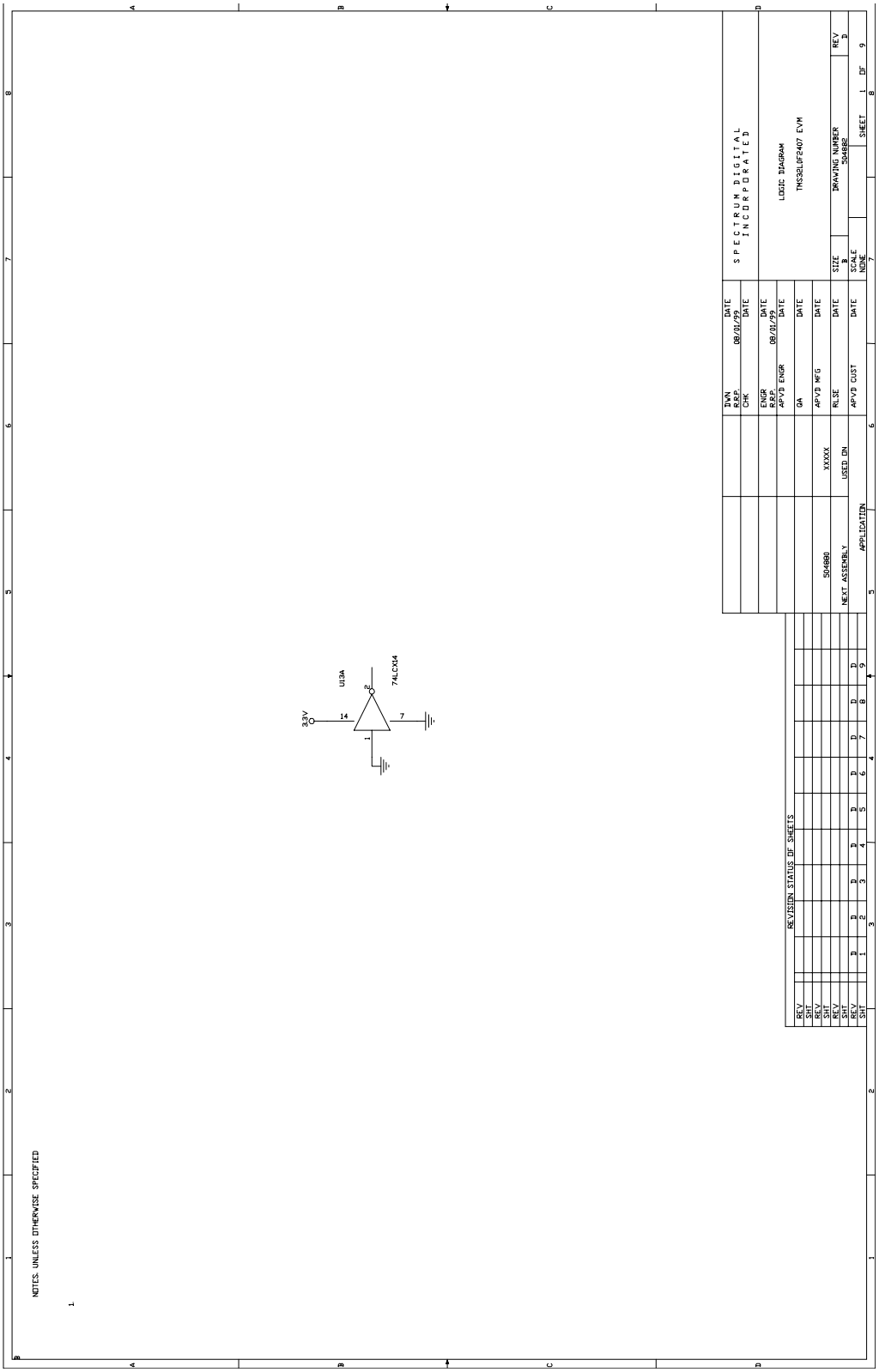

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Appendix B

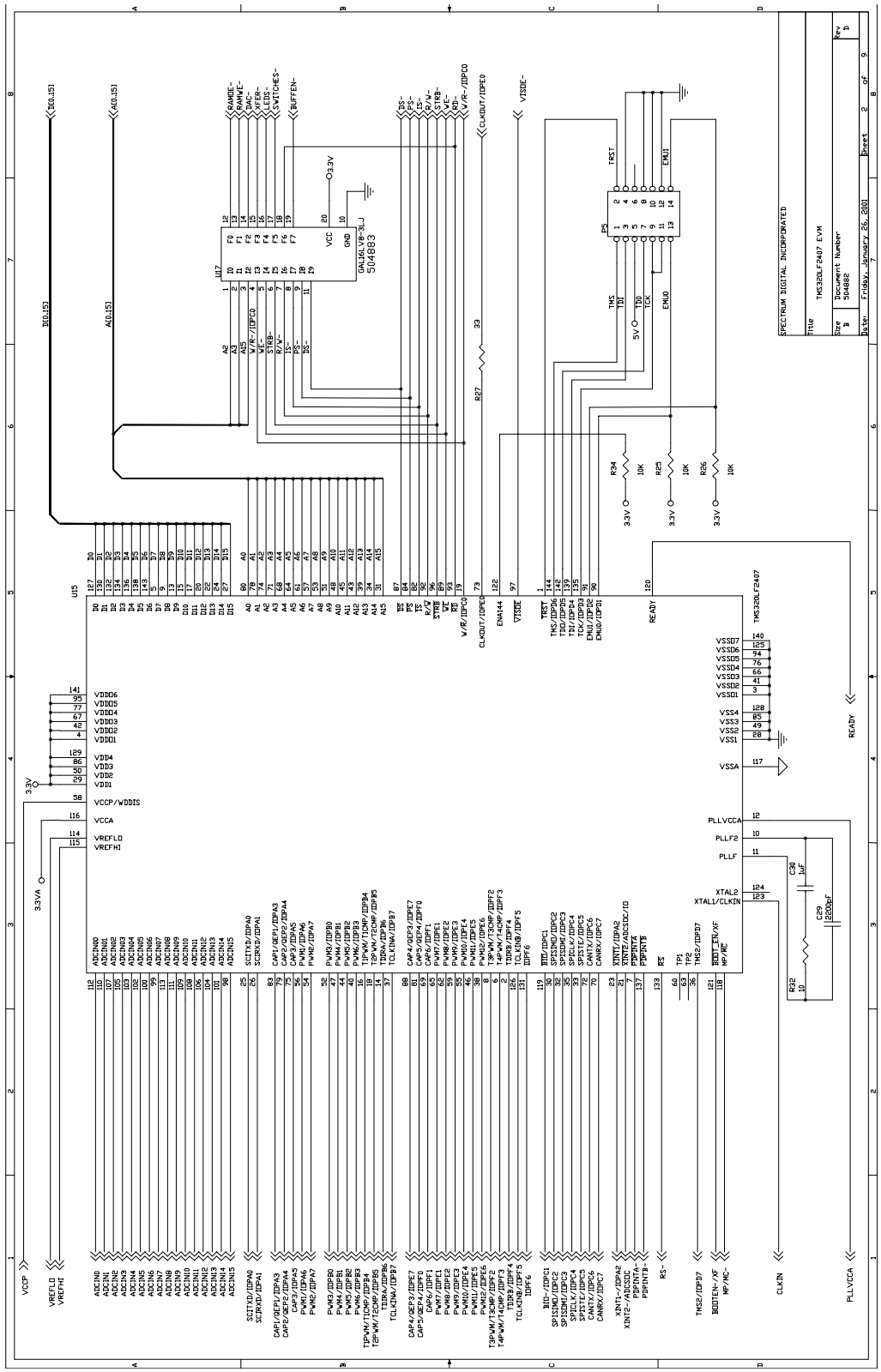
TMS320LF2407 EVM Schematics

This appendix contains the schematics for the TMS320LF2407 EVM. The schematics were drawn on ORCAD.

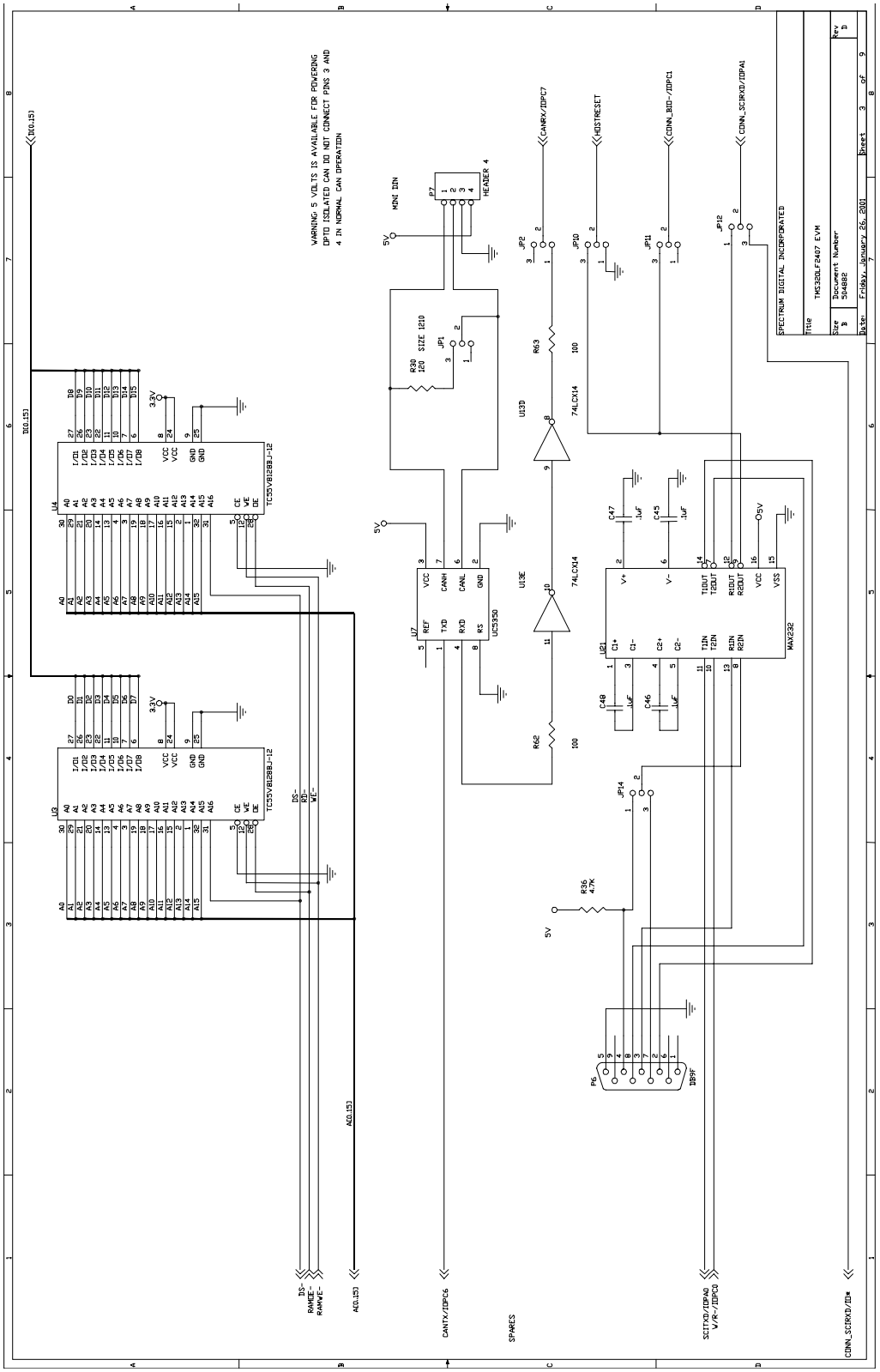
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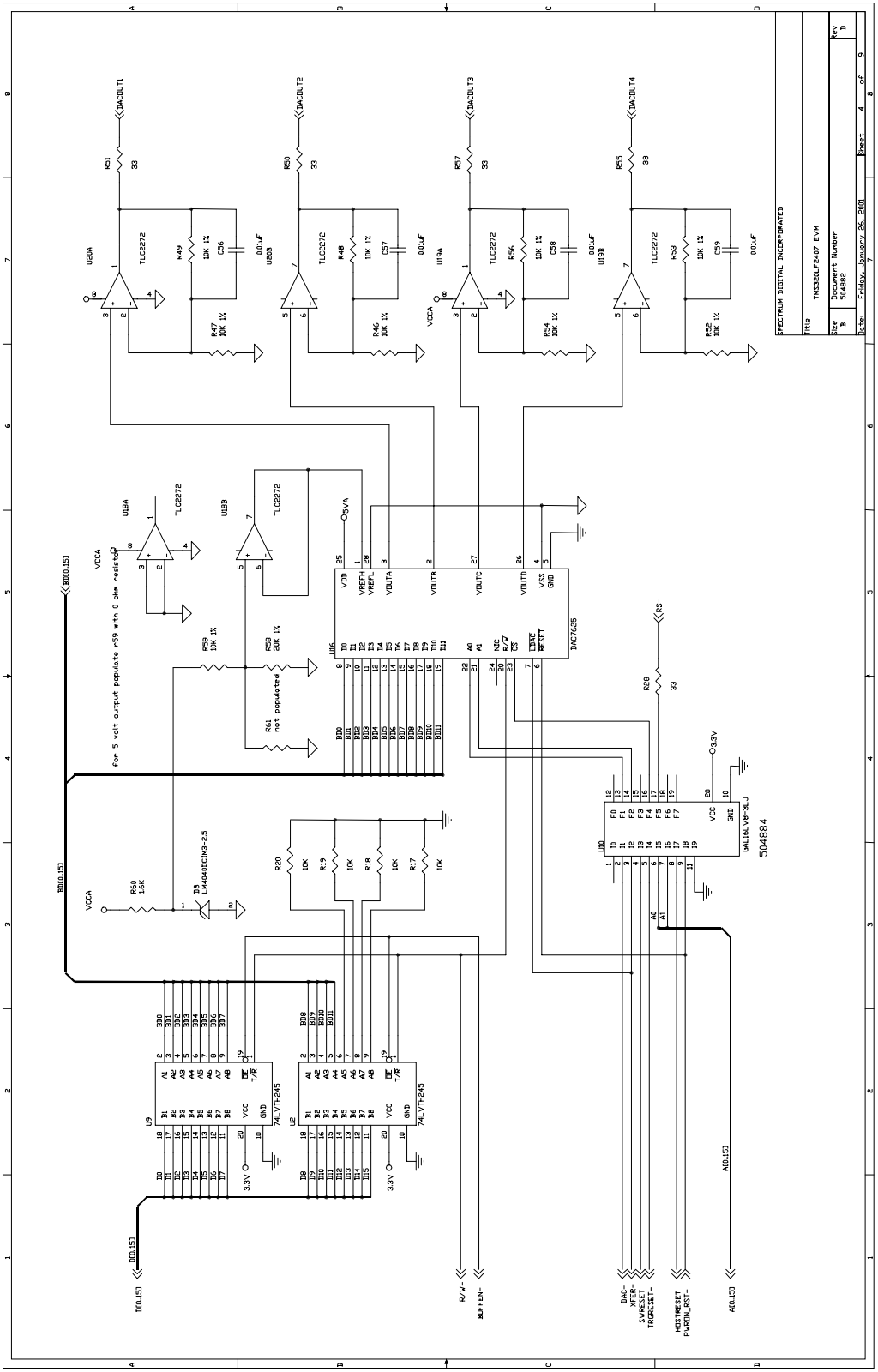
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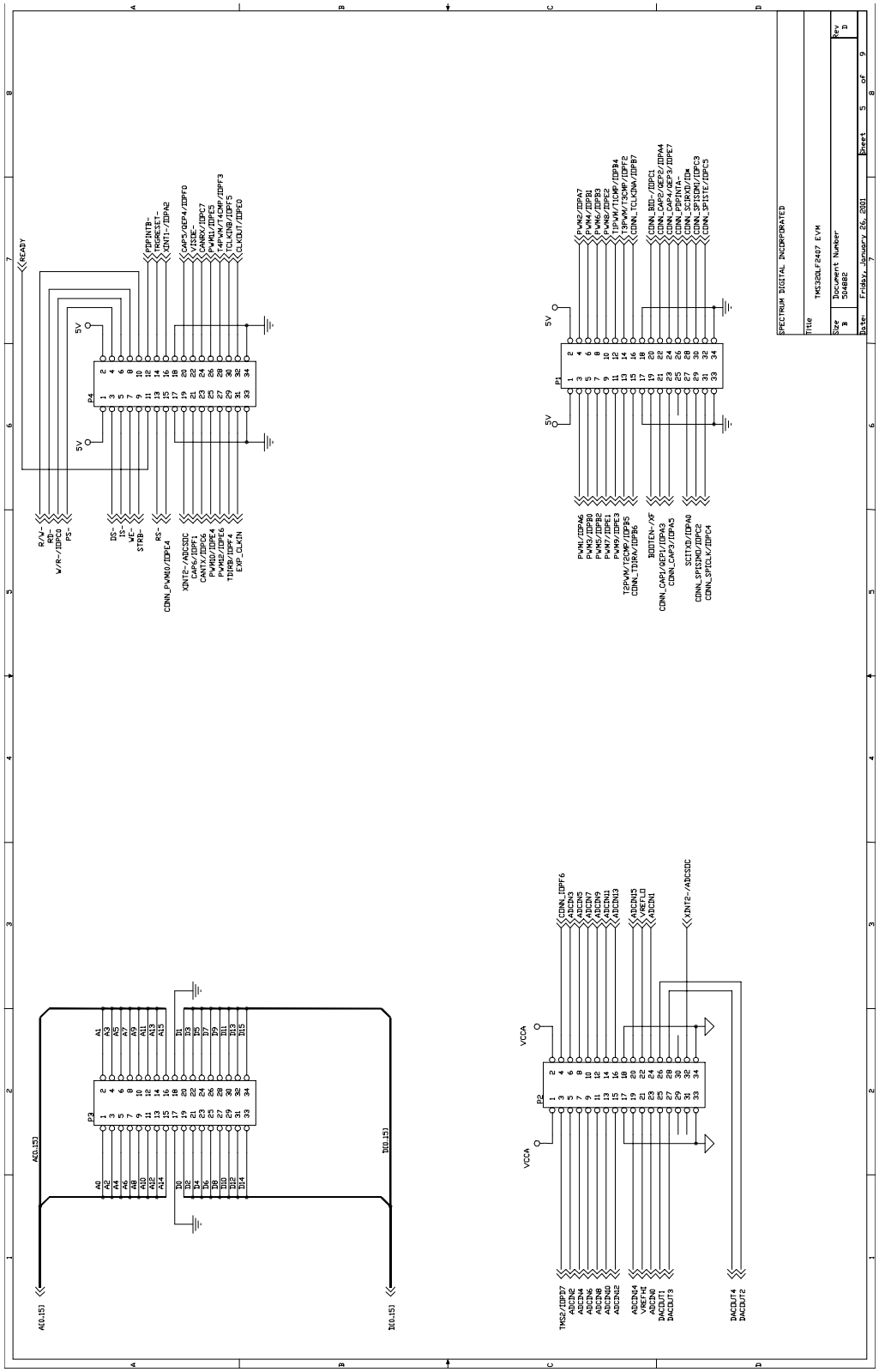
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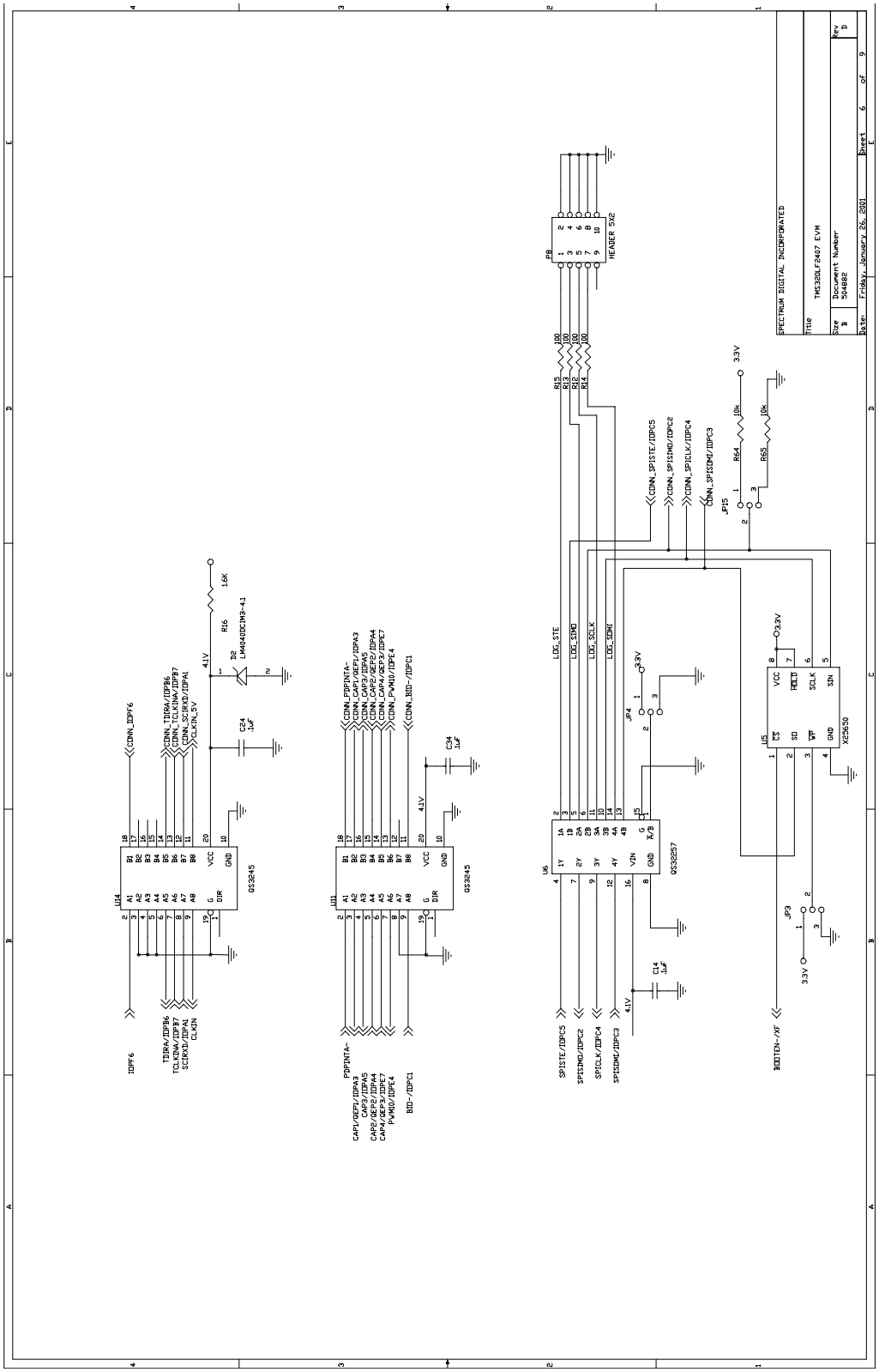
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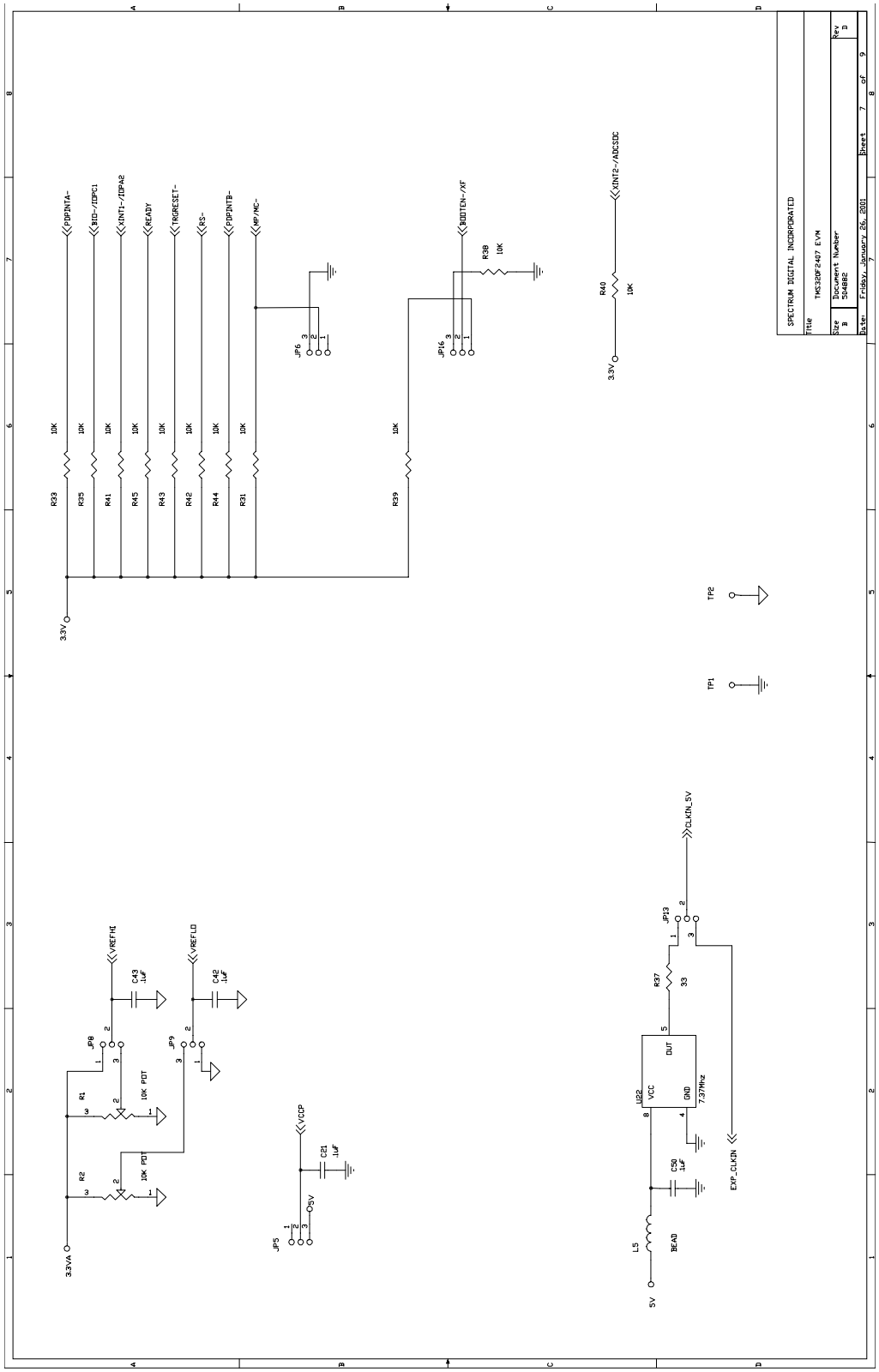
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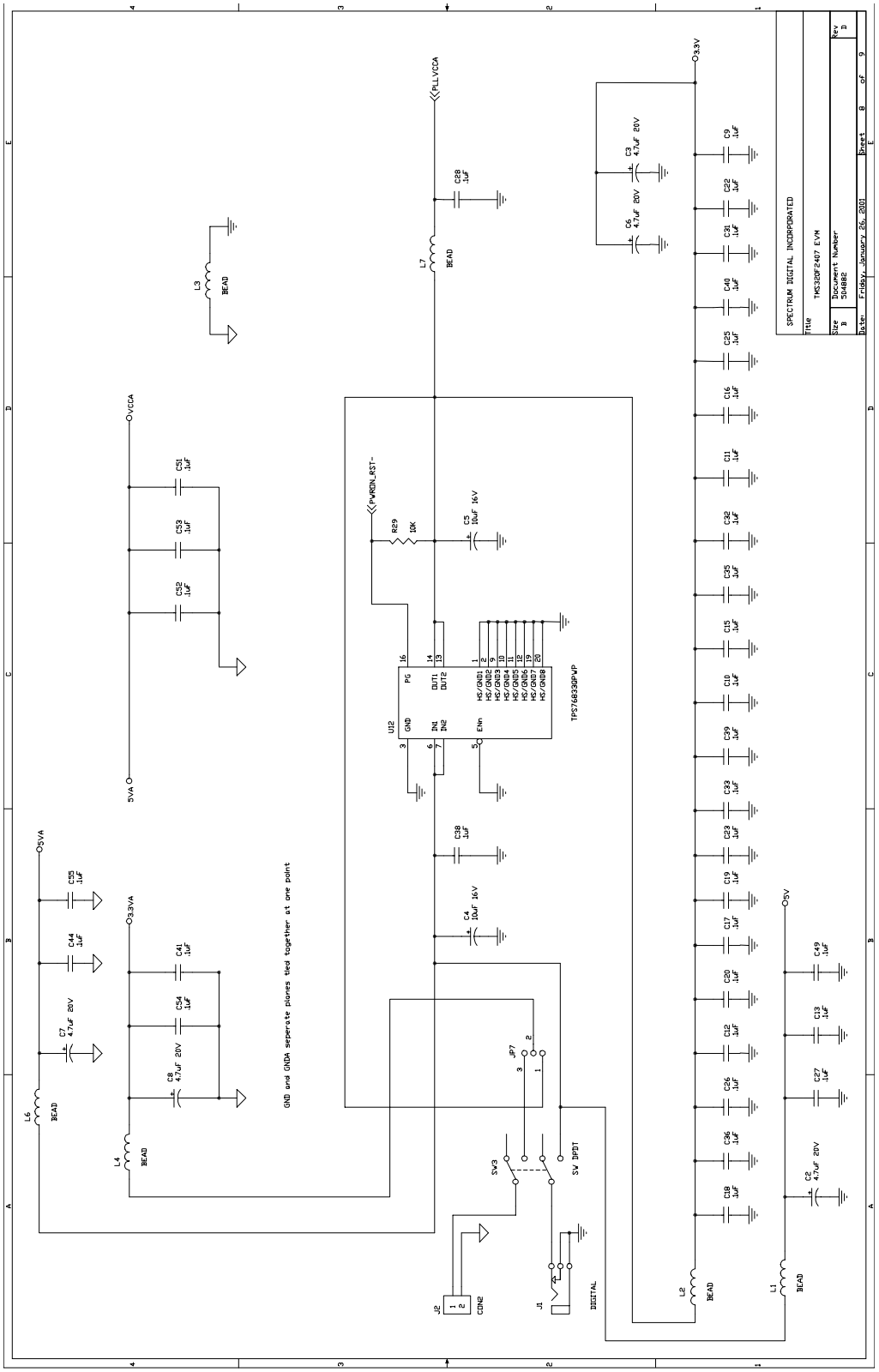
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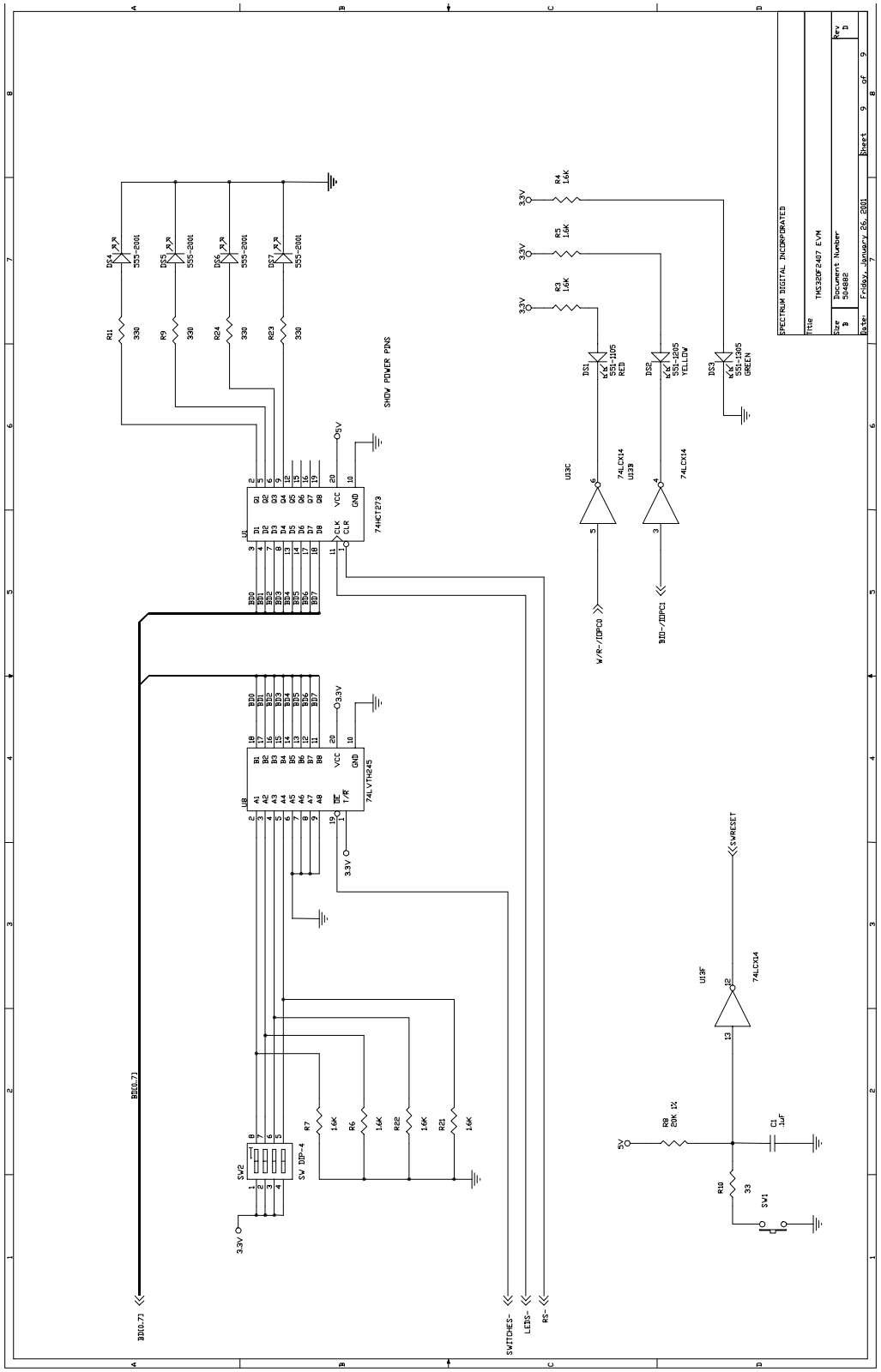
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Appendix C

DAC7625 Digital-to-Analog Converter Programming Information

This appendix contains the programming information for the DAC7625 Digital-to-Analog Converter(DAC) as it is used on the EVM320LF2407 Evaluation Module (EVM).

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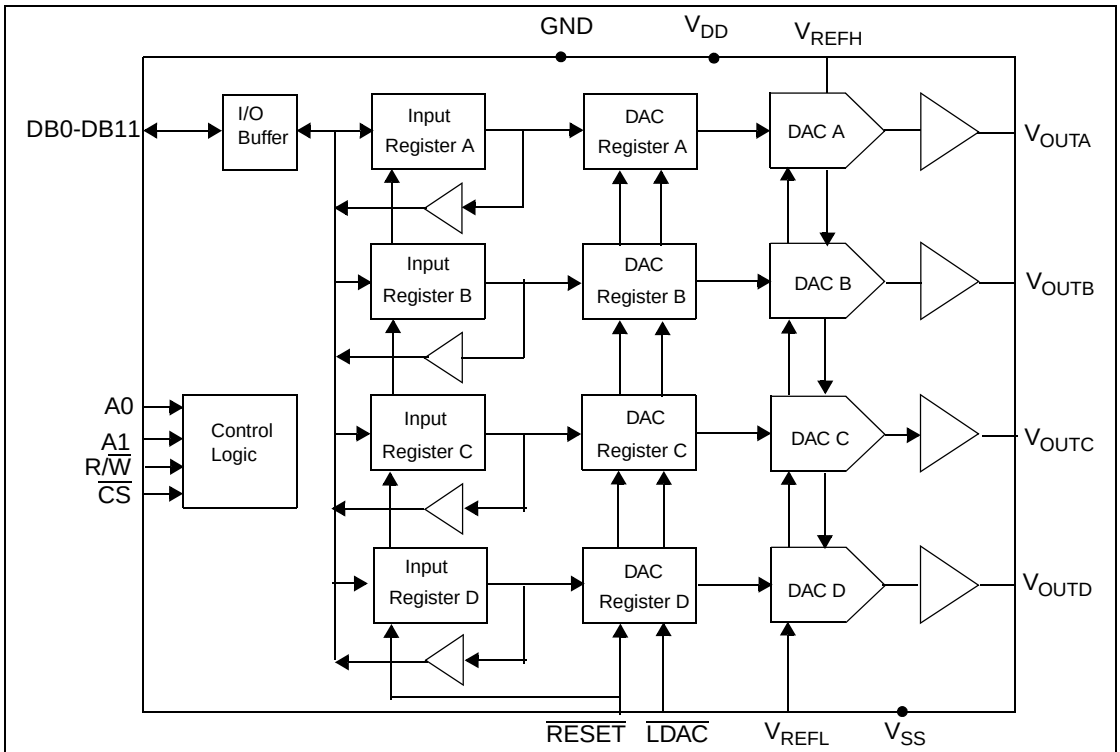
C.1 DAC7625 DIGITAL-to-ANALOG CONVERTER

The EVM320LF2407 uses a DAC7625 Digital-to-Analog Converter (DAC) manufactured by BURR-BROWN. The following sections describe the functionality of this device as it is used on the EVM320LF2407 For complete information regarding this device the user is referred to the data sheet which is available from the BURR-BROWN website at “www.burr-brown.com”.

The DAC7625 is a 4 channel, 12 bit, double buffered DAC. This means that data is written to holding registers before it is transferred to the actual converters. In this manner all four channels can be loaded separately and then converted at the same time. An asynchronous reset clears all registers to a zero-scale of 0x0000.

The main features of the DAC7625 are listed below:

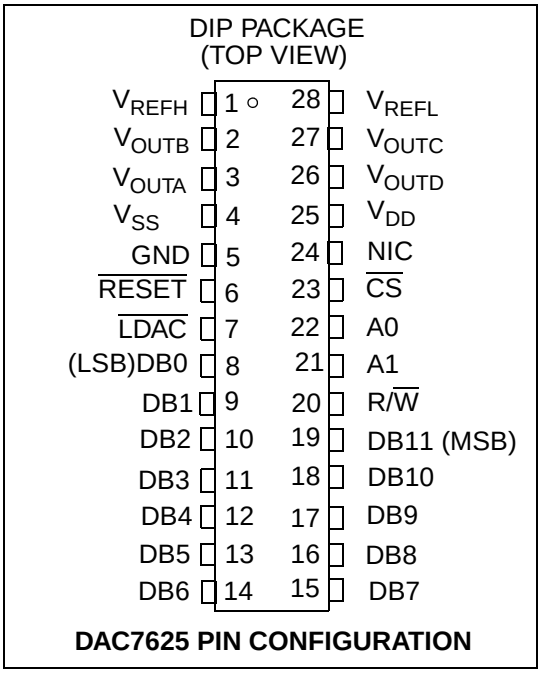
- Low Power: 20 mW
- Unipolar or Bipolar Operation
- Settling Time: 10us to 0.012%
- 12bit linearity and monotonicity: -40 to 85 degrees Centigrade
- Data readback
- double buffered data inputs



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C.2 DAC7625 Pin Configuration



DAC7625 PIN CONFIGURATION

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C.3 Pin Descriptions

Table 1: Pin Descriptions

Pin #	Pin Name	Description
1	V_{REFH}	Reference Input voltage High. Sets maximum output voltage for all DACs.
2	V_{OUTB}	DAC B Voltage Output.
3	V_{OUTA}	DAC A Voltage Output.
4	V_{SS}	Negative Analog Supply Voltage, 0 or -5V.
5	GND	Ground
6	$\overline{\text{RESET}}$	Asychronous Reset Input. Sets DAC and input registers to 0 when low.
7	$\overline{\text{LDAC}}$	Load Dac Input. All DAC registers are transparent when low.
8	DB0	Data bit 0. Least significant bit of 12 bit word.
9	DB1	Data bit 1.
10	DB2	Data bit 2
11	DB3	Data bit 3
12	DB4	Data bit 4.
13	DB5	Data bit 5.
14	DB6	Data bit 6.
15	DB7	Data bit 7.
16	DB8	Data bit 8.
17	DB9	Data bit 9.
18	DB10	Data bit 10.
19	DB11	Data bit 11. Most significant bit of 12 bit word
20	R/$\overline{\text{W}}$	Read/Write Control Input (read=high, write=low)
21	A1	Register/DAC Select (C or D=high, A or B=low)
22	A0	Register/DAC Select (B or D=high, A or C=low)
23	$\overline{\text{CS}}$	Chip Select Input
24	NIC	Not Internally Connected. Pin has no internal connection to device.
25	V_{DD}	Positive analog supply voltage, +5 V nominal
26	V_{OUTD}	DAC D Voltage Output
27	V_{OUTC}	DAC C Voltage OUtput
28	V_{REFL}	Reference Input Voltage Low. Set minimum output voltage for all DACs.

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C.4 Theory of Operation

The DAC7625 is a quad, voltage output, 12 bit digital-to-analog converter (DAC). The architecture is a classic R-2R ladder configuration followed by an operational amplifier that serves as a buffer. Each DAC has its own R-2R ladder network and output op-amp, but all share the reference voltage inputs. The minimum voltage output ("zero-scale") and maximum voltage output ("full-scale) are set by the external voltage references (V_{REFL} and V_{REFH}, respectively). The digital input is a 12-bit parallel word and the DAC input registers offer a readback capability. The converters can be powered from a single +5V or a dual $\pm$5V supply. In this application the +5 volt supply is used. The device offers a reset function which immediately sets all DAC output voltages and DAC registers to zero-scale (DAC7625, code 000_H).

C.5 Analog Outputs

When V_{ss} = -5V (dual supply operation), the output amplifier can swing to within 2.25V of the supply rail, guaranteed over the -40 C to +85 C temperature range. With V_{SS} = 0V (single-supply operation), the output can swing to ground. Note that the settling time of the output op-amp will be longer with voltages very near ground. Also, care must be taken when measuring the zero-scale error when V_{SS} = 0V. Since the output voltage cannot swing below ground, the codes (000_H, 001_H, 002_H, etc.) if the output amplifier has a negative offset.

The behavior of the output amplifier can be critical in some applications. Under short circuit conditions (DAC output shorted or ground), the output amplifier can sink a great deal more current than it can source. See the specification table for more details concerning short circuit current.

C.6 Reference Inputs

The reference inputs, V_{REFL} and V_{REFH}, can be any voltage between V_{SS}=2.25V and V_{DD}-2.25V provided that V_{REFH} is at least 1.25V greater than V_{REFL}. The minimum output of each DAC is equal to V_{REFL} plus a small offset voltage (essentially, the offset of the output op-amp). The maximum output is equal to V_{REFH} plus a similar offset voltage. Note connected to ground or must be in the range of -4.75V to -5.25V. The voltage on V_{SS} is not in one of these two configurations, the bias values may be in error and proper operation of the device is not guaranteed.

The current into the V_{REFH} input depends on the DAC output voltages and can vary from a few microamps to approximately 0.5 milliamps. The V_{REFH} source will not be required to sink current, only source it. Bypassing the reference voltage of voltages with at least a 0.1uF capacitor place as close to the DAC7625 package is strongly recommended.

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C.7 Digital Interface

Table I shows the basic control logic for the DAC7625. Note that each internal register is level triggered and not edge triggered. When the appropriate signal is LOW, the resister becomes more transparent. When the signal is returned HIGH, the digital word currently in the register is latched. The first set of registers (the Input Registers) are triggered via the A0, A1, R/$\overline{W}$, $\overline{CS}$ inputs. Only one of these registers is transparent at any given time. The second set of registers (the DAC registers) are all transparent when $\overline{LDAC}$ input is pulled low.

Each DAC can be updated independently by writing to the appropriate Input Register and then updating the DAC Register. Alternatively, the entire DAC Register set can be configured as always transparent by keeping $\overline{LDAC}$ LOW--the DAC update occurs when the Input Register is written.

The double buffer architecture is mainly designed so that each DAC Input Register can be written at any time and then all DAC voltages updated simultaneously by pulling $\overline{LDAC}$ LOW. It also allows a DAC Input Register to be synchronously changed via a trigger signal connected to $\overline{LDAC}$.

Table 2: DAC7625 Logic Truth Table

A1	A2	R/$\overline{W}$	$\overline{CS}$	$\overline{RESET}$	$\overline{LDAC}$	SELECTED	STATE OF SELECTED INPUT REGISTER	STATE OF ALL DAC REGISTERS
L	L	L	L	H	L	A	Transparent	Transparent
L	H	L	L	H	L	B	Transparent	Transparent
H	L	L	L	H	L	C	Transparent	Transparent
H	H	L	L	H	L	D	Transparent	Transparent
L	L	L	L	H	H	A	Transparent	Latched
L	H	L	L	H	H	B	Transparent	Latched
H	L	L	L	H	H	C	Transparent	Latched
H	H	L	L	H	H	D	Transparent	Latched
L	L	L	H	H	H	A	Readback	Latched
L	H	L	H	H	H	B	Readback	Latched
H	L	L	H	H	H	C	Readback	Latched
H	H	L	H	H	H	D	Readback	Latched
X	X	X	H	H	L	NONE	(All Latched)	Transparent
X	X	X	H	H	H	NONE	(All Latched)	Latched
X	X	X	X	L	X	ALL	Reset	Reset

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C.8 I/O Mapping

The DAC7625 DAC resides at addresses 0x0000-0x0004 in the I/O address space on the EVM420LF2407 These are write only locations. Locations 0x0000 - 0x0003 contain the holding registers for channels 1-4 respectively. By writing to location 0x0004 the data presently in the individual channel holding registers is transferred to the DACs for output conversion. The table below show the addresses of each channel and write strobe:

Table 3: DAC I/O Addresses

I/O Address	Channel #
0x0000	1
0x0001	2
0x0002	3
0x0003	4
0x0004	Transfer

The DAC7625 is a12 bit DAC meaning the valid values to be written are 0x0000 - 0x0fff. This DAC provides 1024 different values over a range of 0-5 volts. This means every bit causes a 0.00488 volt change.

C.9 DAC7625 Programming

The DAC can be programmed in the following manner:

1. Load channels 1-4 by writing to the respective channel holding registers (0x0000 - 0x0003). Channels do not have to be reloaded if the output value for that channel has not changed. Channels do not have to be loaded in a specific order. There is no minimum time between loading consecutive holding registers.

2. Write any value to the transfer register (0x0004). This causes data in the 4 holding registers to be transferred to the converters and output. There is no minimum time between loading a holding register and writing to the transfer register.

C.10 DAC7625 Calibration Considerations

Because of variances in electronics, the outputs of each channel should be calibrated with a scope or meter. This may narrow the actual range of the DAC because the value 0x0000 written to a channel may not actually output 0 volts. Likewise the value of 0x0fff may not output exactly 3.3 volts. The programmer should consider this in calculating or scaling values for output.

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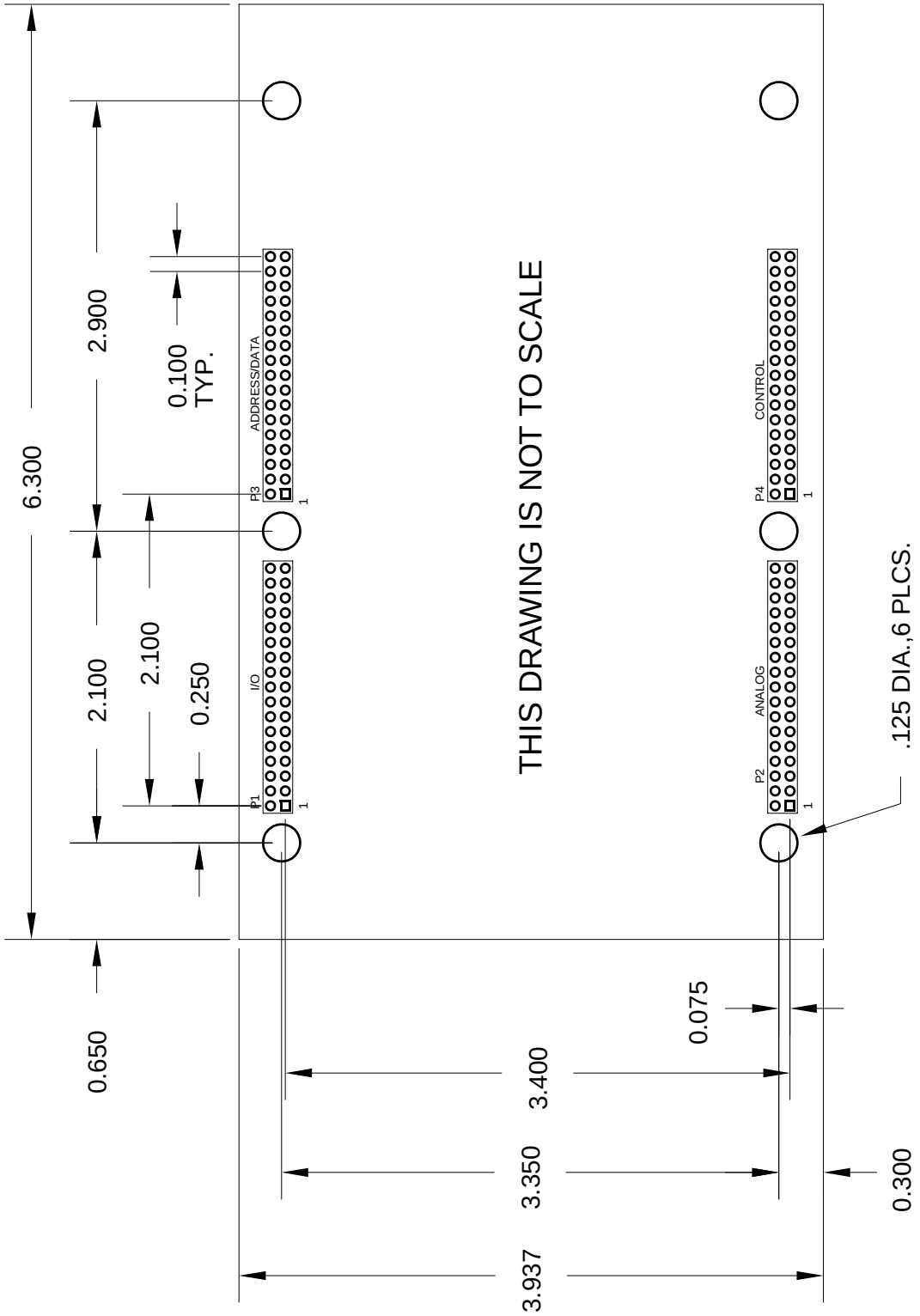
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Appendix D

EVM320 Mechanical Information

This appendix contains the mechanical information about the EVM and Wire Wrap Prototype Modules produced by Spectrum Digital.

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