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MDC40SS

Super SRAM C40
User Guide

Document Number 500-00332

Revision 1.11

January 1999

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Preface

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1 Introduction

1.1. Purpose of This Manual

This manual provides the information you need to use Spectrum's MDC40SS TMS320C40 DSP module. It describes the module's features, architecture, and specifications; and shows you how to install and configure it for your applications.

1.2. Basic MDC40SS Overview

Spectrum's MDC40SS module is a single-width TIM-40 module equipped with one TMS320C40 DSP, a 32K PEROM, and up to 8 megabytes of SRAM. It is intended as a general use, parallel processing, expansion card for applications using the 'C40 DSP.

The MDC40SS module is available in a variety of memory and processor speed configurations. These configurations are summarized in Table 1.

Table 1 MDC40SS Configurations

Model	Process Speed	RAM Size
MDC40SS5-50	50 MHz	4 MB
MDC40SS6-50	50 MHz	8 MB
MDC40SS2-60	60 MHz	1.5 MB
MDC40SS4-60	60 MHz	2 MB
MDC40SS5-60	60 MHz	4 MB
MDC40SS6-60	60 MHz	8 MB

1.3. Feature Summary

- Single-width TIM-40 module
- One TMS320C40 DSP (Refer to the *TMS320C4x User's Guide* for details)
- One 32K PEROM for ID information and/or boot-loading the 'C40
- Up to two banks of 0.5 MB or 2 MB local bus SRAM, depending upon configuration
- Up to two banks of 0.5 MB or 2 MB global bus SRAM, depending upon configuration
- Global bus connector
- 50 MHz or 60 MHz processor speed, depending upon configuration
- Six communication ports available from the 'C40 via the TIM-40 connectors

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1.4. TIM-40 Module Specification

The MDC40SS is a single-width TIM-40 module with three 80-pin connectors. The TIM-40 standard provides physical, electrical interface, and system characteristics for module development. Modules are installed on TIM-40 carrier boards which connect the modules to each other and to the host system. Spectrum offers a variety of TIM-40 carrier boards for use in PCI, PC-ISA, VMEbus, VXI, and other host systems.

For more information about the TIM-40 module, refer to the TIM-40 TMS320C4x Module Specification Version 1.01 available from Texas Instruments.

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2 Installation

2.1. Setting the Module's Switches

Several MDC40SS features are configured through switches. Configure the features according to the following sections, using the information provided in Figure 1 and Table 2 for reference.

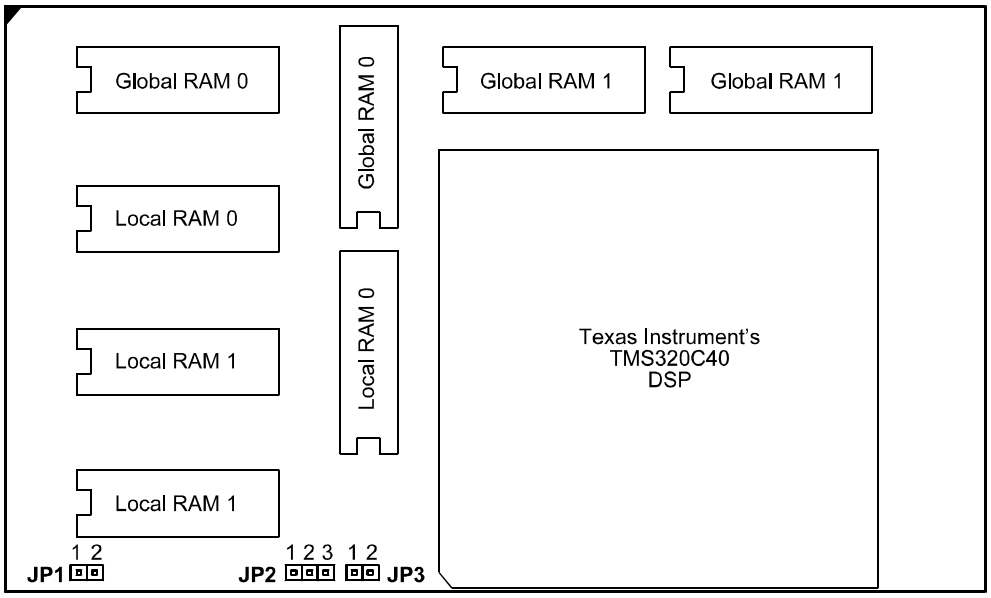


Figure 1 Board Layout and Jumper Locations

Table 2 Jumper Settings

Jumper	Pins	Function
JP1	OUT*	Boot data from first active communication port (IIOF2 = high)
	IN	Boot data from PEROM at address 0x4000 0000 (IIOF2 = low)
JP2	1-2	Use external clock signal
	2-3*	Use internal clock
JP3	OUT	Disable Global RAM
	IN*	Enable Global RAM

* Default values

2.1.1. Boot Data Source

Upon power up or reset, the 'C40 DSP must load its boot program into memory. The source of this data will either be the on-board PEROM or a communication port

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depending upon jumper JP1. When set to boot from its PEROM, the IIOF2 interrupt line is pulled low which causes the ‘C40 to start loading from address 0x4000 0000. When set to boot from a communication port, IIOF2 is pulled high which causes the ‘C40 to load data from the first TIM-40 communication port that it sees active.

- Set JP1 to select the boot data source as either the on-board PEROM or to the first active communication port.

2.1.2. Clock Source

The module’s clock signal can be taken from its own internal oscillator or an external source via the CLKIN line on the TIM-40 connector, depending upon jumper JP2.

- Set JP2 to select the internal or an external clock source.

2.1.3. Global RAM Enable

The SRAM banks on the global memory bus can be disabled by jumper JP3. This allows the carrier board to map the module’s global RAM address space to other memory devices if required.

- Set JP3 to either enable or disable the Global SRAM.

2.2. Installing the module on to the Carrier Board

1. Locate the TIM-40 site on the carrier board in which the module will be installed.

2. Align the module over its TIM-40 site on the carrier board so that the triangle printed on the top right corner of the module PCB is adjacent to the Top Primary Connector of the carrier board.

3. Ensure that the connectors are properly aligned and gently push the module on to the connectors. Be careful to apply pressure over the connectors to prevent the board from bending and causing connector pin damage.

4. Fasten the module to the carrier board with the spacers provided with the module. There are two holes for these spacers at diagonal corners of the TIM-40 site. Screw the spacers between the module and the carrier board at these two holes.

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3 Module Architecture

The single-width MDC40SS TIM-40 module hosts one TMS320C40 digital signal processor (DSP) with a 32K PEROM and up to four banks of SRAM. The general architecture of the module is shown in Figure 2.

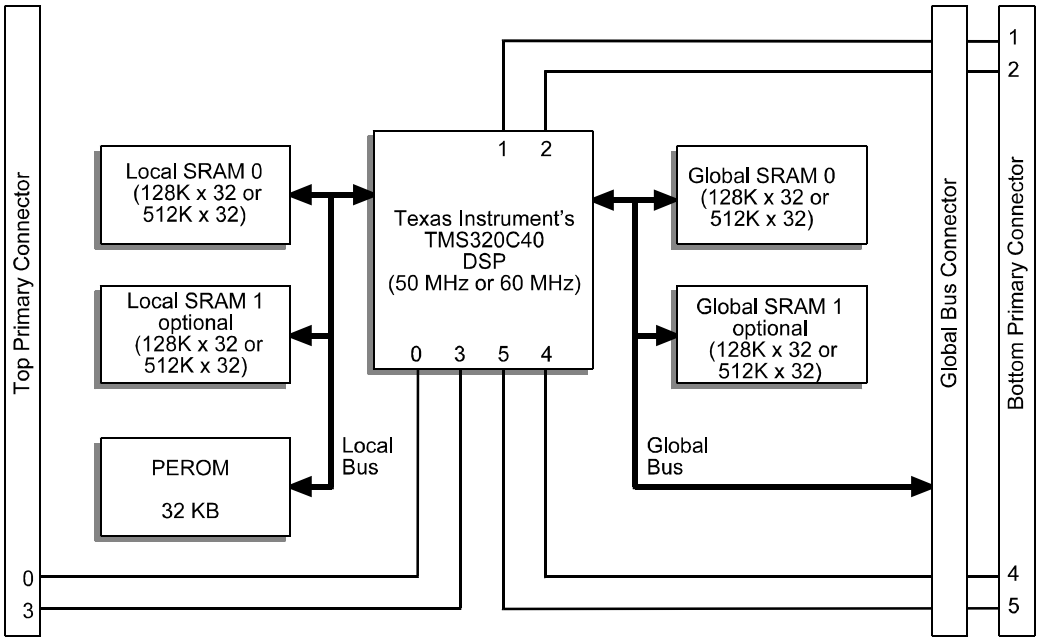


Figure 2 Block Diagram

3.1. Digital Signal Processor

The TMS320C40 DSP (‘C40) has six 20 Mbps parallel communication ports, a local and global memory bus, and a set of interrupt and control lines. Complete information on the C44 can be found in Texas Instrument’s TMS320C44 User Guide.

An on-board clock circuit provides the clock signal for the module, but can be disconnected via a jumper to allow an external clock source to be used.

Communication ports from the ‘C40 are assigned directly to the corresponding ports on the top and bottom TIM-40 connectors.

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3.2. Optimizing DSP Performance

The *TMS320C4x User's Guide* provides several suggestions for optimizing performance:

- Enable the 'C40's internal instruction cache. Refer to *TMS320C4x Parallel Runtime Support Library User's Guide.*
- Use the DMA to transfer data in memory instead of the CPU. Refer to *TMS320C4x Parallel Runtime Support Library User's Guide.*
- Isolate code and data on separate busses (global and local). Refer to the *TMS320 Floating-Point DSP Assembly Language Tools User's Guide.*
- Place time-critical code and data into the 2 internal memory banks. Refer to the *TMS320 Floating-Point DSP Assembly Language Tools User's Guide.*

3.3. Memory Interface

Local memory is addressed from 0x0000 0000 to 0x7FFF FFFF, and global memory from 0x8000 0000 to 0xFFFF FFFF. Memory interface registers in the local address bus configure the busses for wait states, page size, and strobe line activation. Complete details about the 'C40 busses and the their interface control registers can be found in Chapter 7 of the *TMS320C4x User's Guide*.

The following table shows the memory devices and I/O functions located on the local and global busses of the 'C40.

Local Bus	Global Bus
• Internal Boot Loader ROM	• Global SRAM bank 0
• Internal Peripherals	• Global SRAM bank 1
• Local SRAM Bank 0	• Global Expansion Bus
• Local SRAM Bank 1	
• PEROM	

The global and local memory address busses each have two banks of memory. On the board itself, each bank consists of four memory devices. Not all memory banks may be populated; this is determined by the MDC40SS configuration. Table 3 shows which banks are used for the different configurations of the MDC40SS.

Table 3 MDC40SS Memory Bank Configurations

Model	'C40 Speed	Total RAM	Local Bank 1	Local Bank 2	Global Bank 1	Global Bank 2
MDC40SS5-50	50 MHz	4 MB	512x32	empty	512x32	empty
MDC40SS6-50	50 MHz	8 MB	512x32	512x32	512x32	512x32
MDC40SS2-60	60 MHz	1.5 MB	128x32	128x32	128x32	empty
MDC40SS4-60	60 MHz	2 MB	128x32	128x32	128x32	128x32
MDC40SS5-60	60 MHz	4 MB	512x32	empty	512x32	empty
MDC40SS6-60	60 MHz	8 MB	512x32	512x32	512x32	512x32

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3.3.1. Memory Maps

Each configuration of the MDC40SS has a slightly different memory map due to the different memory sizes. The following figures show the memory maps for the four MDC40SS configurations. In addition to addressing, the memory maps also show the number of wait states and strobe lines used for each address range assignment.

	Address Range	Description	Wait States	Strobe
Local Bus	0x0000 0000 - 0x0000 0FFF	Boot Loader ROM (Internal)	0	-
	0x0000 1000 - 0x000F FFFF	RESERVED	0	-
	0x0010 0000 - 0x0010 00FF	Peripherals (Internal)	-	-
	0x0010 0100 - 0x002F F7FF	RESERVED		
	0x002F F800 - 0x002F FBFF	1 K RAM Block 0	0	-
	0x002F FC00 - 0x002F FFFF	1 K RAM Block 1	0	-
	0x0030 0000 - 0x0031 FFFF	External Local SRAM Bank 0 (128k x 32)	0	LSTRB0
	0x0032 0000 - 0x0033 FFFF	External Local SRAM Bank 1 (128k x 32)	0	LSTRB0
	0x0034 0000 - 0x3FFF FFFF	RESERVED	-	
	0x4000 0000 - 0x4000 7FFF	PEROM (32k x 8) BOOT CODE LOCATION	4 (5 write)	LSTRB1 normal reads LSTRB0 boot-up reads LSTRB0 for PEROM write
	0x4000 8000 - 0x6FFF FFFF	RESERVED	-	
	0x7000 0000 - 0x7000 7FFF	ID ROM	4 (5 write)	LSTRB1 normal reads LSTRB0 boot-up reads LSTRB0 for PEROM write
	0x7000 8000 - 0x7FFF FFFF	RESERVED	-	
Global Bus	0x8000 0000 - 0x8001 FFFF	Global SRAM Bank 0 (128k × 32)	0	STRB0
	0x8002 0000 - 0xFFFF FFFF	Global Bus Expansion	-	STRB1

Figure 3 MDC40SS2-60 Memory Map

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	Address Range	Description	Wait States	Strobe
Local Bus	0x0000 0000 - 0x0000 0FFF	Boot Loader ROM (Internal)	0	-
	0x0000 1000 - 0x000F FFFF	RESERVED	0	-
	0x0010 0000 - 0x0010 00FF	Peripherals (Internal)	-	-
	0x0010 0100 - 0x002F F7FF	RESERVED		
	0x002F F800 - 0x002F FBFF	1 K RAM Block 0	0	-
	0x002F FC00 - 0x002F FFFF	1 K RAM Block 1	0	-
	0x0030 0000 - 0x0031 FFFF	External Local SRAM Bank 0 (128k x 32)	0	LSTRB0
	0x0032 0000 - 0x0033 FFFF	External Local SRAM Bank 1 (128k x 32)	0	LSTRB0
	0x0034 0000 - 0x3FFF FFFF	RESERVED	-	
	0x4000 0000 - 0x4000 7FFF	PEROM (32k x 8) BOOT CODE LOCATION	4 (5 write)	LSTRB1 normal reads LSTRB0 boot-up reads LSTRB0 for PEROM write
	0x4000 8000 - 0x6FFF FFFF	RESERVED	-	
	0x7000 0000 - 0x7000 7FFF	ID ROM	4 (5 write)	LSTRB1 normal reads LSTRB0 boot-up reads LSTRB0 for PEROM write
	0x7000 8000 - 0x7FFF FFFF	RESERVED	-	
Global Bus	0x8000 0000 - 0x8001 FFFF	Global SRAM Bank 0 (128k × 32)	0	STRB0
	0x8002 0000 - 0x8003 FFFF	Global SRAM Bank 1 (128k × 32)	0	STRB0
	0x8004 0000 - 0xFFFF FFFF	Global Bus Expansion	-	STRB1

Figure 4 MDC40SS4-60 Memory Map

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	Address Range	Description	Wait States	Strobe
Local Bus	0x0000 0000 - 0x0000 0FFF	Boot Loader ROM (Internal)	0	-
	0x0000 1000 - 0x000F FFFF	RESERVED	0	-
	0x0010 0000 - 0x0010 00FF	Peripherals (Internal)	-	-
	0x0010 0100 - 0x002F F7FF	RESERVED		
	0x002F F800 - 0x002F FBFF	1 K RAM Block 0	0	-
	0x002F FC00 - 0x002F FFFF	1 K RAM Block 1	0	-
	0x0030 0000 - 0x0037 FFFF	External Local SRAM Bank 0 (512k x 32)	0	LSTRB0
	0x0038 0000 - 0x3FFF FFFF	RESERVED	-	
	0x4000 0000 - 0x4000 7FFF	PEROM (32k x 8) BOOT CODE LOCATION	4 (5 write)	LSTRB1 normal reads LSTRB0 boot-up reads LSTRB0 for PEROM write
	0x4000 8000 - 0x6FFF FFFF	RESERVED	-	
	0x7000 0000 - 0x7000 7FFF	ID ROM	4 (5 write)	LSTRB1 normal reads LSTRB0 boot-up reads LSTRB0 for PEROM write
	0x7000 8000 - 0x7FFF FFFF	RESERVED	-	
Global Bus	0x8000 0000 - 0x8007 FFFF	Global SRAM Bank 0 (512k × 32)	0	STRB0
	0x8008 0000 - 0xFFFF FFFF	Global Bus Expansion	-	STRB1

Figure 5 MDC40SS5-50/60 Memory Map

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	Address Range	Description	Wait States	Strobe
Local Bus	0x0000 0000 - 0x0000 0FFF	Boot Loader ROM (Internal)	0	-
	0x0000 1000 - 0x000F FFFF	RESERVED	0	-
	0x0010 0000 - 0x0010 00FF	Peripherals (Internal)	-	-
	0x0010 0100 - 0x002F F7FF	RESERVED		
	0x002F F800 - 0x002F FBFF	1 K RAM Block 0	0	-
	0x002F FC00 - 0x002F FFFF	1 K RAM Block 1	0	-
	0x0030 0000 - 0x0037 FFFF	External Local SRAM Bank 0 (512k x 32)	0	LSTRB0
	0x0038 0000 - 0x003F FFFF	External Local SRAM Bank 1 (512k x 32)	0	LSTRB0
	0x0040 0000 - 0x3FFF FFFF	RESERVED	-	
	0x4000 0000 - 0x4000 7FFF	PEROM (32k x 8) BOOT CODE LOCATION	4 (5 write)	LSTRB1 normal reads LSTRB0 boot-up reads LSTRB0 for PEROM write
	0x4000 8000 - 0x6FFF FFFF	RESERVED	-	
	0x7000 0000 - 0x7000 7FFF	ID ROM	4 (5 write)	LSTRB1 normal reads LSTRB0 boot-up reads LSTRB0 for PEROM write
	0x7000 8000 - 0x7FFF FFFF	RESERVED	-	
Global Bus	0x8000 0000 - 0x8007 FFFF	Global SRAM Bank 0 (512k × 32)	0	STRB0
	0x8008 0000 - 0x800F FFFF	Global SRAM Bank 1 (512k x 32)	0	STRB0
	0x8010 0000 - 0xFFFF FFFF	Global Bus Expansion	-	STRB1

Figure 6 MDC40SS6-50/60 Memory Map

3.3.2. Local and Global Memory Interface Control Registers

To configure the local and global busses with the correct page size, wait states, strobe lines and other parameters, control word values must be written to the global and to the local memory interface control registers. These values are determined by the MDC40SS configuration and, for the local bus, whether the PEROM is being programmed.

These registers are accessed on the local bus. The Local Memory Interface Control Register (LMICR) address is 0x0010 0004h and the Global Memory Interface Control Register (GMICR) address is 0x0010 0000h.

Although the register values can be derived from the information given by the memory maps using the instructions in the *TMS320C4x User's Guide*, they are provided in hexadecimal form in Table 4.

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Table 4 Memory Interface Control Register Values

Model	Local (LMICR) Value	Global (GMICR) Value
Register Address	*0x0010 0004h*	*0x0010 0000h*
MDC40SS5-50 (50 MHz 4MB)	0x3DEC A050	0x324C 8010
MDC40SS6-50 (50 MHz 8MB)	0x3DEC A050	0x334C 8010
MDC40SS2-60 (60 MHz 1.5MB)	0x3DEC 2050	0x304C 8010
MDC40SS4-60 (60 MHz 2MB)	0x3DEC 2050	0x314C 0010
MDC40SS5-60 (60 MHz 4MB)	0x3DEC A050	0x324C 8010
MDC40SS6-60 (60 MHz 8MB)	0x3DEC A050	0x334C 8010
When programming the PEROM	0x3EEB 8550	n.a.

The Local Memory Interface Control Register (LMICR) value used when programming the PEROM is given for information only. The PEROM Utility program used when programming the PEROM loads the correct control word into the LMICR.

The GMICR values can vary depending upon which carrier board the MDC40SS module is installed on. The GMICR parameters relating to /STRB1 must be changed to reflect the settings defined by the carrier board.

The listed GMICR values assume the following:

- The /STRB1 (the strobe signal which can be used to access carrier board addresses) has wait states generated solely by the external /RDY line.
- The /STRB1 uses a page size of 1K (of 32 bit words).
- The STRB SWITCH is active.

Refer to section 7.2 of the *TMS320C4x User's Guide* for complete information to determine GMICR values.

3.4. Interrupts

The four IIOF lines on the MDC40SS module are configured according to the TIM-40 specifications. IIOF0, IIOF1, and IIOF2 go off-module to the carrier board. IIOF3 is used to generate the /CONFIG signal,which goes off-module to the carrier board. Upon reset, the state of the four IIOF lines determines the source of boot code.

3.5. 32K PEROM

The 32K PEROM is programmed as an ID ROM according to the TIM-40 specifications. It can, however, be reprogrammed with user code using the DB40 debugger and the PEROM Utility programs included in the MDC40SS Developer's Kit software. Instructions on programming the PEROMs used on Spectrum TIM-40 modules can be found in the PEROM Utility Guide.

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The Atmel AT29C256 Flash Programmable and Erasable Read Only Memory (PEROM) is used as the PEROM device. It is an 8-bit wide device using data bits LD0 to LD7 and occupying addresses 0x4000 0000 to 0x4000 7FFF on the local bus, and is also aliased from 0x7000 0000 to 0x7000 7FFF for IDROM accesses.

3.6. JTAG Emulation Interface

The TMS320C40 integrates the IEEE 1149.1 JTAG interface for test, emulation, and programming the 32K PEROM.

3.7. Communication Ports

The TIM-40 specification defines six parallel communication ports for a single-width module. The MDC40SS maps each of these ports to the corresponding port on the ‘C40 as shown in the block diagram of Figure 2.

3.8. Power Up and Reset

After power up, the ‘C40 is reset by the carrier board and runs the boot loader program from its internal ROM. The boot loader takes source program data from either the 8-bit PEROM at address 0x4000 0000 or from the first communication port to go active. This source of boot data is jumper configurable as described in the Installation chapter.

If the PEROM is used to bootstrap the DSP, it cannot be used as an ID ROM and vice versa. The boards are shipped with PEROM programmed to be the ID ROM. Refer to the TIM-40 specification for more information regarding the ID ROM.

The source program data specifies the width of the memory device, values for the local and global memory interface control registers, pointers to the interrupt and trap vector tables, as well as blocks of program data. Refer to the *TMS320C4x User’s Guide* for details.

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4 Specifications

4.1. Functional Specifications

Model	MDC40SS2-60	MDC40SS4-60	MDC40SS5-60	MDC40SS6-60	MDC40SS5-50	MDC40SS6-50
DSP	TMS320C40	TMS320C40	TMS320C40	TMS320C40	TMS320C40	TMS320C40
Clock Speed	60 MHz	60 MHz	60 MHz	60 MHz	50 MHz	50 MHz
RAM	1.5 MB	2 MB	4 MB	8 MB	4 MB	8 MB
PEROM	32 kB	32 kB	32 kB	32 kB	32 kB	32 kB
MFLOPS	60	60	60	60	50	50

4.2. Electrical Specifications

Supply Voltage (50 MHz) +5.0V ± 5% at no more than 900 mA typical operating current

Supply Voltage (60 MHz) +5.0V ± 5% at no more than 600 mA typical operating current

4.3. Mechanical Specifications

Single-width TIM-40 module.

Length 4.2” (106.7 mm)

Width 2.5” (64.2 mm)

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Component and mated connector height limits:

Top	0.210” (5.33 mm)
Bottom:	0.150” (3.81 mm)

4.4. Environmental Specifications

Operating Temperature with Forced Air	0 to 50° C (exhaust air temperature from DSP)
Storage Temperature:	-25 to 80° C
Operational Humidity:	10% to 80% non-condensing

4.5. TIM-40 Interface Connectors

Two 80-pin Hirose Electric FX-4 TIM-40 connectors provide the interface between the module and the carrier board according to Texas Instruments TIM-40 TMS320C4x Module Specification Version 1.01. Table 5 shows how the different functions on the TIM-40 connectors are assigned to the MDC40SS.

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Table 5 TIM-40 Interface Function Assignment

TIM-40 Interface Function	Assignment
Communication Port 0	‘C40 Port 0
Communication Port 1	‘C40 Port 1
Communication Port 2	‘C40 Port 2
Communication Port 3	‘C40 Port 3
Communication Port 4	‘C40 Port 4
Communication Port 5	‘C40 Port 5
JTAG	Supported
Reset	Supported
IIOF0	‘C40 IIOF0 Interrupt
IIOF1	‘C40 IIOF1 Interrupt
IIOF2	‘C40 IIOF2 Interrupt
IACK	‘C40 IACK
NMI	‘C40 NMI
CONFIG	Generated by IIOF3
TCLK0	‘C40 TCLK0
TCLK1	‘C40 TCLK1
Clock Output H1	‘C40 H1
Clock Output H3	‘C40 H3
User Defined Pins	NC
Power (+5 V)	700 mA typical
Power (+12 V)	NC
Power (-12 V)	NC

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